Video Frame Buffer Controller v1.0

Introduction

The Xilinx® Video Frame Buffer Controller (VFBC) core is a fully functional VHDL design implemented on a Xilinx FPGA. The VFBC connects to the Multi-Port Memory Controller (MPMC) Native Port Interface (NPI) as a Port Interface Module (PIM) and allows user IP to read and write data in two-dimensional sets regardless of the size or the organization of external memory transactions.

Features

- 2D Data Transfers with sizes of 32, 767 Bytes x 16, 777, 216 Lines Maximum, one 32-bit Word Minimum.
- Asynchronous FIFO Command/Control Interface.
- Separate asynchronous FIFO Write and Read Data Interfaces
- Connects to the MPMC via the NPI
- Supports NPI burst size of 8-word or 32-word bursts
- Configurable NPI data width of 32 or 64
- Independently configurable write and read data widths of 8, 16, 32, or 64-bits
- Configurable FIFO Depths.
- Configurable Almost Full/Empty Flags.
- Independent Write, Read, and Command FIFO Resets
- Data FIFOs Flushable.
- Byte-Enables available for Write Data Interface

Applications

The Video Frame Buffer Controller core can be utilized in video applications where hardware control of 2D data is needed to achieve real time operation. Typical video applications are Motion Estimation, Video Scaling, On Screen Displays, and Video Capture used in video surveillance, video conferencing, and video broadcast.

LogiCORE™ Facts Core Specifics		
Supported Device Families		Virtex™-5, Virtex-4, Spartan™-3A DSP
Resources Used		
Virtex-5	32-Bit NPI	1484 LUTs, 938 FFs, 3 RAMB36s
	64-Bit NPI	1642 LUTs, 1034 FFs, 5 RAMB36s
Virtex-4	32-Bit NPI	2257 LUTs, 961 FFs, 3 RAMB16s
	64-Bit NPI	2356 LUTs, 1056 FFs, 5 RAMB16s
Spartan-3A DSP	32-Bit NPI	2254 LUTs, 960 FFs, 3 RAMB16BWEs
	64-Bit NPI	2351 LUTs, 1054 FFs, 5 RAMB16BWEs
Provided with Core		
Documentation		Data Sheet, User Guide
Design File Formats		VHDL, EDIF
Constraints		UCF
Verification		VHDL Test Bench
Instantiation Template		VHDL Wrapper
Design Tool Requirements		
Synthesis		Xilinx XST 9.2.03i
Xilinx Implementation Tools		Xilinx ISE™ 9.2.03i
Support		
Support provided by Xilinx support at: www.xilinx.com/support		

Functional Description

The VFBC is designed to be the connection layer between video clients and the MPMC external memory controller. The VFBC provides key features not provided by a generic memory controller to address the typical video system's inherently heterogeneous nature, which includes asynchronous interfaces, a mixture of data widths, long data bursts (or streaming), and 2D data transfers. The VFBC is designed to efficiently work in conjunction with the MPMC as a Port Interface Module (PIM). It can easily be used with existing MPMC systems by connecting to the Native Port Interface (NPI) of the MPMC. See Figure 1.

The VFBC also includes one independent Asynchronous FIFO interface for command input, write data input, and read data output. This FIFO interface design is useful to decouple the video IP from the Memory Clock Domain. The following diagram shows the VFBC interfaces. Each interface is discussed in more detail below.

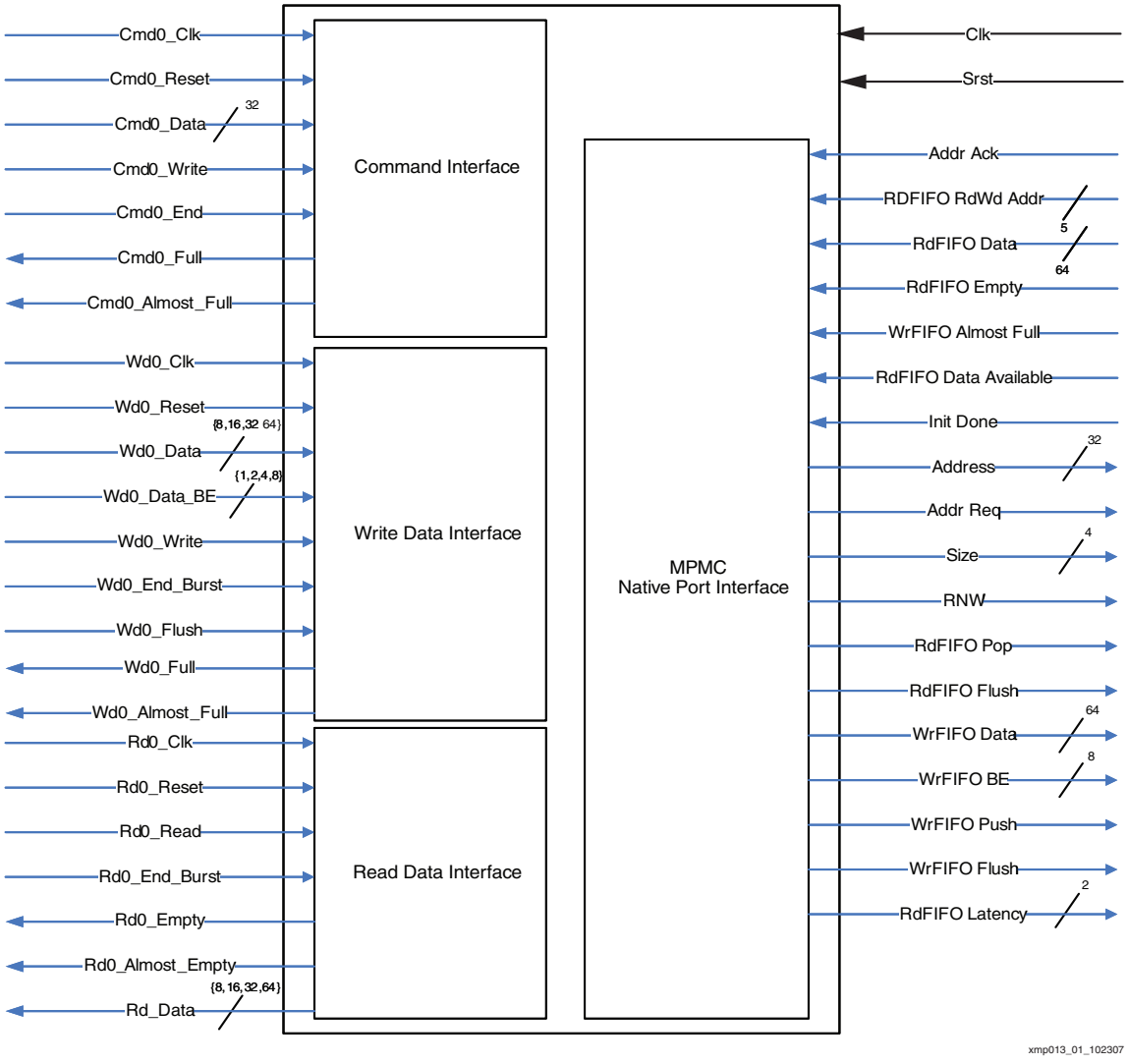

Figure 1: **VFBC Interfaces**

The data transfers to/from the VFBC data FIFOs are controlled by the Command Interface. Commands are written into the Command Interface FIFO in four 32-bit Word Packets. This 4-word packet controls the direction (Read or Write) and the 2D size of the transfer. It includes the following information: Start Address of the 2D transfer, X Size in Bytes, Y Size in Lines, and Width of the Video Frame (Stride).

The VFBC divides each 2D transfer into small 8-word or 32-word transfers that the MPMC utilizes. Figure 2 shows a video frame stored linearly in external memory, which contains a rectangular region of interest to be transferred by the VFBC. This 2D data transfer is divided into smaller 8-word bursts.

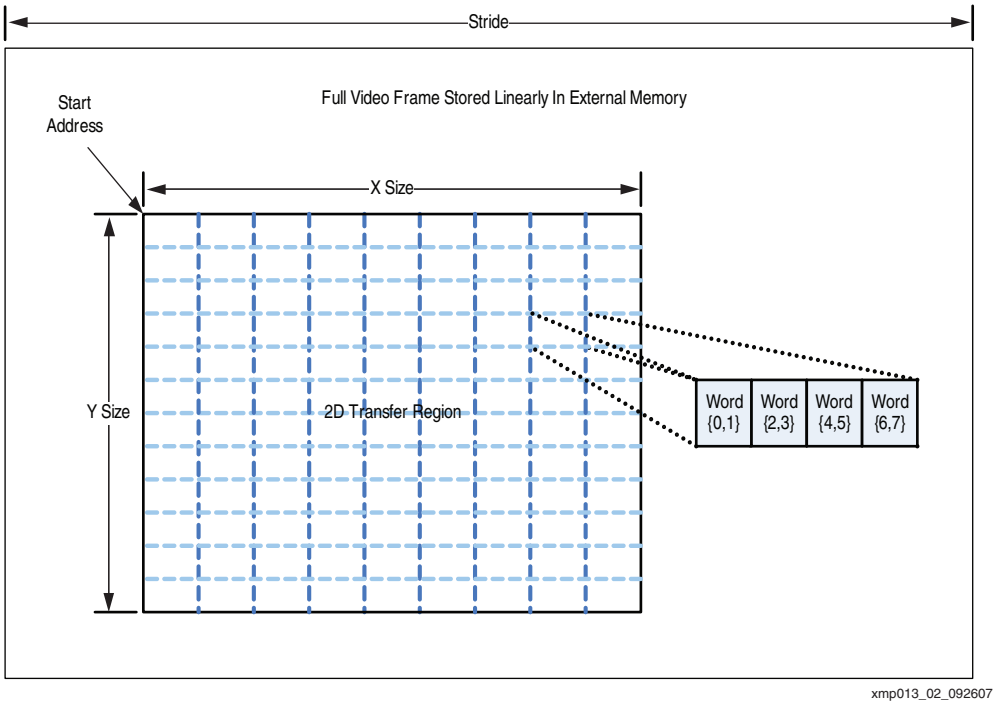

Figure 2: **2D Transfers**

Command Interface

The Command Interface can be implemented as either an Asynchronous or a Synchronous FIFO. The commands are written into the Command Interface FIFO in four 32-bit Word Packets. Each command packet word is pushed onto the Command FIFO during the clock cycle that the Cmd0_Write signal is active. The command words do not have to be written in consecutive clock cycles. Commands are acted upon by the VFBC after the last command word is written. The Command Packets can be written at the same time as data transfers to the Data Interface FIFOs. The 4-Word Command Packet is shown in Table 1.

Table 1: **Command Packet Structure**

Command Packet								
Command Word 0			Command Word 1		Command Word 2		Command Word 3	
[31:24] Port ID	[23:15] Reserved	[14:0] X Size	[31] WNR	[30:0] Start Address	[31:24] Reserved	[23:0] Y Size	[31:24] Reserved	[23:0] Stride

The first word includes the Port ID and the X Size of the transfer. Bits [31:24] are the Port_ID of the write and read data interfaces. Valid values are 0, 1, 2, or 3. Bits [14:0] are the X_Size, which is the number of consecutive linear bytes of the transaction per line (shown in Table 1).

The second word includes the Direction of the transfer and the Start Address. Bit [31] is the Write_NotRead bit. The Write_NotRead bit denotes a write transaction if High and a read transaction if Low. Bits [30:0] are the physical Memory Byte Start Address. This is the start address of the transfer (shown in Figure 2).

The third word includes the Y Size of the transfer. Bits [23:0] are the Y_Size. The Y_Size is the number of lines of the transfer minus 1. Figure 2 shows the Y_Size as 12 lines. The value set in bits [23:0] should be 0x00000b for this transfer.

The fourth word includes the Stride of the transfer. Bits [23:0] are the Stride. The Stride is the number of bytes to skip between the beginning of each line of the transfer. This is the line length (in bytes) of the 2D storage in external memory.

Write Data Interface

The Write Data Interface can be implemented as either an Asynchronous or a Synchronous FIFO. Its depth and data width are configurable. A configurable almost full flag is also provided. The data width can be configured as 8, 16, 32, or 64-bits. Data is pushed onto the FIFO during the same clock cycle as the Wd0_Write signal is active. The Wd0_Flush signal is used to flush all data currently in the FIFO but keep the current Write Command active. The Wd0_Reset signal is used to flush all data in the FIFO and flush the Write Command from the Command FIFO. The Wd0_End_Burst signal is used only when the transfer is not a multiple of the burst size. If the transfer ends on a non 8-word or 32-word boundary, this signal must be asserted High during the last word transferred.

Read Data Interface

The Read Data Interface can be implemented as an Asynchronous or a Synchronous FIFO. Its depth and data width are configurable. A configurable almost empty flag is also provided. The data width can be configured as 8, 16, 32, or 64-bits. Data is popped off of the FIFO during the same clock cycle as the Rd0_Read signal is active. The Rd0_Flush signal is used to flush all data currently in the FIFO but keep the current Read Command active. The Rd0_Reset signal is used to flush all data in the FIFO and flush the Read Command from the Command FIFO. The Rd0_End_Burst signal is used only when the transfer is not a multiple of the burst size. If the transfer ends on a non 8-word or 32-word boundary, this signal must be asserted High during the last word transferred.

MPMC NPI Interface

See the *MPMC User Guide* regarding the Native Port Interface, which can be found at the following location: **www.xilinx.com/esp/wired/optical/xlnx_net/mpmc2/ug253.pdf**.

Performance

The target clock maximum frequencies are summarized in Table 2.

Table 2: **Target Clock Maximum Frequencies**

FPGA Family	Clock F_{Max}	Notes
Spartan-3A DSP	133 MHz	With FIFO depths of 1024 32-bit words or less.
Virtex-4	167 MHz	With FIFO depths of 1024 32-bit words or less.
Virtex-5	200 MHz	With FIFO depths of 1024 32-bit words or less.

Ordering Information

The Video Frame Buffer Controller (VFBC) reference design is provided under the terms of the Design License Agreement. The VFBC design is included at no additional charge with the Spartan-3A DSP FPGA Video Starter Kit. Additional information on the Video Starter Kit and reference designs can be found at the following location:

www.xilinx.com/products/devboards/reference_design/vsk_s3.htm.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/29/07	1.0	Initial Xilinx release.

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