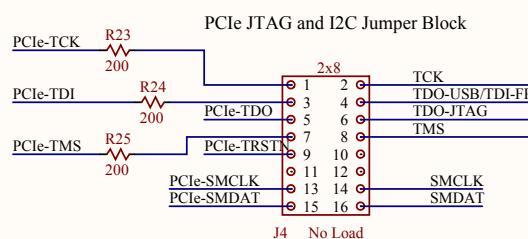
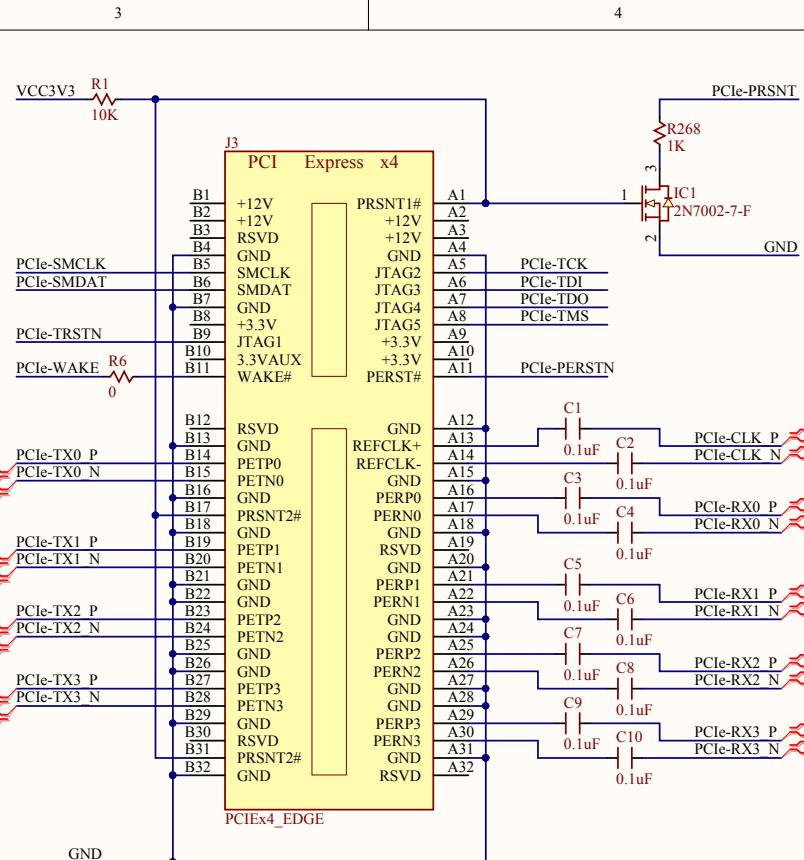
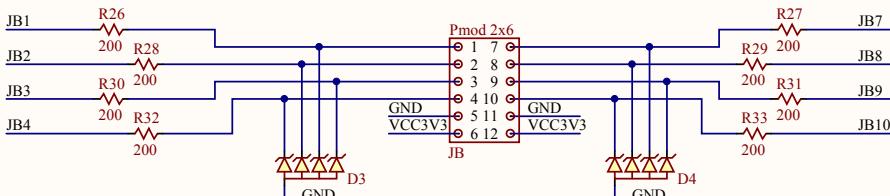
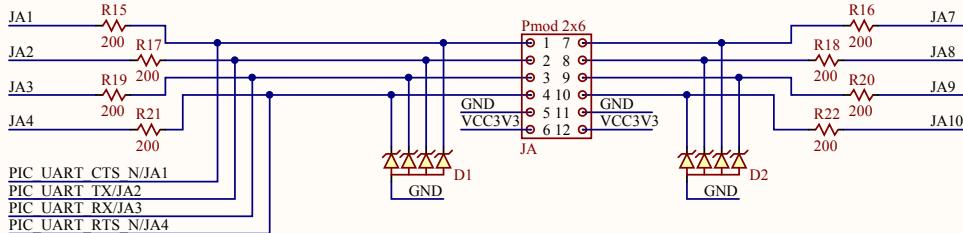
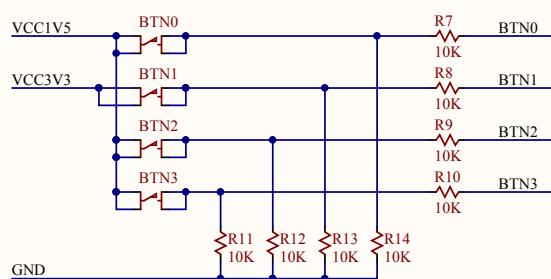
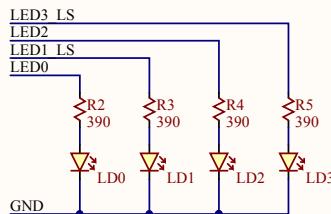
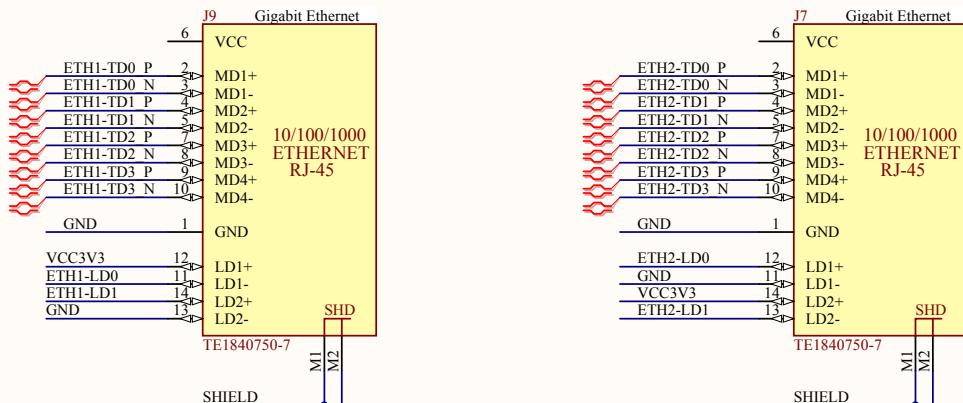


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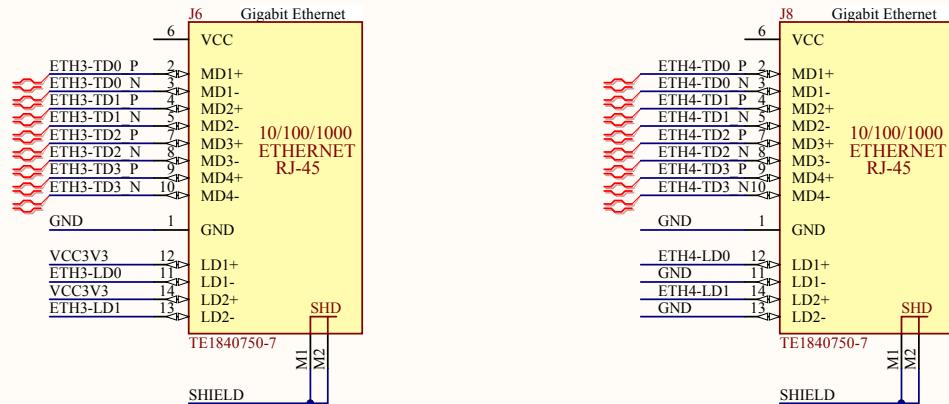


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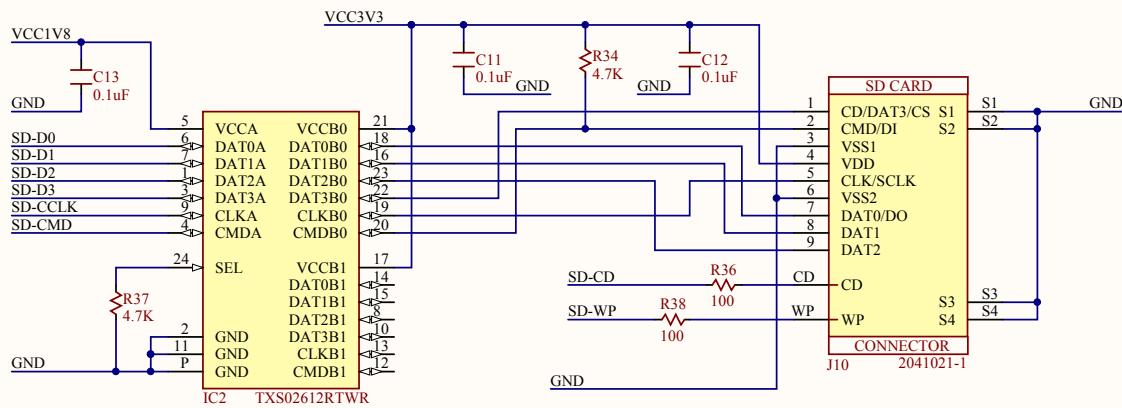
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Title

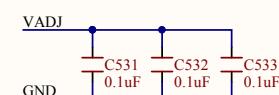
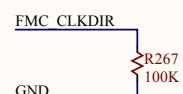
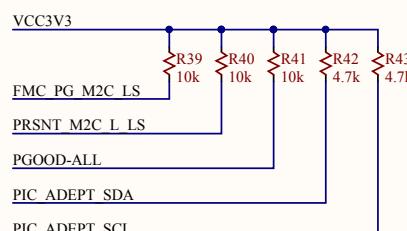
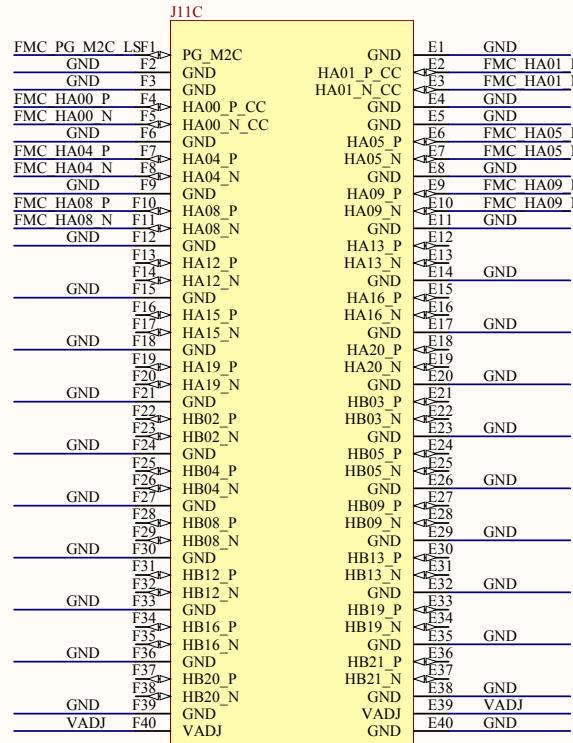
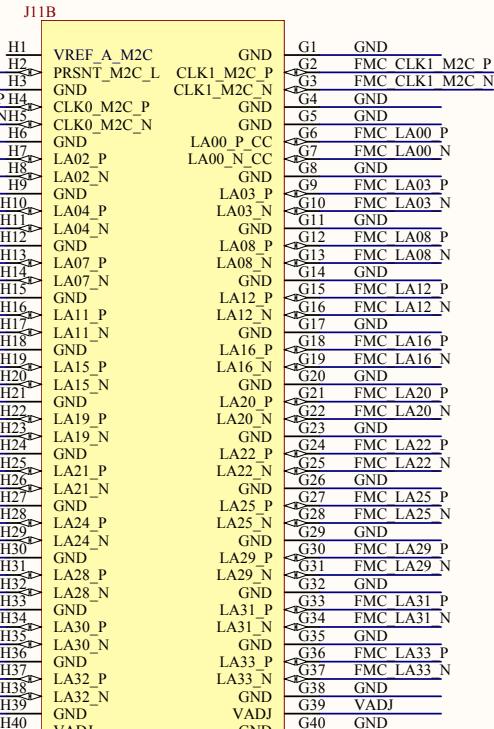
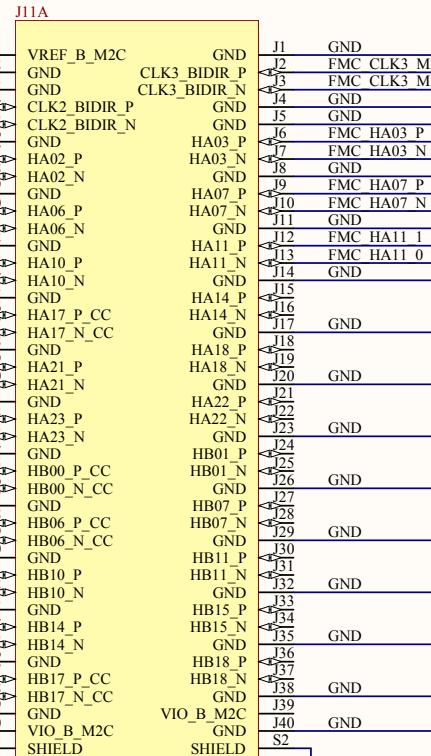
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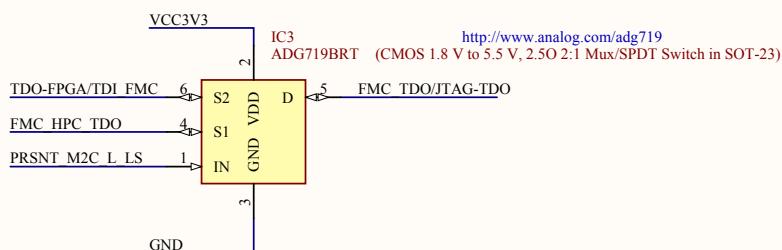
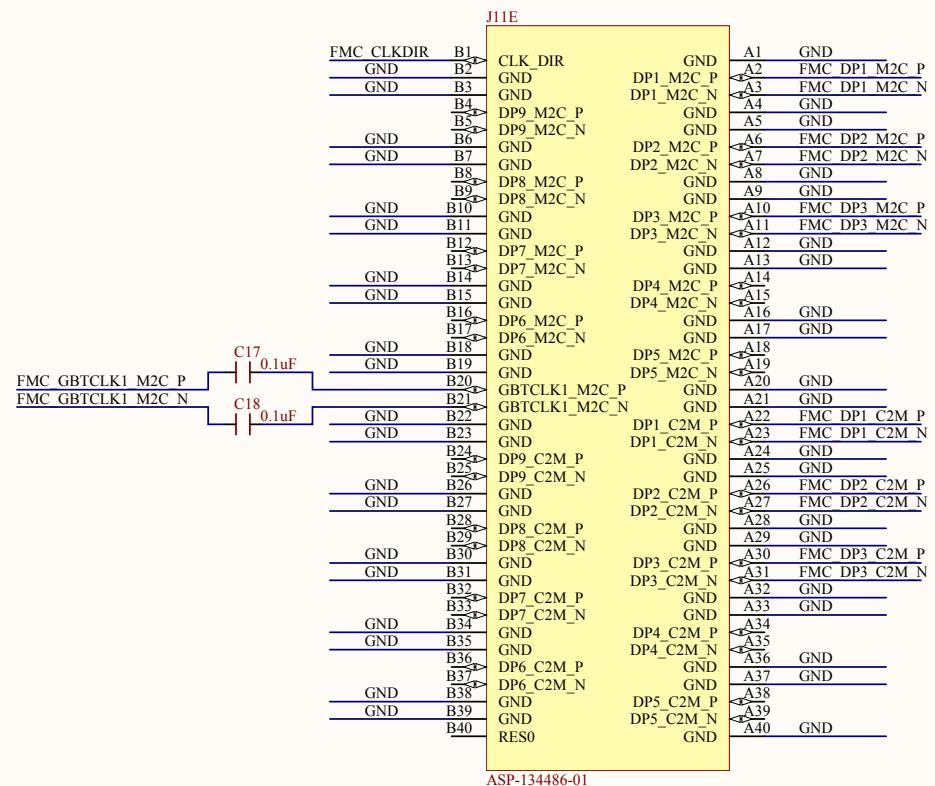
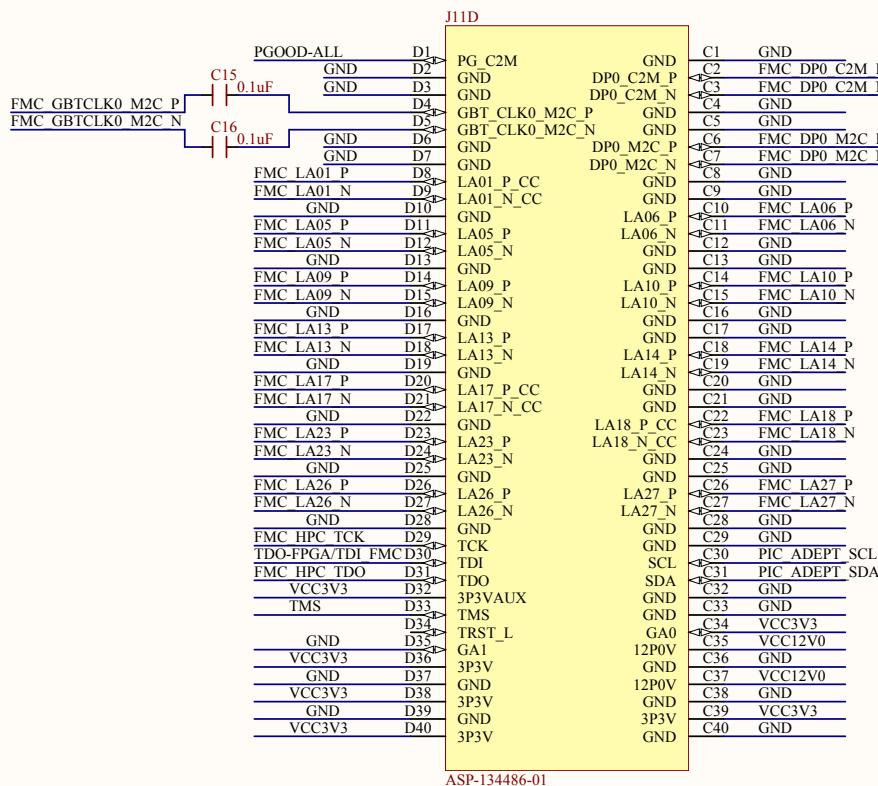
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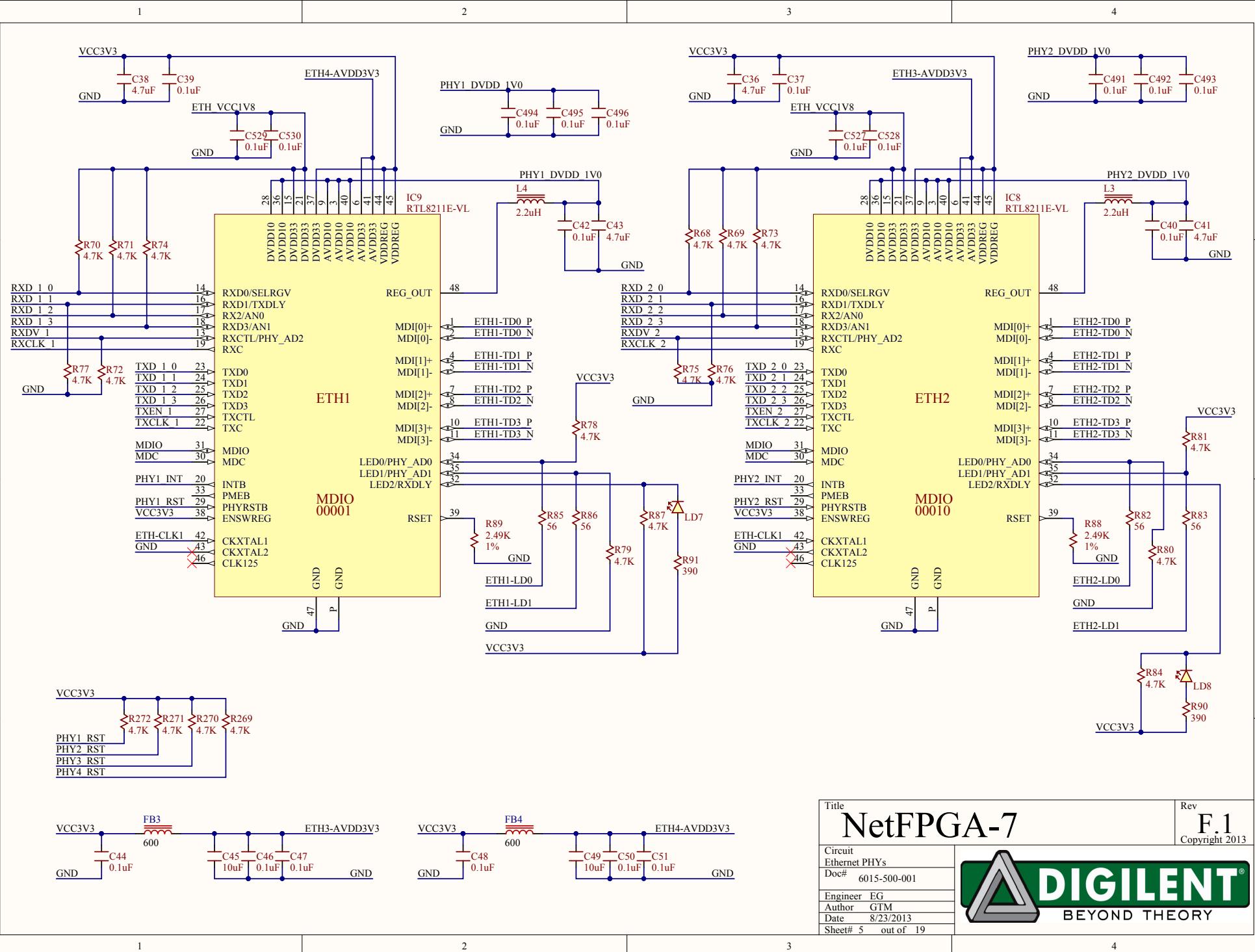
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Doc#

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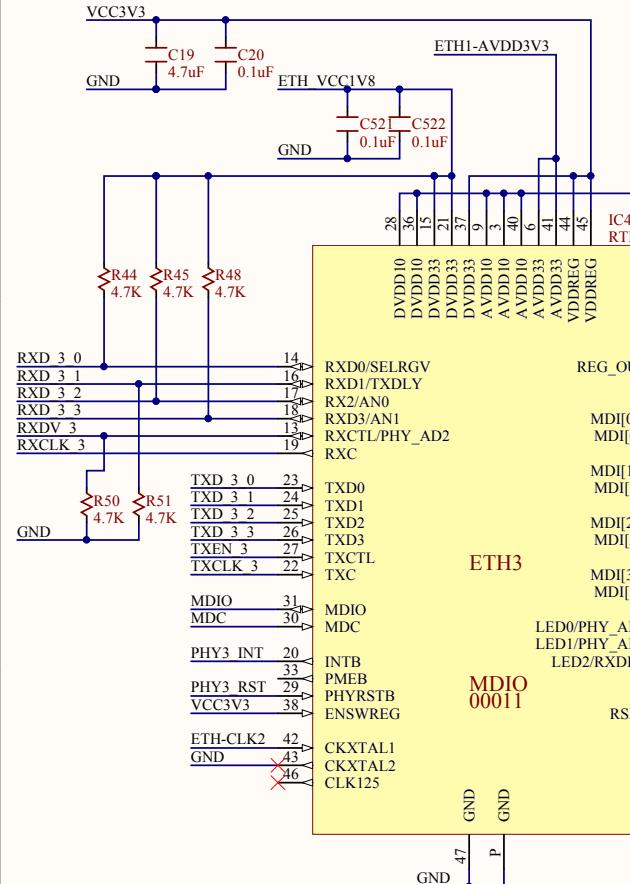
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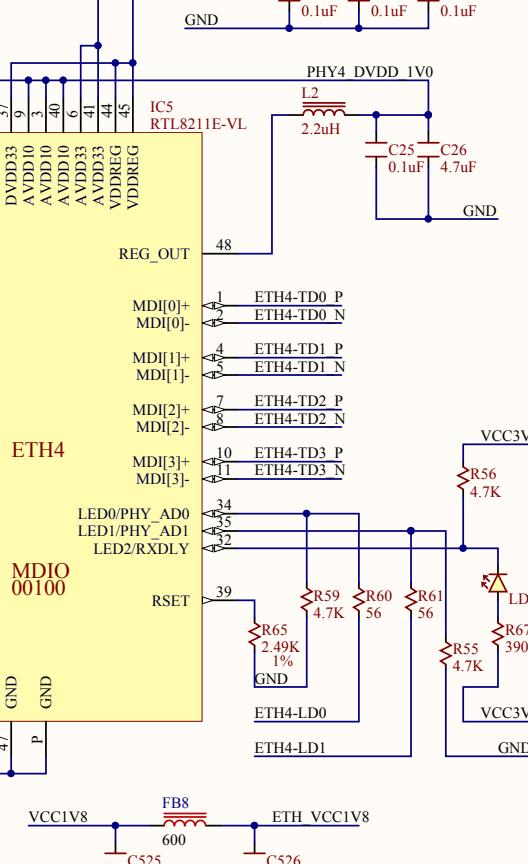
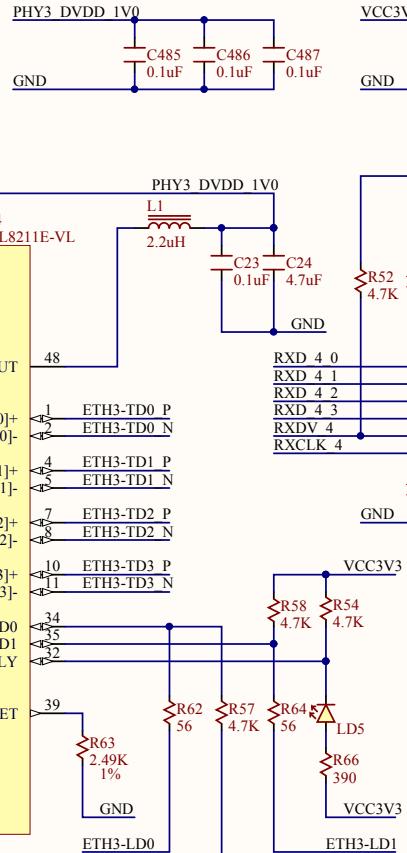
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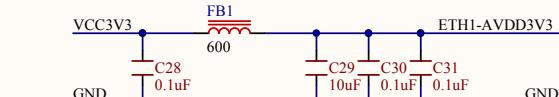
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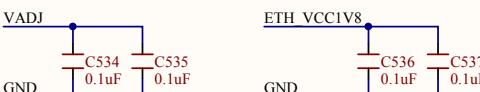
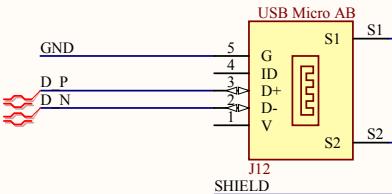
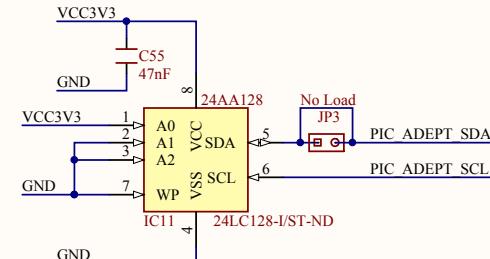
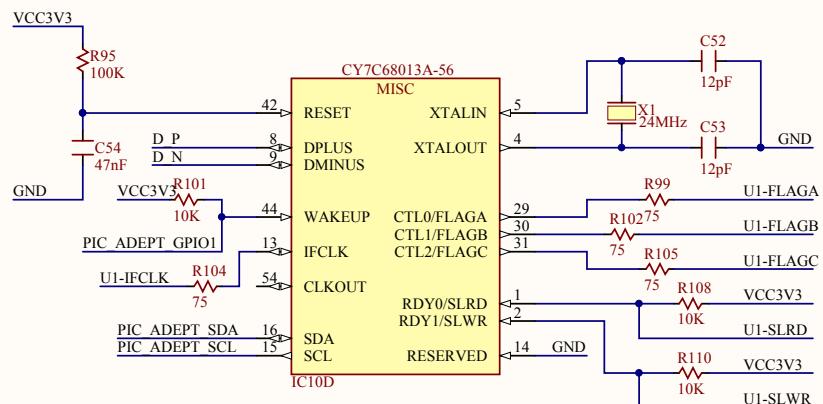
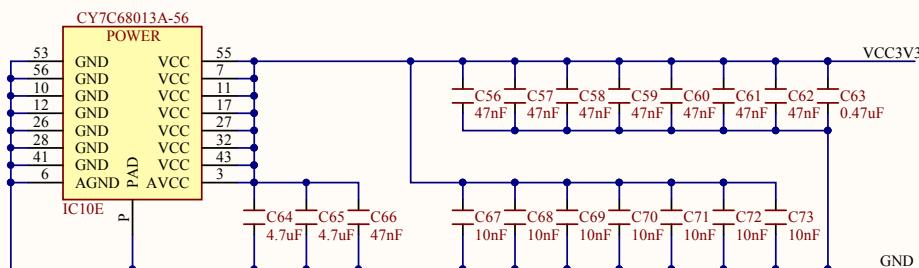
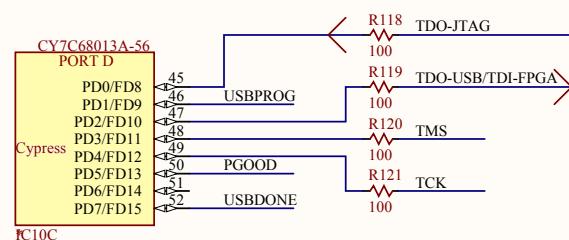
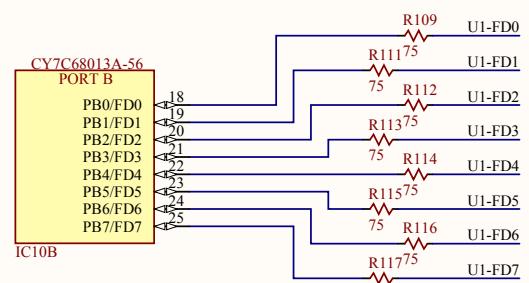
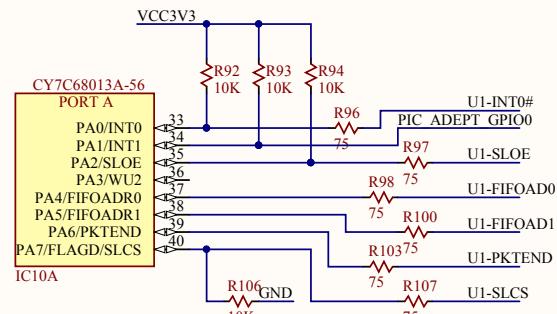


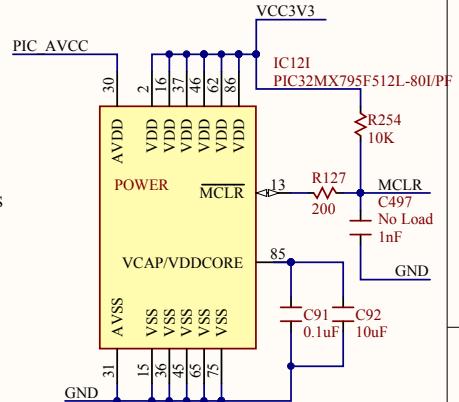
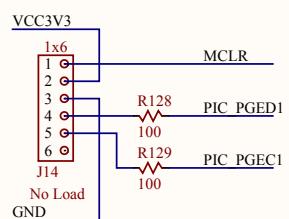
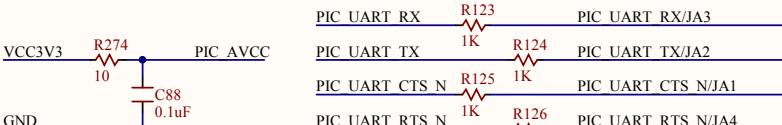
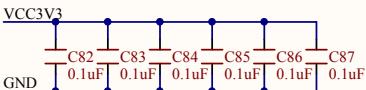
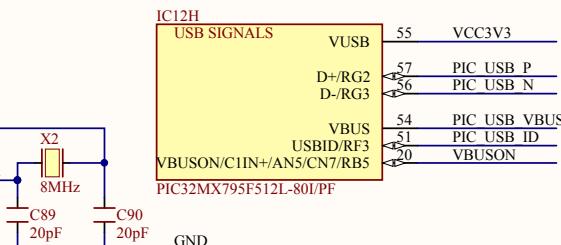
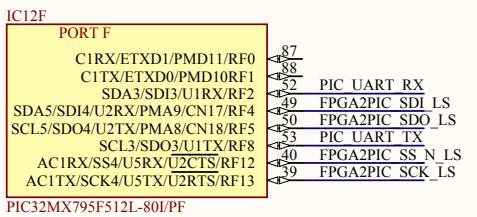
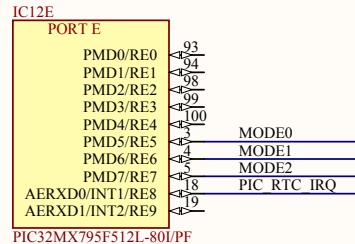
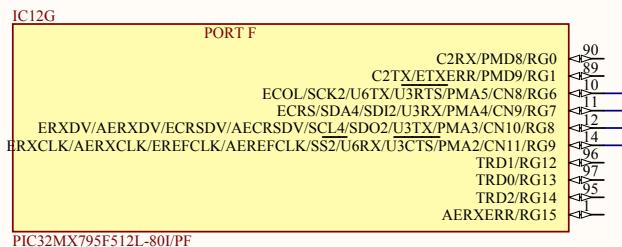
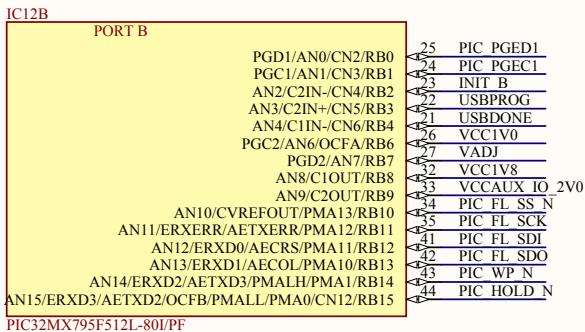
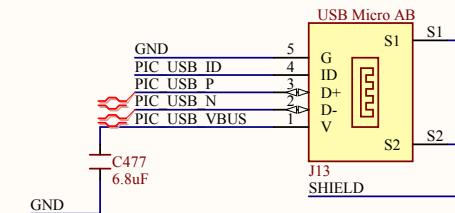
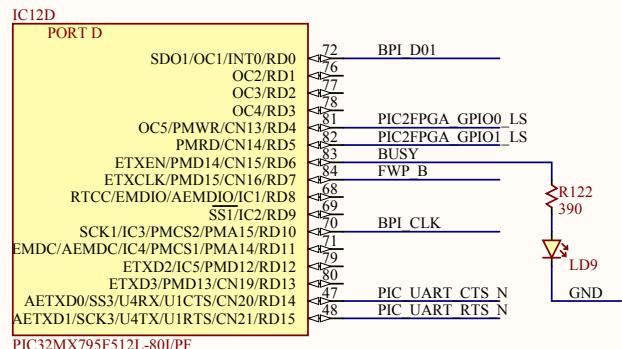
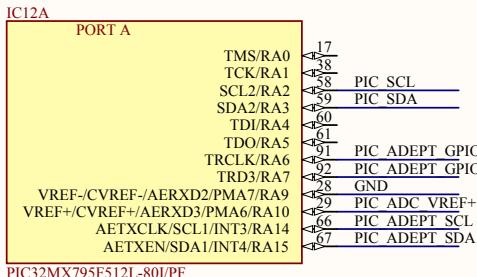
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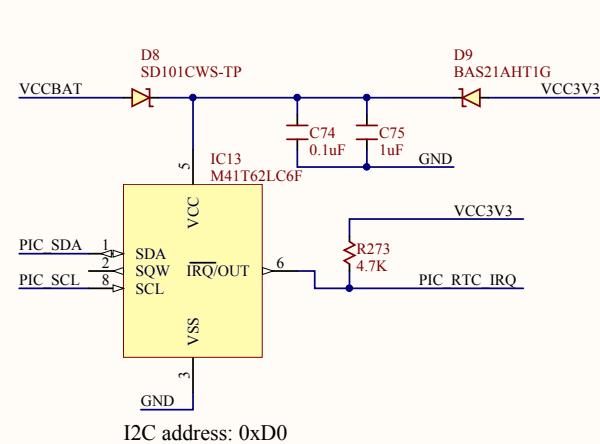
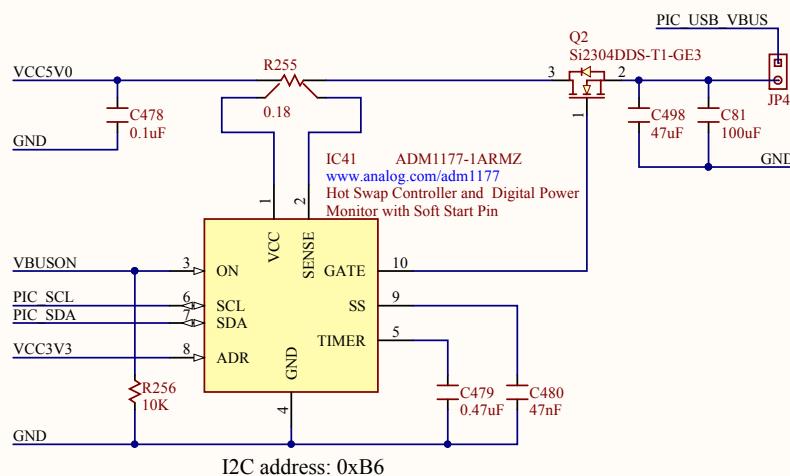


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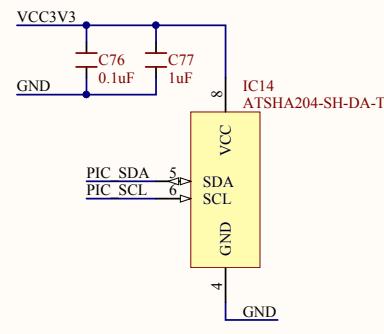
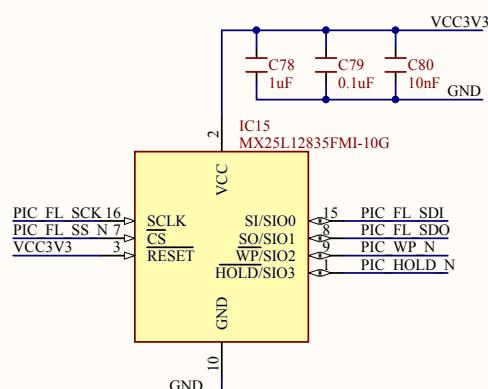
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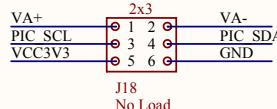
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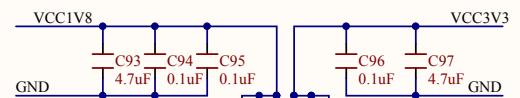
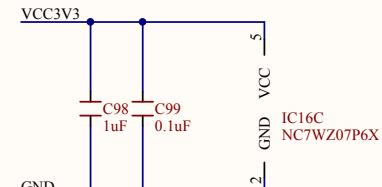
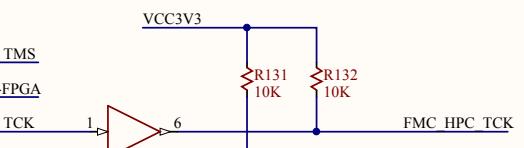
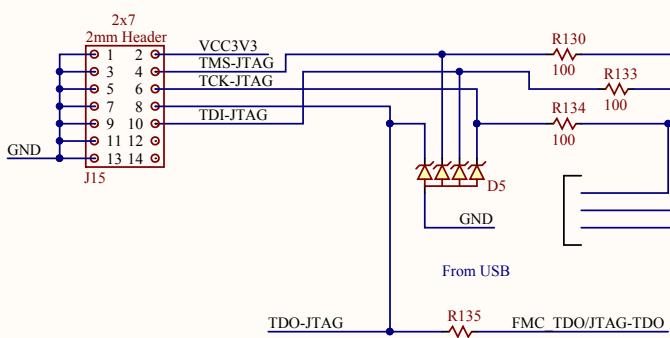
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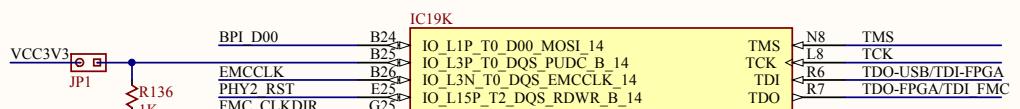
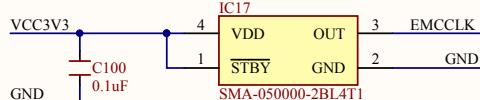
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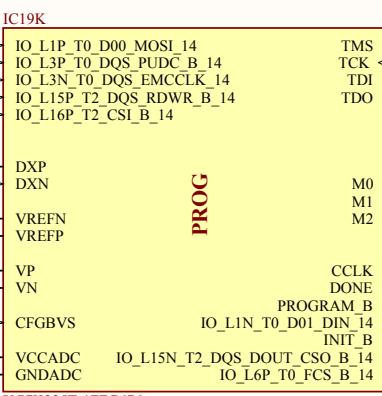
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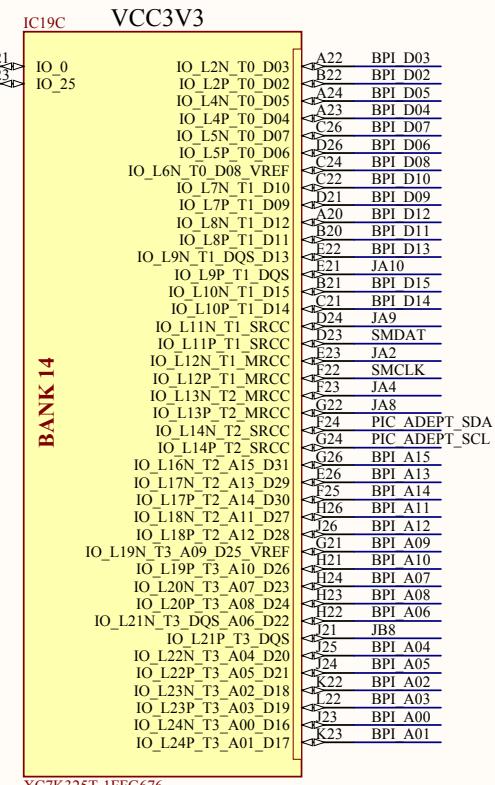
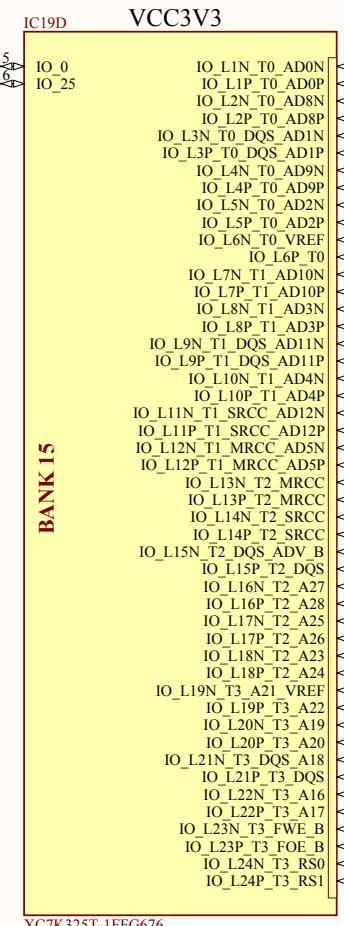
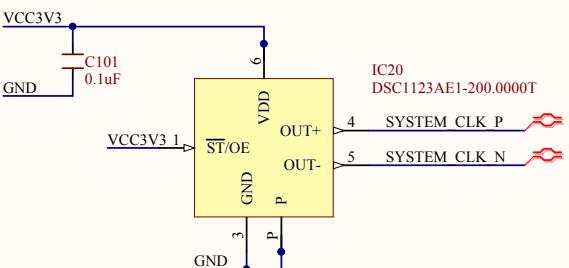
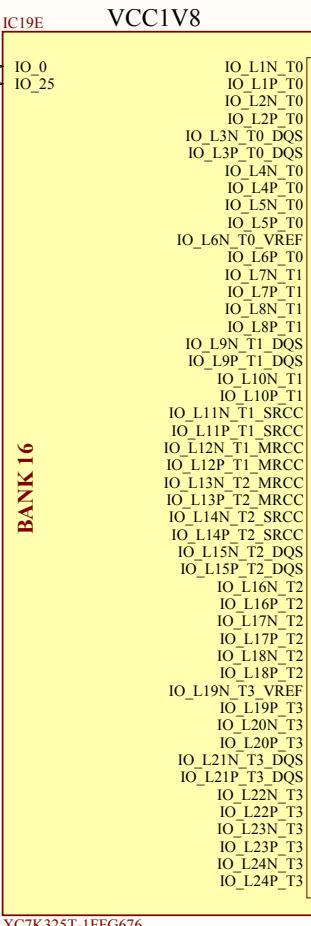
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BPI A24	A24	V <sub>CC</sub>
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BPI WE	G8	WE
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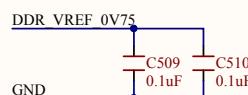
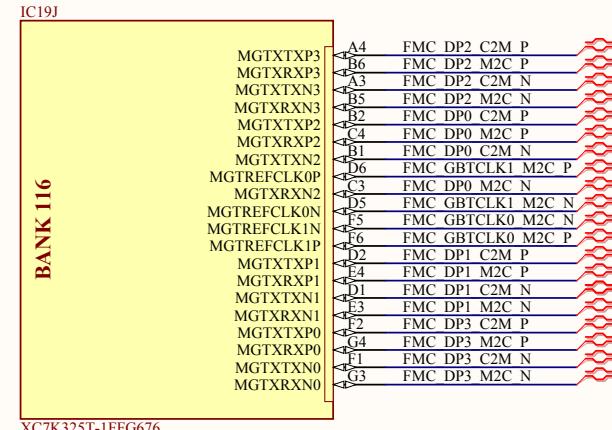
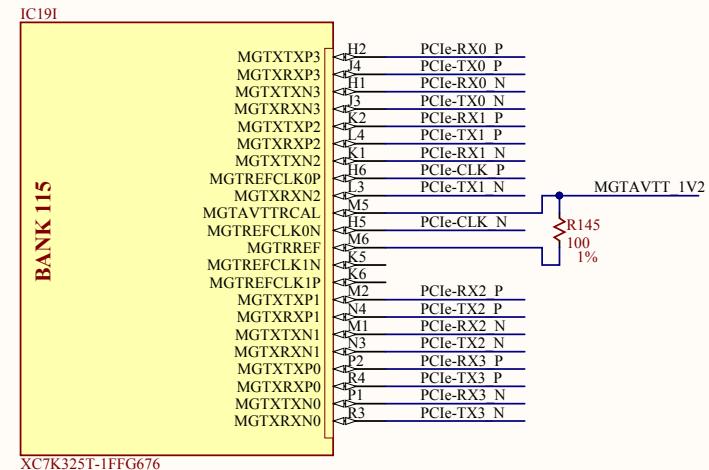
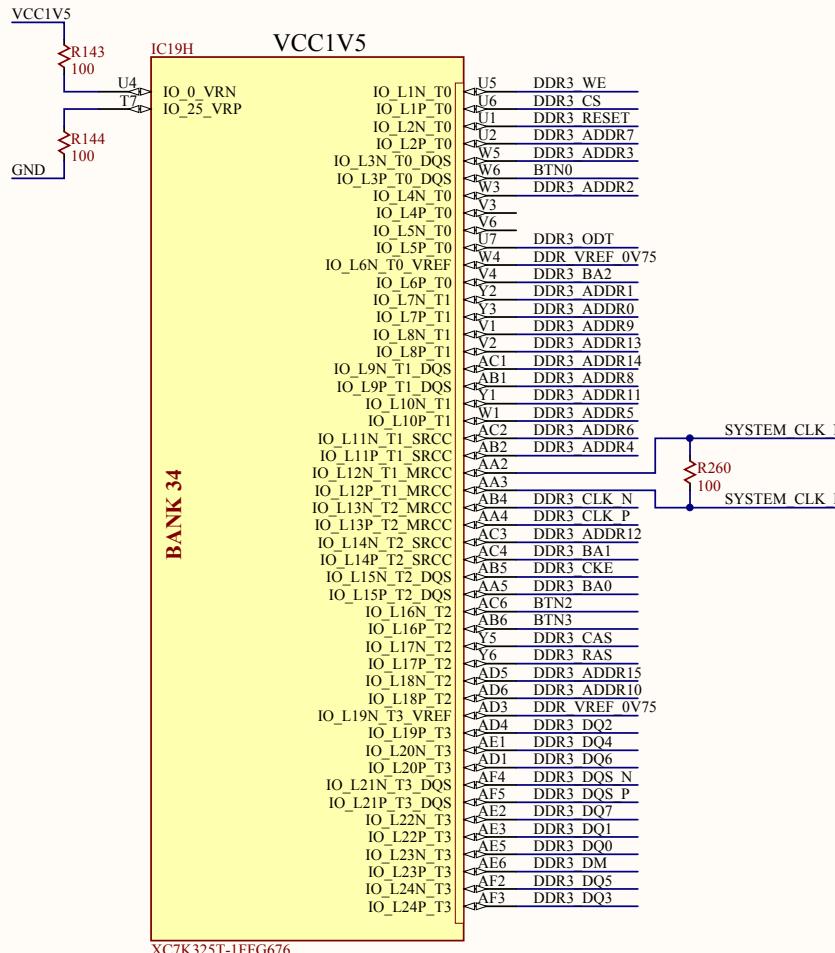
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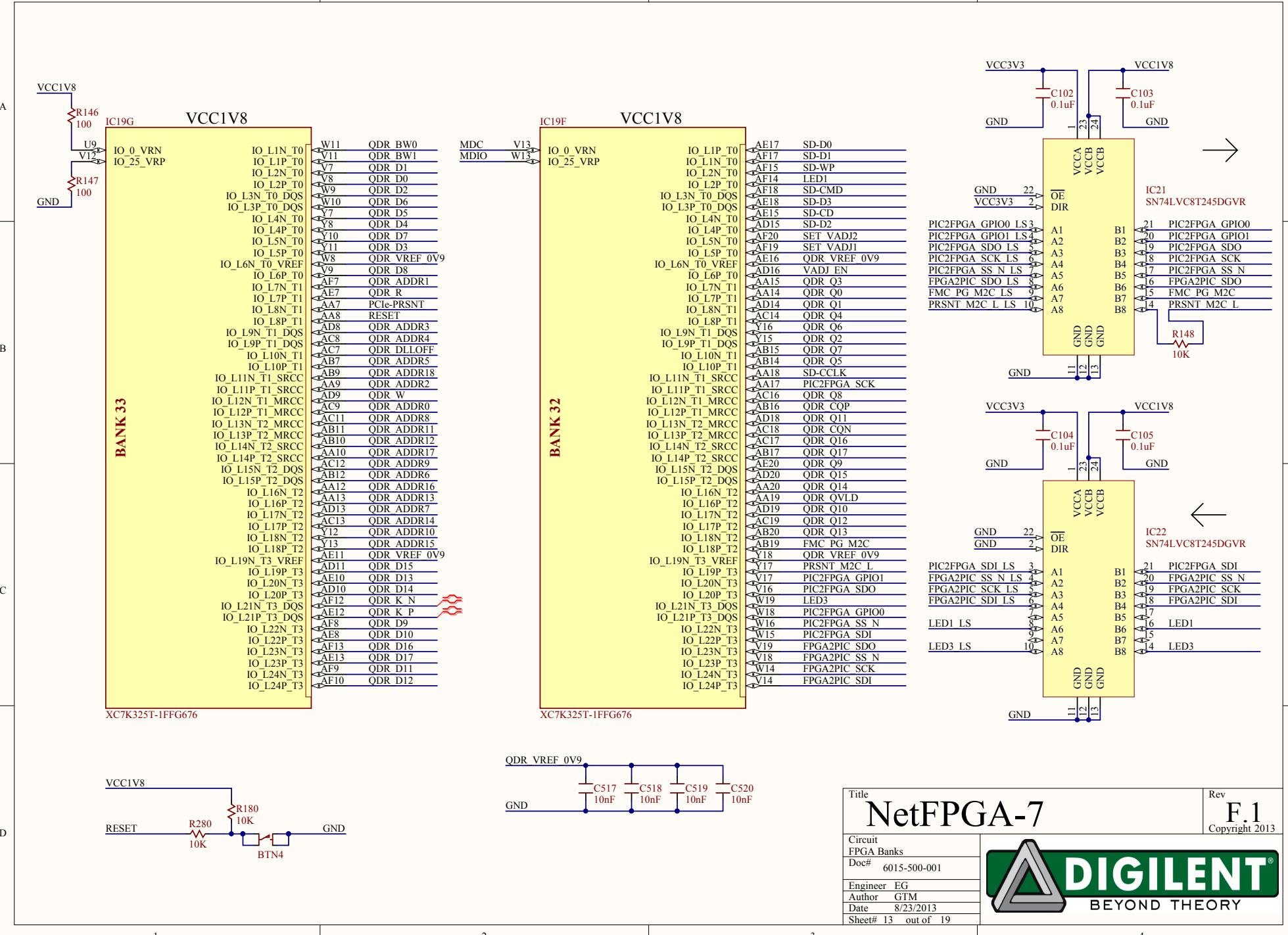


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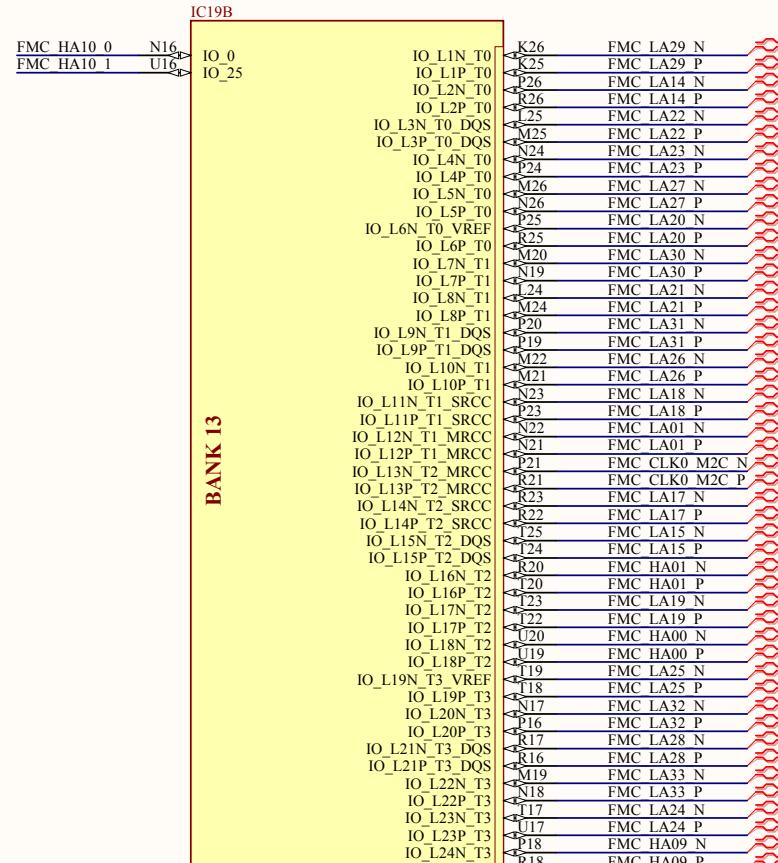
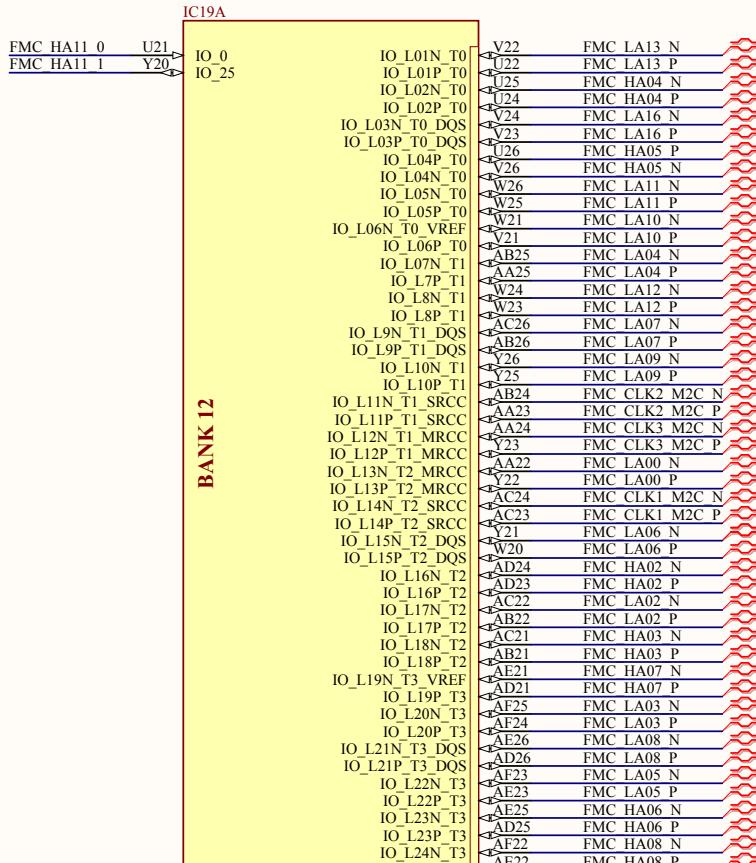






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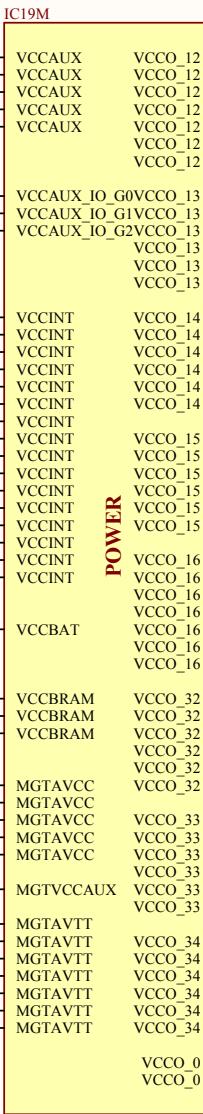
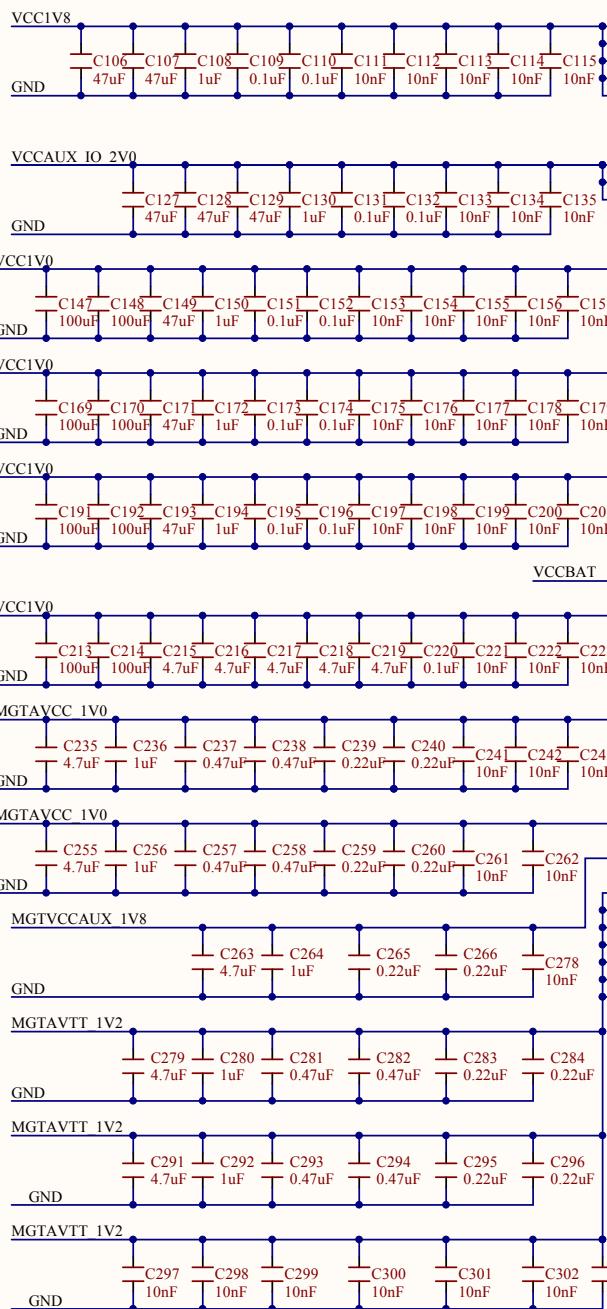
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A6	GND	K11
A7	GND	K13
A16	GND	K13
A26	GND	K19
AA6	GND	L1
AA16	GND	L5
AA26	GND	L10
AB3	GND	L12
AB13	GND	L14
AB23	GND	L16
AC10	GND	L26
AC20	GND	M4
AD7	GND	M7
AD17	GND	M9
AE4	GND	M13
AE14	GND	M15
AE24	GND	M23
AF1	GND	N1
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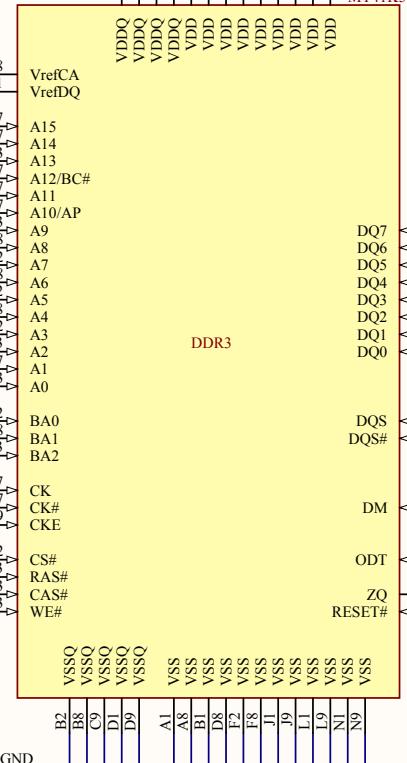
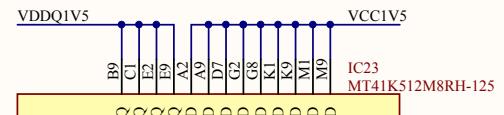
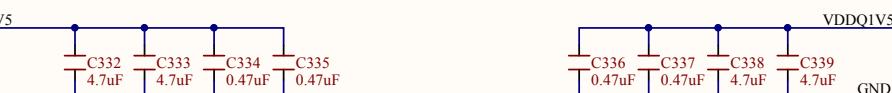
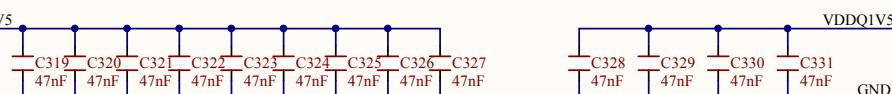
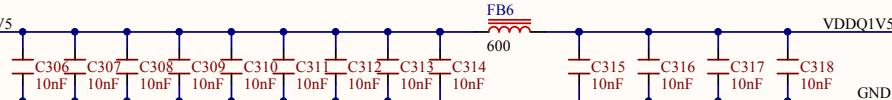
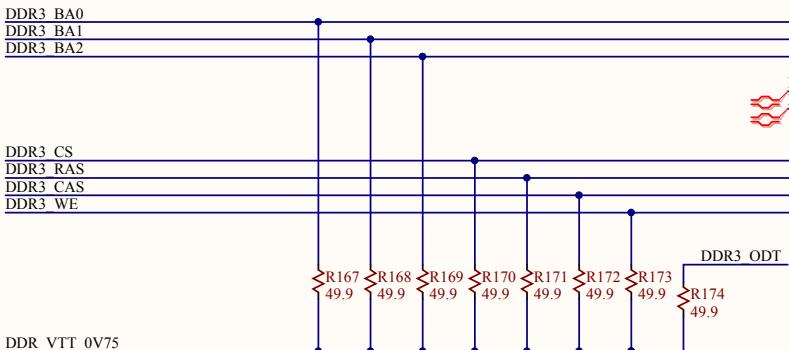
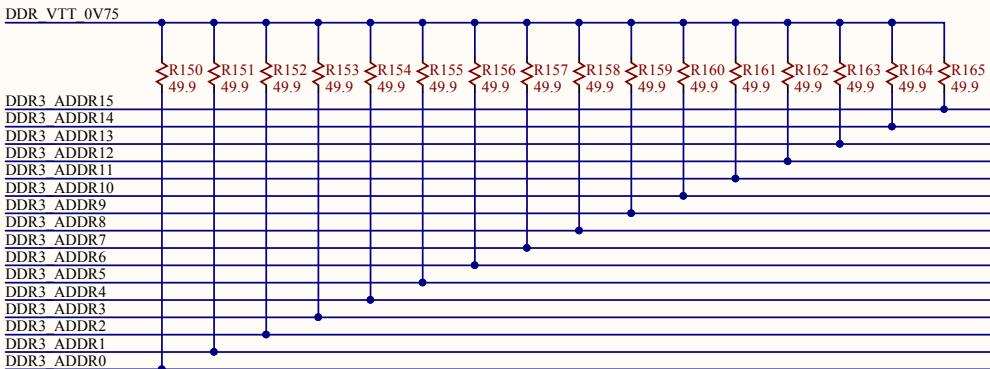
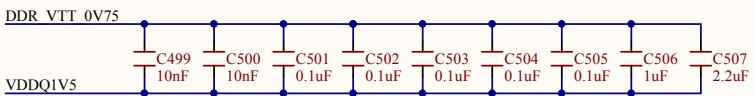


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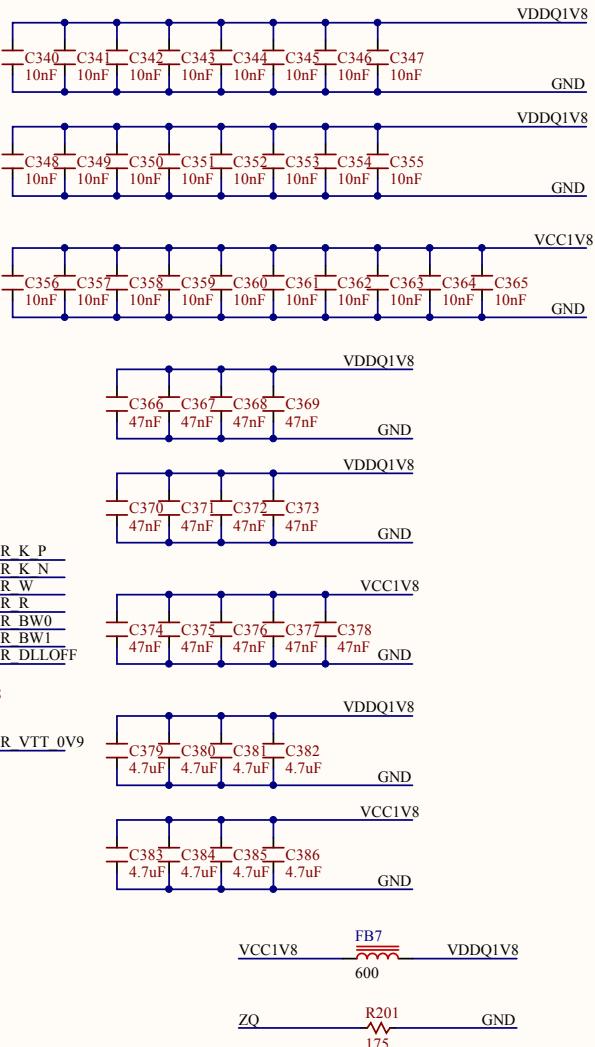
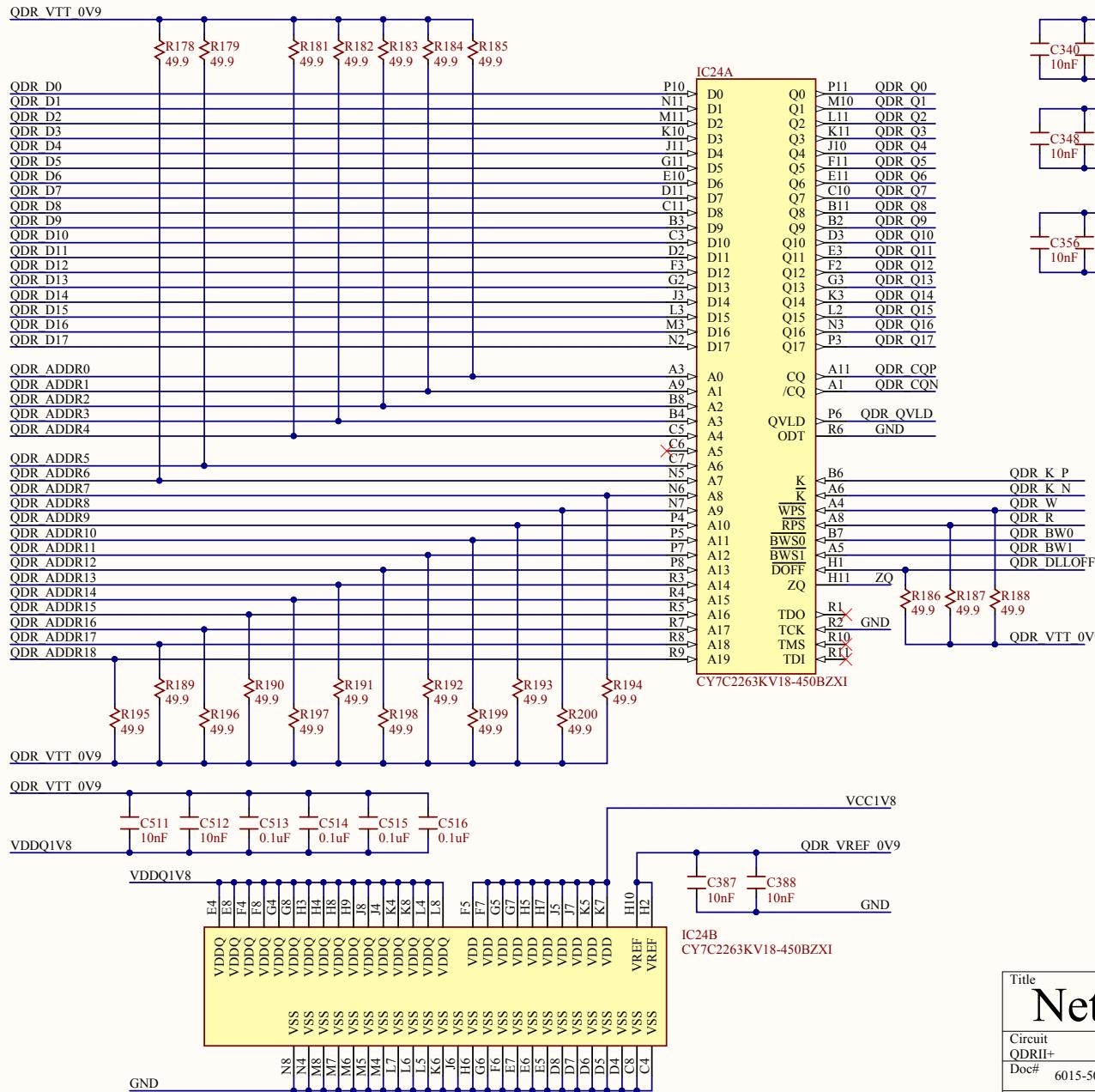
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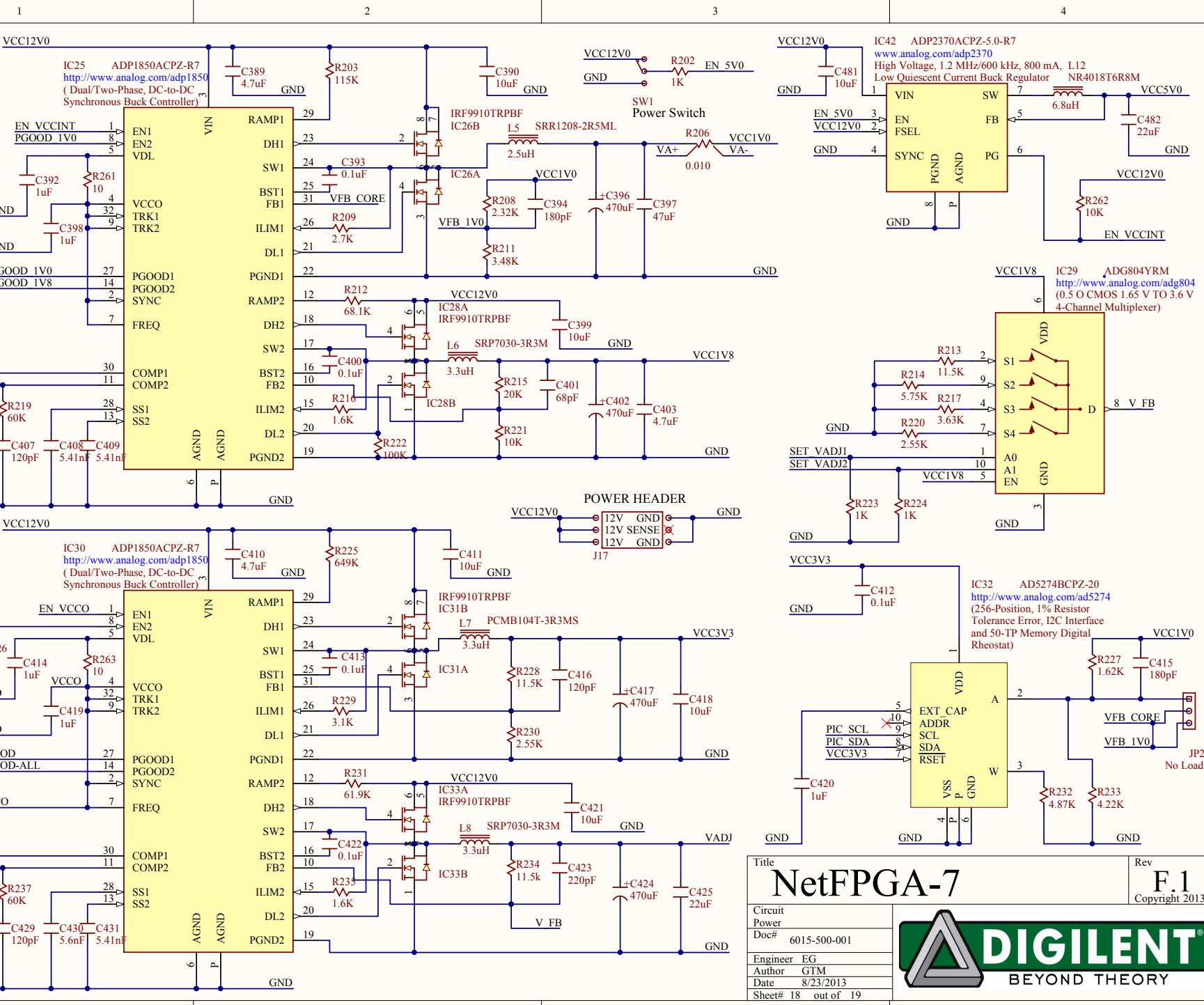


Title

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Doc#	6015-500-001
Engineer	EG
Author	GTM
Date	8/23/2013
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Title  
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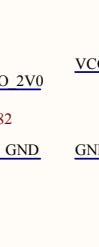
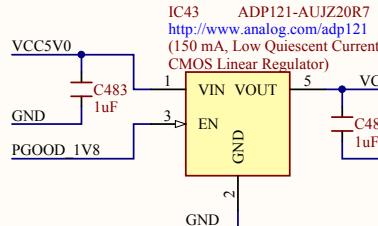
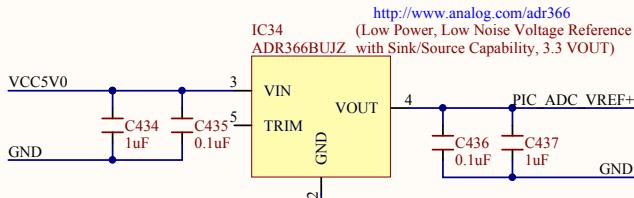
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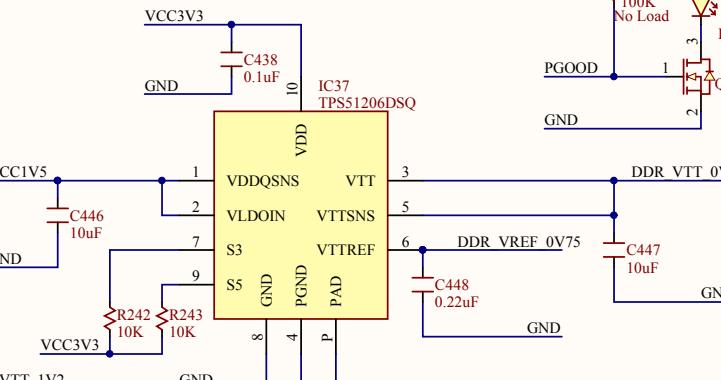
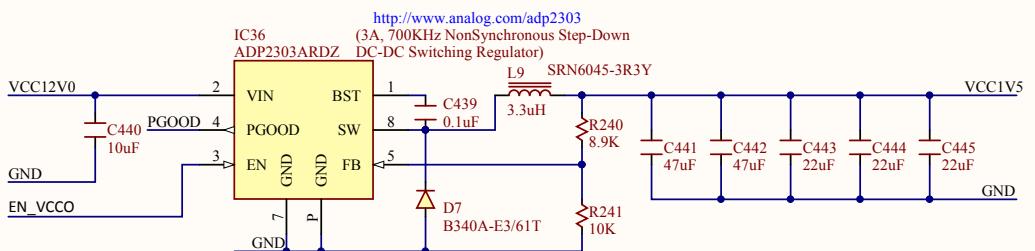
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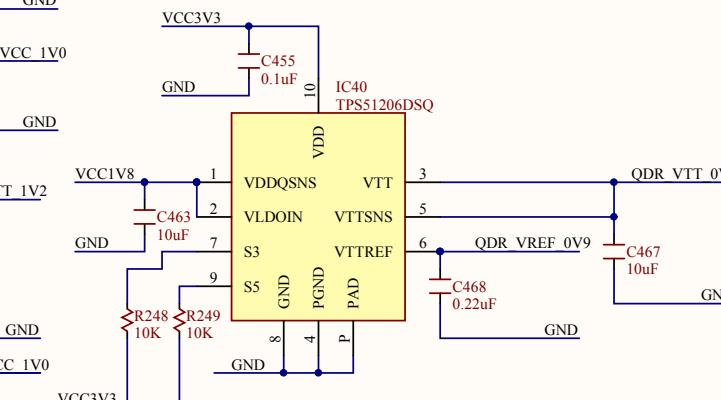
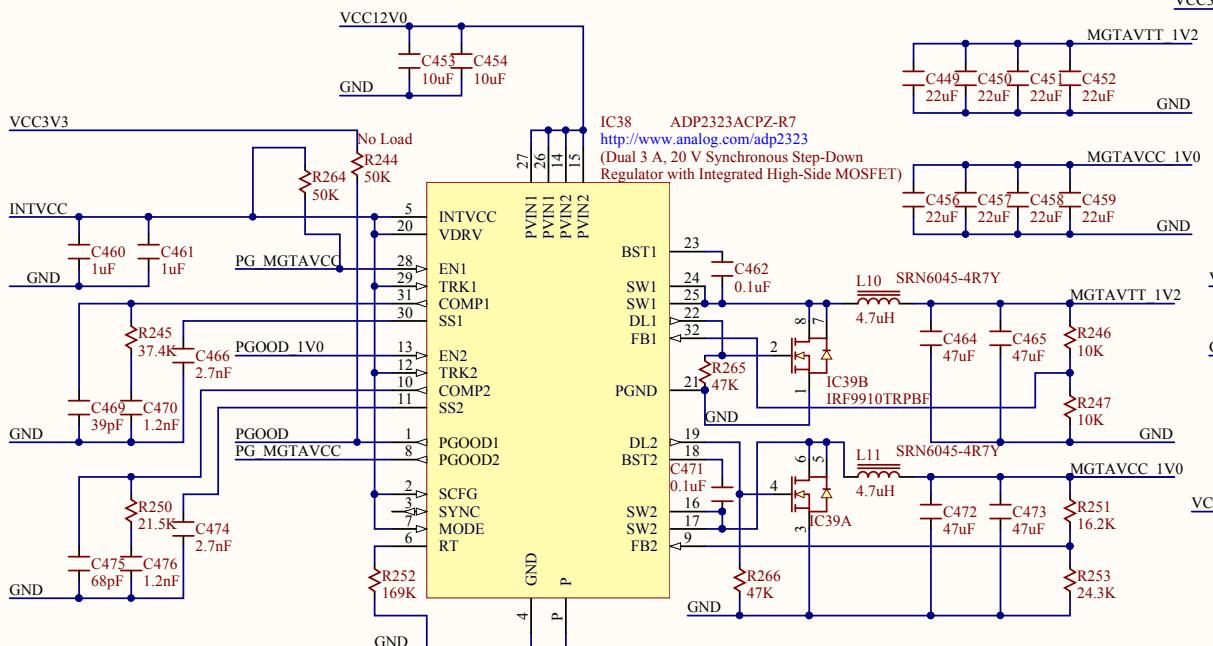
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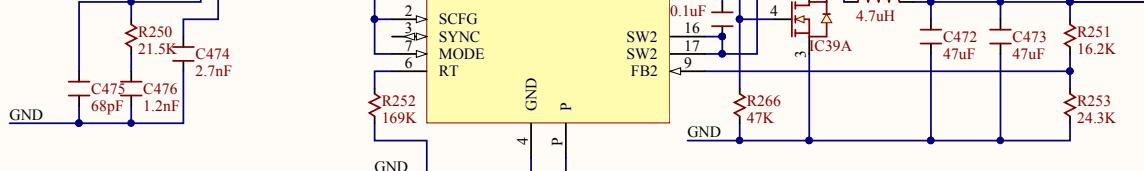
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C



C

D



D

NetFPGA-7

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2

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