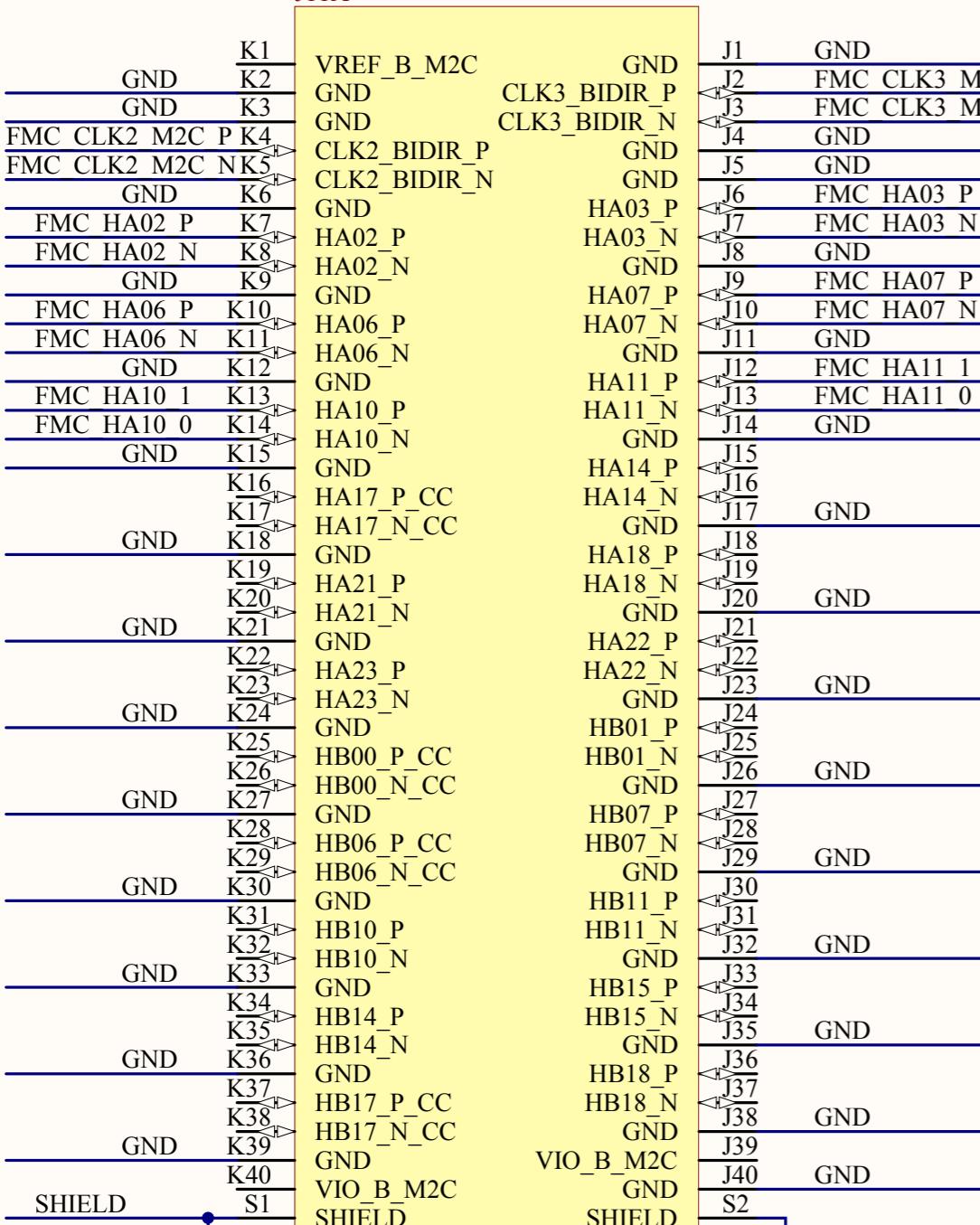


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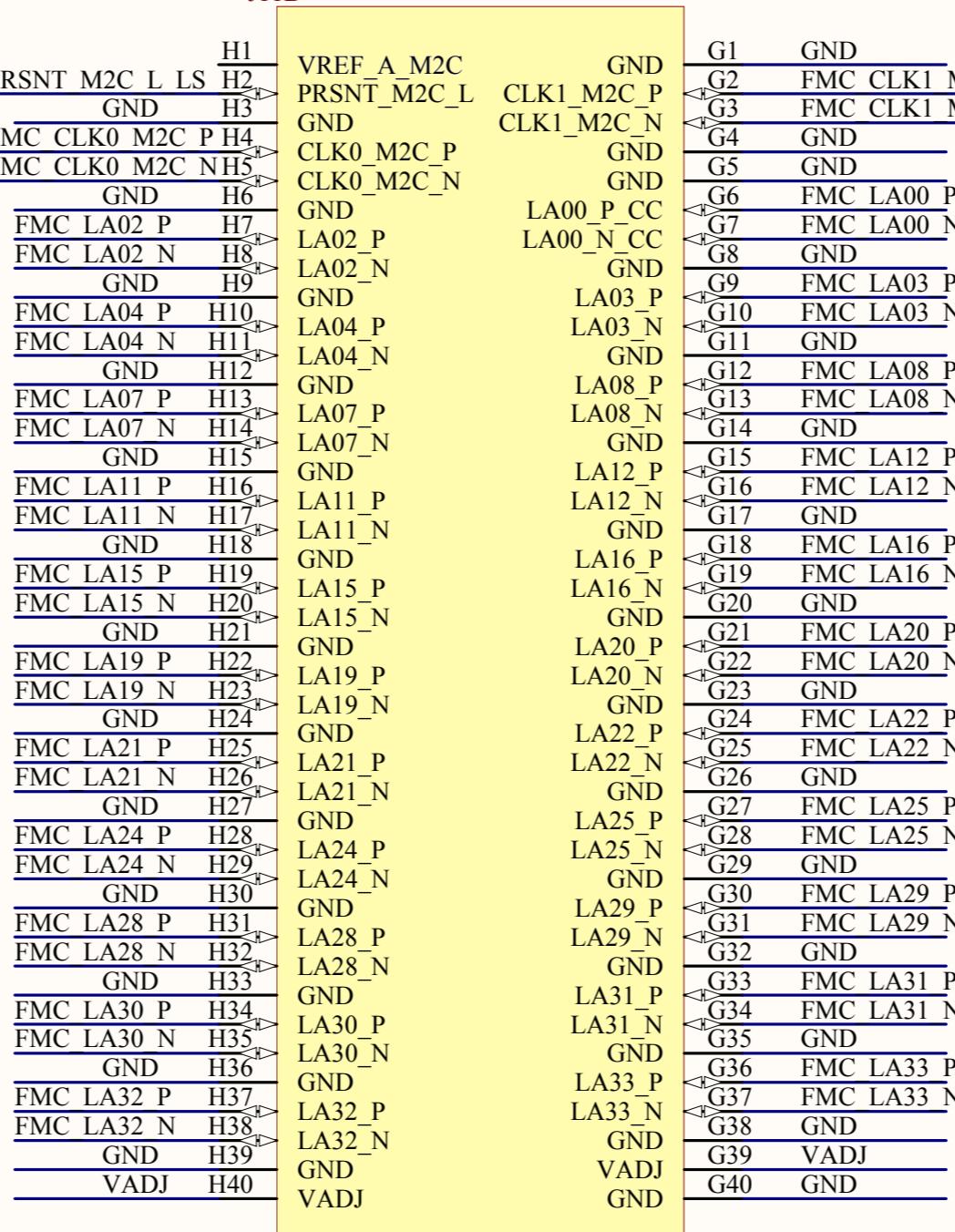
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Engineer EG	Author GTM
Date 6/18/2013	Sheet# 2 out of 19

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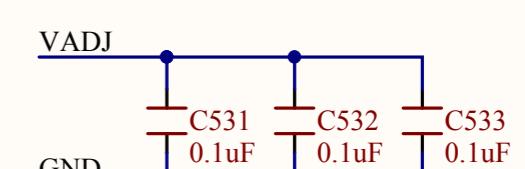
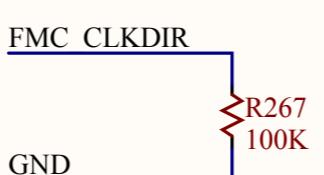
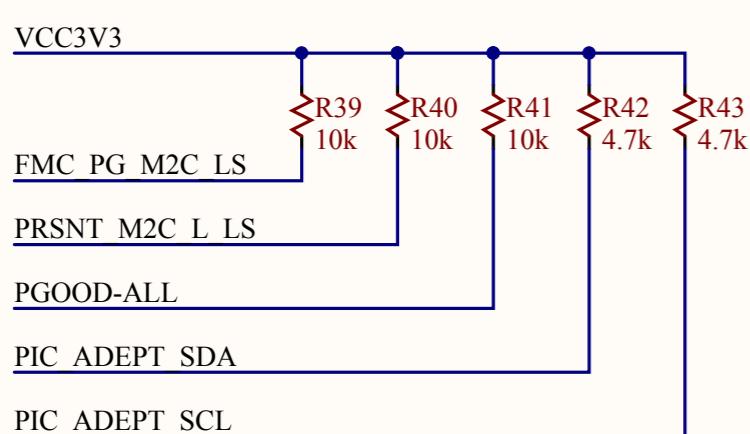
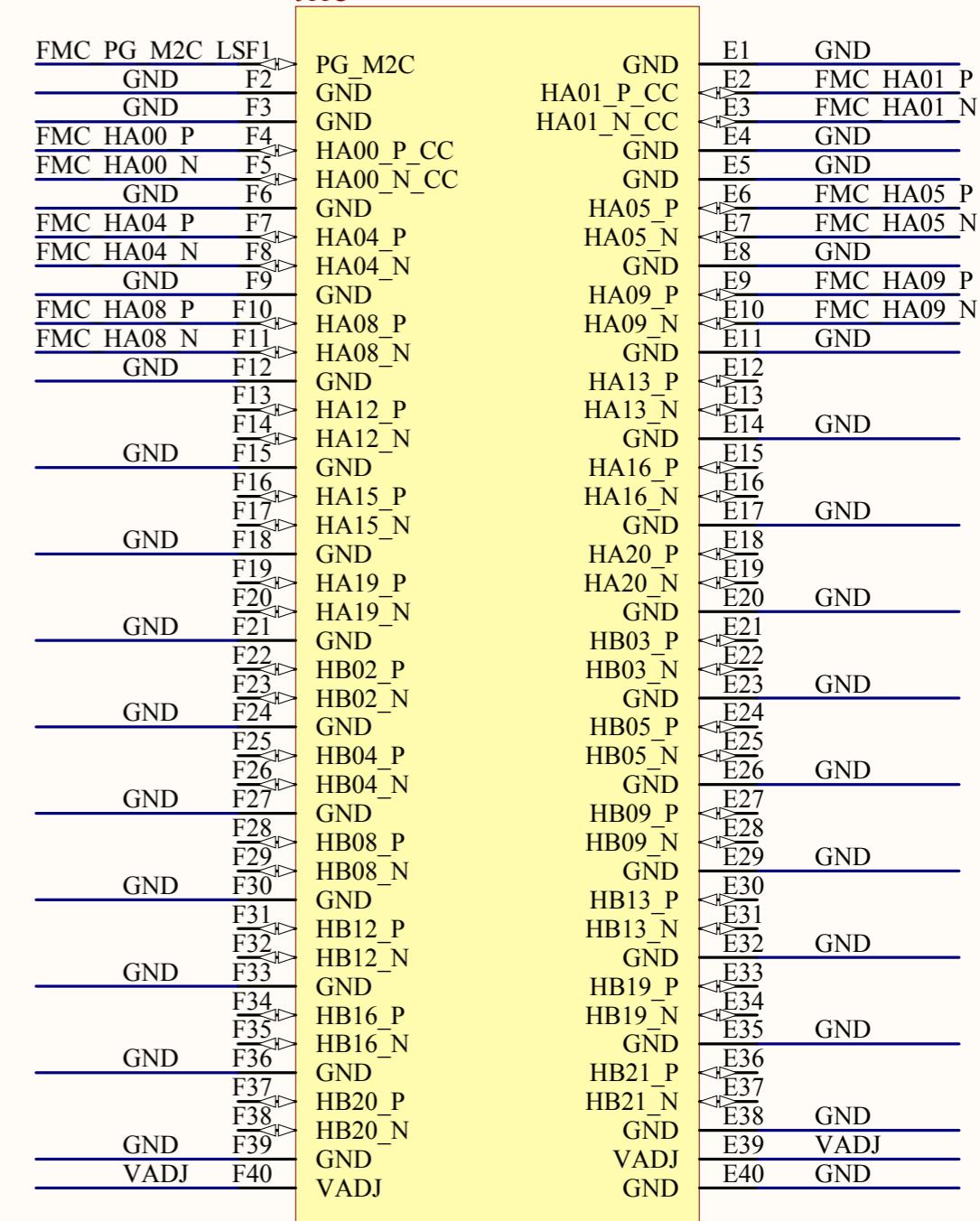
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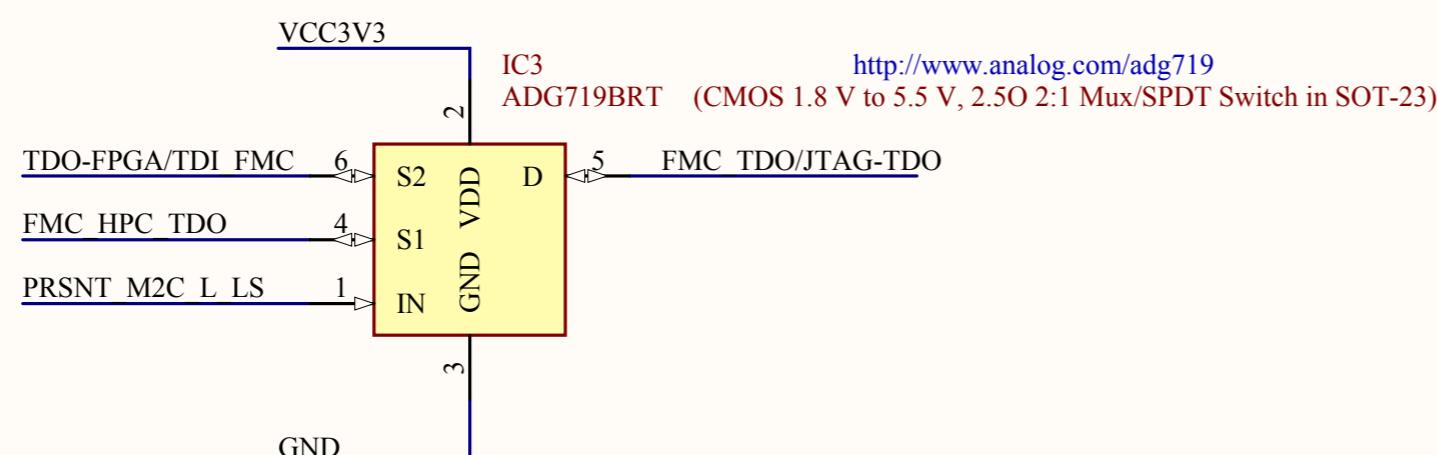
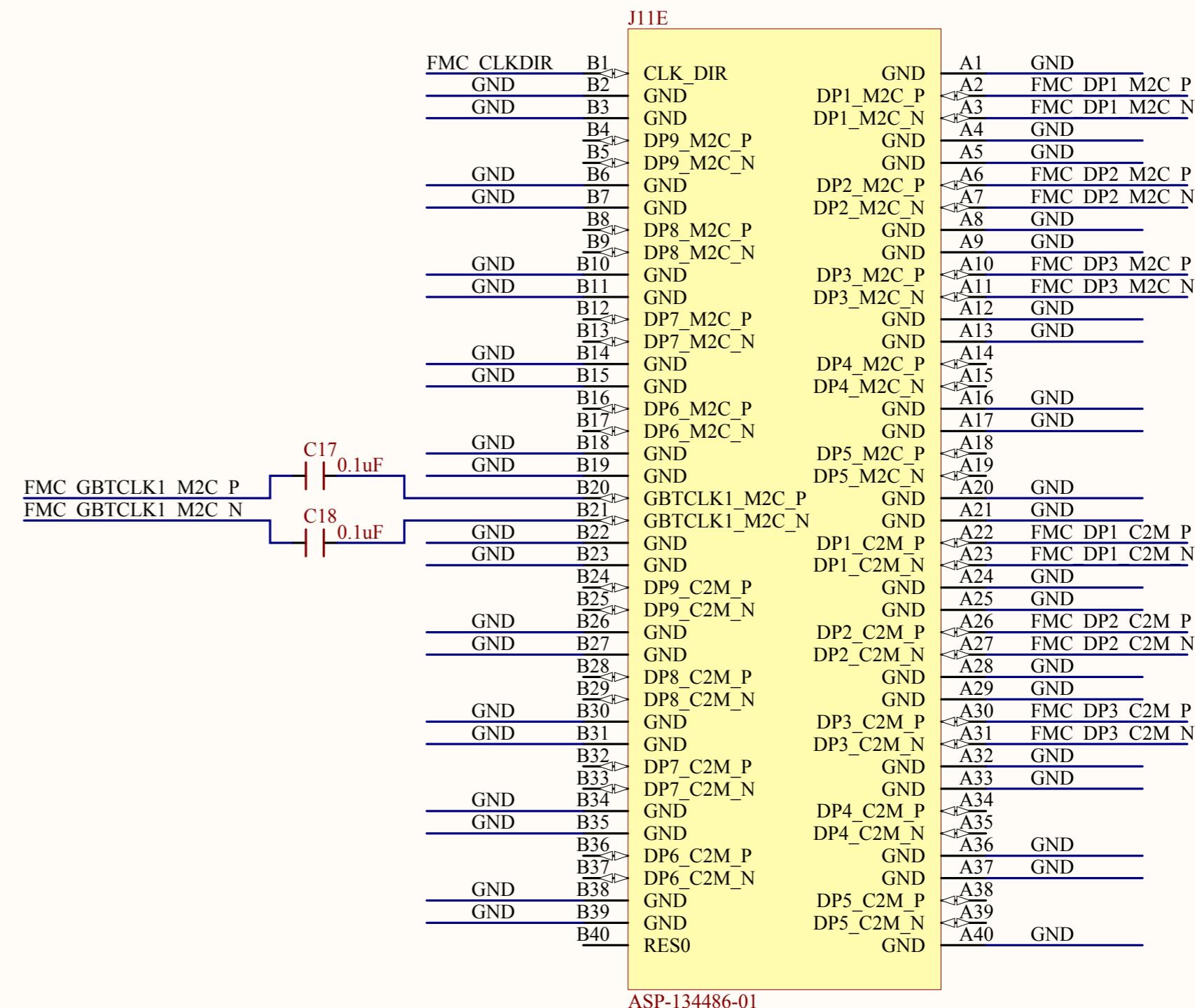
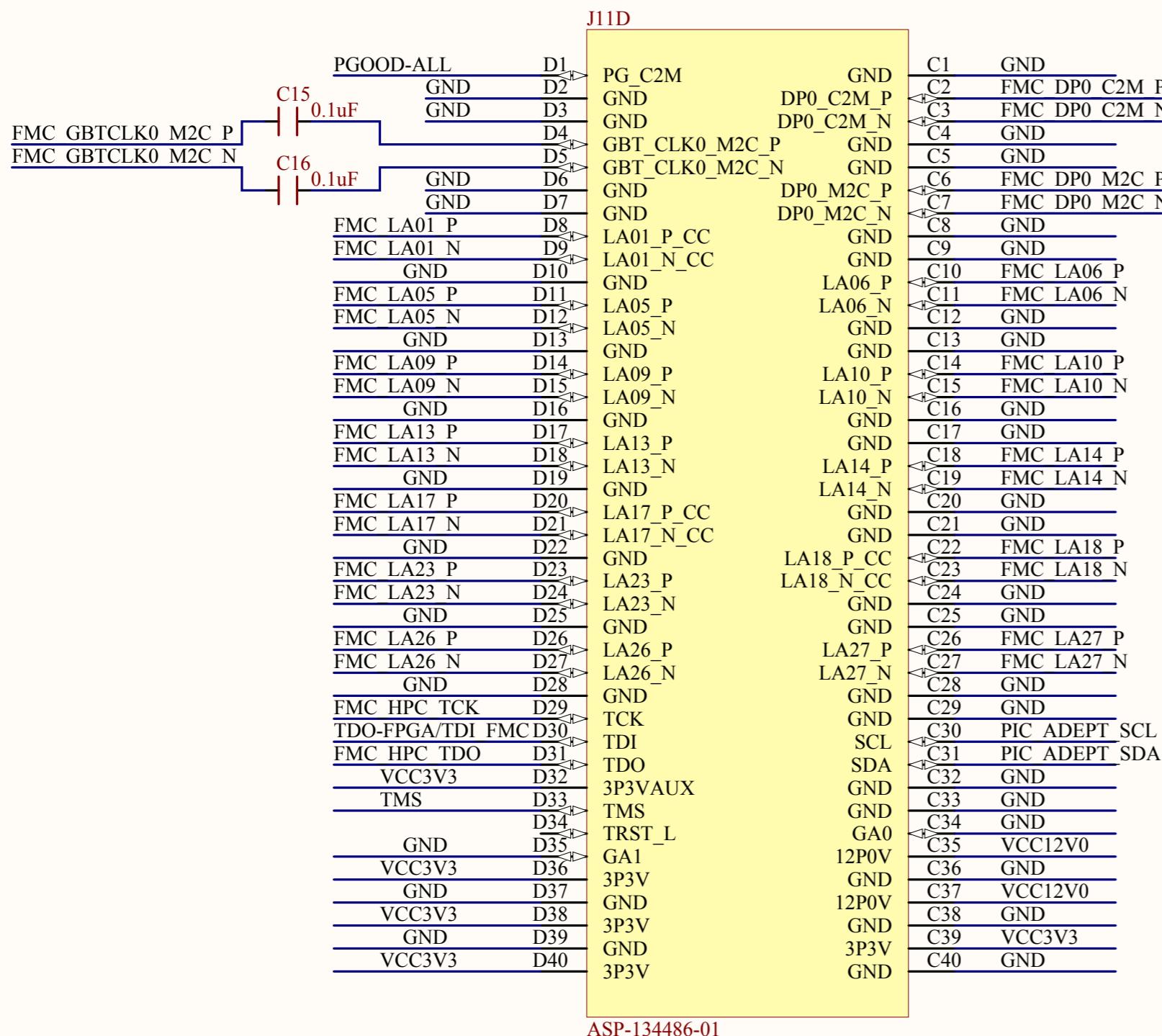


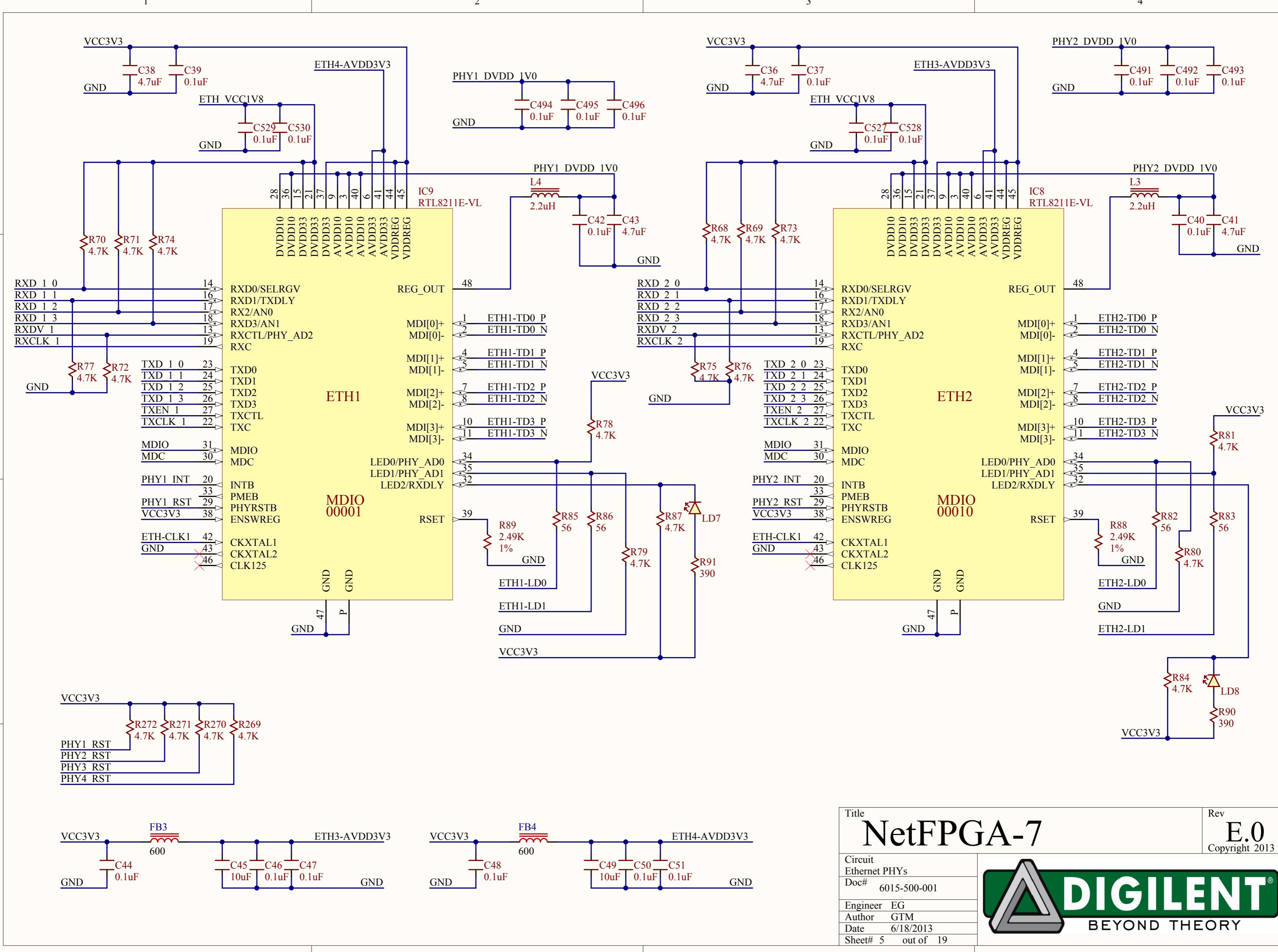
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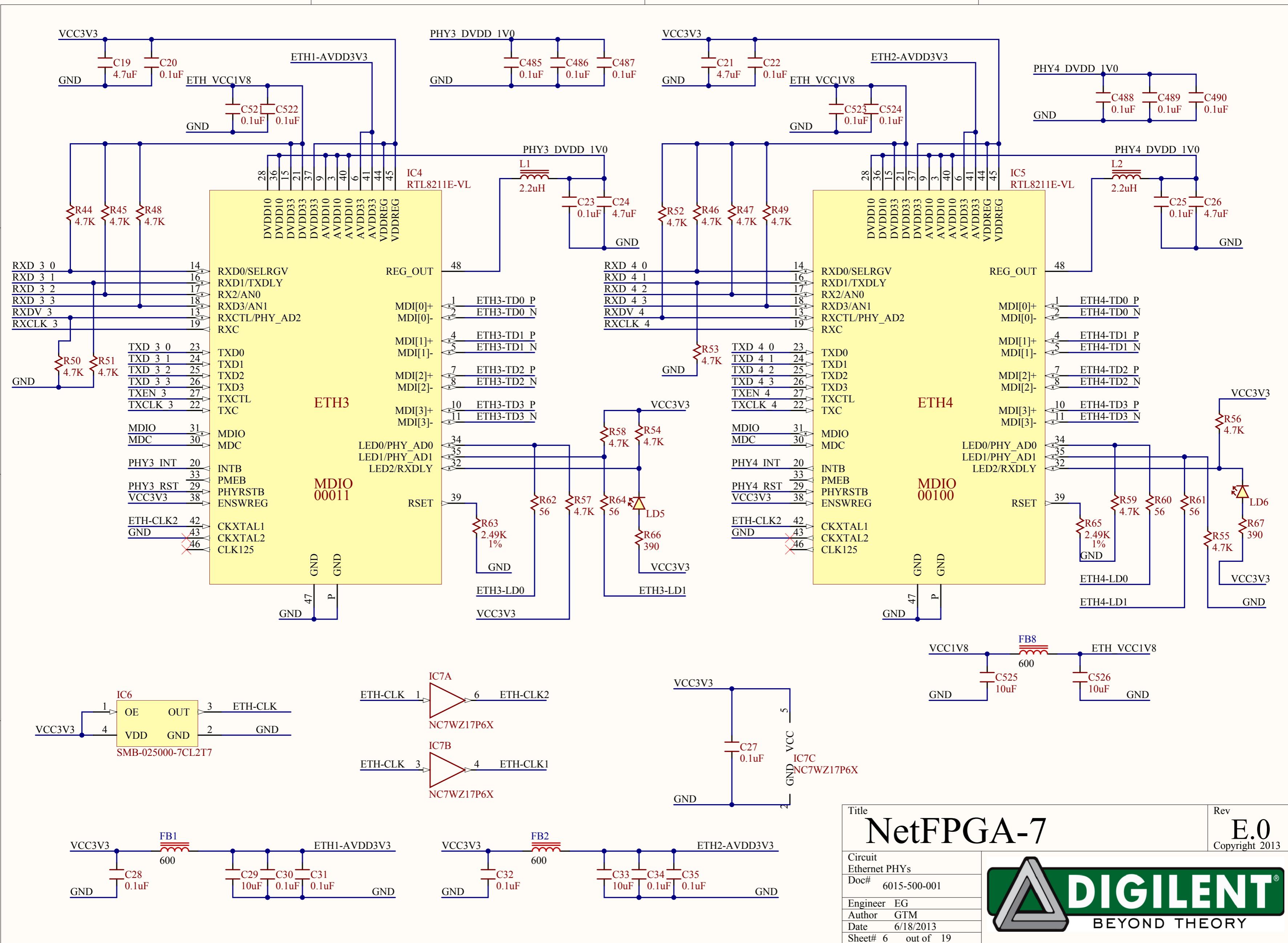


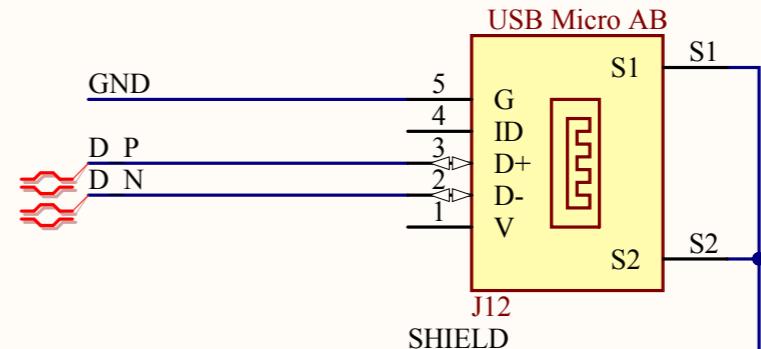
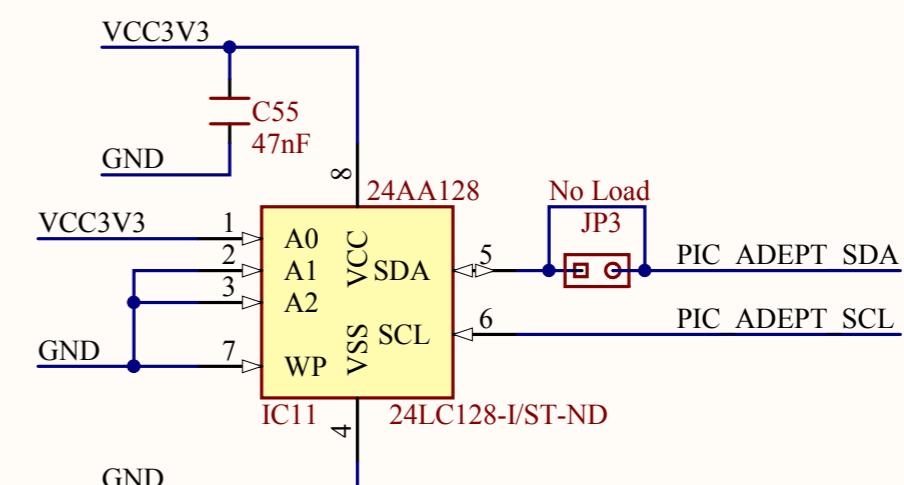
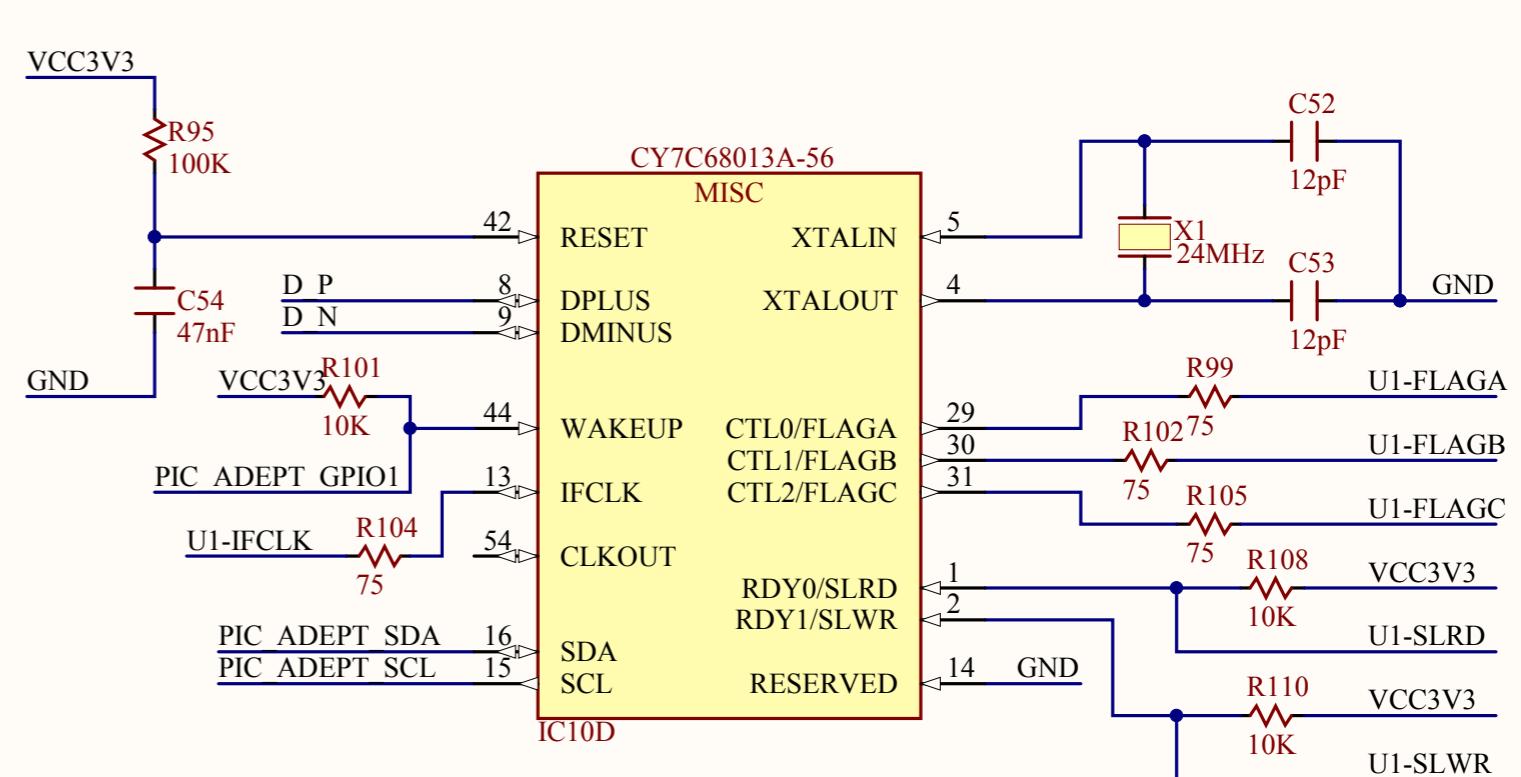
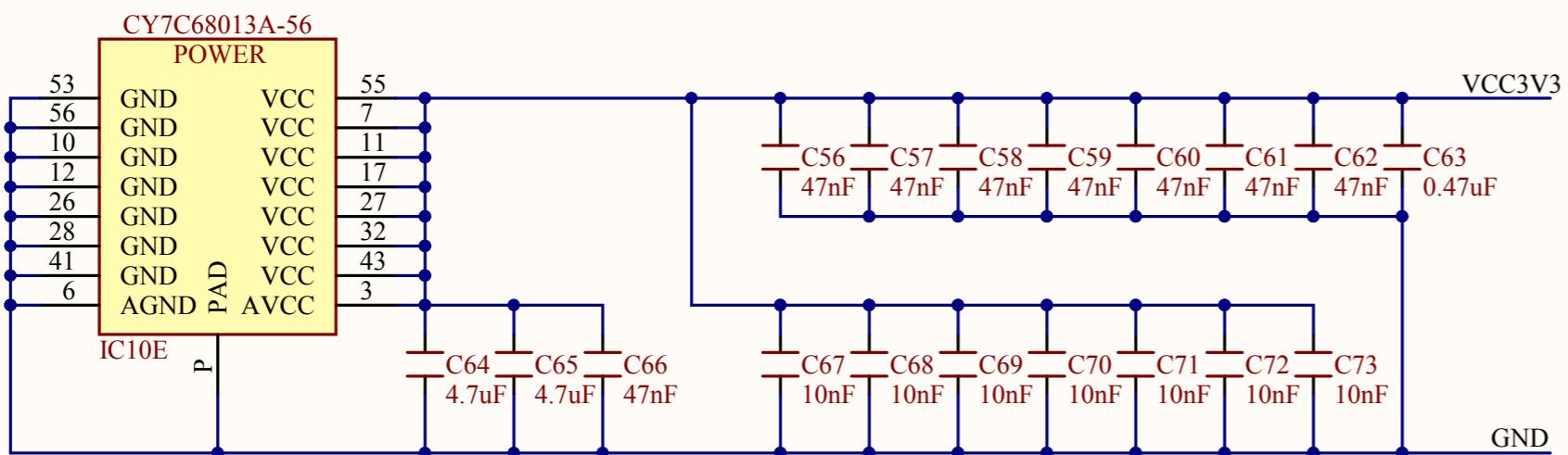
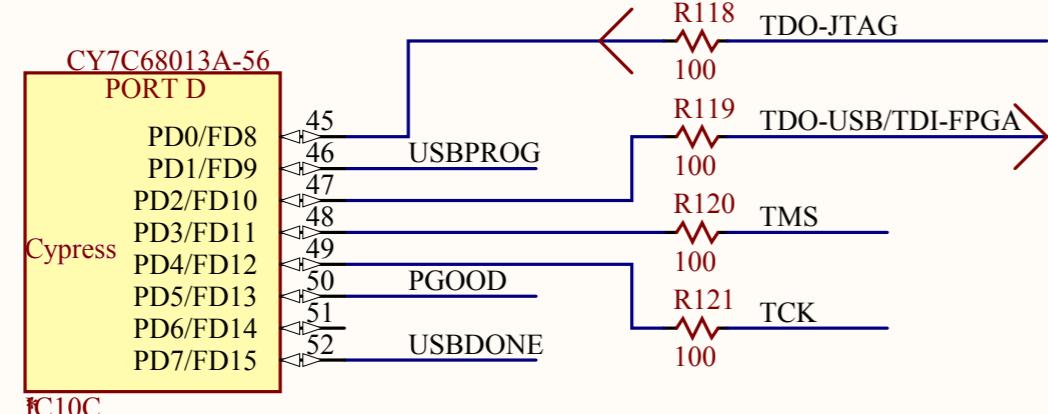
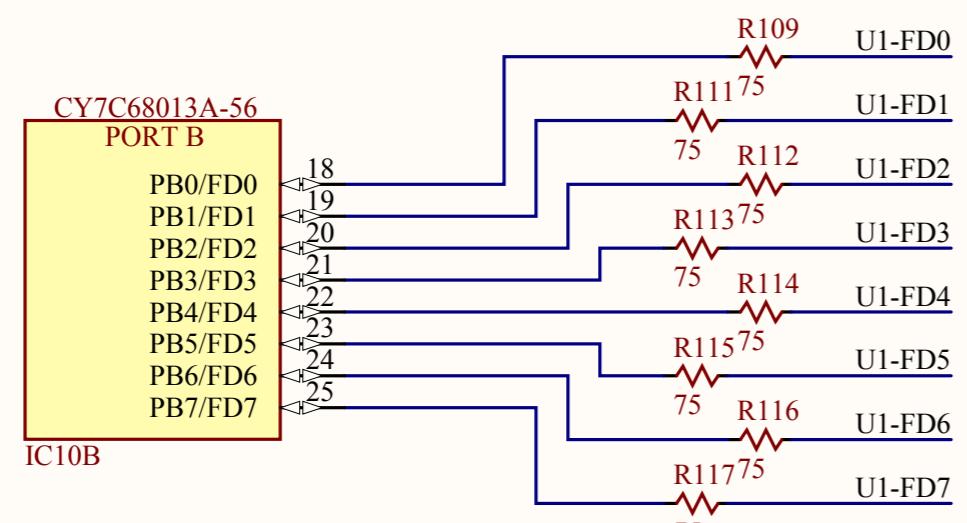
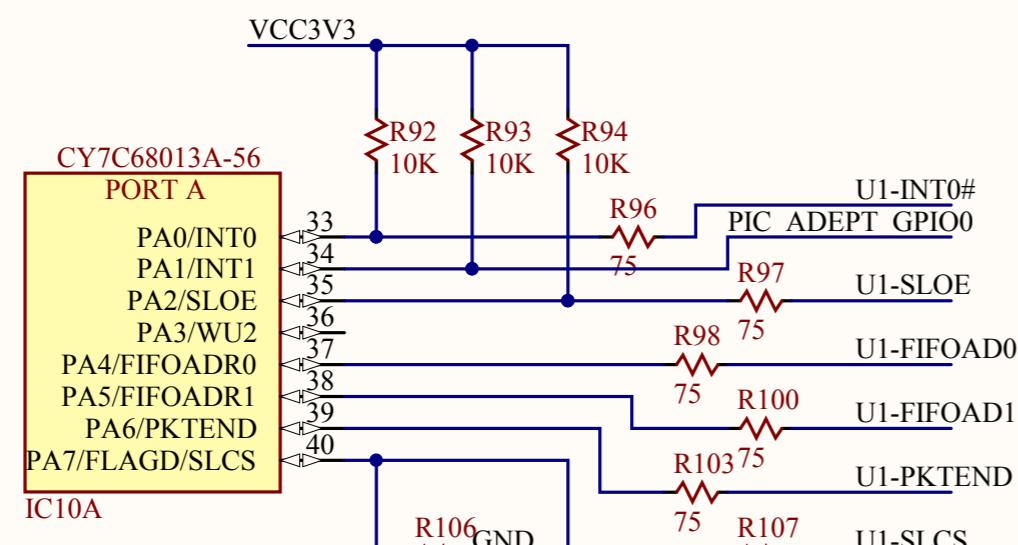
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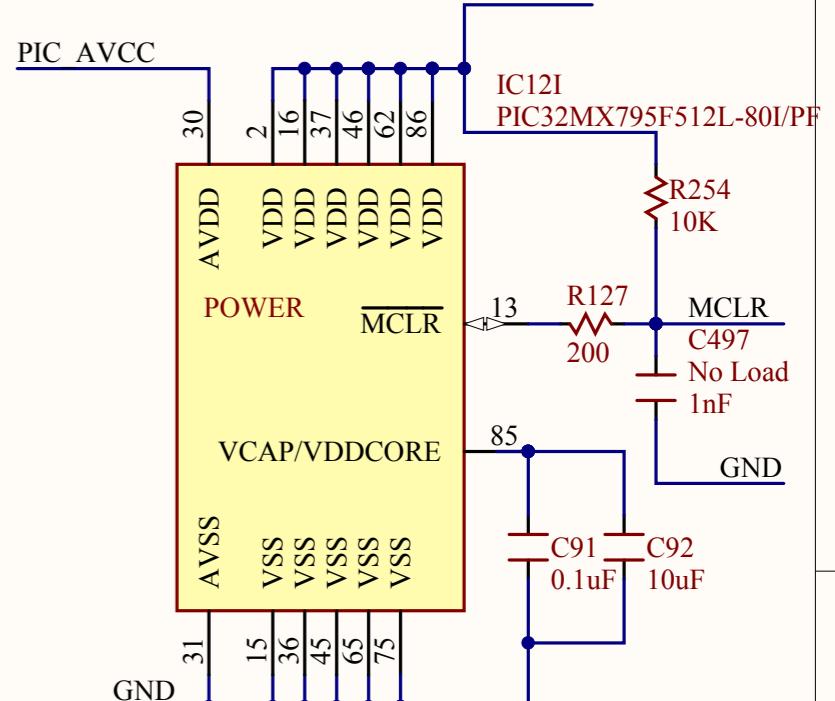
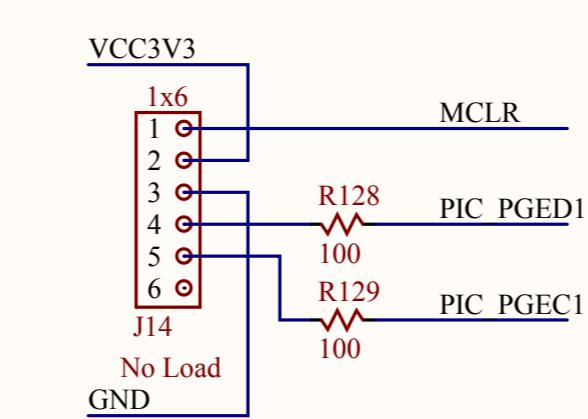
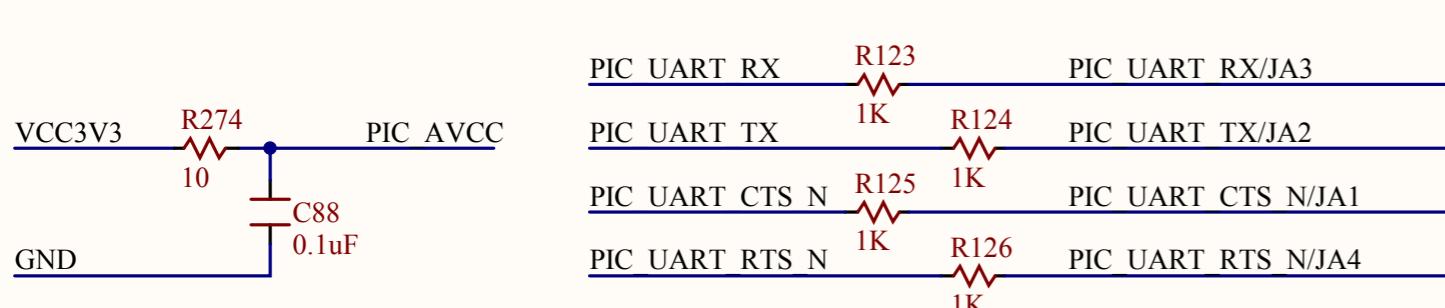
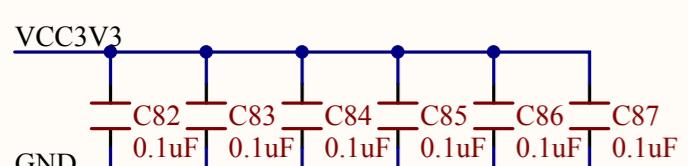
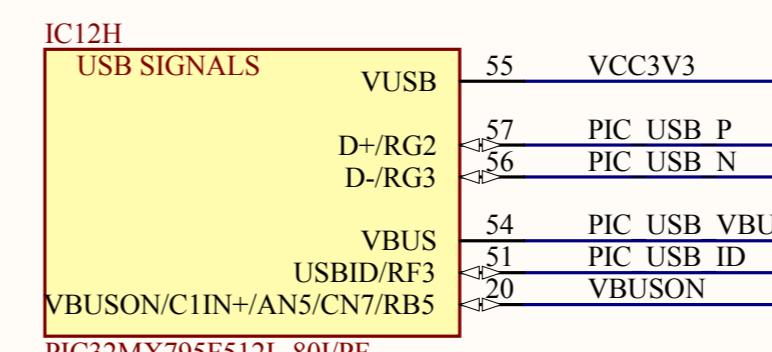
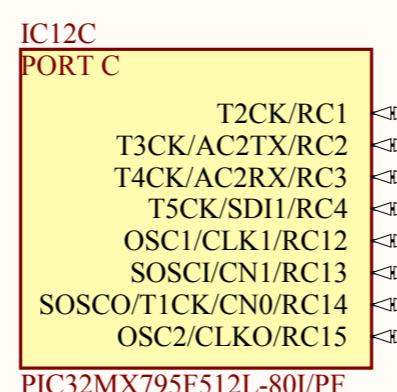
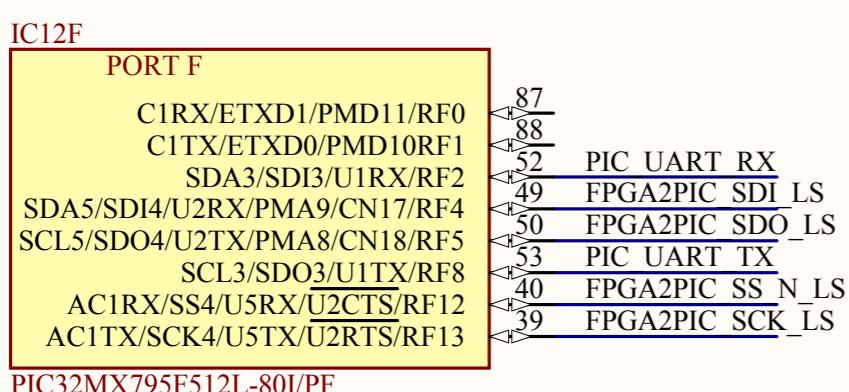
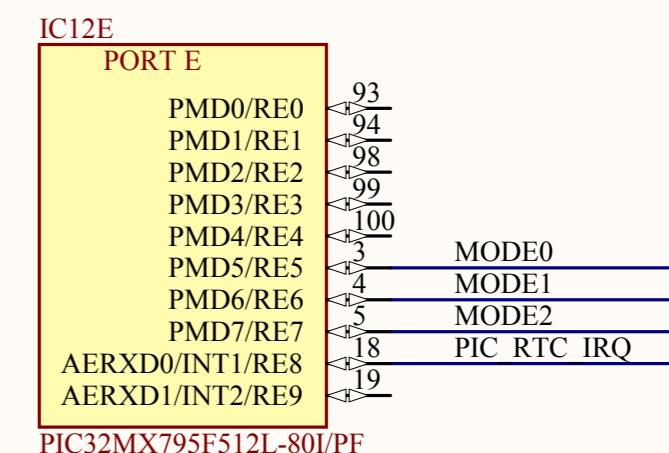
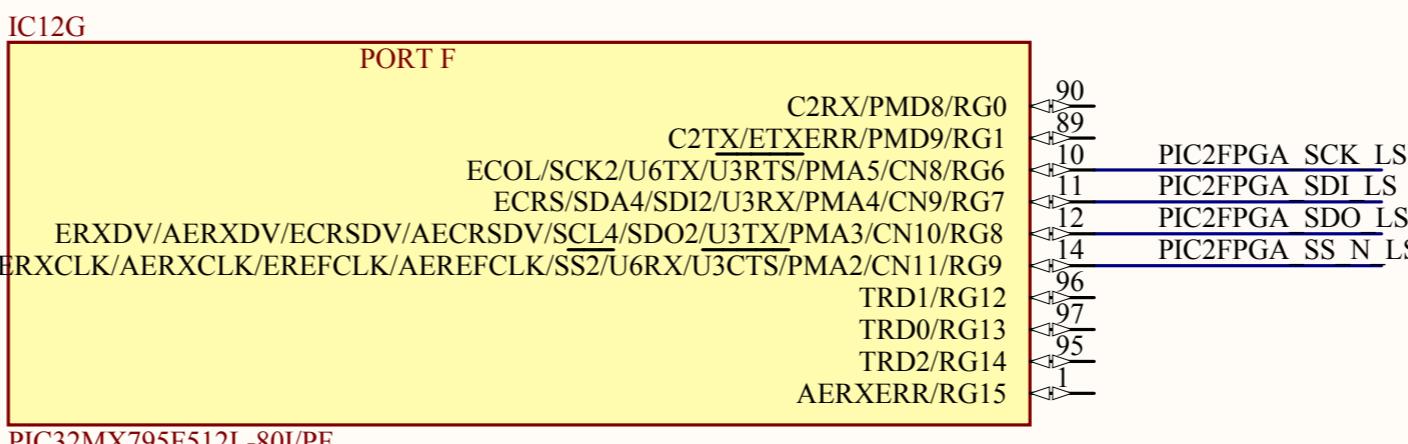
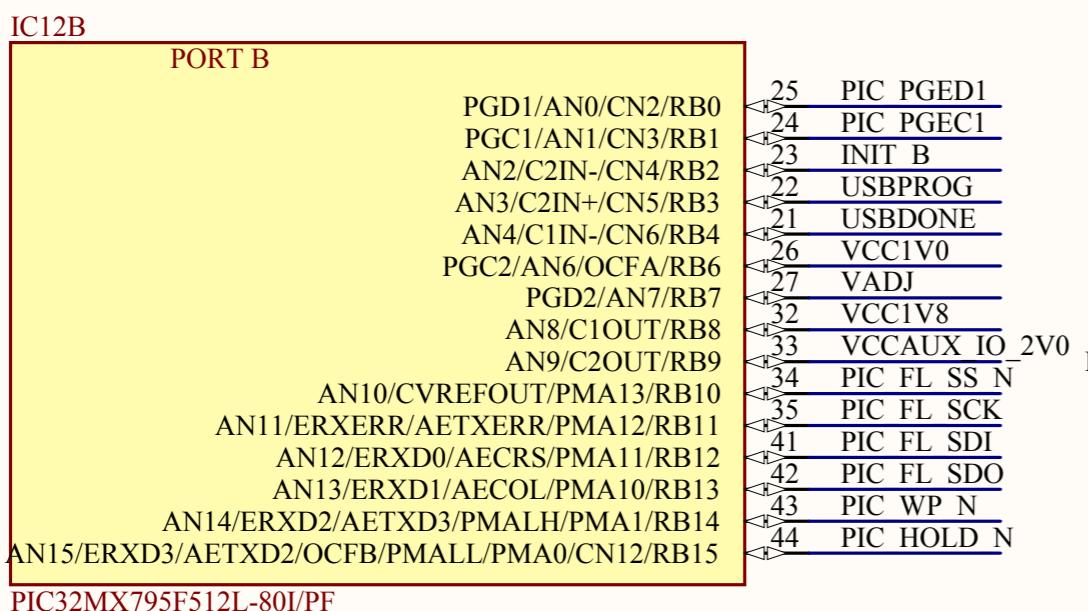
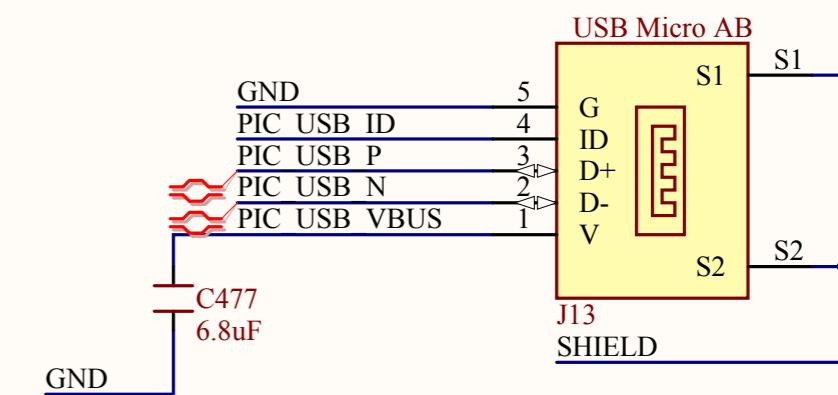
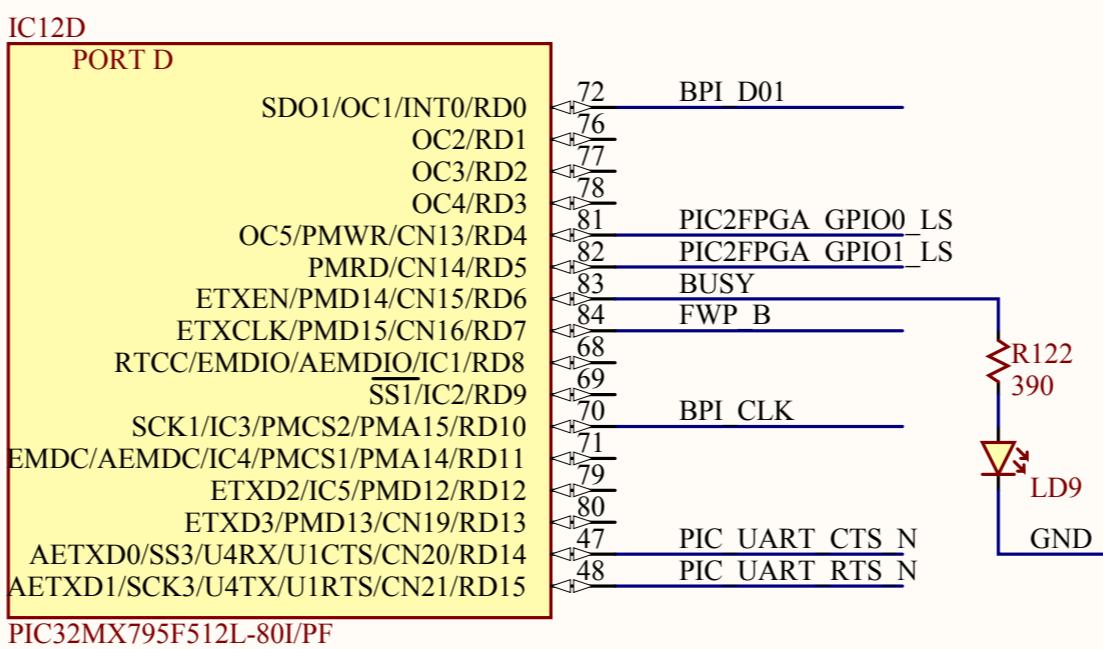
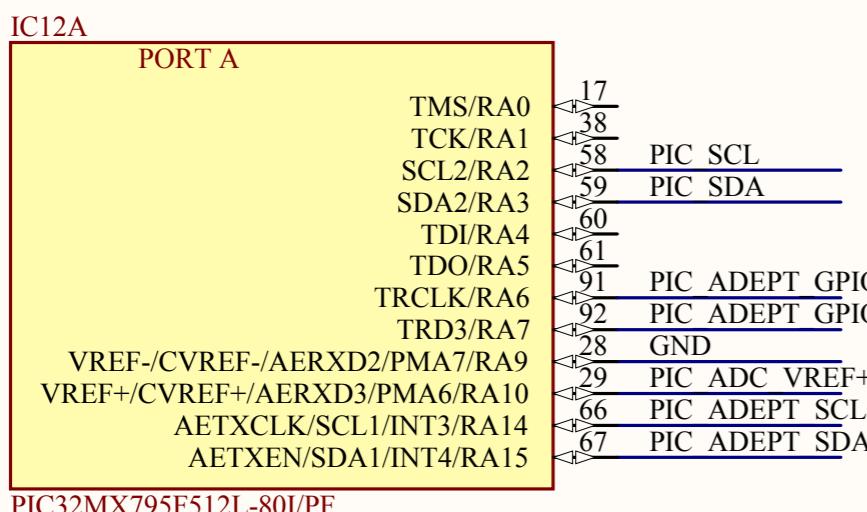




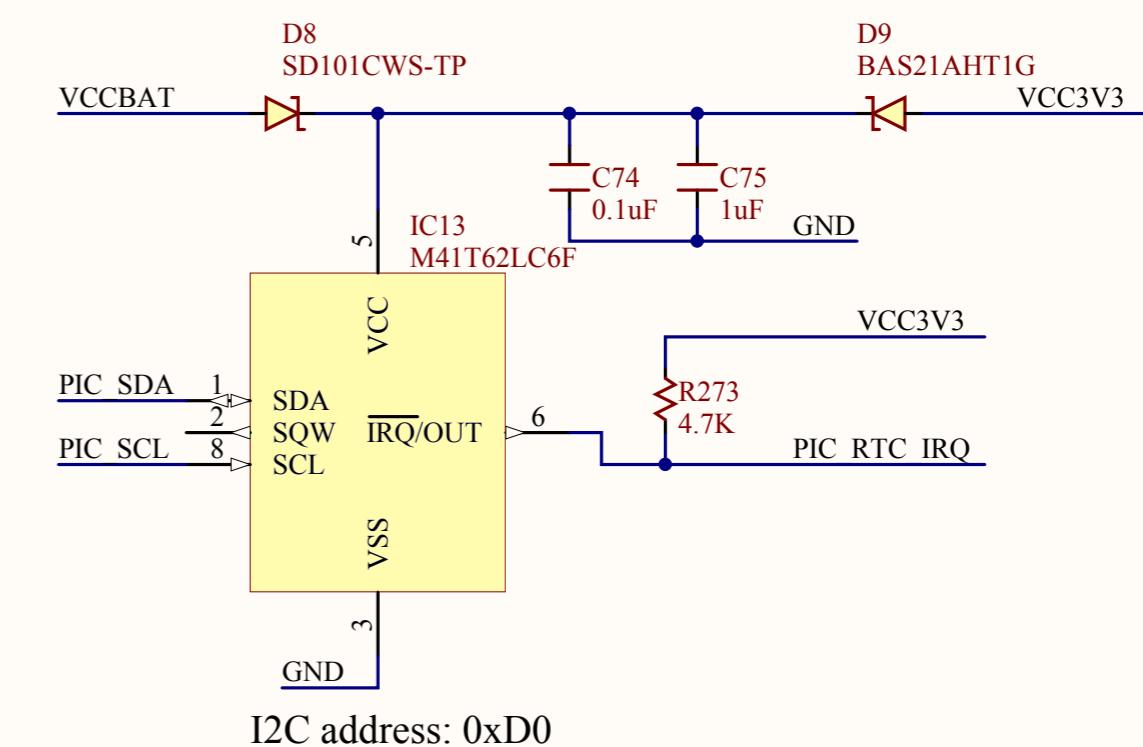
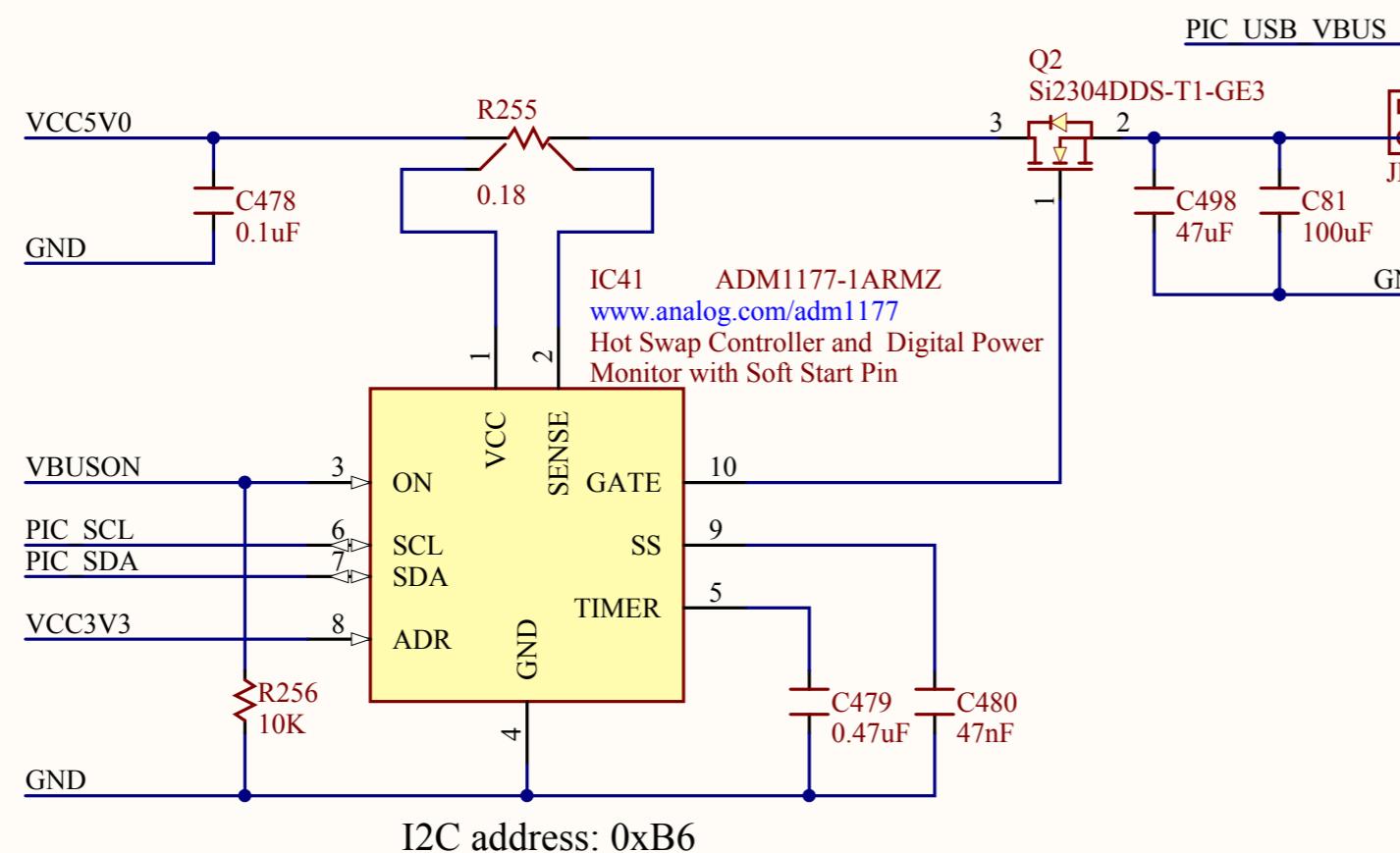




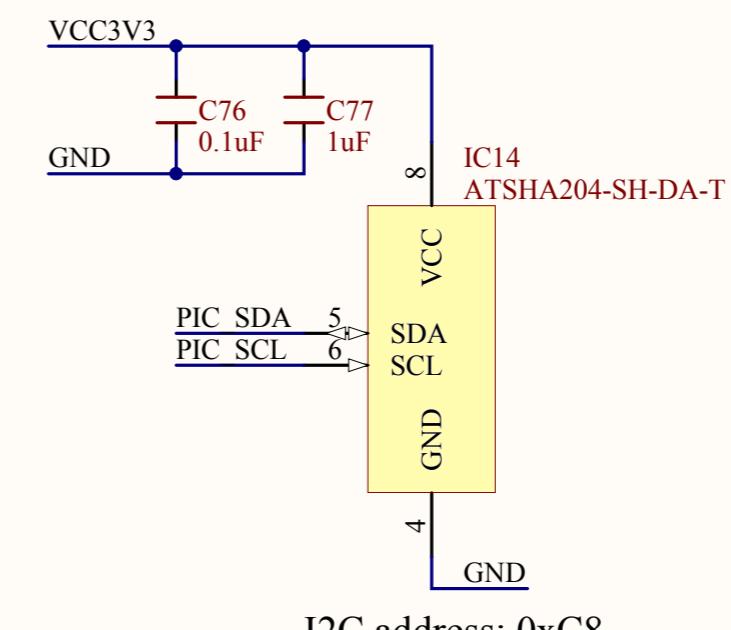
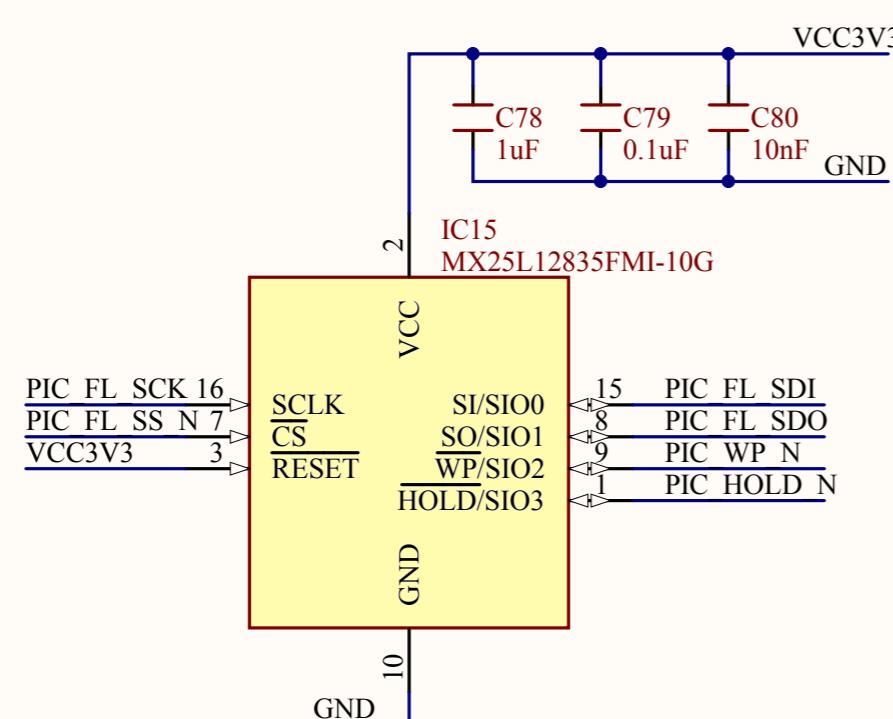




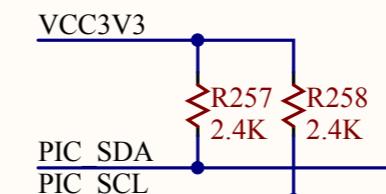
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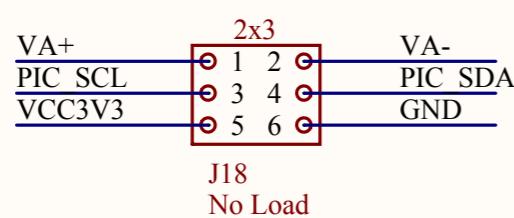
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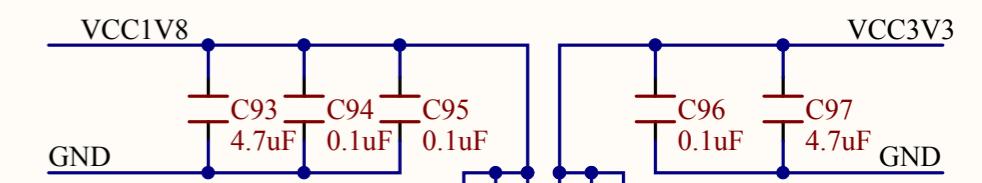
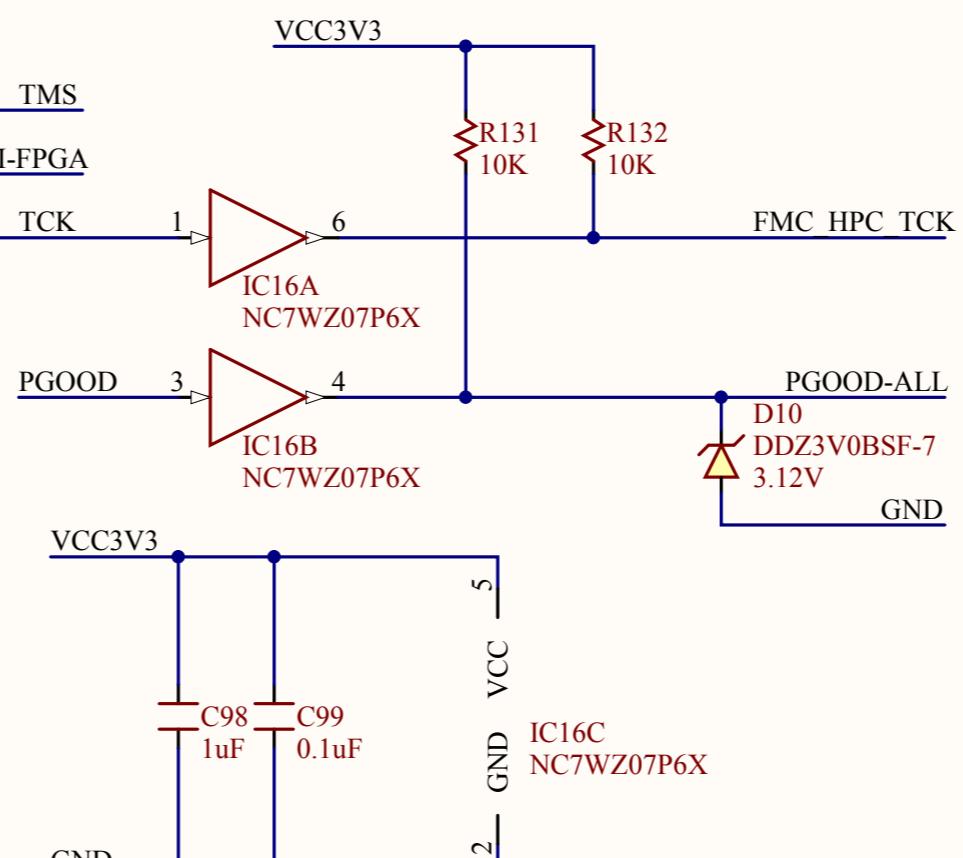
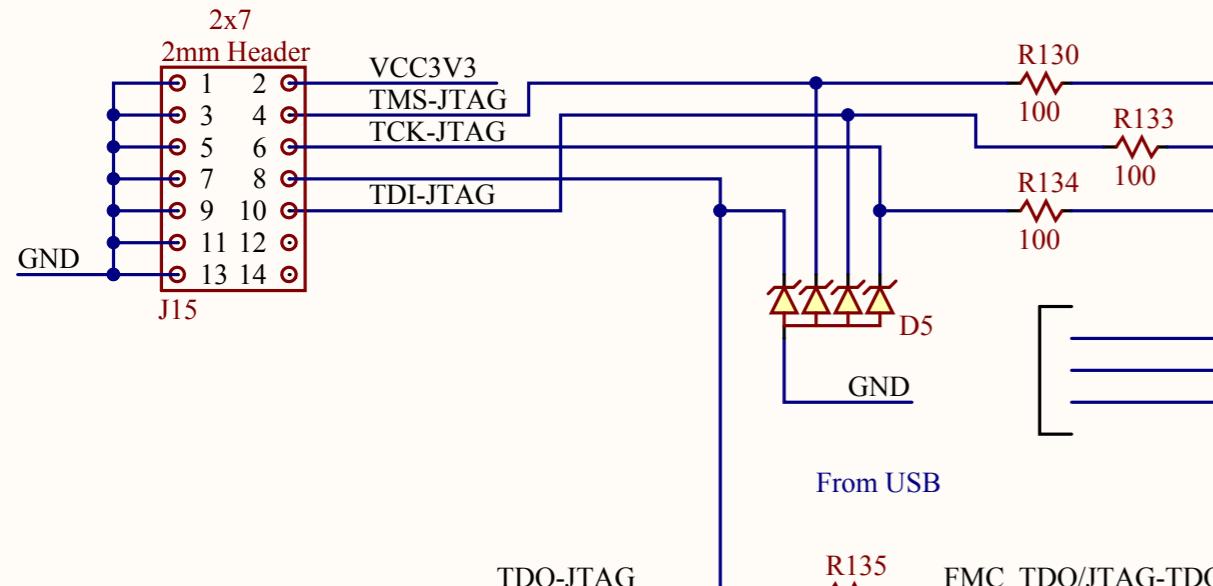
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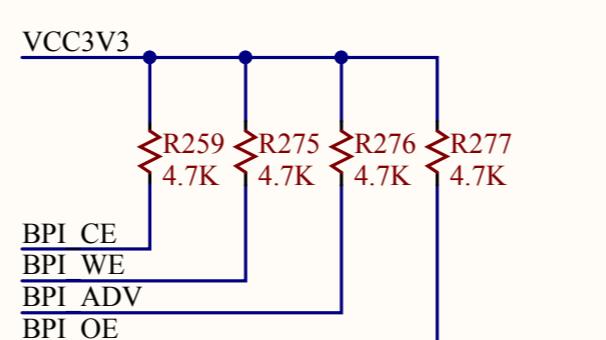
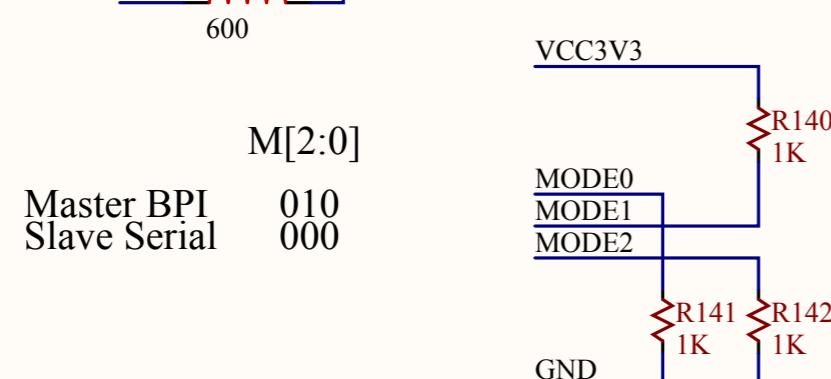
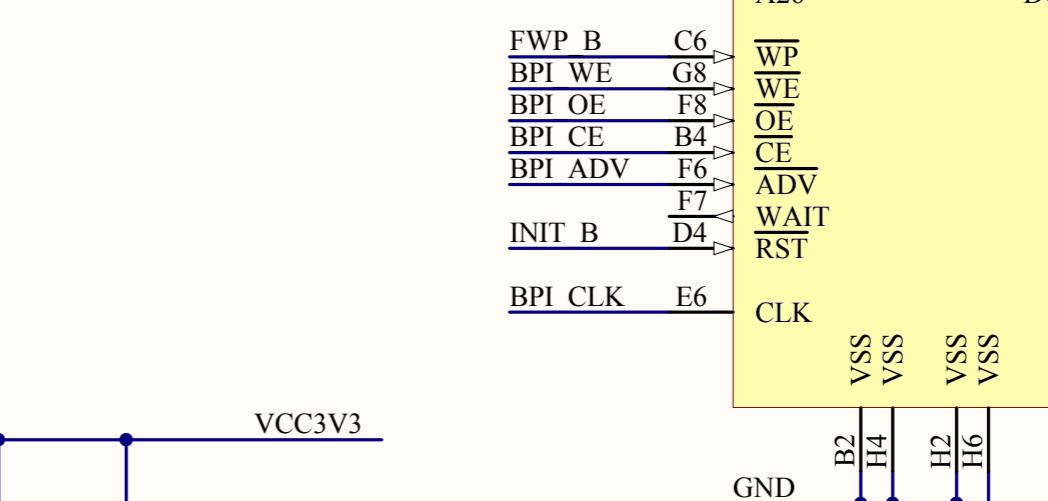
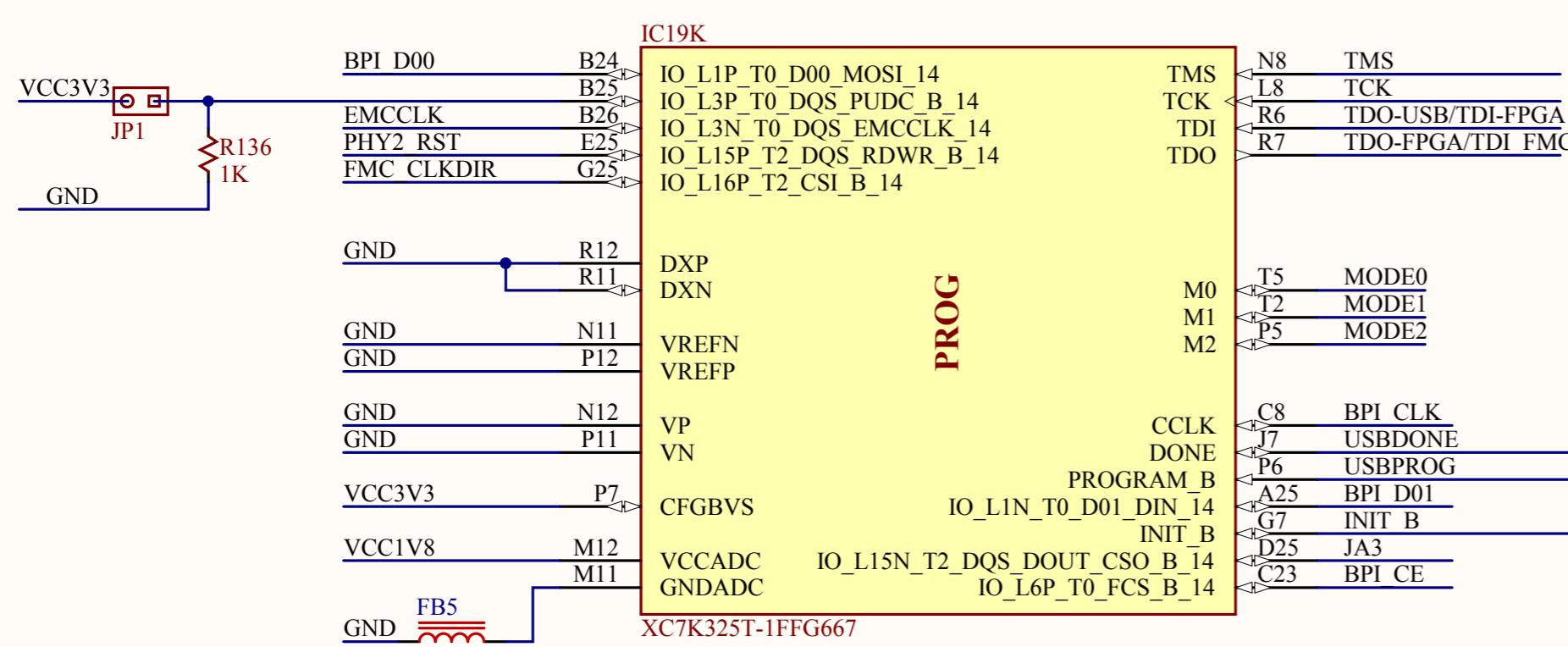
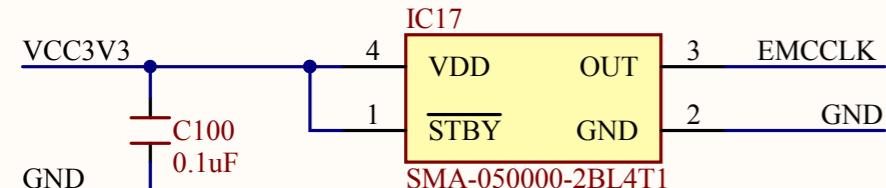


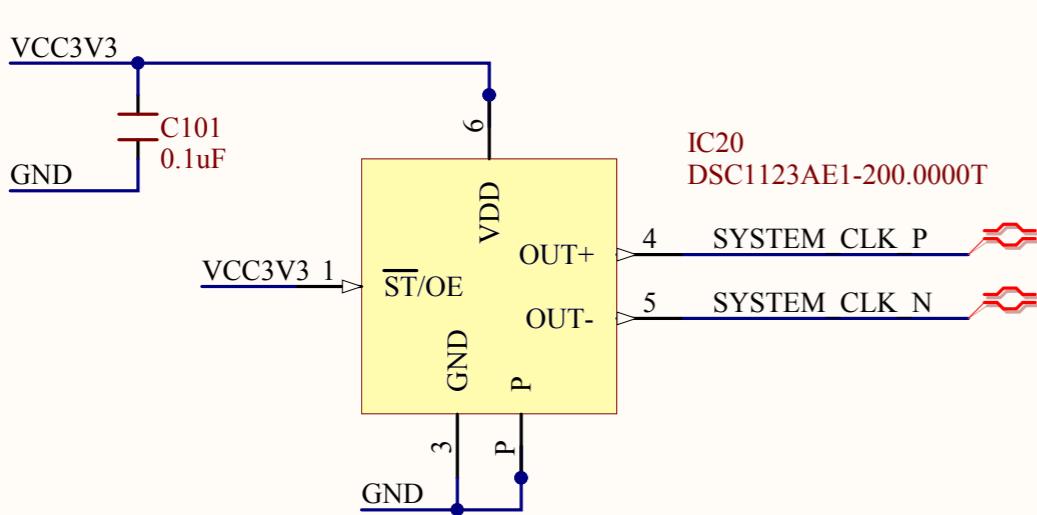
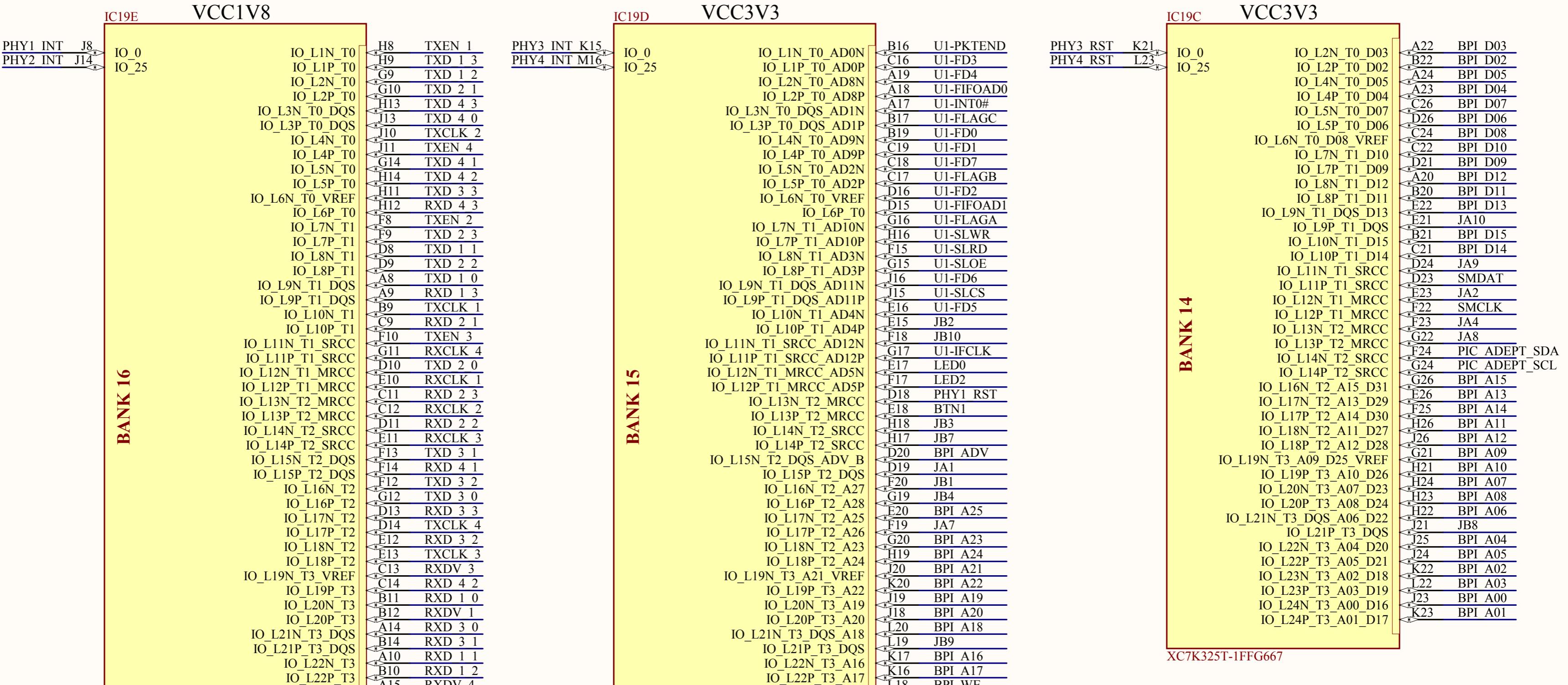
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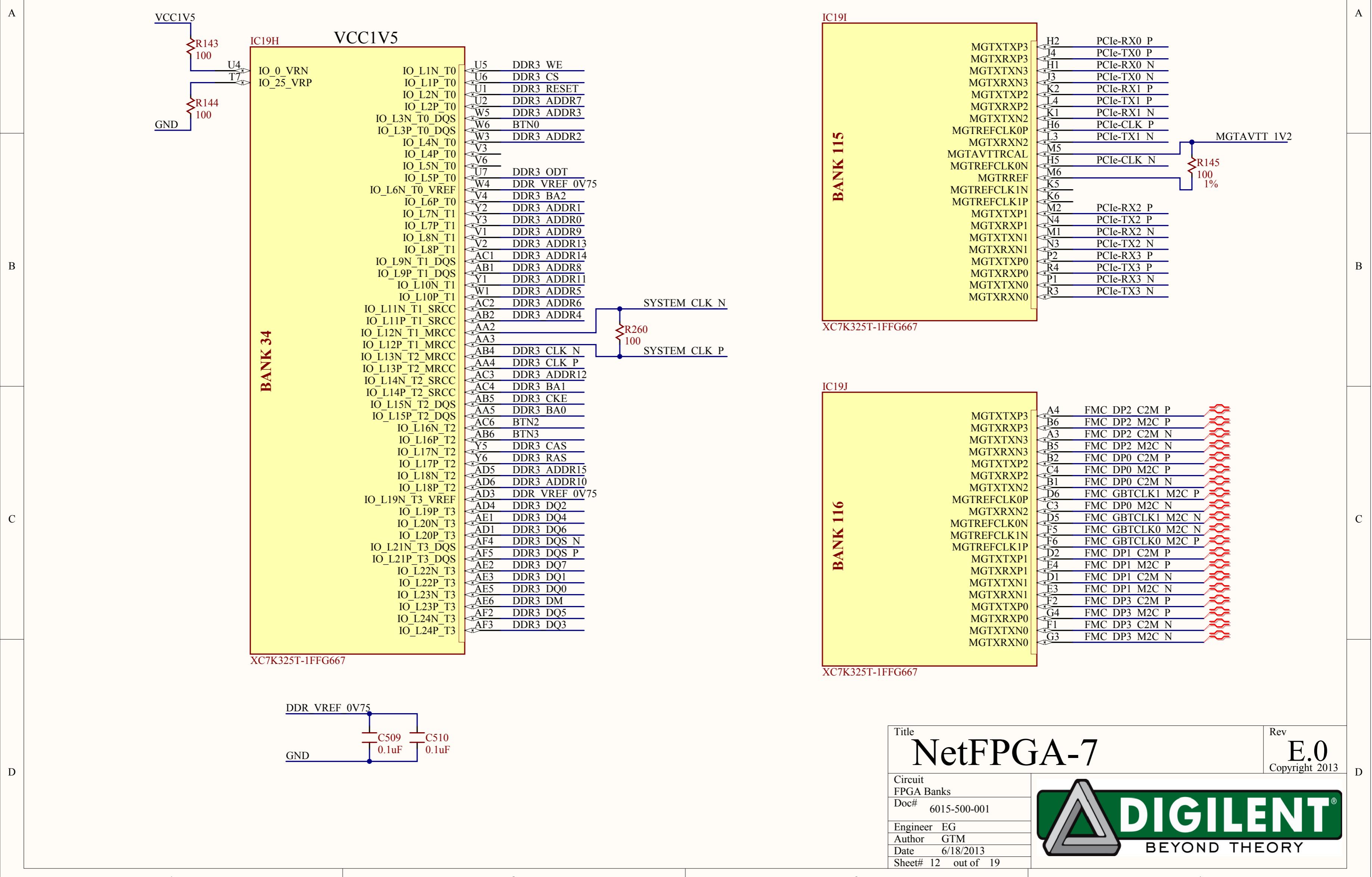


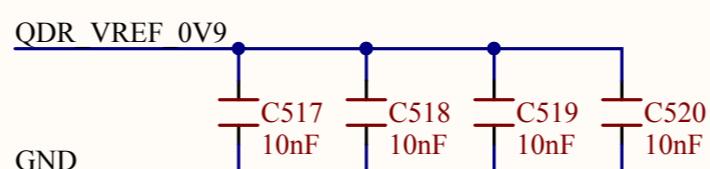
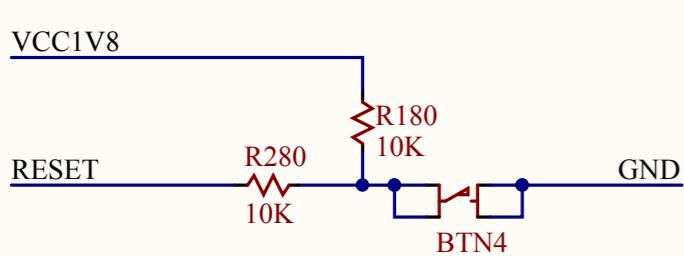
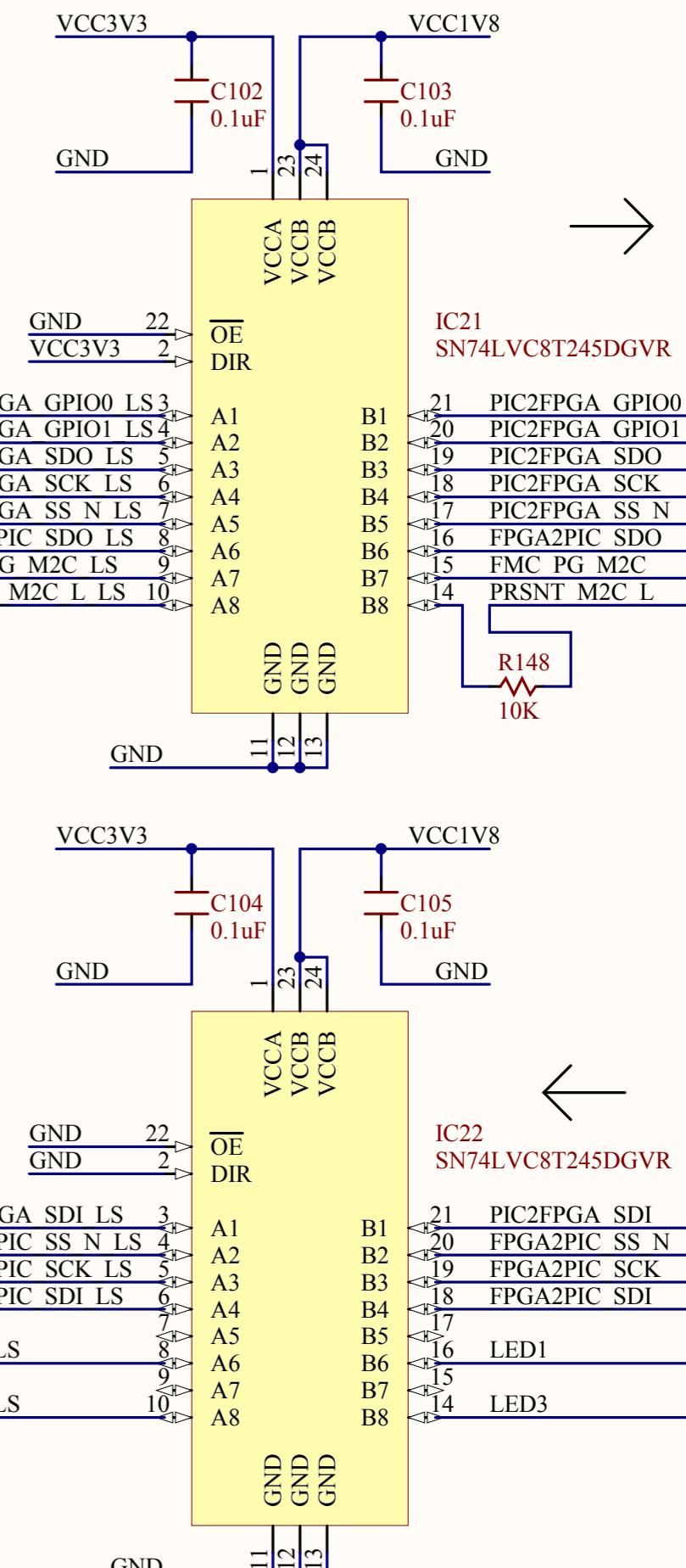
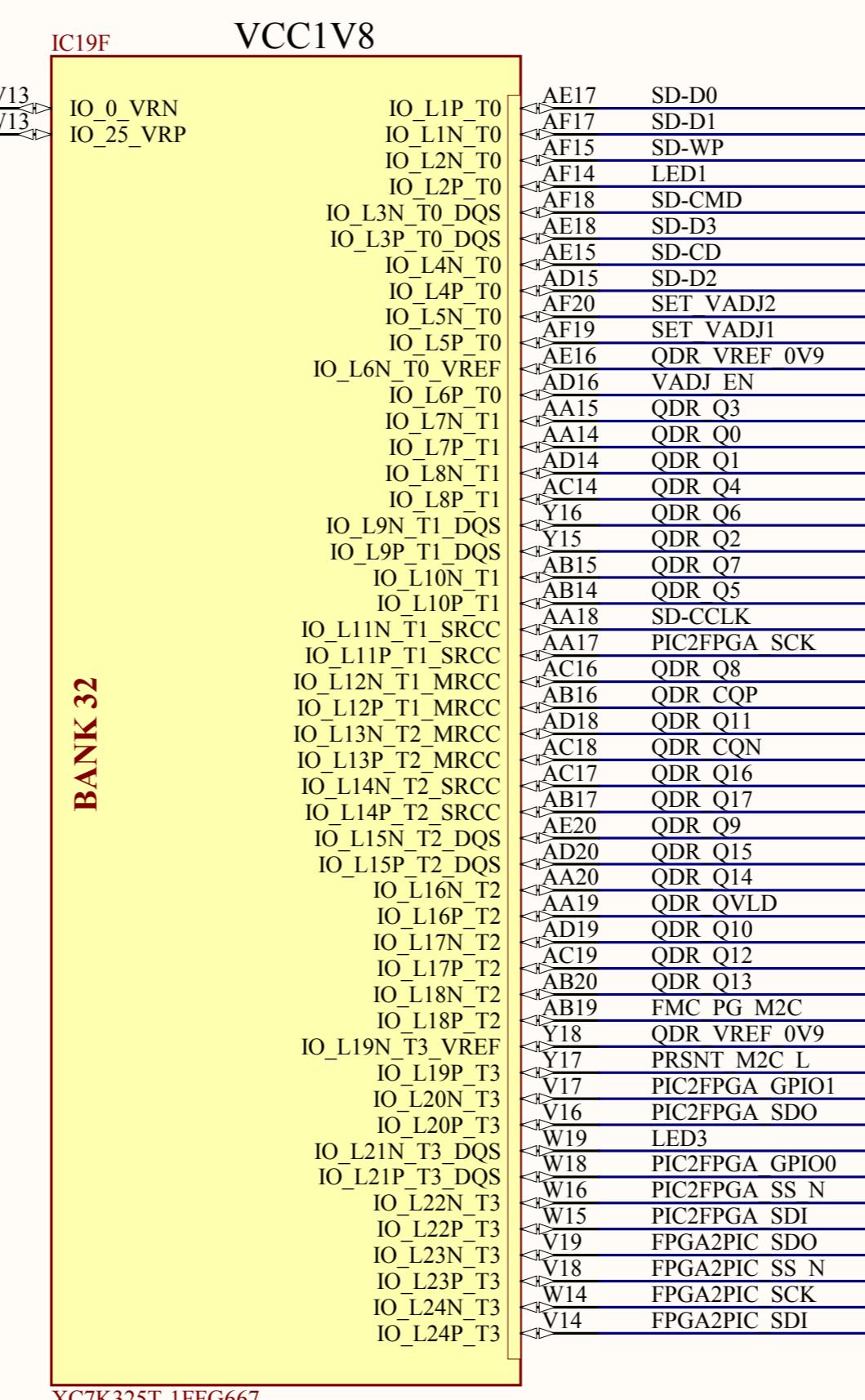
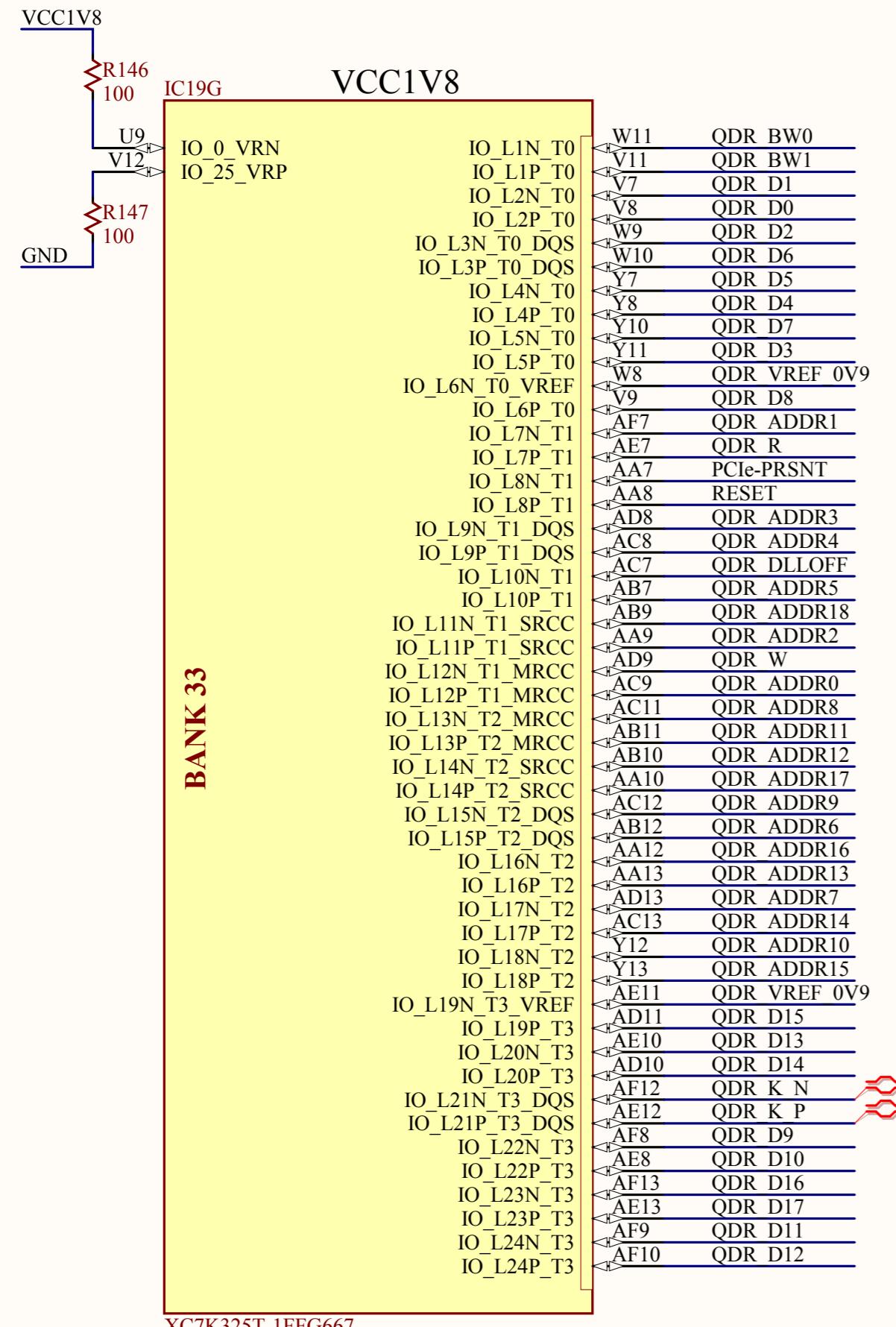
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BPI A10	D3	A11
BPI A11	C4	A12
BPI A12	A5	A13
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BPI A21	A8	A22
BPI A22	G1	A23
BPI A23	H8	A24
BPI A24	B6	A25
BPI A25	B8	A26
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BPI WE	G8	WE
BPI OE	F8	OE
BPI CE	B4	CE
BPI ADV	F6	ADV
INIT B	D4	WAIT
BPI CLK	E6	CLK

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E2	BPI D01
G3	BPI D02
E4	BPI D03
DQ1	
E5	BPI D04
G5	BPI D05
G6	BPI D06
H7	BPI D07
E1	BPI D08
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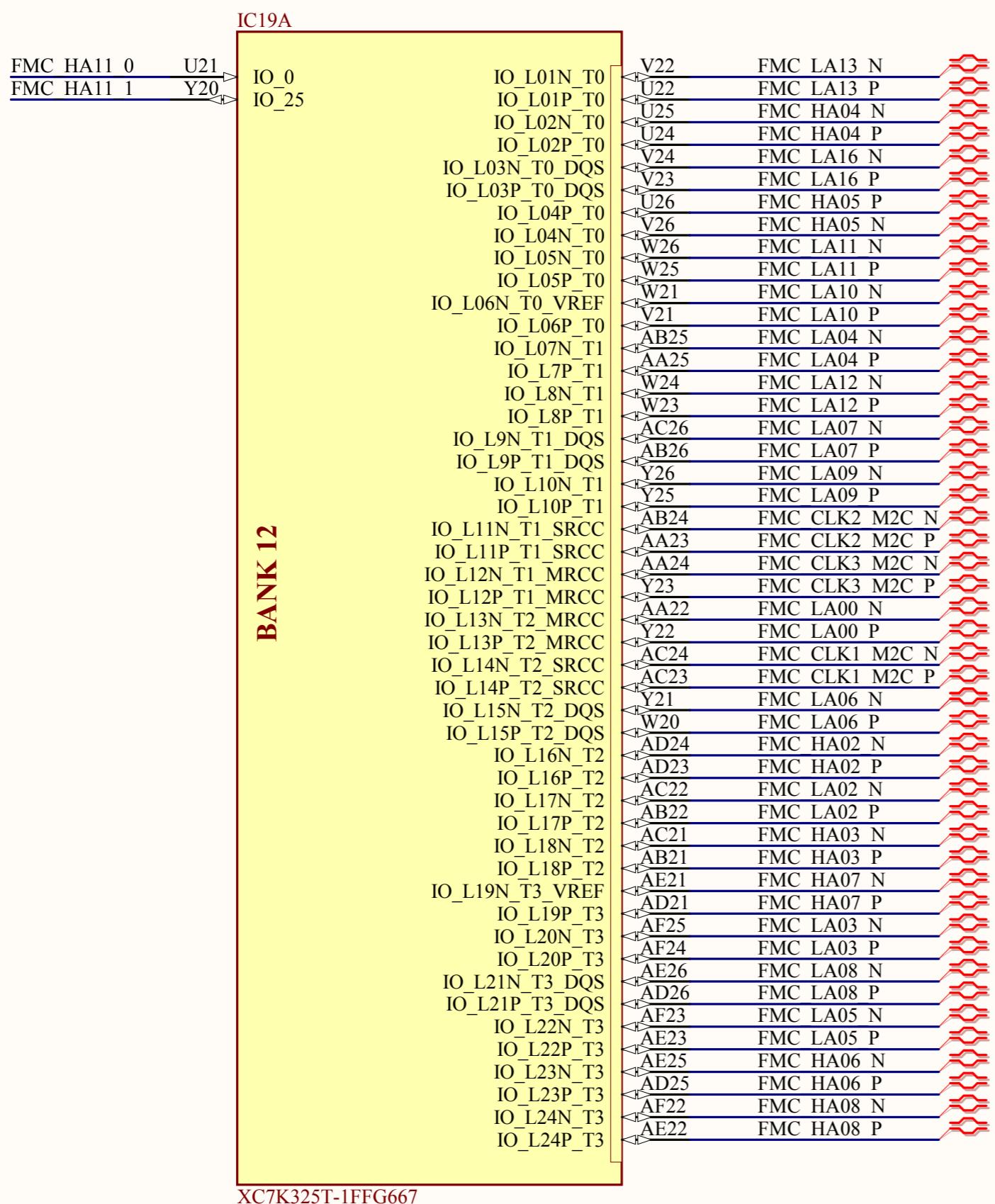




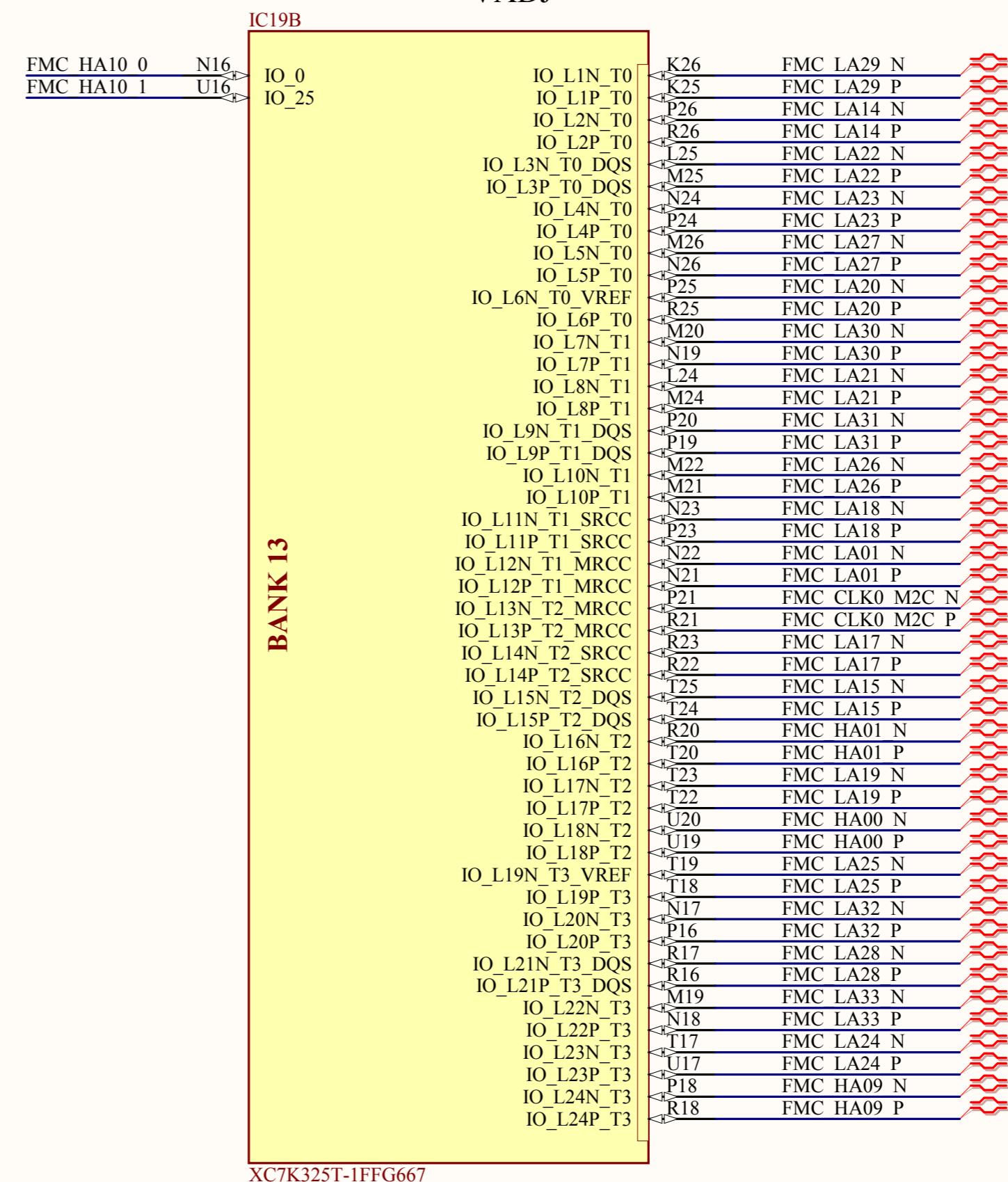


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VADJ



VADJ



Title

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FPGA Banks
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Author GTM
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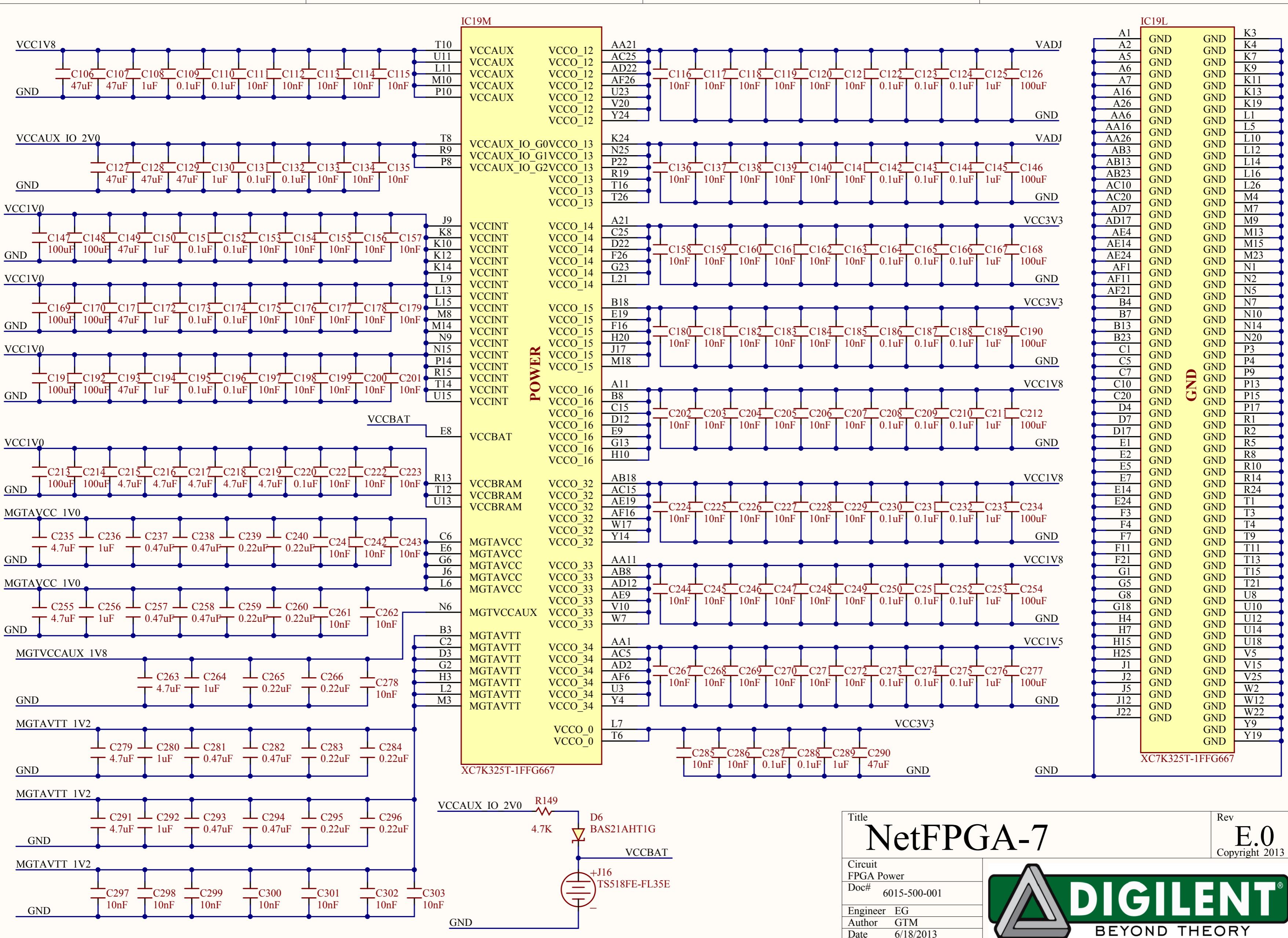


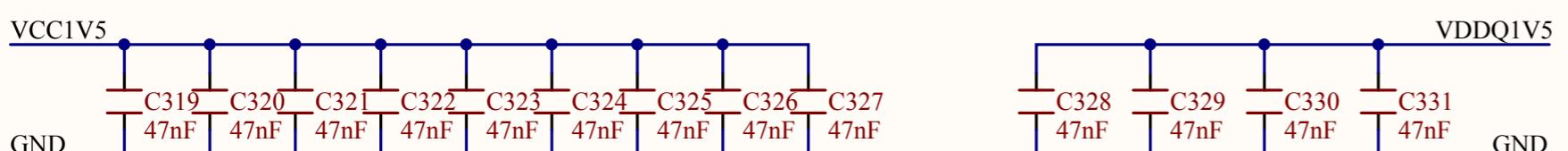
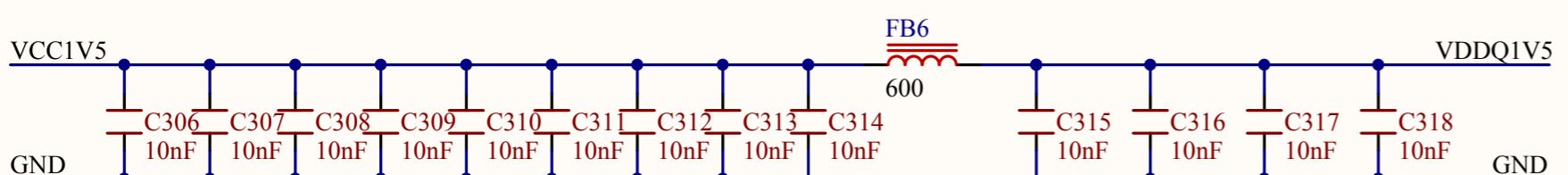
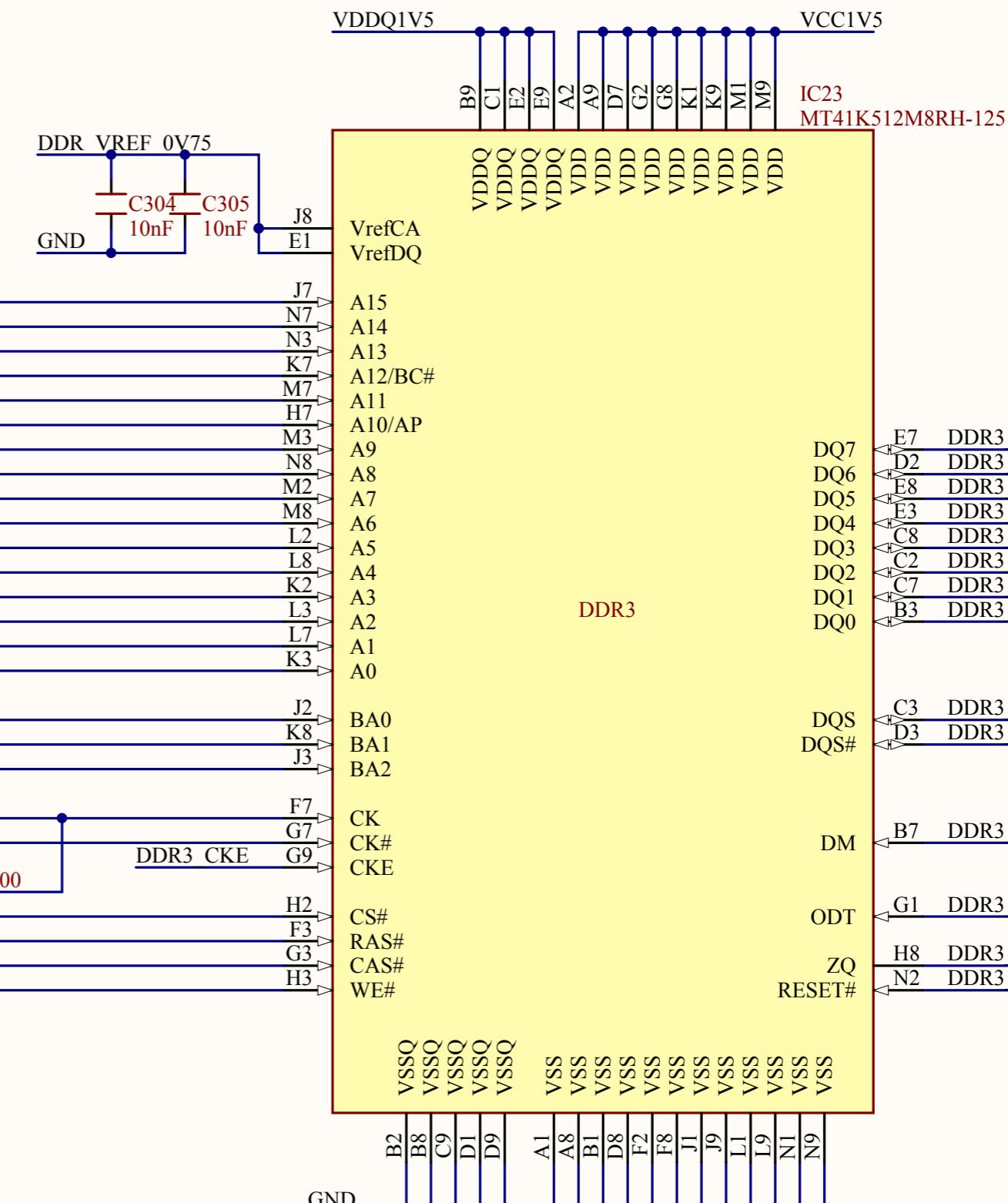
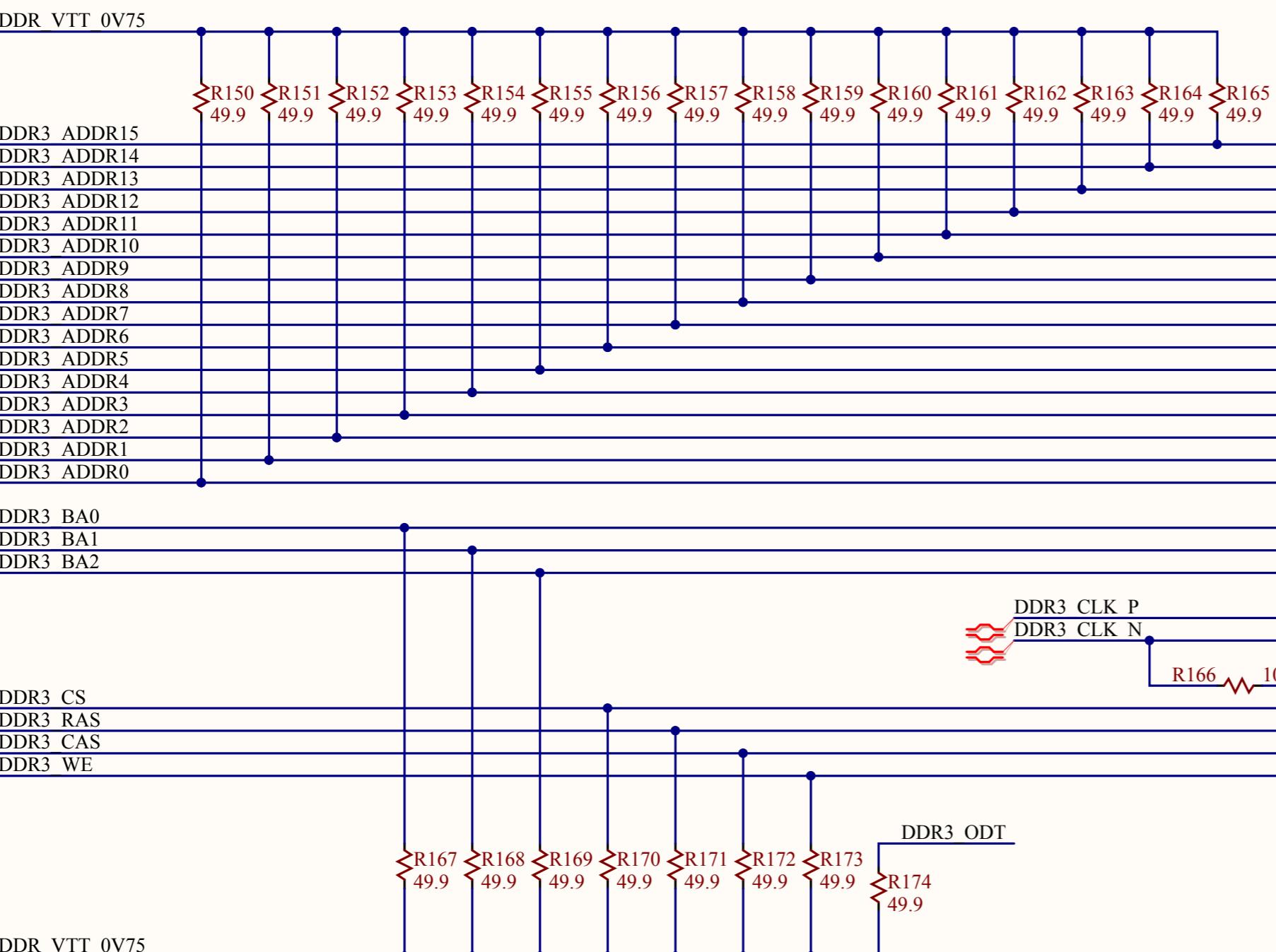
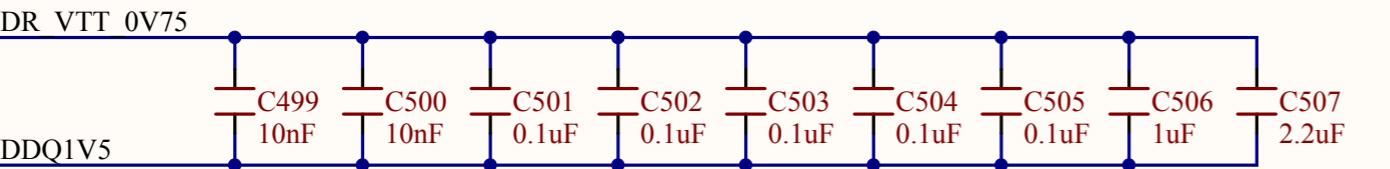
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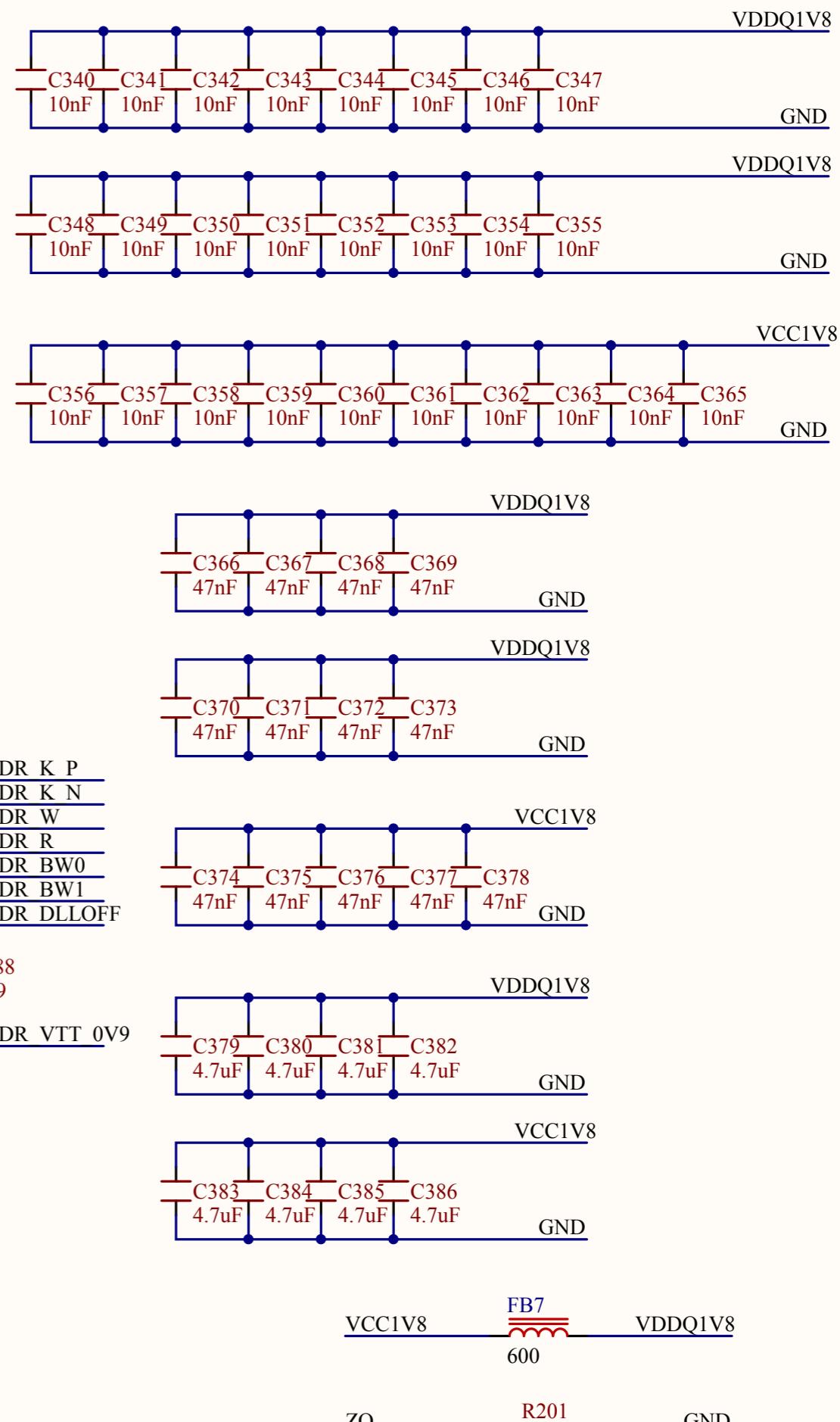
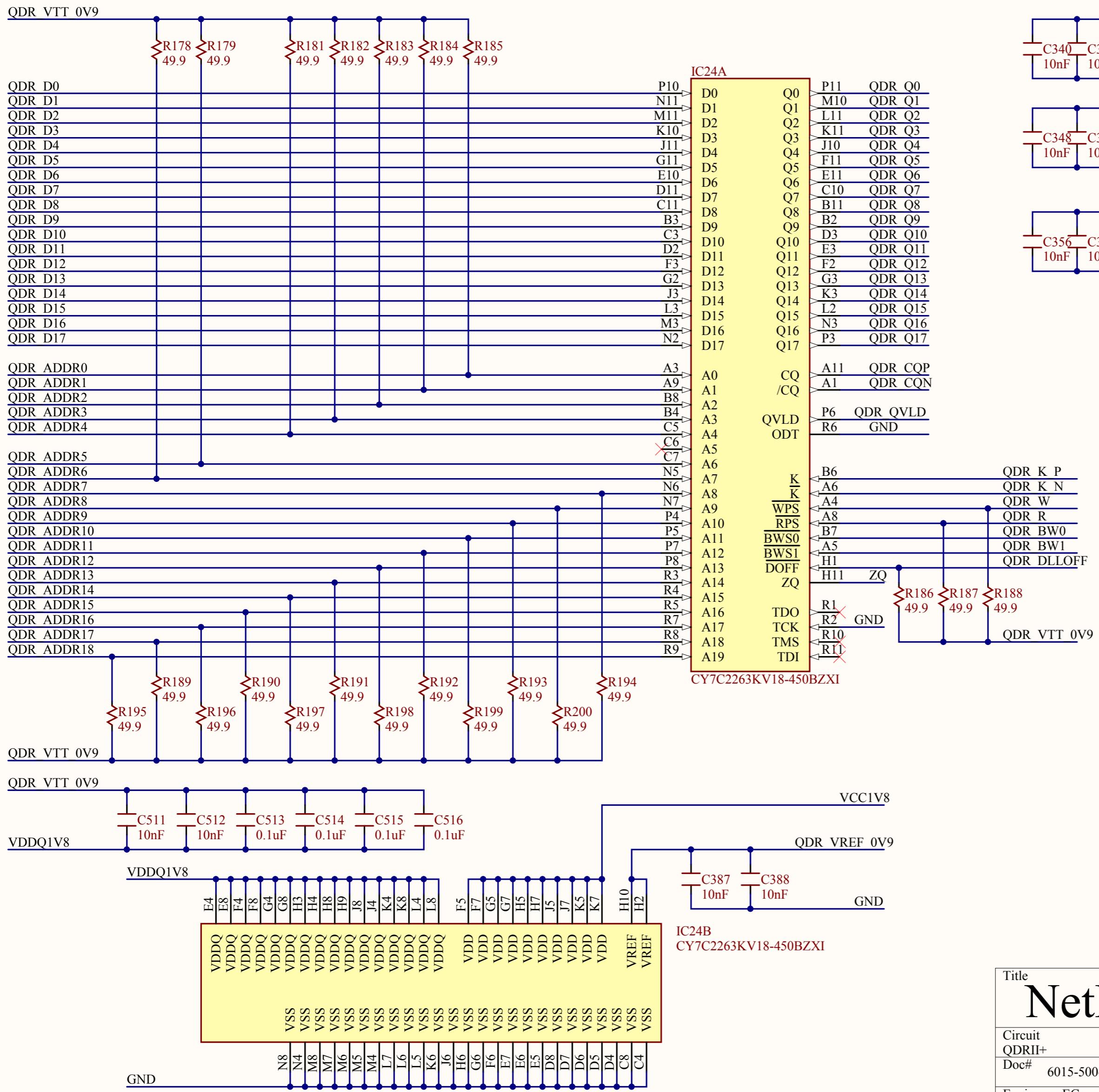
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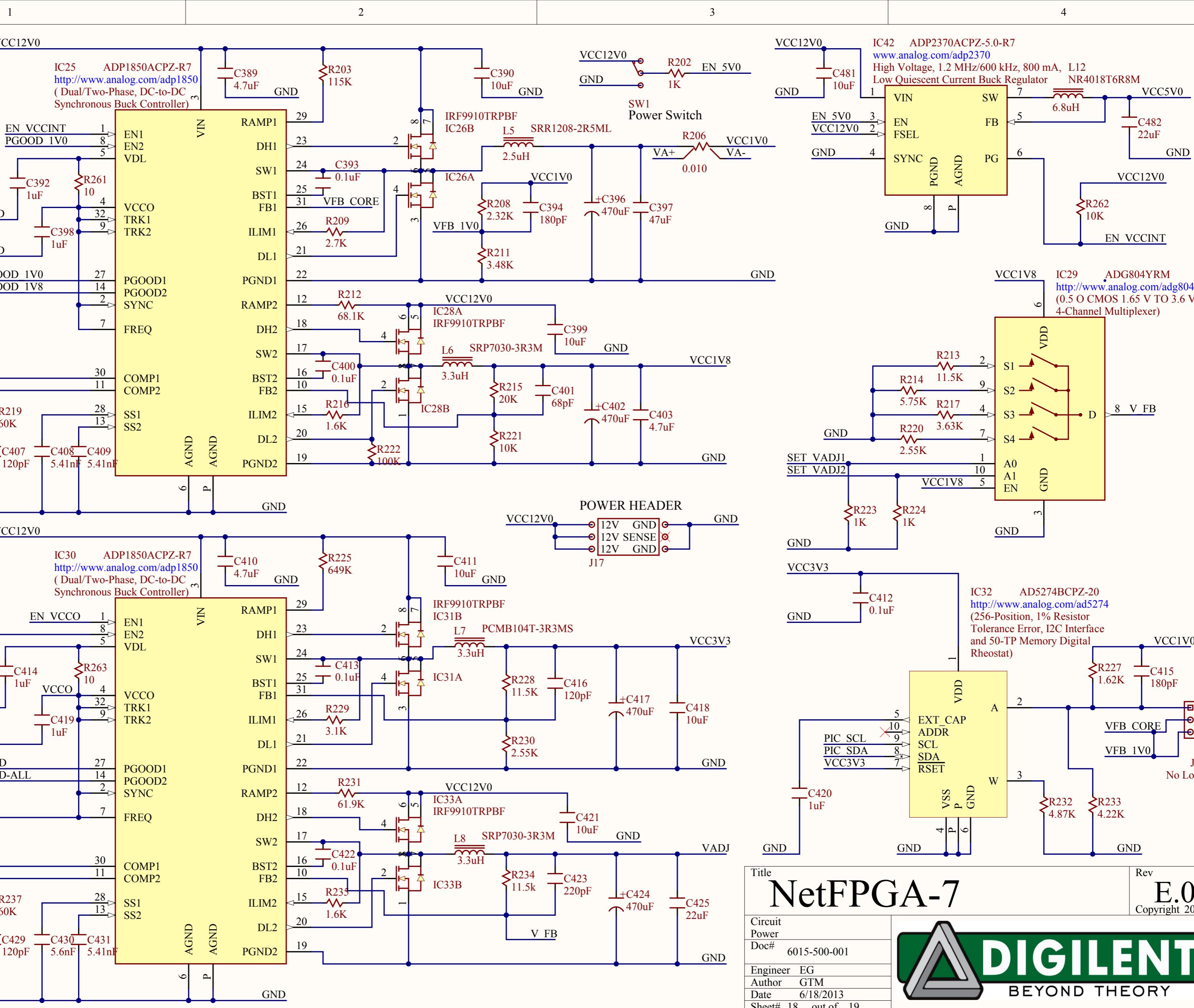




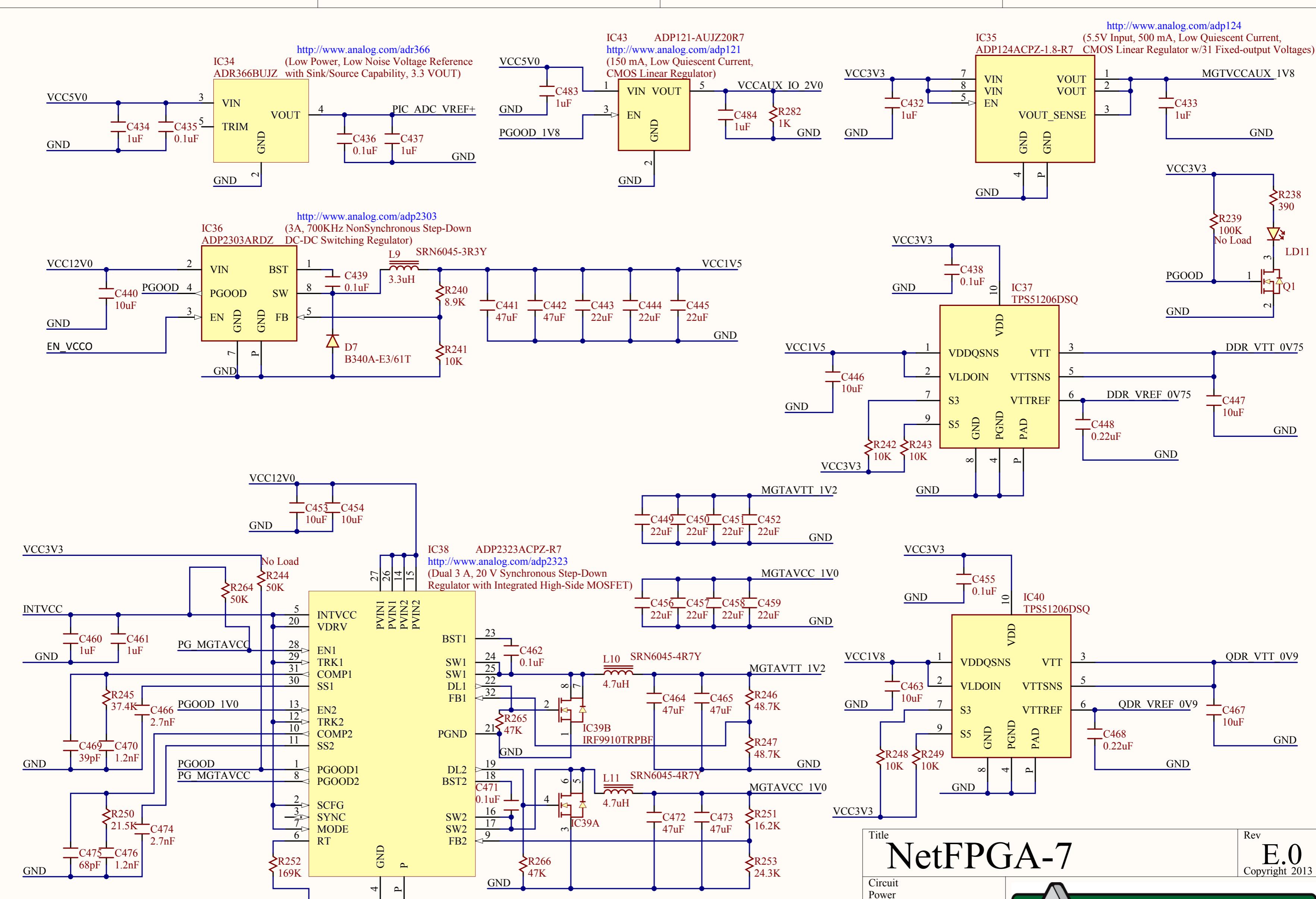
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Doc#	6015-500-001	
Engineer	EG	
Author	GTM	
Date	6/18/2013	
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<http://www.analog.com/adp124ACPZ-1.8-R7>
 (5.5V Input, 500 mA, Low Quiescent Current,
 CMOS Linear Regulator w/31 Fixed-output Voltages)

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