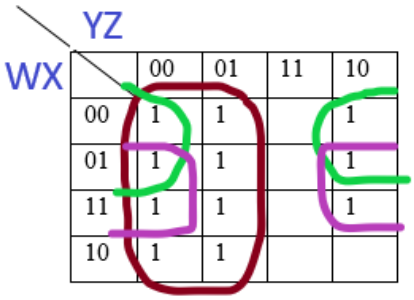
REPORT

1)F (w , x , y , z) = $\sum(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$

A)Truth Table

W	X	Y	Z	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

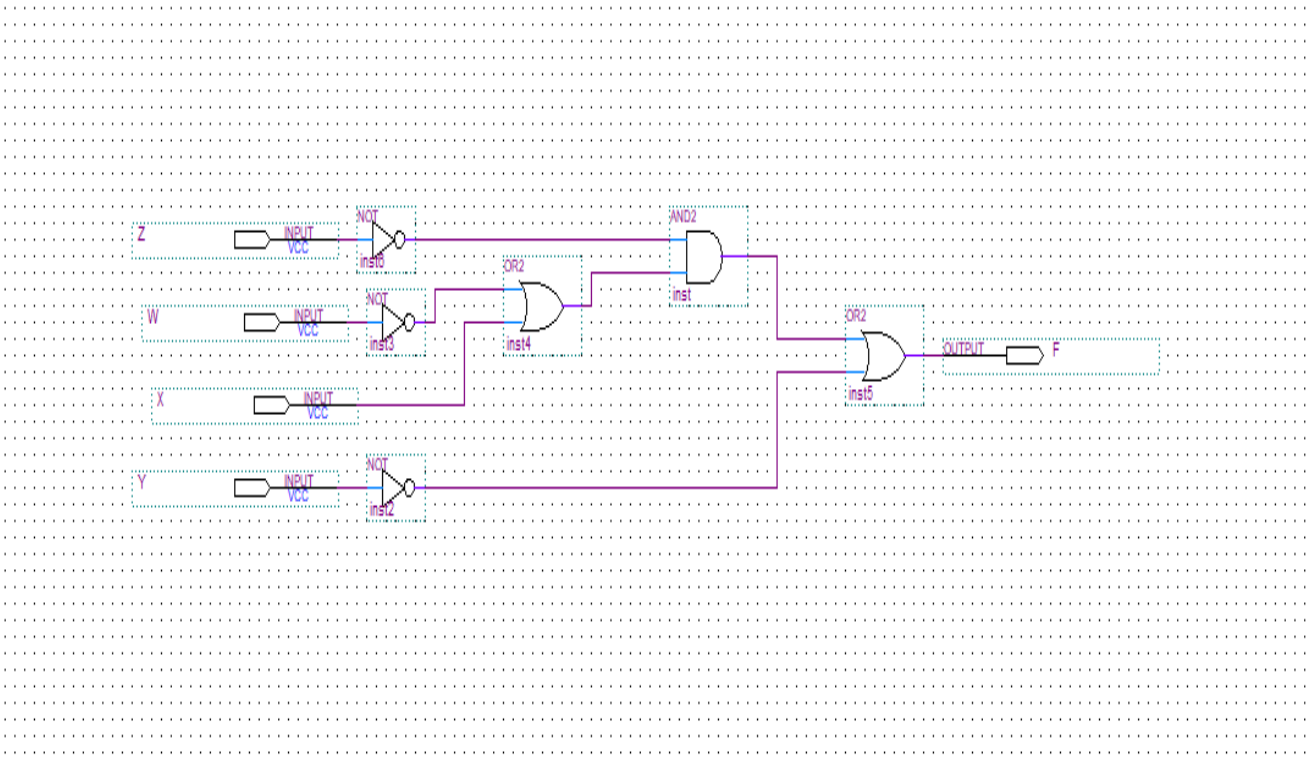
Karnaugh map.



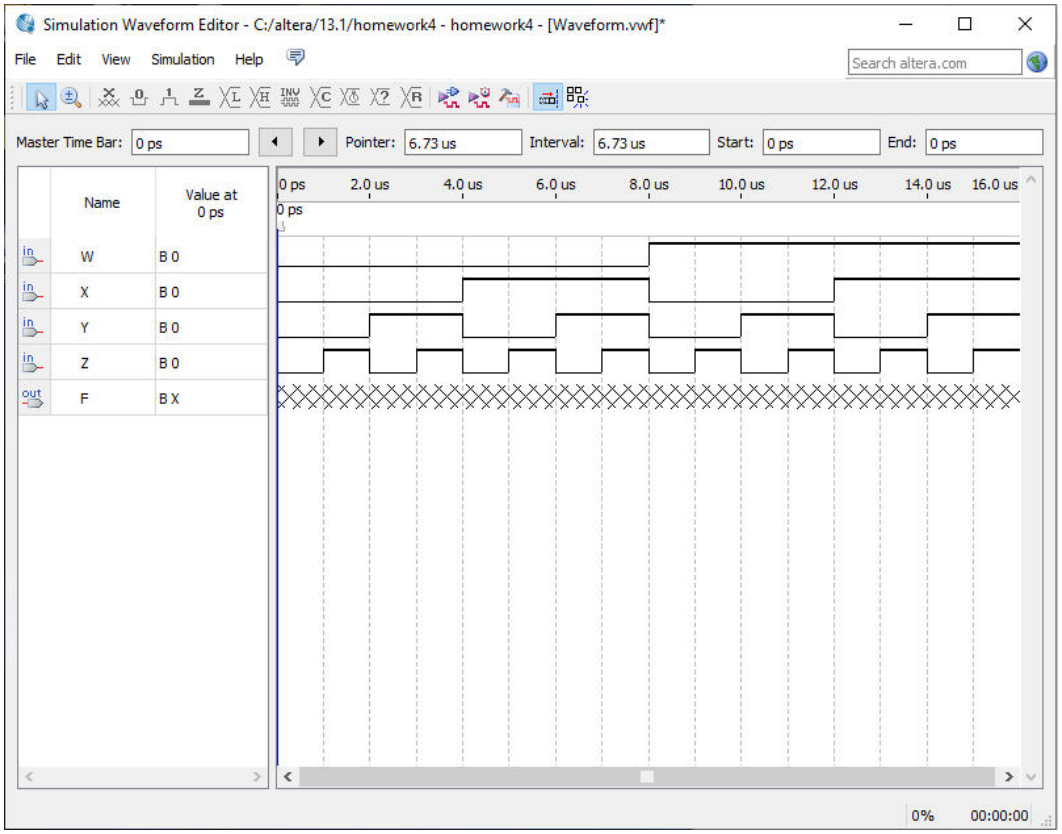
F:Y'+W'Z'+XZ'

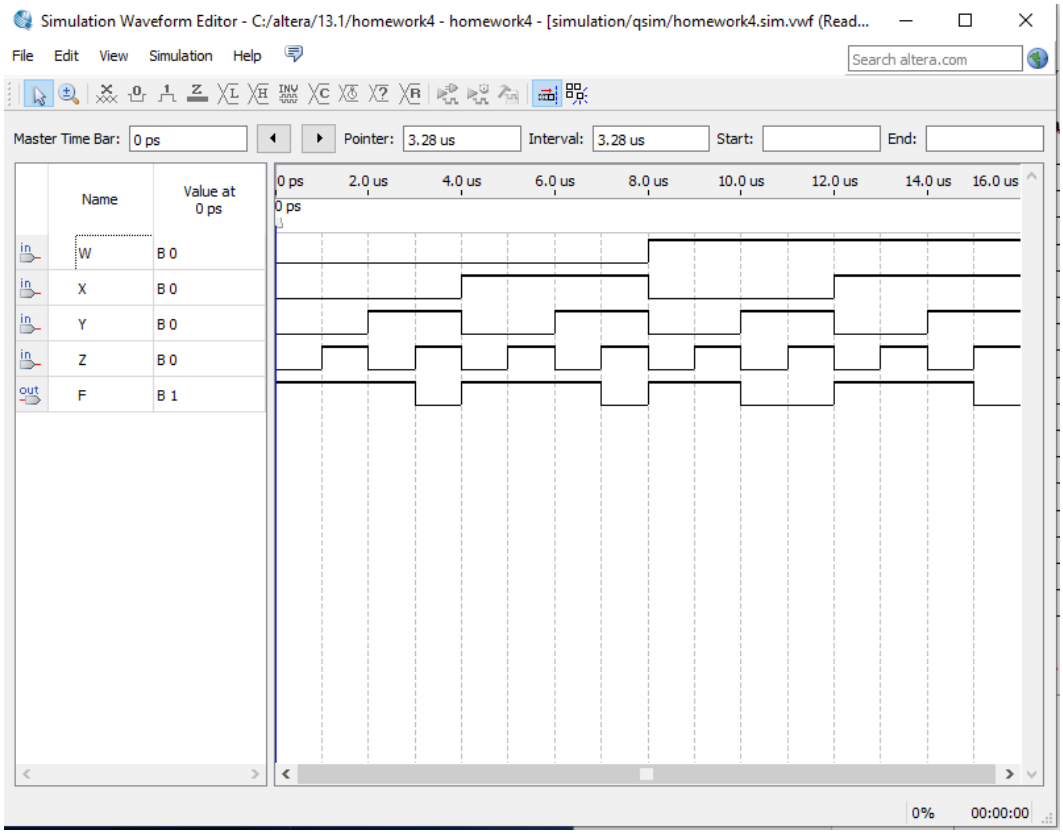
F:Y'+Z'(W'+X)

B) Quartus

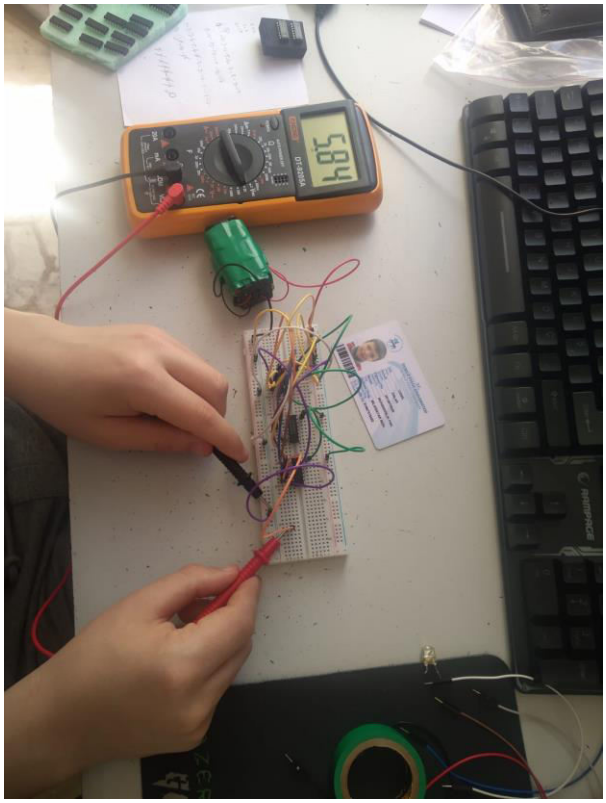


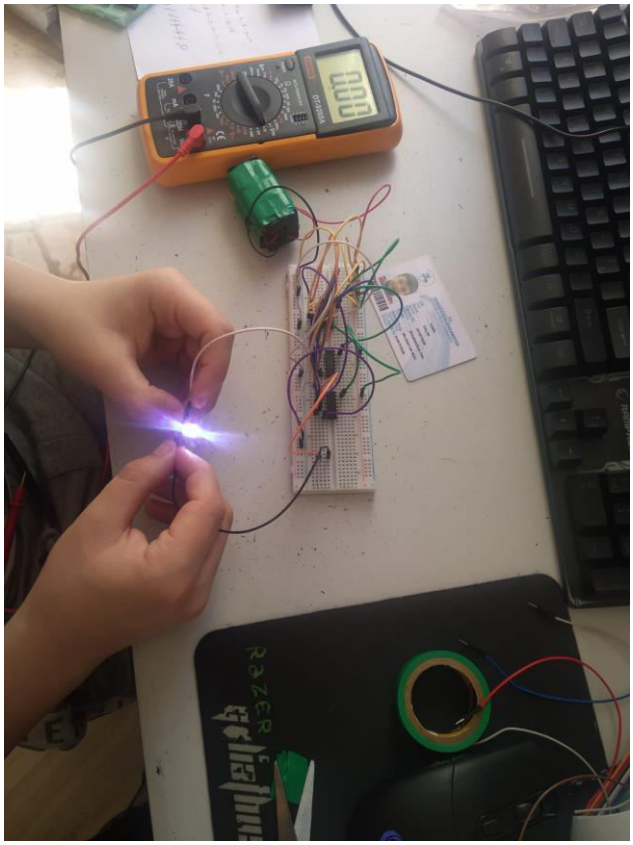
C) Waveform function of F





D) F function on breadboard





2)Half Adder And Full Adder

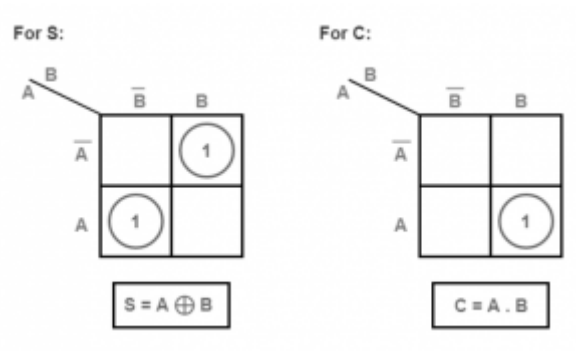
A)Half Adder

The addition of 2 bits is done using a combination circuit called Half adder. The input variables are augend and addend bits and output variables are sum & carry bits. A and B are the two input bits. These are half adder's truth table and karnaugh map

a)Truth Table

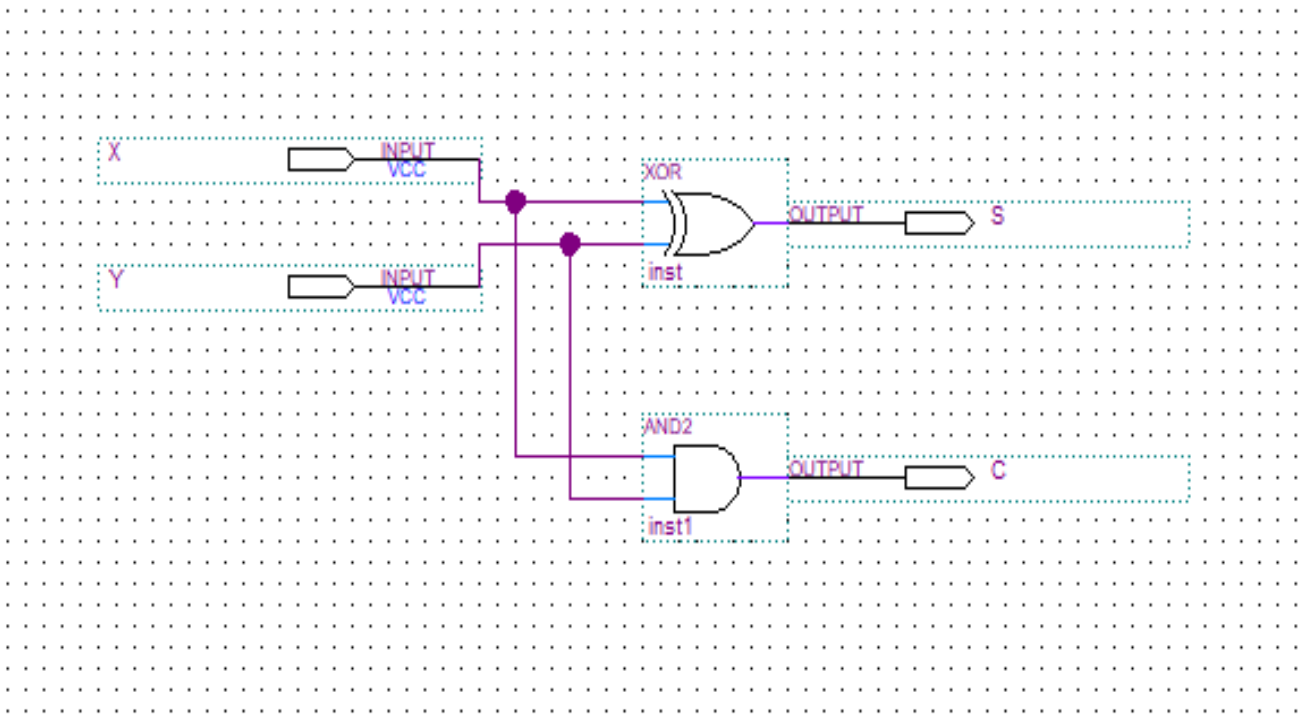
X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Karnaugh Map

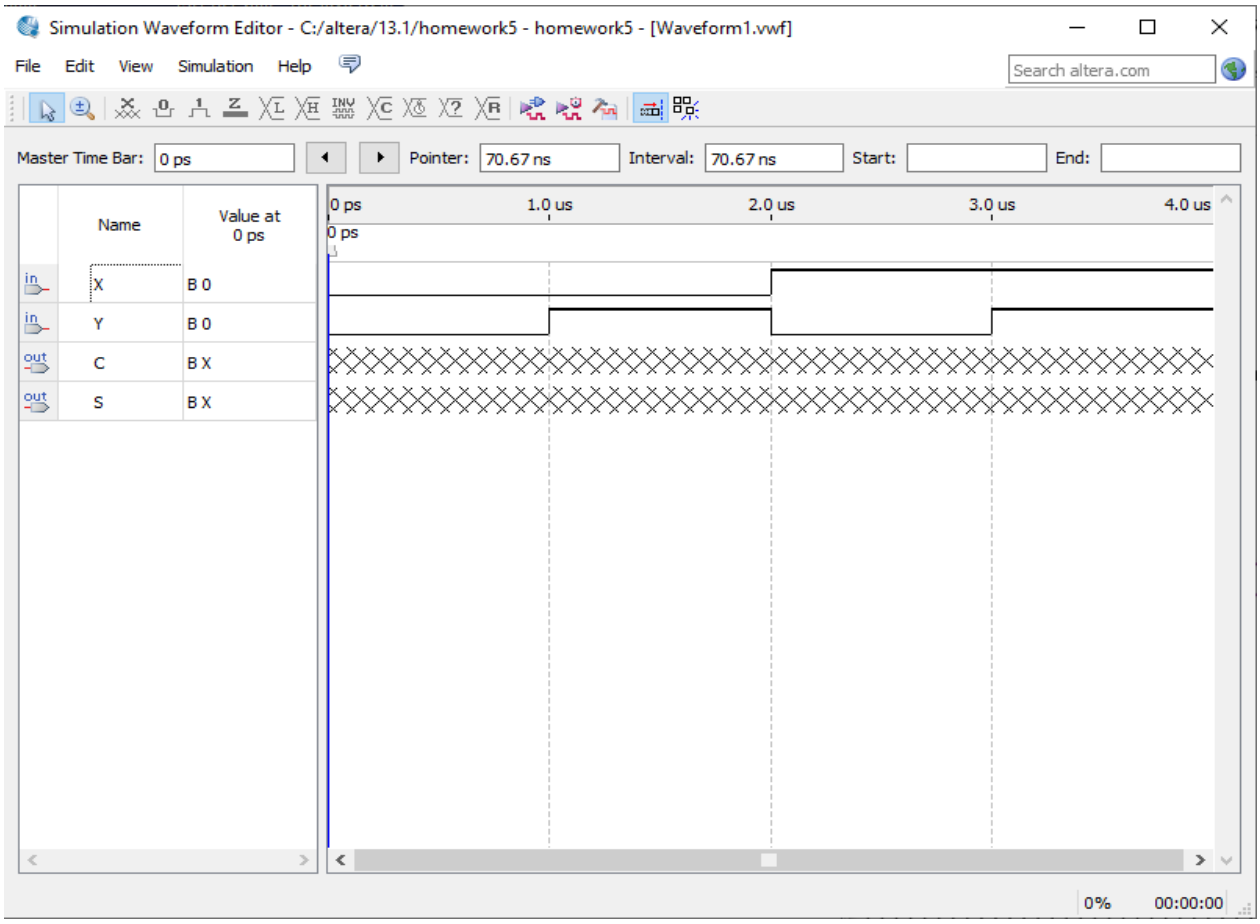


b)Quartus

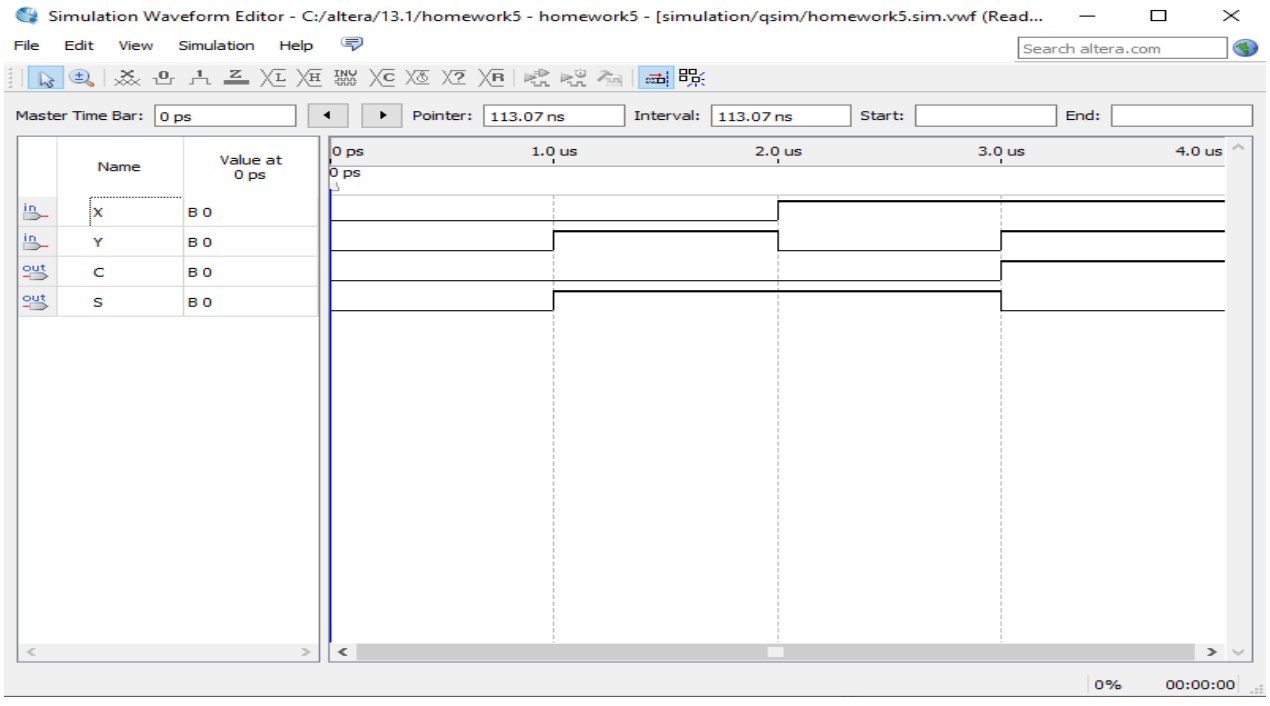
Half adder's implementation on quartus:



c) Waveform of half adder

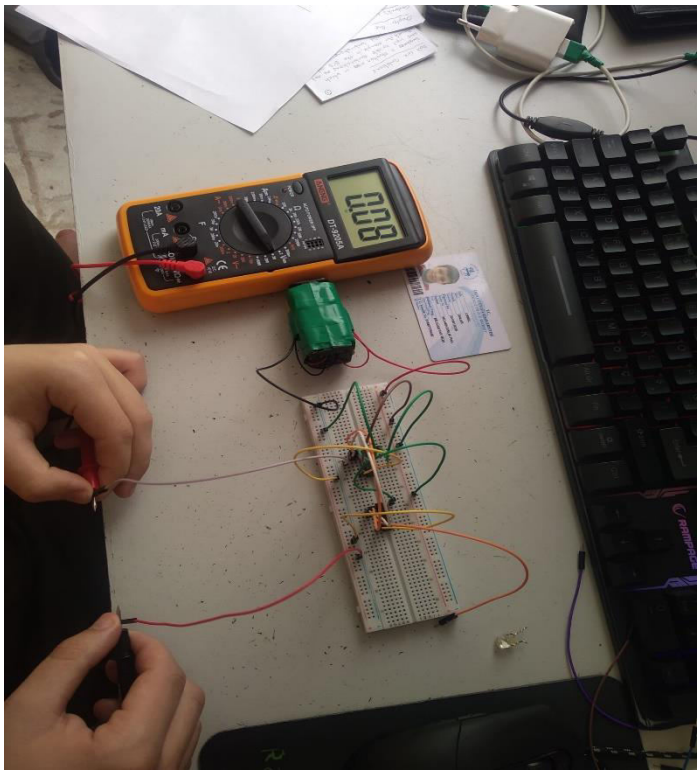


Half adder's waveform result

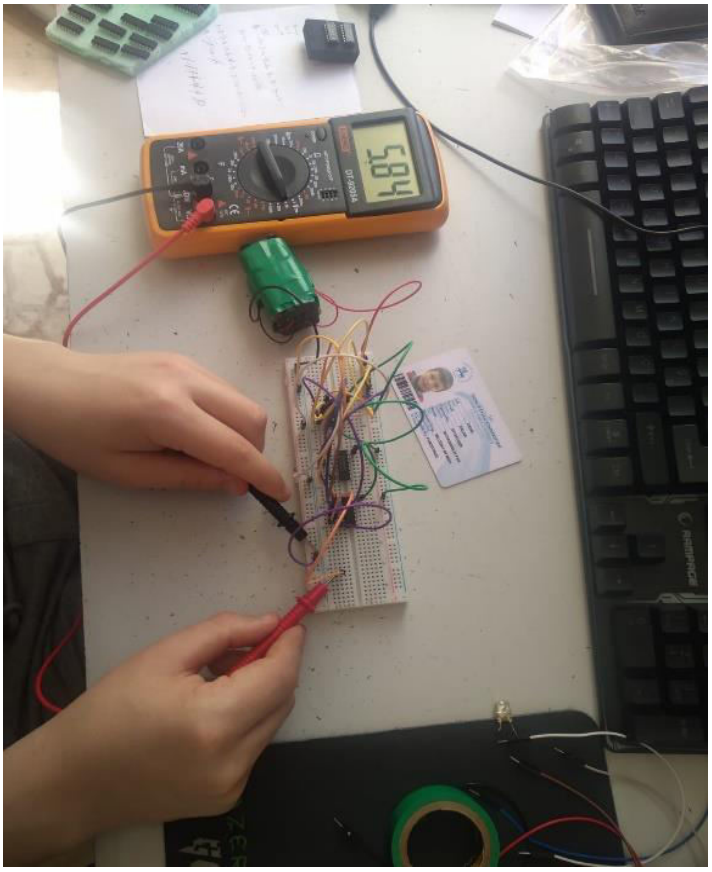


d) Half adder on breadboard

When x equals 1 and y equals 0, c(carry) took the value 0.



When x equals 1 and y equals 0, s(sum) took the value 1.



B)Full Adder

2 Half Adders and a OR gate is required to implement a Full Adder.

a)Truth Table

X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Karnaugh Map

C

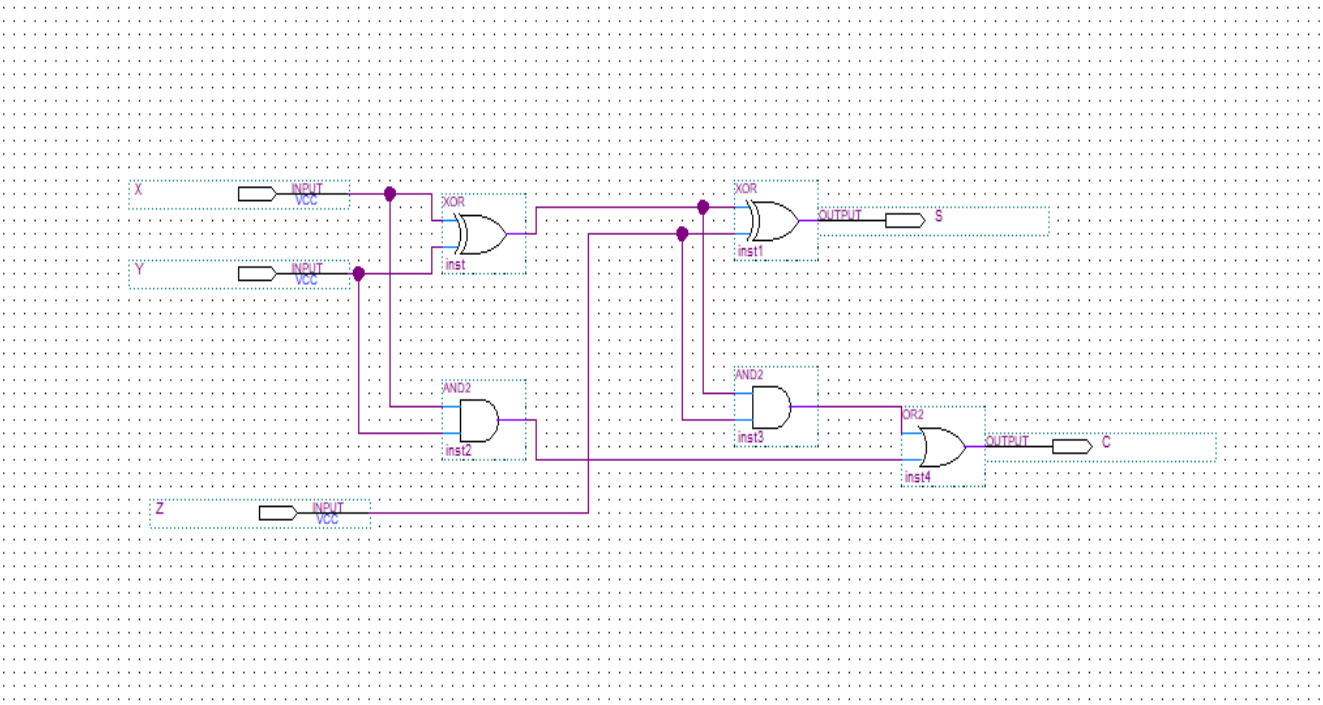
X \ YZ	00	01	11	10
0	0	0	1	0
1	0	1	1	1

S

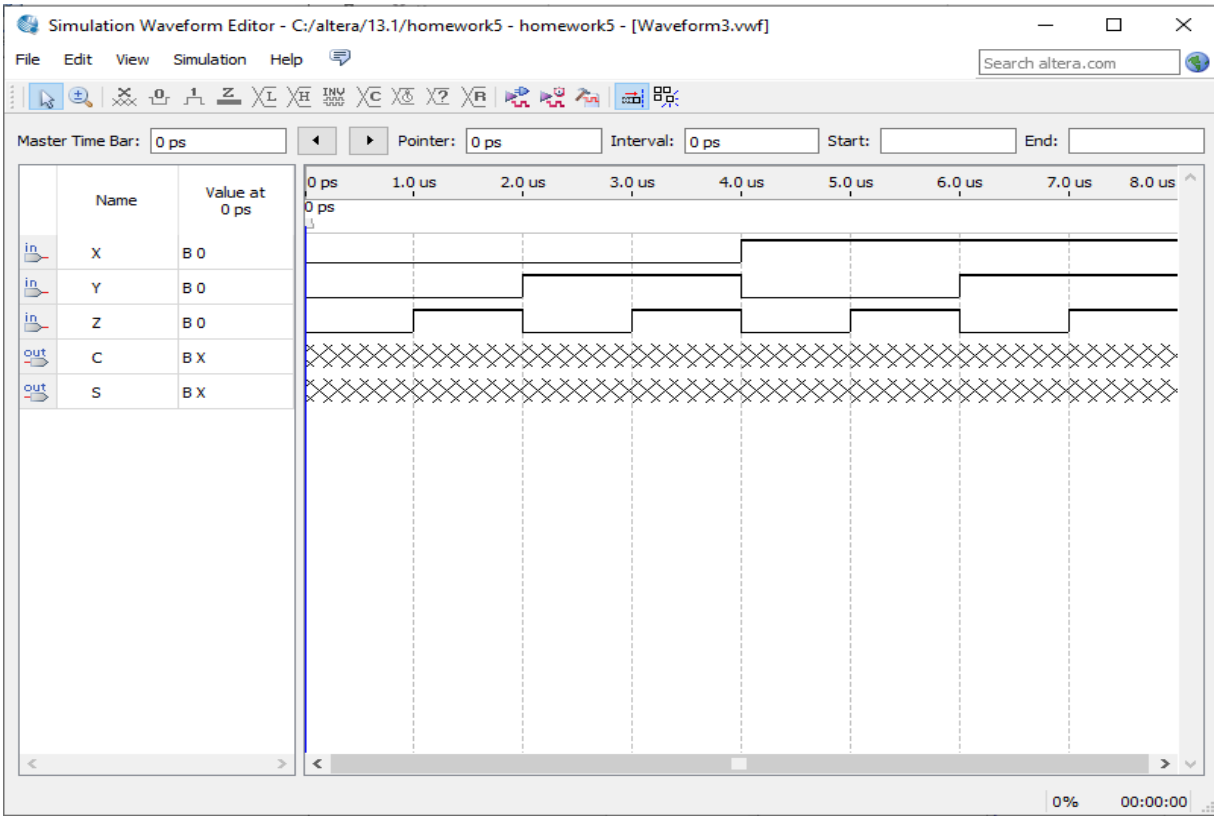
X \ YZ	00	01	11	10
0	0	1	0	1
1	1	0	1	0

b)Quartus

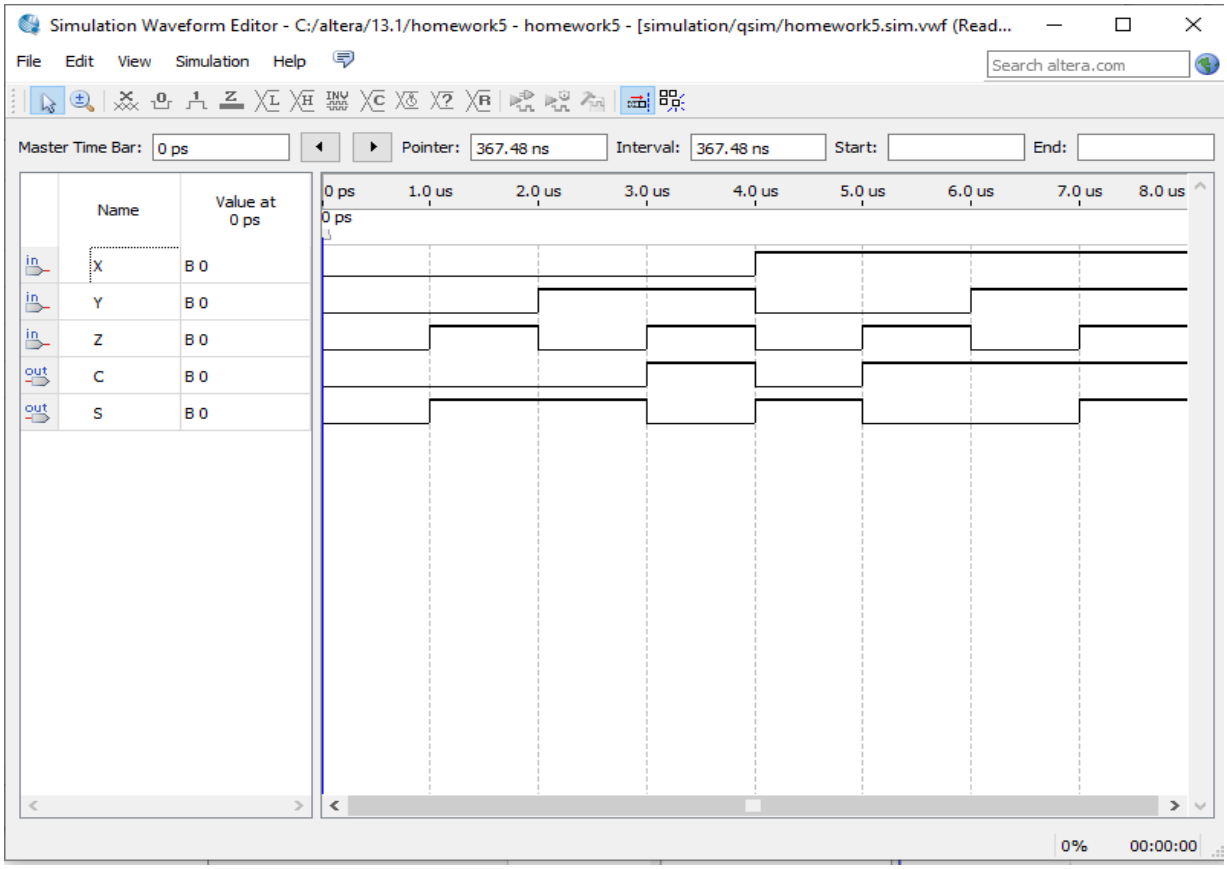
Full adder's implementation on quartus:



c)Waveform of full adder

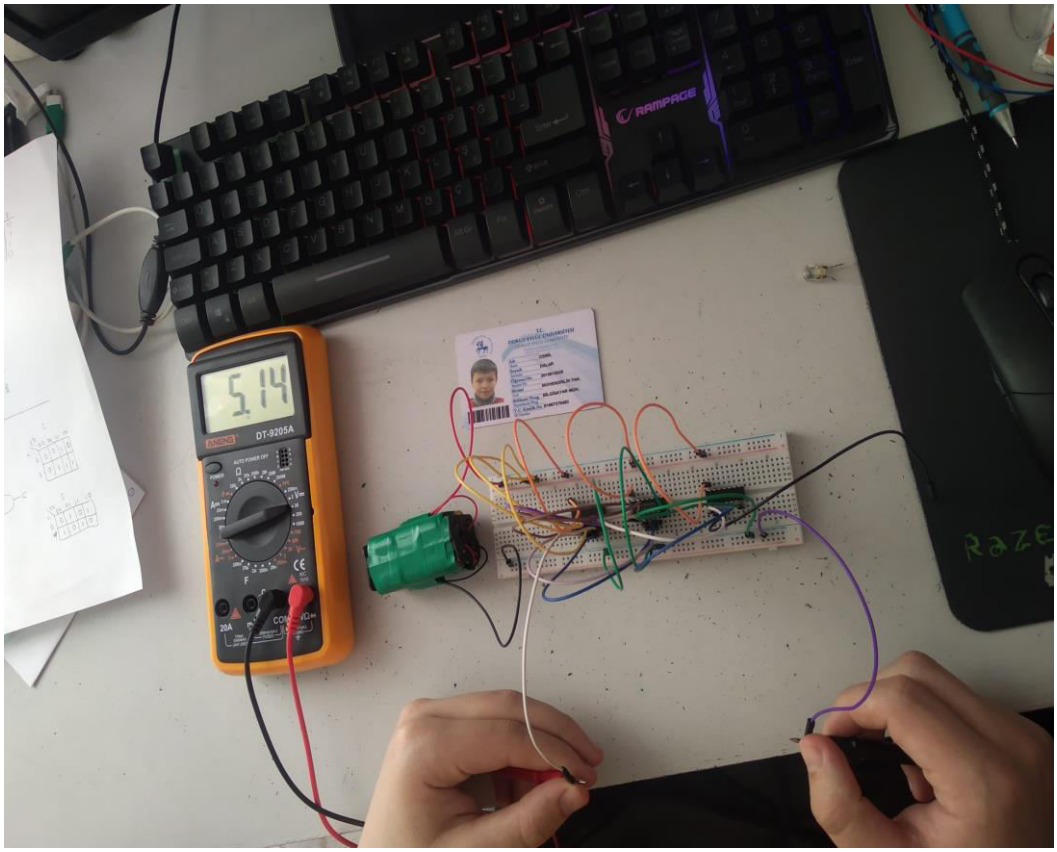


Full adder's waveform result



d)Full adder on breadboard

When x equals 1,y equals 1 and z equals 1, s(sum) took the value 1.



When x equals 1,y equals 1 and z equals 1, c(carry) took the value 1.