S7817 Touch Controller Datasheet

PN: 505-000570-01 Rev. 1

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Introduction

The S7817 is a high performance touchscreen controller. The S7817 has 118 sensing channels (72 RX x 46 TX), for use in touchscreen displays of up to 17.3 inches diagonal.

General description

The S7817 supports self-capacitance, mutual-capacitance, hybrid sensing, and passive stylus with up to 10-finger detection. Fast report rates (up to 150 Hz) and flexible sensing frequency from 50 to 500 kHz (configurable in 69 ns steps/cycle) are also supported.

Optimum SNR performance is achieved with on-chip charge pumps and Signal Clarity™. The controller supports 3312 nodes (72 RX x 46 TX configuration) and a maximum touchscreen size is 17.3 inches (diagonal) with a 16:10 ratio and a pitch of 5 mm.

The S7817 touch controller provides high performance hardware filtering for AC charger noise mitigation, moisture, and severe common mode noise. The devices also offers high performance charge pump, patented CDM driving schemes, and advanced firmware algorithms. Finally, the device has patented display synchronization technology that eliminates display noise from horizontal refresh.

Benefits and features

- **Package**:
  - S7817 165 BGA package (5 mm x 10.5 mm x 0.6 mm)
- **Two representative detection modes:**

20 mm Hover Height	1 mm Stylus Sensing
Up to 12” touchscreens	Up to 13.3" touchscreens with 4 mm pitch

  - Glove and finger nail usage.
- **Power modes:**
  - Touch active
  - Hover active
  - Idle/Large object doze (LOZE)
  - Low-power active mode (LPAM)
- **Digital core:**
  - 16-bit MCU core (proprietary, hardware multi-threaded Synaptics MCU).
- **Serial interfaces:**
  - I^2C (100/400 kHz)
  - SPI slave
  - USB
- **Power supply schemes:**
  - 2.7V to 3.6V supply voltage.
  - 1.65V to 3.6V host interface voltage.
  - 1.2V chip core for low power operation.
  - Internal positive and negative charge pumps for increased TX voltage.
  - Internal LDO regulators with 1.2V and 1.8V outputs.
- **Best-in-class capacitance sensing:**
  - Up to 10-finger detection and simultaneous tracking.
  - 3312 nodes (72 TX × 46 RX configuration) with positional interpolation providing best-in-class accuracy and resolution.
  - Optimum SNR performance: on-chip charge pump with Signal Clarity™.
- **In-system reprogrammability (reflash) support.**
- **Internal power-on reset detector.**
- **Hardware filtering for AC charger noise mitigation.**
- **Internal charge pumps for TX drive.**
- **Supports configurable frequency shifting with Synaptics® Design Studio ™ 5.**
- **Supports advanced sensor/display architecture including:**
  - Touch controller IC on sensor FPC tail.
  - Touch controller IC on main board.
  - Sensor ITO pattern on lens.
  - Curved lens designs.
  - Built-in sensor ID and test features.
  - Self-calibrating — no host side calibration needed.
  - Fully compatible with Synaptics Design Studio 5 tool chain for production-ready touch sensing development.

Applications

- Recommended for use in tablets or notebook PCs with a touchscreen of up to 17.3 inches (in diagonal) with a 16:10 ratio and a pitch of 5 mm. For passive pen support, the maximum touchscreen size is 13.3 inches (in diagonal) with a pitch of 4 mm.

Detailed description

System block diagram

The S7817 touch controller is a fully self-contained, ready-to-use, capacitance-sensing SOC (system-on-a chip).

Synaptics' proprietary 16-bit microcontroller and firmware handles all calibration and operation of the capacitance sensors, computation of finger position and gestures.

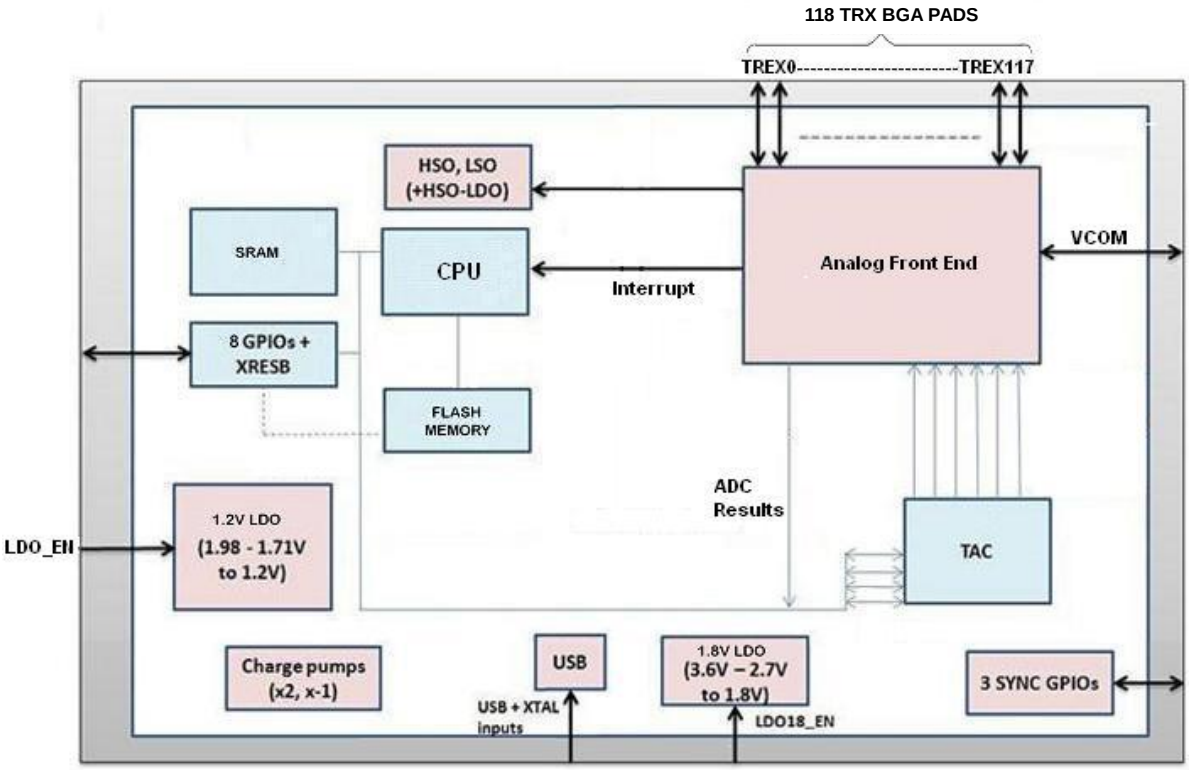

Figure 1. S7817 block diagram

Power supply configurations

The S7817 touch controller is designed to support several power supply configurations ranging from one to four external power supply rails. Table 1 provides the possible configurations.

For details on sensor/FPCA design and routing guidelines, see *ClearPad Sensor Design Guidelines* (PN: 511-000384-01).

Table 1. Power supply configurations

Config	VDD12	VDD18	VDDH	VDDBUS	LDO12EN	LDO18EN	Description
1	Int	Int	Ext	Ext	Float	Float	External VDDBUS, VDDH; Internal +1.8V, +1.2V
2	Int	Ext	Ext	Ext	Float	GND	External VDDBUS, VDD18; VDDH; Internal +1.2V
3	Int	Int	Ext	Int	Float	Float	External VDDH; Internal +1.2V, +1.8V, VDDBUS tied to VDDH18 or VDDH.
4	Int	Ext	Ext	Int	Float	GND	External VDD18, VDDH; Internal +1.2V; VDDBUS tied to VDD18 or VDDH.

Power on sequence and initialization

VDDBUS supplies the communication IO and GPIOs. VDDH supplies analog power. VDD18 and VDD12 supply the digital IC core power. The S7817 touch controller “Power OK” circuitry monitors the VDD18, VDD12, and VDDBUS supply inputs. In order for the POR cycle to commence, the power supplies must start at a lower voltage than the power OK falling threshold and rise monotonically and settle within their tolerances in 25 ms. All three power inputs must be valid before a power on reset condition begins (see Figure 3).

The XRESB, external hardware reset input can also be used to force the chip into a reset condition, when the power supply cannot be shut off completely. The VDDBUS power input is provided so that the I^2C bus can remain functional while other power is removed from the touch controller. In this case the VDDBUS power will remain on and other devices that share the I^2C can continue to function. Pull-up resistors on the I^2C bus should be connected to VDDBUS. The SCL and SDA pins are true open-drain IO pins and will not allow current leakage into the touch controller when the other power rails are switched off. VDDBUS also allows voltage translation with systems using from +1.8V to +3.3V logic.

VDDBUS, VDDH, VDD18, and VDD12 can be powered up in any order. The power state of VDDH is monitored by firmware. The touch controller ATTN interrupt output, typically GPIO PA5, has ESD protection devices that may allow current to leak from the pull-up resistor into the VDDBUS supply, when power is removed. For this reason it is important to connect pull-up resistors to the VDDBUS supply (and not other supplies). Another reason is that if VDDBUS and VDD18 are combined, the leakage current from the pull-up resistor may prevent the VDD18 from decaying fast after power is removed. And much time will be required for the voltage to decay low enough for the POR cycle to function normally.

When powering the S7817 up or down, system design should ensure that the voltages on the signal pins in the Absolute Maximum Ratings table are observed. Failure to follow this requirement may lead to unreliable operation or damage to the device. Open-drain signals (for example, SCL/PA9 and SDA/PA8) are high-impedance at power-up and will transition high when the external pull-ups power (VDDBUS) is applied.

During the initialization phase (Tpowerup), the sensor hardware reset and firmware initialization routines may take up to 45 ms. During this time, the ATTN signal will be de-asserted and no host commands will be recognized. After the sensor is fully initialized, the ATTN pin will be asserted and host communication is enabled.

Power supply sequencing

The power supplies must start at below the power OK falling threshold and rise monotonically to their specified tolerance within 25 ms. Thereafter they must stay within the permitted tolerance. During power up when all power inputs are valid, IO pin PA3 is driven high by the touch controller and will remain high until the hardware power on reset timer expires (min of 5 ms, max of 21 ms) at which time pin PA3 will pulse low.

In systems where pin PA3 is used, the host should expect this power up pulse behavior. If this behavior is not tolerable, other GPIO pins should be used instead. It is strongly recommended that the touch subsystem is the last to be powered up in a device. Doing so will allow the touch controller to measure its baseline with other subsystems (such as an LCD) powered on enabling optimized performance.

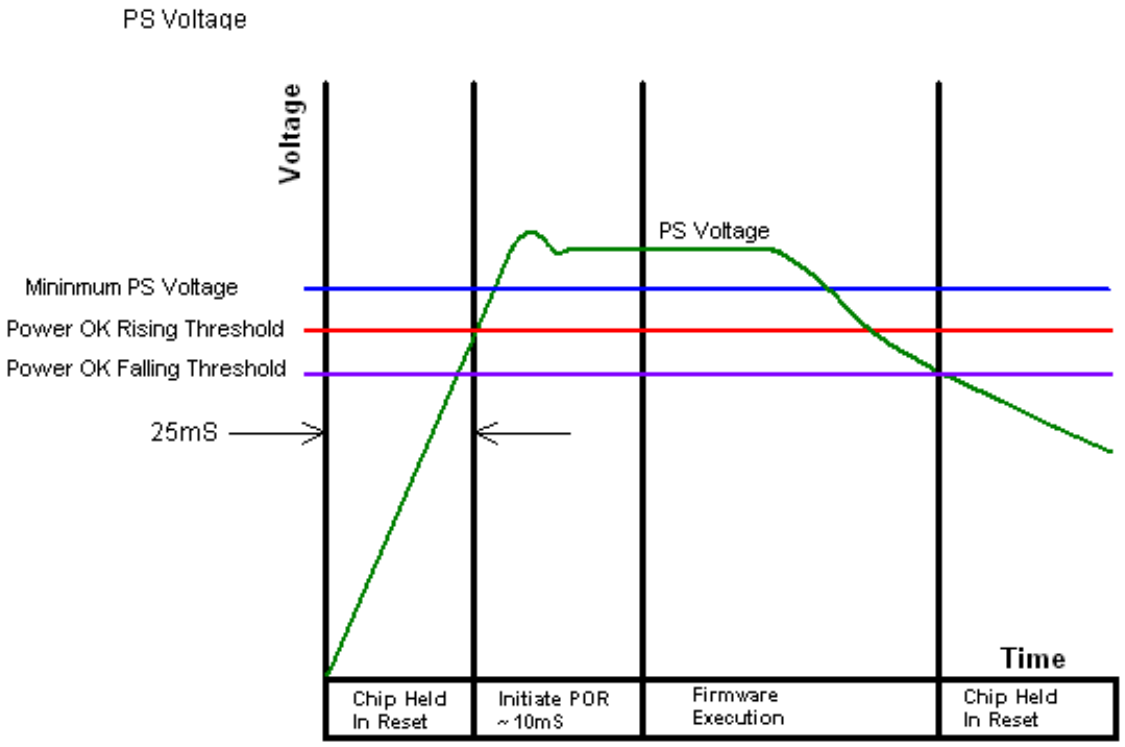

Figure 2. Power supply power-on sequence and start firmware execution

Table 2. Power OK characteristics

Power Supply	Power OK Rising Threshold	Power OK Falling Threshold	Power Supply Minimum Voltage
VDD12	1.08V	1.02V	1.14V
VDD18	1.62V	1.53V	1.71V
VDDBUS	1.62V	1.53V	1.71V

Power-up interface timing

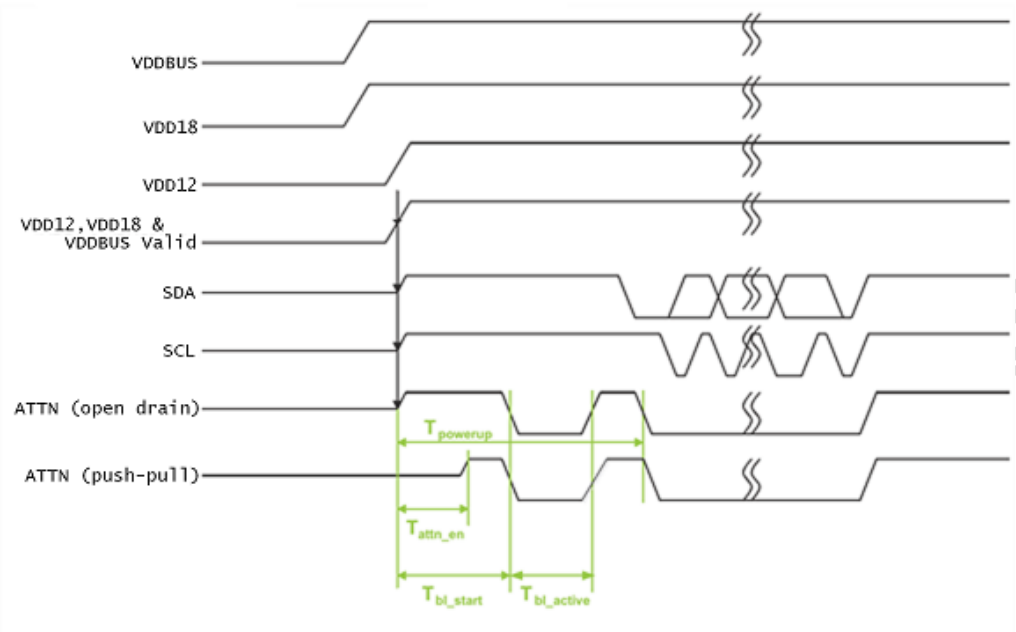

Figure 3. Power-up interface timing diagram

Table 3. Power-up sequence and external reset timing

Subject	Minimum	Maximum
T_{attn_en}	5 ms	21 ms
$T_{powerup}$	—	45 ms
T_{bl_start} (bootloader start)	—	30 ms
T_{bl_active} (bootloader active)	—	15 ms
T_{reset}	100 ns	—

External reset timing

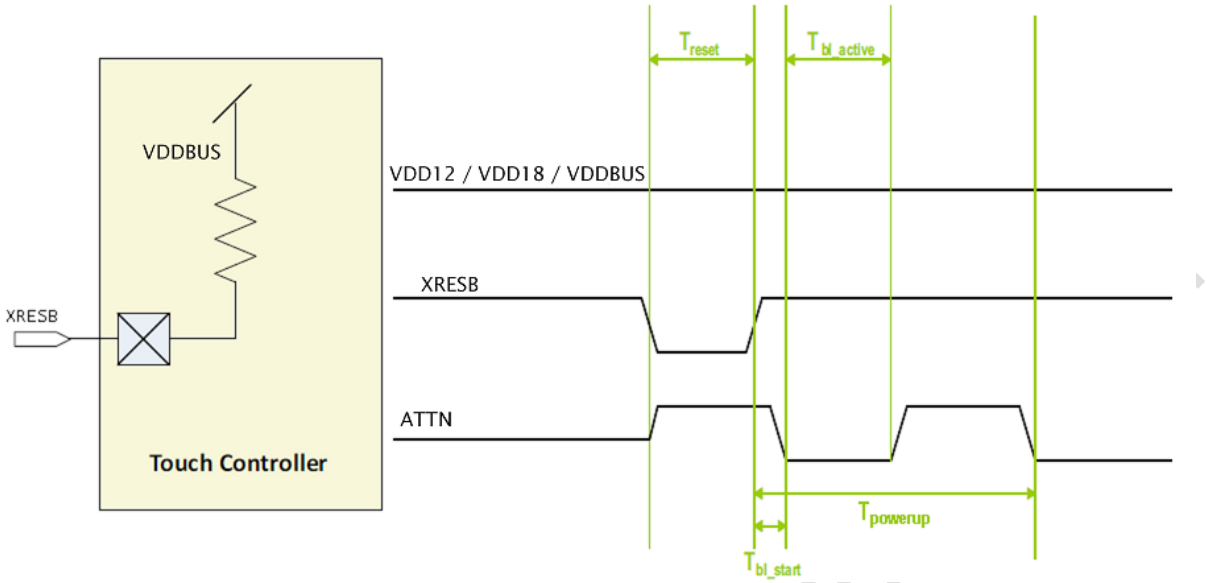

Figure 4. External reset timing diagram

Host interface

The S7817 touch controller is available with an I²C host interface. The host communicates with the S7817 by reading and writing 8-bit data registers. Full details of Synaptics interface protocols can be found in the *Synaptics RMI4 Specification* (PN: 511-000405-01).

Attention signal

In addition to standard I²C signals, the S7817 provides an attention output (ATTN) that is asserted to indicate that new data is available for reading by the host. The ATTN signal is intended to be used as an interrupt source to a host processor. ATTN functionality is added by UI firmware so pin allocation, polarity and drive options (open-drain or push-pull) are defined at the time of firmware build. Operation of the ATTN signal is shown in Figure 5.

Note: The attention line is also de-asserted when the host disables interrupts.

I²C interfacing

Connection

Figure 6. shows an example of host connection using the S7817 I²C interface. The values of the pull-up resistors should be chosen to ensure that the rise times of the SDA and SCL signals are within the limits set by the I²C specification. This depends on what other slave devices, if any, are on the I²C bus but typically would fall within the range of 2.2 kΩ — 10 kΩ.

Refer to the *ClearPad Integration Guide* (PN: 511-000399-01) for additional information.

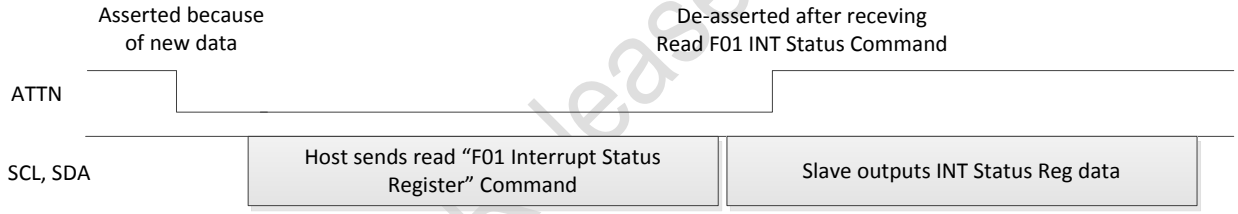

Figure 5. Attention line behavior (I²C interface shown)

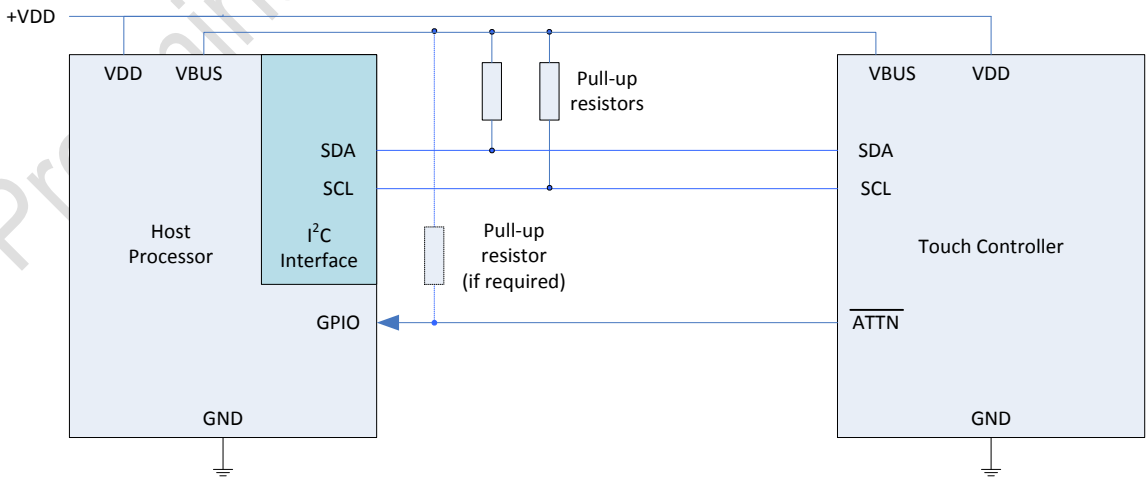

Figure 6. I²C host connection

Clock stretching

Special attention should be paid to clock stretching when interfacing with a Synaptics touch controller over I^2C. The host processor must support clock stretching. The first byte of a transaction contains the slave address and read/write bit. At the end of the first byte, the controller holds SCL low (clock stretches) and checks that the slave address matches its own. If the slave address does not match, the S7817 will not stretch the clock on subsequent byte transmissions until it detects the next start condition. If the slave address does match, the controller acknowledges and may stretch the clock after some or all of the subsequent bytes within the same transaction (Figure 7).

Note: Typical clock stretch time (Tcstr) is less than 25 ms.

In-system reprogrammability

The S7817 touch controller includes firmware in order to support finger tracking and position reporting. This firmware is stored in non-volatile (flash) memory on-chip and may be updated at any time over the host interface. This capability allows freedom and flexibility when operating with Synaptics devices; simply choose the firmware image that is applicable to your design. Figure 8 illustrates the firmware storage methodology.

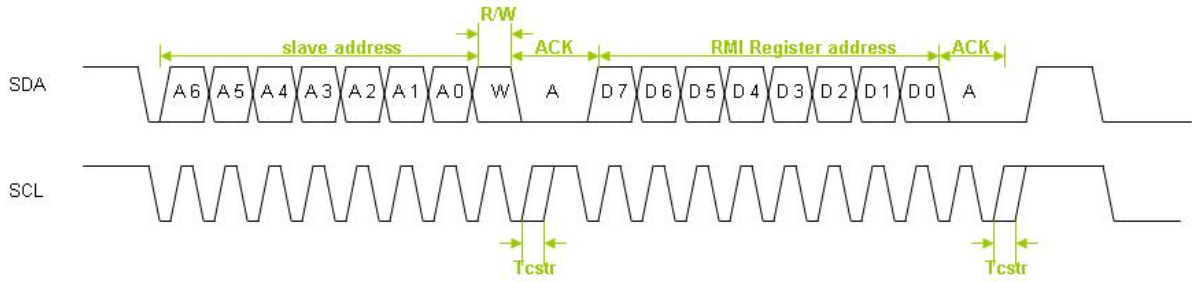

Figure 7. Clock stretching with an I^2C transaction

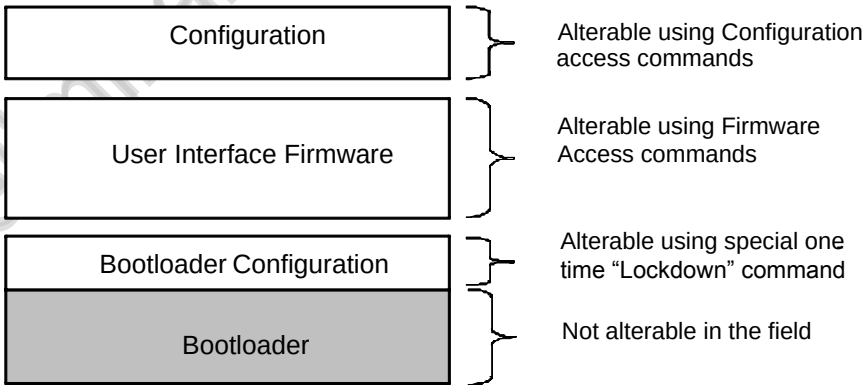

Figure 8. Firmware structure

Bootloader: This is pre-programmed and cannot be changed. The bootloader:

- checks the integrity of the UI firmware space, and
- provides the ability to re-flash a new UI or configuration area.

Bootloader configuration: This can be set by a one-time lockdown process when adding UI firmware for the first time. This permits the same S7817 parts to be deployed in different hosts systems where required bootloader configuration may be different for each.

User Interface firmware: The UI firmware space contains the firmware that implements the primary function of the device. UI firmware images are provided by Synaptics in an encrypted form to ensure they can only be executed on an appropriate device. It is not possible to erase the UI firmware space without also erasing the configuration space.

Configuration: The configuration space stores the default values of the device's control registers. The bootloader provides a mechanism to erase and reprogram this space. Because an existing configuration may not be valid for a new firmware revision, any update to the UI firmware should be followed by an update of the configuration space.

Reference code is available from Synaptics which implements the steps for reprogramming the configuration and UI firmware space.

AC electrical characteristics

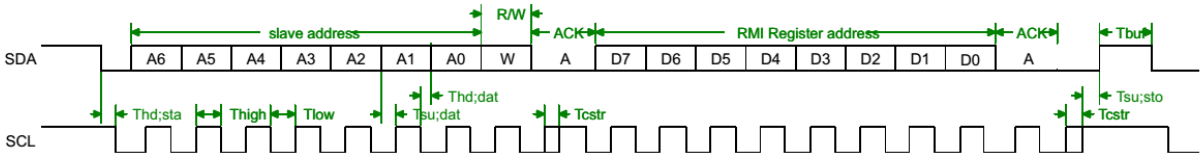

Figure 9. I²C timing

Table 4. I²C parameters

Parameter	Symbol	Standard Mode			Fast mode			Unit
		Minimum	Typical	Maximum	Minimum	Typical	Maximum	
SCL clock frequency	f_{SCL}	--	--	100	--	--	400	kHz
Stretch time	t_{CSTR}	--	25	--	--	25	--	µs
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	--	--	0.6	--	--	µs
LOW period of the SCL clock	t_{LOW}	4.7	--	--	1.3	--	--	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	--	--	0.6	--	--	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	--	--	0.6	--	--	µs
Data hold time	$t_{HD;DAT}$	0	--	3.45	0	--	0.9	µs
Data out hold time	$t_{HD;DATO}$	--	--	0	--	--	0	µs
Data set-up time	$t_{SU;DAT}$	250	--	--	100	--	--	ns
Rise time of both SDA and SCL signals	t_r	--	--	1000	20 + 0.1 C_b	--	300	ns
Fall time of both SDA and SCL signals	t_f	--	--	300	20 + 0.1 C_b	--	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	4.0	--	--	0.6	--	--	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	--	--	1.3	--	--	µs
Capacitive load for each bus line	C_b	--	--	400	--	--	400	pF

Electrical characteristics

Absolute maximum ratings

Table 5. Absolute maximum ratings

Subject	Minimum	Maximum	Units
Voltage on any TRX pin(1)	– 3.6	+7	V
Voltage on any GPIO pin(1)	– 0.3	+4	V
VDDUSB/VDDBUS	– 0.3	+4	V
VDD12	– 0.3	+1.32	V
VDD18	– 0.3	+1.98	V
VDDH/VDDRX	– 0.3	+4.0	V
VDDTX	– 0.3	+7.2	V
Input current at any pin(1)	—	100	mA
Package input current(1)	—	200	mA
Operating temperature	–20	+85	ºC
Storage temperature, unbiased	–55	+125	ºC
Lead soldering temperature (10 seconds)	—	+260	ºC

Note: 1 When the input voltage at any pin exceeds the associated power supply, the current at that pin should be limited to 100 mA. The 200 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 100 mA to two pins. The maximum time this condition can be applied is approximately 10 seconds.

Power supply characteristics

Table 6. Electrical characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Analog supply input 1	VDDH	—	2.7	3.3	3.6	V
Analog filter pin 1	VDDRX	—	2.6	—	3.5	V
Analog filter pin 2	VDDA	—	2.6	—	3.5	V
Digital core supply	VDD12	—	1.14	1.2	1.32	V
Analog supply input 2	VDD18	—	1.71	1.8	1.98	V
Internal +1.2V LDO supply input	VDD12LDO	—	1.71	1.8	1.98	V
Internal +1.8 LDO supply input	VDD18LDO	—	2.7	3.3	3.6	V
GPIO/USB power supply(1)	VDDBUS	—	1.65	1.8	3.6	V
Positive voltage charge pump output	VDDCP	VDDH = +3.3V	—	—	6.6	V
Negative voltage charge pump output	VBBCP	VDDH = +3.3V	-3.6	—	0	V

Note 1: The minimum voltage for USB is 3V.

Reliability characteristics

Table 7. Reliability characteristics

Symbol	Parameter	Minimum	Maximum	Units	Reference Test Method
$FLASH_{DR}$	Flash data retention	10	—	Years	Accelerated test
$FLASH_{ENPB}$	Flash write endurance	1000	—	Erase/Write Cycles	—
V_{ZAPHBM}	ESD susceptibility HBM	—	± 2	kV	HBM, ANSI/ESD S20.20-2007
V_{ZAP}	ESD susceptibility CDM	—	± 500	V	CDM, Q100-001/C2

Table 8. GPIO PA0 – PA7 characteristics; push-pull

Operating conditions must be specified; for example, VDDH = +3.3V, VDD18 = +1.8V, VDD12 = +1.2V, VDDBUS = +1.8V, T_A = 25C unless otherwise noted.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Input high-level voltage	V_{IH}	VDDBUS = +1.8V	1.2	—	—	V
Input low-level voltage	V_{IL}	VDDBUS = +1.8V	—	—	0.5	V
Input hysteresis	V_{HYS}	VDDBUS = +1.8V	—	90	—	mV
Input capacitance	C_{IN}	VDDBUS = +1.8V	—	5	—	pF
Output voltage high	V_{OH}	VDDBUS = +1.8V; I_O = -3 mA	1.4	—	—	V
Output voltage low	V_{OL}	VDDBUS = +1.8V; I_O = 3 mA	—	—	0.4	V

Table 9. GPIO PA8 – PA9 characteristics; open drain I^2C

Operating conditions must be specified; for example, VDDH = +3.3V, VDD18 = +1.8V, VDD12= +1.2V, VDDBUS = +1.8V, T_A = 25C unless otherwise noted.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Input high-level voltage	V_{IH}	VDDBUS = +1.8V	1.2	—	—	V
Input low-level voltage	V_{IL}	VDDBUS = +1.8V	—	—	0.5	V
Input hysteresis	V_{HYS}	VDDBUS = +1.8V	—	90	—	mV
Input capacitance	C_{IN}	VDDBUS = +1.8V	—	10	—	pF
Output voltage low	V_{OL}	VDDBUS = +1.8V; I_O = 3 mA	—	—	0.36	V

IC specification

Operating conditions must be specified; for example, V_{AVDD} = 3.0V, VDVDD = VDVDDIO = 1.8V, VAGND = VDGND =0, no load, T_A = -40℃to +85℃ unless otherwise noted. Typical values are at T_A = 25℃.

Table 10. IC specification

POWER SUPPLIES						
Parameter	**Symbol**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
Analog power supply input	VDDH	Analog power supply voltage	2.7	—	3.6	V
Analog filtered supply 1	VDDA	External capacitor connection	2.6	—	3.5	V
Analog filtered supply 2	VDDRX	External capacitor connection	2.6	—	3.5	V
Digital core supply	VDD12	—	1.14	1.2	1.32	V
Analog supply input	VDD18	—	1.71	1.8	1.98	V
Internal +1.2V LDO supply input	VDD12LDO	LDO power supply input	1.71	1.8	1.98	V
Internal +1.8V LDO supply input	VDD18LDO	LDO power supply input	2.7	3.3	3.6	V
D_{VDDIO}/GPIO/USB power supply voltage	VDDBUS	—	1.65	1.8	3.6	V
Positive voltage charge pump output	VDDCP	VDDH = +3.3V	—	—	6.6	V
Negative voltage charge pump output	VBBCP	VDDH = +3.3V	-3.6	—	—	V
TRANSMITTER (TX)						
Parameter	**Symbol**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
Driving voltage range	V_{TX}	TX charge pump voltage	3.3	—	10.8	V
Number of TX channels	N_{TX}	46	—	—	—	—
Programmable frequency range	f	—	51		500	kHz
Programmable frequency step resolution	f_{STEP}	69 ns step per cycle resolution	—	—	14.5	MHz
RECEIVER (RX)						
Parameter	**Symbol**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
Number of RX channels	N_{RX}	72 max	—	—	72	—
Signal-to-noise ratio (10-phi)	SNR	100 Hz report rate	—	35	—	dB
Signal-to-interference ratio (TBD)	SIR	—	—	—	—	dB
DIGITAL IO CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
Input voltage high	V_{IH}	VDDBUS = +1.8V	1.26	—	—	V
Input voltage low	V_{IL}	VDDBUS = +1.8V	—		0.54	V
Input hysteresis	V_{HYS}	VDDBUS = +1.8V	—	90	—	mV
Input capacitance	C_{IN}	VDDBUS = +1.8V	—	5	—	pF
Input leakage current	I_{IL}	1	—	—	—	—
Output voltage high	V_{OH}	VDDBUS = +1.8V; IO = -3 mA	1.4	—	—	V
Output voltage low	V_{OL}	VDDBUS = +1.8V; IO = 3 mA	—	—	0.4	V

Power consumption for each power mode

Table 11. Power consumption external VDDH and VDD18 (internal 1.2V LDO active)

ACTIVE MODE (ONE FINGER)				
V_{DDH} supply current	IDDH	Hover active @ 60Hz	TBD	mA
		Touch active @ 90Hz	TBD	mA
V_{DD18} supply current	IDD18	Hover active @ 60Hz	TBD	mA
		Touch active @ 90Hz	TBD	mA
IDLE MODE				
V_{DDH} supply current	IDDH	Hover idle @ 100Hz	TBD	mA
		Touch idle @ 30Hz	TBD	mA
V_{DD18} supply current	IDD18	Hover idle @ 100Hz	TBD	mA
		Touch idle @ 30Hz	TBD	mA
LOW POWER ACTIVE MODE				
VDDH supply current	IDDH	LPDM active @ 10Hz	TBD	mA
VDD18 supply current	IDD18	LPDM active @ 10Hz	TBD	mA
LOW POWER IDLE MODE				
VDDH supply current	IDDH	LPDM idle @ 10Hz	TBD	mA
VDD18 supply current	IDD18	LPDM idle @ 10Hz	TBD	mA

Note: Using a 1.2V supply decreases the power consumption by ~ 10 mW.

Pin description

Pin diagram

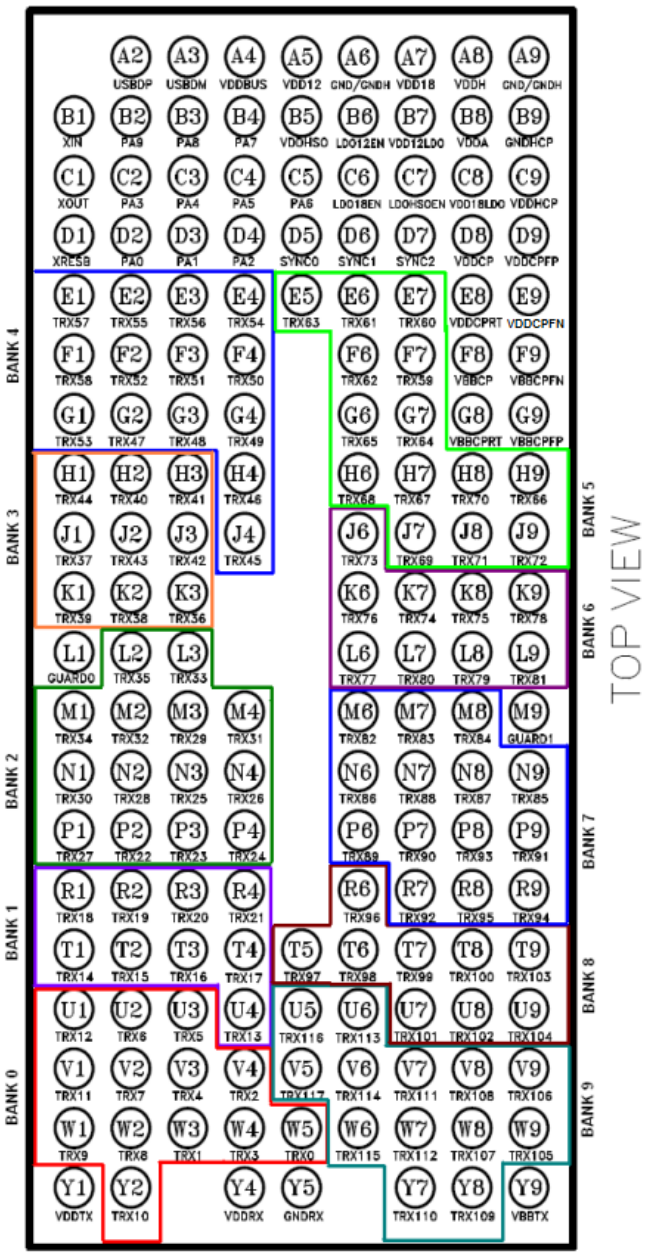

Figure 10. S7817 165 BGA pin assignments (top view)

165 BGA pin signal connections: I²C

Table 12. Pin connections for S7817

Pin Location	Signal	IO Type	Description
A2	USBDP	USBIO	USB D+.
A3	USBDM	USBIO	USB D-.
A4	VDDBUS	Power In	Power supply for the USB core / Power supply for all GPIO pin.
A5	VDD12	Power	+1.2V source for digital core. Output of internal 1.2V LDO, requires external bypass capacitor. +1.2V source from external supply when LDO12EN is grounded.
A6	GND/GNDH	Power	Package digital ground.
A7	VDD18	Power	+1.8V source for digital core. Output of internal 1.8V LDO, requires external bypass capacitor. +1.8V source from external supply when LDO18EN is grounded.
A8	VDDH	Power In	Analog power input, +3V.
A9	GND/GNDH	Power	Package digital ground.
B1	XIN	Input	Input pin from 48 MHz crystal resonator.
B2	PA9/SCL/SCLK	GPIO OD	I²C clock (SCL); Alternate SPI SCLK; true open drain IO.
B3	PA8/SDA/MOSI	GPIO OD	I²C data (SDA); Alternate SPI MOSI; true open drain IO.
B4	PA7	GPIO	Spare GPIO.
B5	VDDHSO	Power	HSO/LDO power supply pin; do not connect.
B6	LDO12EN	Input	Enable Internal 1.2V LDO. Float to enable. GND to disable.
B7	VDD12LDO	Power In	External +1.8V power input to internal LDO.
B8	VDDA	Filter Pin	Low-pass filtered version of VDDH used by Charge Integrators.
B9	GNDHCP	Power	Charge pump GND.
C1	XOUT	Output	Output to Colpitts crystal resonator circuit.
C2	PA3	GPIO	Spare GPIO.
C3	PA4	GPIO	Spare GPIO.
C4	PA5/ATTN/ MISO	GPIO	I²C ATTN Interrupt; SPI MISO.
C5	PA6	GPIO	Spare GPIO.
C6	LDO18EN	Input	Enable Internal 1.8V LDO. Float to enable. GND to disable.
C7	LDOHSOEN	Input	Enable Internal Oscillator. Float to enable. GND to disable.
C8	VDD18LDO	Power In	External +3.3V power input to internal LDO.
C9	VDDHCP	Power In	External +3V power input to internal charge pumps.
D1	XRESB	Input	Dedicated active low reset pin; Has internal pullup to VDDBUS.
D2	PA0	GPIO	Spare GPIO.
D3	PA1	GPIO	Spare GPIO.
D4	PA2	GPIO	Spare GPIO.
D5	SYNC0	IO	Multi-chip synchronization signal.
D6	SYNC1	IO	Multi-chip synchronization signal.
D7	SYNC2	IO	Multi-chip synchronization signal.
D8	VDDCP	Power Out	Output of positive CP (external voltage should never be applied).
D9	VDDCPFP	Analog	Positive charge pump capacitor, positive side.
E1	TRX57	IO	Transmitter or Receiver electrode, configurable in bank 4 grouping.
E2	TRX55	IO	Transmitter or Receiver electrode, configurable in bank 4 grouping.
E3	TRX56	IO	Transmitter or Receiver electrode, configurable in bank 4 grouping.
E4	TRX54	IO	Transmitter or Receiver electrode, configurable in bank 4 grouping.

Pin Location	Signal	IO Type	Description
E5	TRX63	IO	Transmitter or Receiver electrode, configurable in bank 5 grouping.
E6	TRX61	IO	Transmitter or Receiver electrode, configurable in bank 5 grouping.
E7	TRX60	IO	Transmitter or Receiver electrode, configurable in bank 5 grouping.
E8	VDDCPRT	Power In	Power input to the positive CP bypass switch (external voltage can be applied).
E9	VDDCPFN	Analog	Positive charge pump capacitor, negative side.
F1	TRX58	IO	Transmitter or Receiver electrode, configurable in bank 4 grouping.
F2	TRX52	IO	Transmitter or Receiver electrode, configurable in bank 4 grouping.
F3	TRX51	IO	Transmitter or Receiver electrode, configurable in bank 4 grouping.
F4	TRX50	IO	Transmitter or Receiver electrode, configurable in bank 4 grouping.
F6	TRX62	IO	Transmitter or Receiver electrode, configurable in bank 5 grouping.
F7	TRX59	IO	Transmitter or Receiver electrode, configurable in bank 5 grouping.
F8	VBBCP	Power Out	Output of negative CP.
F9	VBBCPFN	Analog	Negative charge pump capacitor, negative side.
G1	TRX53	IO	Transmitter or Receiver electrode, configurable in bank 4 grouping.
G2	TRX47	IO	Transmitter or Receiver electrode, configurable in bank 4 grouping.
G3	TRX48	IO	Transmitter or Receiver electrode, configurable in bank 4 grouping.
G4	TRX49	IO	Transmitter or Receiver electrode, configurable in bank 4 grouping.
G6	TRX65	IO	Transmitter or Receiver electrode, configurable in bank 5 grouping.
G7	TRX64	IO	Transmitter or Receiver electrode, configurable in bank 5 grouping.
G8	VBBCPRT	Power In	Power input to the negative CP bypass switch (external voltage can be applied).
G9	VBBCPFP	Analog	Negative charge pump capacitor, positive side.
H1	TRX44	IO	Transmitter or Receiver electrode, configurable in bank 3 grouping.
H2	TRX40	IO	Transmitter or Receiver electrode, configurable in bank 3 grouping.
H3	TRX41	IO	Transmitter or Receiver electrode, configurable in bank 3 grouping.
H4	TRX46	IO	Transmitter or Receiver electrode, configurable in bank 4 grouping.
H6	TRX68	IO	Transmitter or Receiver electrode, configurable in bank 5 grouping.
H7	TRX67	IO	Transmitter or Receiver electrode, configurable in bank 5 grouping.
H8	TRX70	IO	Transmitter or Receiver electrode, configurable in bank 5 grouping.
H9	TRX66	IO	Transmitter or Receiver electrode, configurable in bank 5 grouping.
J1	TRX37	IO	Transmitter or Receiver electrode, configurable in bank 3 grouping.
J2	TRX43	IO	Transmitter or Receiver electrode, configurable in bank 3 grouping.
J3	TRX42	IO	Transmitter or Receiver electrode, configurable in bank 3 grouping.
J4	TRX45	IO	Transmitter or Receiver electrode, configurable in bank 4 grouping.
J6	TRX73	IO	Transmitter or Receiver electrode, configurable in bank 6 grouping.
J7	TRX69	IO	Transmitter or Receiver electrode, configurable in bank 5 grouping.
J8	TRX71	IO	Transmitter or Receiver electrode, configurable in bank 5 grouping.
J9	TRX72	IO	Transmitter or Receiver electrode, configurable in bank 5 grouping.
K1	TRX39	IO	Transmitter or Receiver electrode, configurable in bank 3 grouping.
K2	TRX38	IO	Transmitter or Receiver electrode, configurable in bank 3 grouping.
K3	TRX36	IO	Transmitter or Receiver electrode, configurable in bank 3 grouping.
K6	TRX76	IO	Transmitter or Receiver electrode, configurable in bank 6 grouping.
K7	TRX74	IO	Transmitter or Receiver electrode, configurable in bank 6 grouping.
K8	TRX75	IO	Transmitter or Receiver electrode, configurable in bank 6 grouping.

Pin Location	Signal	IO Type	Description
K9	TRX78	IO	Transmitter or Receiver electrode, configurable in bank 6 grouping.
L1	GUARD0	Output	Guard amplifier 0 output
L2	TRX35	IO	Transmitter or Receiver electrode, configurable in bank 2 grouping.
L3	TRX33	IO	Transmitter or Receiver electrode, configurable in bank 2 grouping.
L6	TRX77	IO	Transmitter or Receiver electrode, configurable in bank 6 grouping.
L7	TRX80	IO	Transmitter or Receiver electrode, configurable in bank 6 grouping.
L8	TRX79	IO	Transmitter or Receiver electrode, configurable in bank 6 grouping.
L9	TRX81	IO	Transmitter or Receiver electrode, configurable in bank 6 grouping.
M1	TRX34	IO	Transmitter or Receiver electrode, configurable in bank 2 grouping.
M2	TRX32	IO	Transmitter or Receiver electrode, configurable in bank 2 grouping.
M3	TRX29	IO	Transmitter or Receiver electrode, configurable in bank 2 grouping.
M4	TRX31	IO	Transmitter or Receiver electrode, configurable in bank 2 grouping.
M6	TRX82	IO	Transmitter or Receiver electrode, configurable in bank 7 grouping.
M7	TRX83	IO	Transmitter or Receiver electrode, configurable in bank 7 grouping.
M8	TRX84	IO	Transmitter or Receiver electrode, configurable in bank 7 grouping.
M9	GUARD1	Output	Guard amplifier 0 output
N1	TRX30	IO	Transmitter or Receiver electrode, configurable in bank 2 grouping.
N2	TRX28	IO	Transmitter or Receiver electrode, configurable in bank 2 grouping.
N3	TRX25	IO	Transmitter or Receiver electrode, configurable in bank 2 grouping.
N4	TRX26	IO	Transmitter or Receiver electrode, configurable in bank 2 grouping.
N6	TRX86	IO	Transmitter or Receiver electrode, configurable in bank 7 grouping.
N7	TRX88	IO	Transmitter or Receiver electrode, configurable in bank 7 grouping.
N8	TRX87	IO	Transmitter or Receiver electrode, configurable in bank 7 grouping.
N9	TRX85	IO	Transmitter or Receiver electrode, configurable in bank 7 grouping.
P1	TRX27	IO	Transmitter or Receiver electrode, configurable in bank 2 grouping.
P2	TRX22	IO	Transmitter or Receiver electrode, configurable in bank 2 grouping.
P3	TRX23	IO	Transmitter or Receiver electrode, configurable in bank 2 grouping.
P4	TRX24	IO	Transmitter or Receiver electrode, configurable in bank 2 grouping.
P6	TRX89	IO	Transmitter or Receiver electrode, configurable in bank 7 grouping.
P7	TRX90	IO	Transmitter or Receiver electrode, configurable in bank 7 grouping.
P8	TRX93	IO	Transmitter or Receiver electrode, configurable in bank 7 grouping.
P9	TRX91	IO	Transmitter or Receiver electrode, configurable in bank 7 grouping.
R1	TRX18	IO	Transmitter or Receiver electrode, configurable in bank 1 grouping.
R2	TRX19	IO	Transmitter or Receiver electrode, configurable in bank 1 grouping.
R3	TRX20	IO	Transmitter or Receiver electrode, configurable in bank 1 grouping.
R4	TRX21	IO	Transmitter or Receiver electrode, configurable in bank 1 grouping.
R6	TRX96	IO	Transmitter or Receiver electrode, configurable in bank 8 grouping.
R7	TRX92	IO	Transmitter or Receiver electrode, configurable in bank 7 grouping.
R8	TRX95	IO	Transmitter or Receiver electrode, configurable in bank 7 grouping.
R9	TRX94	IO	Transmitter or Receiver electrode, configurable in bank 7 grouping.
T1	TRX14	IO	Transmitter or Receiver electrode, configurable in bank 1 grouping.
T2	TRX15	IO	Transmitter or Receiver electrode, configurable in bank 1 grouping.
T3	TRX16	IO	Transmitter or Receiver electrode, configurable in bank 1 grouping.
T4	TRX17	IO	Transmitter or Receiver electrode, configurable in bank 1 grouping.

Pin Location	Signal	IO Type	Description
T5	TRX97	IO	Transmitter or Receiver electrode, configurable in bank 8 grouping.
T6	TRX98	IO	Transmitter or Receiver electrode, configurable in bank 8grouping.
T7	TRX99	IO	Transmitter or Receiver electrode, configurable in bank 8 grouping.
T8	TRX100	IO	Transmitter or Receiver electrode, configurable in bank 8 grouping.
T9	TRX103	IO	Transmitter or Receiver electrode, configurable in bank 8 grouping.
U1	TRX12	IO	Transmitter or Receiver electrode, configurable in bank 0 grouping.
U2	TRX6	IO	Transmitter or Receiver electrode, configurable in bank 0 grouping.
U3	TRX5	IO	Transmitter or Receiver electrode, configurable in bank 0 grouping.
U4	TRX13	IO	Transmitter or Receiver electrode, configurable in bank 1 grouping.
U5	TRX116	IO	Transmitter or Receiver electrode, configurable in bank 9 grouping.
U6	TRX113	IO	Transmitter or Receiver electrode, configurable in bank 9 grouping.
U7	TRX101	IO	Transmitter or Receiver electrode, configurable in bank 8 grouping.
U8	TRX102	IO	Transmitter or Receiver electrode, configurable in bank 8 grouping.
U9	TRX104	IO	Transmitter or Receiver electrode, configurable in bank 8 grouping.
V1	TRX11	IO	Transmitter or Receiver electrode, configurable in bank 0 grouping.
V2	TRX7	IO	Transmitter or Receiver electrode, configurable in bank 0 grouping.
V3	TRX4	IO	Transmitter or Receiver electrode, configurable in bank 0 grouping.
V4	TRX2	IO	Transmitter or Receiver electrode, configurable in bank 0 grouping.
V5	TRX117	IO	Transmitter or Receiver electrode, configurable in bank 9 grouping.
V6	TRX114	IO	Transmitter or Receiver electrode, configurable in bank 9 grouping.
V7	TRX111	IO	Transmitter or Receiver electrode, configurable in bank 9 grouping.
V8	TRX108	IO	Transmitter or Receiver electrode, configurable in bank 9 grouping.
V9	TRX106	IO	Transmitter or Receiver electrode, configurable in bank 9 grouping.
W1	TRX9	IO	Transmitter or Receiver electrode, configurable in bank 0 grouping.
W2	TRX8	IO	Transmitter or Receiver electrode, configurable in bank 0 grouping.
W3	TRX1	IO	Transmitter or Receiver electrode, configurable in bank 0 grouping.
W4	TRX3	IO	Transmitter or Receiver electrode, configurable in bank 0 grouping.
W5	TRX0	IO	Transmitter or Receiver electrode, configurable in bank 0 grouping.
W6	TRX115	IO	Transmitter or Receiver electrode, configurable in bank 9 grouping.
W7	TRX112	IO	Transmitter or Receiver electrode, configurable in bank 9 grouping.
W8	TRX107	IO	Transmitter or Receiver electrode, configurable in bank 9 grouping.
W9	TRX105	IO	Transmitter or Receiver electrode, configurable in bank 9 grouping.
Y1	VDDTX	Test	Reserved, do not connect.
Y2	TRX10	IO	Transmitter or Receiver electrode, configurable in bank 0 grouping.
Y4	VDDRX	Filter Pin	Low-pass filtered version of VDDH used by DEMOD/FILT/ADC.
Y5	GNDRX	Power	Analog ground.
Y7	TRX110	IO	Transmitter or Receiver electrode, configurable in bank 9 grouping.
Y8	TRX109	IO	Transmitter or Receiver electrode, configurable in bank 9 grouping.
Y9	VBBTX	Test	Reserved, do not connect.

Transmitter and receiver pin-out configurations

Table 13. TX and RX configurations

Bank0	Bank1	Bank2	Bank3	Bank4	Bank5	Bank6	Bank7	Bank8	Bank9
TRX0	TRX13	TRX22	TRX36	TRX45	TRX59	TRX73	TRX82	TRX96	TRX105
TRX1	TRX14	TRX23	TRX37	TRX46	TRX60	TRX74	TRX83	TRX97	TRX106
TRX2	TRX15	TRX24	TRX38	TRX47	TRX61	TRX75	TRX84	TRX98	TRX107
TRX3	TRX16	TRX25	TRX39	TRX48	TRX62	TRX76	TRX85	TRX99	TRX108
TRX4	TRX17	TRX26	TRX40	TRX49	TRX63	TRX77	TRX86	TRX100	TRX109
TRX5	TRX18	TRX27	TRX41	TRX50	TRX64	TRX78	TRX87	TRX101	TRX110
TRX6	TRX19	TRX28	TRX42	TRX51	TRX65	TRX79	TRX88	TRX102	TRX111
TRX7	TRX20	TRX29	TRX43	TRX52	TRX66	TRX80	TRX89	TRX103	TRX112
TRX8	TRX21	TRX30	TRX44	TRX53	TRX67	TRX81	TRX90	TRX104	TRX113
TRX9	—	TRX31	—	TRX54	TRX68	—	TRX91	—	TRX114
TRX10	—	TRX32	—	TRX55	TRX69	—	TRX92	—	TRX115
TRX11	—	TRX33	—	TRX56	TRX70	—	TRX93	—	TRX116
TRX12	—	TRX34	—	TRX57	TRX71	—	TRX94	—	TRX117
—	—	TRX35	—	TRX58	TRX72	—	TRX95	—	—

Table 14. S7817 165 BGA configurable pin options with a maximum of 72 RX and 46 TX

Axis Setting	0	1	2	3
Bank0	13R	13R	13R	13R
Bank1	9R	9R	9T	9T
Bank2	14R	14T	14R	14T
Bank3	9T	9T	9R	9R
Bank4	14T	14R	14T	14R
Bank5	14T	14R	14T	14R
Bank6	9T	9T	9R	9R
Bank7	14R	14T	14R	14T
Bank8	9R	9R	9T	9T
Bank9	13R	13R	13R	13R
Total RX	72	72	72	72
Total TX	46	46	46	46

Sample I²C schematic with +1.8V and +3V external power supplies

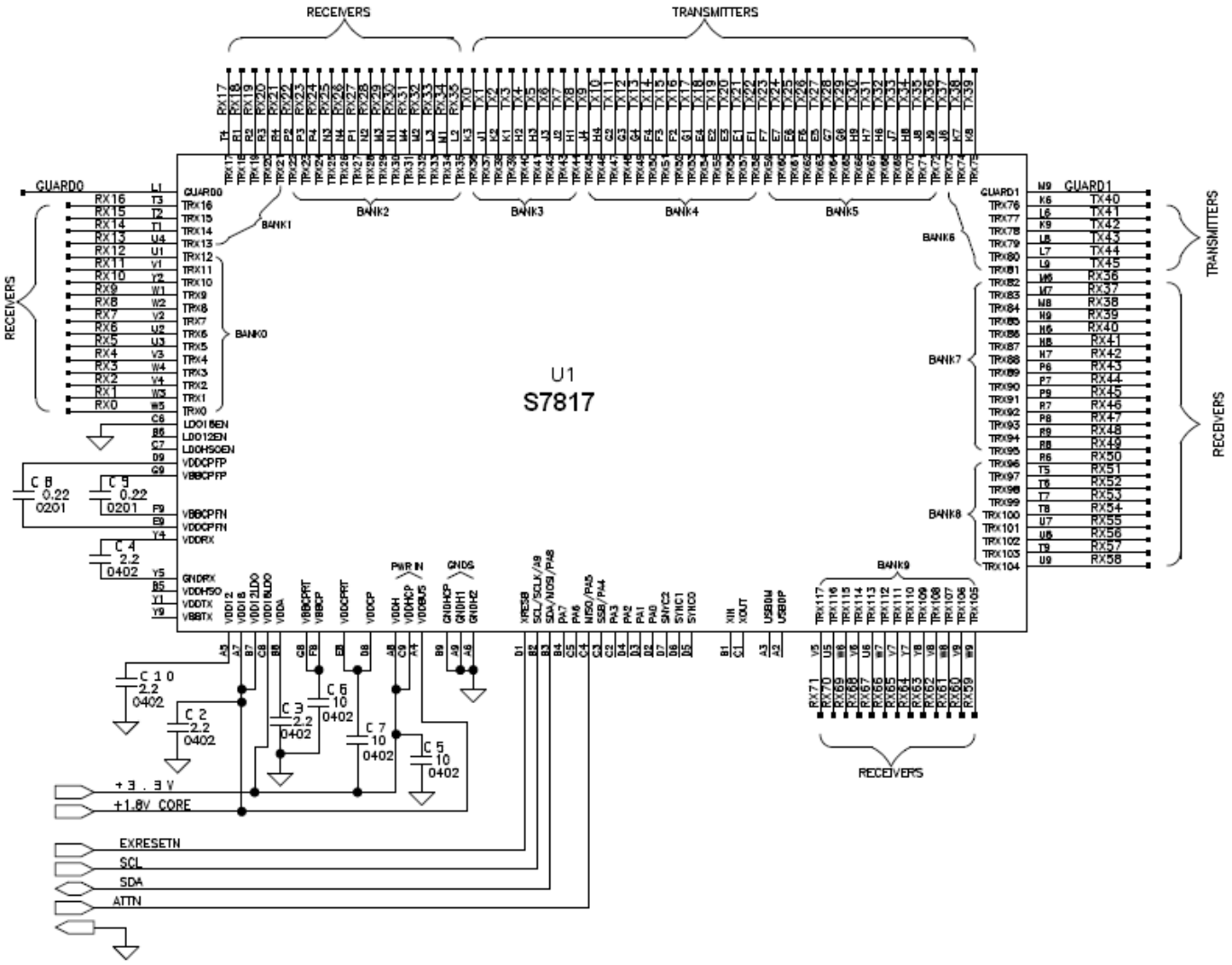

Figure 11. Sample I²C schematic with two external power supplies

Sample I²C schematic parts designator

The component values shown in the following table are typical values suitable for most applications. However, each system design has different requirements that may require different component values to better match that system. Please consult your Synaptics FAE if you have special system design requirements beyond those outlined in the datasheet.

Table 15. I²C schematic part designators

Designator	Description	Manufacturers Part Number
C2	CAPACITOR, 2.2UF, X5R, 20%, 6.3V, 0402	GRM155R60J225ME95D, JMK105BJ225MV-F, or equivalent
C3	CAPACITOR, 2.2UF, X5R, 20%, 6.3V, 0402	GRM155R60J225ME95D, JMK105BJ225MV-F, or equivalent
C4	CAPACITOR, 2.2UF, X5R, 20%, 6.3V, 0402	GRM155R60J225ME95D, JMK105BJ225MV-F, or equivalent
C5	CAPACITOR, 10UF, X5R, 20%, 6.3V, 0402	NMC0402X5R106M6.3TRPF, CL05A106MQ5NUNC, or equivalent
C6	CAPACITOR, 10UF, X5R, 20%, 6.3V, 0402	NMC0402X5R106M6.3TRPF, CL05A106MQ5NUNC, or equivalent
C7	CAPACITOR, 10UF, X5R, 20%, 6.3V, 0402	NMC0402X5R106M6.3TRPF, CL05A106MQ5NUNC, or equivalent
C8	CAPACITOR, 0.22UF, X5R, 20%, 6.3V, 0201	GRM033R60J224ME15D, or equivalent
C9	CAPACITOR, 0.22UF, X5R, 20%, 6.3V, 0201	GRM033R60J224ME15D, or equivalent
C10	CAPACITOR, 2.2UF, X5R, 20%, 6.3V, 0402	GRM155R60J225ME95D, JMK105BJ225MV-F, or equivalent

Sample USB schematic

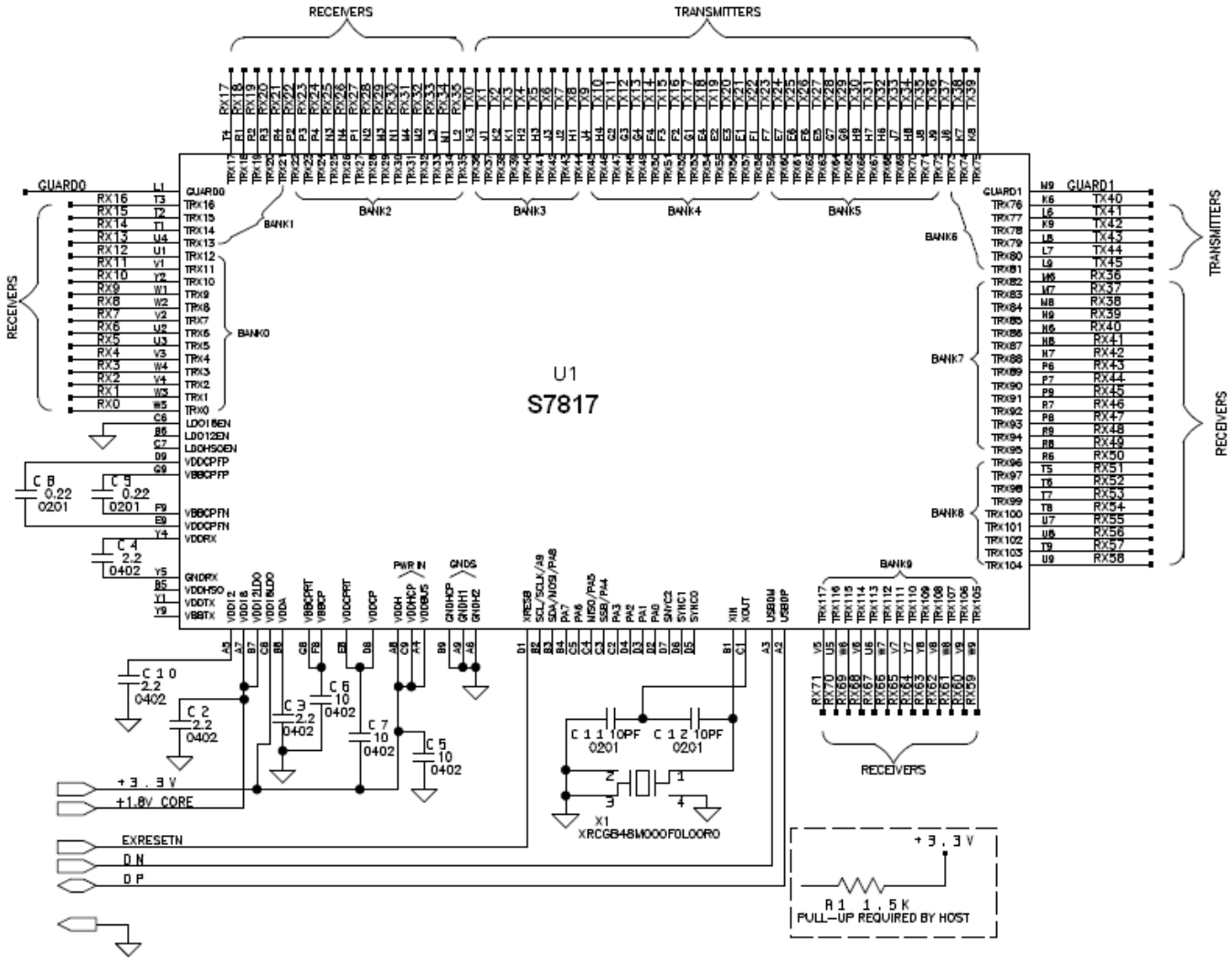

Figure 12. Sample USB schematic

Sample USB schematic parts designator

The component values shown in the following table are typical values suitable for most applications. However, each system design has different requirements that may require different component values to better match that system. Please consult your Synaptics FAE if you have special system design requirements beyond those outlined in the datasheet.

Table 16. USB schematic part designators

Designator	Description	Manufacturers Part Number
C2	CAPACITOR, 2.2UF, X5R, 20%, 6.3V, 0402	GRM155R60J225ME95D, JMK105BJ225MV-F, or equivalent
C3	CAPACITOR, 2.2UF, X5R, 20%, 6.3V, 0402	GRM155R60J225ME95D, JMK105BJ225MV-F, or equivalent
C4	CAPACITOR, 2.2UF, X5R, 20%, 6.3V, 0402	GRM155R60J225ME95D, JMK105BJ225MV-F, or equivalent
C5	CAPACITOR, 10UF, X5R, 20%, 6.3V, 0402	NMC0402X5R106M6.3TRPF, CL05A106MQ5NUNC, or equivalent
C6	CAPACITOR, 10UF, X5R, 20%, 6.3V, 0402	NMC0402X5R106M6.3TRPF, CL05A106MQ5NUNC, or equivalent
C7	CAPACITOR, 10UF, X5R, 20%, 6.3V, 0402	NMC0402X5R106M6.3TRPF, CL05A106MQ5NUNC, or equivalent
C8	CAPACITOR, 0.22UF, X5R, 20%, 6.3V, 0201	GRM033R60J224ME15D, or equivalent
C9	CAPACITOR, 0.22UF, X5R, 20%, 6.3V, 0201	GRM033R60J224ME15D, or equivalent
C10	CAPACITOR, 2.2UF, X5R, 20%, 6.3V, 0402	GRM155R60J225ME95D, JMK105BJ225MV-F, or equivalent
C11	CAPACITOR,10PF+/- 0.5PF,NPO, 25V, 0201	GRM0335C1E100JA01D, TMK063CG100DT-F, or equivalent
C12	CAPACITOR,10PF+/- 0.5PF,NPO, 25V, 0201	GRM0335C1E100JA01D, TMK063CG100DT-F, or equivalent
X11	CRYSTAL,48 MHZ,+/-100PPM , 2.0x1.6mm	XRCGB48M000F0L00R0, or equivalent

Package information

165 pin BGA package drawing

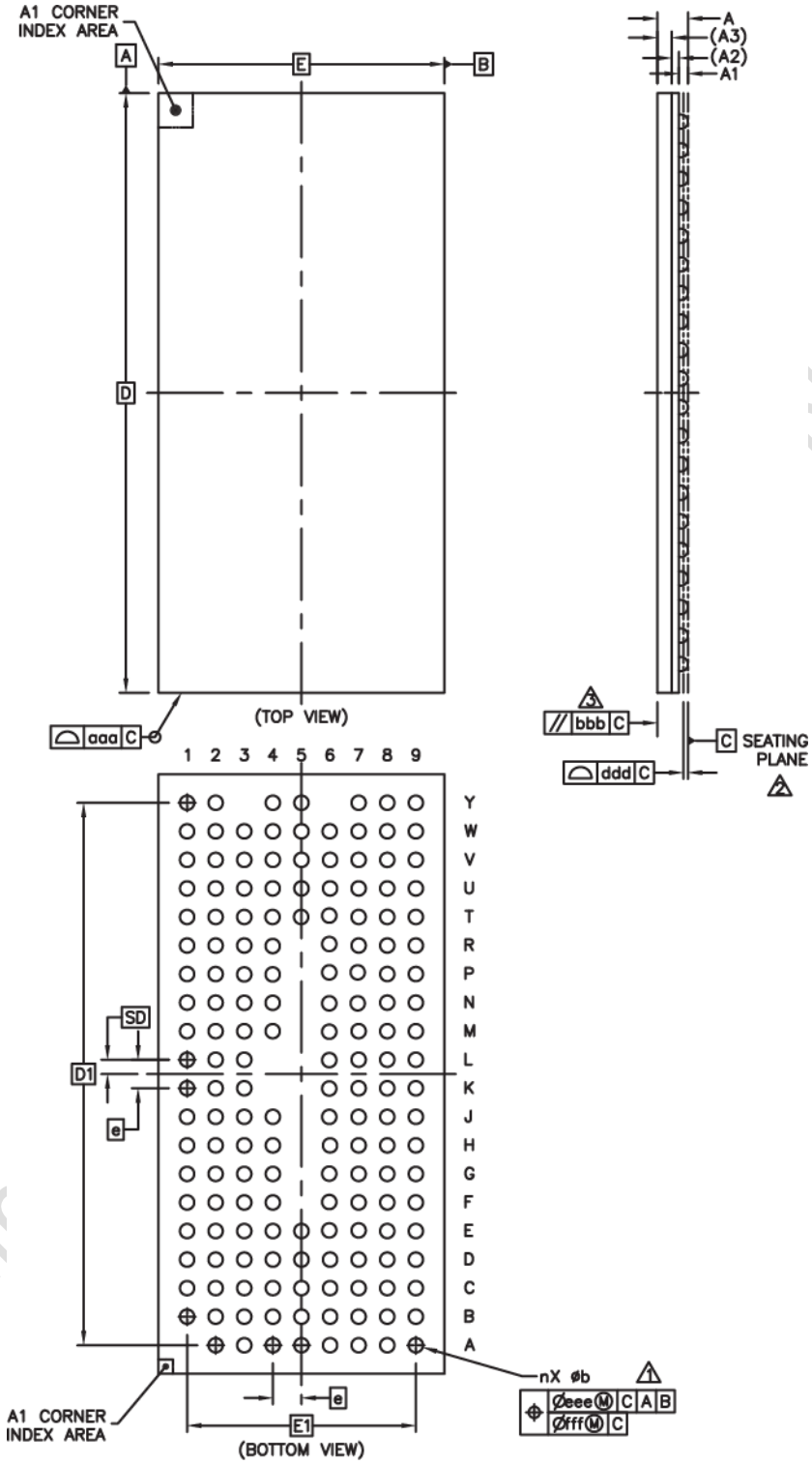

Figure 13. Package drawing

165 BGA pad package drawing

All measurements are given in millimeters unless otherwise specified.

Table 17. 165 pin BGA package dimensions

Aspect	Symbol	Common Dimensions		
		Minimum	Typical	Maximum
Total thickness	A	—	—	0.6
Stand off	A1	0.12	—	0.2
Substrate thickness	A2	0.125 REF		
Mold thickness	A3	0.25 REF		
Body size	D	10.5 BSC		
	E	5 BSC		
Ball diameter	Not applicable	—	0.25	—
Ball opening	Not applicable	—	0.25	—
Ball width	b	0.2	—	0.3
Ball pitch	e	0.5 BSC		
Ball count	n	—	165	—
Edge ball center to center	D1	9.5 BSC		
	E1	4 BSC		
Body center to contact ball	SD	0.25 BSC		
	SE	—	—	—
Package edge tolerance	a a a	—	0.1	—
Mold flatness	b b b	—	0.1	—
Coplanarity	d d d	—	0.08	—
Ball offset (package)	e e e	—	0.15	—
Ball offset (ball)	f f f	—	0.08	—

Package marking

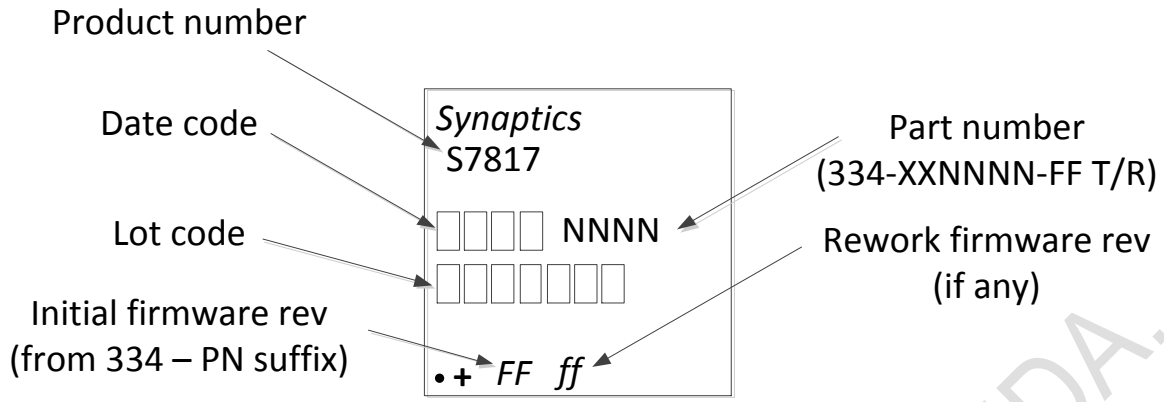

Figure 14. Package marking diagram

Shipment packaging

The S7817 touch controller can be shipped either in trays or in tape-and-reel packaging.

For information about tape-and-reel packaging, see the *ASIC Tape-and-Reel Specification* (PN: 528-000187-01).

For tray packaging specifics, please contact Synaptics.

Environmental and regulatory compliance

This Synaptics product is built in compliance with the *RoHS Directive and the Synaptics Quality Specification, Environmental Conservation Program* (PN: 526-000223-01). This product is also Halogen-Free (HF) compliant.

Reference documents

- *The I²C Bus Specification Version 2.1 Jan 2000* (http://www.nxp.com/acrobat_download/literature/9398/39340011.pdf)
- *ASIC Tape-and-Reel Package Specification* (PN: 528-000187-01)
- *Measuring Touch Performance on Synaptics ClearPad Products* (PN: 506-000502-01)
- RoHS Directive and the Synaptics Quality Specification, Environmental Conservation Program (PN: 526-000223-01).
- *Synaptics RMI4 Specification* (PN: 511-000405-01)
- *Touch Controller Ordering Guide* (PN: 511-000481-01)

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Revision history

Revision	ECO	Description
1	62236	Initial preliminary release.

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