

# eragon

820

## Hardware Reference Manual



Designed by  eInfochips

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## 1 Document Details

### 1.1 Document History

Version	Author		Reviewer		Approver		Description Of Changes
	Name	Date	Name	Review Date	Name	Date	
Release 1.0	eInfochips	22-March-16	eInfochips	27-March-16	eInfochips	27-March-16	Initial release
Release 1.1	eInfochips	30-May-17	eInfochips	12-Jun-17	eInfochips	12-Jun-17	Release updated

Table 1: Documents History

### 1.2 Definition, Acronyms and Abbreviations

Definition/Acronym/Abbreviation	Description
SOM	System On Module
BLE	Bluetooth Low Energy
BOM	Bill of Material
Bpp	Bits Per Pixel
BT	Bluetooth
CPU	Central Processing Unit
CSI	Camera Serial Interface
DC	Direct Current
DDR	Double Data Rate
DMIPS	Dhrystone MIPS (Million Instructions Per Second)
DSI	Display Serial Interface
el	eInfochips
GB	Giga Byte
GPIO	General Purpose Input output

GPS	Global Positioning System
HD	High Definition
HDMI	High Definition Multimedia Interface
HSIC	High-speed Serial Interface Connect
I/O	Input/Output
I2C	Inter-IC (Integrated Circuit)
IC	Integrated Circuit
JTAG	Joint Test Application Group
KB	Kilo Byte
LAN	Local Area Network
LNA	Low Noise Amplifier
LPDDR	Lower Power DDR
MB	Mega Byte
Mbps	Mega Bits Per Second
MIPI	Mobile Industry Processor Interface
MIPS	Million Instruction Per Second
MISO	Master In Slave Out
mm	Millimeter
MMC	Multi Media Card
MOSI	Master Out Slave In
MP	Mega Pixel
MPP	Multipurpose Pin
OTG	On The Go
PCIe	Peripheral Component Interface – Express
PLL	Phase-Locked Loop
PMIC	Power Management IC

RAM	Random Access Memory
RF	Radio Frequency
RH	Relative Humidity
RoHS	Restriction of Hazardous Substances
Rx	Receiver
SATA	Serial Advanced Technology Attachment
SiP	System In Package
SMPS	Switched Mode Power Supply
SOM	System On Module
SPI	Serial peripheral Interface
Tx	Transmitter
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VCO	Voltage Controlled Oscillator
WLAN	Wireless LAN
PCM	Pulse Coded Modulation

**Table 2: Definition, Acronyms and Abbreviations**

### 1.3 References

Sr. No.	Document	Version	Remarks
1	ERAGON820_Carrier Schematic File	1.0	
2	ERAGON820_Carrier Layout File	1.0	

**Table 3: References**

## 2 License Agreement

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### 3 Preface

This document provides an overview of the ERAGON820 Carrier design based on Qualcomm's APQ8096 SoC. It provides detailed information about the hardware components and associated software (Android 6.0.1).

#### 3.1 Intended Audience

This document is intended for technically qualified personnel. It is not intended for general audience.

#### 3.2 Intended Use

The development platform supports a wide range of industry interfaces and offers a comprehensive hardware and software design. It comes with Android 6.0.1 software packages and sample demo applications for easy adaption.

This platform enables developers to evaluate and create solutions targeted at various market segments while customers and OEMs can build their products based on these designs directly or with customizations.

## 4 Overview

The ERAGON820 Carrier board is based on ERAGON820 SOM for developers to accelerate the application development process and is ideal for rapid prototyping of the end product. With support for almost all the peripherals, it reduces the design time of innovative applications and helps achieve early time to market. With variety of peripherals, this kit is targeted for wide range of applications supporting bulk storage, faster connectivity, higher through put and performance at lower power.

### 4.1 Applications

The ERAGON820 Carrier with ERAGON820 SOM can be used in a wide range of products across many different target markets. Some of the typical applications are:

- Domestic Robot security & Surveillance
- Biometric Access Control Systems
- Human-machine interface
- Portable medical Instruments
- Machine vision
- IoT
- Robotic Applications

## 5 ERAGON820 Carrier Board Block Diagram

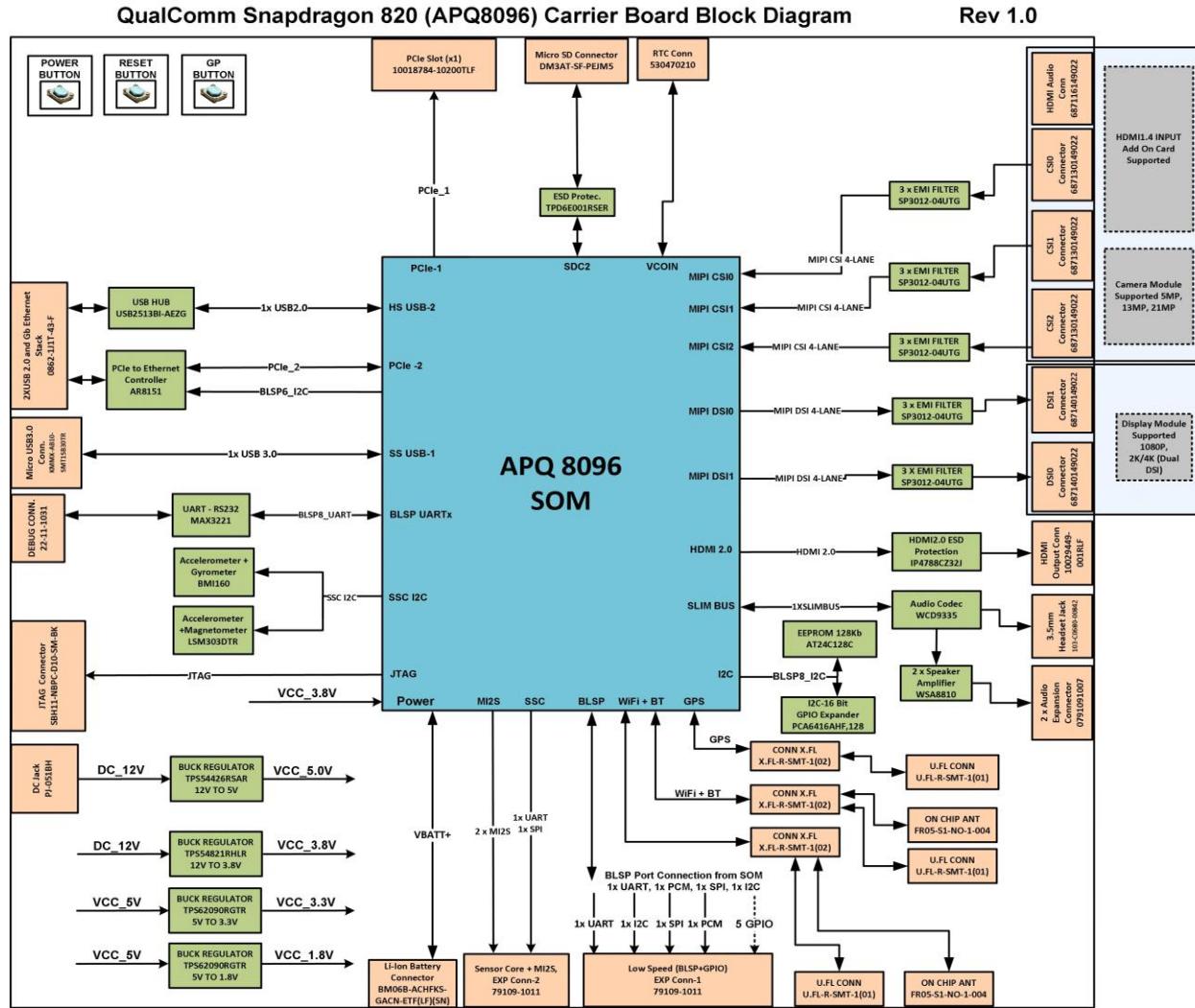


Figure 1: ERAGON820 Carrier Block Diagram

## 5.1 ERAGON820 Development Board

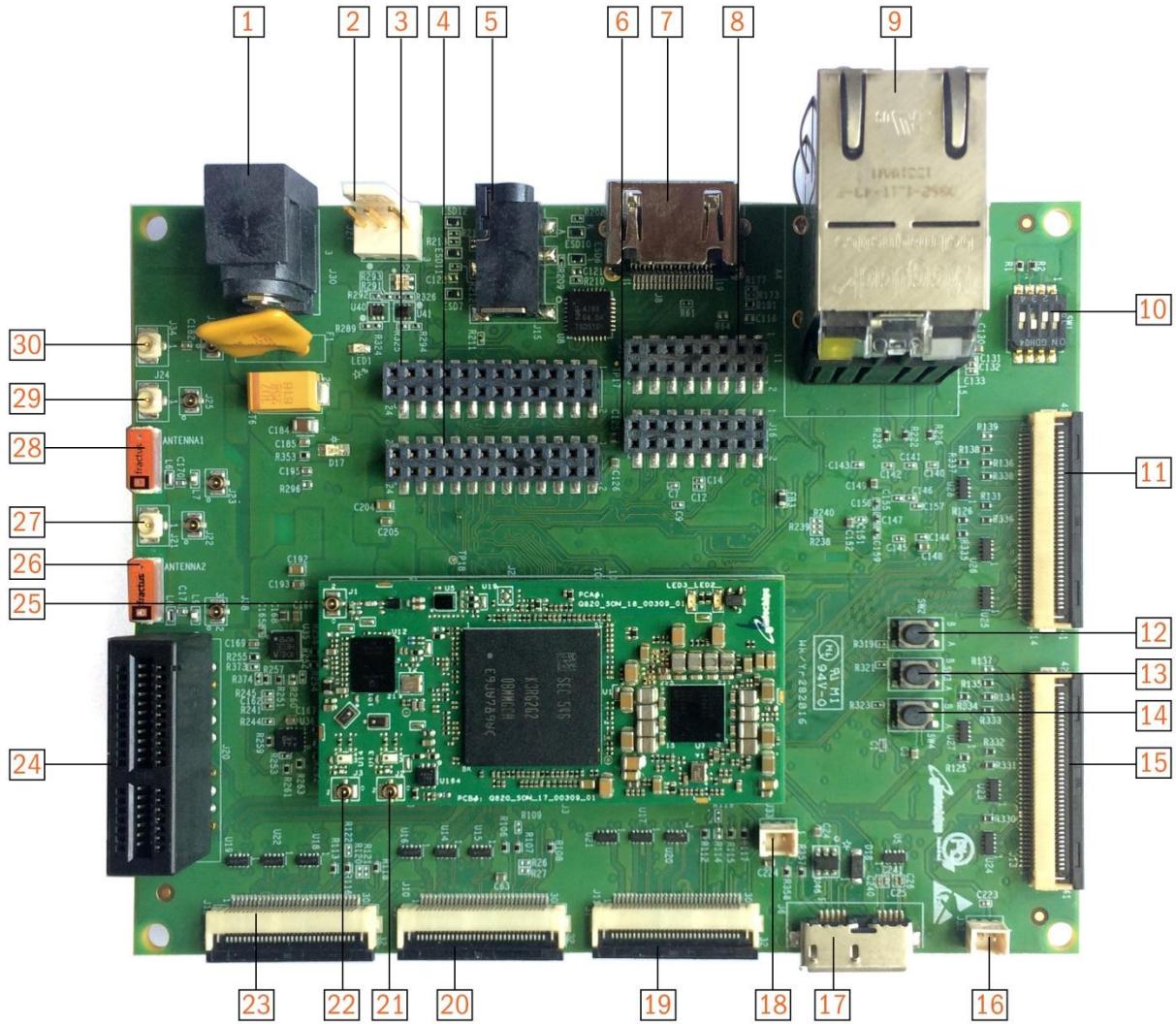


Figure 2: Top View of ERAGON820 CARRIER

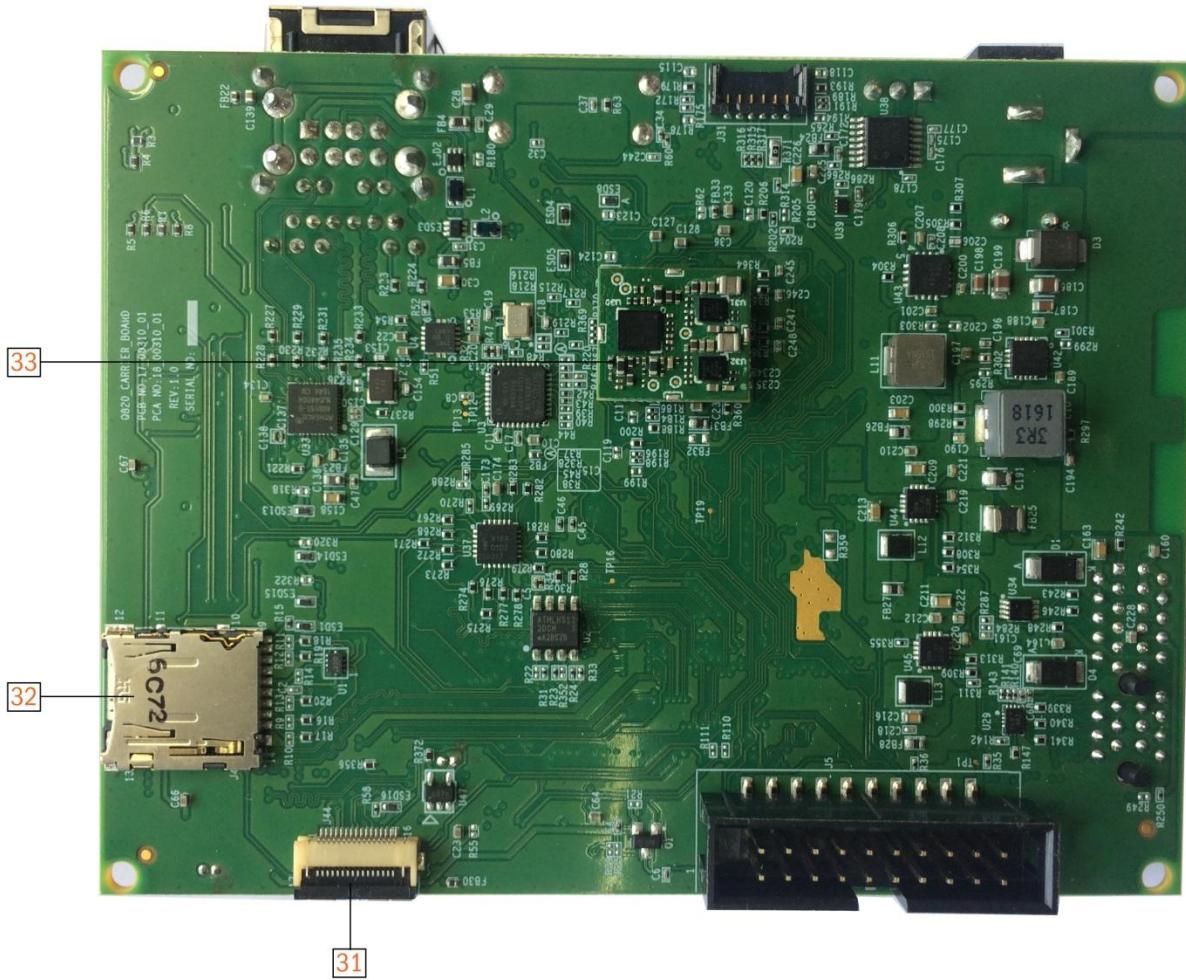


Figure 3: Bottom View of ERAGON820 CARRIER

The ERAGON 820 board supports a wide array of interfaces and peripherals, including several high speed signals through its edge connector. Other salient features include the on-board antenna connectors for WiFi, Bluetooth and GPS interface.

ERAGON820 Components Details	
1	DC Power Jack
2	Serial Debug Port
3	Sensor Core Expansion Connector
4	Low Speed Expansion Connector
5	Headset Jack
6	Digital Expansion Connector
7	HDMI Connector
8	Analog Expansion Connector
9	Ethernet Jack
10	Boot Switch Button
11	DSI1 Connector
12	Power Button
13	Volume Up Button
14	Volume Down Button
15	DSI0 Connector
16	RTC Battery Connector
17	USB 3.0 Connector
18	DC Fan Connector
19	CSI1 connector
20	CSI0 Connector
21	WiFi/Bluetooth Connector
22	WiFi/Bluetooth Connector
23	CSI2 Connector
24	PCIe Card connector
25	GPS Connector for External Antenna
26	WiFi Antenna
27	External WiFi Antenna Connector
28	WiFi Antenna
29	External WiFi Antenna Connector
30	GPS Connector for External Antenna
31	HDMI Audio Connector
32	SD Card Connector
33	Audio Board Connector

Table 4: ERAGON820 Components Details

The ERAGON820 Carrier has three Hirose DF40C-100DP-0.4V (51) Connectors. The pinouts for these connectors is described as follows.

Pin No.	Net Name	Default Pin Function
J1.1	MIPI_DSI0_CLK_P	MIPI DSIO 3 Clock line High out
J1.2	MIPI_DSI0_D3_P	MIPI DSIO 3 Data3 High out
J1.3	MIPI_DSI0_CLK_M	MIPI DSIO Clock line Low out
J1.4	MIPI_DSI0_D3_M	MIPI DSIO Data3 Low out
J1.5	GND	Digital Ground
J1.6	GND	Digital Ground
J1.7	DSI_BACKLIGHT_PWM	PWM Signal for External Display
J1.8	MIPI_DSI0_D2_P	MIPI DSIO Data2 High out
J1.9	CSI_I2C1_SDA	I2C interface Data for CSI
J1.10	MIPI_DSI0_D2_M	MIPI DSIO Data2 Low out
J1.11	CSI_I2C1_SCL	I2C interface Clock for CSI
J1.12	GND	Digital Ground
J1.13	CSI_I2C0_SDA	I2C interface Data for CSI
J1.14	MIPI_DSI0_D0_M	MIPI DSIO Data0 Low out
J1.15	CSI_I2C0_SCL	I2C interface Clock for CSI
J1.16	MIPI_DSI0_D0_P	MIPI DSIO Data0 High out
J1.17	BLSP12_DSI_I2C_SCL	BLSP interface I2C Clock for DSI
J1.18	GND	Digital Ground
J1.19	BLSP12_DSI_I2C_SDA	BLSP interface I2C Data Lane for DSI
J1.20	MIPI_DSI0_D1_P	MIPI DSIO Data1 High out
J1.21	BLSP8_I2C_SCL	BLSP interface I2C Clock
J1.22	MIPI_DSI0_D1_M	MIPI DSIO Data1 Low out
J1.23	HDMI_HOTPLUG_DET	HDMI Hot Plug Detect Signal
J1.24	GND	Digital Ground
J1.25	HDMI_CEC	HDMI interface CEC line
J1.26	USB1_SS_TM	Super Speed USB interface TX –Low
J1.27	USB_HUB_RESET_N	USB HUB RESET signal (active low)
J1.28	USB1_SS_TP	Super Speed USB interface TX –HIGH
J1.29	HDMI_DDC_CLK	HDMI interface DDC clock line
J1.30	GND	Digital Ground
J1.31	HDMI_DDC_DATA	HDMI interface DDC data line
J1.32	USB1_SS_RP	Super Speed USB interface RX –HIGH

J1.33	BLSP9_SPI_CLK	BLSP interface SPI Clock
J1.34	USB1_SS_RM	Super Speed USB interface RX –LOW
J1.35	BLSP8_UART_TX	BLSP interface UART TX
J1.36	GND	Digital Ground
J1.37	BLSP8_UART_RX	BLSP interface UART RX
J1.38	BOOT_CONFIG_2	Boot configuration bit 2
J1.39	PCIE2_CLK_REQ_N	PCIE Clock Request Signal (active Low)
J1.40	BOOT_CONFIG_3/CSI1_RST	Boot configuration bit 2 / CSI1 RESET Signal
J1.41	PCIE2_WAKE_N	PCIE interface WAKE Signal (Active Low)
J1.42	USB_BOOT/HDMI_MI2S_4_MCLK	USB BOOT Signal/ HDMI MI2S 4 Master Clock
J1.43	BLSP8_I2C_SDA	BLSP interface I2C Data Line
J1.44	MAG_SENSOR_INT1	Interrupt Signal for Magneto sensor
J1.45	PCIE2_RST_N	PCIE interface RESET Signal (Active Low)
J1.46	MAG_SENSOR_INT2	Interrupt Signal for Magneto sensor
J1.47	AUDIO_INT1	Interrupt Signal for Audio interface
J1.48	ALSPG_INT_N	Processor GPIO for Sensors
J1.49	TX_GTR_THRES	PMIC GPIO for Sensors
J1.50	GYRO_SENSOR_INT2	Interrupt Signal for Gyro Sensor
J1.51	BLSP9_SPI_CS_N	BLSP interface for SPI Chip select
J1.52	BATT_THERM	Battery Thermistor Pin
J1.53	BLSP9_SPI_MISO	BLSP interface for SPI MISO
J1.54	GND	Digital Ground
J1.55	BLSP9_SPI_MOSI	BLSP interface for SPI MOSI
J1.56	AUDIO_INT2	Interrupt Signal for Audio interface
J1.57	VREG_S12A_1P15	1.15V Supply for Carrier Board
J1.58	VOLUME_UP_N	Volume UP pin for Audio (Active Low)
J1.59	VREG_S12A_1P15	1.15V Supply for Carrier Board
J1.60	GND	Digital Ground
J1.61	PM_RESIN_N	PMIC RESET input pin (Active Low)
J1.62	PM_MPP_GPIO_07	PMIC MPP GPIO pin on Carrier Board
J1.63	PHONE_ON_N	PHONE ON General purpose pin
J1.64	DSIO_RST_N	RESET pin for DSI interface
J1.65	PM_MPP_GPIO_06	PMIC GPIO on Carrier Board
J1.66	GND	Digital Ground

J1.67	USB_SS_ID	Super Speed USB ID detect pin
J1.68	GYRO_SENSOR_INT1	Interrupt Signal for Gyro Sensor
J1.69	PM_MPP_GPIO_02	PMIC GPIO for Carrier Board
J1.70	DSI_TOUCH_INT	Interrupt Signal for DSI Touchscreen
J1.71	PM_MPP_GPIO_04	PMIC GPIO for Carrier Board
J1.72	BOOT_CONFIG_1	Boot configuration bit 1
J1.73	GND	Digital Ground
J1.74	HDMI_MI2S_4_D3	HDMI MI2S 4 Data Lane 3 signal
J1.75	VREG_L13A_2P95	2.95V Supply for Carrier Board
J1.76	HDMI_MI2S_4_D0	HDMI MI2S 4 Data Lane 0 signal
J1.77	VREG_L13A_2P95	2.95V Supply for Carrier Board
J1.78	HDMI_MI2S_4_WS	HDMI MI2S 4 Word Select signal
J1.79	USB_HS1_VBUS_DET	High Speed USB VBUS Detect signal
J1.80	HDMI_MI2S_4_D1	HDMI MI2S 4 Data Lane 1 signal
J1.81	GND	Digital Ground
J1.82	HDMI_MI2S_4_SCK	HDMI MI2S 4 Serial Clock signal
J1.83	VCOIN	Input supply from Coin Cell Battery
J1.84	HDMI_MI2S_4_D2	HDMI MI2S 4 Data Lane 2 signal
J1.85	VREG_L21A_2P95	2.95V Supply for Carrier Board
J1.86	LTE_COEX_RX	LTE COEX RX test Point Pin.
J1.87	VREG_L21A_2P95	2.95V Supply for Carrier Board
J1.88	LTE_COEX_TX	LTE COEX TX test Point Pin.
J1.89	VREG_S4A_1P8	1.8V Supply for Carrier Board
J1.90	VREG_S4A_1P8	1.8V Supply for Carrier Board
J1.91	VREG_S4A_1P8	1.8V Supply for Carrier Board
J1.92	GND	Digital Ground
J1.93	VREG_S4A_1P8	1.8V Supply for Carrier Board
J1.94	GND	Digital Ground
J1.95	AUDIO_CODEC_MCLK	Audio Codec Interface Master Clock Pin
J1.96	GND	Digital Ground
J1.97	VREG_1P225	1.225V Supply for Carrier Board.
J1.98	GND	Digital Ground
J1.99	VREG_1P225	1.225V Supply for Carrier Board.
J1.100	GND	Digital Ground

**Table 5: Board to Board Connector J1**

Pin No.	Net Name	Default Pin Function
J2.1	VBATT+	Main battery Input supply (3.8V)
J2.2	VBATT+	Main battery Input supply (3.8V)
J2.3	VBATT+	Main battery Input supply (3.8V)
J2.4	VBATT+	Main battery Input supply (3.8V)
J2.5	VBATT+	Main battery Input supply (3.8V)
J2.6	VBATT+	Main battery Input supply (3.8V)
J2.7	VBATT+	Main battery Input supply (3.8V)
J2.8	VBATT+	Main battery Input supply (3.8V)
J2.9	VBATT+	Main battery Input supply (3.8V)
J2.10	VBATT+	Main battery Input supply (3.8V)
J2.11	VBATT+	Main battery Input supply (3.8V)
J2.12	VBATT+	Main battery Input supply (3.8V)
J2.13	VBATT+	Main battery Input supply (3.8V)
J2.14	VBATT+	Main battery Input supply (3.8V)
J2.15	VBATT+	Main battery Input supply (3.8V)
J2.16	VBATT+	Main battery Input supply (3.8V)
J2.17	USB_VBUS	USB Input power supply
J2.18	VBATT+	Main battery Input supply (3.8V)
J2.19	USB_VBUS	USB_VBUS Input supply
J2.20	USB2_VBUS_DET	USB2 input power Detection pin Test Point.
J2.21	USB_VBUS	USB Input power supply
J2.22	SPKR_AMP_EN1	Speaker Amplifier1 Enable
J2.23	USB_VBUS	USB Input power supply
J2.24	SPKR_AMP_EN2	Speaker Amplifier2 Enable
J2.25	GND	Digital Ground
J2.26	VSENSE_BATT_P	Battery Supply High Sense pin
J2.27	LEDO_RED_DRV	RGB LED driver(From PMI8994)
J2.28	VSENSE_BATT_M	Battery Supply Low Sense pin
J2.29	LEDO_GREEN_DRV	RGB LED driver(From PMI8994)
J2.30	WLED_VREG	LCD Back Light supply
J2.31	LEDO_BLUE_DRV	RGB LED driver (From PMI8994)
J2.32	WLED_SINK1	WLED Low Side Input Sink1
J2.33	LED1_GREEN_DRV	RGB LED driver(From PMI8994)
J2.34	WLED_SINK2	WLED Low Side Input Sink2

J2.35	PCIE1_RST_N	PCIE Slot Reset Pin
J2.36	BACKLIGHT_CNTL	LCD Backlight Control PWM
J2.37	PCIE1_WAKE_N	PCIE Slot Wake GPIO
J2.38	GND	Digital Ground
J2.39	PCIE1_CLK_REQ_N	PCIE Slot CLK Request GPIO Pin
J2.40	USB1_HS_DM	USB Interface 1 Data Low line
J2.41	CLK_SDC2_SD_CARD	SD Card CLK Pin
J2.42	USB1_HS_DP	USB Interface 1 Data HIGH line
J2.43	BLSP6_I2C_SDA	BLSP6 I2C Data lane
J2.44	GND	Digital Ground
J2.45	BLSP3_I2C_SDA	BLSP3 I2C Data lane
J2.46	USB2_HS_DM	USB interface 2 data LOW line
J2.47	SD_CARD_DET	SD Card Detection Pin
J2.48	USB2_HS_DP	USB Interface 2 Data High line
J2.49	BLSP6_I2C_SCL	BLSP6 I2C Clock lane
J2.50	GND	Digital Ground
J2.51	BLSP1_UART_RX	BLSP1 UART RX Data lane
J2.52	JTAG_TDO	JTAG interface TDO Pin
J2.53	AUDIO_SLIMBUS_D0	Audio-Slim Bus Interface Data 0 Pin.
J2.54	JTAG_SRST_N	JTAG Interface System Reset Pin.
J2.55	AUDIO_SLIMBUS_D1	Audio-Slim Bus Interface Data 1 Pin.
J2.56	JTAG_TRST_N	JTAG interface Reset Pin.
J2.57	BLSP3_I2C_SCL	BLSP3 I2C Clock lane
J2.58	JTAG_TMS	JTAG interface TMS Pin.
J2.59	BLSP1_UART_CTS_N	BLSP1 UART Clear To Send Pin
J2.60	JTAG_TDI	JTAG interface Data Input Pin.
J2.61	SDC2_DAT3	SDC2 Interface Data 3 lane
J2.62	JTAG_TCK	JTAG interface Clock Pin
J2.63	SDC2_CMD	SDC2 Interface Command line
J2.64	PCM2_CLK	PCM interface 2 Clock line
J2.65	SDC2_DAT0	SDC2 Interface Data 0 lane
J2.66	CODEC_RST_N	Audio Codec Reset Pin
J2.67	SDC2_DAT2	SDC2 Interface Data 2 lane
J2.68	PCM2_DIN	PCM Interface 2 Data input
J2.69	SDC2_DAT1	SDC2 Interface data lane 1

J2.70	PCM2_SYNC	PCM Interface 2 SYNC Pin
J2.71	BLSP1_UART_RTS_N	BLSP1 UART Ready To Send Pin
J2.72	PCM2_DOUT	PCM interface 2 DOUT Pin
J2.73	BLSP1_UART_TX	BLSP1 UART Ready To Send Pin
J2.74	MI2S_3_D0	MI2S Interface 3 Data 0
J2.75	AUDIO_SLIMBUS_CLK	Slim bus Interface Clock pin.
J2.76	MI2S_3_MCLK	MI2S Interface 3 Clock Pin
J2.77	APQ_RESET_N	APQ Reset Out Pin Test Point
J2.78	MI2S_3_D1	MI2S Interface 3 Data 1 Pin
J2.79	SSC_PWR_EN	SSC Power Enable Pin
J2.80	MI2S_3_WS	MI2S Interface 3 WS Pin
J2.81	SSC_I2C_2_SDA	SSC Interface I2C2 Data lane
J2.82	MI2S_3_SCK	MI2S Interface 3 Serial Clock Pin
J2.83	SSC_I2C_2_SCL	SSC Interface I2C 2 Clock lane
J2.84	HDMI_RST_N	HDMI Input Reset Pin (Active Low)
J2.85	SSC_SYNC_OUT	SSC Interface Sync Out Pin
J2.86	GND	Digital Ground
J2.87	SSC_SPI_3_MISO	SSC Interface SPI 3 MISO Pin
J2.88	HDMI_INT_GPIO	HDMI Input Interrupt Pin.
J2.89	SSC_SPI_3_CS_N	SSC Interface SPI 3 Chip Select Pin
J2.90	SSC_UART_3_RX	SSC Interface UART 3 Receive Pin
J2.91	SSC_SPI_3_CLK	SSC Interface SPI 3 Clock Pin
J2.92	SSC_I2C_1_SDA	SSC Interface I2C 1 Data lane
J2.93	SSC_SPI_3_MOSI	SSC Interface SPI 3 MOSI Pin
J2.94	GND	Digital Ground
J2.95	SSC_I2C_1_SCL	SSC Interface I2C 1 Clock lane
J2.96	USB3OTG_VBUS_EN	USB3 OTG VBUS Enable Pin.
J2.97	SSC_UART_3_TX	SSC Interface UART 3 Transmit Pin
J2.98	CSI2_RST	MIPI CSI2 Camera Reset Pin.
J2.99	JTAG_PS_HOLD	JTAG PS Hold Pin
J2.100	CSI0_RST	MIPI CSI0 Camera Reset Pin.

Table 6: Board to Board Connector J2

Pin No.	Net Name	Default Pin Function
J3.1	HDMI_TX2_M	HDMI interface line 2 Low Output
J3.2	GND	Digital Ground
J3.3	HDMI_TX2_P	HDMI interface line 2 High Output
J3.4	MIPI_DSI1_D1_M	MIPI DSI1 Data 1 Low out
J3.5	GND	Digital Ground
J3.6	MIPI_DSI1_D1_P	MIPI DSI1 Data 1 High out
J3.7	HDMI_TX0_M	HDMI interface line 0 Low Output
J3.8	GND	Digital Ground
J3.9	HDMI_TX0_P	HDMI interface line 0 High Output
J3.10	MIPI_DSI1_CLK_M	MIPI DSI1 Clock line Low out
J3.11	GND	Digital Ground
J3.12	MIPI_DSI1_CLK_P	MIPI DSI1 Clock line High out
J3.13	MIPI_CSI1_D3_P	MIPI CSI1 Data3 High out
J3.14	GND	Digital Ground
J3.15	MIPI_CSI1_D3_M	MIPI CSI1 Data3 Low out
J3.16	MIPI_DSI1_D0_P	MIPI DSI1 Data0 High out
J3.17	GND	Digital Ground
J3.18	MIPI_DSI1_D0_M	MIPI DSI1 Data0 Low out
J3.19	MIPI_CSI1_D0_M	MIPI CSI1 Data0 Low out
J3.20	GND	Digital Ground
J3.21	MIPI_CSI1_D0_P	MIPI CSI1 Data0 High out
J3.22	MIPI_DSI1_D2_P	MIPI DSI1 Data2 High out
J3.23	GND	Digital Ground
J3.24	MIPI_DSI1_D2_M	MIPI DSI1 Data2 Low out
J3.25	MIPI_CSI1_D1_P	MIPI CSI1 Data1 High out
J3.26	GND	Digital Ground
J3.27	MIPI_CSI1_D1_M	MIPI CSI1 Data1 Low out
J3.28	MIPI_DSI1_D3_P	MIPI DSI1 Data3 High out
J3.29	GND	Digital Ground
J3.30	MIPI_DSI1_D3_M	MIPI DSI1 Data3 Low out
J3.31	MIPI_CSI1_D2_P	MIPI CSI1 Data2 High out
J3.32	GND	Digital Ground
J3.33	MIPI_CSI1_D2_M	MIPI CSI1 Data2 Low out
J3.34	HDMI_TX1_M	HDMI interface line 1 Low Output

J3.35	GND	Digital Ground
J3.36	HDMI_TX1_P	HDMI interface line 1 High Output
J3.37	MIPI_CSI1_CLK_M	MIPI CSI1 Clock line Low out
J3.38	GND	Digital Ground
J3.39	MIPI_CSI1_CLK_P	MIPI CSI1 Clock line High out
J3.40	HDMI_CLK_M	HDMI interface line Clock Low Output
J3.41	GND	Digital Ground
J3.42	HDMI_CLK_P	HDMI interface line Clock High Output
J3.43	CAM_MCLK1	MIPI CSI CAM Master Clock1 Pin
J3.44	GND	Digital Ground
J3.45	CAM_MCLK2	MIPI CSI CAM Master Clock2 Pin
J3.46	CSI_SW_SEL	CSI Switch Select GPIO Pin
J3.47	GND	Digital Ground
J3.48	GND	Digital Ground
J3.49	CAM_MCLK3	MIPI CSI CAM Master Clock3 Pin
J3.50	MIPI_CSIO_CLK_P	MIPI CSIO Clock line High out
J3.51	CAM_MCLK0	MIPI CSI CAM Master Clock0 Pin
J3.52	MIPI_CSIO_CLK_M	MIPI CSIO Clock line Low out
J3.53	GND	Digital Ground
J3.54	GND	Digital Ground
J3.55	MIPI_CSI2_CLK_M	MIPI CSI2 Clock line Low out
J3.56	MIPI_CSIO_D0_P	MIPI CSIO Data0 out
J3.57	MIPI_CSI2_CLK_P	MIPI CSI2 Clock line High out
J3.58	MIPI_CSIO_D0_M	MIPI CSIO Data0 Low out
J3.59	GND	Digital Ground
J3.60	GND	Digital Ground
J3.61	MIPI_CSI2_D0_M	MIPI CSI2 Data0 Low out
J3.62	MIPI_CSIO_D1_P	MIPI CSIO Data1 High out
J3.63	MIPI_CSI2_D0_P	MIPI CSI2 Data0 High out
J3.64	MIPI_CSIO_D1_M	MIPI CSIO Data1 Low out
J3.65	GND	Digital Ground
J3.66	GND	Digital Ground
J3.67	MIPI_CSI2_D1_P	MIPI CSI2 Data1 High out
J3.68	MIPI_CSIO_D2_P	MIPI CSIO Data2 High out
J3.69	MIPI_CSI2_D1_M	MIPI CSI2 Data1 Low out

J3.70	MIPI_CSIO_D2_M	MIPI CSIO Data2 Low out
J3.71	GND	Digital Ground
J3.72	GND	Digital Ground
J3.73	MIPI_CSIO_D2_P	MIPI CSIO Data2 High out
J3.74	MIPI_CSIO_D3_P	MIPI CSIO Data3 High out
J3.75	MIPI_CSIO_D2_M	MIPI CSIO Data2 Low out
J3.76	MIPI_CSIO_D3_M	MIPI CSIO Data3 Low out
J3.77	GND	Digital Ground
J3.78	GND	Digital Ground
J3.79	MIPI_CSIO_D3_P	MIPI CSIO Data3 High out
J3.80	PCIE1_CLK_M	PCIE interface 1 Clock Low Output
J3.81	MIPI_CSIO_D3_M	MIPI CSIO Data3 Low out
J3.82	PCIE1_CLK_P	PCIE interface 1 Clock High Output
J3.83	GND	Digital Ground
J3.84	GND	Digital Ground
J3.85	PCIE2_CLK_P	PCIE interface 2 Clock High Output
J3.86	PCIE1_RX_M	PCIE interface 1 Receive Low Output
J3.87	PCIE2_CLK_M	PCIE Interface 2 Clock Low Output
J3.88	PCIE1_RX_P	PCIE interface 1 Receive High Output
J3.89	GND	Digital Ground
J3.90	GND	Digital Ground
J3.91	PCIE2_RX_M	PCIE interface 2 Receive Low Output
J3.92	PCIE1_TX_M	PCIE interface 1 Transmit Low Output
J3.93	PCIE2_RX_P	PCIE interface 2 Receive High Output
J3.94	PCIE1_TX_P	PCIE interface 1 Transmit High Output
J3.95	GND	Digital Ground
J3.96	GND	Digital Ground
J3.97	PCIE2_TX_P	PCIE interface 2 Transmit High Output
J3.98	VREG_DISP	Supply for External Display High
J3.99	PCIE2_TX_M	PCIE interface 2 Transmit Low Output
J3.100	VREG_DISN	Supply for External Display Low Output

**Table 7: Board to Board Connector J3**

## 5.2 ERAGON820 Development Kit Major Blocks

### 5.2.1 Memory Interface

The ERAGON820 carrier board Micro SD slot signals are routed directly to the APQ8096 SDC2 interface from the Micro SD card connector (J4). The Connector is a push-push type with a dedicated support for card detect signal. The ERAGON820 carrier board uses Four Data Signals Starting from SDC2\_DATA0 to SDC2\_DATA3, one SDC2\_CMD for command, one CLK\_SDC2\_SD\_CARD Micro SD card Clock and One GPIO APQ GPIO\_95 as the SD\_CARD\_DET.

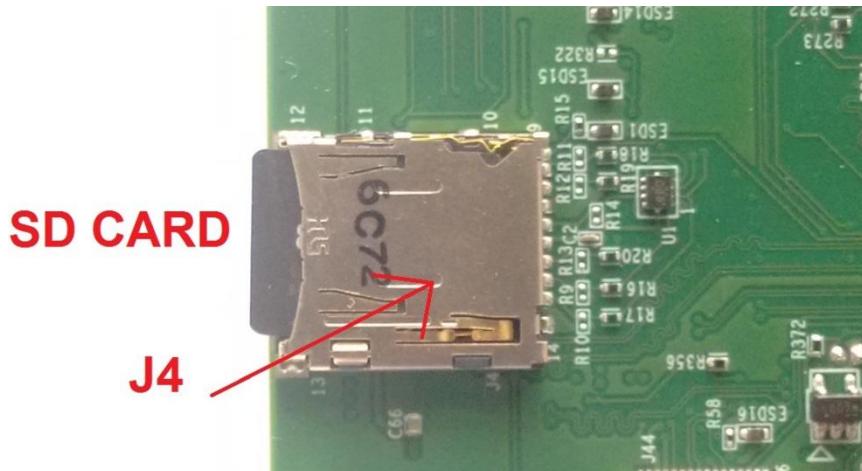


Figure 4: Micro SD slot

### 5.2.2 WiFi/BT

The ERAGON820 Carrier board deployed Qualcomm's RF chip QCA6174A-1 solution that integrates two different wireless connectivity technologies into a single device, to achieve this board contains an on chip antenna.

- WLAN dual-band 2x2 MIMO with IEEE802.11a/b/g/n/ac and Bluetooth V4.1.
- Supports WLAN 20MHz/40MHz at 2.4GHz and 20/40/80 MHz at 5GHz.
- Supports BT4.1+HS, BLE and be backwards compatible with BT1.x, 2.x+EDR.
- Supports BT for class 1 power level transmissions without requiring an external PA.
- Supports Low power PCIe(w/L1 sub-state) interface for WLAN and UART/PCM interface for BT.

**For Integrating On-Board Antenna** - Connect two X.FL cable between SOM and Carrier board. Connect cable from J2 connector of SOM to J23 connector of Carrier board. Similarly, connect cable from J3 connector of SOM to J38 connector of the Carrier board.

**For Integrating External Antenna** - Connect two X.FL cable between SOM and Carrier board. Connect cable from J2 connector of SOM to J22 connector of Carrier board. Similarly, connect cable from J3

connector of SOM to J25 connector of Carrier board. User can connect Wi-Fi external antenna on U.FL connectors on the J21 and J24 of the carrier Board.

Please refer to the following images to understand the Wi-Fi/Bluetooth connections.

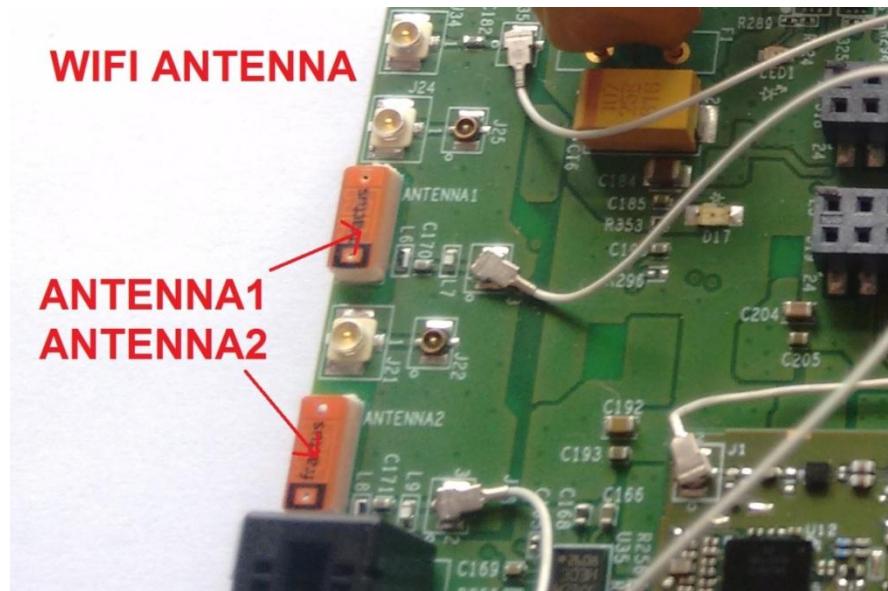


Figure 5: On Board Wi-Fi Connection

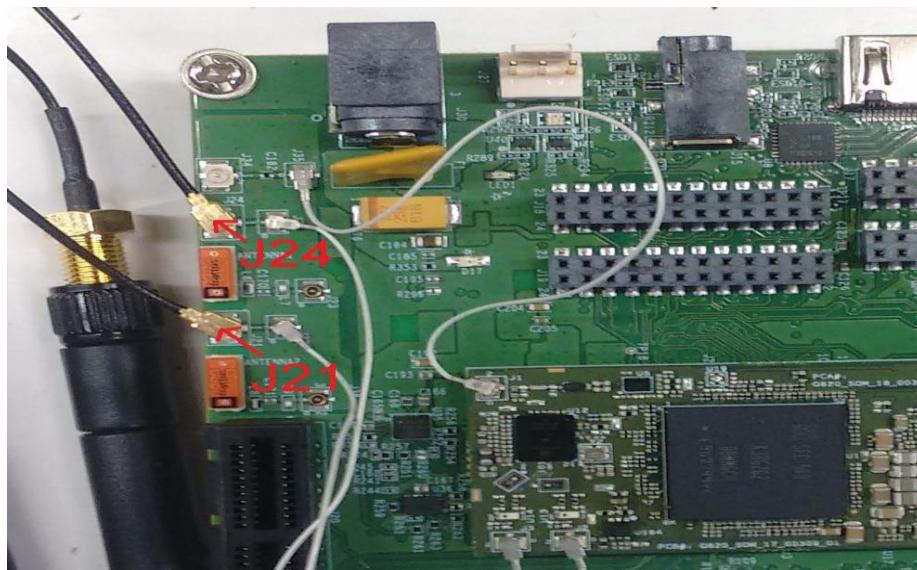


Figure 6: External Wi-Fi Connection

### 5.2.3 MIPI CSI Interface

The ERAGON820 Carrier board provides three 4-Lane MIPI CSI Interface having the following features:

- Three 4-Lanes MIPI CSI with 4+4+4 or 4+4+2+1 Configuration, 2.0 Gbps per Lane.
- 4+4+2+1 can be configured via software support and external bridge board which can be designed by user as per requirements.
- Supports Dual ISP mode and camera up to 28MP.
- Two Dedicated I2C (CCIO & CCI1) channel and BLSP3\_I2C (Low Speed Expansion Header) for Camera Control.

#### 5.2.3.1 MIPI CSIO Interface

The pin specification for CSIO (J10) are described in the table below.

Pin No.	Net Name	Default Pin Function
J10.1	GND	Digital Ground
J10.2	MIPI_CSIO_CLK_P	MIPI Camera Serial Interface 0 Clock lane HIGH
J10.3	MIPI_CSIO_CLK_M	MIPI Camera Serial Interface 0 Clock lane LOW
J10.4	GND	Digital Ground
J10.5	MIPI_CSIO_D2_M	MIPI Camera Serial Interface 0 Data Lane-2 LOW
J10.6	MIPI_CSIO_D2_P	MIPI Camera Serial Interface 0 Data Lane-2 HIGH
J10.7	GND	Digital Ground
J10.8	MIPI_CSIO_D1_P	MIPI Camera Serial Interface 0 Data Lane-1 HIGH
J10.9	MIPI_CSIO_D1_M	MIPI Camera Serial Interface 0 Data Lane-1 LOW
J10.10	GND	Digital Ground
J10.11	MIPI_CSIO_D0_P	MIPI Camera Serial Interface 0 Data Lane-0 HIGH
J10.12	MIPI_CSIO_D0_M	MIPI Camera Serial Interface 0 Data Lane-0 LOW
J10.13	GND	Digital Ground
J10.14	MIPI_CSIO_D3_M	MIPI Camera Serial Interface 0 Data Lane-3 LOW
J10.15	MIPI_CSIO_D3_P	MIPI Camera Serial Interface 0 Data Lane-3 HIGH
J10.16	GND	Digital Ground
J10.17	VCC_5V0	VCC 5V Supply
J10.18	VCC_5V0	VCC 5V Supply
J10.19	VCC_5V0	VCC 5V Supply
J10.20	CSIO_PWDN	MIPI Camera Serial Interface 0 Power Down Signal
J10.21	CAM_MCLK0	Master clock 0 for camera
J10.22	CSIO_RST	MIPI Camera Serial Interface 0 RESET Signal
J10.23	GND	Digital Ground
J10.24	CSI_I2C0_SDA	Camera I2C0 Data Line
J10.25	CSI_I2C0_SCL	Camera I2C0 Clock Line
J10.26	GND	Digital Ground
J10.27	CAM_MCLK3	Master clock3 for camera
J10.28	CSIO_CAM_GPIO_1	GPIO for CSIO Camera
J10.29	CSIO_CAM_GPIO_2	GPIO for CSIO Camera

J10.30	GND	Digital Ground
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Table 8: MIPI CSI0 Pinouts

### 5.2.3.2 MIPI CSI1 Interface

The pin specifications for CSI1 (J11) are described in the table below.

Pin No.	Net Name	Default Pin Function
J11.1	GND	Digital Ground
J11.2	MIPI_CSI1_CLK_P	MIPI Camera Serial Interface 1 Clock HIGH
J11.3	MIPI_CSI1_CLK_M	MIPI Camera Serial Interface 1 Clock LOW
J11.4	GND	Digital Ground
J11.5	MIPI_CSI1_D2_M	MIPI Camera Serial Interface 1 Data Lane-2 LOW
J11.6	MIPI_CSI1_D2_P	MIPI Camera Serial Interface 1 Data Lane-2 HIGH
J11.7	GND	Digital Ground
J11.8	MIPI_CSI1_D1_P	MIPI Camera Serial Interface 1 Data Lane-1 HIGH
J11.9	MIPI_CSI1_D1_M	MIPI Camera Serial Interface 1 Data Lane-1 LOW
J11.10	GND	Digital Ground
J11.11	MIPI_CSI1_D0_P	MIPI Camera Serial Interface 1 Data Lane-0 HIGH
J11.12	MIPI_CSI1_D0_M	MIPI Camera Serial Interface 1 Data Lane-0 LOW
J11.13	GND	Digital Ground
J11.14	MIPI_CSI1_D3_M	MIPI Camera Serial Interface 1 Data Lane-3 LOW
J11.15	MIPI_CSI1_D3_P	MIPI Camera Serial Interface 1 Data Lane-3 HIGH
J11.16	GND	Digital Ground
J11.17	VCC_5V0	VCC 5V Supply
J11.18	VCC_5V0	VCC 5V Supply
J11.19	VCC_5V0	VCC 5V Supply
J11.20	CSI1_PWDN	MIPI Camera Serial Interface Power Down Signal
J11.21	CAM_MCLK1	Master clock 1 for camera
J11.22	CSI1_RST	MIPI Camera Serial Interface 0 RESET Signal
J11.23	GND	Digital Ground
J11.24	CSI1_I2C_SDA	Camera I2C Data Line
J11.25	CSI1_I2C_SCL	Camera I2C Clock Line
J11.26	GND	Digital Ground
J11.27	CAM_MCLK3	Master Clock3 for camera
J11.28	CSI1_CAM_GPIO_1	GPIO for CSI1 Camera
J11.29	CSI1_CAM_GPIO_2	GPIO for CSI1 Camera
J11.30	GND	Digital Ground

Table 9: MIPI CSI1 Pinouts

### 5.2.3.3 MIPI CSI2 Interface

The pin specification for CSI2 (J12) are described in the table below:

Pin No.	Net Name	Default Pin Function
J12.1	GND	Digital Ground
J12.2	MIPI_CSI2_CLK_P	MIPI Camera Serial Interface 2 Clock HIGH
J12.3	MIPI_CSI2_CLK_M	MIPI Camera Serial Interface 2 Clock LOW
J12.4	GND	Digital Ground
J12.5	MIPI_CSI2_D2_M	MIPI Camera Serial Interface 2 Data Lane-2 LOW
J12.6	MIPI_CSI2_D2_P	MIPI Camera Serial Interface 2 Data Lane-2 HIGH
J12.7	GND	Digital Ground
J12.8	MIPI_CSI2_D1_P	MIPI Camera Serial Interface 2 Data Lane-1 HIGH
J12.9	MIPI_CSI2_D1_M	MIPI Camera Serial Interface 2 Data Lane-1 LOW
J12.10	GND	Digital Ground
J12.11	MIPI_CSI2_D0_P	MIPI Camera Serial Interface 2 Data Lane-0 HIGH
J12.12	MIPI_CSI2_D0_M	MIPI Camera Serial Interface 2 Data Lane-0 LOW
J12.13	GND	Digital Ground
J12.14	MIPI_CSI2_D3_M	MIPI Camera Serial Interface 2 Data Lane-3 LOW
J12.15	MIPI_CSI2_D3_P	MIPI Camera Serial Interface 2 Data Lane-3 HIGH
J12.16	GND	Digital Ground
J12.17	VCC_5V0	VCC 5V Supply
J12.18	VCC_5V0	VCC 5V Supply
J12.19	VCC_5V0	VCC 5V Supply
J12.20	CSI2_PWDN	MIPI Camera Serial Interface Power Down Signal
J12.21	CAM_MCLK2	Master clock 1 for camera
J12.22	CSI2_RST	MIPI Camera Serial Interface 0 RESET Signal
J12.23	GND	Digital Ground
J12.24	CSI_I2C1_SDA	Camera I2C Data Line
J12.25	CSI_I2C1_SCL	Camera I2C Clock Line
J12.26	GND	Digital Ground
J12.27	CAM_MCLK3	Master Clock3 for Camera
J12.28	CSI2_CAM_GPIO_1	GPIO for CSI2 Camera
J12.29	CSI2_CAM_GPIO_2	GPIO for CSI2 Camera
J12.30	GND	Digital Ground

Table 10: MIPI CSI2 Pinouts

## 5.2.4 MIPI DSI Interface

The ERAGON820 Carrier board provides two 4-Lanes MIPI DSI Interface for display up to 3840 X 2400 resolution at 60 fps.

### 5.2.4.1 MIPI DSIO Interface

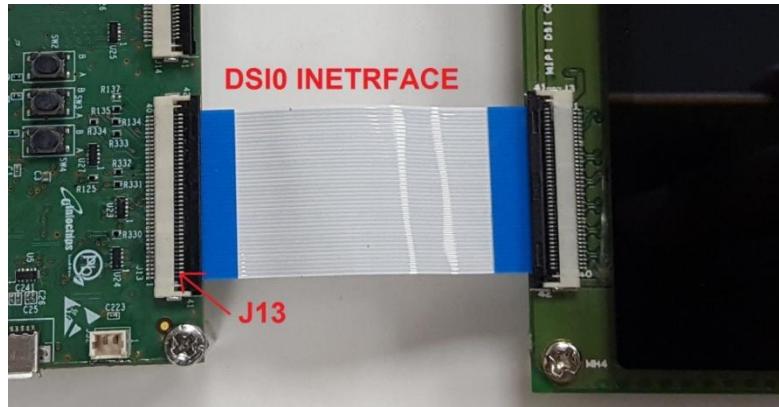


Figure 7: MIPI DSIO Connector

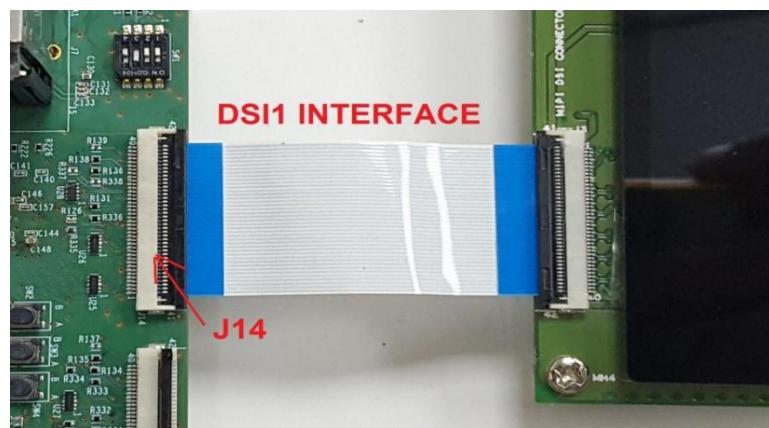
The pin specifications for DSIO (J13) are described in the table below:

Pin No.	Net Name	Default Pin Function
J13.1	GND	Digital Ground
J13.2	WLED_VREG	LED anode for Backlight control
J13.3	MIPI_DSIO_CLK_P	MIPI Display Serial Interface 0 Clock HIGH
J13.4	VREG_DISP	Voltage Supply for Display LOW
J13.5	MIPI_DSIO_CLK_M	MIPI Display Serial Interface 0 Clock LOW
J13.6	VREG_DISP	Voltage Supply for Display HIGH
J13.7	GND	Digital Ground
J13.8	VCC_5V0	VCC Supply Voltage
J13.9	MIPI_DSIO_D0_P	MIPI Display Serial Interface 0 Data Lane-0 HIGH
J13.10	VCC_5V0	VCC Supply Voltage
J13.11	MIPI_DSIO_D0_M	MIPI Display Serial Interface 0 Data Lane-0 LOW
J13.12	GND	Digital Ground
J13.13	GND	Digital Ground
J13.14	NC	Not Connected
J13.15	MIPI_DSIO_D1_P	MIPI Display Serial Interface 0 Data Lane-1 HIGH
J13.16	DSIO_RST_N	MIPI Display Serial Interface 0 Reset ( Active Low)
J13.17	MIPI_DSIO_D1_M	MIPI Display Serial Interface 0 Data Lane-1 LOW
J13.18	NC	Not Connected
J13.19	GND	Digital Ground
J13.20	DSI_BACKLIGHT_PWM	MIPI Display Serial Interface 0 Backlight Control
J13.21	MIPI_DSIO_D2_P	MIPI Display Serial Interface 0 Data Lane-2 HIGH

J13.22	GND	Digital Ground
J13.23	MIPI_DSI0_D2_M	MIPI Display Serial Interface 0 data Lane-2 LOW
J13.24	BL1_EN	MIPI Display Serial Interface 0 Backlight Enable
J13.25	GND	Digital Ground
J13.26	WLED_SINK1	MIPI Display Serial Interface 0 Analog Signal
J13.27	MIPI_DSI0_D3_P	MIPI Display Serial Interface 0 Data Lane-3 HIGH
J13.28	WLED_SINK2	MIPI Display Serial Interface 0 Analog Signal
J13.29	MIPI_DSI0_D3_M	MIPI Display Serial Interface 0 Data Lane-3 HIGH
J13.30	BACKLIGHT_CNTL	MIPI Display Serial Interface 0 Backlight Control
J13.31	GND	Digital Ground
J13.32	GND	Digital Ground
J13.33	DSI0_I2C2_CLK	MIPI Display Serial Interface 0 I2C clock lane
J13.34	DSI_TOUCH_INT	MIPI Display Serial Interface 0 Touch Interrupt
J13.35	DSI0_I2C2_DATA	MIPI Display Serial Interface 0 I2C Data lane
J13.36	TOUCH_RST	MIPI Display Serial Interface 0 Touch Reset
J13.37	GND	Digital Ground
J13.38	TOUCH_GPIO	MIPI Display Serial Interface 0 Touch GPIO
J13.39	GND	Digital Ground
J13.40	NC	Not Connected

**Table 11: MIPI DSIO Pinouts**

#### 5.2.4.2 MIPI DSI1 Interface


**Figure 8: MIPI DSI1**

The pin specifications for DSI1 (J14) are described in the table below:

Pin No.	Net Name	Default Pin Function
J14.1	GND	Digital Ground
J14.2	WLED_VREG	LED anode for Backlight control
J14.3	MIPI_DSI1_CLK_P	MIPI Display Serial Interface 1 Clock HIGH
J14.4	VREG_DISN	Voltage Supply for Display LOW
J14.5	MIPI_DSI1_CLK_M	MIPI Display Serial Interface 1 Clock LOW
J14.6	VREG_DISP	Voltage Supply for Display HIGH
J14.7	GND	Digital Ground
J14.8	VCC_5V0	VCC Supply Voltage
J14.9	MIPI_DSI1_D0_P	MIPI Display Serial Interface 1 Data Lane-0 HIGH
J14.10	VCC_5V0	VCC Supply Voltage
J14.11	MIPI_DSI1_D0_M	MIPI Display Serial Interface 1 Data Lane-0 LOW
J14.12	GND	Digital Ground
J14.13	GND	Digital Ground
J14.14	NC	Not Connected
J14.15	MIPI_DSI1_D1_P	MIPI Display Serial Interface 1 Data Lane-1 HIGH
J14.16	DSI0_RST_N	MIPI Display Serial Interface 1 Reset ( Active Low)
J14.17	MIPI_DSI1_D1_M	MIPI Display Serial Interface 1 Data Lane-1 LOW
J14.18	NC	Not Connected
J14.19	GND	Digital Ground
J14.20	DSI_BACKLIGHT_PWM	MIPI Display Serial Interface 1 Backlight Control
J14.21	MIPI_DSI1_D2_P	MIPI Display Serial Interface 1 Data Lane-2 HIGH
J14.22	GND	Digital Ground
J14.23	MIPI_DSI1_D2_M	MIPI Display Serial Interface 1 Data Lane-2 LOW
J14.24	BL1_EN	MIPI Display Serial Interface 1 Backlight Enable
J14.25	GND	Digital Ground
J14.26	WLED_SINK1	MIPI Display Serial Interface 1 Analog Signal
J14.27	MIPI_DSI1_D3_P	MIPI Display Serial Interface 1 Data Lane-3 HIGH
J14.28	WLED_SINK2	MIPI Display Serial Interface 1 Analog Signal
J14.29	MIPI_DSI1_D3_M	MIPI Display Serial Interface 1 Data Lane-3 HIGH
J14.30	BACKLIGHT_CNTL	MIPI Display Serial Interface 1 Backlight Control
J14.31	GND	Digital Ground
J14.32	GND	Digital Ground
J14.33	DSI1_I2C2_CLK	MIPI Display Serial Interface 1 I2C clock lane
J14.34	DSI_TOUCH_INT	MIPI Display Serial Interface 1 Touch Interrupt
J14.35	DSI1_I2C2_DATA	MIPI Display Serial Interface 1 I2C Data lane
J14.36	TOUCH_RST	MIPI Display Serial Interface 1 Touch Reset
J14.37	GND	Digital Ground
J14.38	TOUCH_GPIO	MIPI Display Serial Interface 1 Touch GPIO
J14.39	GND	Digital Ground
J14.40	NC	Not Connected

**Table 12: MIPI DSI1 Pinouts**

### 5.2.5 HDMI Interface

The ERAGON820 Carrier board provide HDMI output using standard type A connector for display purpose. It can support up to 4K resolution with standard pinouts.



**Figure 9: HDMI Connector**

Pinouts for HDMI Interface are described in the table below:

Pin No.	Net Name	Default Pin Function
J8.1	HDMI_TX2_P_CON	HDMI Transmit-2 HIGH
J8.2	D2_SHIELD	Shield Ground
J8.3	HDMI_TX2_M_CON	HDMI Transmit-2 LOW
J8.4	HDMI_TX1_P_CON	HDMI Transmit-1 HIGH
J8.5	D1_SHIELD	Shield Ground
J8.6	HDMI_TX1_M_CON	HDMI Transmit-1 LOW
J8.7	HDMI_TX0_P_CON	HDMI Transmit-0 HIGH
J8.8	D0_SHIELD	Shield Ground
J8.9	HDMI_TX0_M_CON	HDMI Transmit-0 LOW
J8.10	HDMI_CLK_P_CON	HDMI Clock HIGH
J8.11	CK_SHIELD	Shield Ground
J8.12	HDMI_CLK_M_CON	HDMI Clock LOW
J8.13	HDMI_CEC_CONN	HDMI CEC(Consumer Electronic Control) Signal
J8.14	HEC	HDMI Ethernet Channel
J8.15	HDMI_DDC_CLK_CONN	HDMI DDC Clock Lane
J8.16	HDMI_DDC_DATA_CONN	HDMI DDC Data Lane
J8.17	GND	Digital ground
J8.18	HDMI_5V	5V supply for HDMI
J8.19	HDMI_HPD_CONN	HDMI Hot Plug Detect Pin

**Table 13: HDMI Pinouts**

### 5.2.6 Digital Audio I2S Interface

The ERAGON820 Carrier boards provide two digital I2S ports (MI2S3 and HDMI\_MI2S4) on the Connector (J18). Both the I2S ports are provided on the Expansion Connector & out of them one (HDMI\_MI2S4) is also used for HDMI Audio signals.

Pinouts for I2S Interface are described in the table below.

Pin No.	Net Name	Default Pin Function
J18.15	MI2S_3_D0	MI2S 3 Data Signal Lane 0
J18.14	MI2S_3_D1	MI2S 3 Data Signal Lane 1
J18.10	MI2S_3_MCLK	MI2S 3 Master Clock Signal
J18.12	MI2S_3_WS	MI2S 3 Word Select Signal
J18.13	MI2S_3_SCK	MI2S 3 Serial Clock Signal
J18.19	HDMI_MI2S_4_D3	MI2S 4 Data Signal Lane 3
J18.20	HDMI_MI2S_4_D2	MI2S 4 Data Signal Lane 2
J18.21	HDMI_MI2S_4_D1	MI2S 4 Data Signal Lane 1
J18.22	HDMI_MI2S_4_D0	MI2S 4 Data Signal Lane 0
J18.18	USB_BOOT/ HDMI_MI2S_4_MCLK	MI2S 4 Master Clock Signal/ Forced USB Boot Pin
J18.17	HDMI_MI2S_4_WS	MI2S 4 Word Select Signal
J18.16	HDMI_MI2S_4_SCK	MI2S 4 Serial Clock signal

**Table 14: I2S Pinouts**

### 5.2.7 PCM Interface

APQ8096 supports four PCM Ports, out of them one PCM (PCM1) port is used for interfacing with Wi-Fi+BT (QCA6174) Interface. Other PCM port (PCM2) is provided on carrier board as a low speed expansion connector.

Pinouts of PCM2 interface are described in the table below.

Pin No.	Net Name	Default Pin Function
J19.17	PCM2_CLK	PCM Interface 2 Clock signal
J19.19	PCM2_DIN	PCM Interface 2 Data In signal
J19.20	PCM2_DOUT	PCM Interface 2 Data Out signal
J19.18	PCM2_SYNC	PCM Interface 2 Sync signal

**Table 15: PCM Interface Pinouts**

## 5.2.8 USB Interface

The ERAGON820 carrier board supports two USB ports: one is USB 2.0 high speed (USB2) and other one is USB 3.0 super speed (USB1). The USB 3.0 super speed is backward compatible with USB 2.0 high speed.

### 5.2.8.1 USB 2.0 High Speed

This USB port connect to the USB hub. This leads to two USB 2.0 host ports on J7.

Pinouts for USB 2.0 interface are described in the image below:

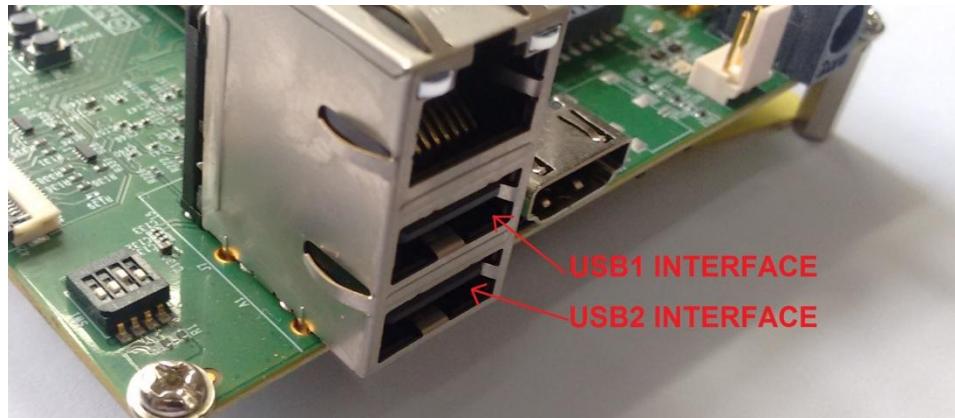


Figure 10: USB Interface

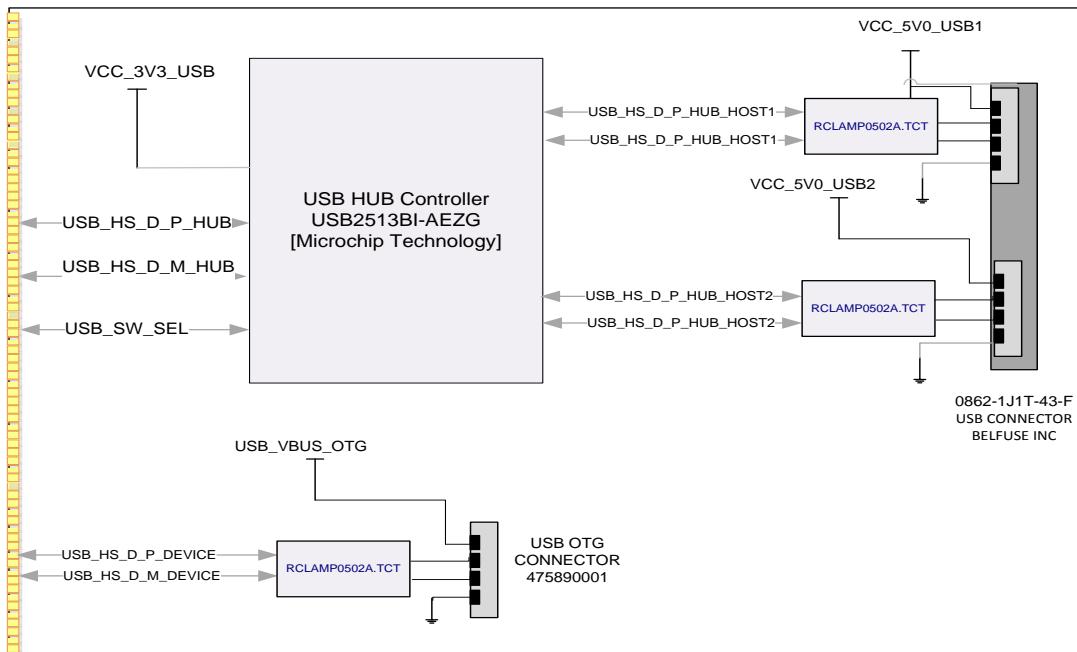


Figure 11: USB 2.0 Interface Pinouts

### 5.2.8.2 USB 3.0 OTG Interface

ERAGON820 Carrier board contains one USB 3.0 port which can be implemented as OTG or in Device Mode. This port is referred to as J6.

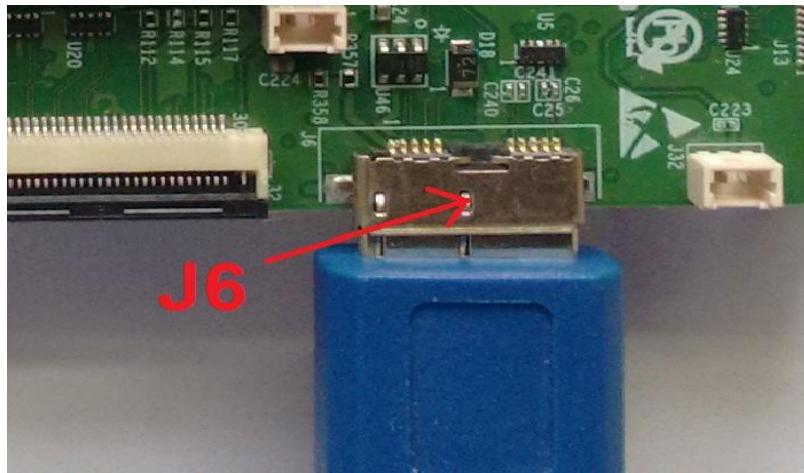


Figure 12: USB 3.0

Pin descriptions for USB 3.0 connector are as mentioned below:

Pin No.	Net Name	Default Pin Function
J6.3	USB1_HS_DP	High Speed USB Interface 1 Data lane HIGH
J6.2	USB1_HS_DM	High Speed USB Interface 1 Data lane LOW
J6.7	USB1_SS_TP	Super Speed USB Interface 1 Transmit HIGH
J6.6	USB1_SS_TM	Super Speed USB Interface 1 Transmit LOW
J6.10	USB1_SS_RP	Super Speed USB Interface 1 Receive HIGH
J6.9	USB1_SS_RM	Super Speed USB Interface 1 Receive LOW
J6.1	USB_VBUS	USB_VBUS Detect Signal
J6.4	USB_SS_ID	USB Interface ID Pin

Table 16: USB 3.0 Interface Pinouts

### 5.2.9 JTAG Interface

The ERAGON820 Carrier board has one 20 pin JTAG connector for programming and debugging purpose.

The signal descriptions are as follows.

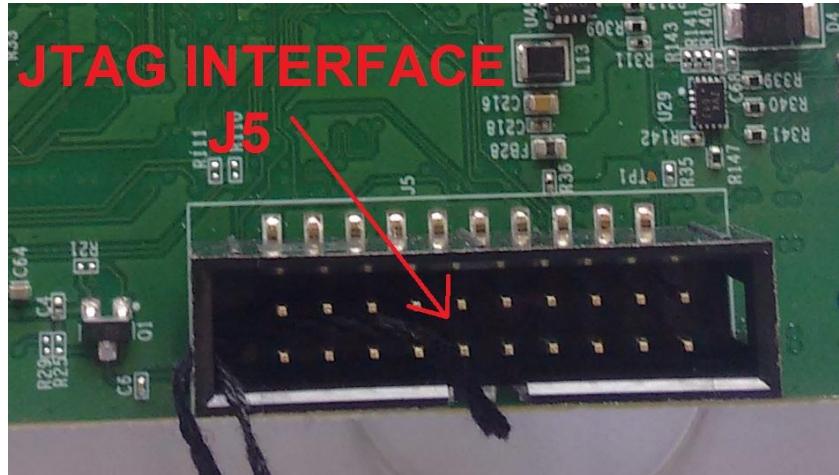


Figure 13: JTAG CONNECTOR

Pin No.	Net Name	Default Pin Function
J5.13	JTAG_TDO	JTAG Data Output
J5.7	JTAG_TMS	JTAG Mode-Select Input
J5.5	JTAG_TDI	JTAG Data Input
J5.9	JTAG_TCK	JTAG Clock Input
J5.15	JTAG_SRST_N	JTAG Reset for debug
J5.3	JTAG_TRST_N	JTAG Reset
J5.1	JTAG_PS_HOLD	Power-Supply Hold Control Input

Table 17 : JTAG Interface Pinouts

### 5.2.10 Ethernet Interface

The ERAGON820 Carrier board is compliant with AR8151L-B, the fifth generation Gigabit Ethernet (GbE) Controller solution from Atheros. The AR8151L-B consists of a 10/100/1000BASE-T GbE media access controller (MAC), a triple-speed Ethernet physical layer transceiver (PHY) and a PCI Express bus interface.

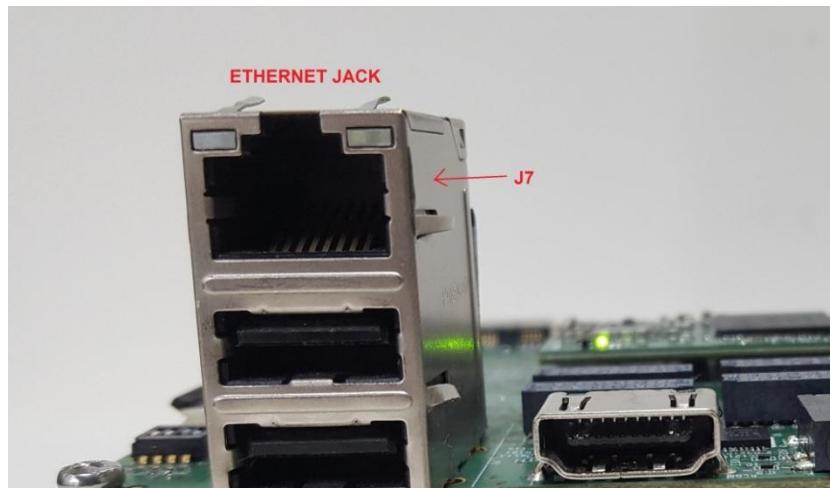
The AR8151L-B is compliant with IEEE 802.3u specification for 10/100 Mbps Ethernet and IEEE 802.3ab specification for 1000 Mbps Ethernet. The AR8151L-B device has functionalities such as pulse shaping, Tx/Rx PCS, echo canceller, NEXT canceller, equalizer, decoder, and timing recovery functions to deliver robust signal performance in noisy environments.

### 5.2.10.1 PHY Interface

The Ethernet PHY is a component that operates at the physical layer of the OSI network model. It implements the Ethernet physical layer portion of the 1000BASE-T, 100BASE-TX, and 10BASE-T standards. More specifically, the Ethernet PHY is a chip that implements the hardware send and receive function of Ethernet frames.

- Integrated PHY for 10/100/1000 Mbps
- IEEE 802.3 Auto-Negotiation Support
- IEEE 802.3ab PHY compliance and compatibility
- Supports automatic MDI/MDIX functionality
- IEEE 802.3az support

The Ethernet jack, part number 0862-1J1T-43-F has integrated magnetics for protection from user interface. It is a stacked structure connector which is also consists of two USB 2.0 high speed connector.



**Figure 14: Ethernet Connector**

The signal descriptions of Ethernet port described in the table below.

Pin No.	Net Name	Default Pin Function
J7B.2	ETH_TRX0_P	Ethernet Transmit-0 HIGH
J7B.3	ETH_TRX0_N	Ethernet Transmit-0 LOW
J7B.4	ETH_TRX1_P	Ethernet Transmit-1 HIGH
J7B.5	ETH_TRX1_N	Ethernet Transmit-1 LOW
J7B.7	ETH_TRX2_P	Ethernet Transmit-2 HIGH
J7B.8	ETH_TRX2_N	Ethernet Transmit-2 LOW
J7B.9	ETH_TRX3_P	Ethernet Transmit-3 HIGH
J7B.10	ETH_TRX3_N	Ethernet Transmit-3 LOW
J7B.11	ETH_LED1_LINK#	Ethernet Link State Signal

J7B.13	ETH_LED0_ACT#	Ethernet Active State Signal
J7B.15	ETH_LED2_1Gbps#	Ethernet Speed State Signal

**Table 18: Ethernet pinouts**

### 5.2.11 HDMI Input Audio Interface

The ERAGON820 Carrier Board contains the 16 pin HDMI Input Audio Connector (Ref J44). A 3-wire (audio out only) I2S channel is routed directly to the HDMI to CSI bridge Board through HDMI Input Audio connector.


**Figure 15: HDMI AUDIO**

Pin description of HDMI audio input connector are described in the table below.

Pin No.	Net Name	Default Pin Function
J7B.2	BLSP8_I2C_SDA	BLSP8 I2C Data Line
J7B.3	BLSP8_I2C_SCL	BLSP8 I2C Clock Line
J7B.4	HDMI_MI2S_4_SCK	HDMI I2S Clock Frequency
J7B.5	HDMI_MI2S_4_WS	HDMI Word Select pin
J7B.7	HDMI_MI2S_4_D3	HDMI I2S Data Signal
J7B.8	HDMI_MI2S_4_D2	HDMI I2S Data Signal
J7B.9	HDMI_MI2S_4_D1	HDMI I2S Data Signal
J7B.10	HDMI_MI2S_4_D0	HDMI I2S Data Signal
J7B.11	HDMI_RST_N	HDMI Reset ( Active Low)
J7B.13	HDMI_INT_GPIO	HDMI Interrupt GPIO

**Table 19: HDMI AUDIO Pinout**

### 5.2.12 GPS Interface

The ERAGON820 Carrier board contains U.FL (J34) connector from which the GPS data directly goes to the WGR7640 receiver via X.FL connector J35 on carrier board.

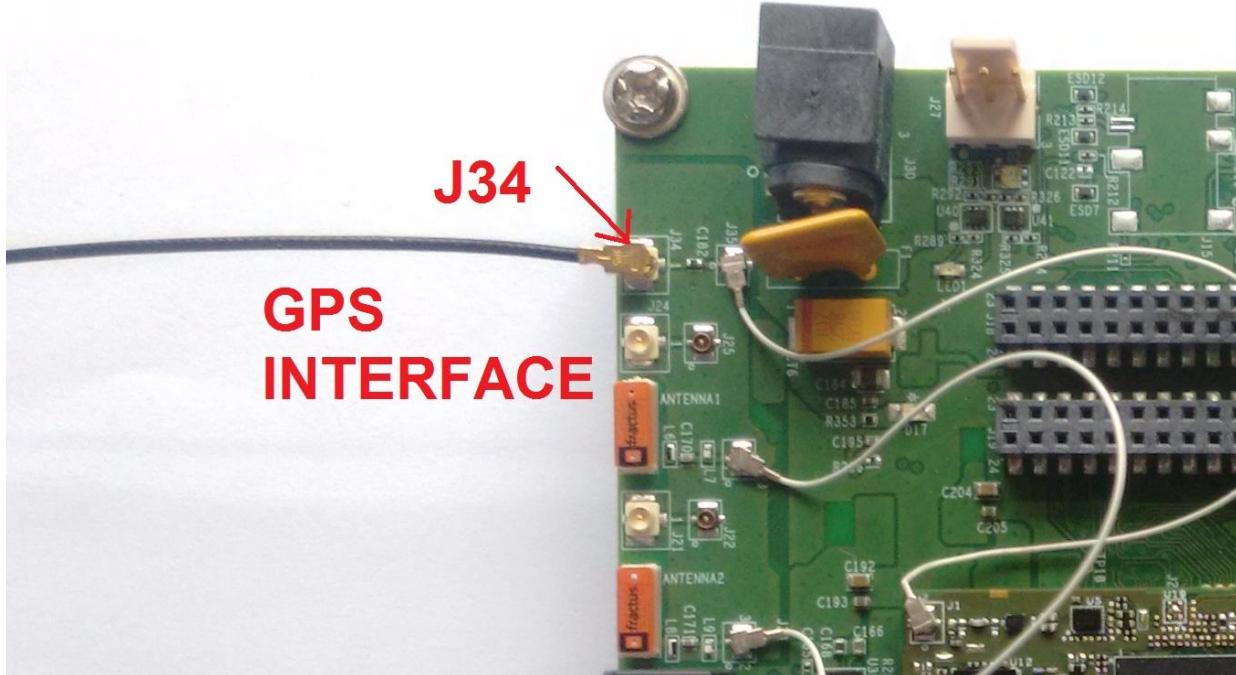


Figure 16: GPS Connection

### 5.2.13 Debug Interface

ERAGON820 has one 3 pin debug console connector using BLSP8\_UART. This is used for a serial console application. The pin descriptions are described as below.



Figure 17: Debug Connector

Pin No.	Net Name	Default Pin Function
J27.1	BLSP8_UART_RX	UART Receiver Pin.
J27.2	BLSP8_UART_TX	UART Transmitter Pin
J27.3	GND	Ground Pin

**Table 20: Debug Pinouts**

### 5.2.14 Boot Configuration

The ERAGON820 Carrier board has 4 pin switches for Boot Configuration. According to the status of the boot configuration pins, the user can boot the board in different modes. User can also use these pins as GPIOs. The different combinations of the pins 5, 7 and 8 of the SW1 switch are used to boot the board in different boot configuration modes as enlisted in table below.

**BOOT CONFIGURATIONS**

BOOT_CONFIG[3:1]	BOOT OPTIONS
0x00	SDC1 => SDC2 => USB3.0
0x01	SDC2
0x02	SDC1
0x03	USB3.0
0x04	UFS
0x05	SDC2 => UFS

Default Boot Config (0x00) is UFS only.

**Figure 18: BOOT Configuration Switch****Figure 19: Normal Boot Mode Configuration**

For initial firmware and software installation purposes, the board need to boot up in the download (QFIL) mode. Please refer to the below image for better understanding.

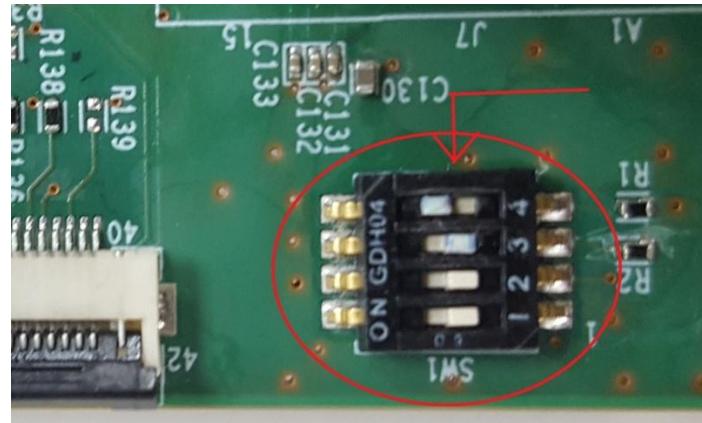


Figure 20: Download (QFIL) Mode Configuration

### 5.2.15 DC Fan Connector

ERAGON820 Carrier Board contains a 2 pin connector for connecting 5 Volt DC fan. This is used for preventing over-heating of the board, if required. The 1<sup>st</sup> pin must be connected to 5V and 2<sup>nd</sup> pin to the ground.



Figure 21: DC FAN Connector

### 5.2.16 External Battery Connector

ERAGON820 has one external battery connector (J31) for connecting external battery provisionally, for testing the functionality of SOM. This feature is for future purposes and the current design does not support this feature.. Pin description is as described in the figure below.



Figure 22: Battery connector

Pin No.	Net Name	Default Pin Function
J31.1	VSENSE_BATT_P	VBATT HIGH Terminal
J31.2	VSENSE_BATT_P	VBATT HIGH Terminal
J31.3	BAT_ID	Battery ID Detect Pin
J31.4	BATT_THERM	Battery Temperature Sense Pin
J31.5	GND	Ground
J31.6	VSENSE_BATT_M	VBATT LOW Terminal

Table 21: Battery connector Pinouts

## 6 Switches

### 6.1 Power Switch

The push-button SW2 serves as the power-on/sleep button. When it is pressed for shorter duration upon applying power to the board, the boot process will start. Once the board is up and running, the user can power-off the board by pressing the power button.

If the board is in Sleep Mode, pressing the power button will activate the board.



Figure 23: Power Switch

### 6.2 Volume High Button

The push-button SW3 serves as the volume high/volume + button. This switch can also be used with the power button (SW2) to boot the board in Fast Boot mode when both are pressed simultaneously.



Figure 24: Volume High Switch

### 6.3 Volume Low Button

The push-button SW4 serves as the volume low/volume - button.



Figure 25: Volume Low Switch

## 7 Connectors

### 7.1 Audio Board to Board Connector

The ERAGON820 Carrier board has two 30 pin on board audio header (J36 and J37) for connecting an external audio board. Audio board contains one audio codec and two speaker amplifier for mic and speaker control.



Figure 26: Audio Board Connector

Pin No.	Signal Name(J36)	Signal Name(J37)
1	VCC_AUDIO	GND
2	VREG_S4A_1P8	GND
3	VCC_AUDIO	MBHC
4	VREG_S4A_1P8	CDC_HPH_L
5	VCC_AUDIO	CDC_MIC_BIAS3
6	VREG_S4A_1P8	CDC_HPH_REF
7	TX_GTR_THRES	CDC_MIC_BIAS1
8	VREG_S4A_1P8	CDC_HPH_R
9	SPKR_AMP_EN2	CODEC_RST_N
10	CDC_DMIC_CLK2	CDC_EAR_M
11	GND	CDC_MIC_BIAS4
12	CDC_DMIC_DATA2	CDC_EAR_P
13	CDC_SPEAKER2_OUT_M	CDC_MIC_BIAS2
14	CDC_DMIC_CLK0	CDC_LINE_OUT1_M
15	CDC_SPEAKER2_OUT_P	CDC_IN5_M
16	CDC_DMIC_DATA0	CDC_LINE_OUT1_P
17	GND	CDC_IN5_P

18	CDC_DMIC_DATA1	CDC_LINE_OUT2_P
19	SPKR_AMP_EN1	CDC_IN6_P
20	CDC_DMIC_CLK1	CDC_LINE_OUT2_M
21	GND	CDC_IN6_M
22	AUDIO_SLIMBUS_D1	AUDIO_CODEC_MCLK
23	CDC_SPEAKER1_OUT_M	CDC_IN4_M
24	AUDIO_SLIMBUS_D0	CDC_IN1_P
25	CDC_SPEAKER1_OUT_P	CDC_IN4_P
26	GND	CDC_IN1_M
27	GND	CDC_IN3_M
28	AUDIO_INT1	CDC_IN2_M
29	AUDIO_SLIMBUS_CLK	CDC_IN3_P
30	AUDIO_INT2	CDC_IN2_P

Table 22: Audio Board Connector Pinouts

## 7.2 Audio Headset connector

ERAGON820 Carrier Board has 3.5mm audio jack (J15).

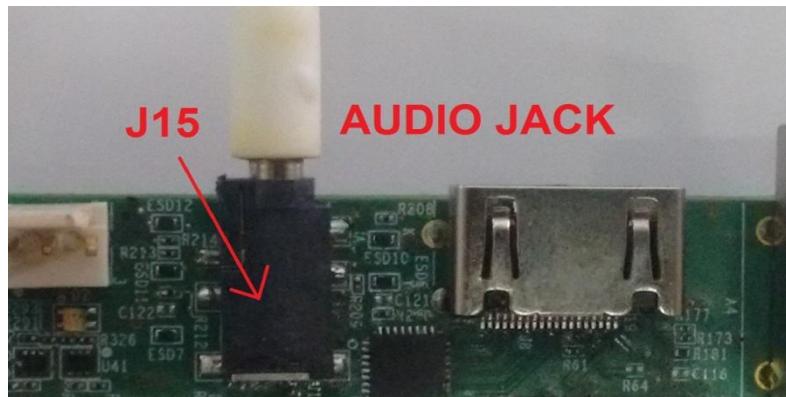


Figure 27: Headset Connector

Pin descriptions for headset connector are described in the table below.

Pin No.	Net Name	Default Pin Function
J15.1	CONN_CDC_MIC2_P	MIC2 Terminal
J15.2	CDC_HPH_REF	Ground for reference
J15.3	CDC_HPH_L	Left Speaker
J15.4	MBHC	Headset Detect Pin
J15.5	CDC_HPH_R	Right Speaker
J15.6	CONN_CDC_MIC4_P	MIC4 Terminal
J15.7	CONN_CDC_MIC3_P	MIC3 Terminal

Table 23: Headset Pinouts

### 7.3 Audio Expansion Connector

ERAGON820 Carrier has given a 16 pin analog expansion connector (J17) on which three analog MIC, two speaker and one earpiece ports are available.



Figure 28: Analog Expansion Connector

Pin No.	Net Name	Default Pin Function
J17.1	CONN_CDC_MIC1_P	For Analog MIC1
J17.2	GND	Ground
J17.3	GND	Ground
J17.4	CONN_CDC_MIC5_P	For Analog MIC5
J17.5	CONN_CDC_MIC6_P	For Analog MIC6
J17.6	GND	Ground
J17.7	GND	Ground
J17.8	GND	Ground
J17.9	CDC_SPEAKER1_OUT_P	Speaker1 Out High
J17.10	CDC_SPEAKER2_OUT_P	Speaker2 Out High
J17.11	CDC_SPEAKER1_OUT_M	Speaker1 Out Low
J17.12	CDC_SPEAKER2_OUT_M	Speaker2 Out Low
J17.13	GND	Ground
J17.14	GND	Ground
J17.15	CDC_EAR_P	Earpiece High Pin
J17.16	CDC_EAR_M	Earpiece Low Pin

Table 24: Analog Expansion Pinouts

## 7.4 Digital Expansion Connector

ERAGON820 Carrier board has a 16 pin Digital Expansion connector (J16) for digital MIC and Speaker line output.



Figure 29: Digital Expansion Connector

Pin No.	Net Name	Default Pin Function
J16.1	CDC_MIC_BIAS3	Bias Voltage for MIC3
J16.2	CDC_MIC_BIAS4	Bias Voltage for MIC4
J16.3	GND	Ground
J16.4	GND	Ground
J16.5	CDC_MIC_BIAS1	Bias Voltage for MIC1
J16.6	CDC_DMIC_CLK1	Digital MIC 1 Clock Line
J16.7	GND	Ground
J16.8	CDC_DMIC_DATA1	Digital MIC1 Data Line
J16.9	CDC_DMIC_CLK0	Digital MIC 0 Clock line
J16.10	CDC_DMIC_CLK2	Digital MIC 2 Clock Line
J16.11	CDC_DMIC_DATA0	Digital MIC 0 Data Line
J16.12	CDC_DMIC_DATA2	Digital MIC 2 Data Line
J16.13	CDC_LINE_OUT2_P	Speaker 2 Out High
J16.14	CDC_LINE_OUT1_P	Speaker 1 Out High
J16.15	CDC_LINE_OUT2_M	Speaker 2 Out Low
J16.16	CDC_LINE_OUT1_M	Speaker 1 Out Low

Table 25: Digital Expansion Pinouts

## 7.5 Low Speed Expansion Connector

ERAGON820 Carrier board has 24 pin low speed expansion connector (J19). The pin descriptions are described in the table below.

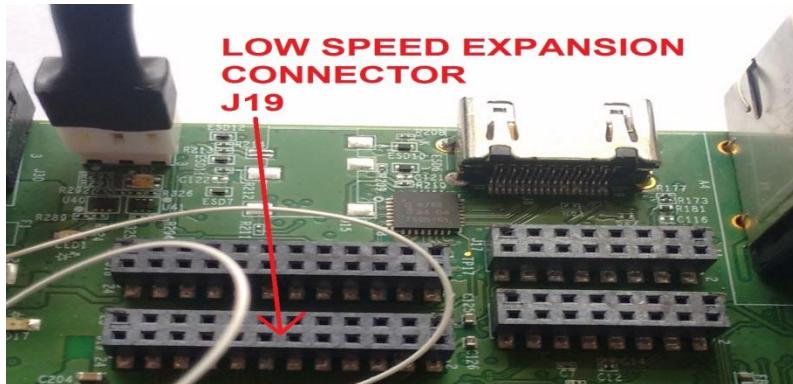


Figure 30: Low Speed Expansion Connector

Pin No.	Net Name	Default Pin Function
J19.1	VCC_1V8	VCC 1.8 Volt Supply
J19.2	VCC_3V3	VCC 3.3 Volt Supply
J19.3	BLSP1_UART_TX	BLSP1 UART Transmit
J19.4	BLSP1_UART_RX	BLSP1 UART Receive
J19.5	BLSP1_UART_RTS_N	BLSP1 UART Ready To Send ( Active Low)
J19.6	BLSP1_UART_CTS_N	BLSP1 UART Clear To Send ( Active Low)
J19.7	BLSP9_SPI_CLK	BLSP9 SPI Clock Line
J19.8	BLSP9_SPI_CS_N	BLSP9 SPI Chip Select ( Active Low)
J19.9	BLSP9_SPI_MISO	BLSP9 SPI Master In Slave Out
J19.10	BLSP9_SPI_MOSI	BLSP9 SPI Master Out Slave In
J19.11	BLSP3_I2C_SCL	BLSP3 I2C Clock Line
J19.12	BLSP3_I2C_SDA	BLSP3 I2C Data Line
J19.13	PM_MPP_GPIO_02	User configurable PMIC GPIO
J19.14	PM_MPP_GPIO_06	User configurable PMIC GPIO
J19.15	PM_MPP_GPIO_04	User configurable PMIC GPIO
J19.16	PM_MPP_GPIO_07	User configurable PMIC GPIO
J19.17	PCM2_CLK	PCM2 Clock Line
J19.18	PCM2_SYNC	PCM2 Synchronization signal
J19.19	PCM2_DIN	PCM2 Data Input Line
J19.20	PCM2_DOUT	PCM2 Data Output Line
J19.21	ALSPG_INT_N	User configurable APQ8096 GPIO
J19.22	SSC_PWR_EN	Sensor Core Power Enable
J19.23	GND	Ground
J19.24	SSC_SYNC_OUT	Sensor Core Synchronization

Table 26: Low Speed Expansion Pinouts

## 7.6 Sensor Core Expansion Connector

ERAGON820 Carrier board has a 24 pin Sensor Core expansion connector (J18) having SSC, MI2S and HDMI\_MI2S signals on it. Pin descriptions for sensor core expansion connector are described in the table below.

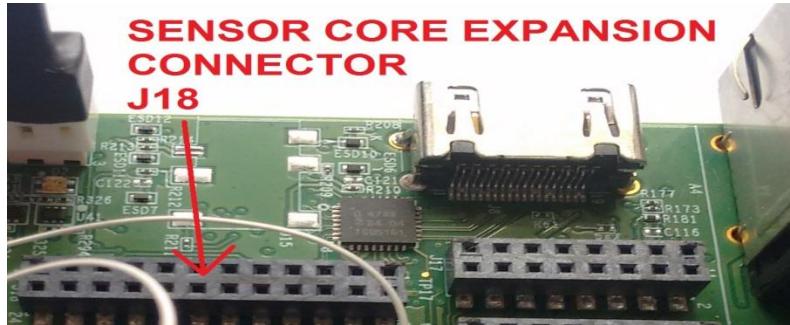


Figure 31: Sensor Core Connector

Pin No.	Net Name	Default Pin Function
J18.1	VCC_1V8	VCC 1.8 Volt Supply
J18.2	VCC_3V3	VCC 3.3 Volt Supply
J18.3	SSC_I2C_2_SDA	SSC I2C 2 DATA Line
J18.4	SSC_SPI_3_CS_N	SSC SPI 3 Chip select (Active Low)
J18.5	SSC_I2C_2_SCL	SSC SPI 2 Serial Clock
J18.6	SSC_SPI_3_MOSI	SSC SPI 3 Master Out Slave In
J18.7	SSC_SPI_3_CLK	SSC SPI 3 Clock
J18.8	SSC_UART_3_RX	SSC UART 3 Receive
J18.9	SSC_SPI_3_MISO	SSC SPI 3 Master In Slave Out
J18.10	MI2S_3_MCLK	MI2S 3 Master Clock Line
J18.11	SSC_UART_3_TX	SSC UART 3 Transmit
J18.12	MI2S_3_WS	MI2S 3 Word Select
J18.13	MI2S_3_SCK	MI2S 3 Serial Clock
J18.14	MI2S_3_D1	MI2S 3 Data Line
J18.15	MI2S_3_D0	MI2S Data Line
J18.16	HDMI_MI2S_4_SCK	HDMI MI2S 4 Serial Clock
J18.17	HDMI_MI2S_4_WS	HDMI MI2S 4 Word Select
J18.18	USB_BOOT/HDMI_MI2S_4_MCLK	HDMI MI2S 4 Master Clock
J18.19	HDMI_MI2S_4_D3	HDMI MI2S 4 Data Line
J18.20	HDMI_MI2S_4_D2	HDMI MI2S 4 Data Line
J18.21	HDMI_MI2S_4_D1	HDMI MI2S 4 Data Line
J18.22	HDMI_MI2S_4_D0	HDMI MI2S 4 Data Line
J18.23	GND	Ground
J18.24	GND	Ground

Table 27: Sensor Core Pinouts

## 7.7 PCIe Slot

ERAGON820 has one 36-pin PCIe slot (J20) to support high speed PCIe Express card.

Pin descriptions of PCIe connector are described in the table below:

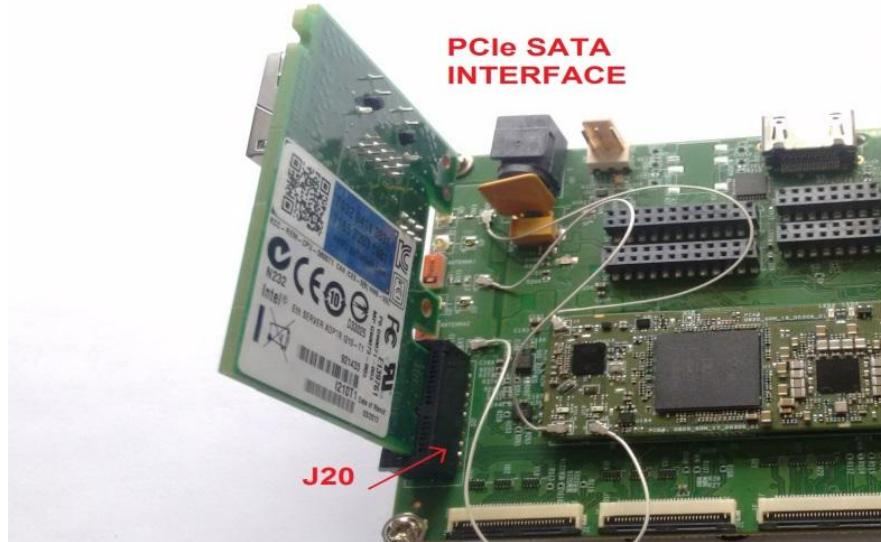


Figure 32: PCIe Card Connector

Pin No.	Net Name	Default Pin Function
A1	GND	Digital Ground
A2	PCIE_12V	12V Supply for PCIe Card
A3	PCIE_12V	12V Supply for PCIe Card
A4	GND	Digital Ground
A5	NC	Not Connected
A6	NC	Not Connected
A7	NC	Not Connected
A8	NC	Not Connected
A9	PCIE_3V3	3.3V supply for PCIe Card
A10	PCIE_3V3	3.3V supply for PCIe Card
A11	PCI1_RST_N_3V3	PCIe Reset Pin (Active Low)
A12	GND	Digital Ground
A13	PCIE1_CLK_P	PCIe1 Differential Clock High
A14	PCIE1_CLK_M	PCIe1 Differential Clock Low
A15	GND	GND
A16	PCIE1_RX_P	PCIe Receive High
A17	PCIE1_RX_M	PCIe Receive Low
A18	GND	GND

B1	PCIE_12V	12V Supply for PCIe Card
B2	PCIE_12V	12V Supply for PCIe Card
B3	PCIE_12V	12V Supply for PCIe Card
B4	GND	GND
B5	BLSP6_I2C_SCL_3V3	BLSP6 I2C Clock Line
B6	BLSP6_I2C_SDA_3V3	BLSP6 I2C Data Line
B7	GND	GND
B8	PCIE_3V3	3.3V supply for PCIe Card
B9	NC	Not Connected
B10	PCIE_3V3	3.3V supply for PCIe Card
B11	PCI1_WAKE_N_3V3	PCIe Wake Signal ( Active Low)
B12	PCI1_CLK_REQ_N_3V3	PCIe Clock Request (Active Low)
B13	GND	GND
B14	PCIE1_TX_P	PCIe Transmit High
B15	PCIE1_TX_M	PCIe Transmit Low
B16	GND	GND
B17	PCIE_SLT_PRSNT_3V3	PCIe Detect Pin
B18	GND	GND

**Figure 33: PCIe Card Slot**

## 8 Power Management

ERAGON820 Carrier Board has dedicated DC Jack for input supply and it has on-board Buck Converters to generate the required Power Supply.

The ERAGON820 carrier board uses four buck convertors, **U42**, **U43**, **U44** and **U45**. **U43** takes the power in to the board and generates **5V at 4A**. This voltage feeds the USB HOST power limit switches and other peripherals. This 5V supply is used by buck convertor (**U44**) to generate the **3.3V at 2A** and **U45** to generate **1.8V at 2A**.

**U42** takes the power in to the board and generates **3.8V at 8A**. This voltage serves as the input Supply to the **PMIC PM8996** mounted on SOM. The **PMIC PM8996** generates different voltages that required for the Processor, Memory and for the other peripherals on Carrier board.

### 8.1 DC Power Input

The ERAGON820 Carrier board requires an Input Supply (Range: 4.5V-18V) from a dedicated DC jack J30. Typical Power Adapter used is of 12V & 3A.

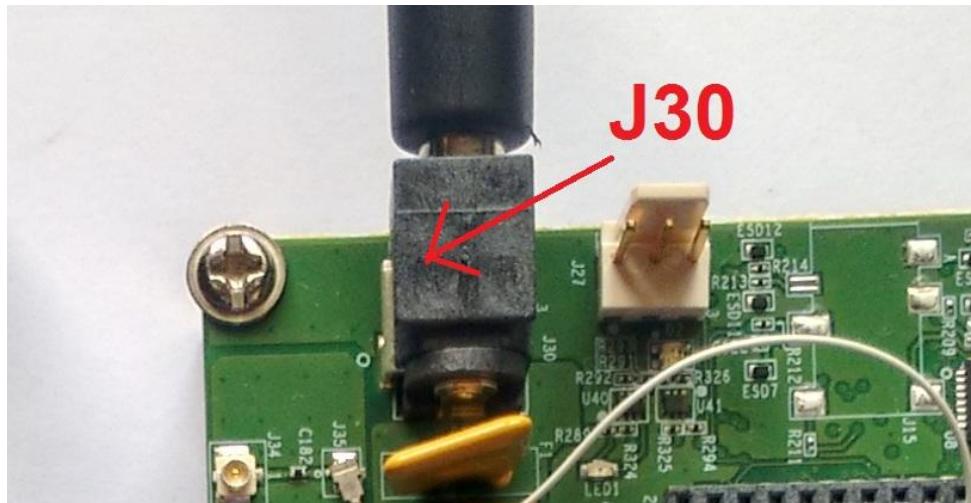


Figure 34: DC Power Jack

### 8.2 Power Sequencing

Upon applying power to the ERAGON820 Carrier board through a DC jack Connector (J30) all buck regulators will be enabled and will start regulating their target voltages. When the output of U42 on the carrier board is on, it will power ON the SOM board PMIC. The 5 Volt output of U43 supplies to U44 and U45 and additionally supplies to the other interface of the device.

## 9 DC ELECTRICAL SPECIFICATIONS

All AC & DC specifications mentioned in this datasheet are valid for the following voltage ranges.

Power Supply	MIN	TYP	MAX	Unit
Main Power Supply, DC VIN	9	12	18	V
Supply for SOM Component (Generated internally on the SOM)	3	3.7	4.5	V

Table 28: Typical Voltage Ranges

Parameter	MIN	MAX	Unit	Group
VIH	1.17	-	V	EMMC, UFS JTAG, digital I/Os
VIL	-	0.63	V	
VOH	1.35	-	V	
VOL	-	0.45	V	

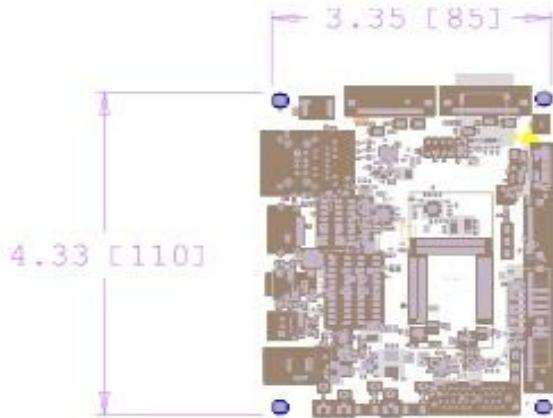
Table 29: Digital I/O characteristics for 1.8V nominal

Parameter	MIN	MAX	Unit	Group
VIH	1.84	3.25	V	SD card Interface
VIL	-0.3	0.73	V	
VOH	2.22	2.95	V	
VOL	0	0.36	V	

Table 30: Digital I/O characteristics for 2.95V nominal

## 10 MECHANICAL SPECIFICATIONS

The Dimension of ERAGON820 Carrier is 85mm x 110mm.



**Figure 35: Carrier Board Dimension**

## 11 Special Care when using ERAGON820 Carrier Board

- The ERAGON820 Carrier board has connectivity to SOM board via three 100 pin board to board connector, so proper care must be taken while connecting the SOM with the Carrier board.
- Before turning ON the board, all the connections must be proper.
- Avoid connecting and disconnecting the SOM board from the carrier board for multiple times.
- Always use ESD protection while handling the Kit.

### 11.1 Development Device Notice

This device contains RF/digital hardware and software intended for engineering development, engineering evaluation, or demonstration purposes only. It is intended for use in a controlled environment. It is highly recommended to avoid selling this device for usage in a residential environment or for usage by the general public as an end user device.

### 11.2 Anti-Static Handling Procedure

This device has exposed PCB and chips. Accordingly, proper anti-static precautions should be employed when handling the kit, this includes:

- Use a grounded anti-static mat
- Use a grounded wrist or foot strap

## 12 Eragon820 Daughter Boards

### 12.1 Camera Interface Board-21MP

This board is add-on accessory to Eragon820. This is designed to interface various types of camera sensors to Eragon820 boards. This board supports camera sensors up to 21MP and connected to CSI interface of Eragon 820 at Primary Camera Connector (J12) on the Board. It uses SONY-IMX230 (21MP) Sensors. This board has five LDOs (U1, U2, U3, U4 & U5) to generate supplies VCC\_2V8, VCC\_2V5, VCC\_3V7, VCC1V8 & VCC1V1.

The camera control and configuration mechanism uses I2C interface. It has mating connector (J2) for Primary Camera Connector (J12) of the ERAGON 820 Board and camera connector (J1).

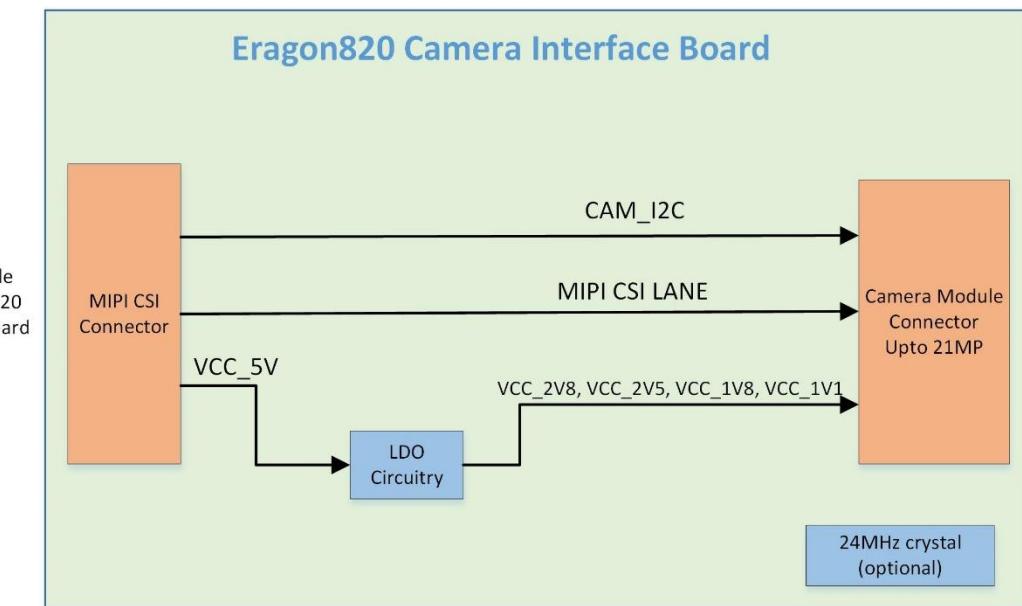


Figure 36 : Camera Interface Board-21MP

The pin description of camera connector J1 is as follows:

Pin No.	Signal Name	Specification
1	DGND	Digital Ground
2	DGND	Digital Ground
3	DGND	Digital Ground
4	RESET	MIPI CSI Reset Pin (active Low)
5	AF_VDD	VCC_2V8
6	NC (AF_EN)	Not connect, used for Auto Focus Enable
7	SDA	CSI I2C Data Line
8	DOVDD	VCC_1V8
9	SCL	CSI I2C Clock Line

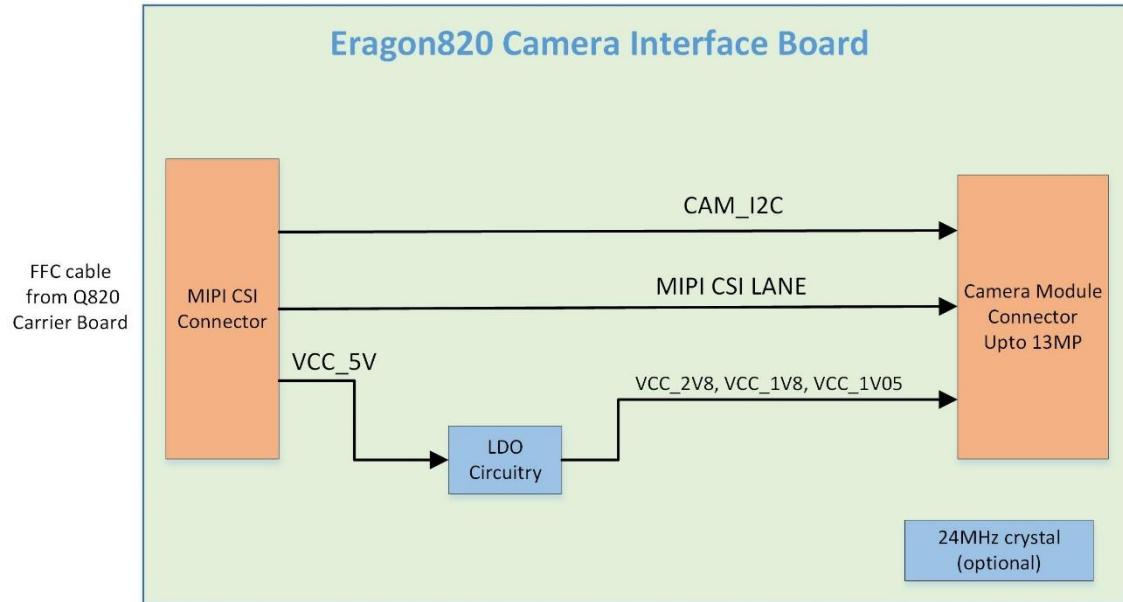
10	DVDD	VCC_1V1
11	DGND	Digital Ground
12	NC (PWDN)	Not Connect, used for Power Down Signal
13	MCN	MIPI CSI Clock Lane Low
14	NC	Not Connect
15	MCP	MIPI CSI Clock Lane High
16	DGND	Digital Ground
17	MDN0	MIPI CSI Data Lane0 Low
18	MCLK	Master Clock
19	MDP0	MIPI CSI Data Lane0 High
20	DGND	Digital Ground
21	MDN1	MIPI CSI Data Lane1 Low
22	NC (FLASH)	Not Connect, used as GPIO signal for Flash
23	MDP1	MIPI CSI Data Lane1 High
24	AVDD	VCC_2V5
25	NC	Not Connect
26	AGND	Analog Ground
27	MDN2	MIPI CSI Data Lane2 Low
28	MDN3	MIPI CSI Data Lane3 Low
29	MDP2	MIPI CSI Data Lane2 High
30	MDP3	MIPI CSI Data Lane3 High

Table 31: 21MP camera connector pin out

## 12.2 Camera Interface Board-13MP

This board is add-on accessory to Eragon820. This is designed to interface various types of camera Sensors to Eragon820 boards. This board supports camera sensors up to 13MP and connected to CSI interface of Eragon 820 at Primary Camera Connector (J11) on the Board. It uses Truly CMA921 (13MP) Sensors. This board has four LDOs (U1, U2, U3 & U4) to generate supplies VCC\_1V8, VCC\_3V7, VCC\_1V05, & VCC2V8.

The camera control and configuration mechanism uses I2C interface. It has mating connector (J1) for Primary Camera Connector (J11) of the ERAGON 820 Board and camera connector (J2).



**Figure 37: Camera Interface Board-13MP**

The pin description of camera connector (J2) is as follows:

Pin No.	Signal Name	Specification
1	AGND	Analog Ground
2	AVDD	VCC_2V8
3	AF_GND	Digital Ground
4	AF_VDD	VCC_2V8
5	DVDD	VCC_1V05
6	DOVDD	VCC_1V8
7	AF_EN	Auto Focus Enable
8	SDA	CSI I2C Data Line
9	SCL	CSI I2C Clock Line
10	PWDN	Power Down Signal
11	MCLK	Master Clock
12	DGND	Digital Ground
13	RESET	MIPI CSI Reset Pin (active Low)
14	CAM_ID	Test Point
15	DGND	Digital Ground
16	MDP2	MIPI CSI Data Lane2 High
17	MDN2	MIPI CSI Data Lane2 Low
18	DGND	Digital Ground
19	MDP3	MIPI CSI Data Lane3 High

20	MDN3	MIPI CSI Data Lane3 Low
21	DGND	Digital Ground
22	MDP1	MIPI CSI Data Lane1 High
23	MDN1	MIPI CSI Data Lane1 Low
24	DGND	Digital Ground
25	MDP0	MIPI CSI Data Lane0 High
26	MDN0	MIPI CSI Data Lane0 Low
27	DGND	Digital Ground
28	MCP	MIPI CSI Clock Lane High
29	MCN	MIPI CSI Clock Lane Low
30	DGND	Digital Ground

Table 32: 13MP Camera Connector Pinout

## 12.3 Camera Interface Board-5MP

This board is add-on accessory to Eragon820. This is designed to interface various types of camera Sensors to Eragon820 boards. This board supports camera sensors up to 5MP and connected to CSI interface of Eragon 820 at Primary Camera Connector (J10) on the Board. It uses Omni Vision OV5645 (5MP) Sensors. This board has four LDOs (U1, U2, U3 & U4) to generate supplies VCC\_1V5, VCC\_2V8, VCC\_1V8, & VCC3V7.

The camera control and configuration mechanism uses I2C interface. It has mating connector (J1) for Primary Camera Connector (J11) of the ERAGON 820 Board and camera connector (J2).

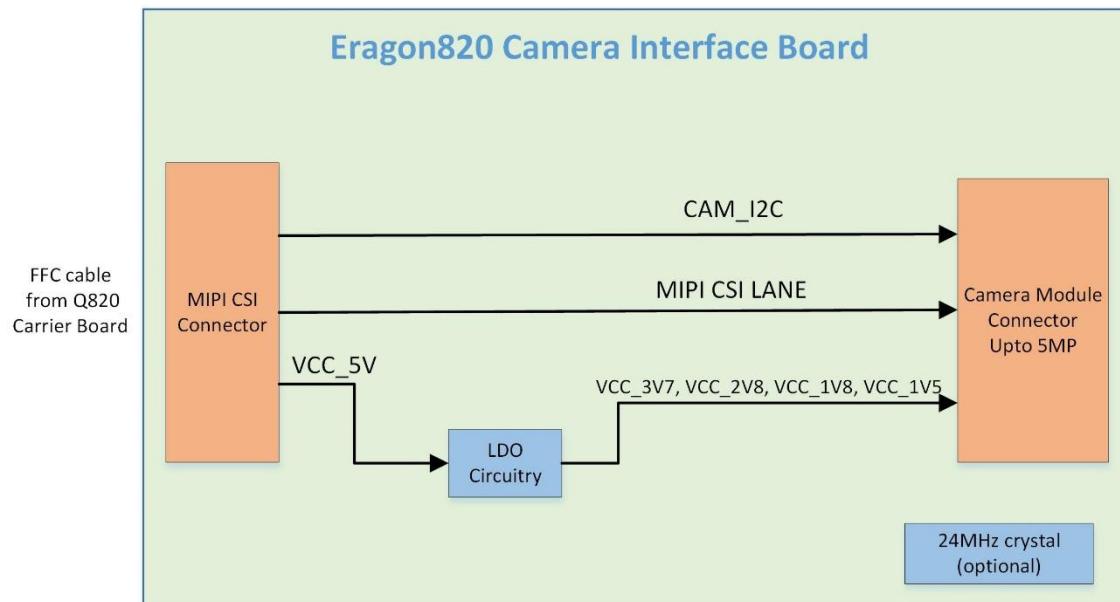


Figure 38: Camera Interface Board-5MP

The pin description of camera connector (J2) is as follows:

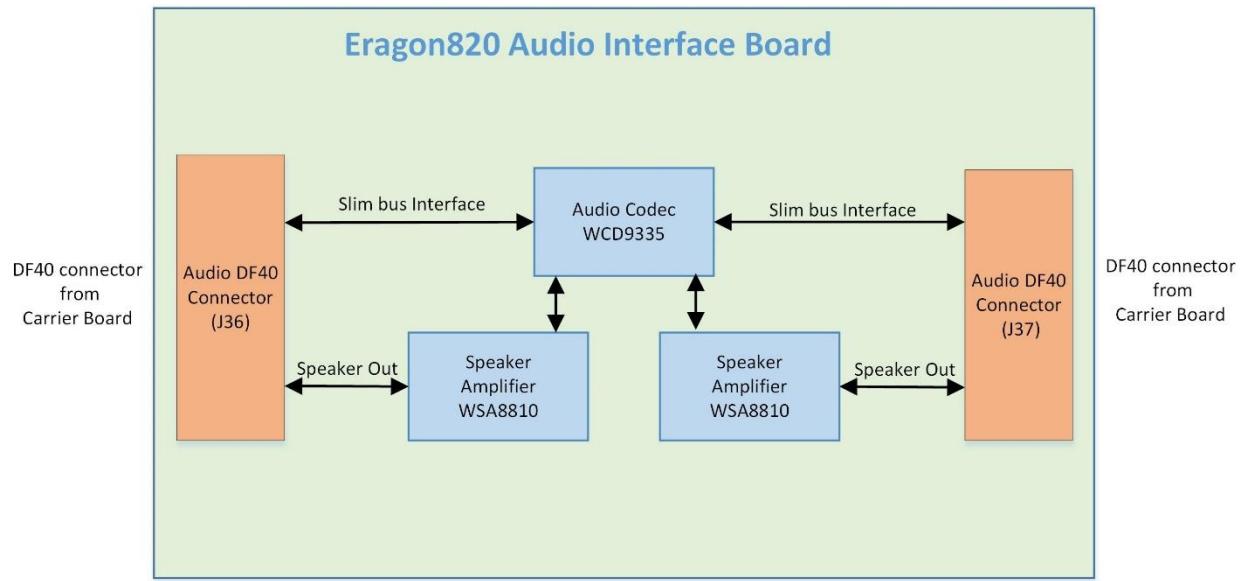
Pin No.	Signal Name	Specification
1	AF_VDD	VCC_2V8
2	AVDD	VCC_2V8
3	SCL	CSI I2C Clock Line
4	SDA	CSI I2C Data Line
5	RESET	MIPI CSI Reset Pin (active Low)
6	PWDN	Power Down Signal
7	DOVDD	VCC_1V8
8	DVDD	VCC_1V5
9	GND	Digital Ground
10	XCLK	CSI Master Clock
11	DGND	Digital Ground
12	DGND	Digital Ground
13	MDN0	MIPI CSI Data Lane0 Low
14	MCP	MIPI CSI Clock Lane High
15	MDP0	MIPI CSI Data Lane0 High
16	MCN	MIPI CSI Clock Lane Low
17	DGND	Digital Ground
18	DGND	Digital Ground
19	DGND	Digital Ground
20	MDP1	MIPI CSI Data Lane1 High
21	DGND	Digital Ground
22	MDN1	MIPI CSI Data Lane1 Low
23	DGND	Digital Ground
24	DGND	Digital Ground

Table 33: Camera Connector Pinout

## 12.4 Audio Interface Board

This board is add-on accessory to Eragon820. This is designed to interface audio codec to Eragon820 boards. This board exhibits one audio codec WCD9335 (U30) and two audio amplifier WSA8810 (U31 & U32) for left and right speaker.

The audio interface board has matting DF40 board to board connector (J36 & J37) with Eragon820 carrier board (J36 & J37).



**Figure 39: Audio Interface Board**

The pin description of audio board connectors J36 & j37 are as follows:

Pin No.	Signal Name	Specification
J36.1	VCC_AUDIO	Power for the LDO and microphone bias circuits
J36.2	VREG_S4A_1P8	1.8V Power Supply
J36.3	VCC_AUDIO	Power for the LDO and microphone bias circuits
J36.4	VREG_S4A_1P8	1.8V Power Supply
J36.5	VCC_AUDIO	Power for the LDO and microphone bias circuits
J36.6	VREG_S4A_1P8	1.8V Power Supply
J36.7	TX_GTR_THRES	Indicates GSM RF power amplifier is about to burst
J36.8	VREG_S4A_1P8	1.8V Power Supply
J36.9	SPKR_AMP_EN2	WSA shutdown control for Speaker Amplifier 2
J36.10	CDC_DMIC_CLK2	Clock for digital microphones 5 and 6
J36.11	DGND	Digital Ground
J36.12	CDC_DMIC_DATA2	Data for digital microphones 5 and 6
J36.13	CDC_SPEAKER2_OUT_M	Speaker amplifier 2 output-Low
J36.14	CDC_DMIC_CLK0	Clock for digital microphones 1 and 2
J36.15	CDC_SPEAKER2_OUT_P	Speaker amplifier 2 output-High
J36.16	CDC_DMIC_DATA0	Data for digital microphones 1 and 2
J36.17	DGND	Digital Ground
J36.18	CDC_DMIC_DATA1	Data for digital microphones 3 and 4

J36.19	SPKR_AMP_EN1	WSA shutdown control for Speaker Amplifier 1
J36.20	CDC_DMIC_CLK1	Clock for digital microphones 3 and 4
J36.21	DGND	Digital Ground
J36.22	AUDIO_SLIMBUS_D1	Bidirectional (Rx/Tx) SLIMbus data bit 2
J36.23	CDC_SPEAKER1_OUT_M	Speaker amplifier 1 output-Low
J36.24	AUDIO_SLIMBUS_D0	Bidirectional (Rx/Tx) SLIMbus data bit 1
J36.25	CDC_SPEAKER1_OUT_P	Speaker amplifier 1 output-High
J36.26	DGND	Digital Ground
J36.27	DGND	Digital Ground
J36.28	AUDIO_INT1	Audio Interrupt Output 1
J36.29	AUDIO_SLIMBUS_CLK	Bidirectional (Rx/Tx) SLIMbus clock
J36.30	AUDIO_INT2	Audio Interrupt Output 1
J37.1	DGND	Digital Ground
J37.2	DGND	Digital Ground
J37.3	MBHC	Mechanical tip-detection pin
J37.4	CDC_HPH_REF	Headphone ground reference
J37.5	CDC_MIC_BIAS3	Microphone bias output voltage 3
J37.6	CDC_HPH_REF	headphone PA's ground reference
J37.7	CDC_MIC_BIAS1	Microphone bias output voltage 1
J37.8	CDC_HPH_R	Headphone right output
J37.9	CODEC_RST_N	WCD9335 Reset Signal (active LOW)
J37.10	CDC_EAR_M	Earpiece amplifier output, differential-LOW
J37.11	CDC_MIC_BIAS4	Microphone bias output voltage 4
J37.12	CDC_EAR_P	Earpiece amplifier output, differential-LOW
J37.13	CDC_MIC_BIAS2	Microphone bias output voltage 2
J37.14	CDC_LINE_OUT1_M	Audio line output 1, differential-LOW
J37.15	CDC_IN5_M	Analog microphone 5 input, differential -LOW
J37.16	CDC_LINE_OUT1_P	Audio line output 1, differential -HIGH
J37.17	CDC_IN5_P	Analog microphone 5 input, differential -HIGH
J37.18	CDC_LINE_OUT2_P	Audio line output 2, differential -HIGH
J37.19	CDC_IN6_P	Analog microphone 6 input, differential -HIGH
J37.20	CDC_LINE_OUT2_M	Audio line output 2, differential -LOW
J37.21	CDC_IN6_M	Analog microphone 6 input, differential -LOW
J37.22	AUDIO_CODEC_MCLK	Master Clock for Audio Codec
J37.23	CDC_IN4_M	Analog microphone 4 input, differential -LOW
J37.24	CDC_IN1_P	Analog microphone 1 input, differential -HIGH
J37.25	CDC_IN4_P	Analog microphone 4 input, differential -HIGH

J37.26	CDC_IN1_M	Analog microphone 1 input, differential -LOW
J37.27	CDC_IN3_M	Analog microphone 3 input, differential -LOW
J37.28	CDC_IN2_M	Analog microphone 2 input, differential -LOW
J37.29	CDC_IN3_P	Analog microphone 3 input, differential -HIGH
J37.30	CDC_IN2_P	Analog microphone 2 input, differential -HIGH

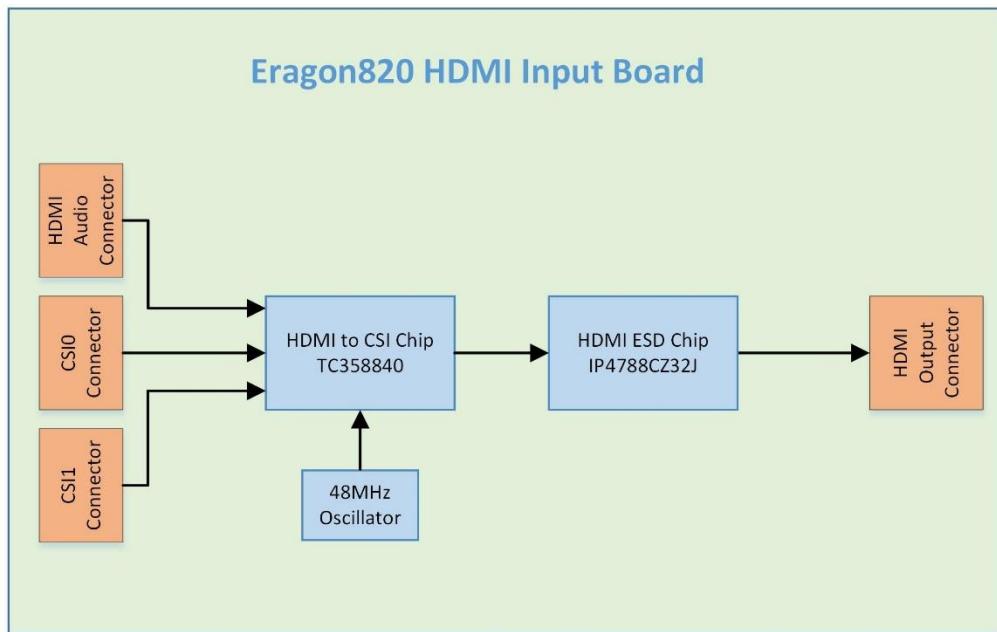
**Table 34: Audio Connector Pin out**

## 12.5 HDMI Input Board

This board is add-on accessory to Eragon820. The HDMI Input board incorporates a HDMI to CSI convertor chip (U3), ESD chip for HDMI signals (U1).

CSI signals are inputs to the HDMI to CSI chip through matting connector (J2 & J3 on HDMI Board) of Eragon 820 Carrier board (J10 & J11) connector. HDMI signals are connected to the HDMI output connector (J1).

Audio signals are connected to the HDMI input connector (J4) from J44 on Eragon820 carrier board through I2S interface for HDMI audio.



**Figure 40: HDMI Input Board**

The pin descriptions of the different connectors on HDMI Input board are as follows:

## HDMI Output Connector

Pin No.	Signal Name	Specification
J1.1	HDMI1_TMDS_TX2_P_CON	HDMI Transmit Data 2 High
J1.2	GND	Digital Ground
J1.3	HDMI1_TMDS_TX2_M_CON	HDMI Transmit Data 2 Low
J1.4	HDMI1_TMDS_TX1_P_CON	HDMI Transmit Data 1 High
J1.5	GND	Digital Ground
J1.6	HDMI1_TMDS_TX1_M_CON	HDMI Transmit Data 1 Low
J1.7	HDMI1_TMDS_TX0_P_CON	HDMI Transmit Data 0 High
J1.8	GND	Digital Ground
J1.9	HDMI1_TMDS_TX0_M_CON	HDMI Transmit Data 0 Low
J1.10	HDMI1_TMDS_TXC_P_CON	HDMI Transmit Clock High
J1.11	GND	Digital Ground
J1.12	HDMI1_TMDS_TXC_M_CON	HDMI Transmit Clock Low
J1.13	HDMI1_CEC_CONN	HDMI CEC control pin
J1.14	NC	Not Connect
J1.15	HDMI1_DDC_SCL_CONN	HDMI I2C Clock signal
J1.16	HDMI1_DDC_SDA_CONN	HDMI I2C Data signal
J1.17	GND	Digital Ground
J1.18	HDMI1_5V	5V supply for HDMI
J1.19	HDMI1_HPD_CONN	Hot Plug Detect pin

Table 35: HDMI Output Connector Pinout

## HDMI Input Connector

Pin No.	Signal Name	Specification
J4.1	DGND	Digital Ground
J4.2	DGND	Digital Ground
J4.3	HDMI_RST_N	HDMI Reset Signal (Active LOW)
J4.4	HDMI_INT_GPIO	HDMI Interrupt signal
J4.5	HDMI_MI2S_4_D0	HDMI MI2S Data 0 Signal
J4.6	HDMI_MI2S_4_D1	HDMI MI2S Data 1 Signal
J4.7	HDMI_MI2S_4_D2	HDMI MI2S Data 2 Signal
J4.8	HDMI_MI2S_4_D3	HDMI MI2S Data 3 Signal
J4.9	HDMI_MI2S_4_WS	HDMI MI2S Word Select Signal
J4.10	HDMI_MI2S_4_SCK	HDMI MI2S Serial Clock
J4.11	BLSP8_I2C_SCL	I2C Serial Clock for HDMI

J4.12	BLSP8_I2C_SDA	I2C Serial Data for HDMI
J4.13	VCC_1V8	1.8V Power Supply
J4.14	VREG_1P225	1.225V Power Supply
J4.15	VCC_3V3	3.3V Power Supply
J4.16	VCC_3V3	3.3V Power Supply

**Table 36: HDMI Input Connector Pinout**

### CSI0 Connector

Pin No.	Signal Name	Specification
J2.1	DGND	Digital Ground
J2.2	NC	Not Connect
J2.3	NC	Not Connect
J2.4	NC	Not Connect
J2.5	DGND	Digital Ground
J2.6	HDMI_I2C_SCL	HDMI I2C Clock signal
J2.7	HDMI_I2C_SDA	HDMI I2C Data signal
J2.8	DGND	Digital Ground
J2.9	NC	Not Connect
J2.10	NC	Not Connect
J2.11	NC	Not Connect
J2.12	VCC_5V0	5V supply for HDMI
J2.13	VCC_5V0	5V supply for HDMI
J2.14	VCC_5V0	5V supply for HDMI
J2.15	DGND	Digital Ground
J2.16	MIPI_CSI0_D3_P	MIPI CSI0 Data Lane3-HIGH
J2.17	MIPI_CSI0_D3_M	MIPI CSI0 Data Lane3-LOW
J2.18	DGND	Digital Ground
J2.19	MIPI_CSI0_D0_M	MIPI CSI0 Data Lane0-LOW
J2.20	MIPI_CSI0_D0_P	MIPI CSI0 Data Lane0-HIGH
J2.21	DGND	Digital Ground
J2.22	MIPI_CSI0_D1_M	MIPI CSI0 Data Lane1-LOW
J2.23	MIPI_CSI0_D1_P	MIPI CSI0 Data Lane1-HIGH
J2.24	DGND	Digital Ground
J2.25	MIPI_CSI0_D2_P	MIPI CSI0 Data Lane2-HIGH
J2.26	MIPI_CSI0_D2_M	MIPI CSI0 Data Lane2-LOW
J2.27	DGND	Digital Ground
J2.28	MIPI_CSI0_CLK_M	MIPI CSI0 Clock Lane – LOW

J2.29	MIPI_CSIO_CLK_P	MIPI CSIO Clock Lane – HIGH
J2.30	DGND	Digital Ground

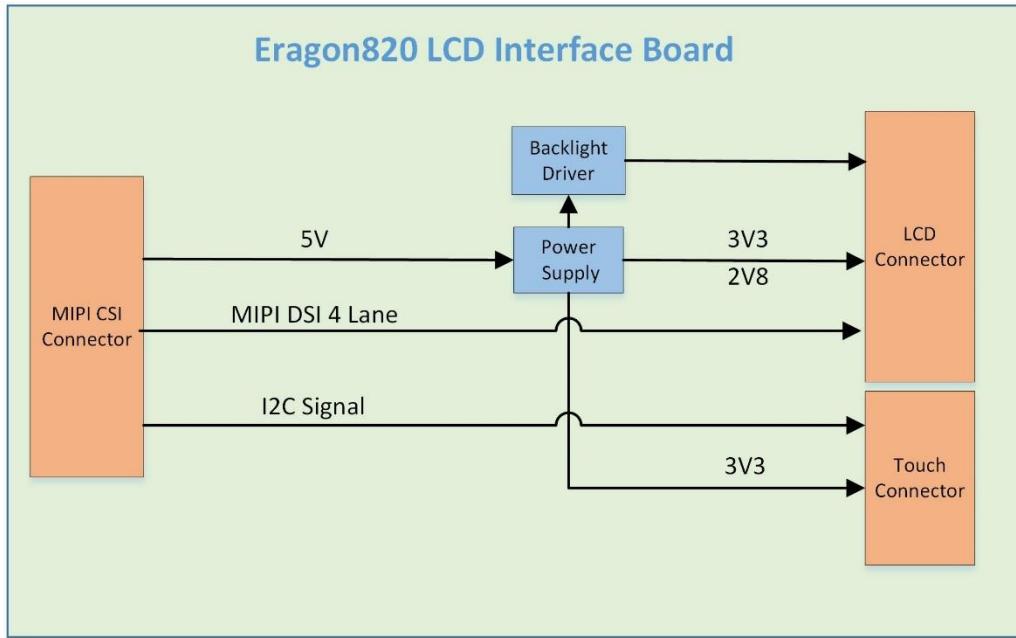
**Table 37: CSI Connector Pin out**
**CSI1 Connector**

Pin No.	Signal Name	Specification
J3.1	DGND	Digital Ground
J3.2	TP2	Test Point 2
J3.3	TP3	Test Point 1
J3.4	NC	Not Connect
J3.5	DGND	Digital Ground
J3.6	CSI_I2C0_SCL	I2C Clock Lane
J3.7	CSI_I2C0_SDA	I2C Data Lane
J3.8	DGND	Digital Ground
J3.9	NC	Not Connect
J3.10	NC	Not Connect
J3.11	NC	Not Connect
J3.12	VCC_5V0	5V Power Supply
J3.13	VCC_5V0	5V Power Supply
J3.14	VCC_5V0	5V Power Supply
J3.15	DGND	Digital Ground
J3.16	MIPI_CSI1_D3_P	MIPI CSI1 Data Lane 3-High
J3.17	MIPI_CSI1_D3_M	MIPI CSI1 Data Lane 3-Low
J3.18	DGND	Digital Ground
J3.19	MIPI_CSI1_D0_M	MIPI CSI1 Data Lane 0-Low
J3.20	MIPI_CSI1_D0_P	MIPI CSI1 Data Lane 0-High
J3.21	DGND	Digital Ground
J3.22	MIPI_CSI1_D1_M	MIPI CSI1 Data Lane 1-Low
J3.23	MIPI_CSI1_D1_P	MIPI CSI1 Data Lane 1-High
J3.24	DGND	Digital Ground
J3.25	MIPI_CSI1_D2_P	MIPI CSI1 Data Lane 2-High
J3.26	MIPI_CSI1_D2_M	MIPI CSI1 Data Lane 2-Low
J3.27	DGND	Digital Ground
J3.28	MIPI_CSI1_CLK_M	MIPI CSI1 Clock Lane-Low
J3.29	MIPI_CSI1_CLK_P	MIPI CSI1 Clock Lane-High
J3.30	DGND	Digital Ground

**Table 38: CSI Connector Pin out**

## 12.6 LCD Interface Board

This board is designed to integrate high resolution LCD and touch screen interface. The board supports 5.5" LCD from OSD displays. It is connected to MIPI interface of Eragon820. LCD control and configuration mechanism uses I2C interface. Touch screen is connected with Eragon820 using I2C interface. It has mating connector (J1) for MIPI Display connector (J13) of ERAGON820 Board.



**Figure 41: LCD Interface Board**

The pin specification of the Display connector (J4) is mentioned below:

Pin No.	Signal Name	Specification
1	NC	Not Connect
2	GND	Digital Ground
3	VCC	5V_POS
4	VCC	5V_NEG
5	GND	Digital Ground
6	GND	Digital Ground
7	MIPI_DSI0_DATA2_P_EXP_CONN	DSI Data2 Differential Positive.
8	MIPI_DSI0_DATA2_M_EXP_CONN	DSI Data2 Differential Negative.
9	GND	Digital Ground
10	MIPI_DSI0_DATA1_P_EXP_CONN	DSI Data1 Differential Positive
11	MIPI_DSI0_DATA1_M_EXP_CONN	DSI Data1 Differential Negative.
12	GND	Digital Ground
13	MIPI_DSI0_DATA0_P_EXP_CONN	DSI Data0 Differential Positive.

14	MIPI_DSI0_DATA0_M_EXP_CONN	DSI Data0 Differential Negative.
15	GND	Digital Ground
16	MIPI_DSI0_DATA3_P_EXP_CONN	DSI Data3 Differential Positive.
17	MIPI_DSI0_DATA3_M_EXP_CONN	DSI Data3 Differential Negative.
18	GND	Digital Ground
19	MIPI_DSI0_CLK_P_EXP_CONN	DSI CLK Differential Positive.
20	MIPI_DSI0_CLK_M_EXP_CONN	DSI CLK Differential Negative.
21	GND	Digital Ground
22	NC	Not Connect
23	IOVCC	1V8 Power Supply
24	IOVCC	1V8 Power Supply
25	GND	Digital Ground
26	PWM_OUT On Test point	
27	NC	Not Connect
28	LCD_RESET_N	LCD Reset(active low_3V3)
29	GND	Digital Ground
30	LEDA	BACKLIGHT LED Anode
31	LEDA	BACKLIGHT LED Anode
32	LEDK	BACKLIGHT LED Cathode
33	LEDK	BACKLIGHT LED Cathode

**Table 39: Display Connector Pin out**

The pin specification of the Touch connector (J5) is mentioned below:

Pin No.	Signal Name	Specification
1	GND	Digital Ground
2	VCC	3V3 Power Supply
3	GND	Digital Ground
4	INT LCD	Touch Interrupt
5	SDA	LCD I2C DATA
6	SCL	LCD I2C Clock
7	Reset	Reset(Active low)

**Table 40: Touch Connector Pin out**

## 13 APPENDIX 1 (HIGH LEVEL BOM)

#	Description	Manufacturer	Manufacturer Part #
1	Chip antenna for Wifi and BT	Fractus	FR05-S1-N-O-1004
2	LED RED/GREEN/BLUE WTRCLEAR SMD	Kingbright	APTF1616SEEZGQBDC
3	Board to Board & Mezzanine Connectors 100P 2R 3MM RECPT SMT VERT 0.4MM PITCH	Hirose connectors	DF40HC(3.0)-100DS-0.4V(51)
4	CONN MICRO SD CARD PUSH-PUSH R/A	Hirose Eletric	DM3AT-SF-PEJM5
5	CONN HEADR 2.54MM 20POS GOLD SMD	Sullins Connector Solutions	SBH11-NBPC-D10-SM-BK
6	Connector Receptacle USB - micro B 3.0	Mill-Max Manufacturing Corp.	897-10-010-40-300002
7	CONN MAGJACK 3PORT 1000 BASE-T	Bel Fuse	0862-1J1T-43-F
8	CONN RCPT HDMI TYPE A R/A SMD	FCI	10029449-001RLF
9	CONN .5MM HORZ BOTTOM SMD 30POS	Wurth Electronics Inc	6.8713E+11
10	CONN .5MM HORZ BOTTOM SMD 40POS	Wurth Electronics Inc	6.8714E+11
11	3.50mm Sink Audio Jack Connector	Amphenol	103-C0680-00842
12	CONN RECEPTE 16POS 2MM VERT SMD	Molex Connector Corporation	791091007
13	CONN RECEPTE 24POS 2MM VERT SMD	Molex Connector Corporation	79109-1011
14	PCIE CONNECTOR	FCII	10018784-10200TLF
15	CONN UMC JACK STR 50 OHM SMD	Hirose	U.FL-R-SMT-1(01)
16	CONN X.FL RECEPTE SMD	Hirose	X.FL-R-SMT-1(02)
17	CONN HEADER VERT 3POS 2.5MM GOLD	Molex	22111031
18	CONN POWERJACK MINI R/A PCMT	Switchcraft	RAPC712X
19	CONN HEADER ACH SIDE 6POS 1.2MM	JST Sales America Inc.	BM06B-ACHFKS-GACN-ETF
20	CONN HEADER 2POS 1.25MM VERT TIN	Molex Inc	530470210
21	CONN RCPT 30POS 0.4MM SMD GOLD	Hirose Electric Co Ltd	DF40HC(3.0)-30DS-0.4V(51)
22	CONN .5MM HORZ BOTTOM SMD 16POS	Wurth Electronics Inc	6.87116E+11

23	LED GREEN CLEAR 0603 SMD	Lite-On Inc	LTST-C190KGKT
24	SWITCH TACTILE SPST-NO 0.05A 16V	C&K Components	PTS810 SJM 250 SMTR LFS
25	TVS DIODE 10UQFN	Texas Instruments	TPD6E001RSER
26	IC EEPROM 128KBIT 1MHZ 8SOIC	Atmel	AT24C128C-SSHM-B
27	3-PORT USB 2.0 HUB CTRLR 36VQFN	Microchip Technology	USB2513B-AEZC-TR
28	IC POWER DIST SWITCH ADJ 10SON	Texas Instruments	TPS2561DRCT
29	TVS DIODE 5VWM 7VC UDFN10	Littelfuse Inc.	SP3012-04UTG
30	IC DVI/HDMI ESD PROTECT 32HVQFN	NXP Semiconductors	IP4788CZ32J
31	IC BUS TRANSCVR 4BIT DUAL 16QFN	TI	SN74AVC4T774RSVR
32	IC PCI to PHY Converter	Artheros	AR8151-B
33	IC VOLT LEVEL TRANSLATOR US8	Texas Instruments	PCA9306DCUR
34	ACCELEROMETER 3D MAGNO 16LGA	STMicroelectronics	LSM303DTR
35	IMUs - Inertial Measurement Units 6-Axis	Bosch Sensortec	BMI160
36	IC I/O EXPANDER I2C 16B 24WQFN	NXP Semiconductors	PCA6416AHF,128
37	IC DRVR/RCVR RS232 1CH 16-TSSOP	Texas Instruments	MAX3221EIPWR
38	IC TRANSLATOR VOLTAGE 8-X2SON	Texas Instruments	TXS0102DQER
39	TRANS PREBIAS DUAL NPN EMT6	Rohm Semiconductor	EMH9T2R
40	IC REG BUCK ADJ 8A SYNC 14QFN	Texas Instruments	TPS54821RHLR
41	IC REG BUCK SYNC ADJ 4A 16QFN	Texas Instruments	TPS54426RSAR
42	IC REG BUCK ADJ 3A SYNC 16QFN	Texas Instruments	TPS62090RGTR
43	TVS DIODE 6SOT	Texas Instruments	TPD3S044DBVR
44	IC BUFF/DVR NON-INVERT SOT235	Texas Instruments	SN74LVC1G07DBVR
45	Crystal 24.0000MHz, SMD	Abracan	ABM8-24.000MHZ-B2-T
46	CRYSTAL 25MHZ 18PF SMD	Abracan Corporation	ABM8G-25.000MHZ-18-D2Y-T

**Table 41: High Level BOM**

## 14 About eInfochips

eInfochips is a Product and Semiconductor Design Solutions company, based out of Sunnyvale (USA) and Ahmedabad (India). The company has delivered turnkey solutions from its global offshore development centres for industries like Aerospace & Defence, Security & Surveillance, Semiconductor, Consumer Electronics, Medical Devices, Media & Broadcast, Retail and Software.

Being an innovation driven company, eInfochips has a portfolio of in-house hardware and software IPs to accelerate product development and testing. Having contributed to over 500+ customer products that have more than 10 Million deployments worldwide, eInfochips expertise has been recognized by reputed global agencies like Gartner, Frost & Sullivan and Zinnov.

Comprehensive expertise and intricate understanding of Qualcomm Technologies, Inc.'s Qualcomm® Snapdragon™ processors makes eInfochips an ideal partner for efficient and high performance designs

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