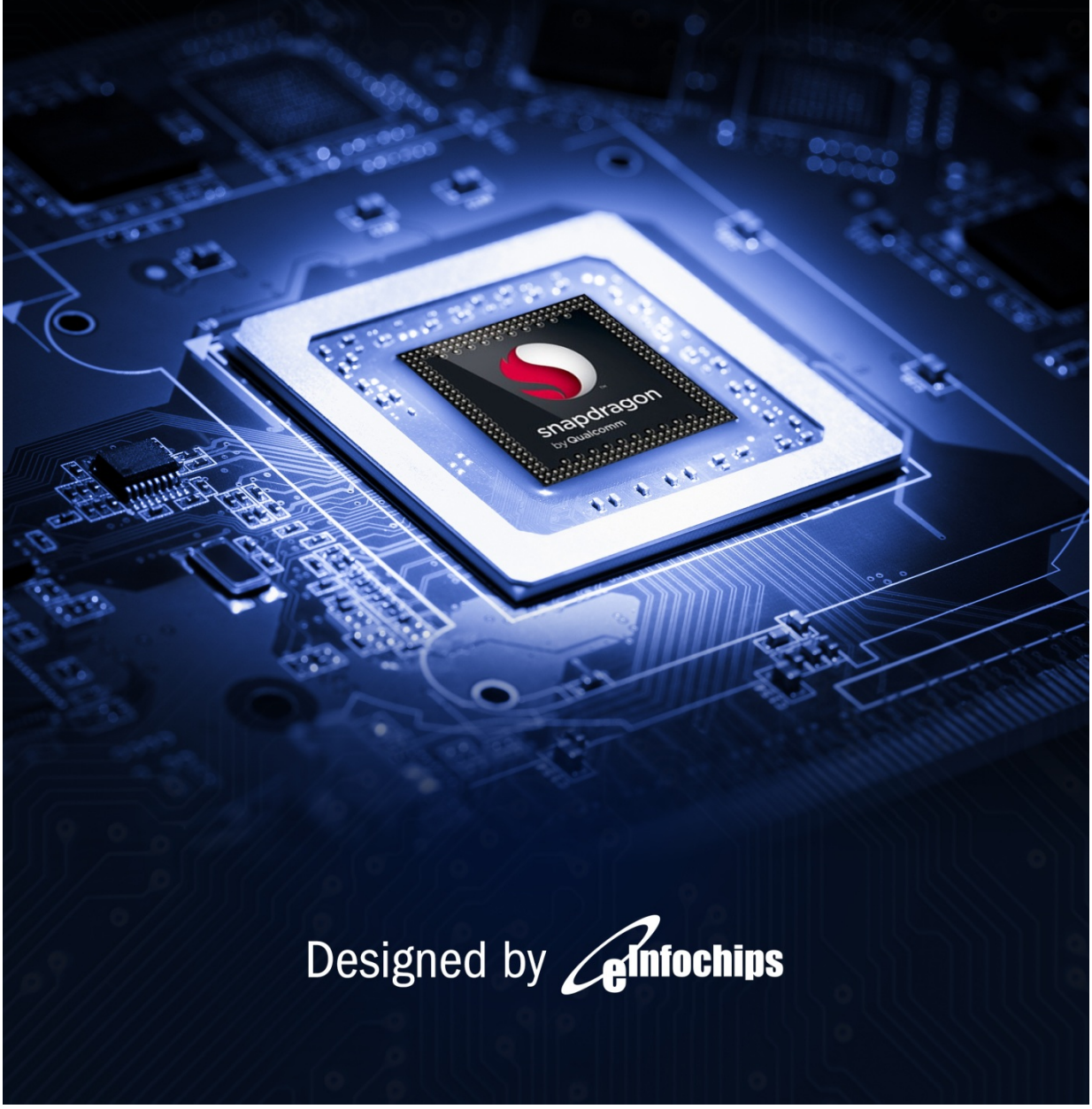
eragon 820

Chipset Overview



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1 Document Details

1.1 Document History

Version	Author		Reviewer		Approver		Description Of Changes
	Name	Date	Name	Date	Name	Date	
Release ver. 1.0	*eInfochips*	*03-Sep-2016*	*eInfochips*	*03-Sep-2016*	*eInfochips*	*23-Sep-2016*	*Initial release*

Table 1 Document History

1.2 Definition, Acronyms and Abbreviations

Term	Definition
ADC	Analog-to-digital converter
AGC	Automatic gain control
ANC	Active noise cancellation
bps	Bits per second
BER	Bit error rate
BLSP	BAM-based low-speed peripheral
CA	Carrier aggregation
CDMA	Code division multiple access
CRC	Cyclic redundancy check
CSI	Camera serial interface
DAC	Digital-to-analog converter
DC-HSPA+	Dual-carrier HSPA+
DDR	Double data rate
DLCA	Downlink carrier aggregation
DMB	Digital mobile broadcast
DRM	Digital Rights Management
DSI	Display serial interface
DSP	Digital signal processor
EBI	External bus interface
EDGE	Enhanced data rates for GSM evolution
EDR	Enhanced data rate

Term	Definition
eMMC	Embedded multimedia card
ET	Envelope tracking
ETM	Embedded trace macrocell
EV-DO	Evolution data optimized
FB	Feedback
FDD	Frequency division duplex
FE	Front-end
FFA	Form-fit-accurate evaluation platform
GFX	Graphics
GLONASS	Global orbiting navigation satellite system
GNSS	Global navigation satellite system
GPIO	General-purpose input/output
GPRS	General packet radio services
GPS	Global positioning system
GRFC	Generic RF controller
GSM	Global system for mobile communications
HB	High-Band
HDCP	High-bandwidth digital content protection
HDMI	High-definition multimedia interface
HEVC	High Efficiency Video Coding
HSDPA	High-speed downlink packet access
HSIC	High-speed inter-chip
HSPA+	High-speed packet access
HSUPA	High-speed uplink packet access
I2C	Inter-integrated circuit
I2S	Inter-IC sound
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group (ANSI/ICEEE Std. 1149.1-1990)
kbps	kilobits per second
LB	Low-Band
LCD	Liquid crystal display
LPA	Low-power audio
LPASS	Low-power audio subsystem
LPDDR	Low-power DDR

Term	Definition
LSB	The LSB can either be the least significant bit or least significant byte. All instances of LSB used in this manual are assumed to be LSByte, unless specified otherwise.
LTE	Long-term evolution
MB	Mid-Band
MBHC	Multiple button headset control
MBP	Mobile broadcast platform
MDP	Mobile display processor
MIPI	Mobile industry processor interface
MMC	Multimedia card
MNSP	Package-on-package nanoscale package
MPM	Modem power management
MSB	The MSB can either be the most significant bit or most significant byte. All instances of MSB used in this manual are assumed to be MSByte, unless specified otherwise.
NFC	Near field communicator
NSP	Nanoscale package
OMA	Open Mobile Alliance
PA	Power amplifier
PCB	Printed circuit board
PCIe	Peripheral component interconnect express
PCM	Pulse-coded modulation
PDM	Pulse-density modulation
PM	Power management
PoP	Package-on-package
QDSS	Qualcomm debug subsystem
QFPROM	Qualcomm fuse programmable read-only memory
QLIC	Quasi-linear interference cancellation
QTI	Qualcomm Technologies, Inc.
radioOne	Zero-IF (ZIF) radio architecture
RBDS	Radio broadcast data system
RDS	Radio data system
RFFE	RF front end
RLP	Radio link protocol
RPM	Resource power manager
SD	Secure digital

Term	Definition
SDC	Secure digital controller
SDRAM	Synchronous dynamic random access memory
SEE	Secure Execution Environment
SFS	Secure file system
SIM	Subscriber identity module
SLIMbus	Serial Low-power Inter-chip Media Bus
SMT	Surface mount technology
SPI	Serial peripheral interface
SPMI	Serial power management interface
sps	Symbols per second (or samples per second)
SSC	Snapdragon sensor core
SVA	Snapdragon voice activation
TAP	Test access port
TCXO	Temperature-compensated crystal oscillator
TD-SCDMA	Time Division Synchronous Code Division Multiple Access
TDD	Time division duplex
TSIF	Transport stream interface
UART	Universal asynchronous receiver transmitter
UFS	Universal Flash Storage
UICC	Universal integrated circuit card
UIM	User identity module
ULCA	Uplink carrier aggregation
UMTS	Universal mobile telecommunications system
USB	Universal serial bus
USB-OTG	Universal serial bus on-the-go
USIM	UMTS subscriber identity module
WAN	Wide area network
WCDMA	Wideband code division multiple access
WCN	Wireless connectivity network
WiGig	Wireless Gigabit Alliance
WLAN	Wireless local area network
WTR	Wafer-scale RF transceiver
XO	Crystal oscillator

Term	Definition
ZIF	Zero intermediate frequency

Table 2 Definition, Acronyms and Abbreviations

2 License Agreement

The use of this document is subject to and governed by those terms and conditions in the eInfochips Ltd. Purchase and Software License Agreement for the APQ8096 based development platform, which you or the legal entity you represent, as the case may be, accepted and agreed to when purchasing ERAGON820 development platform from eInfochips Ltd. ("Agreement"). You may use this document, which shall be considered part of the defined term "Documentation" for purposes of the Agreement, solely in support of your permitted use of the ERAGON820 development platform under the Agreement. Distribution of this document is strictly prohibited without the express written permission of eInfochips Ltd. and its respective licensors, which they can withhold, condition or delay in its sole discretion.

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3 Preface

This document provides an overview of the APQ8096 SoC.

3.1 Intended Audience

This document is intended for technically qualified personnel. It is not intended for general audience.

3.2 Intended Use

The development platform supports a wide range of industry interfaces and offers a comprehensive hardware and software design. It comes with Android 6.0 software packages and pre-built sample demo applications for easy adaption.

This platform enables developers to evaluate and create solutions targeted at various market segments while customers and OEMs can build their products based on these designs directly or with customizations.

3.3 Conventions

The following conventions are used in this document.


CAUTION: Cautions warn the user about how to prevent damage to hardware or loss of data.


NOTE: Notes call attention to important information.

4 Introduction

This document describes features and functionality of the Qualcomm® Snapdragon™ 820 processor (model APQ8096) for embedded computing.
Qualcomm processors designed to perform embedded computing are dedicated to support embedded device OEMs in several ways such as

- Providing detailed documentation for developers.
- Ease of availability of development kits/community board for early access.
- Support for Multiple OS including support for mainline Linux.
- Availability of several computing module partners for customization for your individual projects/products.

Snapdragon 820 processors deliver high-performance computing, low power consumption and a rich multimedia experience for embedded devices.

It is an ideal solution for any application requiring computing horsepower and integrated Wi-Fi/Bluetooth connectivity. These applications can be Smart Home; Industrial Appliances, Digital Media and TV dongles, Smart Surveillance and Robotics.

Snapdragon supports a clear deployment path for embedded device OEMs and developers ranging from single-board computers and development kits to providing robust solutions to customer requirements, integration services and building production-ready as well as customizable computing modules.

4.1 About Chipset and ERAGON820 Development Kit

Customers can now get access to the QUALCOMM Snapdragon APQ8096 chipset through ERAGON820 SoM and Development Kit. The complete kit and platform is available for purchase via eInfochips Inc.
For more information, please visit our website www.einfochips.com

To obtain any information that is not included in this document or any information beyond the scope of this document, contact eInfochips.

For accessing additional documentation and software updates, please visit our support center at www.supportcenter.einfochips.com

For software and hardware support, please email us at qcsupport@einfochips.com

4.2 Special Marks

Defines special marks used in this document.

	Guidelines
[ ]	Brackets ([ ]) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, DATA [7:4] may indicate a range that is 4 bits in length, or DATA [7:0] may refer to all eight DATA pins.
_N	A suffix of _N indicates an active low signal. For example, RESIN_N.
0x0000	Hexadecimal numbers are identified with an x in the number (for example, 0x0000). All numbers are decimal (base 10) unless specified otherwise. Binary numbers have the term binary enclosed in parentheses at the end of the number; for example, 0011 (binary).
|	A blue vertical bar in the outer margin of a page indicates that a change was made since the previous revision of this document

Table 3 Special Marks

5 APQ8096 Overview

Embedded computing devices continue to integrate more and increasingly complex functions. They support more functionality while increasing performance and reducing the board space and cost.

These demands are met by the APQ8096 – with its processor system that includes a customized 64-bit ARMv8-compliant quad-core applications processor (Qualcomm Kryo) – which further expands the mass-market chipset capabilities by making rich multimedia features accessible to more consumers worldwide.

The APQ8096 has a high level of integration that reduces the bill-of-material (BOM), which delivers board-area savings. The cost and time-to-market advantages of this IC will help drive adoption in mass markets around the world.

Wireless products based on the APQ8096 chipset may include:

- Music player-enabled devices and applications
- Cameras
- Devices with gaming, video streaming, and video conferencing features
- GPS, GLONASS, and BeiDou for global location-based service (with WGR7640).
- Wireless connectivity–Bluetooth, WLAN, and FM receiver (with QCA6174A-1)

The APQ8096 benefits are applied to each of these product types and include:

- Higher integration to reduce PCB surface area, time-to-market, and BOM costs while adding capabilities and processing power
- Integrated application processors and hardware cores to eliminate multimedia coprocessors, and to provide superior image quality and resolution for devices while extending application times.
- Higher computing power for high-end applications, and DC power savings for longer run times
- Position location and navigation systems supported through the WGR7640 global navigation satellite system (GNSS) receiver
- The APQ8096 Chipset supports Gen 8C operation
    - Standalone GPS, GLONASS, and COMPASS
    - Small, power- and thermal-efficient WGR7640 packaging
- A single platform providing dedicated support for all market-leading codecs and other multimedia formats to support deployments around the world
- DC power reduction using innovative techniques
- Support for the latest, most popular operating systems.

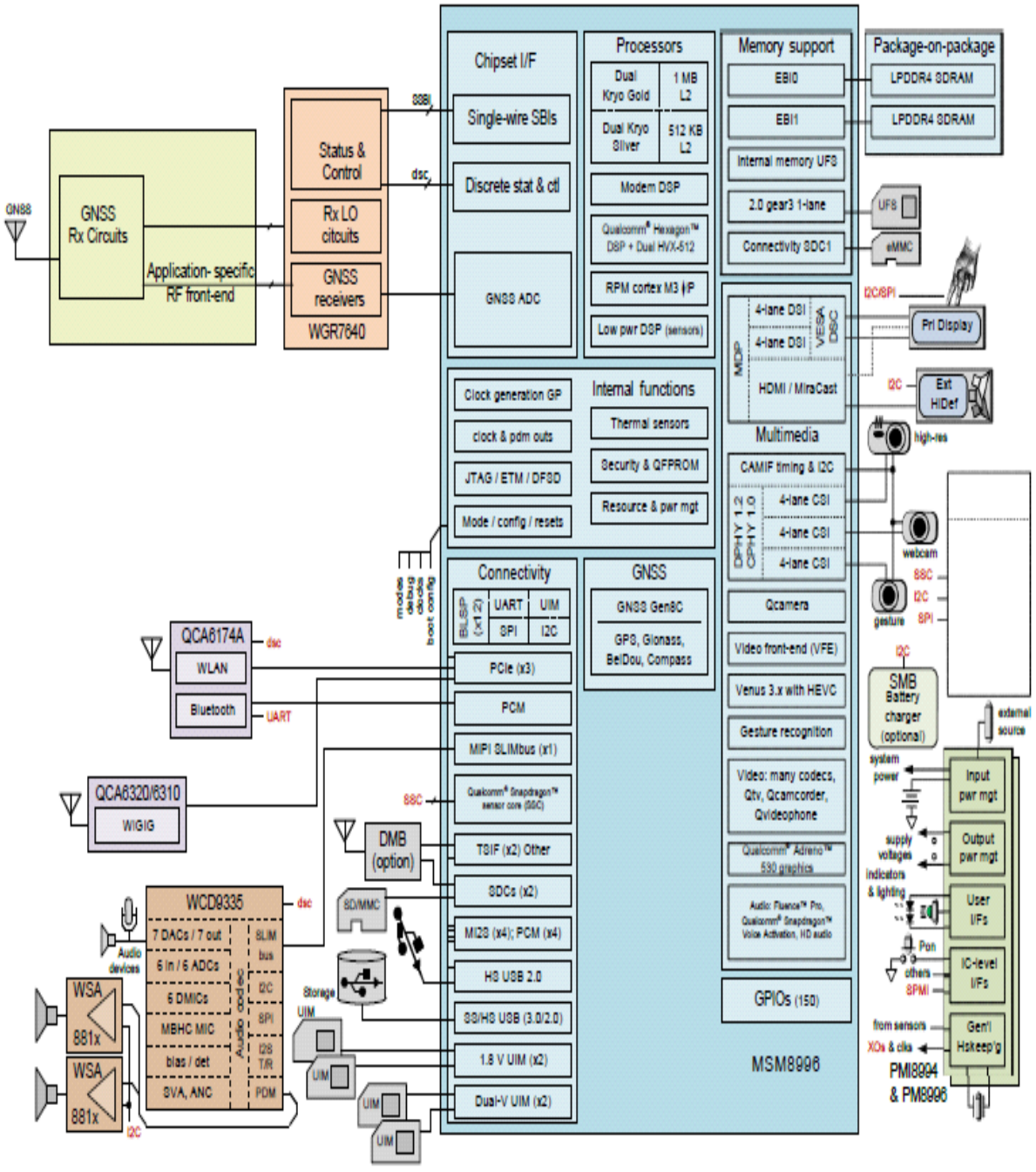


Figure 1 APQ8096 functional block diagram and example application

The APQ8096 is fabricated using the advanced 14 nm FinFET process for lower active power dissipation and faster peak CPU performance. It is available in the 994C MNSP 11, a 15.6 × 15 × 0.64 mm package-on-package (PoP) system (height dimension does not include the memory device). Its bottom footprint is equivalent to a 994-pin nanoscale package (994 NSP), and it accepts memory modules from above that are equivalent to a 387-pin chip-scale package (387 CSP).The bottom includes many ground pins for improved electrical grounding, mechanical strength, and thermal continuity.

The APQ8096 supports high-performance applications worldwide using GPS, GNSS, and BeiDou wireless networks.

Complementary ICs within the APQ8096 chipset include:

- Power management and charger ICs:
  - PMI8994 power management IC
  - PM8996 power management IC
  - SMB1351 battery charger IC
- Wireless connectivity ICs:
  - QCA6174A for WLAN and Bluetooth
  - QCA6320/QCA6310 WiGig IC
- Audio ICs:
  - WCD9335 audio codec IC
  - WSA8810 speaker driver IC

Since the APQ8096 includes so many diverse functions, its operation is more easily understood by considering major functional blocks individually. Therefore, the APQ8096 document set is organized according to the following block partitioning:

- Architecture and baseband processors
- Memory support
- Air interfaces
- Multimedia
- Connectivity
- Internal functions
- Interfaces to other functions (including the other ICs within the chipset)
- Configurable general-purpose input/output (GPIO) ports

Most of the information contained in this device specification is organized accordingly – including the circuit groupings within its functional block diagram (Figure 1), pin descriptions (Section Pin Definitions), and detailed electrical specifications (Section Electrical Specifications).

5.1 APQ8096 features


NOTE: *Some of the hardware features integrated within the APQ8096 device must be enabled by software. See the latest version of the applicable software release notes to identify the hardware features that are enabled.*

Features integrated into APQ8096 are as follows:

- 14 nm FinFET process for lower active power dissipation and faster peak CPU performance
- Customized 64-bit ARMv8-compliant quad-core applications processor (Kryo) organized in two clusters
  - Two high-performance Kryo cores – gold cluster (target 2.15 GHz)
  - Two low-power Kryo cores – silver cluster (target 1.6 GHz)
- Hexagon DSP with dual-Hexagon vector processor (HVX-512) designed for 825 MHz
- Dual-channel PoP high-speed memory – LPDDR4 SDRAM designed for 1866 MHz clock rate
- Two 4-lane DSI DPHY 1.2 and HDMI 2.0 (4k60) or 4k30 Miracast
- Display 3840 × 2400 at 60fps, 2560 buffer width (10 layers blending), VESA DSC 1.1
- Complete 4k60 entertainment system (4k60 H.265/VP9 decode with uncompressed 4k display, HDMI 2.0)
  - Improved video decode performance – 1080p240/4K60/8x1080p30: H.264, VP8, HEVC 8/10-bit, VP9 1080p60
  - Improved video encode performance – 1080p120/4K30/4x1080p30: H.264, VP8, HEVC
  - Improved concurrent video performance – 4K60 decode + 4K30 4:2:0 encode, 4K60 decode
- Three 4-lane CSI (4+4+4 or 4+4+2+1) DPHY1.2 at 2.0 Gbps per lane or Three 3-trio CPHY1.0 at 17Gbps
- Dual 14-bit image signal processing (ISP) – 28 MP and 13 MP, 600 MHz; 32 MP 30 ZSL with dual-ISP; 16 MP 30 ZSL with single-ISP; TempNR v2, ASF3, Demosaic, Dual-AF, LTM, CAC, Green Imbalance, Pedestal, stats upgrades, and image quality enhancements
- Adreno 530 graphics processing unit (GPU) with 64-bit addressing; designed for 624 MHz
- Support for UFS2.0 gear 3 (1-lane), eMMC5.1, and SD3.0
- Dedicated low-power SSC with DSP to support always-on use cases
- WLAN 802.11ac and Bluetooth 4.1 supported through QCA6174A; WiGig (802.11ad/ 60 GHz) with QCA9500 – through respective PCIe interfaces
- Three PCIe interfaces

5.2 Summary of APQ8096 features

APQ8096 features are summarized in Table 4

Feature	APQ8096 capability
Processors	
Applications	Customized 64-bit ARMv8-compliant quad-core applications processor (Kryo) ▪ Two high-performance Kryo cores – Gold cluster (2.15 GHz) ▪ Two low-power Kryo cores – Silver cluster (1.593 GHz)
Digital signal processing	Hexagon DSP with dual-Hexagon vector processor (HVX-512) (target 825 MHz)
RPM system	Cortex M3 ▪ Better suited for code certification and warm boot ▪ Brings up secure root of trust (SROT) application processors quickly ▪ The only master of the APQ power manager (APM) ▪ APM coordinates shutdown/wakeup, clock rates, and VDDs
Sensor core	Dedicated low-power Snapdragon sensor core with DSP with direct access to internal cores to support always-on low-power use cases.
Memory support	
System memory via PoP and EBI	Dual-channel PoP high-speed memory – LPDDR4 SDRAM designed for 1866 MHz clock
Other internal memory	256 KB OCIMEM 1 MB GMEM for GFX 512 KB VMEM for Video
External memory	
Via UFS	UFS2.0 gear3 – 1 lane
Via SDC1	eMMC5.1 NAND flash device
Air interfaces	
WLAN/Bluetooth	Yes (with QCA6174A)
GNSS – IZat engine	Gen 8C; GPS, GLONASS, and BeiDou
Multimedia	
Display support	Up to three concurrent displays; two panels + external
MIPI_DSI	Two; 4-lane + 4-lane; DSI DPHY 1.2; VESA DSC 1.1
HDMI	Yes; v2.0 (4k 60)
Miracast	Yes; v2.0
Example combinations	3840 × 2400 at 60 fps 2560 buffer width (10 layers blending) VESA DSC 1.1
General display features	Color depth – 24-bit pp; TFT, LTPS, CSTN, OLED panels
Camera interfaces	Qcamera; 1 GP dual ISP
MIPI_CSI	Three 4-lane ▪ Legacy mode CSIx_LANEx_P/M (DPHY1.2, maximum 8 Gbps 4-lanes) ▪ New trio mode with 3-lanes of 3-pins each (CPHY1.0, maximum 17 Gbps)
2D performance	Dual 14-bit ISP 28 MP + 13 MP, 600 MHz each 28 MP30 ZSL with dual ISP 16 MP30 ZSL with single ISP TempNR v2, ASF3, Demosaic, Dual AF, LTM, CAC, Green Imbalance, Pedestal, statistics upgrades, image quality enhancements
Flexible 3A	Tier 1 customization support, gyro integration
Hardware post processor	Hardware temporal NR, zooming, rotator, upscaling

Feature	APQ8096 capability
VFE features	No LBC, move LSC, ABF3, demosaic, dual AF, CSC, LTM, gamma, green imbalance, pedestal, stats upgrades, 14-bit pipeline
Mobile display processor	MDP 570
Video applications performance	
Encode	1080p120/4K30/4x 1080p30: H.264, VP8, HEVC
Decode	1080p240/4K60/8x 1080p30: H.264, VP8, HEVC 8/10-bit, VP9
Concurrency	4K30 decode + 4K30 encode 4K60 decode + 1080p60 encode
Graphics	Adreno 530 3D graphics accelerator with 64-bit addressing 624 MHz OpenGL ES 3.0/3.1/GEP, GL4.4, DX11.3/4, Path Rendering OpenCL 2.0 Full, Renderscript-Next
Audio	
Codec	Integrated within the hi-fi audio codec WCD9335 device: ▪ Seven DACs, seven outputs ▪ Six differential analog inputs with dedicated ADCs ▪ Six digital microphones ▪ Snapdragon voice activation (SVA) subsystem for ultra low voice wake-up ▪ MBHC, ANC ▪ 130 dB dynamic range, 24-bit DAC ▪ 44.1 kHz native playback ▪ SLIMbus to I2S bridge
Speaker amplifier	Integrated within the WSA8810/WSA8815 class D/G, low noise Smart Amplifier: ▪ 4 W output power into 8 Ω load ▪ Integrated SmartBoost ▪ Integrated feedback speaker protection for excursion and temperature control of the transducers ▪ Battery voltage monitoring
Low-power audio	Low-power, low-complexity; 7.1 surround sound
Voice codec support	SILK; QCELP, EVRC, EVRC-B, EVRC-WB; G.711, G.729A/AB; GSM-FR, -EFR, -HR; AMR-NB, -WB
Audio codec support	MP3; AAC, +, eAAC; WMA 9/Pro; Dolby AC-3, eAC-3, DTS
Enhanced audio	▪ Surround sound: Dolby True-HD; DTS-HD; DTS express 7.1 ▪ Fluence noise cancellation; enhanced speaker protection ▪ QAudioFX/Qconcert/QEnsemble
A/V output – HDMI Rev 2.0	Yes ▪ Integrated HDMI Tx core and HDMI PHY ▪ 1080p at 60 Hz refresh; 24-bit RGB color ▪ 4k × 2k at 60 fps + 4k × 2k at 30 fps HDMI ▪ Up to 8-channel audio for 7.1 surround sound ▪ Dolby Digital Plus, Dolby True-HD, and DTS-HD Master
Digital mobile broadcast (DMB)	External IC required; dual-TSIF for 12 segment ISDB-T
Connectivity	
BLSP ports	12, 4 bits each; multiplexed serial interface functions
UART	Yes – up to 4 MHz
UIM	Yes – SIM, USIM, CSIM
I2C	Yes – cameras, sensors, near field communicator (NFC), etc.
SPI	Yes – cameras, sensors, etc.
UIM (other than via BLSP)	Two – dual voltage (1.8/2.95

Feature	APQ8096 capability
	V) Two – 1.8 V only
USB	Two – one USB 2.0 high-speed and one USB 3.0 super-speed/USB 2.0 high-speed compliant
PCIe	Three – PCI-SIG PCIe v2.1 PHY and 2.1 controller
Secure digital interfaces	▪ Up to three ports; one 8-bit and two 4-bit; SD 3.0 ▪ SDC2 is dual-V ▪ SD/MMC card; eMMC NAND; DMB; eSD/eMMC boot
TSIF	Up to two ports; DMB support
Audio interfaces	
SLIMbus	One; highly multiplexed, high-speed; baseline WCD9335
MI2S	▪ Full duplex stereo or up to quad channel Tx/Rx MI2S (x3) ▪ Up to 8 channel for multi-channel audio applications (x1)
PCM	Short and long sync PCM support
Wireless connectivity	QCA6174A (Wi-Fi + Bluetooth) QCA6320/QCA6310 (802.11ad/60 GHz)
Touchscreen support	Capacitive panels via ext IC (I2C, SPI, and interrupts)
DMB support	Via external DMB device (SDC or TSIF)
Sensors	Snapdragon sensor core (dedicated Q6 low-power island with 512 KB)
Configurable GPIOs	
Number of GPIO ports	150 – GPIO_0 to GPIO_149
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs
Internal functions	
Security	
General security features	Secure boot, SFS, OMA DRM 1.0/2.1, TrustZone, Qualcomm® Secure Execution Environment, secure debug, Microsoft WM DRM10, HDCP for HDMI
Crypto engine	V4; algorithm accelerates file system encryption (AES-XTS) and IPSec and SSL (HMAC-SHA, CCM, CBCMAC)
QFPROM	▪ Large fuse array, replaces previous-generation Qfuse chains ▪ Nonvolatile memory with faster and simpler programming
Security controller	▪ Chip-wide configuration for security, feature enable, and debug ▪ Persistent storage of ID numbers and sensitive key data ▪ Support for the HDCP standard needed for HDMI ▪ Secure HDCP key provisioning and secure debug facility ▪ Gateway for all software and JTAG accesses to the QFPROM ▪ Primary and secondary hardware key blocking for SFS
Boot sequence	1) Applications PBL, 2) RPM, 3) HLOS, 4) modem PBL Emergency boot over USB 3.0
PLLs and clocks	▪ Multiple clock regimes; watchdog and sleep timers ▪ Inputs: 19.2 MHz CXO, CXO_2 ▪ General-purpose outputs: M/N counter, PDM
Resource and power manager	▪ Fundamental to power management ▪ Key blocks: RPM core, Cortex M3, security controller, APM ▪ Improved efficiency via clock control, split-rail power collapse and voltage scaling; several low-power sleep modes
Debug	JTAG, Design for software debug (DFSD), and ETM (all cores)

Feature	APQ8096 capability
Others	Thermal sensors; modes and resets; peripheral subsystem
Chipset and RF front-end (RFFE) interface features	
WTR RF transceivers (not applicable to APQ8096)	
Baseband data	Six Rx and two Tx analog interfaces
Status and control	RFFE for each RFIC, plus other lines as needed via GPIOs
Power management	2-line SPMI; plus other lines as needed via GPIOs
WCD audio codec	
SLIMbus	Highly muxed, high-speed audio data plus status and control
Others	Status, control, and clock lines as needed via GPIOs
Wireless connectivity	
WLAN baseband data	PCIe
Bluetooth	PCM and UART interfaces
Fabrication technology and package	
Digital die	14 nm FinFET process for lower active power dissipation, faster peak CPU
NG PoP – small, thermally efficient package	994C MNSP: 15.6 × 15.0 × 0.64 mm (without memory device on top)
Bottom pin array of PoP	Same as 994-pin nanoscale package (994 NSP); 0.4 mm pitch
Top pin array of PoP	Same as 387-pin chipscale package (387 CSP); 0.5 mm pitch

Table 4 Key APQ8096 features

Standard	Feature descriptions
IZat with global navigation satellite system (GNSS) support	
Gen8C	GPS and GLONASS (GNSS), BeiDou/Compass, and Galileo

Table 5 Position location and navigation summary

Standard	Feature descriptions
WLAN	
With QCA6174A	802.11ac, 2 × 2 MIMO
With QCA6320/QCA6310	WiGIG – 802.11ad, 60 GHz
Bluetooth	
With QCA6174A	Bluetooth 4.1 and earlier

Table 6 Wireless connectivity summary by standard

6 Memory Map

The memory map is depicted in the following figure.

0x200000000		
0x800000000	DDR_RAM (6 GB)	Read-Write
0x120000000	RESERVED (1.7 GB)	
0x100000000	MODEM (32 MB)	Read-Write
0x0E0000000	PCIE_2_PCIE20_WRAPPER_AXI (32 MB)	Read-Write
0x0D0000000	PCIE_1_PCIE20_WRAPPER_AXI (16 MB)	Read-Write
0x0C000000	PCIE_0_PCIE20_WRAPPER_AXI (16 MB)	Read-Write
0x0B000000	RESERVED (16 MB)	
0x0A000000	RESERVED (16 MB)	
0x09800000	RESERVED (8 MB)	
0x09000000	LPASS (8 MB)	Read-Write
0x08000000	QDSS_STM (16 MB)	Read-Write
0x07800000	RESERVED (8 MB)	
0x07400000	PERIPH_SS (4 MB)	Read-Write
0x06C00000	RESERVED (8 MB)	
0x06A00000	USB30_PRIM (2 MB)	Read-Write
0x06900000	RESERVED (1 MB)	
0x06800000	MMSS_VMEM (1 MB)	Read-Write
0x066C0000	RESERVED (1.3 MB)	
0x06680000	SYSTEM_IMEM (256 kB)	Read-Write
0x06603000	RESERVED (500 kB)	
0x06602000	RESERVED (4 kB)	
0x06601000	RESERVED (4 kB)	
0x06600000	RESERVED (4 kB)	
0x06400000	RESERVED (2 MB)	
0x06100000	RESERVED (3 MB)	
0x06000000	RESERVED (1 MB)	
0x00000000	CONFIG_NOC (96 MB)	

Figure 2 System Memory Map

7 Pin Definitions

The APQ8096 is the lower device within a package-on-package system, as illustrated and explained in Figure 3

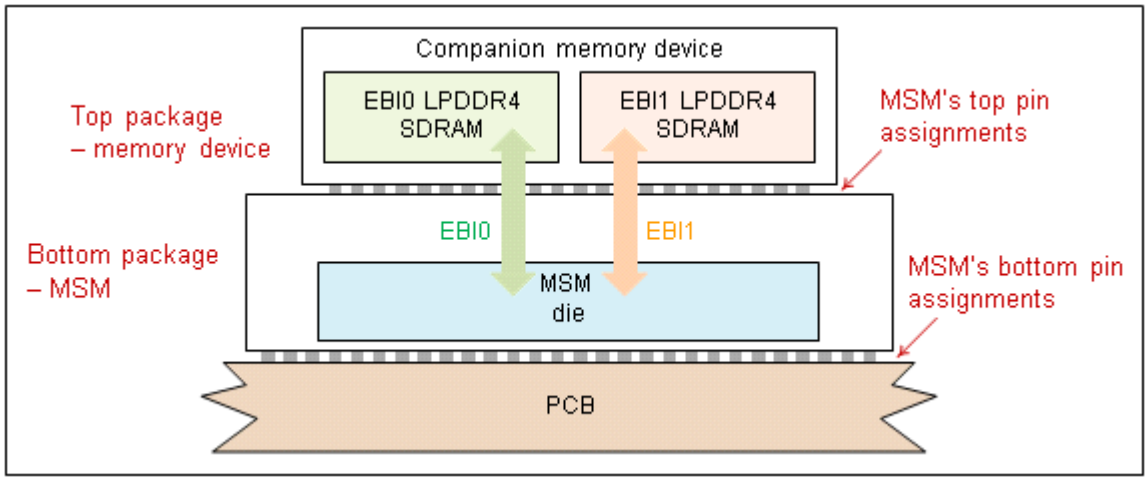


Figure 3 Package-on-package system pin assignments

Two sets of pin assignment details are presented in this document

- APQ8096 bottom pins (Section 7.2)
- APQ8096 top pins (Section 7.4)

7.1 I/O parameter definitions

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input(CMOS)
DO	Digital output(CMOS)
H	High Voltage tolerant
S	Schmitt trigger input
Z	High Impedance (high-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pulldown with programmable options following the colon (:) PU: nppdkp = default pullup with programmable options following the colon (:)

Symbol	Description
	KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pullup device
PD	Contains an internal pulldown device
Pad voltage groupings for baseband circuits	
P1	Pad group 1 (EBI pads); tied to VDD_P1 pins (1.1 V only)
P2	Pad group 2 (SDC2); tied to VDD_P2 pins (1.8 V or 2..95 V)
P3	Pad group 3 (most peripherals); tied to VDD_P3 pins (1.8 V only)
P5	Pad group 5 (UIM1); tied to VDD_P5 pins (1.8 V or 2.95 V)
P6	Pad group 6 (UIM2); tied to VDD_P6 pins (1.8 V or 2.95 V)
P7	Pad group 7 (SDC1); tied to VDD_P7 pins (1.8 V only)
P9	Pad group 9 (CXO_2 and QREFS_REXT); tied to VDD_P9 pins (1.8 V only)
P10	Pad group 10 (UFS_CLK and UFS_RESET); tied to VDD_P10 pins (1.2 V only)
P11	Pad group 11 (CXO); tied to VDD_P11 pins (1.8 V only)
P12	Pad group 12 (SSC); tied to VDD_P12 pins (1.8 V only)
CSI	Supply voltage for MIPI_CSI circuits and I/Os; tied to VDD_MIPI_CSI (1.8 V only)
DSI	Supply voltage for MIPI_DSI circuits and I/Os; tied to VDD_MIPI_DSI (1.8 V only)
Output current drive strength	
3.0 V (H) pads	Programmable drive strength, 2–8 mA in 2 mA steps.
1.8 V UIM pads	Programmable drive strength for 1.8 V UIM pads, TBD to TBD mA in TBD mA steps.
Others [1]	Programmable drive strength, 2–16 mA in 2 mA steps.

1. Digital pads other than EBI pads, high-voltage tolerant pads, or 1.8 V UIM pads.

Table 7 I/O description (pad type) parameters

7.2 Pin assignments – APQ8096 bottom

The APQ8096 uses the 994B MNSP package; its bottom surface is equivalent to the 994 NSP.
See Section 7.4 for information about the top pin assignments. A high-level view of the bottom pin assignments is shown in Figure 5

. The pins are colour coded to indicate which function type they support, as defined in Figure 4.

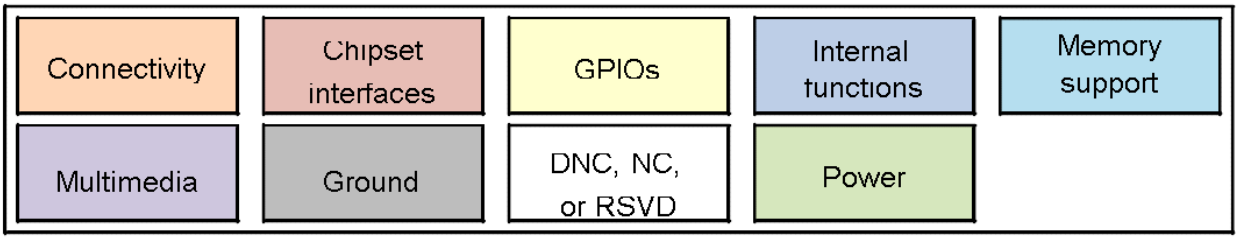


Figure 4 APQ8096 bottom pin assignments – legend

The text within Figure 5 is difficult to read when viewing an 8½" × 11" hard copy. Other viewing options are available

- Print that one page on an 11" × 17" sheet.
- View the graphic soft copy and zoom in – the resolution is sufficient for comfortable reading.

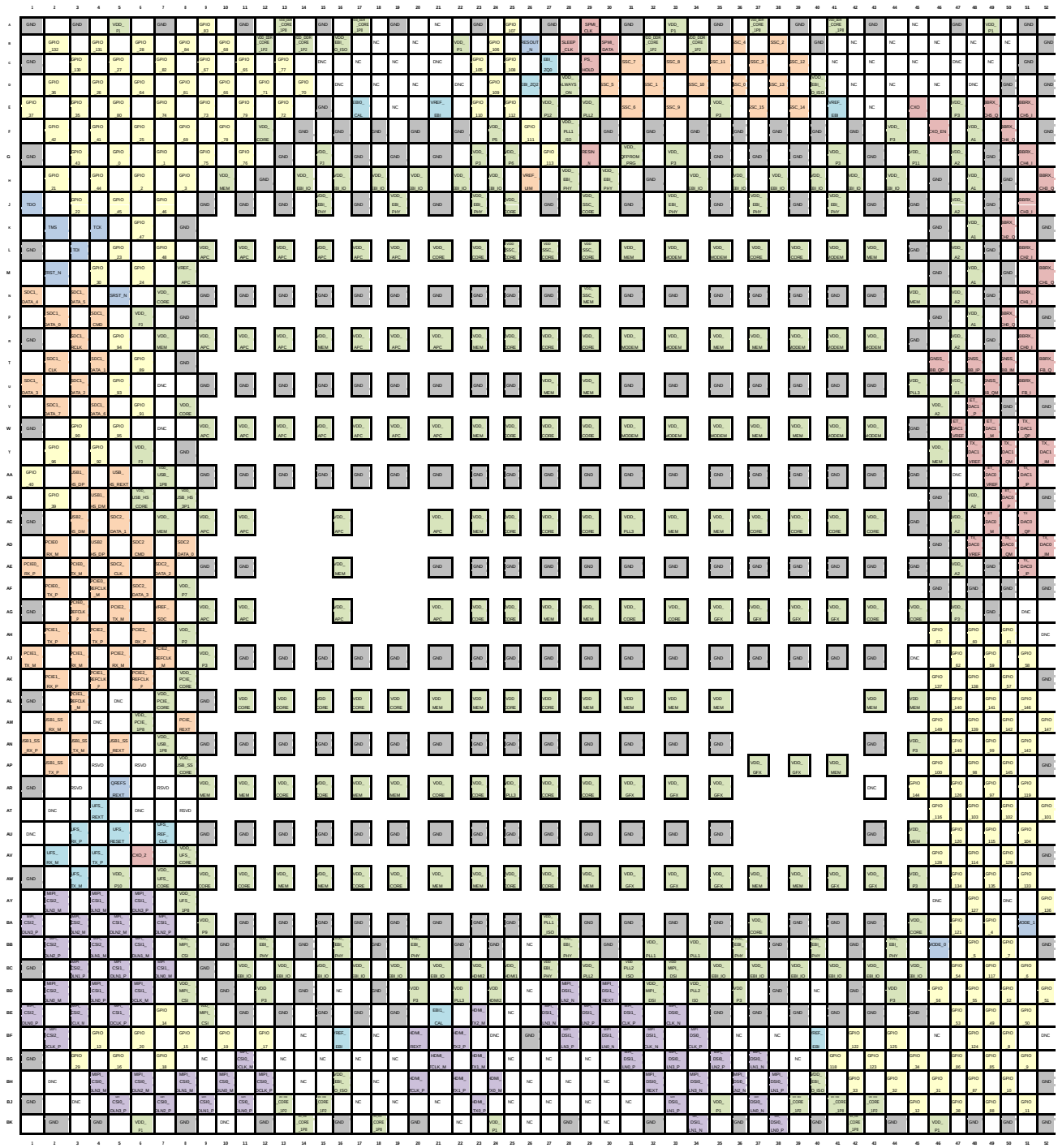


Figure 5 High-level view of APQ8096 bottom pin assignments (from above, through the package)

7.3 Pin descriptions – APQ8096 bottom

Descriptions of bottom pins are presented in the following tables, organized by functional group:

Table 9 Pin descriptions – memory support functions
Table 10 Pin descriptions – multimedia functions
Table 11 Pin descriptions – connectivity functions
Table 13 Pin descriptions – internal functions
Table 16 Pin descriptions – chipset interface functions
Table 17 Pin descriptions – RF front-end functions
Table 18 Pin descriptions – general-purpose input/output ports

Table 19 Pin descriptions – no connection, do not connect, and reserved pins

Table 20 Pin descriptions – power supply pins
Table 21 Pin descriptions – ground pins

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AK50	FORCED_USB_BOOT	GPIO_57	P3	DI B-PD:nppukp	Forced USB boot Configurable I/O
AT52	WDOG_DISABLE	GPIO_101	P3	DI B-PD:nppukp	Watchdog disable Configurable I/O
AT50	BOOT_CONFIG_1	GPIO_102	P3	DI B-PD:nppukp	fast_boot_select bit 0 (configure external boot device) Configurable I/O
AT48	BOOT_CONFIG_2	GPIO_103	P3	DI B-PD:nppukp	fast_boot_select bit 1 (configure external boot device) Configurable I/O
AU51	BOOT_CONFIG_3	GPIO_104	P3	DI B-PD:nppukp	fast_boot_select bit 2 (configure external boot device) Configurable I/O
AV48	BOOT_CONFIG_4	GPIO_114	P3	DI B-PD:nppukp	fast_boot_select bit 3 (configure external boot device) Configurable I/O

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AB2	ALL_USE_SERIAL_NUM	GPIO_39	P3	DI B-PD:nppukp	Selects the serial number Configurable I/O
V6	MSA_PK_HASH_IN_FUSE	GPIO_91	P3	DI B-PD:nppukp	Public key hash from fuses for MSA boot segment selected Configurable I/O
Y4	MSA_AUTH_EN	GPIO_92	P3	DI B-PD:nppukp	Selects authentication enable for MSA segments Configurable I/O
U5	AP_PK_HASH_IN_FUSE	GPIO_93	P3	DI B-PD:nppukp	Public key hash from fuse for applications boot segment selected Configurable I/O
Y2	AP_AUTH_EN	GPIO_96	P3	DI B-PD:nppukp	Selects authentication enable for applications segments Configurable I/O
AN49	FORCE_MSA_AUTH_EN	GPIO_99	P3	DI B-PD:nppukp	Force authentication enable for MSA segments Configurable I/O

1. See Table 7 for parameter and acronym definitions
2. The boot configuration function of the above GPIOs is sampled at the rising edge of RESOUT_N deassertion

Table 8 Boot configuration GPIOs

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
EBI					
E17	EBI0_CAL	–	–	AI	EBI0 LPDDR4 calibration resistor
BE21	EBI1_CAL	–	–	AI	EBI1 LPDDR4 calibration resistor
E21,E41, BF16, BF40	VREF_EBI	–	–	AI	EBI LPDDR4 DQ and CA reference voltage

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
C27	EBI_ZQ0	–	–	AI	EBI LPDDR4 ZQ resistor for lower x16 memory
D26	EBI_ZQ2	–	–	AI	EBI LPDDR4 ZQ resistor for upper x16 memory
Universal flash storage (UFS) interface – supports high-density storage					
AU3	UFS_RX_P	–	–	AI	UFS receive – plus
AV2	UFS_RX_M	–	–	AI	UFS receive – minus
AV4	UFS_TX_P	–	–	AO	UFS transmit – plus
AW3	UFS_TX_M	–	–	AO	UFS transmit – minus
AU7	UFS_REF_CLK	–	P10	DOZ-PD:nppukp	UFS reference clock
AU5	UFS_RESET	–	P10	DOZ-PD:nppukp	UFS reset
AT4	UFS_REXT	–	–	AI, AO	UFS external resistor
SDC1 is available for eMMC NAND flash – see Table 11					

1. See Table 7 for parameter and acronym definitions

Table 9 Pin descriptions – memory support functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
1 of 3 camera serial interfaces – MIPI_CSI0 – 4-lane differential (plus clock) or 3-lane trio					
BH12	MIPI_CSI0_DCLK_P	DNC	CSI –	AI –	MIPI CSI 0, differential clock – plus Do not connect when CSI0 is configured for CPHY
BG11	MIPI_CSI0_DCLK_M	MIPI_CSI0_TLN0_A	CSI CSI	AI AI, AO	MIPI CSI 0, differential clock – minus MIPI CSI 0, trio lane 0 – A
BJ11	MIPI_CSI0_DLN0_P	MIPI_CSI0_TLN0_B	CSI CSI	AI, AO AI, AO	MIPI CSI 0, differential lane 0 – plus MIPI CSI 0, trio lane 0 – B
BH10	MIPI_CSI0_DLN0_M	MIPI_CSI0_TLN0_C	CSI CSI	AI, AO AI, AO	MIPI CSI 0, differential lane 0 – minus MIPI CSI 0, trio lane 0 – C
BJ9	MIPI_CSI0_DLN1_P	MIPI_CSI0_TLN1_A	CSI CSI	AI, AO AI, AO	MIPI CSI 0, differential lane 1 – plus MIPI CSI 0, trio lane 1 – A
BH8	MIPI_CSI0_DLN1_M	MIPI_CSI0_TLN1_B	CSI	AI, AO	MIPI CSI 0, differential lane 1 – minus

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
			CSI	AI, AO	MIPI CSI 0, trio lane 1 – B
BJ7	MIPI_CSI0_DLN2_P	MIPI_CSI0_TLN1_C	CSI CSI	AI, AO AI, AO	MIPI CSI 0, differential lane 2 – plus MIPI CSI 0, trio lane 1 – C
BH6	MIPI_CSI0_DLN2_M	MIPI_CSI0_TLN2_A	CSI CSI	AI, AO AI, AO	MIPI CSI 0, differential lane 2 – minus MIPI CSI 0, trio lane 2 – A
BJ5	MIPI_CSI0_DLN3_P	MIPI_CSI0_TLN2_B	CSI CSI	AI, AO AI, AO	MIPI CSI 0, differential lane 3 – plus MIPI CSI 0, trio lane 2 – B
BH4	MIPI_CSI0_DLN3_M	MIPI_CSI0_TLN2_C	CSI CSI	AI, AO AI, AO	MIPI CSI 0, differential lane 3 – minus MIPI CSI 0, trio lane 2 – C
2 of 3 camera serial interfaces – MIPI_CSI1 – 4-lane differential (plus clock) or 3-lane trio					
BE5	MIPI_CSI1_DCLK_P	DNC	CSI –	AI –	MIPI CSI 1, differential clock – plus Do not connect when CSI1 is configured for CPHY
BD6	MIPI_CSI1_DCLK_M	MIPI_CSI1_TLN0_A	CSI CSI	AI AI, AO	MIPI CSI 1, differential clock – minus MIPI CSI 1, trio lane 0 – A
BD4	MIPI_CSI1_DLN0_P	MIPI_CSI1_TLN0_B	CSI CSI	AI, AO AI, AO	MIPI CSI 1, differential lane 0 – plus MIPI CSI 1, trio lane 0 – B
BC7	MIPI_CSI1_DLN0_M	MIPI_CSI1_TLN0_C	CSI CSI	AI, AO AI, AO	MIPI CSI 1, differential lane 0 – minus MIPI CSI 1, trio lane 0 – C
BC5	MIPI_CSI1_DLN1_P	MIPI_CSI1_TLN1_A	CSI CSI	AI, AO AI, AO	MIPI CSI 1, differential lane 1 – plus MIPI CSI 1, trio lane 1 – A
BB6	MIPI_CSI1_DLN1_M	MIPI_CSI1_TLN1_B	CSI CSI	AI, AO AI, AO	MIPI CSI 1, differential lane 1 – minus MIPI CSI 1, trio lane 1 – B
BA7	MIPI_CSI1_DLN2_P	MIPI_CSI1_TLN1_C	CSI CSI	AI, AO AI, AO	MIPI CSI 1, differential lane 2 – plus MIPI CSI 1, trio lane 1 – C
BA5	MIPI_CSI1_DLN2_M	MIPI_CSI1_TLN2_A	CSI CSI	AI, AO AI, AO	MIPI CSI 1, differential lane 2 – minus MIPI CSI 1, trio lane 2 – A
AY6	MIPI_CSI1_DLN3_P	MIPI_CSI1_TLN2_B	CSI CSI	AI, AO AI, AO	MIPI CSI 1, differential lane 3 – plus MIPI CSI 1, trio lane 2 – B
AY4	MIPI_CSI1_DLN3_M	MIPI_CSI1_TLN2_C	CSI CSI	AI, AO AI, AO	MIPI CSI 1, differential lane 3 – minus MIPI CSI 1, trio lane 2 – C
3 of 3 camera serial interfaces – MIPI_CSI2 – 4-lane differential (plus clock) or 3-lane trio					
BF2	MIPI_CSI2_DCLK_P	DNC	CSI –	AI –	MIPI CSI 2, differential clock – plus Do not connect when CSI2 is configured for CPHY
BE3	MIPI_CSI2_DCLK_M	MIPI_CSI2_TLN0_A	CSI CSI	AI AI,AO	MIPI CSI 2, differential clock – minus MIPI CSI 2, trio lane 0 – A
BE1	MIPI_CSI2_DLN0_P	MIPI_CSI2_TLN0_B	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 0 – plus MIPI CSI 2, trio lane 0 – B
BD2	MIPI_CSI2_DLN0_M	MIPI_CSI2_TLN0_C	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 0 – minus MIPI CSI 2, trio lane 0 – C

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
BC3	MIPI_CSI2_DLN1_P	MIPI_CSI2_TLN1_A	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 1 – plus MIPI CSI 2, trio lane 1 – A
BB4	MIPI_CSI2_DLN1_M	MIPI_CSI2_TLN1_B	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 1 – minus MIPI CSI 2, trio lane 1 – B
BB2	MIPI_CSI2_DLN2_P	MIPI_CSI2_TLN1_C	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 2 – plus MIPI CSI 2, trio lane 1 – C
BA3	MIPI_CSI2_DLN2_M	MIPI_CSI2_TLN2_A	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 2 – minus MIPI CSI 2, trio lane 2 – A
BA1	MIPI_CSI2_DLN3_P	MIPI_CSI2_TLN2_B	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 3 – plus MIPI CSI 2, trio lane 2 – B
AY2	MIPI_CSI2_DLN3_M	MIPI_CSI2_TLN2_C	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 3 – minus MIPI CSI 2, trio lane 2 – C
Camera-related timing and CCI signals					
BF4	CAM_MCLK0	GPIO_13	P3	DO B-PD:nppukp	Camera master clock 0 Configurable I/O
BE7	CAM_MCLK1	GPIO_14	P3	DO B-PD:nppukp	Camera master clock 1 Configurable I/O
BF8	CAM_MCLK2	GPIO_15	P3	DO B-PD:nppukp	Camera master clock 2 Configurable I/O
BG5	CAM_MCLK3	GPIO_16	P3	DO B-PD:nppukp	Camera master clock 3 Configurable I/O
BF12	CCI_I2C0_SDA	GPIO_17	P3	B B-PD:nppukp	Dedicated camera control interface I2C 0 serial data Configurable I/O
BG7	CCI_I2C0_SCL	GPIO_18	P3	B B-PD:nppukp	Dedicated camera control interface I2C 0 clock Configurable I/O
BF10	CCI_I2C1_SDA	GPIO_19	P3	B B-PD:nppukp	Dedicated camera control interface I2C 1 serial data Configurable I/O
BF6	CCI_I2C1_SCL	GPIO_20	P3	B B-PD:nppukp	Dedicated camera control interface I2C 1 clock Configurable I/O
H2	CCI_TIMER0	GPIO_21	P3	DO B-PD:nppukp	Camera control interface timer 0 Configurable I/O
J3	CCI_TIMER1	GPIO_22	P3	DO B-PD:nppukp	Camera control interface timer 1 Configurable I/O
L5	CCI_TIMER2	GPIO_23	P3	DO B-PD:nppukp	Camera control interface timer 2 Configurable I/O
M6	CCI_TIMER3	GPIO_24	P3	DO B-PD:nppukp	Camera control interface timer 3 Configurable I/O
3 of 3 camera serial interfaces – MIPI_CSI2 – 4-lane differential (plus clock) or 3-lane trio					

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
BF2	MIPI_CSI2_DCLK_P	DNC	CSI –	AI –	MIPI CSI 2, differential clock – plus Do not connect when CSI2 is configured for CPHY
BE3	MIPI_CSI2_DCLK_M	MIPI_CSI2_TLN0_A	CSI CSI	AI AI, AO	MIPI CSI 2, differential clock – minus MIPI CSI 2, trio lane 0 – A
BE1	MIPI_CSI2_DLN0_P	MIPI_CSI2_TLN0_B	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 0 – plus MIPI CSI 2, trio lane 0 – B
BD2	MIPI_CSI2_DLN0_M	MIPI_CSI2_TLN0_C	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 0 – minus MIPI CSI 2, trio lane 0 – C
BC3	MIPI_CSI2_DLN1_P	MIPI_CSI2_TLN1_A	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 1 – plus MIPI CSI 2, trio lane 1 – A
BB4	MIPI_CSI2_DLN1_M	MIPI_CSI2_TLN1_B	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 1 – minus MIPI CSI 2, trio lane 1 – B
BB2	MIPI_CSI2_DLN2_P	MIPI_CSI2_TLN1_C	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 2 – plus MIPI CSI 2, trio lane 1 – C
BA3	MIPI_CSI2_DLN2_M	MIPI_CSI2_TLN2_A	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 2 – minus MIPI CSI 2, trio lane 2 – A
BA1	MIPI_CSI2_DLN3_P	MIPI_CSI2_TLN2_B	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 3 – plus MIPI CSI 2, trio lane 2 – B
AY2	MIPI_CSI2_DLN3_M	MIPI_CSI2_TLN2_C	CSI CSI	AI, AO AI, AO	MIPI CSI 2, differential lane 3 – minus MIPI CSI 2, trio lane 2 – C
Camera-related timing and CCI signals					
BF4	CAM_MCLK0	GPIO_13	P3	DO B-PD:nppukp	Camera master clock 0 Configurable I/O
BE7	CAM_MCLK1	GPIO_14	P3	DO B-PD:nppukp	Camera master clock 1 Configurable I/O
BF8	CAM_MCLK2	GPIO_15	P3	DO B-PD:nppukp	Camera master clock 2 Configurable I/O
BG5	CAM_MCLK3	GPIO_16	P3	DO B-PD:nppukp	Camera master clock 3 Configurable I/O
BF12	CCI_I2C0_SDA	GPIO_17	P3	B B-PD:nppukp	Dedicated camera control interface I2C 0 serial data Configurable I/O
BG7	CCI_I2C0_SCL	GPIO_18	P3	B B-PD:nppukp	Dedicated camera control interface I2C 0 clock Configurable I/O
BF10	CCI_I2C1_SDA	GPIO_19	P3	B B-PD:nppukp	Dedicated camera control interface I2C 1 serial data Configurable I/O
BF6	CCI_I2C1_SCL	GPIO_20	P3	B B-PD:nppukp	Dedicated camera control interface I2C 1 clock Configurable I/O
H2	CCI_TIMER0	GPIO_21	P3	DO B-PD:nppukp	Camera control interface timer 0 Configurable I/O

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
J3	CCI_TIMER1	GPIO_22	P3	DO B-PD:nppukp	Camera control interface timer 1 Configurable I/O
L5	CCI_TIMER2	GPIO_23	P3	DO B-PD:nppukp	Camera control interface timer 2 Configurable I/O
M6	CCI_TIMER3	GPIO_24	P3	DO B-PD:nppukp	Camera control interface timer 3 Configurable I/O
F6	CCI_TIMER4	GPIO_25	P3	DO B-PD:nppukp	Camera control interface timer 4 Configurable I/O
D4	CCI_ASYNC0	GPIO_26	P3	DI B-PD:nppukp	Camera control interface async 0 Configurable I/O
M6	CCI_ASYNC1	GPIO_24	P3	DI B-PD:nppukp	Camera control interface async 1 Configurable I/O
F6	CCI_ASYNC2	GPIO_25	P3	DI B-PD:nppukp	Camera control interface async 2 Configurable I/O
Mobile display processor (MDP) vertical sync					
BH50	MDP_VSYNC_P	GPIO_10	P3	DI B-PD:nppukp	MDP vertical sync – primary Configurable I/O
AR49	MDP_VSYNC_P_B	GPIO_97	P3	DI B-PD:nppukp	MDP vertical sync – primary B Configurable I/O
BJ51	MDP_VSYNC_S	GPIO_11	P3	DI B-PD:nppukp	MDP vertical sync – secondary Configurable I/O
AP48	MDP_VSYNC_S_B	GPIO_98	P3	DI B-PD:nppukp	MDP vertical sync – secondary B Configurable I/O
BJ45	MDP_VSYNC_E	GPIO_12	P3	DI B-PD:nppukp	MDP vertical sync – external Configurable I/O
1 of 2 display serial interfaces – 4-lane MIPI_DSI0					
BF34	MIPI_DSI0_CLK_P	–	DSI	AO	MIPI display serial interface 0 clock – positive
BE33	MIPI_DSI0_CLK_N	–	DSI	AO	MIPI display serial interface 0 clock – negative
BG33	MIPI_DSI0_LN3_P	–	DSI	AI, AO	MIPI display serial interface 0 lane 3 – positive
BH34	MIPI_DSI0_LN3_N	–	DSI	AI, AO	MIPI display serial interface 0 lane 3 – negative
BG35	MIPI_DSI0_LN2_P	–	DSI	AI, AO	MIPI display serial interface 0 lane 2 – positive
BH36	MIPI_DSI0_LN2_N	–	DSI	AI, AO	MIPI display serial interface 0 lane 2 – negative
BH38	MIPI_DSI0_LN1_P	–	DSI	AI, AO	MIPI display serial interface 0 lane 1 – positive
BG37	MIPI_DSI0_LN1_N	–	DSI	AI, AO	MIPI display serial interface 0 lane 1 – negative
BK38	MIPI_DSI0_LN0_P	–	DSI	AI, AO	MIPI display serial interface 0 lane 0 – positive

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
BJ37	MIPI_DSI0_LN0_N	–	DSI	AI, AO	MIPI display serial interface 0 lane 0 – negative
BH32	MIPI_DSI0_REXT	–	DSI	AI, AO	MIPI DSI1 external calibration resistor
2 of 2 display serial interfaces – 4-lane MIPI_DSI1					
BE31	MIPI_DSI1_CLK_P	–	DSI	AO	MIPI display serial interface 1 clock – positive
BF32	MIPI_DSI1_CLK_N	–	DSI	AO	MIPI display serial interface 1 clock – negative
BF28	MIPI_DSI1_LN3_P	–	DSI	AI, AO	MIPI display serial interface 1 lane 3 – positive
BE27	MIPI_DSI1_LN3_N	–	DSI	AI, AO	MIPI display serial interface 1 lane 3 – negative
BE29	MIPI_DSI1_LN2_P	–	DSI	AI, AO	MIPI display serial interface 1 lane 2 – positive
BD28	MIPI_DSI1_LN2_N	–	DSI	AI, AO	MIPI display serial interface 1 lane 2 – negative
BJ33	MIPI_DSI1_LN1_P	–	DSI	AI, AO	MIPI display serial interface 1 lane 1 – positive
BK34	MIPI_DSI1_LN1_N	–	DSI	AI, AO	MIPI display serial interface 1 lane 1 – negative
BG31	MIPI_DSI1_LN0_P	–	DSI	AI, AO	MIPI display serial interface 1 lane 0 – positive
BF30	MIPI_DSI1_LN0_N	–	DSI	AI, AO	MIPI display serial interface 1 lane 0 – negative
BD30	MIPI_DSI1_REXT	–	DSI	AI, AO	MIPI DSI0 external calibration resistor
High-definition multimedia interface (HDMI)					
BH20	HDMI_TCLK_P	–	–	AO	HDMI differential clock – plus
BG21	HDMI_TCLK_M	–	–	AO	HDMI differential clock – minus
BF22	HDMI_TX2_P	–	–	AO	HDMI differential transmit 2 – plus
BE23	HDMI_TX2_M	–	–	AO	HDMI differential transmit 2 – minus
BH22	HDMI_TX1_P	–	–	AO	HDMI differential transmit 1 – plus
BG23	HDMI_TX1_M	–	–	AO	HDMI differential transmit 1 – minus
BJ23	HDMI_TX0_P	–	–	AO	HDMI differential transmit 0 – plus
BH24	HDMI_TX0_M	–	–	AO	HDMI differential transmit 0 – minus
BF20	HDMI_REXT	–	–	AI, AO	HDMI external calibration resistor
BH46	HDMI_CEC	GPIO_31	P3	B B-PU:nppdkp	HDMI consumer electronics control Configurable I/O
BH44	HDMI_DDC_CLK	GPIO_32	P3	B B-PU:nppdkp	HDMI display data channel – clock Configurable I/O
BH42	HDMI_DDC_DATA	GPIO_33	P3	B B-PU:nppdkp	HDMI display data channel – data Configurable I/O
BG45	HDMI_HOT_PLUG_DET	GPIO_34	P3	DI B-PD:nppukp	HDMI hot plug detect Configurable I/O
M4	HDMI_RCV_DET	GPIO_30	P3	DO B-PD:nppukp	HDMI receive detection Configurable I/O
Also see Table 11 for connectivity ports that are used for multimedia applications: Audio – SLIMbus, I2S, MI2S, PCM; DMB – TSIF, SDC;					

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
controls – I2C, SPI					

1. See Table 7 for parameter and acronym definitions

Table 10 Pin descriptions – multimedia functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics[1]		Functional description
			Voltage	Type	
Super-speed USB 3.0 (USB_SS)					
AN1	USB1_SS_RX_P	–	–	AI	USB super-speed receive – plus
AM2	USB1_SS_RX_M	–	–	AI	USB super-speed receive – minus
AP2	USB1_SS_TX_P	–	–	AO	USB super-speed transmit – plus
AN3	USB1_SS_TX_M	–	–	AO	USB super-speed transmit – minus
AN5	USB1_SS_REXT	–	–	AI, AO	USB super-speed – external resistor
1 of 2 high-speed USB 2.0 (USB1_HS)					
AA3	USB1_HS_DP	–	–	AI, AO	USB high-speed 1 data – plus
AB4	USB1_HS_DM	–	–	AI, AO	USB high-speed 1 data – minus
AA5	USB_HS_REXT	–	–	AI	USB high-speed data – external resistor
2 of 2 high-speed USB 2.0 (USB2_HS)					
AD4	USB2_HS_DP	–	–	AI, AO	USB high-speed 2 data – plus
AC3	USB2_HS_DM	–	–	AI, AO	USB high-speed 2 data – minus
Secure digital controller interfaces – common to all					
AG7	VREF_SDC	–	–	AI	Reference for SDC I/O pads
Secure digital controller 1 (SDC1) interface – supports eMMC NAND					
V2	SDC1_DATA_7	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 7
V4	SDC1_DATA_6	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 6
N3	SDC1_DATA_5	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 5
N1	SDC1_DATA_4	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 4
U1	SDC1_DATA_3	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 3
U3	SDC1_DATA_2	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 2
T4	SDC1_DATA_1	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 1
P2	SDC1_DATA_0	–	P7	B-PD:nppukp	Secure digital controller 1 data bit 0
P4	SDC1_CMD	–	P7	B-PD:nppukp	Secure digital controller 1 command
T2	SDC1_CLK	–	P7	B-NP:pdpukp	Secure digital controller 1 clock
R3	SDC1_RCLK	–	P7	DI-PD:nppukp	Secure digital controller 1 return clock.
Secure digital controller 2 (SDC2) interface – supports dual-voltage SD 3.0					
AF6	SDC2_DATA_3	QDSS_SDC2_TRDATA_3	P2	BH-PD:nppukp DO	Secure digital controller 2 data bit 3 QDSS trace data bit 3 over SDC2
AE7	SDC2_DATA_2	QDSS_SDC2_TRDATA_2	P2	BH-PD:nppukp	Secure digital controller 2 data bit 2

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics[1]		Functional description
			Voltage	Type	
				DO	QDSS trace data bit 2 over SDC2
AC5	SDC2_DATA_1	QDSS_SDC2_TRDATA_1	P2	BH-PD:nppukp DO	Secure digital controller 2 data bit 1 QDSS trace data bit 1 over SDC2
AD8	SDC2_DATA_0	QDSS_SDC2_TRDATA_0	P2	BH-PD:nppukp DO	Secure digital controller 2 data bit 0 QDSS trace data bit 0 over SDC2
AD6	SDC2_CMD	QDSS_SDC2_TRSYNC	P2	BH-PD:nppukp DO	Secure digital controller 2 command QDSS trace sync over SDC2
AE5	SDC2_CLK	QDSS_SDC2_TRCLK	P2	BH-NP:pdpukp DO	Secure digital controller 2 clock QDSS trace clock over SDC2
AA1	SD_WRITE_PROTECT	GPIO_40	P3	DI B-PD:nppukp	Secure digital card write protection Configurable I/O
APQ8096 does not include a secure digital controller 3 (SDC3) interface					
Secure digital controller 4 (SDC4) interface – supports SDIO					
Y4	SDC4_DATA_3	GPIO_92	P3	B B-PD:nppukp	Secure digital controller 4 data bit 3 Configurable I/O
R5	SDC4_DATA_2	GPIO_94	P3	B B-PD:nppukp	Secure digital controller 4 data bit 2 Configurable I/O
W5	SDC4_DATA_1	GPIO_95	P3	B B-PD:nppukp	Secure digital controller 4 data bit 1 Configurable I/O
Y2	SDC4_DATA_0	GPIO_96	P3	B B-PD:nppukp	Secure digital controller 4 data bit 0 Configurable I/O
V6	SDC4_CMD	GPIO_91	P3	B B-PD:nppukp	Secure digital controller 4 command Configurable I/O
U5	SDC4_CLK	GPIO_93	P3	DO B-PD:nppukp	Secure digital controller 4 clock Configurable I/O
Peripheral component interconnect express 0 (PCIe0) interface					
AE1	PCIE0_RX_P	–	–	AI	PCIe 0 receive – plus
AD2	PCIE0_RX_M	–	–	AI	PCIe 0 receive – minus
AF2	PCIE0_TX_P	–	–	AO	PCIe 0 transmit – plus
AE3	PCIE0_TX_M	–	–	AO	PCIe 0 transmit – minus
AG3	PCIE0_REF_CLK_P	–	–	AO	PCIe 0 reference clock – plus
AF4	PCIE0_REF_CLK_M	–	–	AO	PCIe 0 reference clock – minus
AM8	PCIE_REXT	–	–	AI, AO	PCIe external resistor
D2	PCIE0_CLKREQ_N	GPIO_36	P3	DI B-PU:nppdkp	PCIe 0 clock request Configurable I/O
E3	PCIE0_RST_N	GPIO_35	P3	DO B-PD:nppukp	PCIe 0 reset Configurable I/O
Peripheral component interconnect express 1 (PCIe1) interface					
AK2	PCIE1_RX_P	–	–	AI	PCIe 1 receive – plus
AJ3	PCIE1_RX_M	–	–	AI	PCIe 1 receive – minus
AH2	PCIE1_TX_P	–	–	AO	PCIe 1 transmit – plus
AJ1	PCIE1_TX_M	–	–	AO	PCIe 1 transmit – minus
AK4	PCIE1_REF_CLK_P	–	–	AO	PCIe 1 reference clock – plus
AL3	PCIE1_REF_CLK_M	–	–	AO	PCIe 1 reference clock – minus
B4	PCIE1_CLKREQ_N	GPIO_131	P3	DI B-PU:nppdkp	PCIe 1 clock request Configurable I/O

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics[1]		Functional description
			Voltage	Type	
C3	PCIE1_RST_N	GPIO_130	P3	DO B-PD:nppukp	PCIe 1 reset Configurable I/O
Peripheral component interconnect express 2 (PCIe2) interface					
AH6	PCIE2_RX_P	–	–	AI	PCIe 2 receive – plus
AJ5	PCIE2_RX_M	–	–	AI	PCIe 2 receive – minus
AH4	PCIE2_TX_P	–	–	AO	PCIe 2 transmit – plus
AG5	PCIE2_TX_M	–	–	AO	PCIe 2 transmit – minus
AK6	PCIE2_REF_CLK_P	–	–	AO	PCIe 2 reference clock – plus
AJ7	PCIE2_REF_CLK_M	–	–	AO	PCIe 2 reference clock – minus
AU49	PCIE2_CLKREQ_N	GPIO_115	P3	DI B-PU:nppdkp	PCIe 2 clock request Configurable I/O
AV48	PCIE2_RST_N	GPIO_114	P3	DO B-PD:nppukp	PCIe 2 reset Configurable I/O
Snapdragon sensor core (SSC) pins					
E37	SSC_15	SSC_UART_2_RX SSC_SPI_3_MISO	P12	B-PD:nppukp	Snapdragon sensor core bit 15 SSC UART #2 Receive SSC SPI #3 data master in/slave out
E39	SSC_14	SSC_UART_2_TX SSC_SPI_3_MOSI	P12	B-PD:nppukp	Snapdragon sensor core bit 14 SSC UART #2 transmit SSC SPI #3 data master out/slave in
D38	SSC_13	SSC_UART_1_RX SSC_SPI_3_CS_N	P12	B-PD:nppukp	Snapdragon sensor core bit 13 SSC UART #1 receive SSC SPI #3 chip select
C39	SSC_12	SSC_UART_1_TX SSC_SPI_3_CLK	P12	B-PD:nppukp	Snapdragon sensor core bit 12 SSC UART #1 transmit SSC SPI #3 clock
C35	SSC_11	SSC_SPI_1_MISO	P12	B-PD:nppukp	Snapdragon sensor core bit 11 SSC SPI #1 data master in/slave out
D34	SSC_10	SSC_SPI_1_MOSI	P12	B-PD:nppukp	Snapdragon sensor core bit 10 SSC SPI #1 data master out/slave in
E33	SSC_9	SSC_SPI_1_CLK SSC_I2C_1_SCL	P12	B-PD:nppukp	Snapdragon sensor core bit 9 SSC SPI #1 clock SSC I2C #1 serial clock
C33	SSC_8	SSC_SPI_1_CS_N SSC_I2C_1_SDA	P12	B-PD:nppukp	Snapdragon sensor core bit 8 SSC SPI #1 chip select 1 SSC I2C #1 serial data
C31	SSC_7	SSC_UART_3_RX SSC_SPI_2_MISO	P12	B-PD:nppukp	Snapdragon sensor core bit 7 SSC UART #3 Receive SSC SPI #2 data master in/slave out
E31	SSC_6	SSC_UART_3_TX SSC_SPI_2_MOSI	P12	B-PD:nppukp	Snapdragon sensor core bit 6 SSC UART #3 transmit SSC SPI #2 data master out/slave in
D30	SSC_5	SSC_I2C_2_SCL SSC_SPI_2_CLK	P12	B-PD:nppukp	Snapdragon sensor core bit 5 SSC I2C #2 serial clock SSC SPI #2 clock
B36	SSC_4	SSC_I2C_2_SDA	P12	B-PD:nppukp	Snapdragon sensor core bit 4

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics[1]		Functional description
			Voltage	Type	
		SSC_SPI_2_CS_N			SSC I2C #2 serial data SSC SPI #2 chip select
C37	SSC_3	SSC_I2C_3_SCL	P12	B-PD:nppukp	Snapdragon sensor core bit 3 SSC I2C #3 serial clock
B38	SSC_2	SSC_I2C_3_SDA	P12	B-PD:nppukp	Snapdragon sensor core bit 2 SSC I2C #3 serial data
D32	SSC_1	–	P12	B-PD:nppukp	Snapdragon sensor core bit 1 SSC power enable
D36	SSC_0	SSC_SPI_1_CS1_N SYNC_OUT	P12	B-PD:nppukp	Snapdragon sensor core bit 0 SSC SPI #1 chip select 2 Sync signal for sensors
Transport stream interface 1 (TSIF1)					
V6	TSIF1_DATA	GPIO_91	P3	DI B-PD:nppukp	Transport stream interface 1 data Configurable I/O
T6	TSIF1_CLK	GPIO_89	P3	DI B-PD:nppukp	Transport stream interface 1 clock Configurable I/O
AA1	TSIF1_ERROR	GPIO_40	P3	DI B-PD:nppukp	Transport stream interface 1 error Configurable I/O
W3	TSIF1_EN	GPIO_90	P3	DI B-PD:nppukp	Transport stream interface 1 enable Configurable I/O
AB2	TSIF1_SYNC	GPIO_39	P3	DI B-PD:nppukp	Transport stream interface 1 sync Configurable I/O
Transport stream interface 2 (TSIF2)					
W5	TSIF2_DATA	GPIO_95	P3	DI B-PD:nppukp	Transport stream interface 2 data Configurable I/O
U5	TSIF2_CLK	GPIO_93	P3	DI B-PD:nppukp	Transport stream interface 2 clock Configurable I/O
Y2	TSIF2_SYNC	GPIO_96	P3	DI B-PD:nppukp	Transport stream interface 2 sync Configurable I/O
R5	TSIF2_EN	GPIO_94	P3	DI B-PD:nppukp	Transport stream interface 2 enable Configurable I/O
Y4	TSIF2_ERROR	GPIO_92	P3	DI B-PD:nppukp	Transport stream interface 2 error Configurable I/O
Audio SLIMbus – low-power audio subsystem					
D14	LPASS_SLIMBUS_CLK	GPIO_70	P3	DO B-PD:nppukp	Low-power audio SLIMbus clock Configurable I/O
E13	LPASS_SLIMBUS_DATA1	GPIO_72	P3	DO B-PD:nppukp	Low-power audio SLIMbus data 1 Configurable I/O
D12	LPASS_SLIMBUS_DATA0	GPIO_71	P3	DO B-PD:nppukp	Low-power audio SLIMbus data 0 Configurable I/O
Audio I2S interface – speaker					
F8	SPKR_I2S_MCLK	GPIO_69	P3	DO B-PD:nppukp	Speaker I2S master clock Configurable I/O
D14	SPKR_I2S_SCK	GPIO_70	P3	B B-PD:nppukp	Speaker I2S bit clock Configurable I/O

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics[1]		Functional description
			Voltage	Type	
D12	SPKR_I2S_DOUT	GPIO_71	P3	DO B-PD:nppukp	Speaker I2S data output Configurable I/O
E13	SPKR_I2S_WS	GPIO_72	P3	B B-PD:nppukp	Speaker I2S word select (L/R) Configurable I/O
Audio MI2S interface #1					
D6	MI2S_1_MCLK	GPIO_64	P3	DO B-PD:nppukp	MI2S #1 master clock Configurable I/O
C11	MI2S_1_SCK	GPIO_65	P3	B B-PD:nppukp	MI2S #1 bit clock Configurable I/O
D10	MI2S_1_WS	GPIO_66	P3	B B-PD:nppukp	MI2S #1 word select (L/R) Configurable I/O
C9	MI2S_1_D0	GPIO_67	P3	B B-PD:nppukp	MI2S #1 serial data channel 0 Configurable I/O
B10	MI2S_1_D1	GPIO_68	P3	B B-PD:nppukp	MI2S #1 serial data channel 1 Configurable I/O
Audio MI2S interface #2					
E11	MI2S_2_MCLK	GPIO_79	P3	DO B-PD:nppukp	MI2S #2 master clock Configurable I/O
E5	MI2S_2_SCK	GPIO_80	P3	B B-PD:nppukp	MI2S #2 bit clock Configurable I/O
D8	MI2S_2_WS	GPIO_81	P3	B B-PD:nppukp	MI2S #2 word select (L/R) Configurable I/O
C7	MI2S_2_D0	GPIO_82	P3	B B-PD:nppukp	MI2S #2 serial data channel 0 Configurable I/O
A9	MI2S_2_D1	GPIO_83	P3	B B-PD:nppukp	MI2S #2 serial data channel 1 Configurable I/O
Audio MI2S interface #3					
E7	MI2S_3_MCLK	GPIO_74	P3	DO B-PD:nppukp	MI2S #3 master clock Configurable I/O
G9	MI2S_3_SCK	GPIO_75	P3	B B-PD:nppukp	MI2S #3 bit clock Configurable I/O
G11	MI2S_3_WS	GPIO_76	P3	B B-PD:nppukp	MI2S #3 word select (L/R) Configurable I/O
C13	MI2S_3_D0	GPIO_77	P3	B B-PD:nppukp	MI2S #3 serial data channel 0 Configurable I/O
F10	MI2S_3_D1	GPIO_78	P3	B B-PD:nppukp	MI2S #3 serial data channel 1 Configurable I/O
Audio MI2S interface #4					
AK50	MI2S_4_MCLK	GPIO_57	P3	DO	MI2S #4 master clock

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics[1]		Functional description
			Voltage	Type	
				B-PD:nppukp	Configurable I/O
AJ51	MI2S_4_SCK	GPIO_58	P3	B B-PD:nppukp	MI2S #4 bit clock Configurable I/O
AJ49	MI2S_4_WS	GPIO_59	P3	B B-PD:nppukp	MI2S #4 word select (L/R) Configurable I/O
AH48	MI2S_4_D0	GPIO_60	P3	B B-PD:nppukp	MI2S #4 serial data channel 0 Configurable I/O
AH50	MI2S_4_D1	GPIO_61	P3	B B-PD:nppukp	MI2S #4 serial data channel 1 Configurable I/O
AJ47	MI2S_4_D2	GPIO_62	P3	B B-PD:nppukp	MI2S #4 serial data channel 2 Configurable I/O
AH46	MI2S_4_D3	GPIO_63	P3	B B-PD:nppukp	MI2S #4 serial data channel 3 Configurable I/O
Audio PCM interface #1					
C11	PCM1_CLK	GPIO_65	P3	B B-PD:nppukp	Audio PCM clock (port 1) Configurable I/O
D10	PCM1_SYNC	GPIO_66	P3	B B-PD:nppukp	Audio PCM sync (port 1) Configurable I/O
C9	PCM1_DIN	GPIO_67	P3	B B-PD:nppukp	Audio PCM data input (port 1) Configurable I/O
B11	PCM1_DOUT	GPIO_68	P3	B B-PD:nppukp	Audio PCM data output (port 1) Configurable I/O
Audio PCM interface #2					
E5	PCM2_CLK	GPIO_80	P3	B B-PD:nppukp	Audio PCM clock (port 2) Configurable I/O
D8	PCM2_SYNC	GPIO_81	P3	B B-PD:nppukp	Audio PCM sync (port 2) Configurable I/O
C7	PCM2_DIN	GPIO_82	P3	B B-PD:nppukp	Audio PCM data input (port 2) Configurable I/O
A9	PCM2_DOUT	GPIO_83	P3	B B-PD:nppukp	Audio PCM data output (port 2)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics[1]		Functional description
			Voltage	Type	
					Configurable I/O
Audio PCM interface #3					
G9	PCM3_CLK	GPIO_75	P3	B B-PD:nppukp	Audio PCM clock (port 3) Configurable I/O
G11	PCM3_SYNC	GPIO_76	P3	B B-PD:nppukp	Audio PCM sync (port 3) Configurable I/O
C13	PCM3_DIN	GPIO_77	P3	B B-PD:nppukp	Audio PCM data input (port 3) Configurable I/O
F10	PCM3_DOUT	GPIO_78	P3	B B-PD:nppukp	Audio PCM data output (port 3) Configurable I/O
Audio PCM interface #4					
AJ51	PCM4_CLK	GPIO_58	P3	B B-PD:nppukp	Audio PCM clock (port 4) Configurable I/O
AJ49	PCM4_SYNC	GPIO_59	P3	B B-PD:nppukp	Audio PCM sync (port 4) Configurable I/O
AH48	PCM4_DIN	GPIO_60	P3	B B-PD:nppukp	Audio PCM data input (port 4) Configurable I/O
AH50	PCM4_DOUT	GPIO_61	P3	B B-PD:nppukp	Audio PCM data output (port 4) Configurable I/O
Shared audio clock					
F8	AUDIO_REF_CLK	GPIO_69	P3	B B-PD:nppukp	Audio reference clock Configurable I/O
User interface module 1 (UIM1) interfaces – dual-voltage clock, data, and reset; not multiplexed with any BLSP pins					
D24	UIM1_DATA	GPIO_109	P5	B BH-PD:nppukp	UIM1 data (dual-voltage) Configurable I/O
E25	UIM1_PRESENT	GPIO_112	P3	DI B-PD:nppukp	UIM1 presence detection Configurable I/O
F26	UIM1_RESET	GPIO_111	P5	DO BH-PD:nppukp	UIM1 reset (dual-voltage)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics[1]		Functional description
			Voltage	Type	
					Configurable I/O
E23	UIM1_CLK	GPIO_110	P5	DO BH-PD:nppukp	UIM1 clock (dual-voltage) Configurable I/O
User interface module 2 (UIM2) interfaces – dual-voltage clock, data, and reset; not multiplexed with any BLSP pins					
C23	UIM2_DATA	GPIO_105	P6	B BH-PD:nppukp	UIM2 data (dual-voltage) Configurable I/O
C25	UIM2_PRESENT	GPIO_108	P3	DI B-PD:nppukp	UIM2 presence detection Configurable I/O
A25	UIM2_RESET	GPIO_107	P6	DO BH-PD:nppukp	UIM2 reset (dual-voltage) Configurable I/O
B24	UIM2_CLK	GPIO_106	P6	DO BH-PD:nppukp	UIM2 clock (dual-voltage) Configurable I/O
User interface module 3 (UIM3) interfaces – 1.8 V interface; multiplexed with BLSP9 pins					
BE49	UIM3_DATA	GPIO_49	P3	B B-PD:nppukp	UIM3 data Configurable I/O
BD50	UIM3_PRESENT	GPIO_52	P3	DI B-PD:nppukp	UIM3 presence detection Configurable I/O
BD52	UIM3_RESET	GPIO_51	P3	DO B-PD:nppukp	UIM3 reset Configurable I/O
BE51	UIM3_CLK	GPIO_50	P3	DO B-PD:nppukp	UIM3 clock Configurable I/O
User interface module 4 (UIM4) interfaces – 1.8 V interface; multiplexed with BLSP11 pins					
AJ51	UIM4_DATA	GPIO_58	P3	B B-PD:nppukp	UIM4 data Configurable I/O
AH50	UIM4_PRESENT	GPIO_61	P3	DI B-PD:nppukp	UIM4 presence detection Configurable I/O
AH48	UIM4_RESET	GPIO_60	P3	DO B-PD:nppukp	UIM4 reset Configurable I/O
AJ49	UIM4_CLK	GPIO_59	P3	DO B-PD:nppukp	UIM4 clock Configurable I/O
Shared User interface module (UIM) functions					
H26	VREF_UIM		–	AI	Reference for UIM I/O pads
G27	UIM_BATT_ALARM	GPIO_113	P3	DI B-PD:nppukp	UIM battery alarm Configurable I/O
BAM-based low-speed peripheral interface 1 – see Table 12 for application-specific pin assignments					
G5	BLSP1_3	GPIO_0	P3	B B-PD:nppukp	BLSP #1 bit 3; SPI, UART, or UIM

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics[1]		Functional description
			Voltage	Type	
					Configurable I/O
G7	BLSP1_2	GPIO_1	P3	B B-PD:nppukp	BLSP #1 bit 2; SPI, UART, or UIM Configurable I/O
H6	BLSP1_1	GPIO_2	P3	B B-PD:nppukp	BLSP #1 bit 1; SPI, UART, or I2C Configurable I/O
H8	BLSP1_0	GPIO_3	P3	B B-PD:nppukp	BLSP #1 bit 0; SPI, UART, or I2C Configurable I/O
BAM-based low-speed peripheral interface 2 – see Table 12 for application-specific pin assignments					
F4	BLSP2_3	GPIO_41	P3	B B-PD:nppukp	BLSP #2 bit 3; SPI, UART, or UIM Configurable I/O
F2	BLSP2_2	GPIO_42	P3	B B-PD:nppukp	BLSP #2 bit 2; SPI, UART, or UIM Configurable I/O
G3	BLSP2_1	GPIO_43	P3	B B-PD:nppukp	BLSP #2 bit 1; SPI, UART, or I2C Configurable I/O
H4	BLSP2_0	GPIO_44	P3	B B-PD:nppukp	BLSP #2 bit 0; SPI, UART, or I2C Configurable I/O
BAM-based low-speed peripheral interface 3 – see Table 12 for application-specific pin assignments					
J5	BLSP3_3	GPIO_45	P3	B B-PD:nppukp	BLSP #3 bit 3; SPI, UART, or UIM Configurable I/O
J7	BLSP3_2	GPIO_46	P3	B B-PD:nppukp	BLSP #3 bit 2; SPI, UART, or UIM Configurable I/O
K6	BLSP3_1	GPIO_47	P3	B B-PD:nppukp	BLSP#3 bit 1; SPI, UART, or I2C Configurable I/O
L7	BLSP3_0	GPIO_48	P3	B B-PD:nppukp	BLSP #3 bit 0; SPI, UART, or I2C Configurable I/O
BAM-based low-speed peripheral interface 4 – see Table 12 for application-specific pin assignments					
C11	BLSP4_3	GPIO_65	P3	B B-PD:nppukp	BLSP #4 bit 3; SPI, UART, or UIM Configurable I/O
D10	BLSP4_2	GPIO_66	P3	B B-PD:nppukp	BLSP #4 bit 2; SPI, UART, or UIM

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics[1]		Functional description
			Voltage	Type	
					Configurable I/O
C9	BLSP4_1	GPIO_67	P3	B B-PD:nppukp	BLSP #4 bit 1; SPI, UART, or I2C Configurable I/O
B10	BLSP4_0	GPIO_68	P3	B B-PD:nppukp	BLSP #4 bit 0; SPI, UART, or I2C Configurable I/O
BAM-based low-speed peripheral interface 5 – see Table 12 for application-specific pin assignments					
D8	BLSP5_3	GPIO_81	P3	B B-PD:nppukp	BLSP #5 bit 3; SPI, UART, or UIM Configurable I/O
C7	BLSP5_2	GPIO_82	P3	B B-PD:nppukp	BLSP #5 bit 2; SPI, UART, or UIM Configurable I/O
A9	BLSP5_1	GPIO_83	P3	B B-PD:nppukp	BLSP #5 bit 1; SPI, UART, or I2C Configurable I/O
B8	BLSP5_0	GPIO_84	P3	B B-PD:nppukp	BLSP #5 bit 0; SPI, UART, or I2C Configurable I/O
BAM-based low-speed peripheral interface 6 – see Table 12 for application-specific pin assignments					
F6	BLSP6_3	GPIO_25	P3	B B-PD:nppukp	BLSP #6 bit 3; SPI, UART, or UIM Configurable I/O
D4	BLSP6_2	GPIO_26	P3	B B-PD:nppukp	BLSP #6 bit 2; SPI, UART, or UIM Configurable I/O
C5	BLSP6_1	GPIO_27	P3	B B-PD:nppukp	BLSP #6 bit 1; SPI, UART, or I2C Configurable I/O
B6	BLSP6_0	GPIO_28	P3	B B-PD:nppukp	BLSP #6 bit 0; SPI, UART, or I2C Configurable I/O
BAM-based low-speed peripheral interface 7 – see Table 12 for application-specific pin assignments					
BE47	BLSP7_3	GPIO_53	P3	B B-PD:nppukp	BLSP #7 bit 3; SPI, UART, or UIM Configurable I/O
BC47	BLSP7_2	GPIO_54	P3	B B-PD:nppukp	BLSP #7 bit 2; SPI, UART, or UIM Configurable I/O
BD48	BLSP7_1	GPIO_55	P3	B	BLSP #7 bit 1; SPI,

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics[1]		Functional description
			Voltage	Type	
				B-PD:nppukp	UART, or I2C Configurable I/O
BD46	BLSP7_0	GPIO_56	P3	B B-PD:nppukp	BLSP #7 bit 0; SPI, UART, or I2C Configurable I/O
BAM-based low-speed peripheral interface 8 – see Table 12 for application-specific pin assignments					
BA49	BLSP8_3	GPIO_4	P3	B B-PD:nppukp	BLSP #8 bit 3; SPI, UART, or UIM Configurable I/O
BB48	BLSP8_2	GPIO_5	P3	B B-PD:nppukp	BLSP #8 bit 2; SPI, UART, or UIM Configurable I/O
BC51	BLSP8_1	GPIO_6	P3	B B-PD:nppukp	BLSP #8 bit 1; SPI, UART, or I2C Configurable I/O
BB50	BLSP8_0	GPIO_7	P3	B B-PD:nppukp	BLSP #8 bit 0; SPI, UART, or I2C Configurable I/O
BAM-based low-speed peripheral interface 9 – see Table 12 for application-specific pin assignments					
BE49	BLSP9_3	GPIO_49	P3	B B-PD:nppukp	BLSP #9 bit 3; SPI, UART, or UIM Configurable I/O
BE51	BLSP9_2	GPIO_50	P3	B B-PD:nppukp	BLSP #9 bit 2; SPI, UART, or UIM Configurable I/O
BD52	BLSP9_1	GPIO_51	P3	B B-PD:nppukp	BLSP #9 bit 1; SPI, UART, or I2C Configurable I/O
BD50	BLSP9_0	GPIO_52	P3	B B-PD:nppukp	BLSP #9 bit 0; SPI, UART, or I2C Configurable I/O
BAM-based low-speed peripheral interface 10 – see Table 12 for application-specific pin assignments					
BF50	BLSP10_3	GPIO_8	P3	B B-PD:nppukp	BLSP #10 bit 3; SPI, UART, or UIM Configurable I/O
BG51	BLSP10_2	GPIO_9	P3	B B-PD:nppukp	BLSP #10 bit 2; SPI, UART, or UIM Configurable I/O
BH50	BLSP10_1	GPIO_10	P3	B B-PD:nppukp	BLSP #10 bit 1; SPI, UART, or I2C Configurable I/O

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics[1]		Functional description
			Voltage	Type	
BJ51	BLSP10_0	GPIO_11	P3	B B-PD:nppukp	BLSP #10 bit 0; SPI, UART, or I2C Configurable I/O
BAM-based low-speed peripheral interface 11 – see Table 12 for application-specific pin assignments					
AJ51	BLSP11_3	GPIO_58	P3	B B-PD:nppukp	BLSP #11 bit 3; SPI, UART, or UIM Configurable I/O
AJ49	BLSP11_2	GPIO_59	P3	B B-PD:nppukp	BLSP #11 bit 2; SPI, UART, or UIM Configurable I/O
AH48	BLSP11_1	GPIO_60	P3	B B-PD:nppukp	BLSP #11 bit 1; SPI, UART, or I2C Configurable I/O
AH50	BLSP11_0	GPIO_61	P3	B B-PD:nppukp	BLSP #11 bit 0; SPI, UART, or I2C Configurable I/O
BAM-based low-speed peripheral interface 12 – see Table 12 for application-specific pin assignments					
BG49	BLSP12_3	GPIO_85	P3	B B-PD:nppukp	BLSP #12 bit 3; SPI, UART, or UIM Configurable I/O
BG47	BLSP12_2	GPIO_86	P3	B B-PD:nppukp	BLSP #12 bit 2; SPI, UART, or UIM Configurable I/O
BH48	BLSP12_1	GPIO_87	P3	B B-PD:nppukp	BLSP #12 bit 1; SPI, UART, or I2C Configurable I/O
BJ49	BLSP12_0	GPIO_88	P3	B B-PD:nppukp	BLSP #12 bit 0; SPI, UART, or I2C Configurable I/O
Serial peripheral interface (SPI) extra chip selects (supplements BLSP ports configured for SPI protocol) signals [2]					
W3	BLSP1_SPI_CS1_N	GPIO_90	P3	DO-Z B-PD:nppukp	Chip select 1 for SPI on BLSP #1 Configurable I/O
M6	BLSP1_SPI_CS2A_N	GPIO_24	P3	DO-Z B-PD:nppukp	Chip select 2A for SPI on BLSP #1 Configurable I/O
B6	BLSP1_SPI_CS2B_N	GPIO_28	P3	DO-Z B-PD:nppukp	Chip select 2B for SPI on BLSP #1 Configurable I/O
C5	BLSP1_SPI_CS3A_N	GPIO_27	P3	DO-Z B-PD:nppukp	Chip select 3A for SPI on BLSP #1 Configurable I/O
L5	BLSP1_SPI_CS3B_N	GPIO_23	P3	DO-Z B-PD:nppukp	Chip select 3B for SPI on BLSP #1 Configurable I/O
F6	BLSP2_SPI_CS1_N	GPIO_25	P3	DO-Z B-PD:nppukp	Chip select 1 for SPI on BLSP #2 Configurable I/O
BG3	BLSP2_SPI_CS2_N	GPIO_29	P3	DO-Z	Chip select 2 for SPI on BLSP #2

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics[1]		Functional description
			Voltage	Type	
				B-PD:nppukp	Configurable I/O
M4	BLSP2_SPI_CS3_N	GPIO_30	P3	DO-Z B-PD:nppukp	Chip select 3 for SPI on BLSP #2 Configurable I/O
BD52	BLSP10_SPI_CS1A_N	GPIO_51	P3	DO-Z B-PD:nppukp	Chip select 1A for SPI on BLSP #10 Configurable I/O
BE49	BLSP10_SPI_CS1B_N	GPIO_49	P3	DO-Z B-PD:nppukp	Chip select 1B for SPI on BLSP #10 Configurable I/O
BD50	BLSP10_SPI_CS2A_N	GPIO_52	P3	DO-Z B-PD:nppukp	Chip select 2A for SPI on BLSP #10 Configurable I/O
BE51	BLSP10_SPI_CS2B_N	GPIO_50	P3	DO-Z B-PD:nppukp	Chip select 2B for SPI on BLSP #10 Configurable I/O
BJ49	BLSP10_SPI_CS3_N	GPIO_88	P3	DO-Z B-PD:nppukp	Chip select 3 for SPI on BLSP #10 Configurable I/O

1. See Table 7 for parameter and acronym definitions.
2. GPIO 'A/B' multiplexing is explained in Figure 6

Table 11 Pin descriptions – connectivity functions

NOTE *GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the Table 11), designers must identify all the application related requirements and map each GPIO to its function carefully, to avoid conflicts in GPIO assignments. Please refer to Table 18 for a list of all supported functions for each GPIO.*

Twelve 4-pin sets of GPIOs are available as BAM-based low-speed peripheral (BLSP) interface ports that can be configured for UART, UIM, SPI, or I2C operation. Detailed pin assignments are presented in Table 12 for each configuration.

Option	Configuration	BLSP bit 3	BLSP bit 2	BLSP bit 1	BLSP bit 0
	BLSP1 GPIO pins =	GPIO_0	GPIO_1	GPIO_2	GPIO_3
	BLSP2 GPIO pins =	GPIO_41	GPIO_42	GPIO_43	GPIO_44
	BLSP3 GPIO pins =	GPIO_45	GPIO_46	GPIO_47	GPIO_48
	BLSP4 GPIO pins =	GPIO_65	GPIO_66	GPIO_67	GPIO_68
	BLSP5 GPIO pins =	GPIO_81	GPIO_82	GPIO_83	GPIO_84
	BLSP6 GPIO pins =	GPIO_25	GPIO_26	GPIO_27	GPIO_28
	BLSP7 GPIO pins =	GPIO_53	GPIO_54	GPIO_55	GPIO_56
	BLSP8 GPIO pins =	GPIO_4	GPIO_5	GPIO_6	GPIO_7
	BLSP9 GPIO pins =	GPIO_49	GPIO_50	GPIO_51	GPIO_52
	BLSP10 GPIO pins =	GPIO_8	GPIO_9	GPIO_10	GPIO_11
	BLSP11 GPIO pins =	GPIO_58	GPIO_59	GPIO_60	GPIO_61
	BLSP12 GPIO pins =	GPIO_85	GPIO_86	GPIO_87	GPIO_88
1	4-pin UART	UART_TX DO 4-pin UART transmit data	UART_RX DI 4-pin UART receive data	UART_CTS_N DI 4-pin UART clear-to-send	UART_RFR_N DO 4-pin UART ready-for-receive

Option	Configuration	BLSP bit 3	BLSP bit 2	BLSP bit 1	BLSP bit 0
2	2-pin UART + 2-pin I2C	UART_TX DO 2-pin UART transmit data	UART_RX DI 2-pin UART receive data	I2C_SDA B I2C serial data	I2C_SCL B I2C serial clock
3	4-pin SPI	SPI_DATA_MOSI B	SPI_DATA_MISO B	SPI_CS_N B	SPI_CLK B
		4-pin SPI master out/slave in	4-pin SPI master in/slave out	4-pin SPI chip select	4-pin SPI clock
4	2-pin UIM + 2-pin I2C	UIM_DATA B UIM data	UIM_CLK DO UIM clock	I2C_SDA B I2C serial data	I2C_SCL B I2C serial clock
5	2-pin UIM + 2 GPIOs	UIM_DATA B UIM data	UIM_CLK DO UIM clock	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O
6	2 GPIOs + 2-pin I2C	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O	I2C_SDA B I2C serial data	I2C_SCL B I2C serial clock
7	4 GPIOs	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O
		The three rows within shaded cells are: 1) pad function; 2) pad type; and 3) functional description.			

Table 12 BLSP configurations

As noted throughout these pin definition tables, GPIO assignments must be done carefully to avoid conflicts, and to ensure that the intended functionality is achieved. For GPIOs that can be used as BLSPs, three additional factors should be considered when making functional assignments:

1 BLSP11 has additional GPIO multiplex options for UART and I2C functions:
- BLSP11 UART transmit data is also available on GPIO_100
- BLSP11 UART receive data is also available on GPIO_101
- BLSP11 I2C serial data is also available on GPIO_102
- BLSP11 I2C serial clock is also available on GPIO_103

2 Extra chip selects (output only) are available when certain BLSPs are used for SPI:
- BLSP1 has extra CS1, CS2A, CS2B, CS3A, and CS3B for its SPI.
- BLSP2 has extra CS1, CS2, and CS3 for its SPI.
- BLSP10 has extra CS1A, CA1B, CS2A, CS2B, and CS3 for its SPI.

3 Two UIM ports are multiplexed with BLSP pins:
- UIM3 is multiplexed with BLSP9.
- UIM4 is multiplexed with BLSP11.

4 BLSPs that are configured for SPI or I2C or UART functionality require data mover access to achieve their higher throughput rates. In any BLSP, the SPI and I2C share the same FIFO/ADM CRCI interface and the UART/UIM share the same FIFO and ADM CRCI interface.

5 I2C can use only BLSP bits [0] and [1]. UIM can use only BLSP bits [2] and [3]. UART_RX and UART_TX are also only available on bits [2] and [3], as shown in Table 12. These rules apply across all 12 BLSPs.

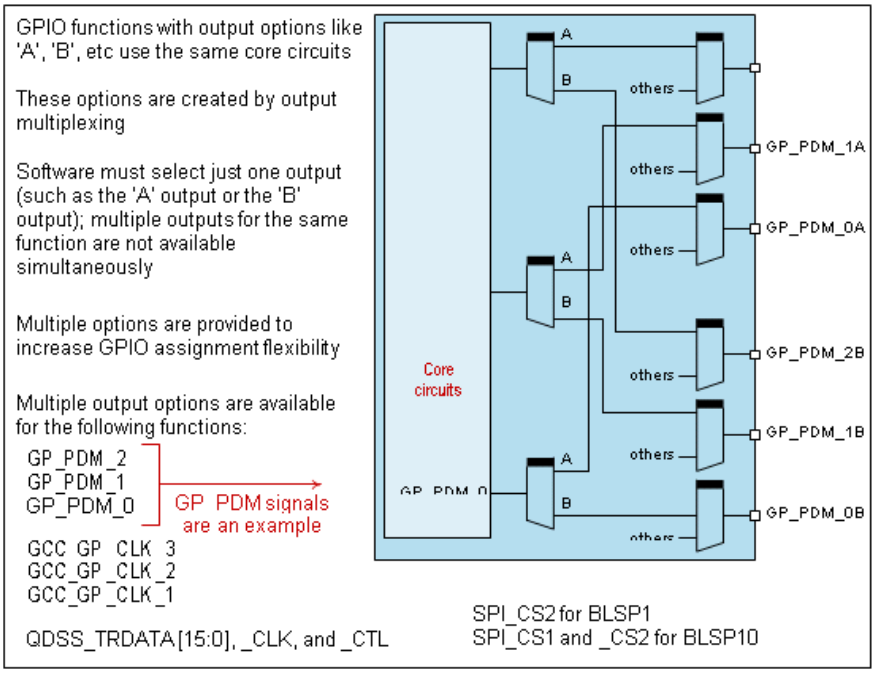


Figure 6 GPIO 'A/B' multiplexing

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
Clocks and related signals [1]					
Also see Table 16 for clock and related functions that interface with the PMIC (SLEEP_CLK, CXO, CXO_EN)					
AR5	QREFS_REXT	–	–	AI, A0	External resistor for on-die clocking
AK50	GCC_GP_CLK_1A	GPIO_57	P3	DO B-PD:nppukp	Global general-purpose clock 1 A Configurable I/O
F10	GCC_GP_CLK_1B	GPIO_78	P3	DO B-PD:nppukp	Global general-purpose clock 1 B Configurable I/O
AJ51	GCC_GP_CLK_2A	GPIO_58	P3	DO B-PD:nppukp	Global general-purpose clock 2 A Configurable I/O
D8	GCC_GP_CLK_2B	GPIO_81	P3	DO B-PD:nppukp	Global general-purpose clock 2 B Configurable I/O
AJ49	GCC_GP_CLK_3A	GPIO_59	P3	DO B-PD:nppukp	Global general-purpose clock 3 A Configurable I/O
C7	GCC_GP_CLK_3B	GPIO_82	P3	DO B-PD:nppukp	Global general-purpose clock 3 B Configurable I/O
E25	GP_CLK0	GPIO_112	P3	DO B-PD:nppukp	General-purpose clock 0 output Configurable I/O
G27	GP_CLK1	GPIO_113	P3	DO B-PD:nppukp	General-purpose clock 1 output Configurable I/O
BG3	GP_MN	GPIO_29	P3	DO B-PD:nppukp	General-purpose M/N:D counter output Configurable I/O
W5	GP_PDM_0A	GPIO_95	P3	DO B-PD:nppukp	General-purpose PDM output 0 A Configurable I/O
BC47	GP_PDM_0B	GPIO_54	P3	DO B-PD:nppukp	General-purpose PDM output 0 B Configurable I/O
BG47	GP_PDM_1A	GPIO_86	P3	DO B-PD:nppukp	General-purpose PDM output 1 A Configurable I/O
BF50	GP_PDM_1B			DO	General-purpose PDM

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
		GPIO_8	P3	B-PD:nppukp	output 1 B Configurable I/O
E11	GP_PDM_2A	GPIO_79	P3	DO B-PD:nppukp	General-purpose PDM output 2 A Configurable I/O
AH46	GP_PDM_2B	GPIO_63	P3	DO B-PD:nppukp	General-purpose PDM output 2 B Configurable I/O
Resets and mode controls – see the list of APQ8096 pins (Table 14) that can wake up the device (thereby supporting APM)					
Also see the boot configuration pins listed in Table 8 Also see Table 16 for reset and mode-control functions that interface with the PMIC (RESIN_N, PS_HOLD)					
BA51	MODE_1	–	P3	DIS-PD	Mode control bit 1 – unconnected for native mode
BB46	MODE_0	–	P3	DIS-PD	Mode control bit 0 – unconnected for native mode
B26	RESOUT_N	–	P3	DO	Reset output
JTAG interface					
N5	SRST_N	–	P3	DI PU	JTAG reset for debug
K4	TCK	–	P3	DI PU	JTAG clock input
L3	TDI	–	P3	DI PU:nppukp	JTAG data input
J1	TDO	–	P3	DO-Z	JTAG data output
K2	TMS	–	P3	DI PU:nppukp	JTAG mode select input
M2	TRST_N	–	P3	DI PD	JTAG reset
QDSS interface for ETM					
AJ51	QDSS_TRDATA_15B	GPIO_58	P3	DO B-PD:nppukp	QDSS trace data bit 15 B Configurable I/O
AK50	QDSS_TRDATA_14B	GPIO_57	P3	DO B-PD:nppukp	QDSS trace data bit 14 B Configurable I/O
BG3	QDSS_TRDATA_13B	GPIO_29	P3	DO B-PD:nppukp	QDSS trace data bit 13 B Configurable I/O
D4	QDSS_TRDATA_12B	GPIO_26	P3	DO B-PD:nppukp	QDSS trace data bit 12 B Configurable I/O

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
L5	QDSS_TRDATA_11B	GPIO_23	P3	DO B-PD:nppukp	QDSS trace data bit 11 B Configurable I/O
J3	QDSS_TRDATA_10B	GPIO_22	P3	DO B-PD:nppukp	QDSS trace data bit 10 B Configurable I/O
H2	QDSS_TRDATA_9B	GPIO_21	P3	DO B-PD:nppukp	QDSS trace data bit 9 B Configurable I/O
BF10	QDSS_TRDATA_8B	GPIO_19	P3	DO B-PD:nppukp	QDSS trace data bit 8 B Configurable I/O
BG7	QDSS_TRDATA_7B	GPIO_18	P3	DO B-PD:nppukp	QDSS trace data bit 7 B Configurable I/O
BF12	QDSS_TRDATA_6B	GPIO_17	P3	DO B-PD:nppukp	QDSS trace data bit 6 B Configurable I/O
BG5	QDSS_TRDATA_5B	GPIO_16	P3	DO B-PD:nppukp	QDSS trace data bit 5 B Configurable I/O
BF8	QDSS_TRDATA_4B	GPIO_15	P3	DO B-PD:nppukp	QDSS trace data bit 4 B Configurable I/O
BE7	QDSS_TRDATA_3B	GPIO_14	P3	DO B-PD:nppukp	QDSS trace data bit 3 B Configurable I/O
BF4	QDSS_TRDATA_2B	GPIO_13	P3	DO B-PD:nppukp	QDSS trace data bit 2 B Configurable I/O

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
Y4	QDSS_TRDATA_1B	GPIO_92	P3	DO B-PD:nppukp	QDSS trace data bit 1 B Configurable I/O
U5	QDSS_TRDATA_0B	GPIO_93	P3	DO B-PD:nppukp	QDSS trace data bit 0 B Configurable I/O
V6	QDSS_TRCLK_B	GPIO_91	P3	DO B-PD:nppukp	QDSS trace clock B Configurable I/O
R5	QDSS_TRCTL_B	GPIO_94	P3	DO B-PD:nppukp	QDSS trace control B Configurable I/O
BC47	QDSS_TRDATA_15A	GPIO_54	P3	DO B-PD:nppukp	QDSS trace data bit 15 A Configurable I/O
BE47	QDSS_TRDATA_14A	GPIO_53	P3	DO B-PD:nppukp	QDSS trace data bit 14 A Configurable I/O
W3	QDSS_TRDATA_13A	GPIO_90	P3	DO B-PD:nppukp	QDSS trace data bit 13 A Configurable I/O
T6	QDSS_TRDATA_12A	GPIO_89	P3	DO B-PD:nppukp	QDSS trace data bit 12 A Configurable I/O
BH48	QDSS_TRDATA_11A	GPIO_87	P3	DO B-PD:nppukp	QDSS trace data bit 11 A Configurable I/O
BG47	QDSS_TRDATA_10A	GPIO_86	P3	DO B-PD:nppukp	QDSS trace data bit 10 A Configurable I/O
BG49	QDSS_TRDATA_9A	GPIO_85	P3	DO B-PD:nppukp	QDSS trace data bit 9 A Configurable I/O
C13	QDSS_TRDATA_8A	GPIO_77	P3	DO	QDSS trace data

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
				B-PD:nppukp	bit 8 A Configurable I/O
G11	QDSS_TRDATA_7A	GPIO_76	P3	DO B-PD:nppukp	QDSS trace data bit 7 A Configurable I/O
G9	QDSS_TRDATA_6A	GPIO_75	P3	DO B-PD:nppukp	QDSS trace data bit 6 A Configurable I/O
E7	QDSS_TRDATA_5A	GPIO_74	P3	DO B-PD:nppukp	QDSS trace data bit 5 A Configurable I/O
C9	QDSS_TRDATA_4A	GPIO_67	P3	DO B-PD:nppukp	QDSS trace data bit 4 A Configurable I/O
D10	QDSS_TRDATA_3A	GPIO_66	P3	DO B-PD:nppukp	QDSS trace data bit 3 A Configurable I/O
C11	QDSS_TRDATA_2A	GPIO_65	P3	DO B-PD:nppukp	QDSS trace data bit 2 A Configurable I/O
D6	QDSS_TRDATA_1A	GPIO_64	P3	DO B-PD:nppukp	QDSS trace data bit 1 A Configurable I/O
AH46	QDSS_TRDATA_0A	GPIO_63	P3	DO B-PD:nppukp	QDSS trace data bit 0 A Configurable I/O
B6	QDSS_TRCLK_A	GPIO_28	P3	DO B-PD:nppukp	QDSS trace clock A

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
					Configurable I/O
C5	QDSS_TRCTL_A	GPIO_27	P3	DO B-PD:nppukp	QDSS trace control A Configurable I/O
QDSS interface for SDC2					
AF6	QDSS_SDC2_TRDATA_3	SDC2_DATA_3	P3	DO B-PD:nppukp	QDSS trace data bit 3 over SDC2 Secure digital controller 2 data bit 3
AE7	QDSS_SDC2_TRDATA_2	SDC2_DATA_2	P2	DO B-PD:nppukp	QDSS trace data bit 2 over SDC2 Secure digital controller 2 data bit 2
AC5	QDSS_SDC2_TRDATA_1	SDC2_DATA_1	P2	DO B-PD:nppukp	QDSS trace data bit 1over SDC2 Secure digital controller 2 data bit 1
AD8	QDSS_SDC2_TRDATA_0	SDC2_DATA_0	P2	DO B-PD:nppukp	QDSS trace data bit 0 over SDC2 Secure digital controller 2 data bit 0
AE5	QDSS_SDC2_TRCLK	SDC2_CLK	P2	DO DO	QDSS trace clock over SDC2 Secure digital controller 2 clock
AD6	QDSS_SDC2_TRSYNC	SDC2_CMD	P2	DO B-PD:nppukp	QDSS trace sync over SDC2 Secure digital controller 2 command
QDSS triggers					
M6	QDSS_CTI_TRIG_IN_A	GPIO_24	P3	DI B-PD:nppukp	QDSS trigger input A Configurable I/O
F6	QDSS_CTI_TRIG_OUT_A	GPIO_25	P3	DO B-PD:nppukp	QDSS trigger output A Configurable I/O
BB48	QDSS_CTI_TRIG_IN_B	GPIO_5	P3	DI B-PD:nppukp	QDSS trigger input B Configurable I/O
BA49	QDSS_CTI_TRIG_OUT_B	GPIO_4	P3	DO B-PD:nppukp	QDSS trigger output B Configurable I/O

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
F2	QDSS_CTI_TRIG_IN_C	GPIO_42	P3	DI B-PD:nppukp	QDSS trigger input C Configurable I/O
F4	QDSS_CTI_TRIG_OUT_C	GPIO_41	P3	DO B-PD:nppukp	QDSS trigger output C Configurable I/O
AT52	QDSS_CTI_TRIG_IN_D	GPIO_101	P3	DI B-PD:nppukp	QDSS trigger input D Configurable I/O
AP46	QDSS_CTI_TRIG_OUT_D	GPIO_100	P3	DO B-PD:nppukp	QDSS trigger output D Configurable I/O

1. GPIO 'A/B' multiplexing is explained in Figure 6.
2. See Table 7 for parameter and acronym definitions.

Table 13 Pin descriptions – internal functions

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the Table 13), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. See Table 18 for a list of all supported functions for each GPIO.

Pad #	Pad name	Pad characteristics [1]		Additional wakeup function description
		Voltage	Type	
G7	GPIO_1	P3	B-PD:nppukp	General-purpose wakeup
BB48	GPIO_5	P3	B-PD:nppukp	General-purpose wakeup
BG51	GPIO_9	P3	B-PD:nppukp	General-purpose wakeup
BJ51	GPIO_11	P3	B-PD:nppukp	General-purpose wakeup
J3	GPIO_22	P3	B-PD:nppukp	General-purpose wakeup
M6	GPIO_24	P3	B-PD:nppukp	General-purpose wakeup
D4	GPIO_26	P3	B-PD:nppukp	General-purpose wakeup
BG45	GPIO_34	P3	B-PD:nppukp	General-purpose wakeup

Pad #	Pad name	Pad characteristics [1]		Additional wakeup function description
		Voltage	Type	
D2	GPIO_36	P3	B-PU:nppdkp	General-purpose wakeup
E1	GPIO_37	P3	B-PD:nppukp	PCIe0 wakeup
BJ47	GPIO_38	P3	B-PD:nppukp	General-purpose wakeup
AA1	GPIO_40	P3	B-PD:nppukp	General-purpose wakeup
F2	GPIO_42	P3	B-PD:nppukp	General-purpose wakeup
J7	GPIO_46	P3	B-PD:nppukp	General-purpose wakeup
BE51	GPIO_50	P3	B-PD:nppukp	General-purpose wakeup
BE47	GPIO_53	P3	B-PD:nppukp	General-purpose wakeup
BC47	GPIO_54	P3	B-PD:nppdkp	General-purpose wakeup
BD46	GPIO_56	P3	B-PD:nppukp	General-purpose wakeup
AK50	GPIO_57	P3	B-PD:nppukp	General-purpose wakeup
AJ51	GPIO_58	P3	B-PD:nppukp	SSC_IRQ_0 interrupt
AJ49	GPIO_59	P3	B-PD:nppukp	SSC_IRQ_1 interrupt
AH48	GPIO_60	P3	B-PD:nppukp	SSC_IRQ_2 interrupt
AH50	GPIO_61	P3	B-PD:nppukp	SSC_IRQ_3 interrupt
AJ47	GPIO_62	P3	B-PD:nppukp	SSC_IRQ_4 interrupt
AH46	GPIO_63	P3	B-PD:nppukp	SSC_IRQ_5 interrupt
D6	GPIO_64	P3	B-PD:nppukp	General-purpose wakeup
D10	GPIO_66	P3	B-PD:nppukp	General-purpose wakeup
D12	GPIO_71	P3	B-PD:nppukp	General-purpose wakeup
E9	GPIO_73	P3	B-PD:nppukp	General-purpose wakeup
C13	GPIO_77	P3	B-PD:nppukp	General-purpose wakeup
F10	GPIO_78	P3	B-PD:nppukp	SSC_IRQ_6 interrupt
E11	GPIO_79	P3	B-PD:nppukp	SSC_IRQ_7 interrupt
E5	GPIO_80	P3	B-PD:nppukp	SSC_IRQ_8 interrupt
C7	GPIO_82	P3	B-PD:nppukp	General-purpose wakeup
BG47	GPIO_86	P3	B-PD:nppukp	General-purpose wakeup
V6	GPIO_91	P3	B-PD:nppukp	General-purpose wakeup
Y4	GPIO_92	P3	B-PD:nppukp	General-purpose wakeup
W5	GPIO_95	P3	B-PD:nppukp	Secure digital card detect
AR49	GPIO_97	P3	B-PD:nppukp	General-purpose wakeup
AT52	GPIO_101	P3	B-PD:nppukp	General-purpose wakeup
AU51	GPIO_104	P3	B-PD:nppukp	General-purpose wakeup
B24	GPIO_106	P3	BH-PD:nppukp	General-purpose wakeup
C25	GPIO_108	P3	B-PD:nppukp	UIM2 presence detection
E23	GPIO_110	P3	BH-PD:nppukp	General-purpose wakeup
E25	GPIO_112	P3	B-PD:nppukp	UIM1 presence detection
G27	GPIO_113	P3	B-PD:nppukp	UIM battery alarm
AU49	GPIO_115	P3	B-PU:nppdkp	General-purpose wakeup
AT46	GPIO_116	P3	B-PD:nppukp	PCIe2 wakeup
BC49	GPIO_117	P3	B-PD:nppukp	SSC_IRQ_9 interrupt
BG41	GPIO_118	P3	B-PD:nppukp	SSC_IRQ_10 interrupt

Pad #	Pad name	Pad characteristics [1]		Additional wakeup function description
		Voltage	Type	
AR51	GPIO_119	P3	B-PD:nppukp	SSC_IRQ_11 interrupt
AU47	GPIO_120	P3	B-PD:nppukp	SSC_IRQ_12 interrupt
BA47	GPIO_121	P3	B-PD:nppukp	SSC_IRQ_13 interrupt
BF42	GPIO_122	P3	B-PD:nppukp	SSC_IRQ_14 interrupt
BG43	GPIO_123	P3	B-PD:nppukp	SSC_IRQ_15 interrupt
BF48	GPIO_124	P3	B-PD:nppukp	SSC_IRQ_16 interrupt
BF44	GPIO_125	P3	B-PD:nppukp	SSC_IRQ_17 interrupt
AR47	GPIO_126	P3	B-PD:nppukp	General-purpose wakeup
AY48	GPIO_127	P3	B-PD:nppukp	General-purpose wakeup
AV50	GPIO_129	P3	B-PD:nppukp	General-purpose wakeup
B4	GPIO_131	P3	B-PU:nppdkp	General-purpose wakeup
B2	GPIO_132	P3	B-PD:nppukp	PCIe1 wakeup
AW51	GPIO_133	P3	B-PD:nppukp	General-purpose wakeup
AP50	GPIO_145	P3	B-PD:nppukp	General-purpose wakeup
T4	SDC1_DATA_1	P7	B-PD:nppukp	Secure digital controller 1 data bit 1
U1	SDC1_DATA_3	P7	B-PD:nppukp	Secure digital controller 1 data bit 3
AC5	SDC2_DATA_1	P2	BH-PD:nppukp	Secure digital controller 2 data bit 1
AF6	SDC2_DATA_3	P2	BH-PD:nppukp	Secure digital controller 2 data bit 3
AD6	SDC2_CMD	P2	BH-PD:nppukp	Secure digital controller 2 command
N5	SRST_N	P3	DI	JTAG reset for debug

1. See Table 7 for parameter and acronym definitions.

Table 14 APQ8096 wakeup pins for APQ power management (APM)

MODE[1:0]	Usage
00	Native mode
11	Boundary-scan mode
Others	Test modes

Table 15 MODE [1:0] settings

Pad #	Pad name and/or function	Pad name or alt function	Pad Characterstics[3]		Functional description
			Voltage	Type	
WTRs – Rx baseband interfaces					
R51	BBRX_CH0_I	–	–	AI	Baseband receiver input, channel 0, in-phase
P50	BBRX_CH0_Q	–	–	AI	Baseband receiver input, channel 0, quadrature-phase
N51	BBRX_CH1_I	–	–	AI	Baseband receiver input, channel 1, in-phase

Pad #	Pad name and/or function	Pad name or alt function	Pad Characterstics[3]		Functional description
			Voltage	Type	
M52	BBRX_CH1_Q	–	–	AI	Baseband receiver input, channel 1, quadrature-phase
L51	BBRX_CH2_I	–	–	AI	Baseband receiver input, channel 2, in-phase
K50	BBRX_CH2_Q	–	–	AI	Baseband receiver input, channel 2, quadrature-phase
J51	BBRX_CH3_I	–	–	AI	Baseband receiver input, channel 3, in-phase
H52	BBRX_CH3_Q	–	–	AI	Baseband receiver input, channel 3, quadrature-phase
G51	BBRX_CH4_I	–	–	AI	Baseband receiver input, channel 4, in-phase
F50	BBRX_CH4_Q	–	–	AI	Baseband receiver input, channel 4, quadrature-phase
E51	BBRX_CH5_I	–	–	AI	Baseband receiver input, channel 5, in-phase
E49	BBRX_CH5_Q	–	–	AI	Baseband receiver input, channel 5, quadrature-phase
U51	BBRX_FB_I	–	–	AI	Baseband receiver input, Tx feedback, in-phase
T52	BBRX_FB_Q	–	–	AI	Baseband receiver input, Tx feedback, quadrature phase
Note: For the APQ8096 device, the BBRX interface is not needed. The pins must be terminated.					
WTRs – GNSS Rx baseband interface					
T48	GNSS_BB_IP	–	–	AI	GNSS receiver baseband input, in-phase plus
T50	GNSS_BB_IM	–	–	AI	GNSS receiver baseband input, in-phase minus
T46	GNSS_BB_QP	–	–	AI	GNSS receiver baseband input, quadrature plus
U49	GNSS_BB_QM	–	–	AI	GNSS receiver baseband input, quadrature minus
WTRs – Tx baseband interfaces					
AE51	TX_DAC0_IP	–	–	AO	Transmitter DAC 0 output, in-phase plus
AD52	TX_DAC0_IM	–	–	AO	Transmitter DAC 0 output, in-phase minus
AC51	TX_DAC0_QP	–	–	AO	Transmitter DAC 0 output, quadrature plus
AD50	TX_DAC0_QM	–	–	AO	Transmitter DAC 0 output, quadrature minus
AD48	TX_DAC0_VREF	–	–	AI	Transmitter DAC 0 voltage reference

Pad #	Pad name and/or function	Pad name or alt function	Pad Characterstics[3]		Functional description
			Voltage	Type	
AA51	TX_DAC1_IP	–	–	AO	Transmitter DAC 1 output, in-phase plus
Y52	TX_DAC1_IM	–	–	AO	Transmitter DAC 1 output, in-phase minus
W51	TX_DAC1_QP	–	–	AO	Transmitter DAC 1 output, quadrature plus
Y50	TX_DAC1_QM	–	–	AO	Transmitter DAC 1 output, quadrature minus
Y48	TX_DAC1_VREF	–	–	AI	Transmitter DAC 1 voltage reference Note
Note: For the APQ8096 device, the TX_DAC interface is not needed. The pins must be terminated.					
WTRs – GSM transmit phase adjust signals					
AW49	GSM_TX_PHASE_D1	GPIO_135	P3	DO B-PD:nppukp	GSM transmit phase adjust data bit 1 for WTR Configurable I/O
AW47	GSM_TX_PHASE_D0	GPIO_134	P3	DO B-PD:nppukp	GSM transmit phase adjust data bit 0 for WTR Configurable I/O
Note: For the APQ8096 device, the GSM_TX_PHASE function is not needed. The pins can be used as general-purpose GPIO pins.					
PMIC interfaces					
B28	SLEEP_CLK	–	P3	DI	Sleep clock
E45	CXO	–	P11	DI	Core crystal oscillator (digital 19.2 MHz system clock)
F46	CXO_EN	–	P3	DO	Core crystal oscillator enable
AV6	CXO_2	–	P9	DI	Core crystal oscillator 2 (analog 19.2 MHz system clock)
G29	RESIN_N	–	P3	DI	Reset input
B30	SPMI_DATA	–	P3	B	Slave and PBUS interface for PMICs – data
A29	SPMI_CLK	–	P3	DO	Slave and PBUS interface for PMICs – clock
C29	PS_HOLD	–	P3	DO	Power-supply hold signal to PMIC
QCA6174A WLAN/Bluetooth interfaces					
–	*See Table 11 for PCIe and UART interface details.*				
AP50	LTE_COEX_RX	GPIO_145	P3	DI B-PD:nppukp	UART Rx for LTE-WLAN coexistence Configurable I/O
AR45	LTE_COEX_TX	GPIO_144	P3	DO B-PD:nppukp	UART Tx for LTE-WLAN coexistence

Pad #	Pad name and/or function	Pad name or alt function	Pad Characterstics[3]		Functional description
			Voltage	Type	
					Configurable I/O
AN51	GNSS_TX_AGGRESSOR	GPIO_143	P3	DI B-PD:nppukp	Tx level may degrade GNSS receiver Configurable I/O
QCA6320/QCA6310 WiGig interfaces					
–	*See Table 11 for PCIe interface details.*				
WCD9335 interfaces					
–	*See Table 11 for SLIMbus details; also for I2S and I2C connectivity ports that can be used as an alternative*				
WSA881x interfaces					
–	*See Table 11 for I2C interface details.*				
Qualcomm RF360 interfaces [1, 2]					
AB50	ET_DAC0_P	–	–	AO	Envelope tracking DAC0 output, plus
AC49	ET_DAC0_M	–	–	AO	Envelope tracking DAC0 output, minus
AA49	ET_DAC0_VREF	–	–	AI	Envelope tracking DAC0 output, voltage reference
V48	ET_DAC1_P	–	–	AO	Envelope tracking DAC1 output, plus
W49	ET_DAC1_M	–	–	AO	Envelope tracking DAC1 output, minus
W47	ET_DAC1_VREF	–	–	AI	Envelope tracking DAC1 output, voltage reference
AM46	RFFE1_CLK	GPIO_149	P3	DO B-PD:nppukp	RF front-end 1 interface clock Configurable I/O
AN47	RFFE1_DATA	GPIO_148	P3	B B-PD:nppukp	RF front-end 1 interface data Configurable I/O
AM52	RFFE2_CLK	GPIO_147	P3	DO B-PD:nppukp	RF front-end 2 interface clock Configurable I/O
AL51	RFFE2_DATA	GPIO_146	P3	B B-PD:nppukp	RF front-end 2 interface data Configurable I/O
AK48	RFFE3_CLK	GPIO_138	P3	DO B-PD:nppukp	RF front-end 3 interface clock Configurable I/O
AK46	RFFE3_DATA	GPIO_137	P3	B B-PD:nppukp	RF front-end 3 interface data Configurable I/O
AL47	RFFE4_CLK	GPIO_140	P3	DO B-PD:nppukp	RF front-end 4 interface clock Configurable I/O
AM48	RFFE4_DATA	GPIO_139	P3	B B-PD:nppukp	RF front-end 4 interface data Configurable I/O
AM50	RFFE5_CLK	GPIO_142	P3	DO B-PD:nppukp	RF front-end 5 interface clock Configurable I/O
AL49	RFFE5_DATA	GPIO_141	P3	B B-PD:nppukp	RF front-end 5 interface data Configurable I/O

Pad #	Pad name and/or function	Pad name or alt function	Pad Characterstics[3]		Functional description
			Voltage	Type	
AR49	RFFE6_CLK	GPIO_97	P3	DO B-PD:nppukp	RF front-end 6 interface clock Configurable I/O
AP48	RFFE6_DATA	GPIO_98	P3	B B-PD:nppukp	RF front-end 6 interface data Configurable I/O
AN49	RFFE7_CLK	GPIO_99	P3	DO B-PD:nppukp	RF front-end 7 interface clock Configurable I/O
AP46	RFFE7_DATA	GPIO_100	P3	B B-PD:nppukp	RF front-end 7 interface data Configurable I/O

1. For the APQ8096 device, the ET_DAC interface is not needed. The pins must be terminated.
2. For the APQ8096 device, the RFFE function is not needed. The pins can be used as general-purpose GPIO.
3. See Table 7 for parameter and acronym definitions.

Table 16 Pin descriptions – chipset interface functions

NOTE *GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the Table 16), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. See Table 18 for a list of all supported functions for each GPIO.*

Pad #	Pad name and/or function	Pad name or alt function	Pad Characteristics [3]		Pad #
			Voltage	Type	
General RF control (GRFC) signals [2]					
AR49	GRFC_0	GPIO_97	P3	DO B-PD:nppukp	Generic RF controller bit 0 Configurable I/O
AP48	GRFC_1	GPIO_98	P3	DO B-PD:nppukp	Generic RF controller bit 1 Configurable I/O
AN49	GRFC_2	GPIO_99	P3	DO B-PD:nppukp	Generic RF controller bit 2 Configurable I/O
AP46	GRFC_3	GPIO_100	P3	DO B-PD:nppukp	Generic RF controller bit 3 Configurable I/O
AT52	GRFC_4	GPIO_101	P3	DO B-PD:nppukp	Generic RF controller bit 4 Configurable I/O
AT50	GRFC_5	GPIO_102	P3	DO B-PD:nppukp	Generic RF controller bit 5 Configurable I/O
AT48	GRFC_6	GPIO_103	P3	DO B-PD:nppukp	Generic RF controller bit 6 Configurable I/O
AU51	GRFC_7	GPIO_104	P3	DO B-PD:nppukp	Generic RF controller bit 7 Configurable I/O
AV48	GRFC_8	GPIO_114	P3	DO	Generic RF controller bit 8

Pad #	Pad name and/or function	Pad name or alt function	Pad Characteristics [3]		Pad #
			Voltage	Type	
				B-PD:nppukp	Configurable I/O
AU49	GRFC_9	GPIO_115	P3	DO B-PU:nppdkp	Generic RF controller bit 9 Configurable I/O
AT46	GRFC_10	GPIO_116	P3	DO B-PD:nppukp	Generic RF controller bit 10 Configurable I/O
AY48	GRFC_11	GPIO_127	P3	DO B-PD:nppukp	Generic RF controller bit 11 Configurable I/O
AV46	GRFC_12	GPIO_128	P3	DO B-PD:nppukp	Generic RF controller bit 12 Configurable I/O
AV50	GRFC_13	GPIO_129	P3	DO B-PD:nppukp	Generic RF controller bit 13 Configurable I/O
AW51	GRFC_14	GPIO_133	P3	DO B-PD:nppukp	Generic RF controller bit 14 Configurable I/O
AY52	GRFC_15	GPIO_136	P3	DO B-PD:nppukp	Generic RF controller bit 15 Configurable I/O
RFFE interfaces					
–	See Table 16 for RFFE interface details.				

1. See Table 7 for parameter and acronym definitions.
2. For the APQ8096 device, the GRFC function is not needed. The pins can be used as general-purpose GPIO.

Table 17 Pin descriptions – RF front-end functions

NOTE *GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the Table 17), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. See Table 18 for a list of all supported functions for each GPIO.*

NOTE *Handset designers must examine each of the external connection and programmed configuration of GPIO's, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:*

- GPIO configuration
  - Input vs. output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

Pad #	Pad name	Configurable function	Pad characteristics[1]		Functional description
			Voltage	Type	
AM46	GPIO_149	RFFE1_CLK	P3	B-PD:nppukp DO	Configurable I/O RF front-end 1 interface clock
AN47	GPIO_148	RFFE1_DATA	P3	B-PD:nppukp B	Configurable I/O RF front-end 1 interface data
AM52	GPIO_147	RFFE2_CLK	P3	B-PD:nppukp DO	Configurable I/O RF front-end 2 interface clock
AL51	GPIO_146	RFFE2_DATA	P3	B-PD:nppukp B	Configurable I/O RF front-end 2 interface data
AP50	GPIO_145	LTE_COEX_RX	P3	B-PD:nppukp DI	Configurable I/O UART Rx for LTE-WLAN coexistence
AR45	GPIO_144	LTE_COEX_TX	P3	B-PD:nppukp DO	Configurable I/O UART Tx for LTE-WLAN coexistence
AN51	GPIO_143	GNSS_TX_AGRESSOR	P3	B-PD:nppukp DI	Configurable I/O Tx level may degrade GNSS receiver
AM50	GPIO_142	RFFE5_CLK	P3	B-PD:nppukp DO	Configurable I/O RF front-end 5 interface clock
AL49	GPIO_141	RFFE5_DATA	P3	B-PD:nppukp B	Configurable I/O RF front-end 5 interface data
AL47	GPIO_140	RFFE4_CLK	P3	B-PD:nppukp DO	Configurable I/O RF front-end 4 interface clock
AM48	GPIO_139	RFFE4_DATA	P3	B-PD:nppukp B	Configurable I/O RF front-end 4 interface data
AK48	GPIO_138	RFFE3_CLK	P3	B-PD:nppukp DO	Configurable I/O RF front-end 3 interface clock
AK46	GPIO_137	RFFE3_DATA	P3	B-PD:nppukp B	Configurable I/O RF front-end 3 interface data
AY52	GPIO_136	GRFC_15	P3	B-PD:nppukp DO	Configurable I/O Generic RF controller bit 15
AW49	GPIO_135	GSM_TX_PHASE_D1	P3	B-PD:nppukp DO	Configurable I/O GSM transmit phase adjust data bit 1 for WTR
AW47	GPIO_134	GSM_TX_PHASE_D0	P3	B-PD:nppukp DO	Configurable I/O GSM transmit phase adjust data bit 0 for WTR
AW51	GPIO_133	GRFC_14	P3	B-PD:nppukp DO	Configurable I/O Generic RF controller bit 14
B2	GPIO_132	-	P3	B-PD:nppukp	Configurable I/O

Pad #	Pad name	Configurable function	Pad characteristics[1]		Functional description
			Voltage	Type	
B4	GPIO_131	PCIE1_CLKREQ_N	P3	B-PU:nppdkp DI	Configurable I/O PCIe 1 clock request
C3	GPIO_130	PCIE1_RST_N	P3	B-PD:nppukp DO	Configurable I/O PCIe 1 reset
AV50	GPIO_129	GRFC_13	P3	B-PD:nppukp DO	Configurable I/O Generic RF controller bit 13
AV46	GPIO_128	GRFC_12	P3	B-PD:nppukp DO	Configurable I/O Generic RF controller bit 12
AY48	GPIO_127	GRFC_11	P3	B-PD:nppukp DO	Configurable I/O Generic RF controller bit 11
AR47	GPIO_126	–	P3	B-PD:nppukp	Configurable I/O
BF44	GPIO_125	–	P3	B-PD:nppukp	Configurable I/O
BF48	GPIO_124	–	P3	B-PD:nppukp	Configurable I/O
BG43	GPIO_123	–	P3	B-PD:nppukp	Configurable I/O
BF42	GPIO_122	–	P3	B-PD:nppukp	Configurable I/O
BA47	GPIO_121	–	P3	B-PD:nppukp	Configurable I/O
AU47	GPIO_120	–	P3	B-PD:nppukp	Configurable I/O
AR51	GPIO_119	–	P3	B-PD:nppukp	Configurable I/O
BG41	GPIO_118	–	P3	B-PD:nppukp	Configurable I/O
BC49	GPIO_117	–	P3	B-PD:nppukp	Configurable I/O
AT46	GPIO_116	PA_INDICATOR GRFC_10	P3	B-PD:nppukp DO	Configurable I/O PA transmit indicator Generic RF controller bit 10
AU49	GPIO_115	GRFC_9 PCIE2_CLKREQ_N	P3	B-PU:nppdkp DO DI	Configurable I/O Generic RF controller bit 9 PCIe 2 clock request
AV48	GPIO_114	GRFC_8 PCIE2_RST_N	P3	B-PD:nppukp DO DO	Configurable I/O Generic RF controller bit 8 PCIe 2 reset
G27	GPIO_113	UIM_BATT_ALARM GP_CLK1	P3	B-PD:nppukp DI DO	Configurable I/O UIM battery alarm General- purpose clock 1
E25	GPIO_112	UIM1_PRESENT GP_CLK0	P3	B-PD:nppukp DI DO	Configurable I/O UIM1 presence detection General-purpose clock 0
F26	GPIO_111	UIM1_RESET	P5	BH-PD:nppukp DO	Configurable I/O UIM1 reset (dual-voltage)
E23	GPIO_110	UIM1_CLK	P5	BH-PD:nppukp	Configurable I/O

Pad #	Pad name	Configurable function	Pad characteristics[1]		Functional description
			Voltage	Type	
				DO	UIM1 clock (dual-voltage)
D24	GPIO_109	UIM1_DATA	P5	BH-PD:nppukp B	Configurable I/O UIM1 data (dual-voltage)
C25	GPIO_108	UIM2_PRESENT	P3	B-PD:nppukp DI	Configurable I/O UIM2 presence detection
A25	GPIO_107	UIM2_RESET	P6	BH-PD:nppukp DO	Configurable I/O UIM2 reset (dual-voltage)
B24	GPIO_106	UIM2_CLK	P6	BH-PD:nppukp DO	Configurable I/O UIM2 clock (dual-voltage)
C23	GPIO_105	UIM2_DATA	P6	BH-PD:nppukp B	Configurable I/O UIM2 data (dual-voltage)
AU51	GPIO_104	GRFC_7	P3	B-PD:nppukp DO	Configurable I/O Generic RF controller bit 7
AT48	GPIO_103	GRFC_6 BLSP11_I2C_SCL_B	P3	B-PD:nppukp DO B	Configurable I/O Generic RF controller bit 6 BLSP11_I2C_SCL_B (copy)
AT50	GPIO_102	GRFC_5 BLSP11_I2C_SDA_B	P3	B-PD:nppukp DO B	Configurable I/O Generic RF controller bit 5 BLSP11_I2C_SDA_B (copy)
AT52	GPIO_101	GRFC_4 BLSP11_UART_RX_B QDSS_CTI_TRIG_IN_D	P3	B-PD:nppukp DO DI DI	Configurable I/O Generic RF controller bit 4 BLSP11_UART_RX_B (copy) QDSS trigger input D
AP46	GPIO_100	GRFC_3 RFFE7_DATA BLSP11_UART_TX_B QDSS_CTI_TRIG_OUT_D	P3	B-PD:nppukp DO B DO DO	Configura ble I/O Generic RF controller bit 3 RF front-end 7 interface data BLSP11_UART_TX_B (copy) QDSS trigger output D
AN49	GPIO_99	GRFC_2 RFFE7_CLK	P3	B-PD:nppukp DO DO	Configurable I/O Generic RF controller bit 7 RF front-end 7 interface clock
AP48	GPIO_98	GRFC_1 RFFE6_DATA MDP_VSYNC_S_B	P3	B-PD:nppukp DO B DI	Configurable I/O Generic RF controller bit 1 RF front-end 6 interface data MDP vertical sync – secondary B

Pad #	Pad name	Configurable function	Pad characteristics[1]		Functional description
			Voltage	Type	
AR49	GPIO_97	GRFC_0 RFFE6_CLK MDP_VSYNC_P_B	P3	B-PD:nppukp DO DO DI	Configurable I/O Generic RF controller bit 0 RF front-end 6 interface clock MDP vertical sync – primary B
Y2	GPIO_96	TSIF2_SYNC SDC4_DATA_0	P3	B-PD:nppukp DI B	Configurable I/O Transport stream interface 2 sync Secure digital controller 4 data bit 0
W5	GPIO_95	TSIF2_DATA SDC4_DATA_1 GP_PDM_0A	P3	B-PD:nppukp DI B DO	Configurable I/O Transport stream interface 2 data Secure digital controller 4 data bit 1 General-purpose PDM output 0 A
R5	GPIO_94	TSIF2_EN SDC4_DATA_2 QDSS_TRCTL_B	P3	B-PD:nppukp DI B DO	Configurable I/O Transport stream interface 2 enable Secure digital controller 4 data bit 2 QDSS trace control B
U5	GPIO_93	TSIF2_CLK SDC4_CLK QDSS_TRDATA_0B	P3	B-PD:nppukp DI DO DO	Configurable I/O Transport stream interface 2 clock Secure digital controller 4 clock QDSS trace data bit 0 B
Y4	GPIO_92	TSIF2_ERROR SDC4_DATA_3 QDSS_TRDATA_1B	P3	B-PD:nppukp DI B DO	Configurable I/O Transport stream interface 2 error Secure digital controller 4 data bit 3 QDSS trace data bit 1 B
V6	GPIO_91	TSIF1_DATA SDC4_CMD QDSS_TRCLK_B	P3	B-PD:nppukp DI B DO	Configurable I/O Transport stream interface 1 data Secure digital controller 4 command QDSS trace clock B
W3	GPIO_90	TSIF1_EN BLSP1_SPI_CS1_N QDSS_TRDATA_13A	P3	B-PD:nppukp DI DO- Z DO	Configurable I/O Transport stream interface 1 enable Chip select 1 for SPI on BLSP #1 QDSS trace data bit 13 A
T6	GPIO_89	TSIF1_CLK QDSS_TRDATA_12A	P3	B-PD:nppukp DI DO	Configurable I/O Transport stream interface 1 clock QDSS trace data bit 12 A
BJ49	GPIO_88	BLSP12_0 BLSP10_SPI_CS3_N	P3	B-PD:nppukp B DO- Z	Configurable I/O BLSP #12 bit 0; SPI, UART, or I2C Chip select 3 for SPI on BLSP #10

Pad #	Pad name	Configurable function	Pad characteristics[1]		Functional description
			Voltage	Type	
BH48	GPIO_87	BLSP12_1 QDSS_TRDATA_11A	P3	B-PD:nppukp B DO	Configurable I/O BLSP #12, bit 1; SPI, UART, or I2C QDSS trace data bit 11 A
BG47	GPIO_86	BLSP12_2 GP_PDM_1A QDSS_TRDATA_10A	P3	B-PD:nppukp B DO DO	Configurable I/O BLSP #12, bit 2; SPI, UART, or UIM General-purpose PDM 1 A output QDSS trace data bit 10 A
BG49	GPIO_85	BLSP12_3 QDSS_TRDATA_9A	P3	B-PD:nppukp B DO	Configurable I/O BLSP #12, bit 3; SPI, UART, or UIM QDSS trace data bit 9 A
B8	GPIO_84	BLSP5_0	P3	B-PD:nppukp B	Configurable I/O BLSP #5, bit 0; SPI, UART, or I2C
A9	GPIO_83	BLSP5_1 MI2S_2_D1 PCM2_DOUT	P3	B-PD:nppukp B B B	Configurable I/O BLSP #5, bit 1; SPI, UART, or I2C MI2S #2 serial data channel 1 Audio PCM data output (port 2)
C7	GPIO_82	BLSP5_2 MI2S_2_D0 PCM2_DIN GCC_GP_CLK_3B	P3	B-PD:nppukp B B B DO	Configurable I/O BLSP #5, bit 2; SPI, UART, or UIM MI2S #2 serial data channel 0 Audio PCM data input (port 2) Global general- purpose clock 3 B
D8	GPIO_81	BLSP5_3 MI2S_2_WS PCM2_SYNC GCC_GP_CLK_2B	P3	B-PD:nppukp B B B DO	Configurable I/O BLSP #5, bit 3; SPI, UART, or UIM MI2S #2 word select (L/R) Audio PCM sync (port 2) Global general-purpose clock 2 B
E5	GPIO_80	MI2S_2_SCK PCM2_CLK	P3	B-PD:nppukp B B	Configura ble I/O MI2S #2 bit clock Audio PCM clock (port 2)
E11	GPIO_79	MI2S_2_MCLK GP_PDM_2A	P3	B-PD:nppukp DO	Configurable I/O MI2S #2 master clock

Pad #	Pad name	Configurable function	Pad characteristics[1]		Functional description
			Voltage	Type	
				DO	General-purpose PDM 2 A output
F10	GPIO_78	MI2S_3_D1 PCM3_DOUT GCC_GP_CLK_1B	P3	B-PD:nppukp B B DO	Configurable I/O MI2S #3 serial data channel 1 Audio PCM data output (port 3) Global general- purpose clock 1 B
C13	GPIO_77	MI2S_3_D0 PCM3_DIN QDSS_TRDATA_8A	P3	B-PD:nppukp B B DO	Configurable I/O MI2S #3 serial data channel 0 Audio PCM data input (port 3) QDSS trace data bit 8 A
G11	GPIO_76	MI2S_3_WS PCM3_SYNC QDSS_TRDATA_7A	P3	B-PD:nppukp B B DO	Configurable I/O MI2S #3 word select (L/R) Audio PCM sync (port 3) QDSS trace data bit 7 A
G9	GPIO_75	MI2S_3_SCK PCM3_CLK QDSS_TRDATA_6A	P3	B-PD:nppukp B B DO	Configura ble I/O MI2S #3 bit clock Audio PCM clock (port 3) QDSS trace data bit 6 A
E7	GPIO_74	MI2S_3_MCLK QDSS_TRDATA_5A	P3	B-PD:nppukp DO DO	Configurable I/O MI2S #3 master clock QDSS trace data bit 5 A
E9	GPIO_73	–	P3	B-PD:nppukp	Configurable I/O
E13	GPIO_72	LPASS_SLIMBUS_DATA1 SPKR_I2S_WS	P3	B-PD:nppukp DO B	Configurable I/O Low-power audio SLIMbus data 1 Speaker I2S word select (L/R)
D12	GPIO_71	LPASS_SLIMBUS_DATA0 SPKR_I2S_DOUT	P3	B-PD:nppukp DO DO	Configurable I/O Low-power audio SLIMbus data 0 Speaker I2S data output
D14	GPIO_70	LPASS_SLIMBUS_CLK SPKR_I2S_SCK	P3	B-PD:nppukp DO B	Configurable I/O Low-power audio SLIMbus clock Speaker I2S bit clock
F8	GPIO_69	SPKR_I2S_MCLK AUDIO_REF_CLK	P3	B-PD:nppukp DO DI	Configurable I/O Speaker I2S master clock Audio reference clock

Pad #	Pad name	Configurable function	Pad characteristics[1]		Functional description
			Voltage	Type	
B10	GPIO_68	BLSP4_0 MI2S_1_D1 PCM1_DOUT	P3	B-PD:nppukp BB B	Configurable I/O BLSP #4, bit 0; SPI, UART, or I2C MI2S #1 serial data channel 1 Audio PCM data output (port 1)
C9	GPIO_67	BLSP4_1 MI2S_1_D0 PCM1_DIN QDSS_TRDATA_4A	P3	B-PD:nppukp BB B DO	Configurable I/O BLSP #4, bit 1; SPI, UART, or I2C MI2S #1 serial data channel 0 Audio PCM data input (port 1) QDSS trace data bit 4 A
D10	GPIO_66	BLSP4_2 MI2S_1_WS PCM1_SYNC QDSS_TRDATA_3A	P3	B-PD:nppukp B B B D0	Configurable I/O BLSP #4, bit 2; SPI, UART, or UIM MI2S #1 word select (L/R) Audio PCM sync (port 1) QDSS trace data bit 3 A
C11	GPIO_65	BLSP4_3 MI2S_1_SCK PCM1_CLK QDSS_TRDATA_2A	P3	B-PD:nppukp B B B DO	Configurable I/O BLSP #4, bit 3; SPI, UART, or UIM MI2S #1 bit clock Audio PCM clock (port 1) QDSS trace data bit 2 A
D6	GPIO_64	MI2S_1_MCLK QDSS_TRDATA_1A	P3	B-PD:nppukp DO DO	Configurable I/O MI2S #1 master clock QDSS trace data bit 1 A
AH46	GPIO_63	MI2S_4_D3 GP_PDM_2B QDSS_TRDATA_0A	P3	B-PD:nppukp B DO DO	Configurable I/O MI2S #4 serial data channel 3 General-purpose PDM output 2 B QDSS trace data bit 0 A
AJ47	GPIO_62	MI2S_4_D2	P3	B-PD:nppukp B	Configurable I/O MI2S #4 serial data channel 2
AH50	GPIO_61	BLSP11_0 MI2S_4_D1 PCM4_DOUT UIM4_PRESENT	P3	B-PD:nppukp B B B DI	Configurable I/O BLSP #11, bit 0; SPI, UART, or I2C MI2S #4 serial data channel 1 Audio PCM data

Pad #	Pad name	Configurable function	Pad characteristics[1]		Functional description
			Voltage	Type	
					output (port 4) UIM4 presence detection
AH48	GPIO_60	BLSP11_1 MI2S_4_D0 PCM4_DIN UIM4_RESET	P3	B-PD:nppukp B B B DO	Configurable I/O BLSP #11, bit 1; SPI, UART, or I2C MI2S #4 serial data channel 0 Audio PCM data input (port 4) UIM4 reset
AJ49	GPIO_59	BLSP11_2 MI2S_4_WS PCM4_SYNC UIM4_CLK GCC_GP_CLK_3A	P3	B-PD:nppukp B B B DO DO	Configurable I/O BLSP #11, bit 2; SPI, UART, or UIM MI2S #4 word select (L/R) Audio PCM sync (port 4) UIM4 clock Global general-purpose clock 3 A
AJ51	GPIO_58	BLSP11_3 MI2S_4_SCK PCM4_CLK UIM4_DATA GCC_GP_CLK_2A QDSS_TRDATA_15B	P3	B-PD:nppukp B B B B DO DO	Configurable I/O BLSP #11, bit 3; SPI, UART, or UIM MI2S #4 bit clock Audio PCM clock (port 4) UIM4 data Global general-purpose clock 2 A QDSS trace data bit 15 B
AK50	GPIO_57	MI2S_4_MCLK GCC_GP_CLK_1A QDSS_TRDATA_14B	P3	B-PD:nppukp DO DO DO	Configurable I/O MI2S #4 master clock Global general-purpose clock 1 A QDSS trace data bit 14 B
BD46	GPIO_56	BLSP7_0	P3	B-PD:nppukp B	Configurable I/O BLSP #7, bit 0; SPI, UART, or I2C
BD48	GPIO_55	BLSP7_1	P3	B-PD:nppukp B	Configurable I/O BLSP #7, bit 1; SPI, UART, or I2C
BC47	GPIO_54	BLSP7_2 GP_PDM_0B QDSS_TRDATA_15A	P3	B-PD:nppukp B DO DO	Configurable I/O BLSP #7, bit 2; SPI, UART, or UIM General-purpose PDM output 0 B QDSS trace data bit 15 A
BE47	GPIO_53	BLSP7_3	P3	B-PD:nppukp	Configurable I/O

Pad #	Pad name	Configurable function	Pad characteristics[1]		Functional description
			Voltage	Type	
		QDSS_TRDATA_14A		B DO	BLSP #7, bit 3; SPI, UART, or UIM QDSS trace data bit 14 A
BD50	GPIO_52	BLSP9_0 UIM3_PRESENT BLSP10_SPI_CS2A_N	P3	B-PD:nppukp B DI DO-Z	Configurable I/O BLSP #9, bit 0; SPI, UART, or I2C UIM3 presence detection Chip select 2A for SPI on BLSP #10
BD52	GPIO_51	BLSP9_1 UIM3_RESET BLSP10_SPI_CS1A_N	P3	B-PD:nppukp B DO DO-Z	Configurable I/O BLSP #9, bit 1; SPI, UART, or I2C UIM3 reset Chip select 1A for SPI on BLSP #10
BE51	GPIO_50	BLSP9_2 UIM3_CLK BLSP10_SPI_CS2B_N	P3	B-PD:nppukp B DO DO-Z	Configurable I/O BLSP #9, bit 2; SPI, UART, or UIM UIM3 clock Chip select 2B for SPI on BLSP #10
BE49	GPIO_49	BLSP9_3 UIM3_DATA BLSP10_SPI_CS1B_N	P3	B-PD:nppukp B B DO-Z	Configurable I/O BLSP #9, bit 3; SPI, UART, or UIM UIM3 data Chip select 1B for SPI on BLSP #10
L7	GPIO_48	BLSP3_0	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 0; SPI, UART, or I2C
K6	GPIO_47	BLSP3_1	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 1; SPI, UART, or I2C
J7	GPIO_46	BLSP3_2	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 2; SPI, UART, or UIM
J5	GPIO_45	BLSP3_3	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 3; SPI, UART, or UIM
H4	GPIO_44	BLSP2_0	P3	B-PD:nppukp B	Configurable I/O BLSP #2, bit 0; SPI, UART, or I2C
G3	GPIO_43	BLSP2_1	P3	B-PD:nppukp B	Configurable I/O BLSP #2, bit 1; SPI, UART, or I2C
F2	GPIO_42	BLSP2_2 QDSS_CTI_TRIG_IN_C	P3	B-PD:nppukp B DI	Configurable I/O BLSP #2, bit 2; SPI, UART, or UIM QDSS trigger input C
F4	GPIO_41	BLSP2_3 QDSS_CTI_TRIG_OUT_C	P3	B-PD:nppukp B DO	Configurable I/O BLSP #2, bit 3; SPI, UART, or UIM QDSS trigger output C
AA1	GPIO_40	SD_WRITE_PROTECT	P3	B-PD:nppukp	Configurable I/O

Pad #	Pad name	Configurable function	Pad characteristics[1]		Functional description
			Voltage	Type	
		TSIF1_ERROR		DI DI	Secure digital card write protection Transport stream interface 1 error
AB2	GPIO_39	TSIF1_SYNC	P3	B-PD:nppukp DI	Configurable I/O Transport stream interface 1 sync
BJ47	GPIO_38	–	P3	B-PD:nppukp	Configurable I/O
E1	GPIO_37	–	P3	B-PD:nppukp	Configurable I/O
D2	GPIO_36	PCIE0_CLKREQ_N	P3	B-PU:nppukp DI	Configurable I/O PCIe 0 clock request
E3	GPIO_35	PCIE0_RST_N	P3	B-PD:nppukp DO	Configura ble I/O PCIe 0 reset
BG45	GPIO_34	HDMI_HOT_PLUG_DET	P3	B-PD:nppukp DI	Configurable I/O HDMI hot plug detect
BH42	GPIO_33	HDMI_DDC_DATA	P3	B-PU:nppdkp B	Configurable I/O HDMI display data channel – data
BH44	GPIO_32	HDMI_DDC_CLK	P3	B-PU:nppdkp B	Configurable I/O HDMI display data channel – clock
BH46	GPIO_31	HDMI_CEC	P3	B-PU:nppdkp B	Configurable I/O HDMI consumer electronics control
M4	GPIO_30	HDMI_RCV_DET BLSP2_SPI_CS3_N	P3	B-PD:nppukp DO DO-Z	Configurable I/O HDMI receive detection Chip select 3 for SPI on BLSP #2
BG3	GPIO_29	GP_MN BLSP2_SPI_CS2_N QDSS_TRDATA_13B	P3	B-PD:nppukp DO DO-Z DO	Configurable I/O General-purpose M/N:D counter output Chip select 2 for SPI on BLSP #2 QDSS trace data bit 13 B
B6	GPIO_28	BLSP6_0 BLSP1_SPI_CS2B_N QDSS_TRCLK_A	P3	B-PD:nppukp B DO- Z DO	Configurable I/O BLSP #6, bit 0; SPI, UART, or I2C Chip select 2B for SPI on BLSP #1 QDSS trace clock A
C5	GPIO_27	BLSP6_1 BLSP1_SPI_CS3A_N QDSS_TRCTL_A	P3	B-PD:nppukp B DO- Z DO	Configurable I/O BLSP #6, bit 1; SPI, UART, or I2C Chip select 3A for SPI on BLSP #1 QDSS trace control A
D4	GPIO_26	BLSP6_2 CCI_ASYNC0	P3	B-PD:nppukp	Configurable I/O

Pad #	Pad name	Configurable function	Pad characteristics[1]		Functional description
			Voltage	Type	
		QDSS_TRDATA_12B		B DI DO	BLSP #6, bit 2; SPI, UART, or UIM Camera control interface async 0 QDSS trace data bit 12 B
F6	GPIO_25	BLSP6_3 CCI_TIMER4 CCI_ASYNC2 BLSP2_SPI_CS1_N QDSS_CTI_TRIG_OUT_A	P3	B-PD:nppukp B DO DI DO-Z DO	Configurable I/O BLSP #6, bit 3; SPI, UART, or UIM Camera control interface timer 4 Camera control interface async 2 Chip select 1 for SPI on BLSP #2 QDSS trigger output A
M6	GPIO_24	CCI_TIMER3 CCI_ASYNC1 BLSP1_SPI_CS2A_N QDSS_CTI_TRIG_IN_A	P3	B-PD:nppukp DO DI DO-Z DI	Configurable I/O Camera control interface timer 3 Camera control interface async 1 Chip select 2A for SPI on BLSP #1 QDSS trigger input A
L5	GPIO_23	CCI_TIMER2 QDSS_TRDATA_11B BLSP1_SPI_CS3B_N	P3	B-PD:nppukp DO DO DO	Configurable I/O Camera control interface timer 2 QDSS trace data bit 11 B Chip select 3B for SPI on BLSP #1
J3	GPIO_22	CCI_TIMER1 QDSS_TRDATA_10B	P3	B-PD:nppukp DO DO	Configurable I/O Camera control interface timer 1 QDSS trace data bit 10 B
H2	GPIO_21	CCI_TIMER0 QDSS_TRDATA_9B	P3	B-PD:nppukp DO DO	Configurable I/O Camera control interface timer 0 QDSS trace data bit 9 B
BF6	GPIO_20	CCI_I2C1_SCL	P3	B-PD:nppukp B	Configurable I/O Dedicated camera control interface I2C 1 clock
BF10	GPIO_19	CCI_I2C1_SDA QDSS_TRDATA_8B DEBUG_OUT_CLK	P3	B-PD:nppukp B DO DO	Configurable I/O Dedicated camera control interface I2C 1 serial data QDSS trace data bit 8 B Test debug clock
BG7	GPIO_18	CCI_I2C0_SCL QDSS_TRDATA_7B	P3	B-PD:nppukp B DO	Configurable I/O Dedicated camera control interface I2C 0 clock QDSS trace data bit 7 B
BF12	GPIO_17	CCI_I2C0_SDA QDSS_TRDATA_6B	P3	B-PD:nppukp B	Configurable I/O Dedicated camera control interface I2C 0 serial data

Pad #	Pad name	Configurable function	Pad characteristics[1]		Functional description
			Voltage	Type	
				DO	QDSS trace data bit 6 B
BG5	GPIO_16	CAM_MCLK3 QDSS_TRDATA_5B	P3	B-PD:nppukp DO DO	Configurable I/O Camera master clock 3 QDSS trace data bit 5 B
BF8	GPIO_15	CAM_MCLK2 QDSS_TRDATA_4B	P3	B-PD:nppukp DO DO	Configurable I/O Camera master clock 2 QDSS trace data bit 4 B
BE7	GPIO_14	CAM_MCLK1 QDSS_TRDATA_3B	P3	B-PD:nppukp DO DO	Configurable I/O Camera master clock 1 QDSS trace data bit 3 B
BF4	GPIO_13	CAM_MCLK0 QDSS_TRDATA_2B	P3	B-PD:nppukp DO DO	Configurable I/O Camera master clock 0 QDSS trace data bit 2 B
BJ45	GPIO_12	MDP_VSYNC_E	P3	B-PD:nppukp DI	Configurable I/O MDP vertical sync – external
BJ51	GPIO_11	BLSP10_0 MDP_VSYNC_S	P3	B-PD:nppukp B DI	Configurable I/O BLSP #10, bit 0; SPI, UART, or I2C MDP vertical sync – secondary
BH50	GPIO_10	BLSP10_1 MDP_VSYNC_P	P3	B-PD:nppukp B DI	Configurable I/O BLSP #10, bit 1; SPI, UART, or I2C MDP vertical sync – primary
BG51	GPIO_9	BLSP10_2	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 2; SPI, UART, or UIM
BF50	GPIO_8	BLSP10_3 GP_PDM_1B	P3	B-PD:nppukp B DO	Configurable I/O BLSP #10, bit 3; SPI, UART, or UIM General-purpose PDM output 1 B
BB50	GPIO_7	BLSP8_0	P3	B-PD:nppukp B	Configurable I/O BLSP #8, bit 0; SPI, UART, or I2C
BC51	GPIO_6	BLSP8_1	P3	B-PD:nppukp B	Configurable I/O BLSP #8, bit 1; SPI, UART, or I2C
BB48	GPIO_5	BLSP8_2 QDSS_CTI_TRIG_IN_B	P3	B-PD:nppukp B DI	Configurable I/O BLSP #8, bit 2; SPI, UART, or UIM QDSS trigger input B

Pad #	Pad name	Configurable function	Pad characteristics[1]		Functional description
			Voltage	Type	
BA49	GPIO_4	BLSP8_3 QDSS_CTI_TRIG_OUT_B	P3	B-PD:nppukp B DO	Configurable I/O BLSP #8, bit 3; SPI, UART, or UIM QDSS trigger output B
H8	GPIO_3	BLSP1_0	P3	B-PD:nppukp B	Configurable I/O BLSP #1, bit 0; SPI, UART, or I2C
H6	GPIO_2	BLSP1_1	P3	B-PD:nppukp B	Configurable I/O BLSP #1, bit 1; SPI, UART, or I2C
G7	GPIO_1	BLSP1_2	P3	B-PD:nppukp B	Configurable I/O BLSP #1, bit 2; SPI, UART, or UIM
G5	GPIO_0	BLSP1_3	P3	B-PD:nppukp B	Configurable I/O BLSP #1, bit 3; SPI, UART, or UIM

1. See Table 7 for parameter and acronym definitions.

Table 18 Pin descriptions – general-purpose input/output ports

Pad #	Pad name	Functional description
C15, C21, C47, D16, D22, D48, U7, W7, AA47, AG51, AH52, AJ45, AL5, AM4, AR43, AT6, AU1, AT2, AY46, AY50, BF24, BF52, BH2, BJ3, BK10	DNC	Do not connect; connected internally, do not connect externally
A21, A45, B18, B20, B42, B44, B46, B48, B50, C17, C19, C41, C43, C45, C49, D18, D20, D42, D44, D46, E19, E43, BB26, BD16, BD26, BD40, BE25, BF14, BF18, BF36, BF38, BF46, BG9, BG13, BG15, BG17, BG19, BG25, BG27, BG29, BG39, BH14, BH18, BH26, BH28, BH30, BJ17, BJ19, BJ21, BJ25, BJ27, BJ29, BJ31, BK22, BK26, BK30	NC	No connect; not connected internally
AP4, AP6, AR3, AR7, AT8	RSVD	Reserved; connected internally for potential future use, do not connect externally

Table 19 Pin descriptions – no connection, do not connect, and reserved pins

Pad #	Pad name	Functional description
F48, H48, K48, M48, P48, U47	VDD_A1	Power for analog circuits – low voltage
G47, J47, L47, N47, R47, V46, AB48, AC47, AE47	VDD_A2	Power for analog circuits – high voltage
D28	VDD_ALWAYS_ON	Always-on power domain
L9, L11, L13, L15, L17, L19, R9, R11, R13, R17, R19, R21, W9, W11,	VDD_APC	Power for Kryo application

Pad #	Pad name	Functional description
W13, W15, W17, W19, W21, AC9, AC11, AC16, AC21, AG9, AG11, AG16, AG21		processor
F12, J25, L21, L23, L37, L39, N7, R25, R27, R29, V8, W25, W27, W29, AC25, AC27, AC29, AC37, AC39, AC41, AC43, AG23, AG25, AG31, AG33, AG43, AG45, AL11, AL13, AL15, AL17, AL19, AL25, AL27, AR13, AR15, AR21, AR23, AR27, AR29, AW9, AW11, AW17, AW19, AW25, AW27, BA37, BA45	VDD_CORE	Power for digital core circuits
B12, B14, B32, B34, BJ13, BJ15, BJ39, BJ43	VDD_DDR_CORE_1P2	Power for PoP DDR memory core – 1.2V (top VDD_2)
A13, A17, A37, A41, BJ41, BK14, BK18, BK42	VDD_DDR_CORE_1P8	Power for PoP DDR memory core – 1.8 V (top VDD_1)
H14, H16, H18, H20, H22, H24, H34, H36, H38, H40, H42, H44, BC11, BC13, BC15, BC17, BC19, BC21, BC35, BC37, BC39, BC41, BC43, BC45	VDD_EBI_IO	Power for EBI I/O circuits
B16, D40, BH16, BH40	VDD_EBI_IO_ISO	Power for EBI I/O circuits that need isolated routing on the PCB
H28, H30, J15, J19, J23, J33, J37, J41, BB12, BB16, BB20, BB28, BB36, BB40, BB44, BC27	VDD_EBI_PHY	Power for EBI PHY circuits
AG35, AG37, AG39, AG41, AP37, AP39, AR31, AR33, AR35, AW31, AW33, AW35, AW41, AW43	VDD_GFX	Power for graphics
BC25	VDD_HDMI1	Power for HDMI circuits – low voltage
BC23, BD24	VDD_HDMI2	Power for HDMI circuits – high voltage
H10, L31, L43, N45, R7, R15, R23, R35, R37, U27, U29, W23, W37, W39, Y46, AC7, AC23, AC33, AC35, AE16, AG27, AG29, AL21, AL23, AL29, AL31, AL33, AL35, AL43, AL45, AP41, AR9, AR11, AR17, AR19, AU45, AW13, AW15, AW21, AW23, AW29, AW37, AW39	VDD_MEM	Power for on-chip memory
BB8, BD8, BE9	VDD_MIPI_CSI	Power for MIPI_CSI I/Os and circuits
BC33, BD32	VDD_MIPI_DSI	Reference for MIPI_DSI I/Os and circuits
L33, L35, L41, R31, R33, R39, R41, R43, W31, W33, W35, W41, W43	VDD_MODEM	Power for modem circuits, including the modem DSP
A5, A33, A49, B22, BJ35, BK6, BK24, BK46	VDD_P1	Power for pad group 1 – EBI and DDR I/O pads
AH8	VDD_P2	Power for pad group 2 – SDC2 pads
E35, E47, F44, G15, G23, G33, G41, P6, Y6, AG47, AJ9, AN45, AW45, BD12, BD20, BD36, BD44	VDD_P3	Power for pad group 3 – most I/O pads
F24	VDD_P5	Power for pad group 5 – UIM1 pads
G25	VDD_P6	Power for pad group 6 – UIM2 pads
AF8	VDD_P7	Power for pad group 7 – SDC1 pads
BA9	VDD_P9	Power for pad group 9 – CXO_2 pad

Pad #	Pad name	Functional description
AW5	VDD_P10	Power for pad group 10 – UFS pad
G45	VDD_P11	Power for pad group 11 – CXO pad
E27	VDD_P12	Power for pad group 12 – SSC pad
AM6	VDD_PCIE_1P8	Power for PCIe I/O circuitry
AK8, AL7	VDD_PCIE_CORE	Power for PCIe core circuitry
BB32, BB34	VDD_PLL1	Power for PLL circuits – 0.925 V
F28, BA27	VDD_PLL1_ISO	Power for PLL circuits – 0.925 V that need isolated routing on the PCB
E29, BC29	VDD_PLL2	Power for PLL circuits – 1.250 V
BC31, BD34	VDD_PLL2_ISO	Power for PLL circuits – 1.250 V that need isolated routing on the PCB
U45, AC31, AR25, BD22	VDD_PLL3	Power for PLL circuits – 1.800 V
G31	VDD_QFPROM_PRG	Power for programming the QFPROM; otherwise, ground
J29, L25, L27, L29	VDD_SSC_CORE	Power for Snapdragon sensor core
N29	VDD_SSC_MEM	Power for Snapdragon sensor core memory
AY8	VDD_UFS_1P8	Power for UFS 1.8 V circuits
AV8, AW7	VDD_UFS_CORE	Power for UFS core circuits
AA7, AN7	VDD_USB_1P8	Power for USB HS1, HS2, and SS – low voltage
AB8	VDD_USB_HS_3P1	Power for USB HS1 and HS2 – high voltage
AB6	VDD_USB_HS_CORE	Power for USB digital core circuits – HS1, HS2
AP8	VDD_USB_SS_CORE	Power for USB digital core circuits – SS1
M8	VREF_APC	Reference voltage for Kryo application processor

Table 20 Pin descriptions – power supply pins

Pad #	Pad name	Functional description
A1, A3, A7, A11, A15, A19, A23, A27, A31, A35, A39, A43, A47, A51, B40, B52, C1, C51, D50, D52, E15, F14, F16, F18, F20, F22, F30, F32, F34, F36, F38, F40, F42, F52, G1, G13, G17, G19, G21, G35, G37, G39, G43, G49, H12, H32, H46, H50, J9, J11, J13, J17, J21, J27, J31, J35, J39, J43, J45, J49, K8, K46, K52, L1, L45, L49, M46, M50, N9, N11, N13, N15, N17, N19, N21, N23, N25, N27, N31, N33, N35, N37, N39, N41, N43, N49, P8, P46, P52, R1, R45, R49, T8, U9, U11, U13, U15, U17, U19, U21, U23, U25, U31, U33, U35, U37, U39, U41, U43, V50, V52, W1, W45, Y8, AA9, AA11, AA13, AA15, AA17, AA19, AA21, AA23, AA25, AA27, AA29, AA31, AA33, AA35, AA37, AA39, AA41, AA43, AA45, AB46, AB52, AC1, AC45, AD46, AE9, AE11, AE21, AE23, AE25, AE27, AE29, AE31, AE33, AE35, AE37, AE39, AE41, AE43, AE45, AE49, AF46, AF48, AF50, AF52, AG1, AG49, AJ11, AJ13, AJ15, AJ17, AJ19, AJ21, AJ23, AJ25, AJ27, AJ29, AJ31, AJ33, AJ35, AJ37, AJ39, AJ41, AJ43, AK52, AL1, AL9, AN9, AN11, AN13, AN15, AN17, AN19, AN21, AN23, AN25, AN27, AN29, AN31, AN33, AN35, AN43, AP52, AR1, AU9, AU11, AU13, AU15, AU17, AU19, AU21, AU23, AU25, AU27, AU29, AU31, AU33, AU35, AU43, AV52, AW1, BA11, BA13, BA15, BA17, BA19, BA21, BA23, BA25, BA29, BA31, BA33, BA35, BA39, BA41, BA43, BB10, BB14, BB18, BB22, BB24, BB30, BB38, BB42, BB52, BC1, BC9, BD10, BD14, BD18, BD38, BD42, BE11, BE13, BE15, BE17, BE19, BE35, BE37, BE39, BE41, BE43, BE45, BF26, BG1, BH52, BJ1, BK2, BK4, BK8, BK12, BK16, BK20, BK28, BK32, BK36, BK40, BK44, BK48, BK50, BK52	GND	Ground

Table 21 Pin descriptions – ground pins

7.4 Pin assignments – APQ8096 top

The APQ8096 is available in the 994B MNSP package. Its top surface is implemented like a 387-pin chip-scale package (387 CSP). See Section 7.2 for information about the bottom pin assignments. A high-level view of the top pin assignments is shown in Figure 8 High-level view of APQ8096 top pin assignments. The pins are color coded to indicate which function type they support, as defined in Figure 7.

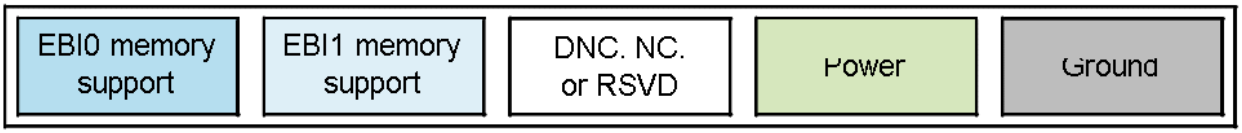


Figure 7 APQ8096 top pin assignments – legend

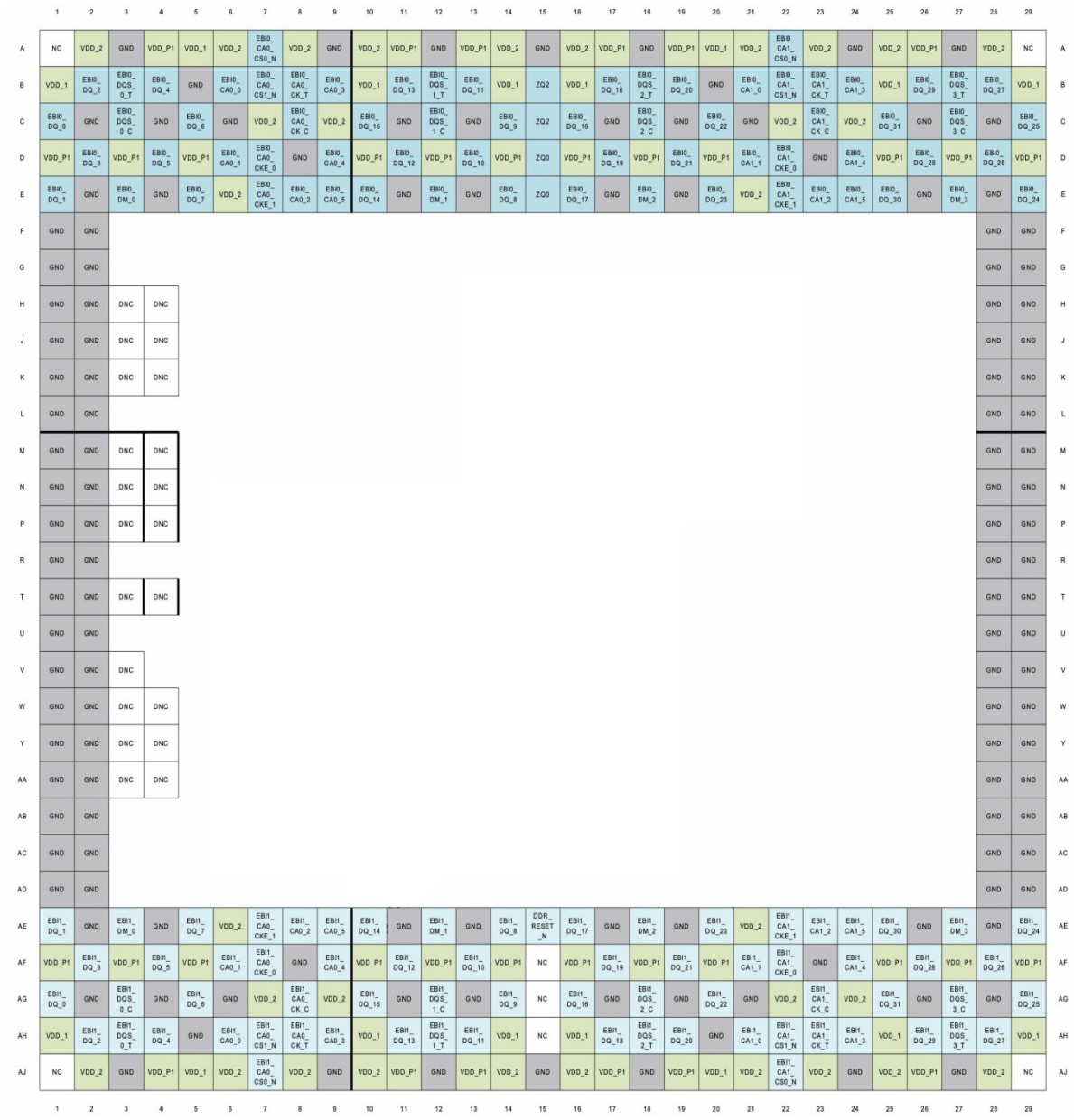


Figure 8 High-level view of APQ8096 top pin assignments

7.5 Pin descriptions – APQ8096 top

Descriptions of top pins are presented in the following tables, organized by functional group:

Table 23 Pin descriptions – no connection, do not connect, and reserved pins

Table 24 Pin descriptions – power supply pins

Table 25 Pin descriptions – ground pins

Pad #	Pad name and/or function	Pad name or alt function	1		Functional description
			Voltage	Type	
EBI0					
E9	EBI0_CA0_5	–	P1	DO	EBI0 LPDDR4 command/address 0 bit 5
D9	EBI0_CA0_4	–	P1	DO	EBI0 LPDDR4 command/address 0 bit 4
B9	EBI0_CA0_3	–	P1	DO	EBI0 LPDDR4 command/address 0 bit 3
E8	EBI0_CA0_2	–	P1	DO	EBI0 LPDDR4 command/address 0 bit 2
D6	EBI0_CA0_1	–	P1	DO	EBI0 LPDDR4 command/address 0 bit 1
B6	EBI0_CA0_0	–	P1	DO	EBI0 LPDDR4 command/address 0 bit 0
E24	EBI0_CA1_5	–	P1	DO	EBI0 LPDDR4 command/address 1 bit 5
D24	EBI0_CA1_4	–	P1	DO	EBI0 LPDDR4 command/address 1 bit 4
B24	EBI0_CA1_3	–	P1	DO	EBI0 LPDDR4 command/address 1 bit 3
E23	EBI0_CA1_2	–	P1	DO	EBI0 LPDDR4 command/address 1 bit 2
D21	EBI0_CA1_1	–	P1	DO	EBI0 LPDDR4 command/address 1 bit 1
B21	EBI0_CA1_0	–	P1	DO	EBI0 LPDDR4 command/address 1 bit 0
C25	EBI0_DQ_31	–	P1	B	EBI0 LPDDR4 data bit 31
E25	EBI0_DQ_30	–	P1	B	EBI0 LPDDR4 data bit 30
B26	EBI0_DQ_29	–	P1	B	EBI0 LPDDR4 data bit 29
D26	EBI0_DQ_28	–	P1	B	EBI0 LPDDR4 data bit 28
B28	EBI0_DQ_27	–	P1	B	EBI0 LPDDR4 data bit 27
D28	EBI0_DQ_26	–	P1	B	EBI0 LPDDR4 data bit 26
C29	EBI0_DQ_25	–	P1	B	EBI0 LPDDR4 data bit 25
E29	EBI0_DQ_24	–	P1	B	EBI0 LPDDR4 data bit 24
E20	EBI0_DQ_23	–	P1	B	EBI0 LPDDR4 data bit 23
C20	EBI0_DQ_22	–	P1	B	EBI0 LPDDR4 data bit 22
D19	EBI0_DQ_21	–	P1	B	EBI0 LPDDR4 data bit 21
B19	EBI0_DQ_20	–	P1	B	EBI0 LPDDR4 data bit 20
D17	EBI0_DQ_19	–	P1	B	EBI0 LPDDR4 data bit 19
B17	EBI0_DQ_18	–	P1	B	EBI0 LPDDR4 data bit 18
E16	EBI0_DQ_17	–	P1	B	EBI0 LPDDR4 data bit 17
C16	EBI0_DQ_16	–	P1	B	EBI0 LPDDR4 data bit 16
C10	EBI0_DQ_15	–	P1	B	EBI0 LPDDR4 data bit 15
E10	EBI0_DQ_14	–	P1	B	EBI0 LPDDR4 data bit 14

B11	EBI0_DQ_13	–	P1	B	EBI0 LPDDR4 data bit 13
D11	EBI0_DQ_12	–	P1	B	EBI0 LPDDR4 data bit 12
B13	EBI0_DQ_11	–	P1	B	EBI0 LPDDR4 data bit 11
D13	EBI0_DQ_10	–	P1	B	EBI0 LPDDR4 data bit 10
C14	EBI0_DQ_9	–	P1	B	EBI0 LPDDR4 data bit 9
E14	EBI0_DQ_8	–	P1	B	EBI0 LPDDR4 data bit 8
E5	EBI0_DQ_7	–	P1	B	EBI0 LPDDR4 data bit 7
C5	EBI0_DQ_6	–	P1	B	EBI0 LPDDR4 data bit 6
D4	EBI0_DQ_5	–	P1	B	EBI0 LPDDR4 data bit 5
B4	EBI0_DQ_4	–	P1	B	EBI0 LPDDR4 data bit 4
D2	EBI0_DQ_3	–	P1	B	EBI0 LPDDR4 data bit 3
B2	EBI0_DQ_2	–	P1	B	EBI0 LPDDR4 data bit 2
E1	EBI0_DQ_1	–	P1	B	EBI0 LPDDR4 data bit 1
C1	EBI0_DQ_0	–	P1	B	EBI0 LPDDR4 data bit 0
C8	EBI0_CA0_CK_C	–	P1	DO	EBI0 CA0 LPDDR4 differential clock (C)
B8	EBI0_CA0_CK_T	–	P1	DO	EBI0 CA0 LPDDR4 differential clock (T)
E7	EBI0_CA0_CKE_1	–	P1	DO	EBI0 CA0 LPDDR4 clock enable 1
D7	EBI0_CA0_CKE_0	–	P1	DO	EBI0 CA0 LPDDR4 clock enable 0
B7	EBI0_CA0_CS1_N	–	P1	DO	EBI0 CA0 LPDDR4 chip select 1
A7	EBI0_CA0_CS0_N	–	P1	DO	EBI0 CA0 LPDDR4 chip select 0
C23	EBI0_CA1_CK_C	–	P1	DO	EBI0 CA1 LPDDR4 differential clock (C)
B23	EBI0_CA1_CK_T	–	P1	DO	EBI0 CA1 LPDDR4 differential clock (T)
E22	EBI0_CA1_CKE_1	–	P1	DO	EBI0 CA1 LPDDR4 clock enable 1
D22	EBI0_CA1_CKE_0	–	P1	DO	EBI0 CA1 LPDDR4 clock enable 0
B22	EBI0_CA1_CS1_N	–	P1	DO	EBI0 CA1 LPDDR4 chip select 1
A22	EBI0_CA1_CS0_N	–	P1	DO	EBI0 CA1 LPDDR4 chip select 0
C27	EBI0_DQS_3_C	–	P1	B	EBI0 LPDDR4 differential data strobe for byte 3 (C)
B27	EBI0_DQS_3_T	–	P1	B	EBI0 LPDDR4 differential data strobe for byte 3 (T)
C18	EBI0_DQS_2_C	–	P1	B	EBI0 LPDDR4 differential data strobe for byte 2 (C)
B18	EBI0_DQS_2_T	–	P1	B	EBI0 LPDDR4 differential data strobe for byte 2 (T)
C12	EBI0_DQS_1_C	–	P1	B	EBI0 LPDDR4 differential data strobe for byte 1 (C)
B12	EBI0_DQS_1_T	–	P1	B	EBI0 LPDDR4 differential data strobe for byte 1 (T)
C3	EBI0_DQS_0_C	–	P1	B	EBI0 LPDDR4 differential data strobe for byte 0 (C)
B3	EBI0_DQS_0_T	–	P1	B	EBI0 LPDDR4 differential data strobe for byte 0 (T)
E27	EBI0_DM_3	–	P1	DO	EBI0 LPDDR4 data mask for byte 3
E18	EBI0_DM_2	–	P1	DO	EBI0 LPDDR4 data mask for byte 2
E12	EBI0_DM_1	–	P1	DO	EBI0 LPDDR4 data mask for byte 1
E3	EBI0_DM_0	–	P1	DO	EBI0 LPDDR4 data mask for byte 0

D15, E15	ZQ0	–	–	AI	LPDDR4 ZQ resistor, lower x16 memory (shared by EBIs)
B15, C15	ZQ2	–	–	AI	LPDDR4 ZQ resistor, upper x16 memory (shared by EBIs)
EBI1					
AE9	EBI1_CA0_5	–	P1	DO	EBI1 LPDDR4 command/address 0 bit 5
AF9	EBI1_CA0_4	–	P1	DO	EBI1 LPDDR4 command/address 0 bit 4
AH9	EBI1_CA0_3	–	P1	DO	EBI1 LPDDR4 command/address 0 bit 3
AE8	EBI1_CA0_2	–	P1	DO	EBI1 LPDDR4 command/address 0 bit 2
AF6	EBI1_CA0_1	–	P1	DO	EBI1 LPDDR4 command/address 0 bit 1
AH6	EBI1_CA0_0	–	P1	DO	EBI1 LPDDR4 command/address 0 bit 0
AE24	EBI1_CA1_5	–	P1	DO	EBI1 LPDDR4 command/address 1 bit 5
AF24	EBI1_CA1_4	–	P1	DO	EBI1 LPDDR4 command/address 1 bit 4
AH24	EBI1_CA1_3	–	P1	DO	EBI1 LPDDR4 command/address 1 bit 3
AE23	EBI1_CA1_2	–	P1	DO	EBI1 LPDDR4 command/address 1 bit 2
AF21	EBI1_CA1_1	–	P1	DO	EBI1 LPDDR4 command/address 1 bit 1
AH21	EBI1_CA1_0	–	P1	DO	EBI1 LPDDR4 command/address 1 bit 0
AG25	EBI1_DQ_31	–	P1	B	EBI1 LPDDR4 data bit 31
AE25	EBI1_DQ_30	–	P1	B	EBI1 LPDDR4 data bit 30
AH26	EBI1_DQ_29	–	P1	B	EBI1 LPDDR4 data bit 29
AF26	EBI1_DQ_28	–	P1	B	EBI1 LPDDR4 data bit 28
AH28	EBI1_DQ_27	–	P1	B	EBI1 LPDDR4 data bit 27
AF28	EBI1_DQ_26	–	P1	B	EBI1 LPDDR4 data bit 26
AG29	EBI1_DQ_25	–	P1	B	EBI1 LPDDR4 data bit 25
AE29	EBI1_DQ_24	–	P1	B	EBI1 LPDDR4 data bit 24
AE20	EBI1_DQ_23	–	P1	B	EBI1 LPDDR4 data bit 23
AG20	EBI1_DQ_22	–	P1	B	EBI1 LPDDR4 data bit 22
AF19	EBI1_DQ_21	–	P1	B	EBI1 LPDDR4 data bit 21
AH19	EBI1_DQ_20	–	P1	B	EBI1 LPDDR4 data bit 20
AF17	EBI1_DQ_19	–	P1	B	EBI1 LPDDR4 data bit 19
AH17	EBI1_DQ_18	–	P1	B	EBI1 LPDDR4 data bit 18
AE16	EBI1_DQ_17	–	P1	B	EBI1 LPDDR4 data bit 17
AG16	EBI1_DQ_16	–	P1	B	EBI1 LPDDR4 data bit 16
AG10	EBI1_DQ_15	–	P1	B	EBI1 LPDDR4 data bit 15
AE10	EBI1_DQ_14	–	P1	B	EBI1 LPDDR4 data bit 14
AH11	EBI1_DQ_13	–	P1	B	EBI1 LPDDR4 data bit 13
AF11	EBI1_DQ_12	–	P1	B	EBI1 LPDDR4 data bit 12
AH13	EBI1_DQ_11	–	P1	B	EBI1 LPDDR4 data bit 11
AF13	EBI1_DQ_10	–	P1	B	EBI1 LPDDR4 data bit 10
AG14	EBI1_DQ_9	–	P1	B	EBI1 LPDDR4 data bit 9
AE14	EBI1_DQ_8	–	P1	B	EBI1 LPDDR4 data bit 8
AE5	EBI1_DQ_7	–	P1	B	EBI1 LPDDR4 data bit 7
AG5	EBI1_DQ_6	–	P1	B	EBI1 LPDDR4 data bit 6
AF4	EBI1_DQ_5	–	P1	B	EBI1 LPDDR4 data bit 5
AH4	EBI1_DQ_4	–	P1	B	EBI1 LPDDR4 data bit 4

AF2	EBI1_DQ_3	–	P1	B	EBI1 LPDDR4 data bit 3
AH2	EBI1_DQ_2	–	P1	B	EBI1 LPDDR4 data bit 2
AE1	EBI1_DQ_1	–	P1	B	EBI1 LPDDR4 data bit 1
AG1	EBI1_DQ_0	–	P1	B	EBI1 LPDDR4 data bit 0
AG8	EBI1_CA0_CK_C	–	P1	DO	EBI1 CA0 LPDDR4 differential clock (C)
AH8	EBI1_CA0_CK_T	–	P1	DO	EBI1 CA0 LPDDR4 differential clock (T)
AE7	EBI1_CA0_CKE_1	–	P1	DO	EBI1 CA0 LPDDR4 clock enable 1
AF7	EBI1_CA0_CKE_0	–	P1	DO	EBI1 CA0 LPDDR4 clock enable 0
AH7	EBI1_CA0_CS1_N	–	P1	DO	EBI1 CA0 LPDDR4 chip select 1
AJ7	EBI1_CA0_CS0_N	–	P1	DO	EBI1 CA0 LPDDR4 chip select 0
AG23	EBI1_CA1_CK_C	–	P1	DO	EBI1 CA1 LPDDR4 differential clock (C)
AH23	EBI1_CA1_CK_T	–	P1	DO	EBI1 CA1 LPDDR4 differential clock (T)
AE22	EBI1_CA1_CKE_1	–	P1	DO	EBI1 CA1 LPDDR4 clock enable 1
AF22	EBI1_CA1_CKE_0	–	P1	DO	EBI1 CA1 LPDDR4 clock enable 0
AH22	EBI1_CA1_CS1_N	–	P1	DO	EBI1 CA1 LPDDR4 chip select 1
AJ22	EBI1_CA1_CS0_N	–	P1	DO	EBI1 CA1 LPDDR4 chip select 0
AG27	EBI1_DQS_3_C	–	P1	B	EBI1 LPDDR4 differential data strobe for byte 3 (C)
AH27	EBI1_DQS_3_T	–	P1	B	EBI1 LPDDR4 differential data strobe for byte 3 (T)
AG18	EBI1_DQS_2_C	–	P1	B	EBI1 LPDDR4 differential data strobe for byte 2 (C)
AH18	EBI1_DQS_2_T	–	P1	B	EBI1 LPDDR4 differential data strobe for byte 2 (T)
AG12	EBI1_DQS_1_C	–	P1	B	EBI1 LPDDR4 differential data strobe for byte 1 (C)
AH12	EBI1_DQS_1_T	–	P1	B	EBI1 LPDDR4 differential data strobe for byte 1 (T)
AG3	EBI1_DQS_0_C	–	P1	B	EBI1 LPDDR4 differential data strobe for byte 0 (C)
AH3	EBI1_DQS_0_T	–	P1	B	EBI1 LPDDR4 differential data strobe for byte 0 (R)
AE27	EBI1_DM_3	–	P1	DO	EBI1 LPDDR4 data mask for byte 3
AE18	EBI1_DM_2	–	P1	DO	EBI1 LPDDR4 data mask for byte 2
AE12	EBI1_DM_1	–	P1	DO	EBI1 LPDDR4 data mask for byte 1
AE3	EBI1_DM_0	–	P1	DO	EBI1 LPDDR4 data mask for byte 0
AE15	DDR_RESET_N	–	P1	DO	LPDDR4 reset (shared by EBIs)

1. See Table 7 for parameter and acronym definitions.

Table 22 Pin descriptions – memory support functions

Pad #	Pad name	Functional description
H3, H4, J3, J3, J4, J4, K3, K3, K4, K4, M3, M3, M4, M4, N3, N3, N4, N4, P3, P3, P4, P4, T3, T3, T4, T4, V3, V3, W3, W3, W4, W4, Y3, Y4, AA3, AA3, AA4, AA4	DNC	Do not connect; connected internally, do not connect externally
A1, A29, AF15, AG15, AH15, AJ1, AJ29	NC	No connect; not connected internally.
–	RSVD	Reserved

Table 23 Pin descriptions – no connection, do not connect, and reserved pins

Pad #	Pad name	Functional description
A5, A20, B1, B10, B14, B16, B25, B29, AH1, AH10, AH14, AH16, AH25, AH29, AJ5, AJ20	VDD_1	Power for memory core (bottom VDD_DDR_CORE_1P8)
A2, A6, A8, A10, A14, A16, A21, A23, A25, A28, C7, C9, C22, C24, E6, E21, AE6, AE21, AG7, AG9, AG22, AG24, AJ2, AJ6, AJ8, AJ10, AJ14, AJ16, AJ21, AJ23, AJ25, AJ28	VDD_2	Power for memory core (bottom VDD_DDR_CORE_1P2)
A4, A11, A13, A17, A19, A26, D1, D3, D5, D10, D12, D14, D16, D18, D20, D25, D27, D29, AF1, AF3, AF5, AF10, AF12, AF14, AF16, AF18, AF20, AF25, AF27, AF29, AJ4, AJ11, AJ13, AJ17, AJ19, AJ26	VDD_P1	Power for memory I/O pads

Table 24 Pin descriptions – power supply pins

Pad #	Pad name	Functional description
A3, A9, A123, A15, A18, A24, A27, B5, B20, C2, C4, C6, C11, C13, C17, C19, C21, C26, C28, D8, D23, E2, E4, E11, E13, E17, E19, E26, E28, F1, F2, F28, F29, G1, G2, G28, G29, H1, H2, H28, H29, J1, J2, J28, J29, K1, K2, K28, K29, L1, L2, L28, L29, M1, M2, M28, M29, N1, N2, N28, N29, P1, P2, P28, P29, R1, R2, R28, R29, T1, T2, T28, T29, U1, U2, U28, U29, V1, V2, V28, V29, W1, W2, W28, W29, Y1, Y2, Y28, Y29, AA1, AA2, AA28, AA29, AB1, AB2, AB28, AB29, AC1, AC2, AC28, AC29, AD1, AD2, AD28, AD29, AE2, AE4, AE11, AE13, AE17, AE19, AE26, AE28, AF8, AF23, AG2, AG4, AG6, AG11, AG13, AG17, AG19, AG21, AG26, AG28, AH5, AH20, AJ3, AJ9, AJ12, AJ15, AJ18, AJ24, AJ27	GND	Ground

Table 25 Pin descriptions – ground pins

8 Electrical Specifications

8.1 Absolute maximum ratings

The absolute maximum ratings (

Table 26) reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Section 8.2.

Power supply	Description	Min	Max	Unit
VDD_CORE	APQ digital core	-0.3	1.177	V
VDD_MEM	APQ on-chip memory	-0.3	1.177	V
VDD_USB_HS_CORE	Power for USB digital core circuits – HS1, HS2			
VDD_GFX	APQ graphics core	-0.3	1.177	V
VDD_APC	Power for quad Kryo applications microprocessors	-0.3	1.353	V
VDD_MODEM	Power for modem circuits, including the two QDSP6s	-0.3	1.177	V
VDD_A1	Power for analog circuits – low voltage	-0.3	1.43	V
VDD_A2	Power for analog circuits – high voltage	-0.3	2.079	V
VDD_QFPROM_PRG	Power for programming the QFPROM			
VDD_EBI_PHY	Power for EBI PHY circuits	-0.3	1.177	V
VDD_EBI_IO	Power for EBI IO circuits			
VDD_EBI_IO_ISO	Power for EBI I/O circuits that need isolated routing on the PCB			
VDD_SSC_CORE	Power for Snapdragon sensor core	-0.3	1.074	V
VDD_SSC_MEM	Power for Snapdragon sensor core memory	-0.3	1.074	V
Power supply	Description	Min	Max	Unit
VDD_PLL1	Power for PLL circuits – 0.925 V	-0.3	1.051	V
VDD_PLL1_ISO	Power for PLL circuits – 0.925 V that need isolated routing on the PCB			
VDD_HDMI1	Power for HDMI circuits – low voltage			
VDD_PCIE_CORE	Power for PCIe core circuitry			
VDD_UFS_CORE	Power for UFS core circuits			
VDD_USB_SS_CORE	Power for USB digital core circuits – SS			
VDD_PLL2	Power for PLL circuits – 1.250 V	-0.3	1.419	V
VDD_PLL2_ISO	Power for PLL circuits – 1.250 V that need isolated routing on the PCB			
VDD_MIPI_CSI	Power for MIPI_CSI I/Os			
VDD_MIPI_DSI	Reference for MIPI_DSI I/Os and circuits			
VDD_PLL3	Power for PLL circuits – 1.800 V	-0.3	2.09	V
VDD_P9	Power for pad group 9 – CXO_2 pad			
VDD_HDMI2	Power for HDMI circuits – high voltage			

Power supply	Description	Min	Max	Unit
VDD_UFS_1P8	Power for UFS 1.8 V circuits			
VDD_USB_1P8	Power for USB HS1, HS2, and SS – low voltage			
VDD_PCIE_1P8	Power for PCIe I/O circuitry			
VDD_P11	Power for pad group 11 – CXO pad			
VDD_P1	Power for pad group 1 – EBI1 pads and DDR memory I/O pads	-0.3	1.287	V
VDD_DDR_CORE_1P2	Power for PoP DDR memory core – for VDD2			
VDD_P2	Power for pad group 2 – SDC2 pads	-0.3	3.344	V
VDD_P3	Power for pad group 3 – most I/O pads	-0.3	2.09	V
VDD_DDR_CORE_1P8	Power for PoP DDR memory core – for VDD1			
VDD_P7	Power for pad group 7 – SDC1 pads			
VDD_P5	Power for pad group 5 – UIM1 pads	-0.3	3.344	V
VDD_P6	Power for pad group 6 – UIM2 pads	-0.3	3.344	V
VDD_P10	Power for pad group 10 – UFS pad	-0.3	1.375	V
VDD_P12	Power for pad group 12 – SSC pad	-0.3	2.09	V
VDD_USB_HS_3P1	Power for USB HS1 and HS2 – high voltage	-0.3	3.52	V

Table 26 Absolute maximum ratings

8.2 Operating Conditions

Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions (Table 27 and Table 28). The APQ8096 meets all the performance specifications when used within the operating conditions (provided the absolute maximum ratings have never been exceeded).

Parameter [1]		Min	Max	Unit
VDD_CORE	APQ digital core			
	Turbo	0.795	1.07	V
	Nominal	0.705	0.976	V
	SVS	0.59	0.8	V
	Low SVS	0.515	0.717	V
VDD_MEM	APQ on-chip memory			
VDD_USB_HS_CORE	Power for USB digital core circuits – HS1, HS2			
	Turbo	0.795	1.07	V
	Nominal	0.785	1.025	V
	SVS [2]	0.785	0.915	V
	Low SVS [2]	0.785	0.915	V

Parameter [1]		Min	Max	Unit
VDD_GFX	APQ graphics core			
	Turbo	0.795	1.07	V
	Nominal L1	0.744	1.036	V
	Nominal	0.705	0.976	V
	SVS L1	0.643	0.888	V
	SVS	0.59	0.8	V
	Low SVS	0.515	0.717	V
	Min SVS	0.545	0.64	V
VDD_APC	Power for quad Kryo applications microprocessors			
	Turbo	0.79	1.23	V
	Nominal	0.695	0.976	V
	SVS	0.59	0.8	V
	Min SVS	0.54	0.646	V
VDD_MODEM	Power for modem circuits			
	Turbo	0.795	1.07	V
	Nominal	0.705	0.976	V
	SVS	0.59	0.8	V
	Low SVS	0.515	0.717	V
VDD_EBI_PHY	Power for EBI PHY circuits			
VDD_EBI_IO	Power for EBI I/O circuits			
VDD_EBI_IO_ISO	Power for EBI I/O circuits that need isolated routing on the PCB			
	Turbo	0.815	1.07	V
	Nominal	0.7	0.97	V
	SVS	0.675	0.915	V
	Low SVS	0.633	0.778	V
VDD_SSC_CORE	Power for Snapdragon sensor core			
	Turbo	0.795	1.07	V
	Nominal	0.705	0.976	V
	SVS	0.59	0.8	V
	Low SVS	0.515	0.717	V
VDD_SSC_MEM	Power for Snapdragon sensor core memory			
	Turbo	0.795	1.07	V
	Nominal	0.785	1.025	V
	SVS [2]	0.785	0.915	V
	Low SVS [2]	0.785	0.915	V

1. Parts with voltages outside the specified ranges are not guaranteed to operate properly.
2. The voltage setting at the PMIC for SVS and low SVS modes for this core is a static 0.85V. There is no scaling.

Table 27 Operating conditions for voltage rails with AVS Type-1

Parameter		Min	Typ [1]	Max	Unit
Power supply voltages					
VDD_A1	Power for analog circuits – low voltage	1.15	1.225	1.3	V
VDD_A2 VDD_QFPROM_PRG	Power for analog circuits – high voltage Power for programming the QFPROM	1.71	1.8	1.89	V
VDD_PLL1	Power for PLL circuits – 0.925 V	0.885	0.925	0.955	V
VDD_PLL1_ISO	Power for PLL circuits – 0.925 V that need isolated routing on the PCB				
VDD_HDMI1	Power for HDMI circuits – low voltage				
VDD_PCIE_CORE	Power for PCIe core circuitry				
VDD_UFS_CORE	Power for UFS core circuits				
VDD_USB_SS_CORE	Power for USB digital core circuits – SS				
VDD_PLL2	Power for PLL circuits – 1.250 V	1.21	1.25	1.29	V
VDD_PLL2_ISO	Power for PLL circuits – 1.250 V that need isolated routing on the PCB				
VDD_MIPI_CSI	Power for MIPI_CSI I/Os				
VDD_MIPI_DSI	Reference for MIPI_DSI I/Os and circuits				
VDD_PLL3	Power for PLL circuits – 1.800 V	1.7	1.8	1.9	V
VDD_P9	Power for pad group 9 – CXO_2 pad				
VDD_HDMI2	Power for HDMI circuits – high voltage				
VDD_UFS_1P8	Power for UFS 1.8 V circuits				
VDD_USB_1P8	Power for USB HS1, HS2, and SS – low voltage				
VDD_PCIE_1P8	Power for PCIe I/O circuitry				
VDD_P11	Power for pad group 11 – CXO pad				
VDD_P1	Power for pad group 1 – EBI1 pads and DDR memory I/O pads	1.07	1.125	1.17	V
VDD_DDR_CORE_1P2	Power for PoP DDR memory core – VDD2 for DDR memory				
VDD_P2	Power for pad group 2 – SDC2 pads	1.7/2.7	1.8/2.95	1.9/3.04	V
VDD_P3	Power for pad group 3 – most I/O pads	1.7	1.8	1.9	V
VDD_DDR_CORE_1P8	Power for PoP DDR memory core – 1.8 V for VDD1				
VDD_P7	Power for pad group 7 – SDC1 pads				
VDD_P5	Power for pad group 5 – UIM1 pads	1.7/2.7	1.8/2.95	1.9/3.04	V
VDD_P6	Power for pad group 6 – UIM2 pads	1.7/2.7	1.8/2.95	1.9/3.04	V
VDD_P10	Power for pad group 10 – UFS pad	1.15	1.2	1.25	V
VDD_P12	Power for pad group 12 – SSC pad	1.7	1.8	1.9	V
VDD_USB_HS_3P1	Power for USB HS1 and HS2 – high voltage	2.98	3.075	3.2	V
Thermal conditions					
T_C	Device operating temperature (case)	-30	+25	+85	°C
	Fuse programming temperature (case)	+10	+25	+85	°C
T_A [2]	3GPP2-mode operating temperature	-30	+25	+60	°C

	(ambient)				
	3GPP-mode operating temperature (ambient)	-20	+25	+60	°C

1. Typical voltages represent the recommended output settings of the companion PMIC device.
2. These temperature ranges are defined by the 3GPP and 3GPP2 system specifications.

Table 28 Operating voltages

8.2.1 Core and memory voltage minimization (retention mode)

The APM supports VDD minimization, also known as VDD_CORE retention mode. This technique reduces the leakage of the digital logic by reducing VDD to the minimum required to maintain the register and memory state.

The V(MIN) for state retention is found through characterization. As in any normal distribution, retention voltages vary across devices. Three fuses are blown to set the core voltage in retention mode. Two fuses are blown to set the memory voltage in retention mode. These fuses are used by software.

VDD_CORE	Bit 31 (MSB)	Bit 30	Bit 29 (LSB)
0.4 V	1	0	0
0.45 V	0	1	1
0.5 V	0	1	0
0.55 V	0	0	1
0.6 V	0	0	0

Table 29 Core voltage in retention mode [1 2]

1. The VDD_CORE voltages specified are PMIC settings.
2. For fuse locations listed in this table, refer to register 0x00070134.

VDD_MEM	Bit 4 (MSB)	Bit 3	Bit 2 (LSB)
0.49 V	1	0	0
0.55 V	0	1	1
0.58 V	0	1	0
0.65 V	0	0	1
0.7 V	0	0	0

Table 30 Memory voltage in retention mode [1 2]

1. The VDD_MEM voltages specified are PMIC settings.
2. For fuse locations listed in this table, refer to register 0x00070148.

VDD_APC	Bit 22 (MSB)	Bit 21	Bit 20 (LSB)

0.4 V	1	0	0
0.45 V	0	1	1
0.5 V	0	1	0
0.55 V	0	0	1
0.6 V	0	0	0

Table 31 APC voltage in retention mode [1 2 3]

1. The VDD_APC voltages specified are PMIC settings.
2. For fuse locations listed in this table, refer to register 0x0007014C.
3. VDD_APC is typically turned OFF in retention mode. However, depending on the use case, software can put the VDD_APC rail in retention voltage.

8.3 Power distribution network

The impedances of the distribution networks that deliver power to the APQ device are critical to its supply voltages, not just at DC but over a wide range of frequencies. An inadequate PDN could cause the minimum/maximum values listed in Table 32 and Table 33 to be violated. Table 34 lists the PDN maximum impedance specifications.

Power domain	Maximum impedance (mΩ)		Port number	Pin number of positive port	Pin number of negative port
	DC–10 Hz	10 Hz–25 MHz			
VDD_APC	2	15	1	All VDD_APC pins	All GND pins
VDD_GFX	3	25	1	All VDD_GFX pins	All GND pins
VDD_MODEM	10	30	1	All VDD_MODEM pins	All GND pins
VDD_CORE	8	–	1	All VDD_CORE pins	All GND pins
VDD_MEM	8	–	1	All VDD_MEM pins	All GND pins
VDD_SSC_CORE	50	85	1	J29, L25, L27, L29	J27, J31, N23, N25, N27, N31
VDD_SSC_MEM	150	200	1	N29	N27, N31

Table 32 APQ8096 PDN specifications – lumped

Power domain	Maximum impedance (mΩ)	Port number	Pin number of positive port	Pin number of negative port
	10 Hz–25 MHz			
VDD_APC	64	1	R9, R11, R13	N9, N11, N13, N15, P8, T8, U9, U11, U13, U15
	64	2	R17, R19, R21	N15, N17, N19, N21, N23, U15, U17, U19, U21, U23
	64	3	AC9, AC11, AG9, AG11	Y8, AA9, AA11, AE9, AE11, AJ11

Power domain	Maximum impedance (mΩ) 10 Hz–25 MHz	Port number	Pin number of positive port	Pin number of negative port
	64	4	AC16, AC21, AG16, AG21	AA15, AA17, AA19, AA21, AE21, AE23, AJ15, AJ17, AJ19, AJ21, AJ23
VDD_GFX	64	1	AW31, AW33, AW35	AU29, AU31, AU33, AU35, BA31, BA33, BA35
	64	2	AW41, AW43	AU43, BA41, BA43, BB42
VDD_MODEM	64	1	L33, L35	J31, J35, N31, N33, N35, N37
	85	2	L41	J39, J43, N39, N41, N43
	70	3	R39, R41, R43	N37, N39, N41, N43, U37, U39, U41
	70	4	W41, W43	U39, U41, AA39, AA41, AA43
VDD_CORE	90	1	F12	F14, G13, H12, J11, J13
	64	2	J25, L21, L23	J21, J27, N19, N21, N23, N25
	80	3	L37, L39	J35, J39, N35, N37, N39, N41
	64	4	N7, V8	N9, P8, T8, U9, Y8
	35	5	R25, R27, R29	N23, N25, N27, N31, U23, U25, U31
	40	6	W25, W27, W29, AC25, AC27, AC29, AG23, AG25, AG31, AG33, AL25, AL27	U23, U25, U31, AA25, AA27, AA29, AE21, AE23, AE25, AE27, AE29, AE31, AE33, AJ21, AJ23, AJ25, AJ27, AJ29, AJ31, AJ33
	64	7	AC37, AC39, AC41, AC43, AG43, AG45	AA35, AA37, AA39, AA41, AA43, AC45, AE35, AE37, AE39, AE41, AE43, AE45, AF46, AJ43
	64	8	AL11, AL13, AL15, AL17, AL19, AR13, AR15	AJ11, AJ13, AJ15, AJ17, AJ19, AJ21, AL9, AN9, AN11, AN13, AN15, AN17, AN19, AN21, AU11, AU13, AU15, AU17
	64	9	AR21, AR23	AN19, AN21, AN23, AU19, AU21, AU23, AU25
	64	10	AR27, AR29	AN29, AN31, AU25, AU27, AU29, AU31
	64	11	AW9, AW11	AU9, AU11, AU13, BA11, BB10, BC9
	64	12	AW17, AW19	AU15, AU17, AU19, AU21, BA15, BA17, BA19, BA21, BB18
	64	13	AW25, AW27	AU23, AU25, AU27, AU29, BA23, BA25, BA29, BB24, BB30
	100	14	BA37	BA35, BA39, BB38
	100	15	BA45	BA41, BA43, BB42
VDD_MEM	90	1	H10	H12, J9, J11
	85	2	L31	H32, J31, N31
	80	3	L43	J43, N41, N43
	80	4	R7	N9, P8, T8, U9
	64	5	R15	N13, N15, N17, U13, U15, U17
	64	6	R23	N21, N23, N25, U21, U23, U25
	50	7	R35, R37, U27, U29, W37, W39, AC33, AC35	N33, N35, N37, N39, U25, U31, U33, U35, U37, U41, AA35, AA37, AA39, AA41, AE31, AE33, AE35, AE37

Power domain	Maximum impedance (mΩ)	Port number	Pin number of positive port	Pin number of negative port
	10 Hz–25 MHz			
	90	8	AC7	Y8, AA9, AE9
	64	9	AC23	AA21, AA25, AE21, AE23, AE25
	70	10	AE16	AA15, AA17, AJ15, AJ17
	64	11	AG27, AG29	AE25, AE27, AE29, AE31, AJ25, AJ27, AJ29, AJ31
	64	12	AL21, AL23, AR17, AR19	AJ19, AJ21, AJ23, AJ25, AN15, AN17, AN19, AN21, AN23, AU15, AU17, AU19, AU21
	64	13	AL29, AL31, AL33, AL35	AJ27, AJ29, AJ31, AJ33, AJ35, AN27, AN29, AN31, AN33, AN35
	64	14	AL43, AL45, AU45	AJ41, AJ43, AN43, AU43
	80	15	AP41	AN43, AU43
	64	16	AR9, AR11	AN9, AN11, AN13, AU9, AU11, AU13
	64	17	AW13, AW15	AU11, AU13, AU15, AU17, BA11, BA13, BA15, BA17
	64	18	AW21, AW23	AU19, AU21, AU23, AU25, BA19, BA21, BA23, BA25, BB22, BB24
	64	19	AW29	AU27, AU29, AU31, BA29, BA31, BB30
	64	20	AW37, AW39	AU35, BA35, BA39, BA41, BB38

Table 33 APQ8096 PDN specifications – distributed

Power domain	Maximum impedance (m)		Maximum effective impedance (m)					Port number	Pin number of positive port	Pin number Of negative port
	Lumped DC	*Distributed DC*	*1 MHz*	*5 MHz*	*9 MHz*	*25 MHz*	*300 MHz*			
VDD_EBI_PHY [1]	20	53	1000	200	200	481	5448	1	J15	E15, F14, F16, F18, F20, F22, G13, G17, G19, G21, H12, J11, J17, J21
			1000	200	200	481	5448	2	J19	E15, F14, F16, F18, F20, F22, G13, G17, G19, G21, H12, J11, J17, J21
			1000	200	200	481	5448	3	J23	E15, F14, F16, F18, F20, F22, G13, G17, G19, G21, H12,

Power domain	Maximum impedance (m)		Maximum effective impedance (m)					Port number	Pin number of positive port	Pin number Of negative port
	Lumped DC	*Distributed DC*	*1 MHz*	*5 MHz*	*9 MHz*	*25 MHz*	*300 MHz*			
										J11, J17, J21
		53	1000	200	200	481	5448	4	J33	F32, F34, F36, F38, F40, F42, G35, G37, G39, G43, H32, J35, J39, J43, J45
			1000	200	200	481	5448	5	J37	F32, F34, F36, F38, F40, F42, G35, G37, G39, G43, H32, J35, J39, J43, J45
			1000	200	200	481	5448	6	J41	F32, F34, F36, F38, F40, F42, G35, G37, G39, G43, H32, J35, J39, J43, J45
		53	1000	200	200	481	5448	7	BB12	BA11, BA13, BA15, BA17, BA19, BA21, BB10, BB14, BB18, BB22, BC9, BD10, BD14, BD18, BE11, BE13, BE15, BE17, BE19
			1000	200	200	481	5448	8	BB16	BA11, BA13, BA15, BA17, BA19, BA21, BB10, BB14, BB18, BB22, BC9, BD10, BD14, BD18, BE11, BE13, BE15, BE17, BE19
			1000	200	200	481	5448	9	BB20	BA11, BA13, BA15, BA17, BA19, BA21, BB10, BB14, BB18, BB22, BC9,

Power domain	Maximum impedance (m)		Maximum effective impedance (m)					Port number	Pin number of positive port	Pin number Of negative port
	Lumped DC	*Distributed DC*	*1 MHz*	*5 MHz*	*9 MHz*	*25 MHz*	*300 MHz*			
										BD10, BD14, BD18, BE11, BE13, BE15, BE17, BE19
VDD_EBI_PHY [1] (cont.)	20	53	1000	200	200	481	5448	10	BB36	BA35, BA39, BA41, BA43, BB38, BB42, BD38, BD42, BE35, BE37, BE39, BE41, BE43, BE45
			1000	200	200	481	5448	11	BB40	BA35, BA39, BA41, BA43, BB38, BB42, BD38, BD42, BE35, BE37, BE39, BE41, BE43, BE45
			1000	200	200	481	5448	12	BB44	BA35, BA39, BA41, BA43, BB38, BB42, BD38, BD42, BE35, BE37, BE39, BE41, BE43, BE45
VDD_EBI_IO [1]	9	38	972	199	199	356	4325	1	H14, H16	E15, F14, F16, F18, F20, F22, G13, G17, G19, G21, H12, J11, J17, J21
			972	199	199	356	4325	2	H18, H20	E15, F14, F16, F18, F20, F22, G13, G17, G19, G21, H12, J11, J17, J21
			972	199	199	356	4325	3	H22, H24	E15, F14, F16, F18, F20, F22, G13, G17, G19, G21, H12, J11, J17, J21

Power domain	Maximum impedance (m)		Maximum effective impedance (m)					Port number	Pin number of positive port	Pin number Of negative port
	Lumped DC	*Distributed DC*	*1 MHz*	*5 MHz*	*9 MHz*	*25 MHz*	*300 MHz*			
VDD_EBI_IO [1]	9	38	972	199	199	356	4325	4	H34, H36	F32, F34, F36, F38, F40, F42, G35, G37, G39, G43, H32, J35, J39, J43, J45
			972	199	199	356	4325	5	H38, H40	F32, F34, F36, F38, F40, F42, G35, G37, G39, G43, H32, J35, J39, J43, J45
			972	199	199	356	4325	6	H42, H44	F32, F34, F36, F38, F40, F42, G35, G37, G39, G43, H32, J35, J39, J43, J45
			972	199	199	356	4325	7	BC11, BC13	BA11, BA13, BA15, BA17, BA19, BA21, BB10, BB14, BB18, BB22, BC9, BD10, BD14, BD18, BE11, BE13, BE15, BE17, BE19
			972	199	199	356	4325	8	BC15, BC17	BA11, BA13, BA15, BA17, BA19, BA21, BB10, BB14, BB18, BB22, BC9, BD10, BD14, BD18, BE11, BE13, BE15, BE17, BE19
			972	199	199	356	4325	9	BC19, BC21	BA11, BA13, BA15, BA17, BA19, BA21, BB10, BB14, BB18, BB22, BC9, BD10, BD14, BD18, BE11, BE13, BE15, BE17, BE19

Power domain	Maximum impedance (m)		Maximum effective impedance (m)					Port number	Pin number of positive port	Pin number Of negative port
	Lumped DC	*Distributed DC*	*1 MHz*	*5 MHz*	*9 MHz*	*25 MHz*	*300 MHz*			
		38	972	199	199	356	4325	10	BC35, BC37	BA35, BA39, BA41, BA43, BB38, BB42, BD38, BD42, BE35, BE37, BE39, BE41, BE43, BE45
			972	199	199	356	4325	11	BC39, BC41	BA35, BA39, BA41, BA43, BB38, BB42, BD38, BD42, BE35, BE37, BE39, BE41, BE43, BE45
			972	199	199	356	4325	12	BC43, BC45	BA35, BA39, BA41, BA43, BB38, BB42, BD38, BD42, BE35, BE37, BE39, BE41, BE43, BE45
	DC		*1 MHz*	*3 MHz*	*10 MHz*	*25 MHz*	*300 MHz*			
VDD_EBI_IO_ISO	60		804	196	196	388	5087	1	B16	A15
	60		804	196	196	388	5087	2	D40	B40
	60		804	196	196	388	5087	3	BH16	BK16
	60		804	196	196	388	5087	4	BH40	BK40

1. Meeting both lumped and distributed DC specifications is required.

Table 34 APQ8096 PDN specifications – EBI

8.4 Power sequencing

The PMIC includes power on circuits that provide the proper power on sequencing for the entire APQ8096 chipset. The supplies are turned on as groups of regulators that are selected by the hardware configuration of some PMIC pins. There will be a hardware default sequence that can be used, however the programmable boot sequence (PBS) module of the PMIC allows for programming of any other sequence required.

A high-level summary of the required default power-on sequence:

1. VDD_MEM (on-chip memory), VDD_USB_HS_CORE (USB digital core circuits – HS1, HS2)

2. VDD_EBI_PHY, VDD_EBI_IO, and VDD_EBI_IO_ISO (EBI0/1 circuits)

3. VDD_CORE (digital core circuits)

4. VREF_SDC/VREF_UIM/VREF_APC (SDC/UIM reference voltage)

5. VDD_P3 (I/Os), VDD_P7 (SDC1), and VDD_DDR_CORE_1P8 (DDR memory core 1.8 V)

6. SLEEP_CLK (32.768 MHz)

7. VDD_PLL3 (PLL circuitry 1.8 V), VDD_UFS_1P8 (UFS 1.8 V circuits), VDD_USB_1P8 (USB 1.8 V circuits), VDD_PCIE_1P8 (PCIe I/O circuits), VDD_HDMI2 (HDMI 1.8 V circuits), VDD_P9 (CXO_2), and VDD_P11 (CXO)

8. VDD_P1 (EBI and DDR I/Os), VDD_DDR_CORE_1P1 (DDR core 1.1 V), and VREF_EBI (EBI0 and EBI1 DQ and CA reference voltage)

9. VDD_USB_HS_3P1 (USB 3 V circuits)

10. VDD_P10 (UFS I/O)

11. VDD_PLL2 and VDD_PLL2_ISO (PLL circuitry 1.25 V), VDD_MIPI_CSI, and VDD_MIPI_DSI

12. VDD_PLL1 and VDD_PLL1_ISO (PLL circuitry 0.925 V), VDD_HDMI1 (HDMI 0.925 V circuits), VDD_PCIE_CORE (PCIe core circuits), VDD_UFS_CORE (UFS core circuits), and VDD_USB_SS_CORE (USB digital core circuits – SS)

13. VDD_P2 (SDC2 I/O)

14. CXO (19.2 MHz for digital circuits)

15. VDD_APC0 (applications processor cluster 0)

16. CXO_2 (19.2 MHz for analog circuits)

Comments regarding this sequence:

- The core voltage (VDD_CORE) needs to power up before the pad circuits (VDD_PX), so that the internal circuits can take control of the I/Os and pads.
- If pad voltages power up first, the output drivers might be stuck in unknown states, and might cause large leakage currents until VDD_CORE powers on.
- The general-purpose pad voltage (VDD_P3) needs to precede the analog voltages (VDD_AX).
- Any other appropriate supplies can be powered on by software after the sequence is completed.
- Each domain needs to reach its 90% value before the next domain starts ramping up. For example, when VDD_CORE reaches 90% of its value, the VDD_P3 supply can start ramping up.

8.4.1 Dhrystone and rock bottom maximum power

Table 35 lists the values for Dhrystone and rock bottom power specifications.

APQ version	Kryo quad-core Dhrystone (W) at 85°C (Tj) [1] [2] [3]	Rock bottom (mW) at 30°C (Tj) [4]
APQ8096	8.0	9.7
APQ8096SG-AC	8.0	9.7
APQ8096SG-AB	7.0	9.7

1. This Kryo quad core Dhrystone specification applies to APQ8096 and APQ8096SG CS devices.
2. Dhrystone power should be measured on the VDD_APC rail, at the point right before PDN capacitors (with a small serial sampling resistor inserted if necessary).
3. Measurement sampling rate should be > 1.25 Msps (or < 0.8 µs), and average window should be > 1 ms (or > 1250 samples).a.b.
4. Rock bottom (VDD_CORE and VDD_MEM) should be measured at VDD_CORE and VDD_MEM rails when VDD_CORE and VDD_MEM are at retention voltage.

Table 35 Dhrystone and rock bottom maximum power for APQ8096 devices

8.4.2 Digital logic characteristics

A digital I/O's performance specification depends on its pad type, its usage, and/or its supply voltage:

- Some are dedicated for interconnections between the APQ device and other ICs within the QTI chipset; therefore, specifications are not required.

- Some are defined by existing standards, such as I2C and SPI. QTI devices comply with those standards; therefore, additional specifications are not required.
- All other digital I/Os require performance specifications.

Parameter	Description	Min	Max	Units
VIH	High-level input voltage, CMOS/Schmitt, (hihys_en = LOW)	0.65 × VDD_Px	VDD_Px + 0.3 V	V
VIL	Low-level input voltage, CMOS/Schmitt, (hihys_en = LOW)	-0.3 V	0.35 × VDD_Px	V
VIH	High-level input voltage, CMOS/Schmitt, (hihys_en = HIGH)	0.7 × VDD_Px	VDD_Px + 0.3 V	V
VIL	Low-level input voltage, CMOS/Schmitt, (hihys_en = HIGH)	-0.3 V	0.3 × VDD_Px	V
VSHYS	Schmitt hysteresis voltage, (hihys_en = LOW)	100	–	mV
VSHYS	Schmitt hysteresis voltage, (hihys_en = HIGH)	300	–	mV
IIH	Input high leakage current (note1)	–	1	µA
IIL	Input low leakage current (note1)	-1	–	µA
IIHPD	Input high leakage current with pull-down	27.5 (60 K)	97.5 (20 K)	µA Ω
IILPU	Input low leakage current with pull-up	-97.5 (20 K)	-27.5 (60 K)	µA Ω
IOZH	High-level, tri-state leakage current 1	–	1	µA
IOZL	Low-level, tri-state leakage current 1	-1	–	µA
IOZHPD	High-level, tri-state leakage current with pull-down	27.5 (60 K)	97.5 (20 K)	µA Ω
IOZLPU	Low-level, tri-state leakage current with pull-up	97.5 (20 K)	27.5 (60 K)	µA Ω
IOZHKP	High-level, tri-state leakage current with keeper 2	-22.5 (20 K)	-7.5 (60 K)	µA Ω
IOZLKP	Low-level, tri-state leakage current with keeper 2	7.5 (60 K)	22.5 (20 K)	µA Ω
VOH	High-level output voltage, CMOS	VDD_Px - 0.45	VDD_Px	V
VOL	Low-level output voltage, CMOS	0.0	0.45	V

1. Pin voltage = VDD_Px maximum. For keeper pins, pin voltage = VDD_Px maximum - 0.45 V.
2. Pin voltage = GND and supply = VDD_Px maximum. For keeper pins, pin voltage = 0.45 V and supply = VDD_Px maximum.

Table 36 DC specification of VDD_P3 = 1.8 V GPIOs

Parameter	VDDP	Min	Typ	Max
VOH	1.8 V	VDD_Px - 0.45 V	–	–
VOL	1.8 V	–	–	0.45 V
VIH	1.8 V	0.65 × VDD_Px	–	VDD_Px + 0.3 V
VIL	1.8 V	-0.3 V	–	0.35 × VDD_Px

Table 37 Digital I/O characteristics for VDD_P7 = 1.8 V nominal (SDC1)

Parameter	Description	Min	Typ	Max	Units
VIH	High-level input voltage	0.625 × VDD_Px	–	VDD_P + 0.3	V
VIL	Low-level input voltage	-0.3	–	0.25 × VDD_Px	V
VHYS	Schmitt hysteresis voltage	100	–	–	mV
IIH	Input high leakage current	–	–	10	µA
IIL	Input low leakage current	-10	–	–	µA
IOZH	High-level, tri-state leakage current	–	–	10	µA
IOZL	Low-level, tri-state leakage current	-10	–	–	µA
Rpullup	Pull-up resistance	10 K	–	100 K	Ω
Rpulldown	Pull-down resistance	10 K	–	100 K	Ω
Rkeeperup	Keeper-up resistance	10 K	–	100 K	Ω
Rkeeperdown	Keeper-down resistance	10 K	–	100 K	Ω
VOH	High-level output voltage	0.75 × VDD_Px	–	VDD_Px	V
VOL	Low-level output voltage	0.0	–	0.125 × VDD_Px	V

Table 38 Digital I/O characteristics for VDD_P2 = 2.95 V nominal (SDC2)

Parameter	Description	Min	Typ	Max	Units
VIH	High-level input voltage	1.27	–	2	V
VIL	Low-level input voltage	-0.3	–	0.58	V
VHYS	Schmitt hysteresis voltage	100	–	–	mV
IIH	Input high leakage current	–	–	5	µA
IIL	Input low leakage current	-5	–	–	µA
IOZH	High-level, tri-state leakage current	-	–	5	µA
IOZL	Low-level, tri-state leakage current	-5	–	–	µA
Rpullup	Pull-up resistance	10 K	–	100 K	Ω
Rpulldown	Pull-down resistance	10 K	–	100 K	Ω
Rkeeperup	Keeper-up resistance	10 K	–	100 K	Ω
Rkeeperdown	Keeper-down resistance	10 K	–	100 K	Ω
VOH	High-level output voltage(note2)	1.4	–	–	V
VOL	Low-level output voltage	–	–	0.45	V

Table 39 Digital I/O characteristics for VDD_P2 = 1.8 V nominal (SDC2)

Parameter	Description	Min	Typ	Max	Units
VIH	High-level input voltage [1]	0.7 × VDD_Px	–	VDD_Px + 0.3	V
VIL	Low-level input voltage [1]	-0.3	–	0.2 × VDD_Px	V
VHYS	Schmitt hysteresis voltage [1]	100	–	–	mV
IIH	Input high leakage current	-20	–	20	µA
IIL	Input low leakage current	–	–	1000	µA
IOZH	High-level, tri-state leakage current	–	–	10	µA
IOZL	Low-level, tri-state leakage current	-10	–	–	µA
Rpullup	Pull-up resistance	10 K	–	100 K	Ω
Rpulldown	Pull-down resistance	10 K	–	100 K	Ω
Rkeeperup	Keeper-up resistance	10 K	–	100 K	Ω
Rkeeperdown	Keeper-down resistance	10 K	–	100 K	Ω
VOH	High-level output voltage [2]	0.8 × VDD_Px	–	VDD_Px	V
VOL	Low-level output voltage [2]	0.0	–	0.4	V

1. VIH and VIL are only applicable for I/O signal.
2. UICC specifies VOL = 0.2 × VDD_Px (RST, CLK) and 0.4 V (I/O) and VOH = 0.8 × VDD_Px (RST) and 0.7 × VDD_Px (CLK, I/O). The worse-case VOL and VOH are used in the table.

Table 40 Digital I/O characteristics for VDD_Px = 2.95 V nominal (UIM1 and UIM2 – Class B)

Parameter	Description	Min	Typ	Max	Units
VIH	High-level input voltage [1]	0.7 × VDD_Px	–	VDD_Px + 0.3	V
VIL	Low-level input voltage [1]	-0.3	–	0.2 × VDD_Px	V
VHYS	Schmitt hysteresis voltage [1]	100	–	–	mV
IIH	Input high leakage current	-20	–	20	µA
IIL	Input low leakage current	–	–	1000	µA
IOZH	High-level, tri-state leakage current	–	–	5	µA
IOZL	Low-level, tri-state leakage current	-5	–	–	µA
Rpullup	Pull-up resistance	10 K	–	100 K	Ω
Rpulldown	Pull-down resistance	10 K	–	100 K	Ω
Rkeeperup	Keeper-up resistance	10 K	–	100 K	Ω
Rkeeperdown	Keeper-down resistance	10 K	–	100 K	Ω
VOH	High-level output voltage [2]	0.8 × VDD_Px	–	VDD_Px	V
VOL	Low-level output voltage [2]	0.0	–	0.4	V

1. VIH and VIL are only applicable for I/O signal.
2. UICC specifies VOL = 0.2 × VDD_Px (RST, CLK) and 0.4 V (I/O) and VOH = 0.8 × VDD_Px (RST) and 0.7 × VDD_Px (CLK, I/O). The worse-case VOL and VOH are used in the table.

Table 41 Digital I/O characteristics for VDD_Px = 1.8 V nominal (UIM1 and UIM2 – Class B)

In all digital I/O cases, VOL and VOH are linear functions (Figure 99) with respect to the drive current (drive currents are given in

Table 7). They can be calculated using these relationships:

$$Vol\,[\max] = \frac{\%drive \times 450}{100}\ mV$$

$$Voh\,[\min] = Vdd\_px - \left(\frac{\%drive \times 450}{100}\right) mV$$

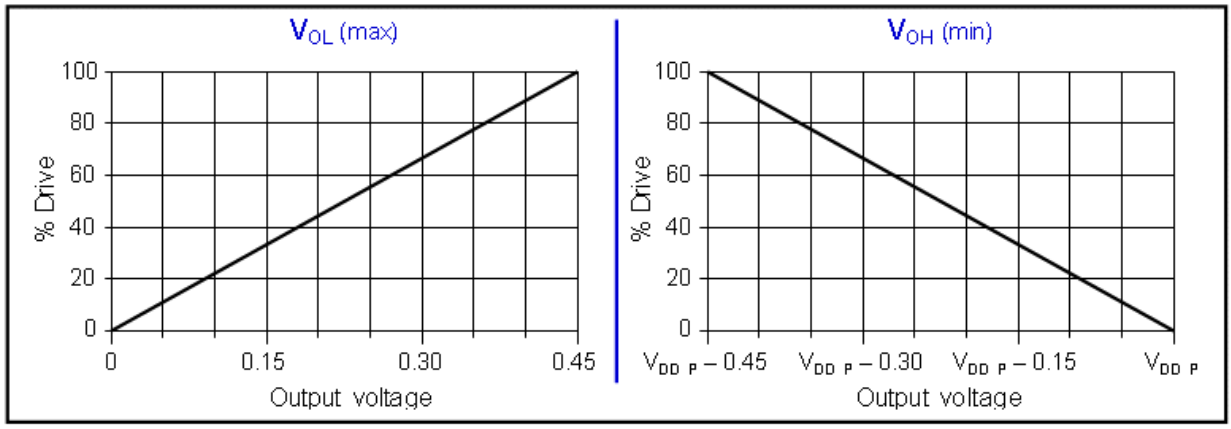


Figure 9 IV curve for VOL and VOH (valid for all VDD_Px)

8.5 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad design methodologies are included here.

NOTE *All APQ8096 devices are characterized with actively terminated loads; therefore, all baseband timing parameters in this document assume no bus loading. This is described further in Section 8.5.2.*

8.5.1 Timing diagram conventions

The conventions used within timing diagrams throughout this document are shown in Figure 10

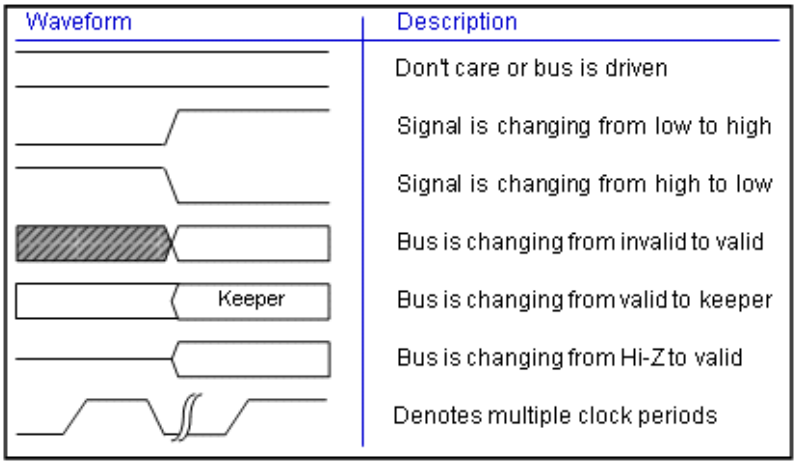


Figure 10 Timing diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
    - For a bus-type signal (multiple bits) – the processor or external interface is driving a value, but that value may or may not be valid.
    - For a single signal – indicates don't care.

8.5.2 Rise and fall time specifications

The testers that characterize APQ8096 devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in Figure 11

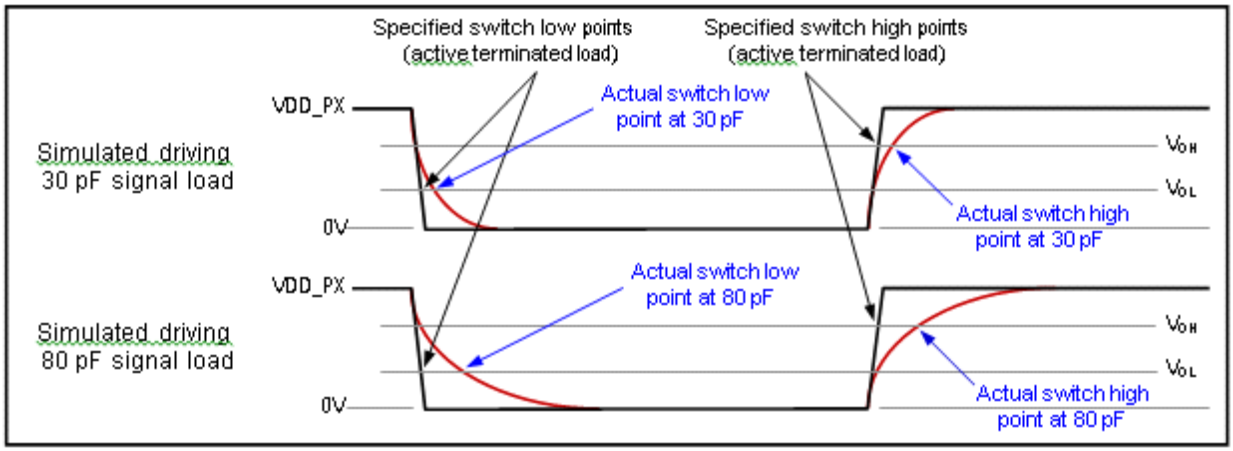


Figure 11 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the APQ device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

NOTE: *Board designers should use the relevant APQ8096 IBIS File for this analysis.*

8.5.3 Pad design

The APQ8096 device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behaviour that is symmetric with respect to the associated VDD_Px supply (Figure 8). The input switch point for pure input-only pads is designed to be VDD_Px/2 (or 50% of VDD_Px). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of VDD_Px for VIL and 65% of VDD_Px for VIH.

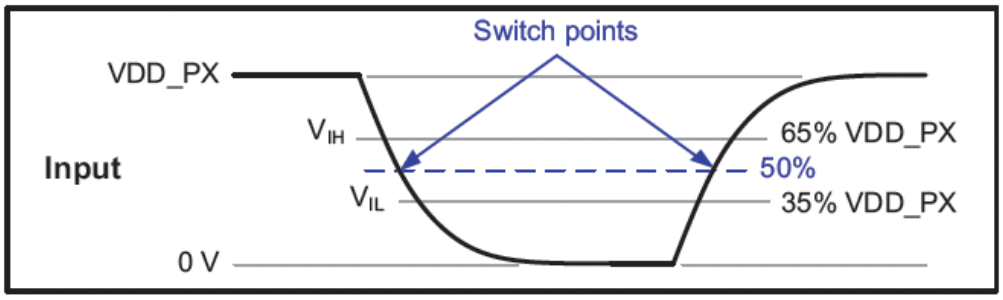


Figure 12 Digital Input signal switch points

Outputs (address, chip selects, clocks, etc.) are designed and characterized to source or sink a large DC output current (several mA) at the documented VOH (min) and VOL (max) levels over worst-case process/voltage/temperature. Because the pad output structures (Figure 9) are essentially CMOS drivers that may have a small amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected zero DC load outputs are estimated to be as follows:

- VOH ~ VDD_Px - 50 mV or more
- VOL ~ 50 mV or less

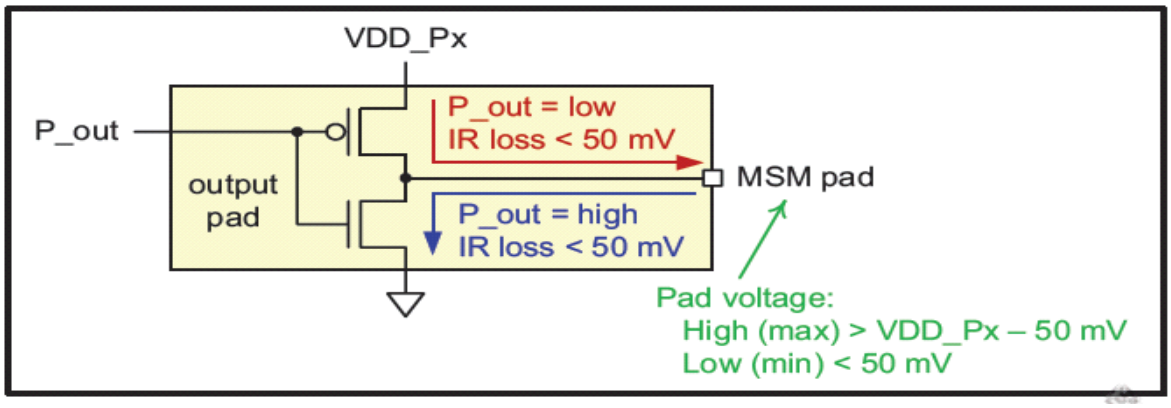


Figure 13 Output-pad equivalent circuit

The DC output drive strength can be approximated by linear interpolations between VOH (min) and VDD_Px - 50 mV, and between VOL (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at VOL (max) will provide approximately 3.0 mA or more at 2/3 × [VOL (max) - 50 mV], and 1.5 mA or more at 1/3 × [VOL (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at VOH (min) will provide approximately 1.25 mA or more at ½ × [VDD_Px - 50 mV + VOH (min)].

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking ISC (SC = short-circuit) of current, where the magnitude of ISC is larger than the current capability at the intended output logic levels.

Since the target application includes a radio, output pads are designed to minimize output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

Output drivers' rise time (t(r)) and fall time (t(f)) values are functions of board loading. Bidirectional pins include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both input and output behaviours were described above.

8.6 Memory support

All timing parameters in this document assume no bus loading. Rise/fall time numbers must be factored into the numbers in this document. For example, setup-time numbers will get worse and hold-time numbers may get better.

NOTE: *Information contained in this section is preliminary and is subject to change.*

8.6.1 EBI0 and EBI1 memory support

The EBI0 and EBI1 ports are dedicated to the PoP LPDDR4 SDRAM memory that is attached to the top of the APQ8096 chipset.

8.6.2 eMMC on SDC1

eMMC NAND flash can be supported via the SDC1 port. See Section 8.8.1 for secure digital interface details.

8.6.3 NOR memory on SPI

SPI can be used to support NOR memory devices with appropriate user-modified software. See Section 8.8.12 for serial peripheral interface details.

8.7 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

8.7.1 Camera interfaces

The APQ8096 device supports up to three 4-lane camera interfaces or up to four (two 4-lane and two 1-lane) camera interfaces.

Applicable standard	Feature exceptions	APQ variations
MIPI Alliance Specification for CSI-2 v1.3	RAW7 not supported DPCM predictor 2 not supported	None
MIPI Alliance Specification for DPHY v1.2	None	None
MIPI Alliance Specification for CPHY v1.0	None	None

Table 42 Supported MIPI_CSI standards and exceptions

8.7.2 Audio support

The APQ8096 supports the WCD9335 audio codec IC to provide the system's audio functions. APQ audio-related interface options with the WCD include:

- SLIMbus : Section 8.8.6
- I2S : Section 8.8.7
- PCM : Section 8.8.8
- I2C : Section 8.8.11

The APQ8096 also supports the audio portion of HDMI using APQ-internal connections; see Section 8.7.4 for supported HDMI specifications.

8.7.3 Display support

The APQ8096 device supports two 4-lane MIPI_DSI interfaces.

Applicable standard	Feature exceptions	APQ variations
MIPI Alliance Specification for Display Serial Interface	None	None
MIPI Alliance Specification for D-PHY V1.2	None	None

Table 43 Supported MIPI_DSI standards and exceptions

8.7.4 A/V outputs

The HDMI port is only supported by the APQ8096.

Applicable standard	Feature exceptions	APQ variations
HDMI Specification Version 2.0	None	None

Table 44 Supported HDMI standards and exceptions

8.7.5 DMB support

The APQ8096 supports an external DMB solution using the following interface options:

- TSIF : Section 8.8.9
- SD : Section 8.8.1

8.8 Connectivity

The connectivity functions supported by the APQ8096 that require electrical specifications include:

- SD, including SD cards and multimedia cards (MMC)
- USB host/slave support with built-in physical layer (PHY)
- Peripheral Component Interconnect Express (PCIe) interfaces
- User-integrated module (UIM) ports, including dual-voltage options
- Serial low-power inter-chip media bus (SLIMbus) interface
- Inter-IC sound (I2S) interfaces
- Pulse-coded modulation (PCM) interfaces
- Transport stream interface (TSIF) interfaces
- Touchscreen connections
- Through proper configuration of the twelve BLSP ports:
- Universal asynchronous receiver/transmitter (UART) ports
- User identity module (UIM) ports, including dual-voltage options
- Inter-integrated circuit (I2C) interfaces
- Serial peripheral interface (SPI) ports

Pertinent specifications for these functions are detailed in the following subsections.

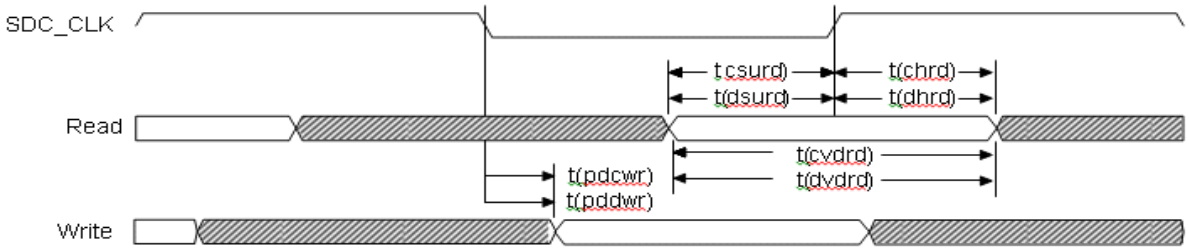
NOTE *In addition to the following hardware specifications, consult the latest software release notes for software-based performance features or limitations.*

8.8.1 SD interfaces

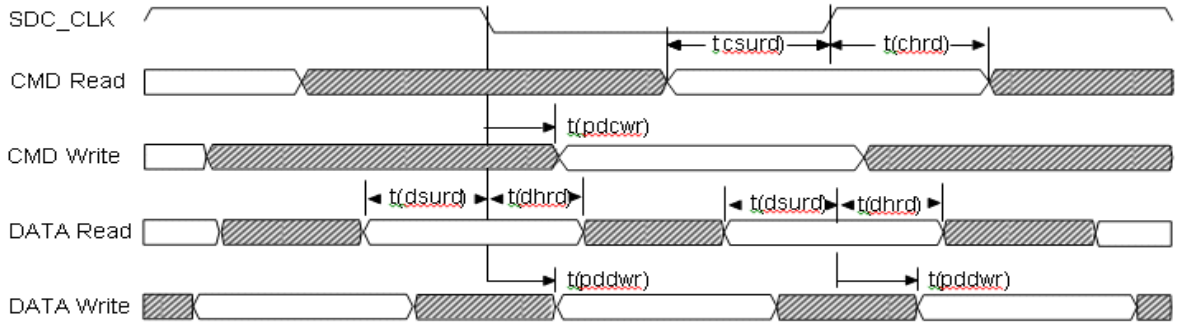
Applicable standard	Feature exceptions	APQ variations
Embedded Multimedia Card (e.MMC) Specification version 5.1	None	Timing specifications – see Figure 14
Secure Digital: Physical Layer Specification version 3.0	None	
SDIO Card Specification version 3.0	None	

Table 45 Supported SD standards and exceptions

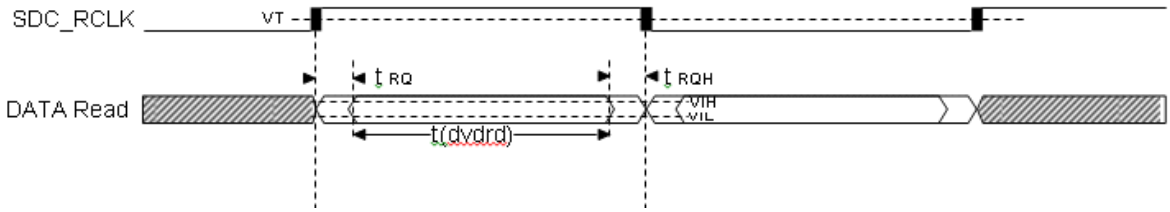
Single data rate – SDR mode



Double data rate – DDR mode



HS400 mode input timing



HS400 mode output timing

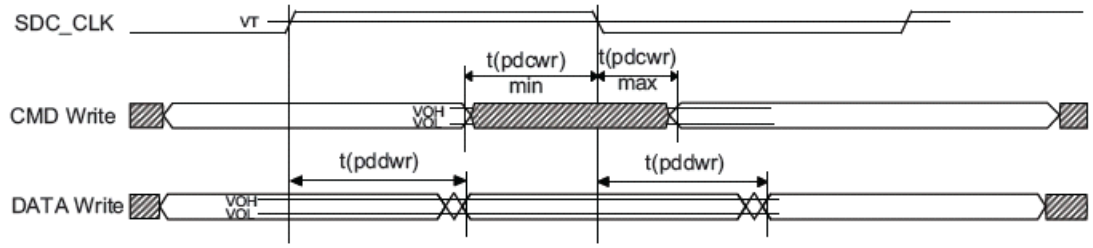


Figure 14 SD interface timing

8.8.2 USB interfaces

Applicable standard	Feature exceptions	APQ variations
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	SS Gen 2	Operating voltages, system clock, and VBUS
UTMI + Low Pin Interface (ULPI) Specification (October 20, 2004 Revision 1.1 or later)	None	None
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	None	None

Table 46 Supported USB standards and exceptions

8.8.3 PCIe interface

Applicable standard	Feature exceptions	APQ variations
PCI Express Specification, Revision 2.1 (March 4, 2009 or later)	None	None

Table 47 Supported PCIe standards and exceptions

8.8.4 UFS interface

Applicable standard	Feature exceptions	APQ variations
Universal Flash Storage (UFS), Version 2.0	None	None

Table 48 Supported UFS standards and exceptions

8.8.5 UICC interface

Applicable standard	Feature exceptions	APQ variations
ISO/IEC 7816-3	None	None

Table 49 Supported UICC standards and exceptions

8.8.6 SLIMbus interface

Applicable standard	Feature exceptions	APQ variations
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None	None

Table 50 Supported SLIMbus standards and exceptions

8.8.7 I2S interfaces

There are two I2S interface types supported by the APQ8096:

- Legacy I2S interfaces for primary and secondary microphones and speakers.
- The multiple I2S (MI2S) interface for microphone and speaker functions, including 7.1 audio for HDMI.

The following information applies to both interface types.

Applicable standards	Feature exceptions	APQ variations
Philips I2S Bus Specifications revised June 5, 1996	None	When an external SCK clock is used, a duty cycle between 45% to 55% is required.

Table 51 Supported I2S standards and exceptions

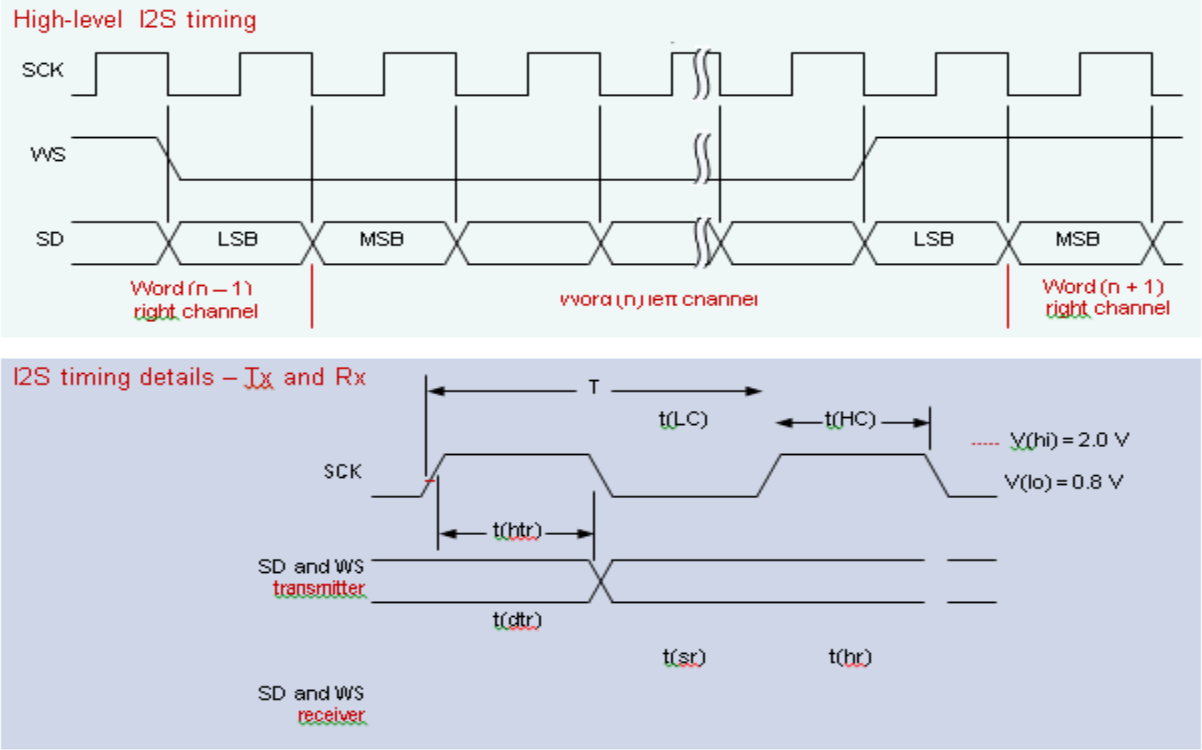


Figure 15 I2S timing diagram

Parameter		Comments [1]	Min	Typ	Max	Unit
Using internal SCK						
Frequency		–	–	–	12.288	MHz
T	Clock period	–	81.380	–	–	ns
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time	–	16.276	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	65.100	ns
t(htr)	SD and WS output hold time	–	0	–	–	ns
Using external SCK						
Frequency		–	–	–	12.288	MHz
T	Clock period	–	81.380	–	–	ns
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time	–	16.276	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	65.100	ns
t(htr)	SD and WS output hold time	–	0	–	–	ns

1. Load capacitance between 10 to 40 pF.

Table 52 I2S interface timing

8.8.8 External-codec PCM interface

- ***Primary PCM interface (2048 kHz clock)***

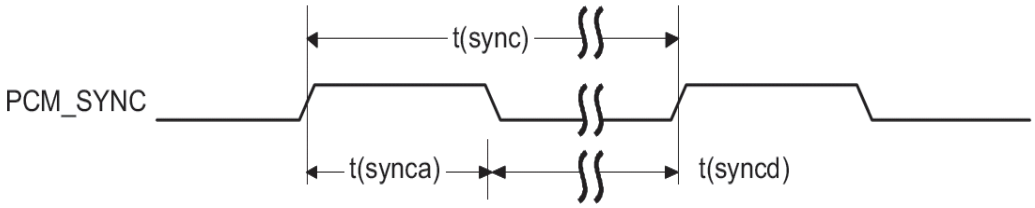


Figure 16 PCM_SYNC timing

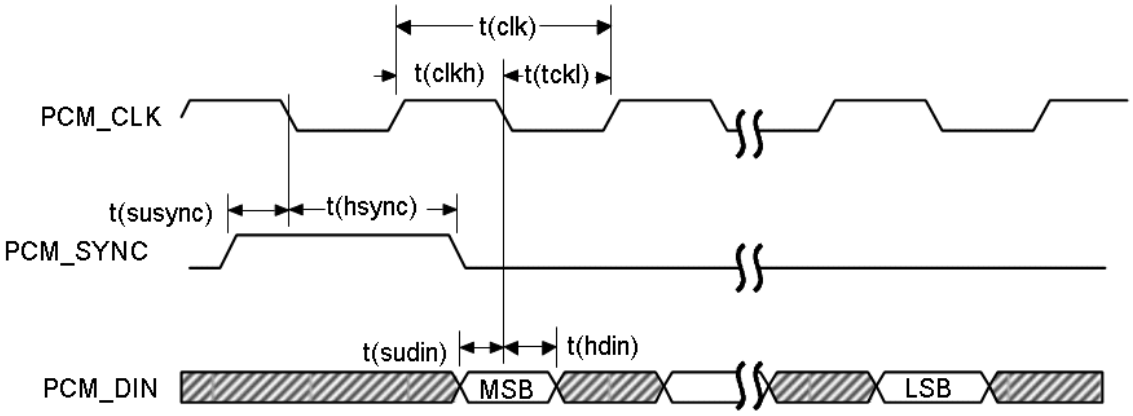


Figure 17 PCM_CODEC to APQ timing

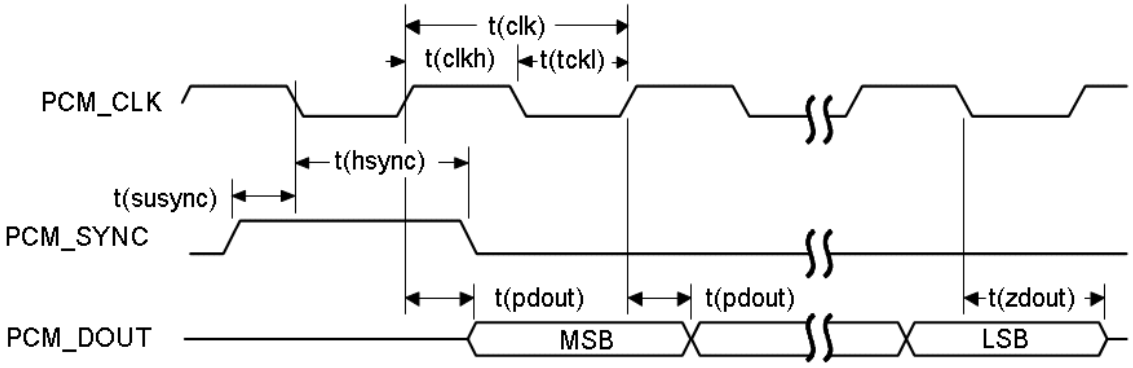


Figure 18 APQ to PCM_CODEC timing

Parameter		Comments	Min	Typ	Max	Unit
t(sync)	PCM_SYNC cycle time	–	–	125	–	µs
t(synca)	PCM_SYNC asserted time	–	–	488	–	ns
t(syncd)	PCM_SYNC deasserted time	–	–	124.5	–	µs
t(clk)	PCM_CLK cycle time	–	–	488	–	ns
t(clkh)	PCM_CLK high time	–	–	244	–	ns
t(clkl)	PCM_CLK low time	–	–	244	–	ns
t(susync)	PCM_SYNC offset time to PCM_CLK falling	–	–	122	–	ns
t(sudin)	PCM_DIN setup time to PCM_CLK falling	–	60	–	–	ns
t(hdin)	PCM_DIN hold time after PCM_CLK falling	–	10	–	–	ns
t(pdout)	Delay from PCM_CLK rising to PCM_DOUT valid	–	–	–	350	ns
t(zdout)	Delay from PCM_CLK falling to	–	–	160	–	ns

Parameter		Comments	Min	Typ	Max	Unit
	PCM_DOUT HIGH-Z					

Table 53 PCM_CODEC timing parameters

- *Auxiliary PCM interface (128 kHz clock)*

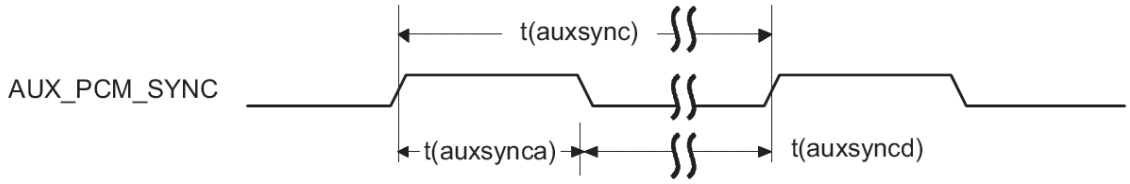


Figure 19 AUX_PCM_SYNC timing

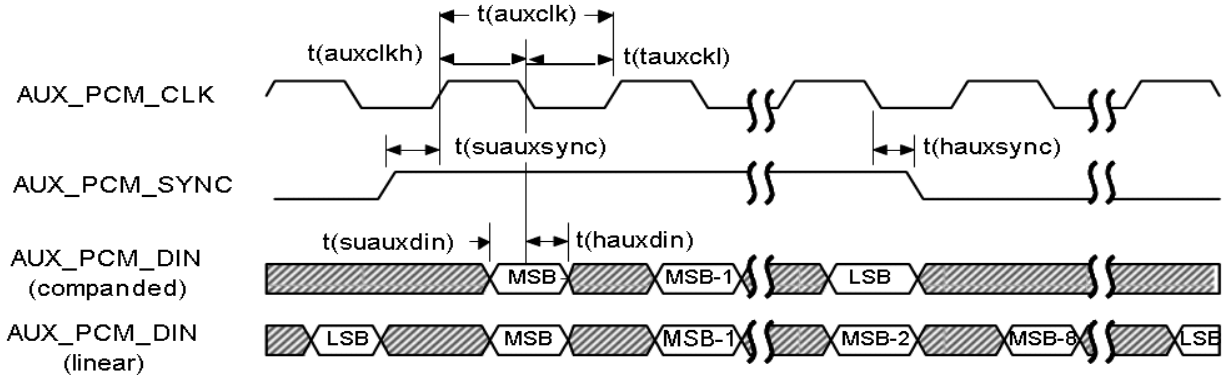


Figure 20 AUX_PCM_CODEC to APQ timing

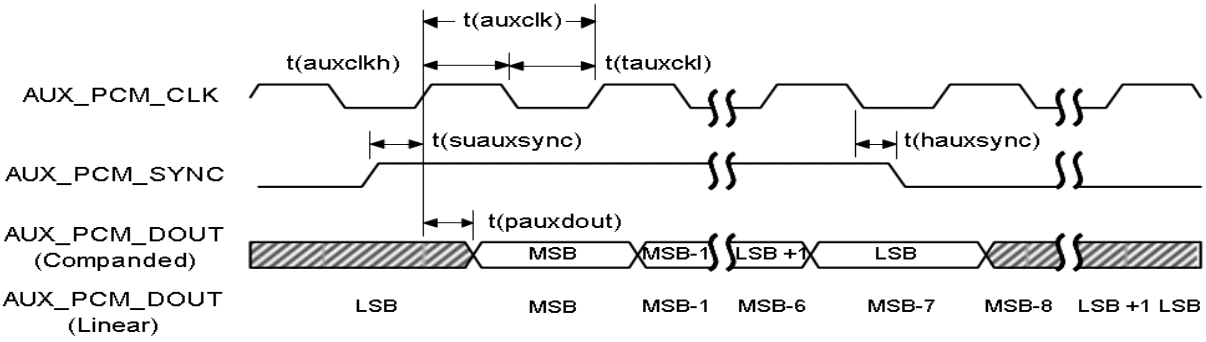


Figure 21 APQ to AUX_PCM_CODEC timing

Parameter		Comments	Min	Typ	Max	Unit
t(auxsync) [1]	AUX_PCM_SYNC cycle time	–	–	125	–	µs
t(auxsynca) [1]	AUX_PCM_SYNC asserted time	–	62.4	62.5	–	µs
t(auxsyncd) [1]	AUX_PCM_SYNC deasserted time	–	62.4	62.5	–	µs
t(auxclk) [1]	AUX_PCM_CLK cycle time	–	–	7.8	–	µs

Parameter		Comments	Min	Typ	Max	Unit
t(auxclkh) [1]	AUX_PCM_CLK high time	–	3.8	3.9	–	µs
t(auxclkl) [1]	AUX_PCM_CLK low time	–	3.8	3.9	–	µs
t(suauxsync)	AUX_PCM_SYNC setup time to AUX_PCM_CLK rising	–	1.95	–	–	ns
t(hauxsync)	PCM_SYNC hold time after AUX_PCM_CLK rising	–	1.95	–	–	ns
t(suauxdin)	AUX_PCM_DIN setup time to AUX_PCM_CLK falling	–	70	–	–	ns
t(hauxdin)	AUX_PCM_DIN hold time after AUX_PCM_CLK falling	–	20	–	–	ns
t(pauxdout)	Delay from AUX_PCM_CLK to AUX_PCM_DOUT valid	–	–	–	50	ns

1. These values require that the CODEC_CTL is not being used to override the codec clock and sync operation.

Table 54 AUX_PCM_CODEC timing parameters

8.8.9 TSIF

Applicable standard	Feature exceptions	APQ variations
ITU-T H.222.0 Transport Stream (HTS); also known as *ISO/IEC 13818-1*	None	None

Table 55 Supported TSIF standards and exceptions

8.8.10 Touchscreen connections

Touchscreen panels are supported using I2C buses (Section 8.8.11) and GPIOs configured as discrete digital inputs (Section 8.4.2). Additional specifications are not required.

8.8.11 I2C interface

Applicable standard	Feature exceptions	APQ variations
I2C Specification, version 3.0	None	HS mode, slave mode, and 10-bit addressing are not supported.

Table 56 Supported I2C standards and exceptions

8.8.12 Serial peripheral interface

The APQ8096 supports SPI only in the master mode. Any one of the 12 BLSP ports can be configured as an SPI master.

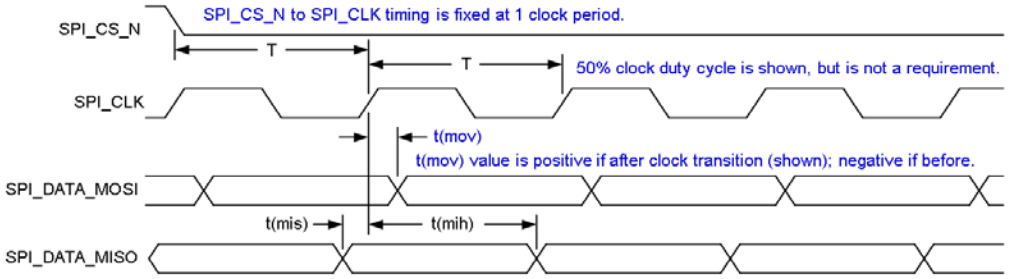


Figure 22 SPI master timing diagram

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clock period) [1]	50 MHz maximum	20	–	–	ns
t(ch)	Clock HIGH	8	–	–	ns
t(cl)	Clock LOW	8	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

1. The minimum clock period includes 1% jitter of maximum frequency.

Table 57 SPI master timing characteristics

8.8.13 Internal functions

Some internal functions require external interfaces to enable their operations. These include clock generation, modes and resets functions.

8.8.13.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

8.8.13.1.1 19.2 MHz CXO input

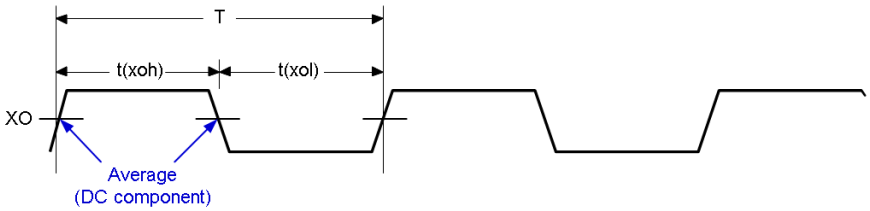


Figure 23 XO timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	XO logic high	–	22.6	–	29.5	ns
t(xol)	XO logic low	–	22.6	–	29.5	ns
T	XO clock period	–	–	52.083	–	ns
1/T	Frequency	19.2 MHz must be used.	–	19.2	–	MHz

Table 58 XO timing parameters

8.8.13.1.2 CXO_2 specification

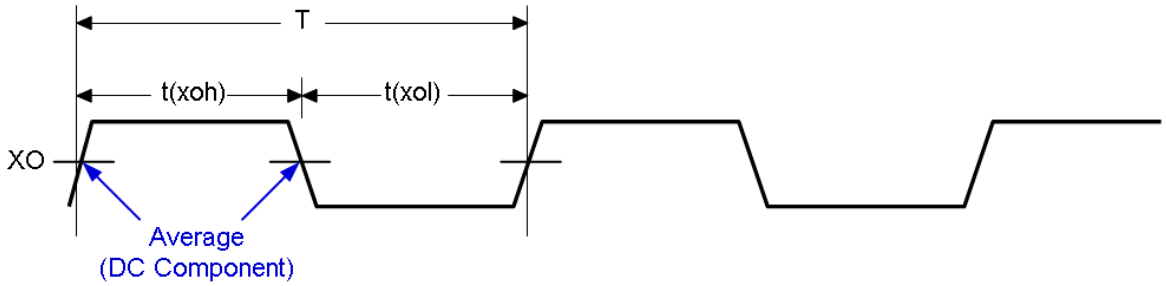


Figure 24 CXO_2 timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	XO logic high		22.6	–	29.5	ns
t(xol)	XO logic low		22.6	–	29.5	ns
T	XO clock period		–	52.083	–	ns
1/T	Frequency	19.2 MHz must be used	–	19.2	–	MHz

Table 59 CXO_2 timing parameters

8.8.13.1.3 Sleep clock

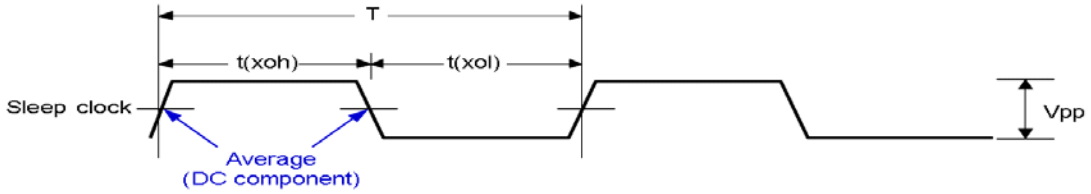


Figure 25 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high	–	4.58	–	25.94	µs
t(xol)	Sleep-clock logic low	–	4.58	–	25.94	µs
T	Sleep-clock period	–	–	30.518	–	µs
F	Sleep-clock frequency	F = 1/T	–	32.768	–	kHz
Vpp	Peak-to-peak voltage	–	–	1.8	–	V

Table 60 Sleep-clock timing parameters

8.8.13.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Section 8.5.

8.8.13.3 SWD

Parameter		Min	Max	Unit
T_{os}	SWDIO output skew to falling edge of SWDCLK	0	17.5	ns
T_{su}	Input setup time between SWDIO and rising edge of SWDCLK	4	–	ns
T_{hd}	Input hold time between SWDIO and rising edge of SWDCLK	1	–	ns

Table 61 AC timing parameters

8.8.14 RF and power management interfaces

The supported chipset and RFFE interfaces are listed in

Table 15 and Table 16. The digital I/Os must meet the logic-level requirements specified in Section 8.4.2. The Rx and Tx baseband interfaces are proprietary, and therefore are not specified

8.8.14.1 RF front end (RFFE)

Applicable standard	Feature exceptions	APQ variations
MIPI Alliance Specification for RF Front-End Control Interface version 1.0	None	None

Table 62 Supported RFFE standards and exceptions

8.8.14.2 System power management interface (SPMI)

Applicable standard	Feature exceptions	APQ variations
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None	None

Table 63 Supported SPMI standards and exceptions

9 About eInfochips

eInfochips is a Product and Semiconductor Design Solutions company, based out of Sunnyvale (USA) and Ahmedabad (India). The company has delivered turnkey solutions from its global offshore development centres for industries like Aerospace & Defence, Security & Surveillance, Semiconductor, Consumer Electronics, Medical Devices, Media & Broadcast, Retail and Software.

Being an innovation driven company, eInfochips has a portfolio of in-house hardware and software IPs to accelerate product development and testing. Having contributed to over 500+ customer products that have more than 10 Million deployments worldwide, eInfochips expertise has been recognized by reputed global agencies like Gartner, Frost & Sullivan and Zinnov.

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Contact Information:

Corporate Headquarter:	USA Office:
eInfochips Ltd. 11 A/B Chandra Colony, Behind Cargo Motors, Off. C. G. Road, Ellisbridge, Ahmedabad 380 006 Tel +91-79-2656 3705 Fax +91-79-2656 0722	eInfochips Ltd. 1230 Midas Way, Suite# 200 Sunnyvale, CA 94085. USA Tel +1-408-496-1882 Fax +1-801-650-1480
Technical Assistance:	eInfochips Qualcomm portal
Technical Support:	qcsupport@einfochips.com
Sales/Marketing Support:	marketing@einfochips.com