GLOBAL EDGE

Intelligence Of Things

ARM Instruction Set

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Agenda

- Caches

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- Caches
  - Non-cached system
  - cached system
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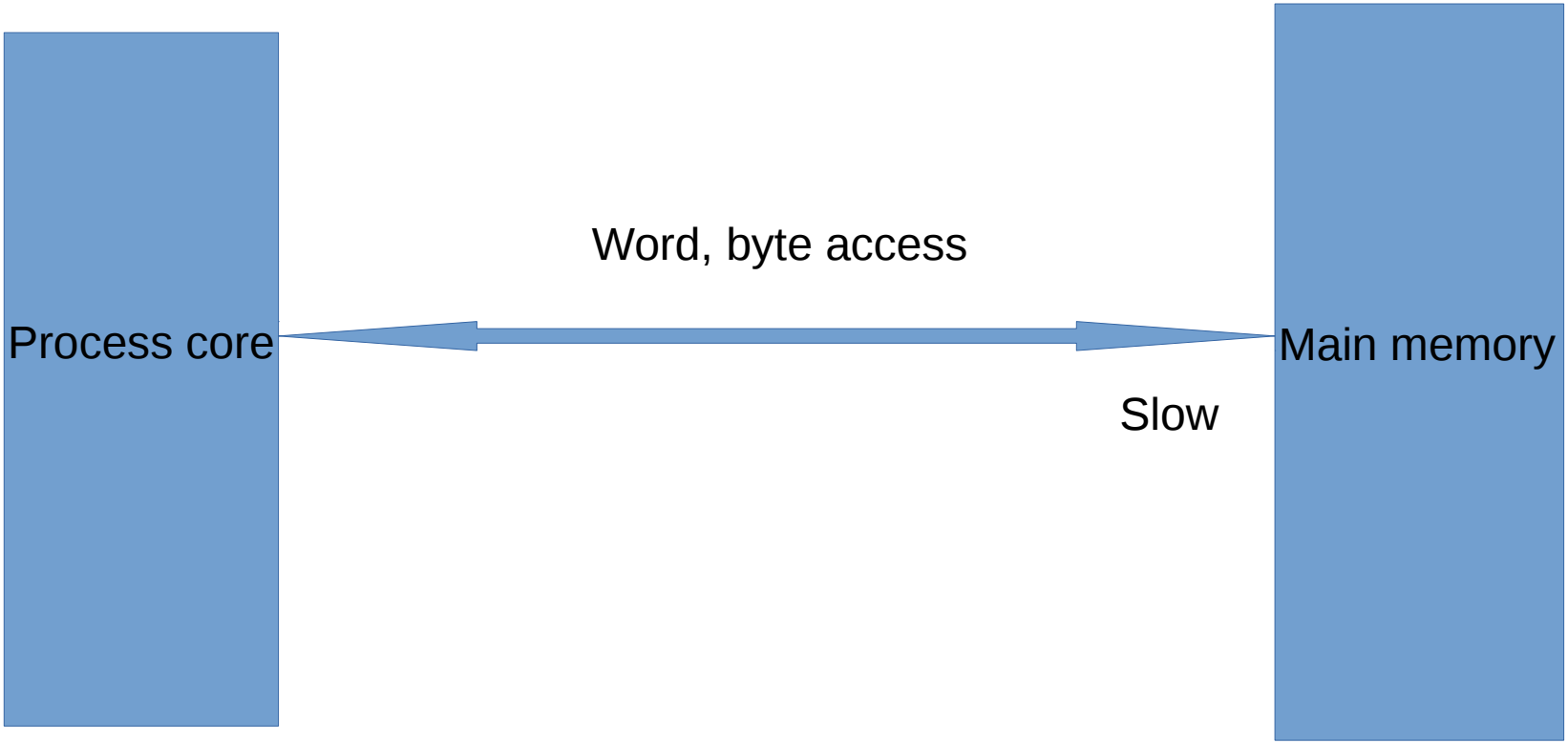
Non-Cached system

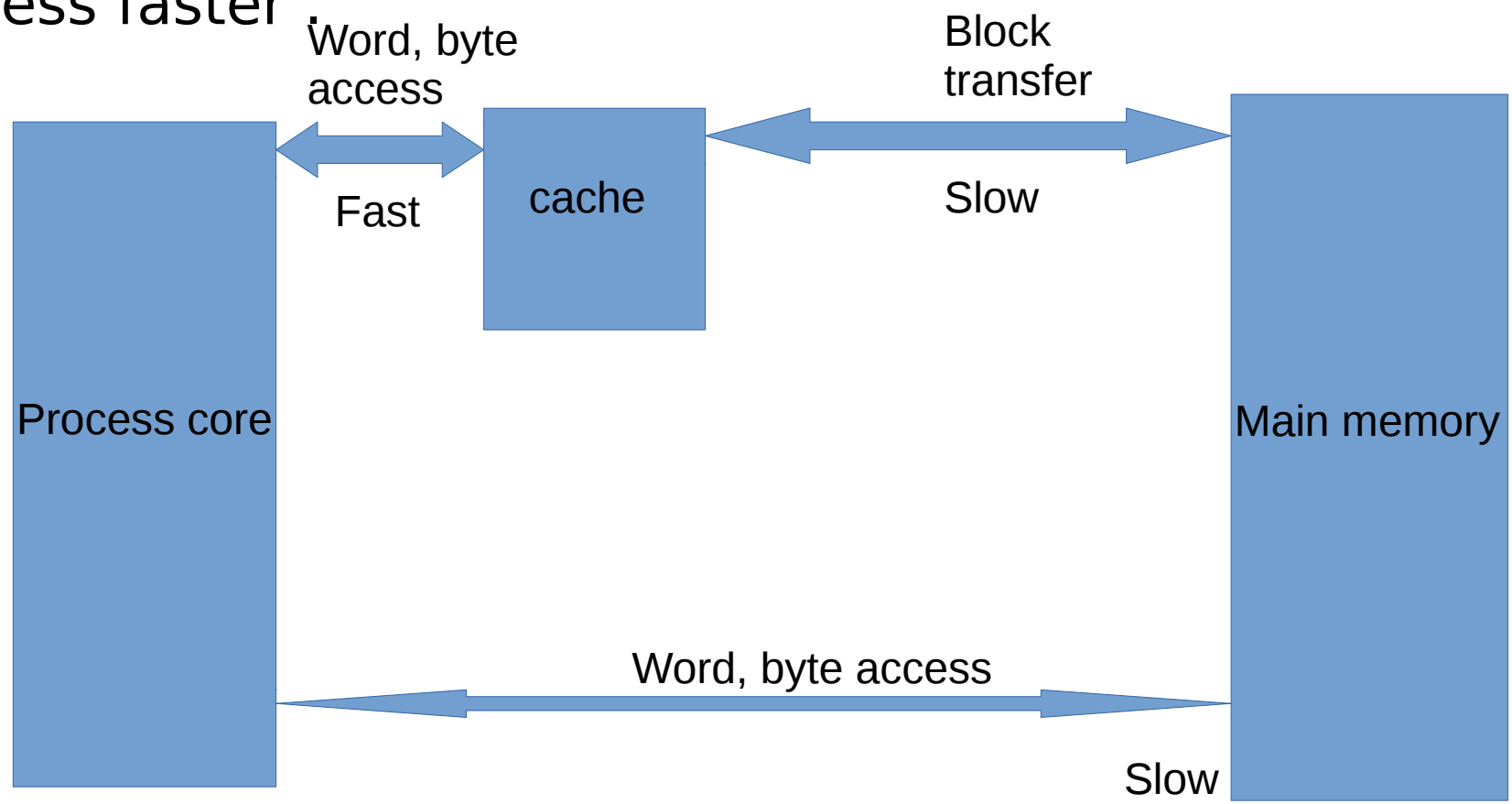
- Main memory is accessed directly by the processor core using the datatypes supported by the processor core.



NonCached system

Cached system

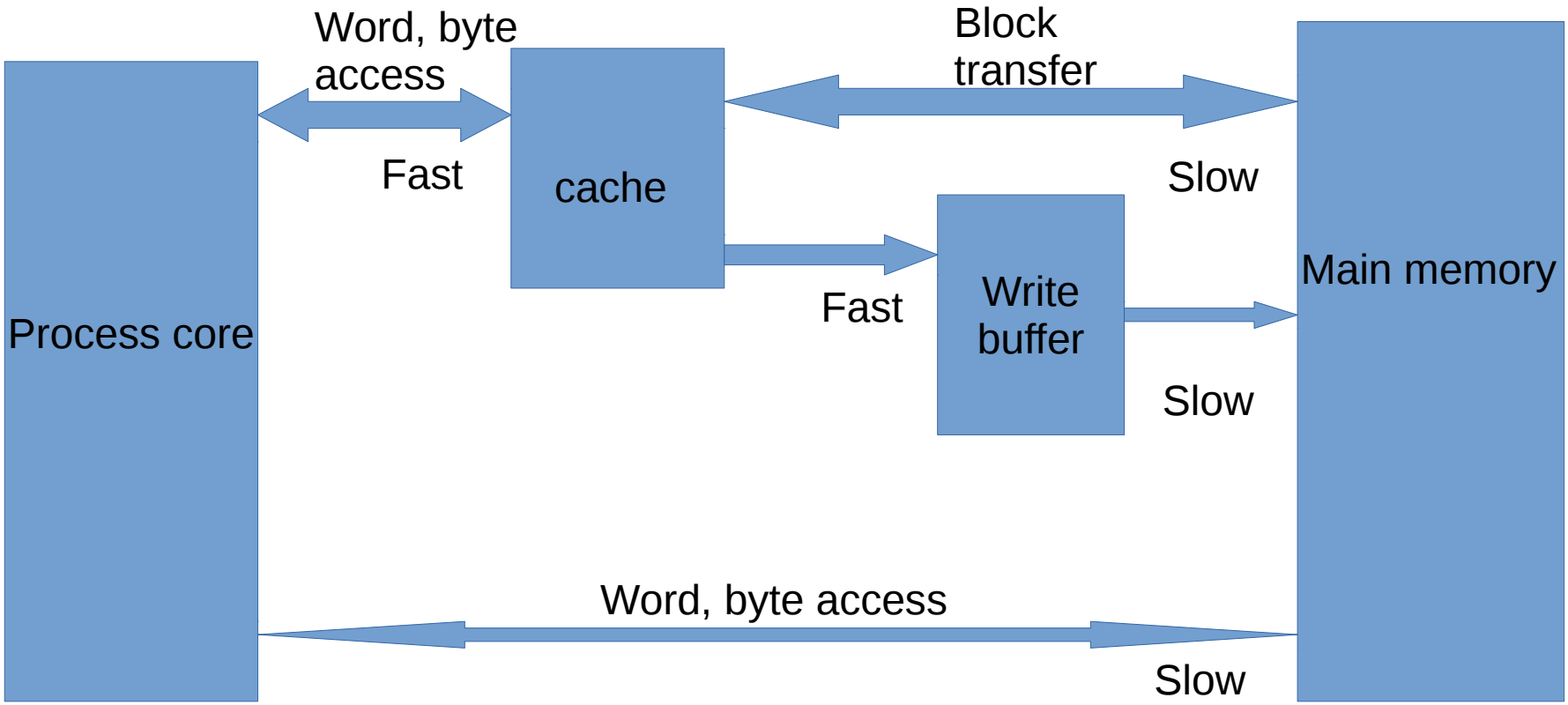
- Small memory placed between processor and main memory to store recently accessed transactions and make memory access faster .



Cached system

Write Buffer

- The write buffer acts as a temporary buffer that frees available space in the cache memory.
- The cache transfers a cache line to the write buffer at high speed and then the write buffer drains it to main memory at slow speed.



Cached system

Most modern desktop and server CPUs have at least three independent caches

- Instruction cache to speed up executable instruction fetch.
- Data cache to speed up data fetch and store.
- TLB(Translation Look-aside Buffer) used to speed up virtual-to-physical address translation for both executable instructions and data.
- Data cache generally is organized as hierarchy with multiple cache levels e.g. L1/L2 etc. This is also called as multi level caches.

The instruction and data cache

IDC operation:-

- The ARM720T contains an 8KB mixed Instruction and Data Cache(IDC).
- The cache comprises four segments of 64 lines each, each line containing eight words.
- The IDC is always reloaded a line at a time. The IDC is enabled or disabled using the ARM720T Control Register and is disabled on HRESETn.
- Note:- The MMU must never be disabled when the cache is on.
- However, you can enable the two devices simultaneously with a single write to the "*Control Register*".

Cachable bit:--

The C bit determines if data being read can be placed in the IDC and used for subsequent read operations. Typically, main memory is marked as cachable to improve system performance,and I/O space is marked as noncachable to stop the data being stored in the ARM720T cache.

Cachable reads (C=1)

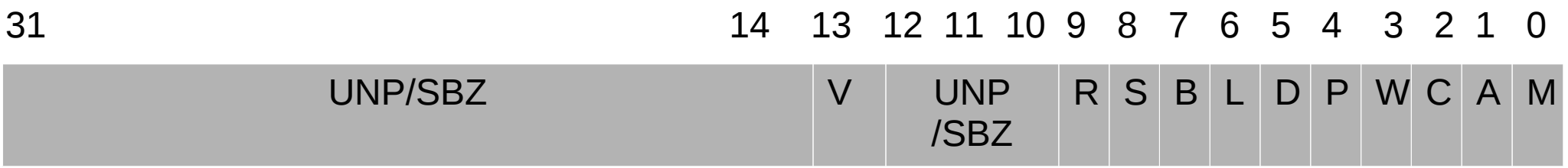
A line fetch of eight words is performed when a cache miss occurs in a cachable area of memory, and it is randomly placed in a cache bank.

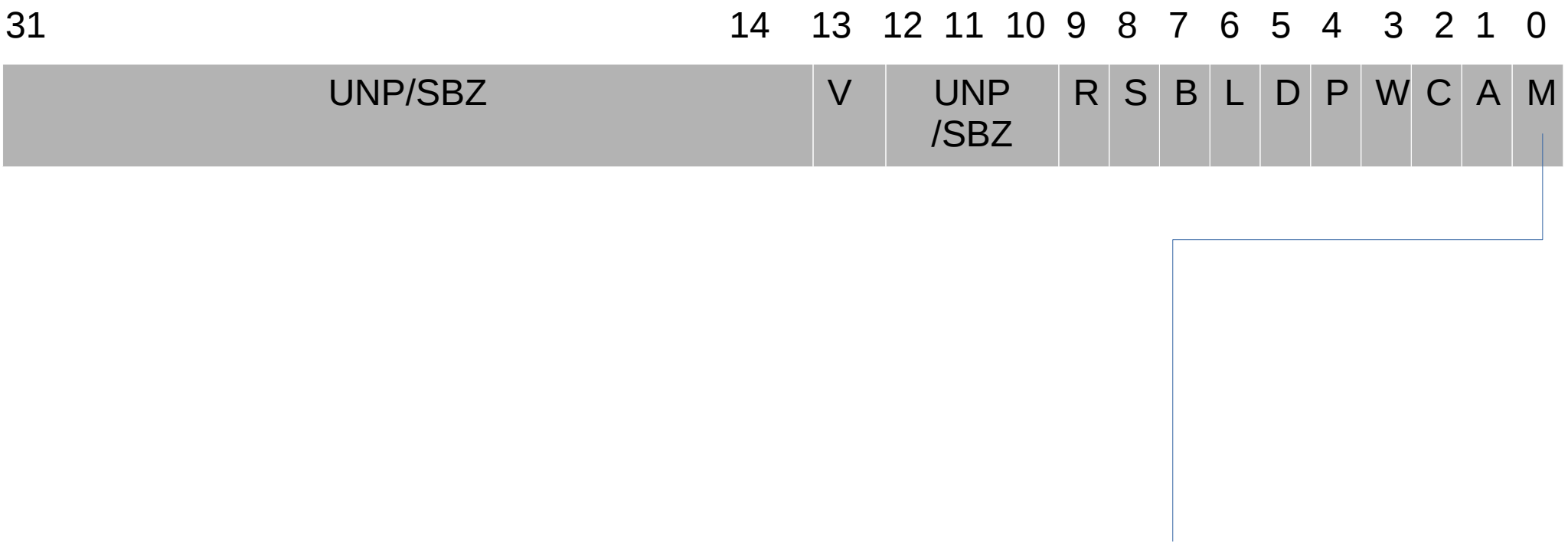
Note:- Memory aborts are not supported on cache line fetches and are ignored.

Uncachable reads (C=0)

An external memory access is performed and the cache is not written.

Control Register

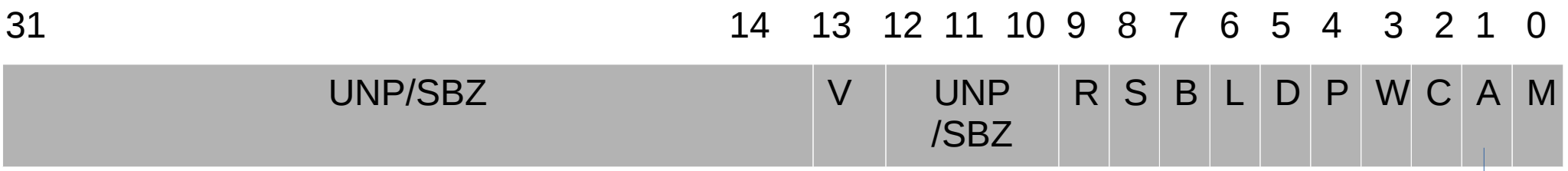




M Bit

MMU enable/disable:

0 = MMU disabled
1 = MMU enabled

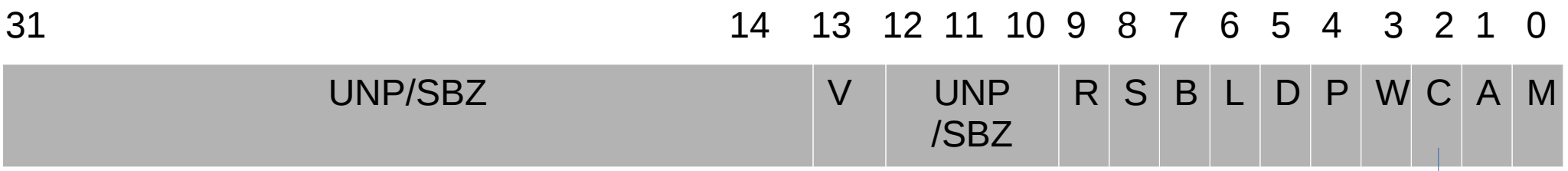


A Bit

Alignment fault enable/disable:

0 = Address Alignment Fault Checking disabled

1 = Address Alignment Fault Checking enabled

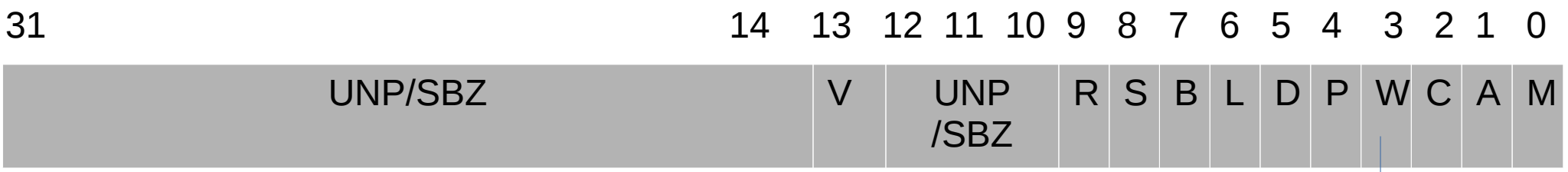


C Bit

Cache enable/disable:

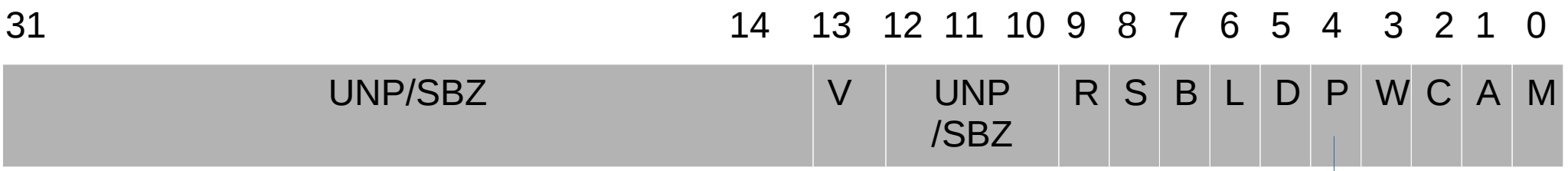
0 = Instruction and/or Data Cache (IDC) disabled

1 = Instruction and/or Data Cache (IDC) enabled



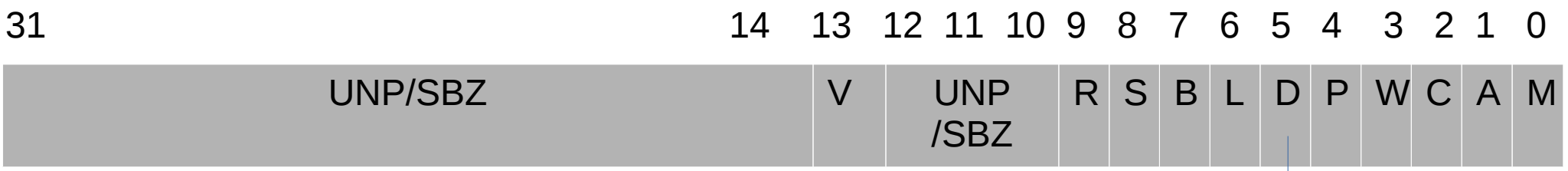
W Bit
Write buffer enable/disable:

0 = Write Buffer disabled
1 = Write Buffer enabled



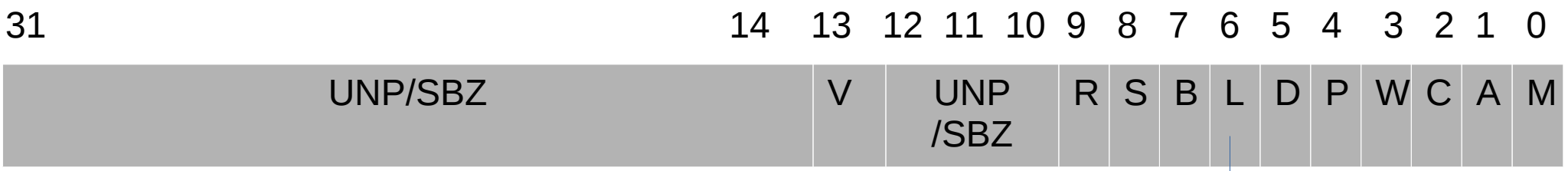
P Bit

When read, returns 1.
When written, is ignored



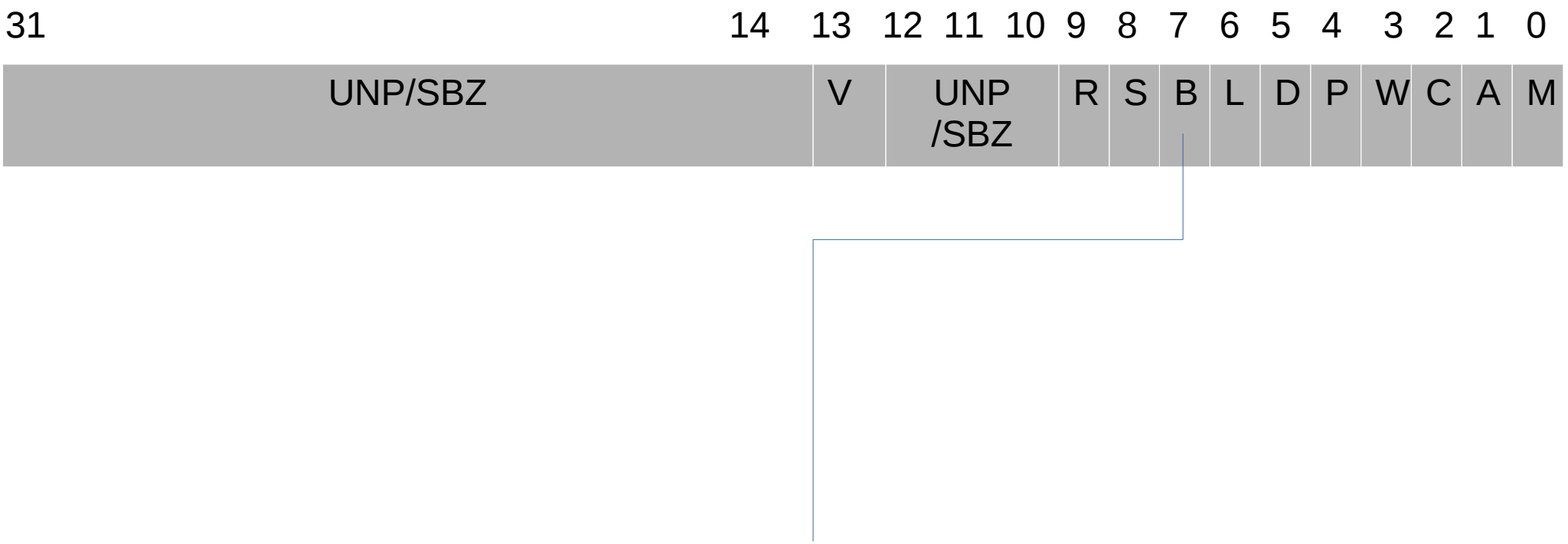
D Bit

When read, returns 1.
When written, is ignored.



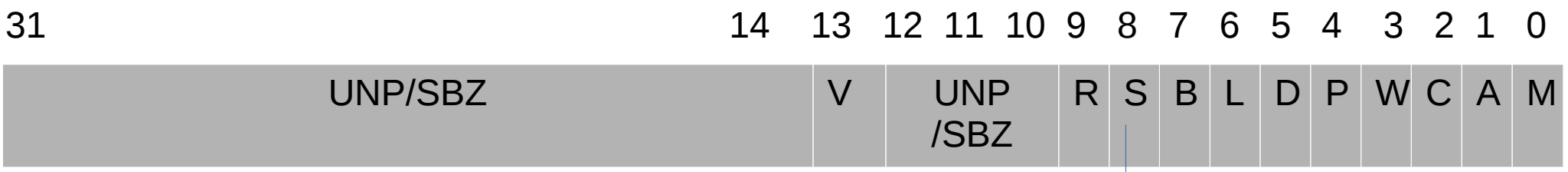
L Bit

When read, returns 1.
When written, is ignored.



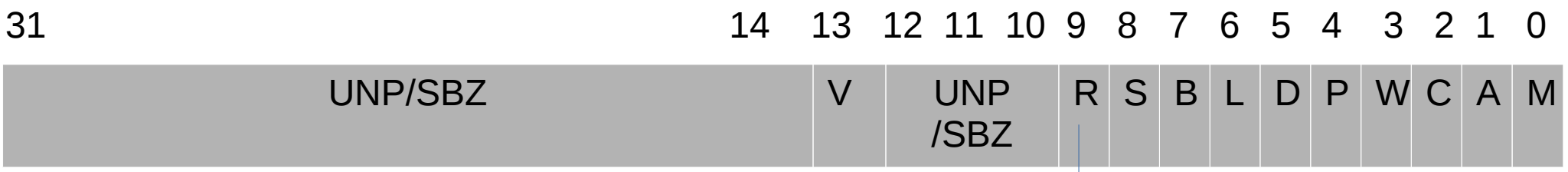
B Bit

Big-endian/little-endian:
0 = Little-endian operation
1 = Big-endian operation.

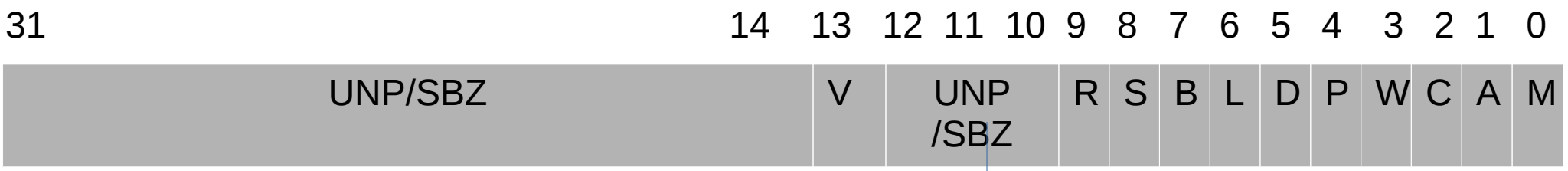


S Bit

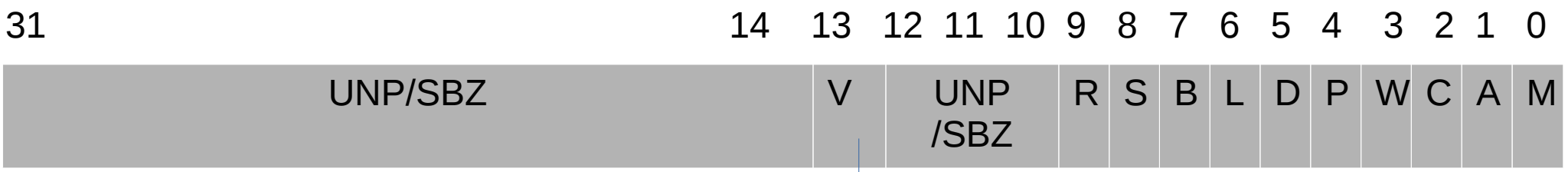
System protection: Modifies the MMU protection system.



R Bit
ROM protection: Modifies the MMU protection system.



Bits 12:10
When read, this returns an Unpredictable value.
When written, it Should Be Zero, or a value read from these bits on the same processor.



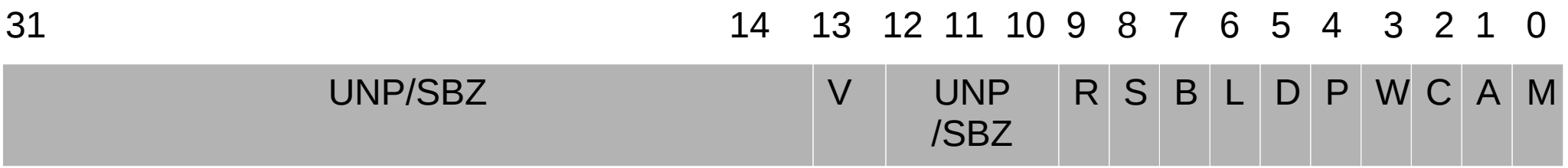
V Bit

Location of exception vectors:

0 = low addresses

1 = high addresses.

The value of the V bit reflects the state of the VINITHI External input, sampled while HRESETn is LOW



Bits 31:14

When read, this returns an Unpred ictable value.

When written, it Should Be Zero, or a value read from these bits on the same processor

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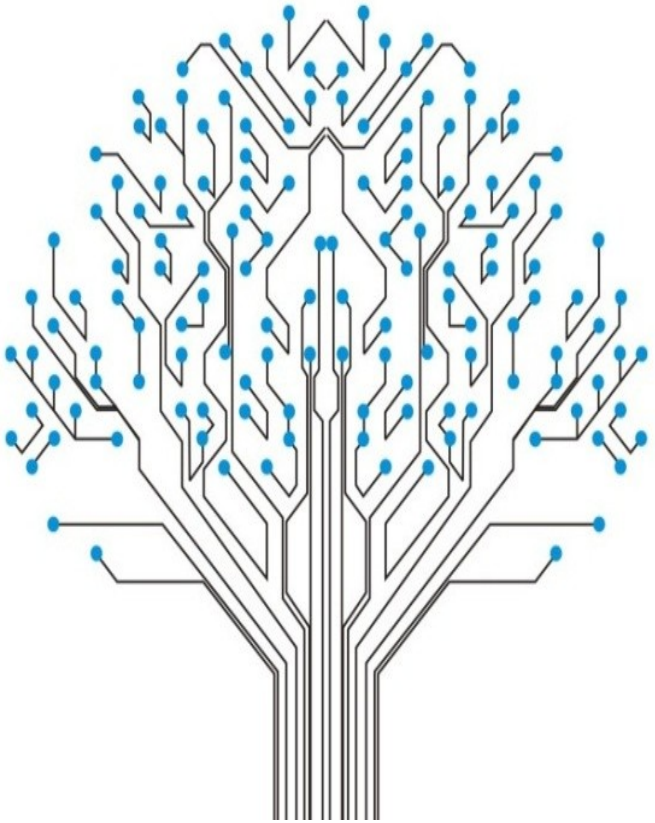
Intelligence Of Things

Thank you



Fairness

Learning

Responsibility

Innovation

Respect