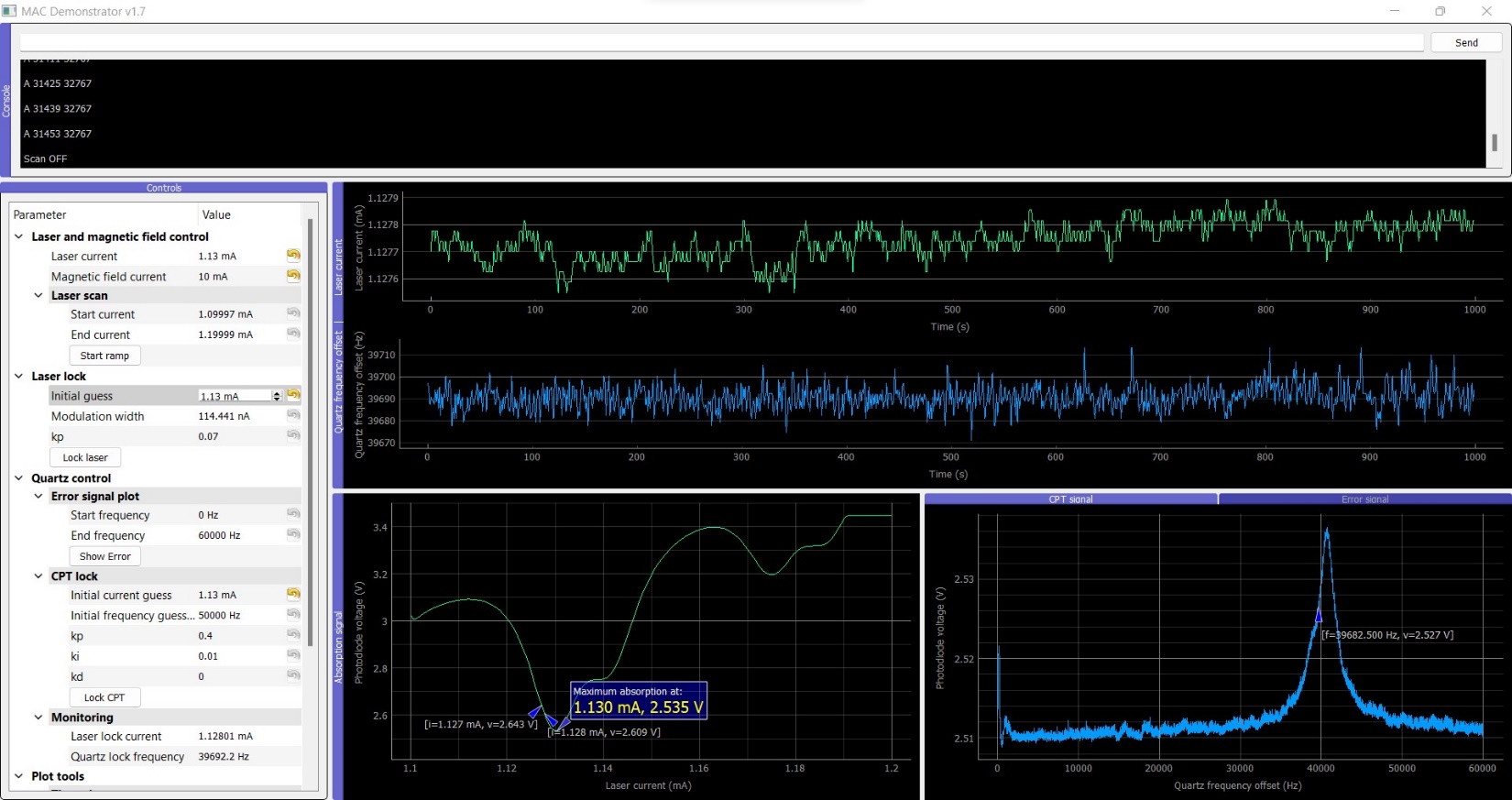
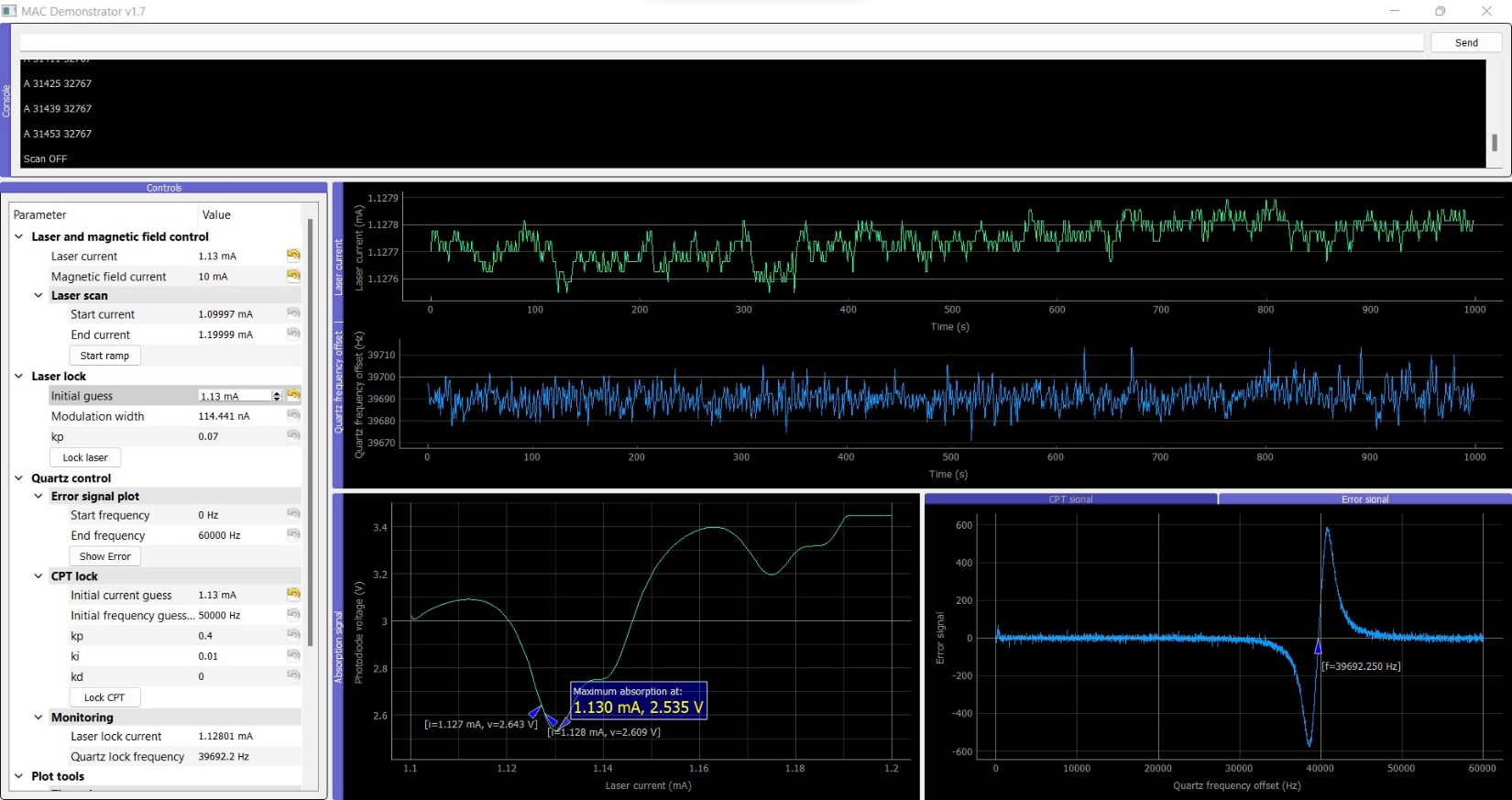
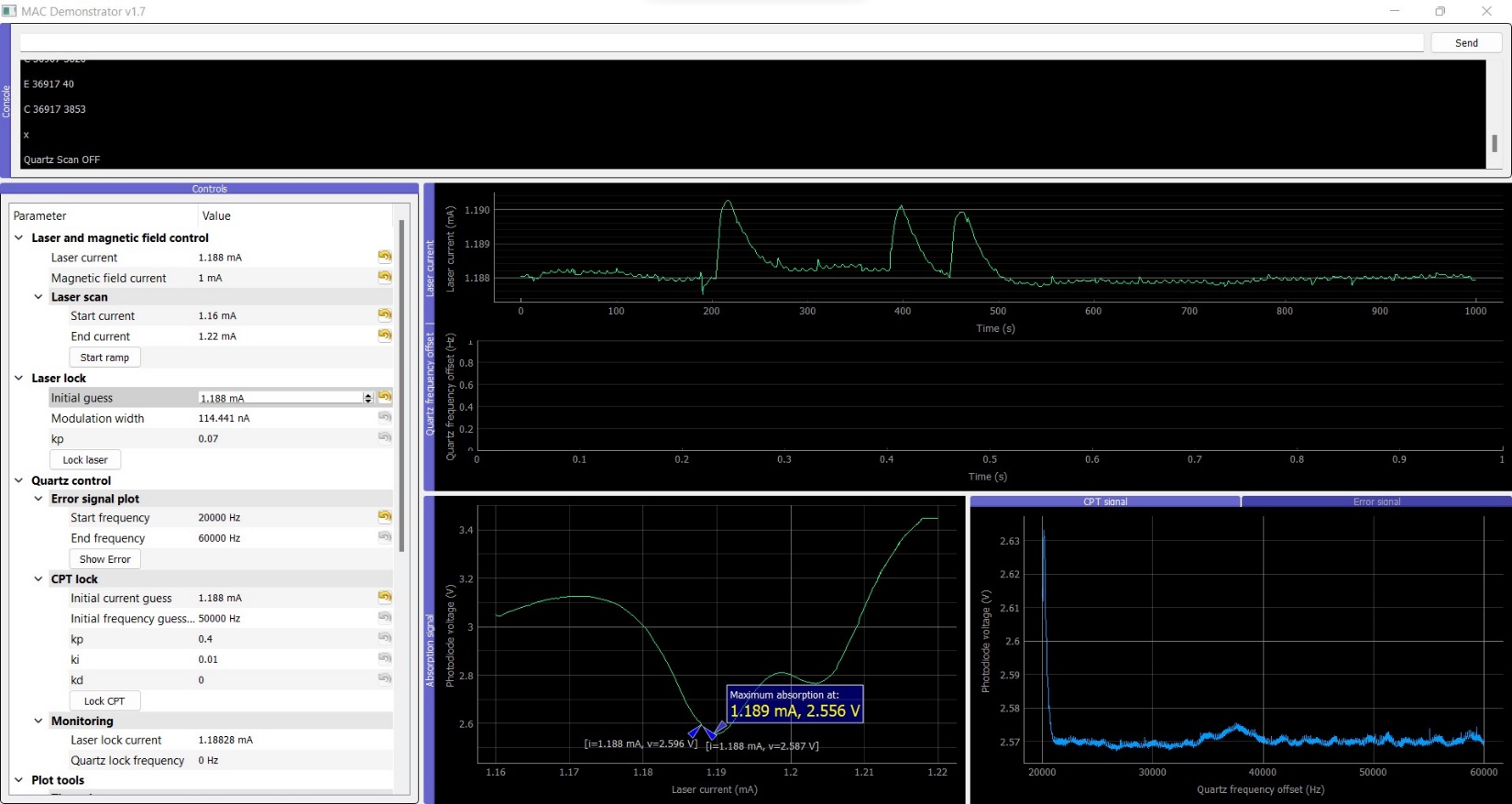
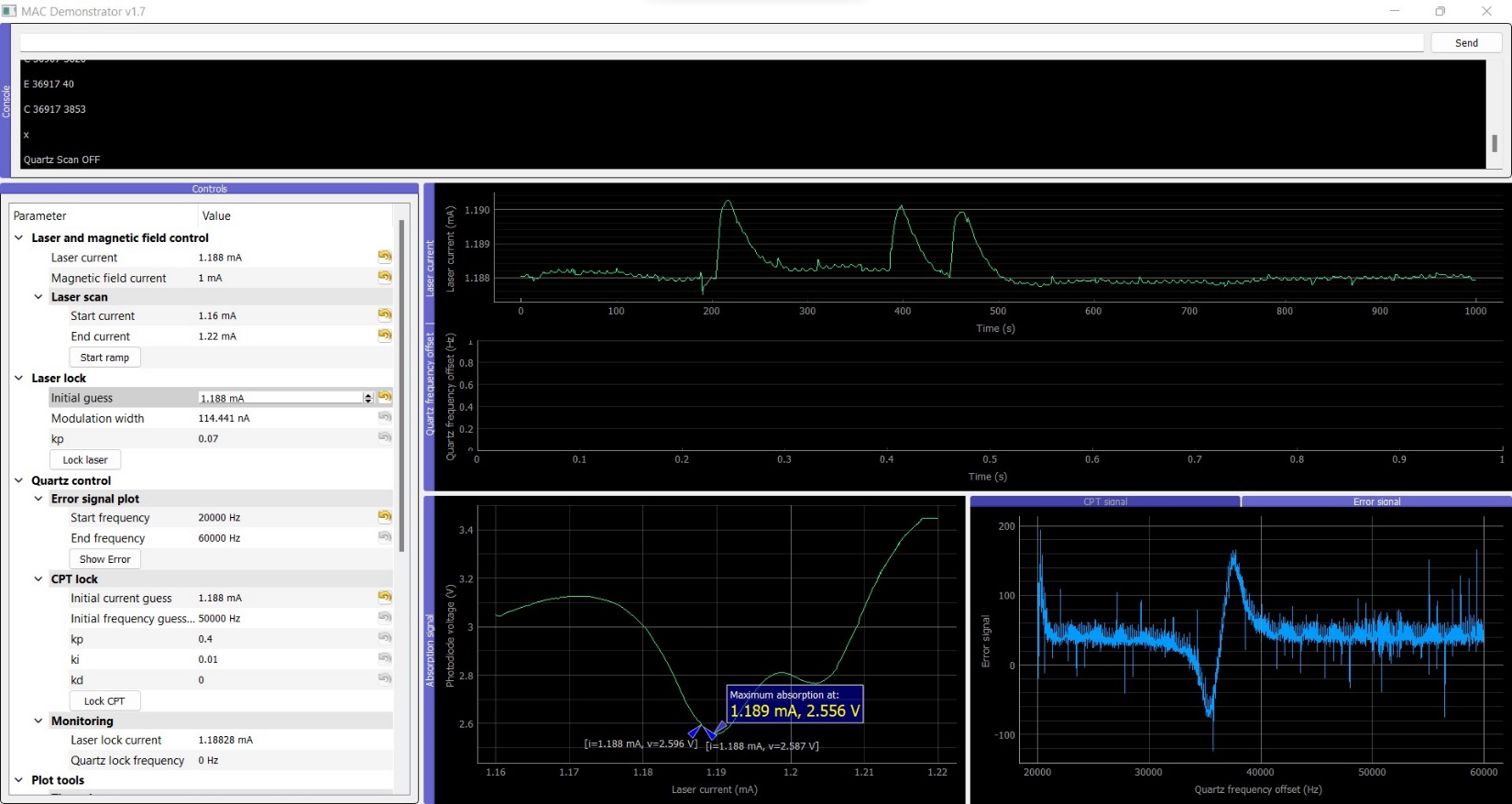
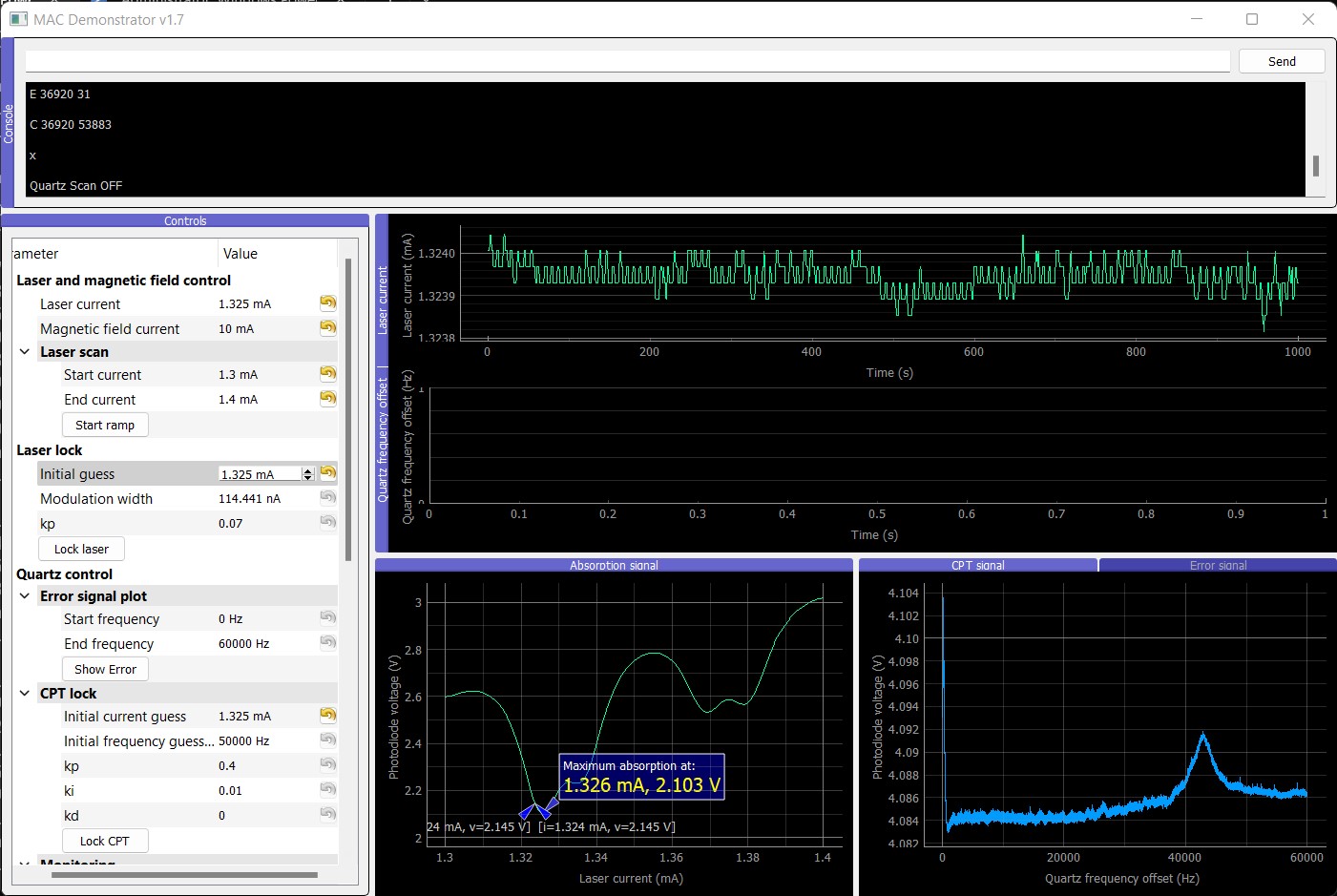
# Testing physical packages:

Clock 1 + Physical Package 1:



Clock 1 + Physical Package 2:

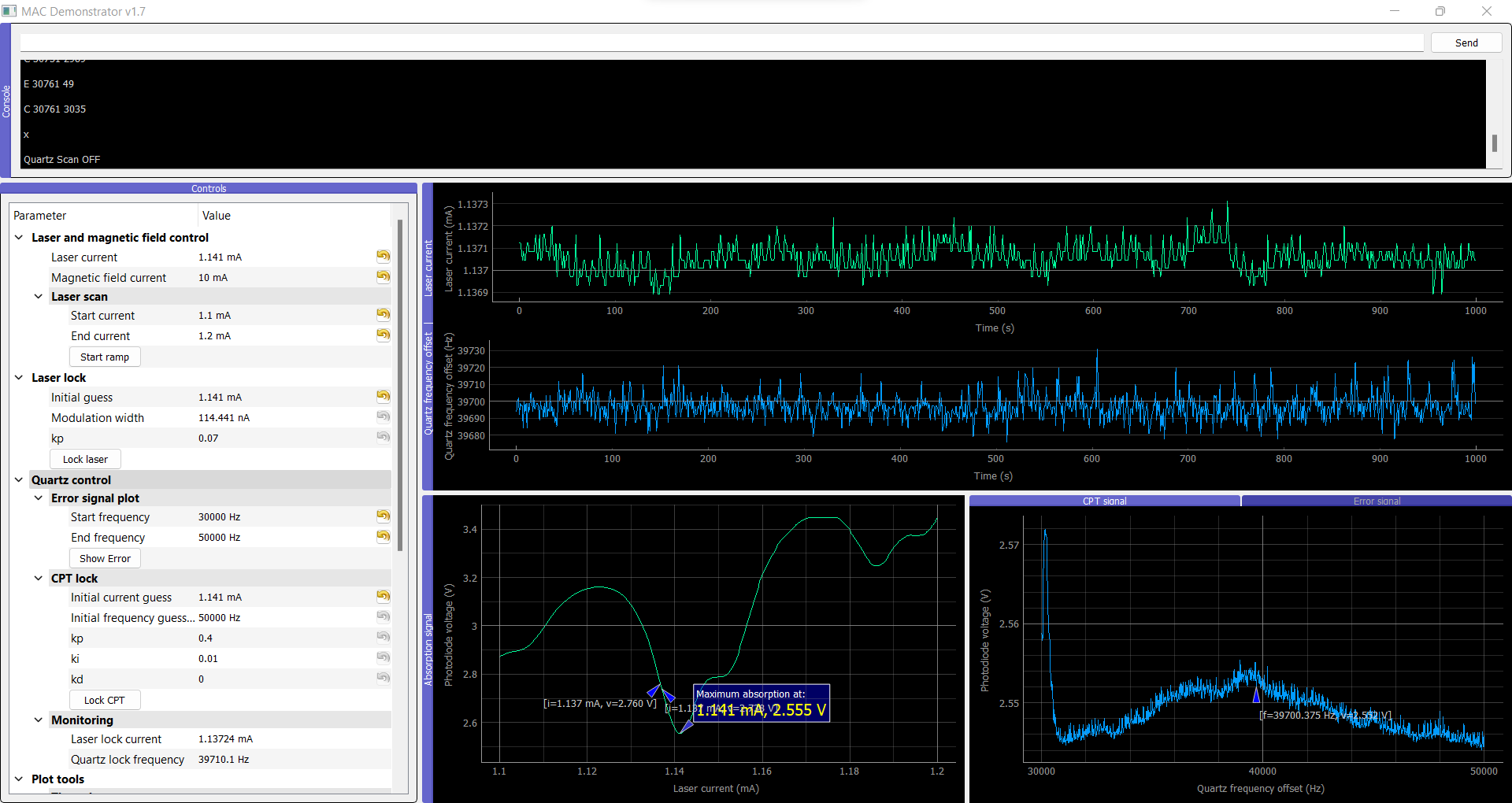


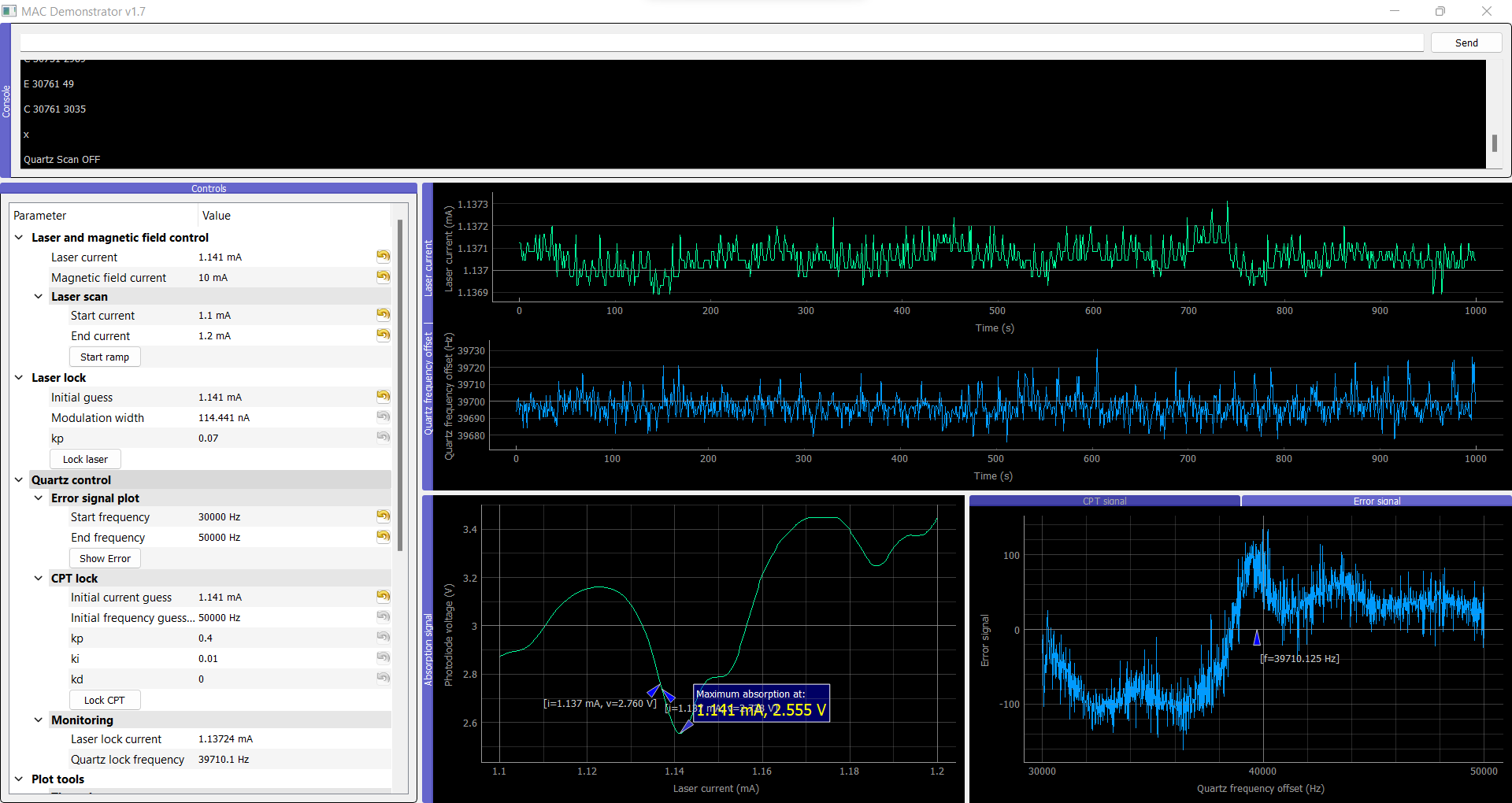
Clock 1 + Physical Package 3:

Conclusion: Physical packages are working (some better that others)

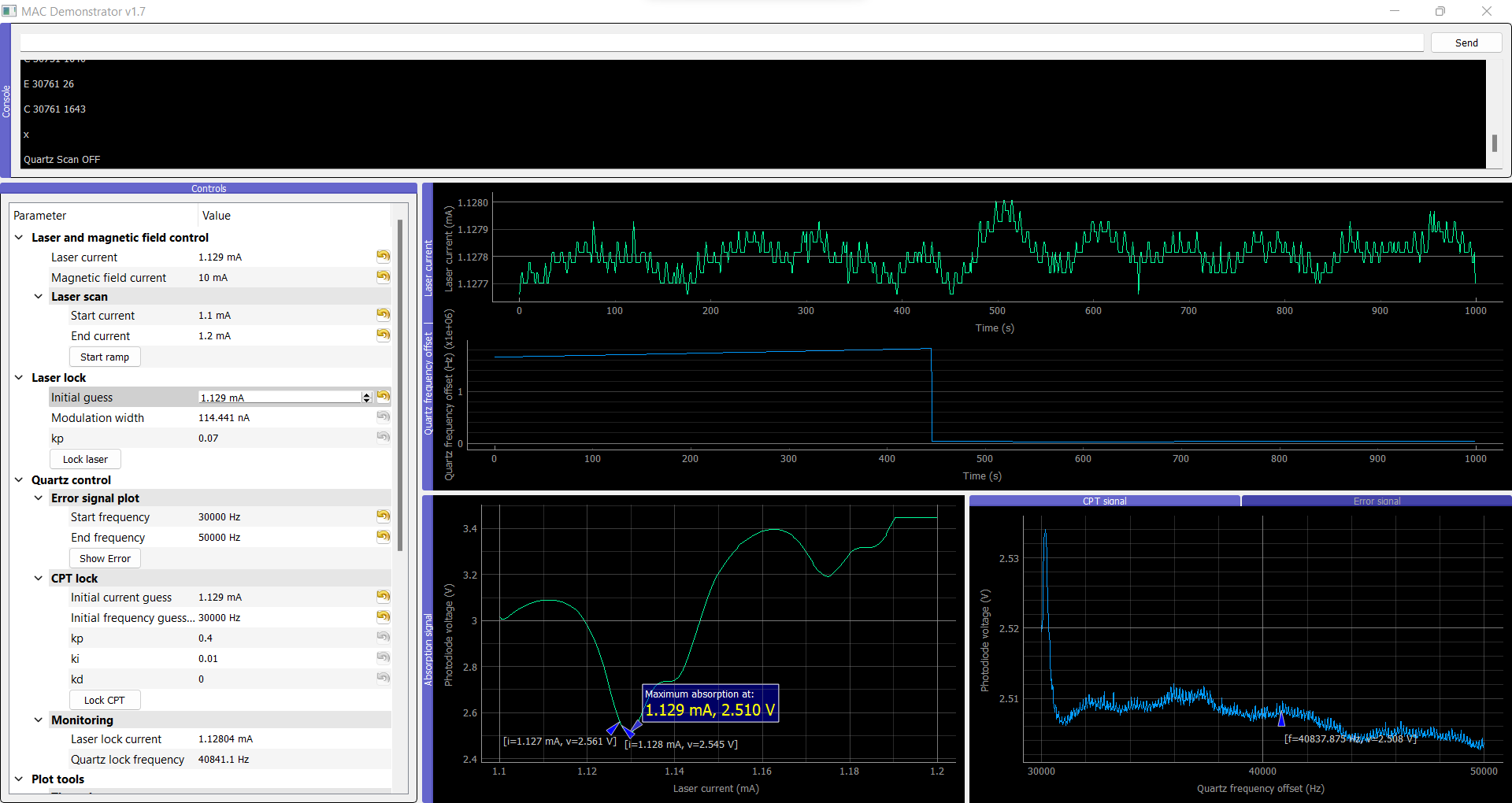
# Testing synthesizers

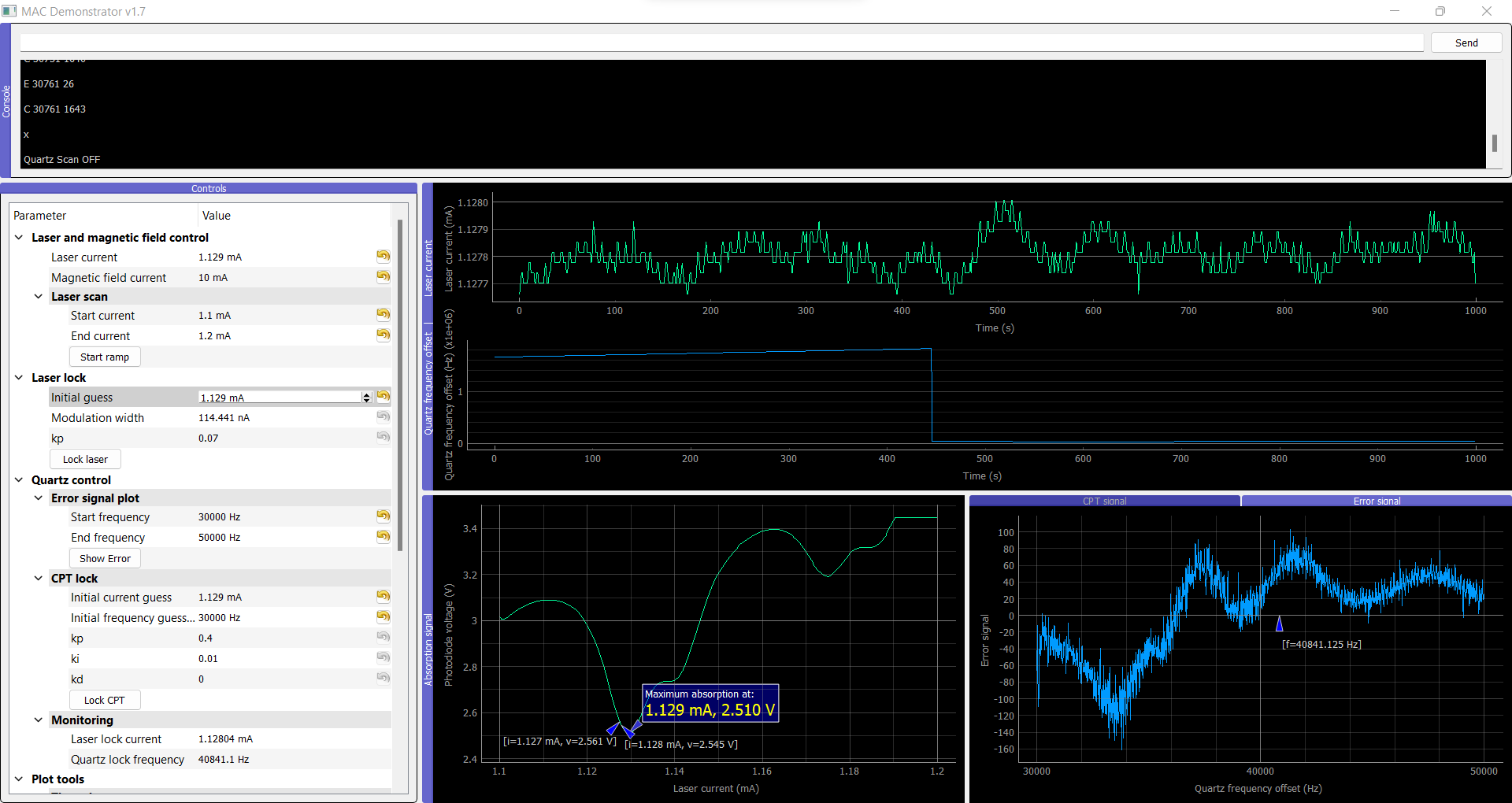
Working clock 1 with synthesizer 2:





Working clock 1 with synthesizer 3:





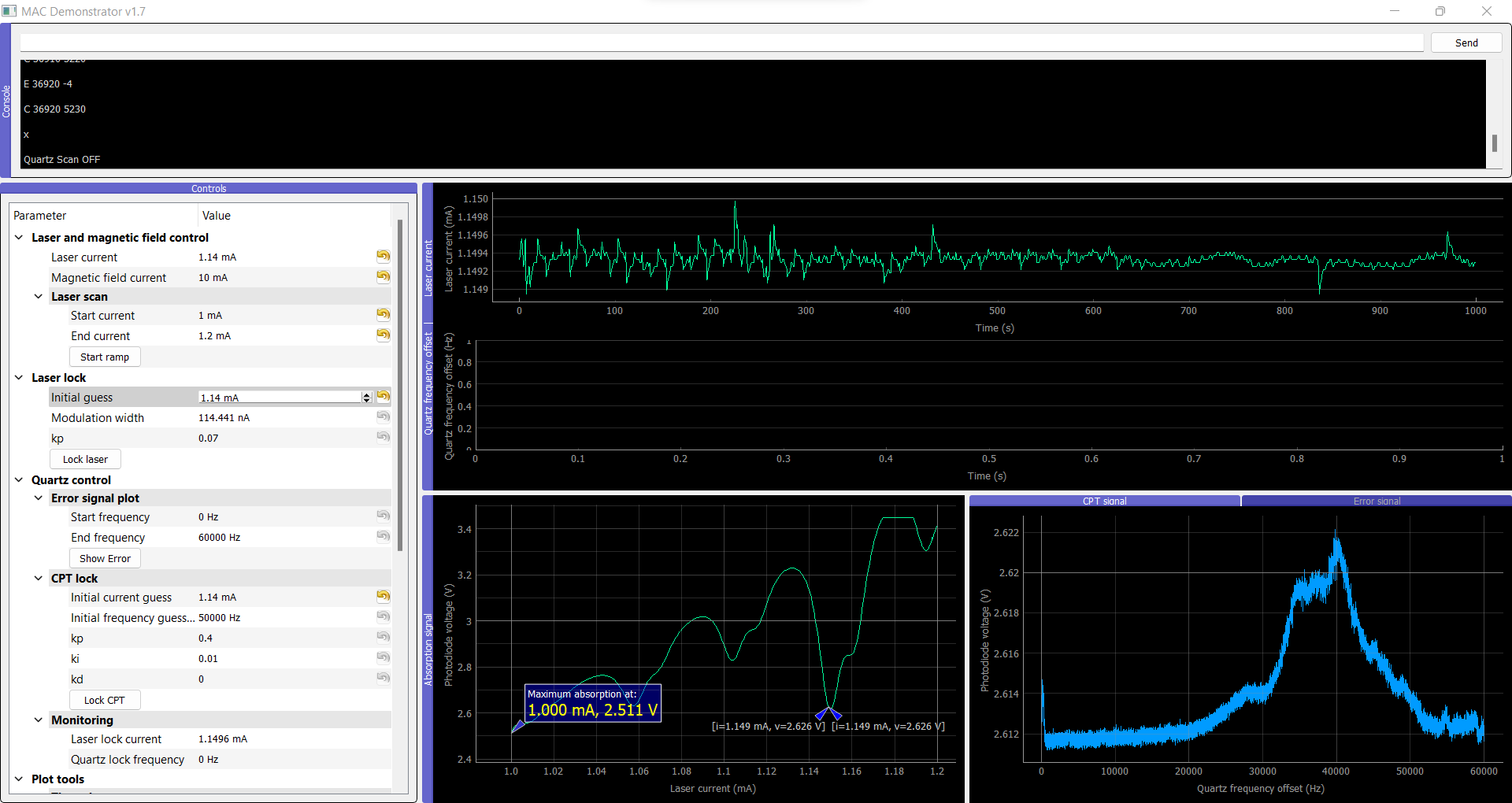
Testing frequency:

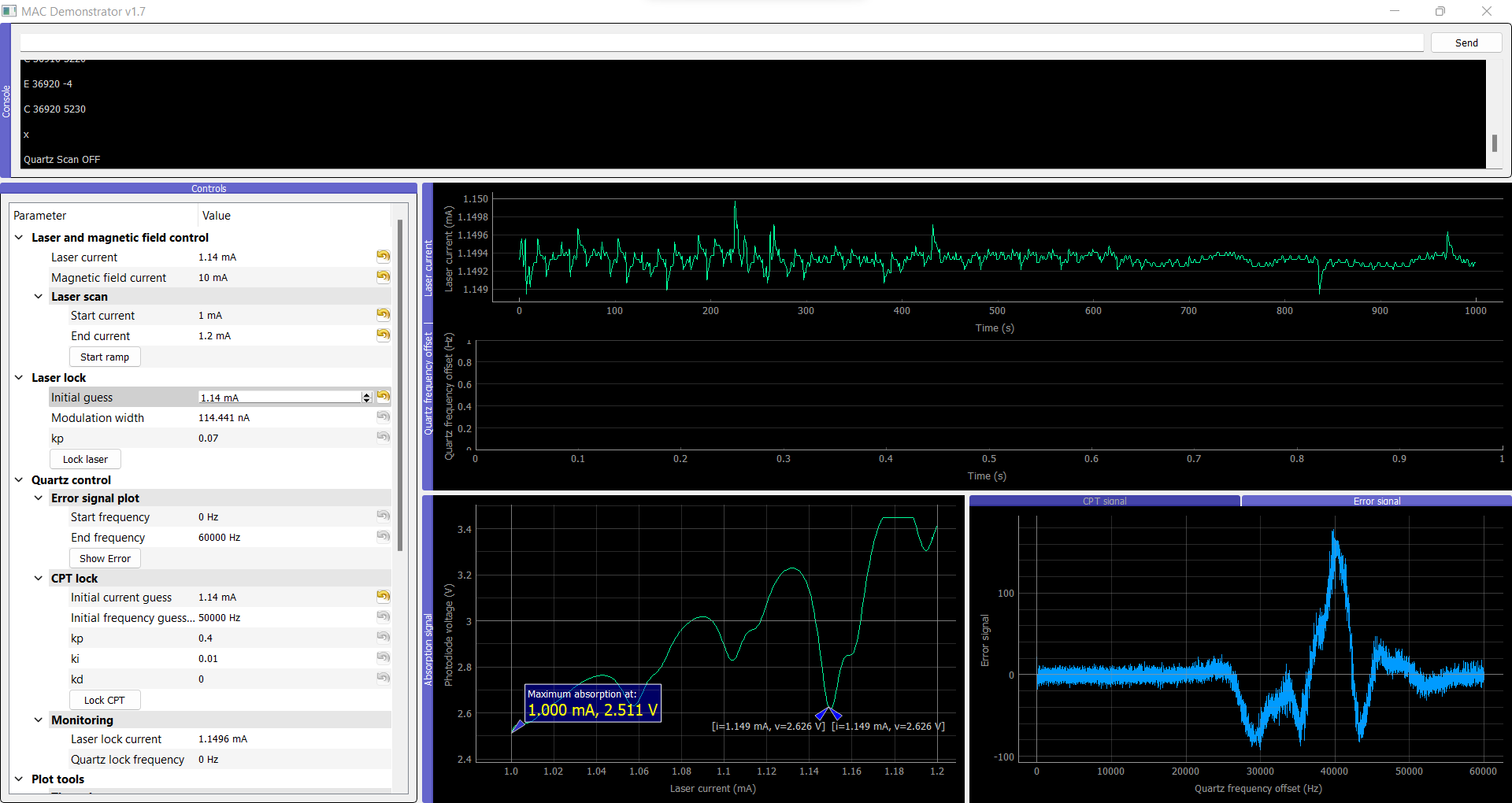
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Synthesizer | Desired freq (GHz) - Arduino | Desired freq (GHz) - Python | Measured | Measured 0 Hz at 1kHz span |
| 1 | 4.596373300 | 4.596374300 | 4.596300719 | 4.596300690 |
| 2 |  | 4.596374300 | 4.596302062 |  |
| 3 |  | 4.596374300 | 4.596306190 |  |
| Test |  |  |  |  |

Testing FSK modulation (at CF: 4.596304305 GHz and Span: 5 kHz):

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Synthesizer | Center frequency (estimated) | Left | Right | Deviation |
| 1 |  | 4.596304305 | 4.596306305 | 1 kHz |
| 2 |  | 4.596346475 | 4.596348487 | 1.01 kHz |
| 3 |  |  |  | 1 kHz |
| Test |  |  |  |  |

Synth 2 on clock 1 (power up):





Calibration:

Function “ADF4158\_Set\_CPT\_lock()”, set frequency: 4.5963733 GHz exactly

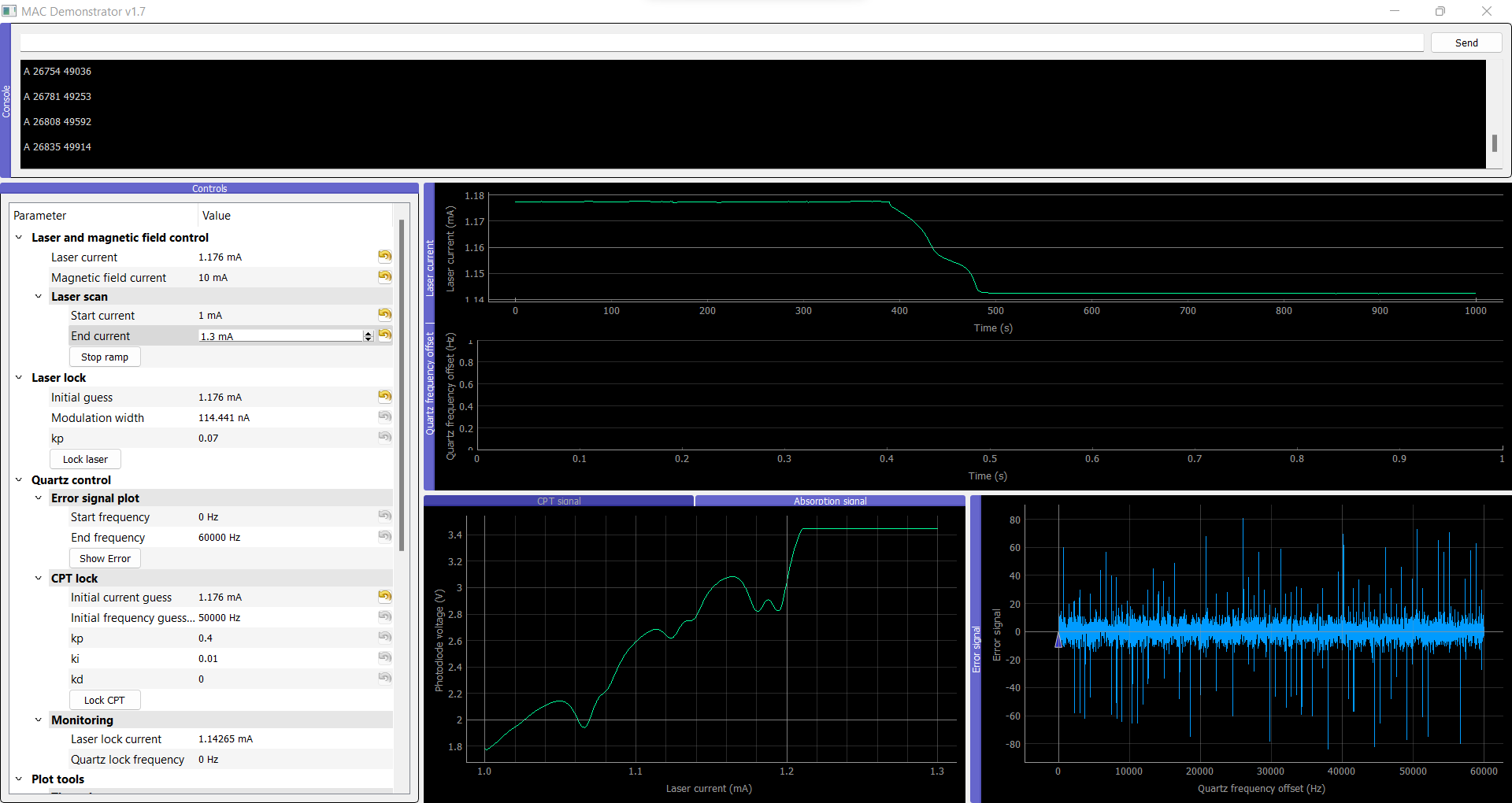
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Clock | Desired frequency | Set frequency | Measured frequency | Correction to match clock 1 | Comments: |
| 1 | **4596233150** | 4596373300 | **4596233150** | none | 0.00304914% error |
| 2 | **4596233150** | 4596373300 | 4596302150 | 4596372300 | 0.00154796% error. Difference is within the scan of 60 000 |
| 3 | **4596233150** |  |  |  |  |
| 4 | **4596233150** |  |  |  |  |

Conclusion: it’s not about the start frequency of the PLL.

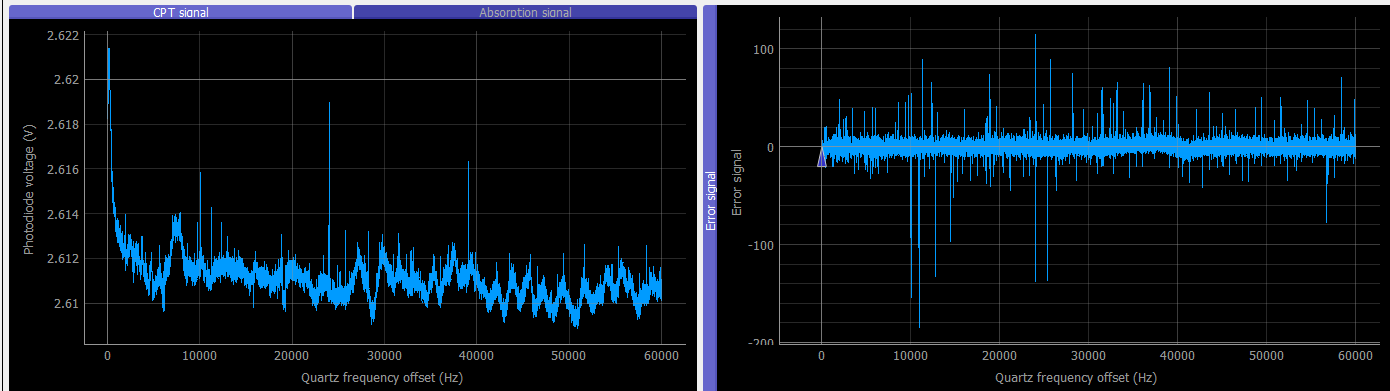
Test:

* Clock 2 + Temp controller 2 + Physical package 2 + Synthesizer 1 = Small improvement

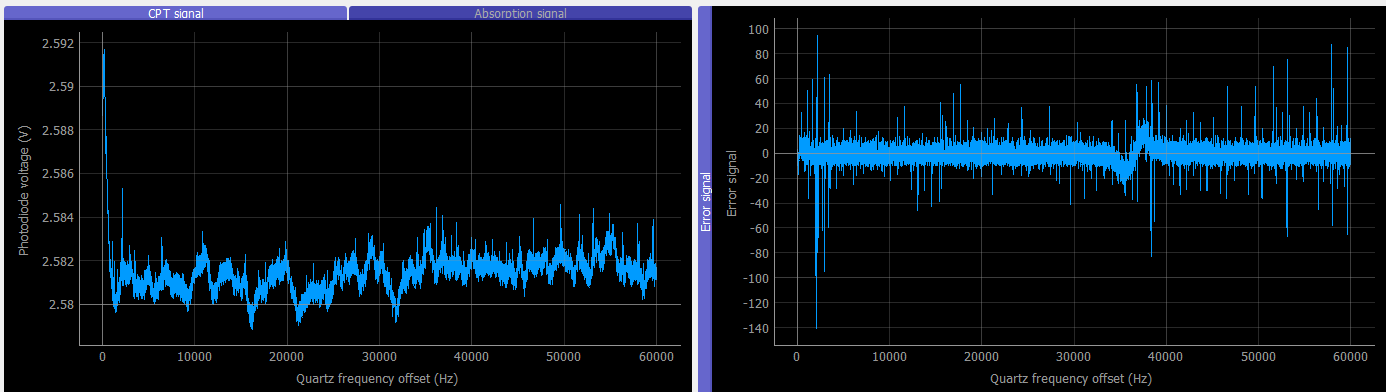
Before: After:

Before:

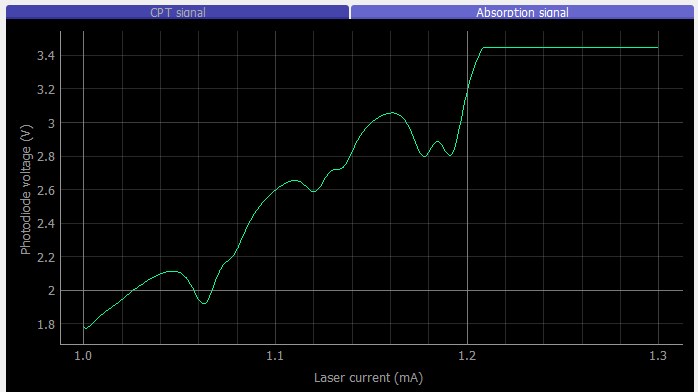


After:



Controller setpoint was 1750, setting at 1480:

Before: After:

Conclusion: Synthesizer can improve signal.

* Clock 2 + Temp controller 1 + Physical package 2 + Synthesizer 2 = Wasn’t able to remove temp controller

Copying the content of the temperature controller from clock 1 to clock 2:

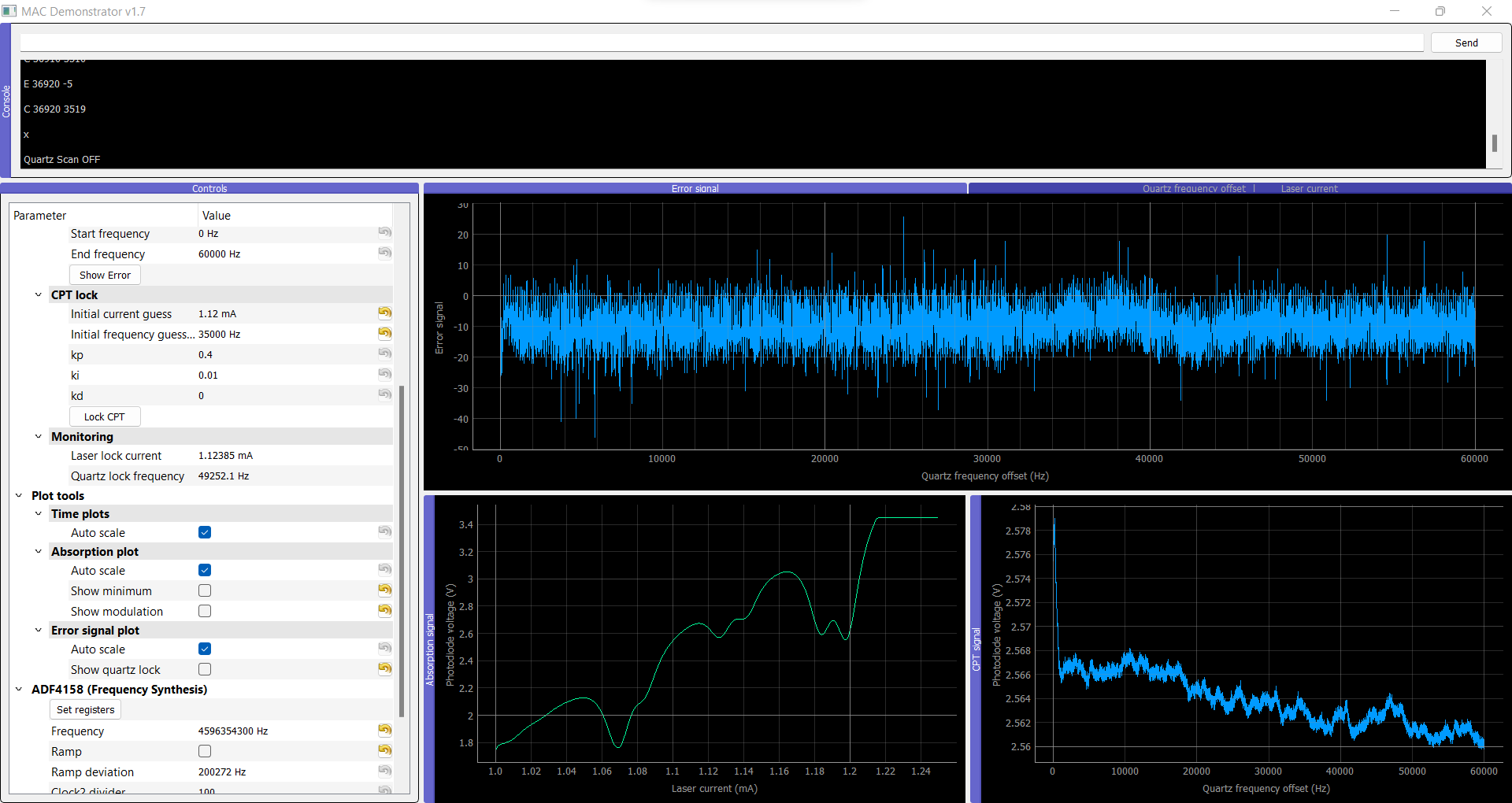
To read binary from Arduino:

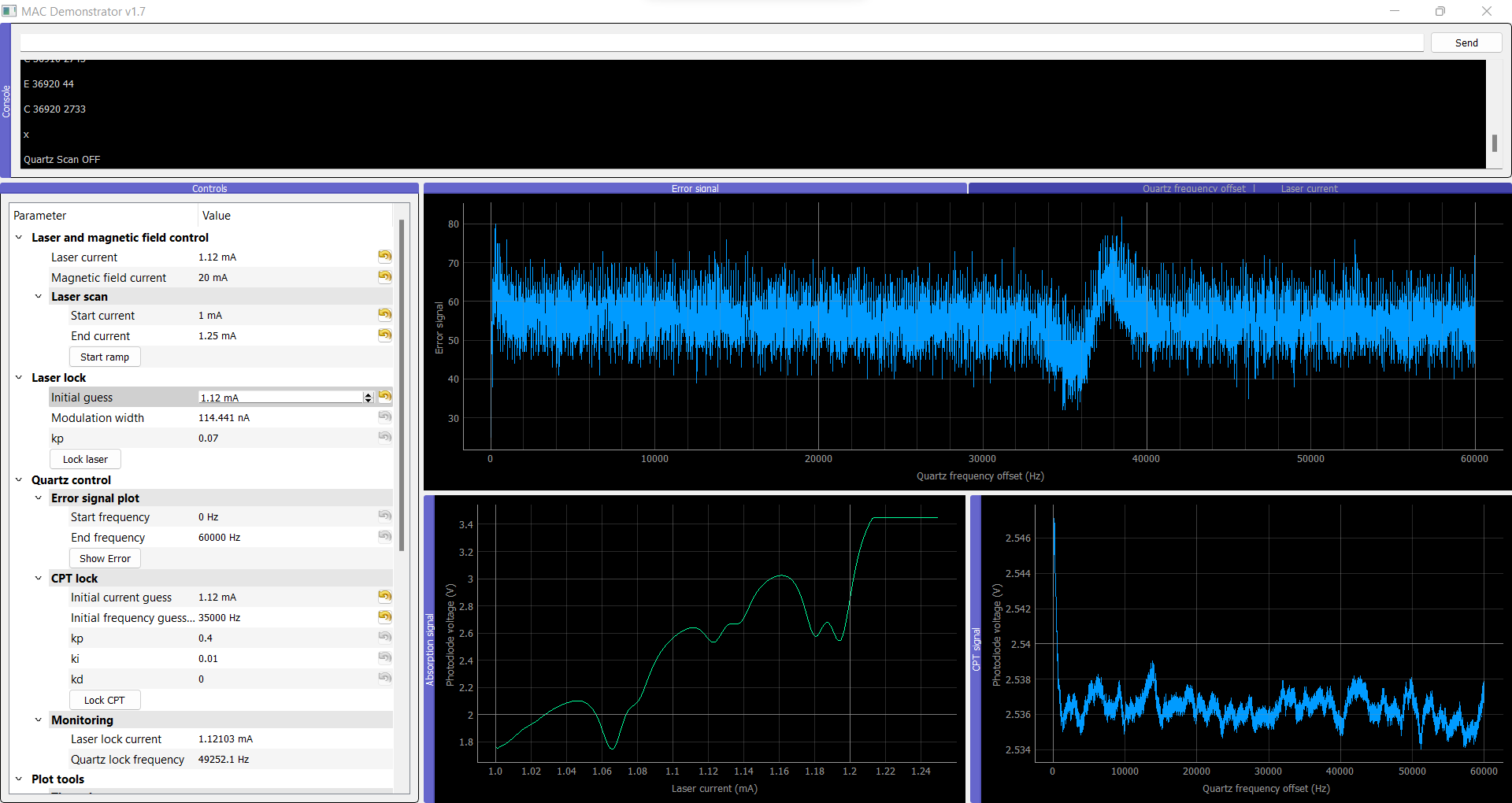
C:\Users\cmrivera\AppData\Local\Arduino15\packages\arduino\tools\avrdude\6.3.0-arduino17/bin/avrdude -CC:\Users\cmrivera\AppData\Local\Arduino15\packages\arduino\tools\avrdude\6.3.0-arduino17/etc/avrdude.conf -v -patmega32u4 -cavr109 -b57600 -PCOM18 -D -Uflash:r:readfile.hex:i

To write binary to Arduino:

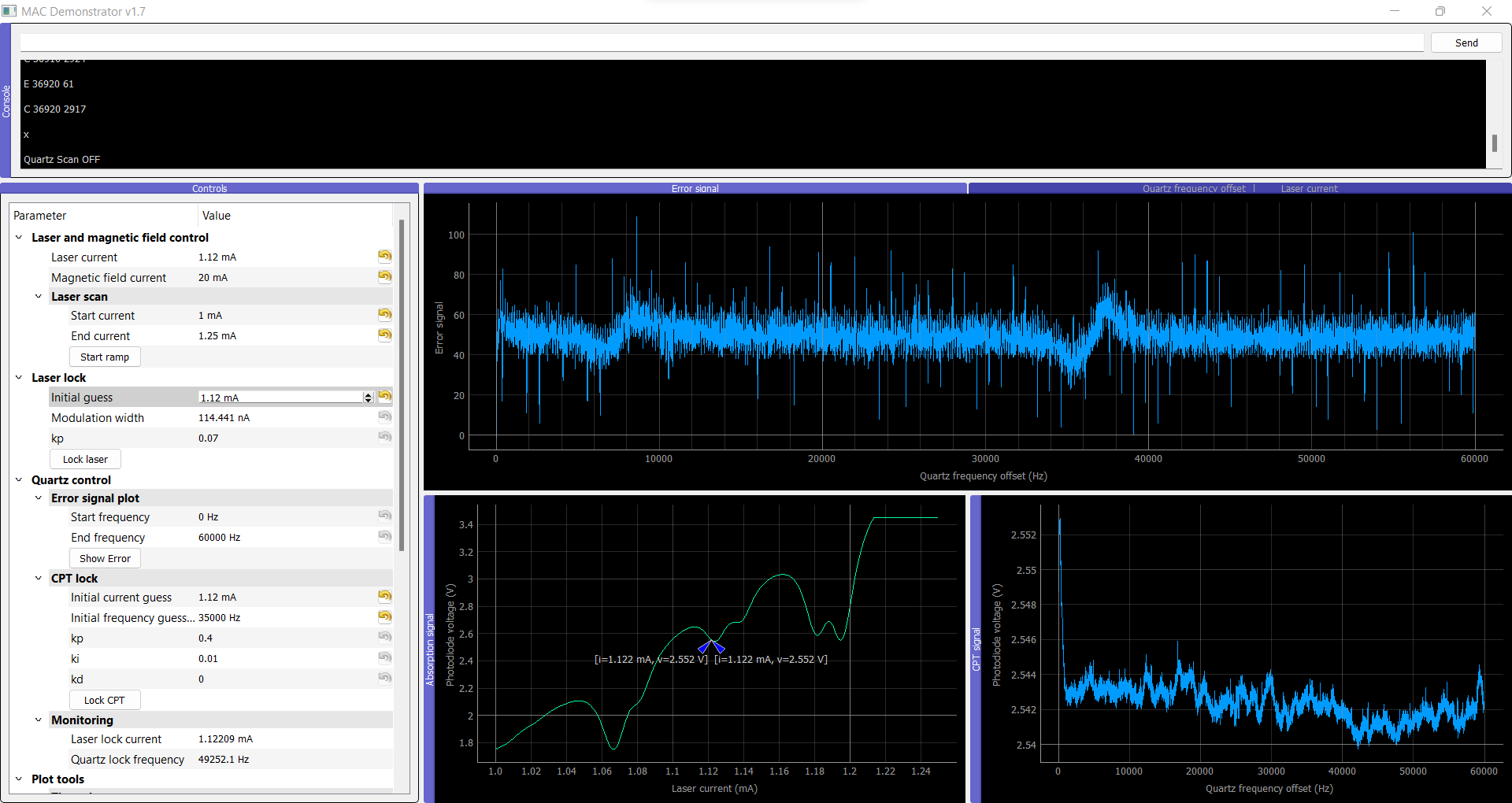
C:\Users\cmrivera\AppData\Local\Arduino15\packages\arduino\tools\avrdude\6.3.0-arduino17/bin/avrdude -CC:\Users\cmrivera\AppData\Local\Arduino15\packages\arduino\tools\avrdude\6.3.0-arduino17/etc/avrdude.conf -v -patmega32u4 -cavr109 -PCOM18 -b57600 -D -Uflash:w:C:\Users\cmrivera\Desktop\readfile.hex:i

Temp controller code cloned, Clock 2 with Synthesizer 2 and 1:

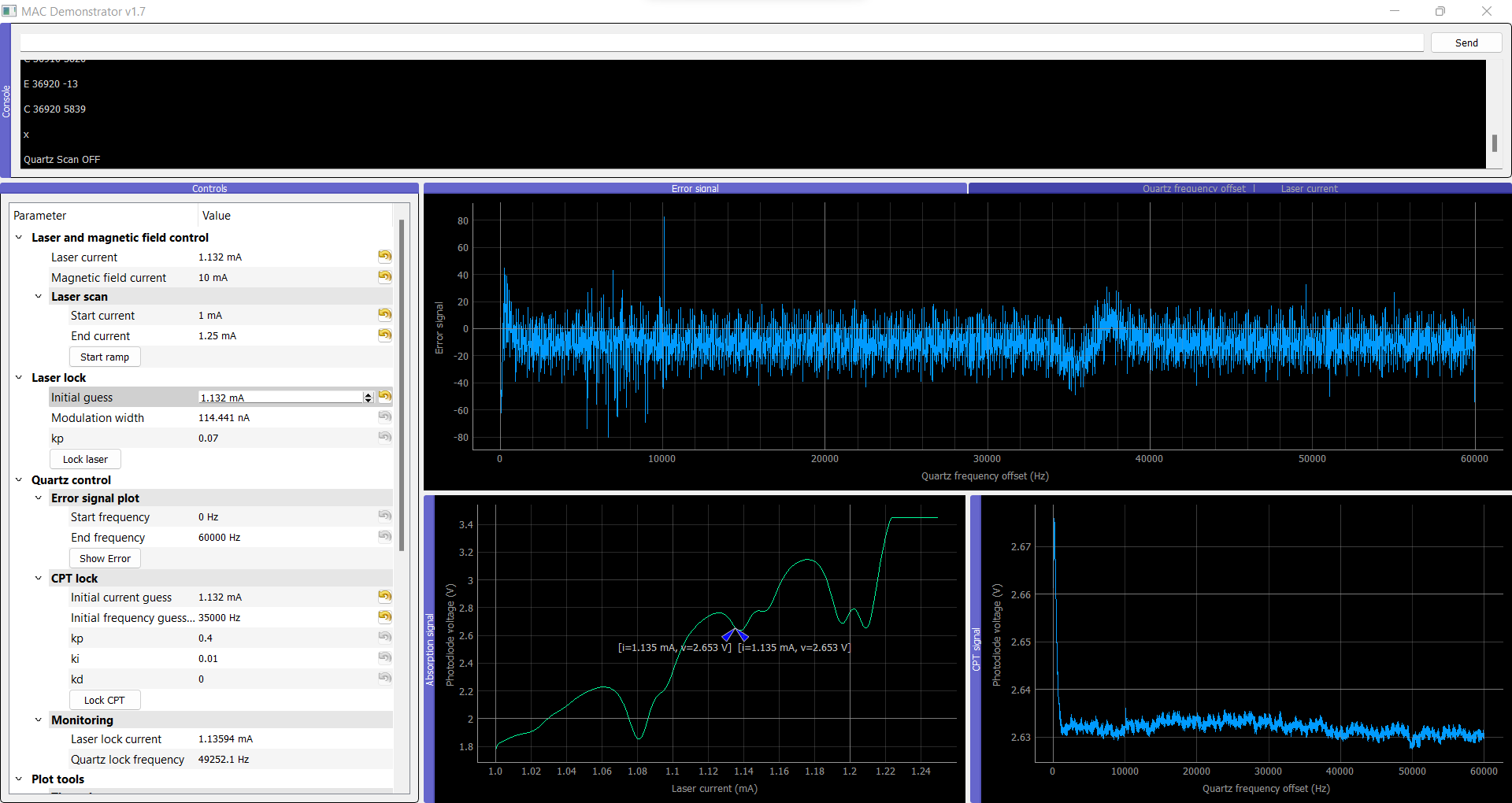




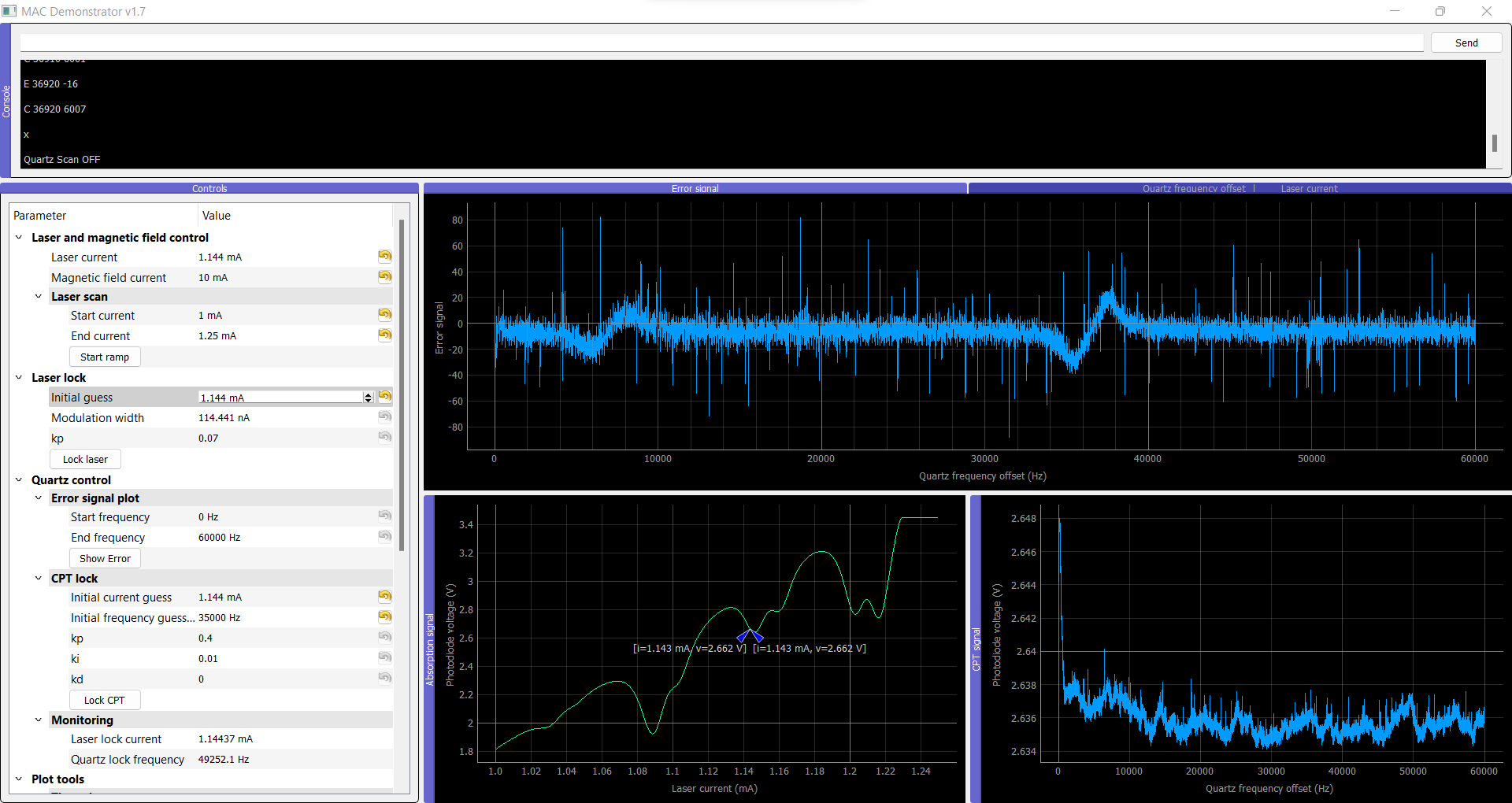
Temp controller circuit 1 in Clock 2 (With PP2 and S1):



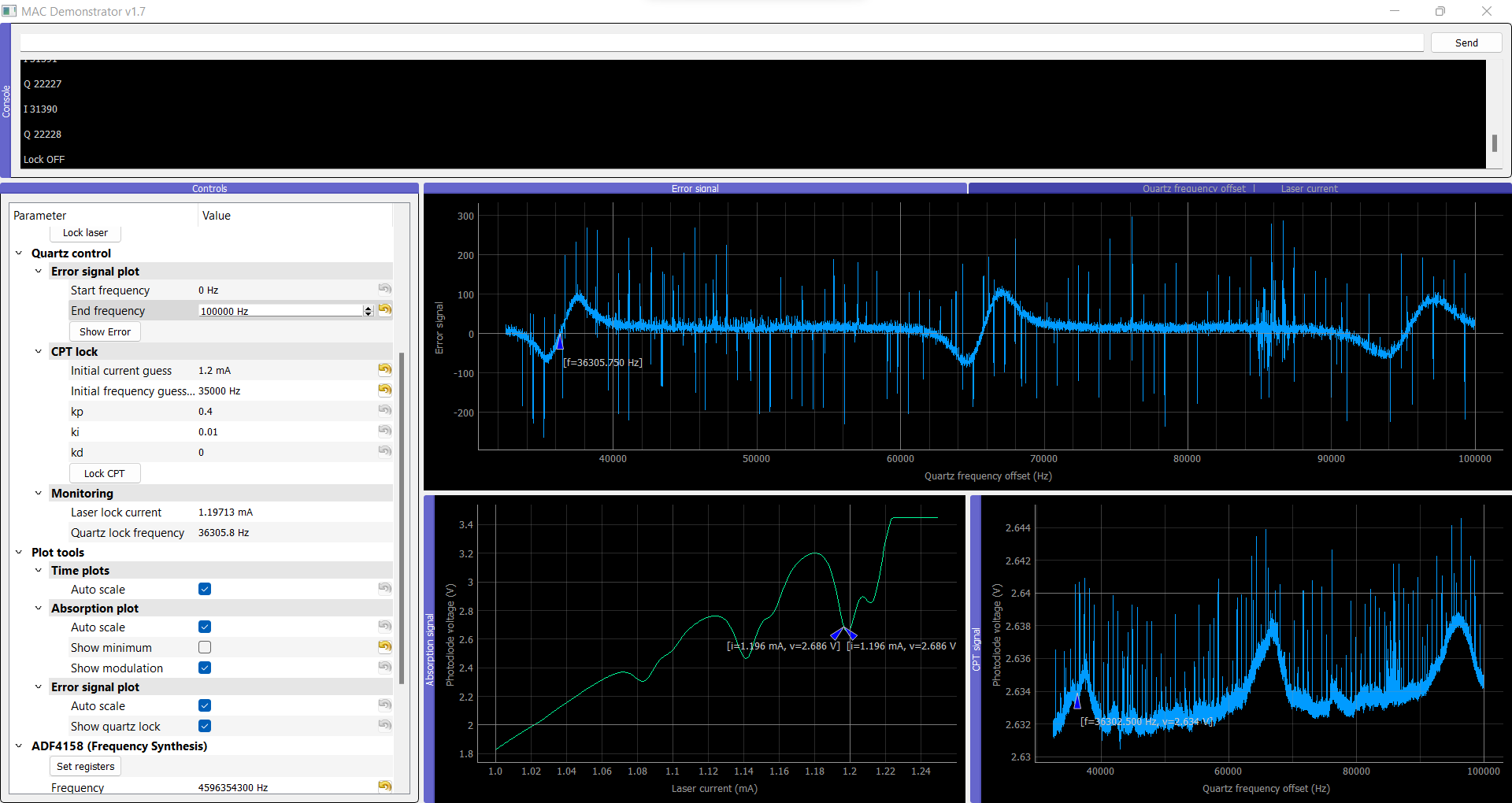
**Clock 2 – PP2 – Synth 1 – TC 2 (cloned 1) and Attenuator 2:**



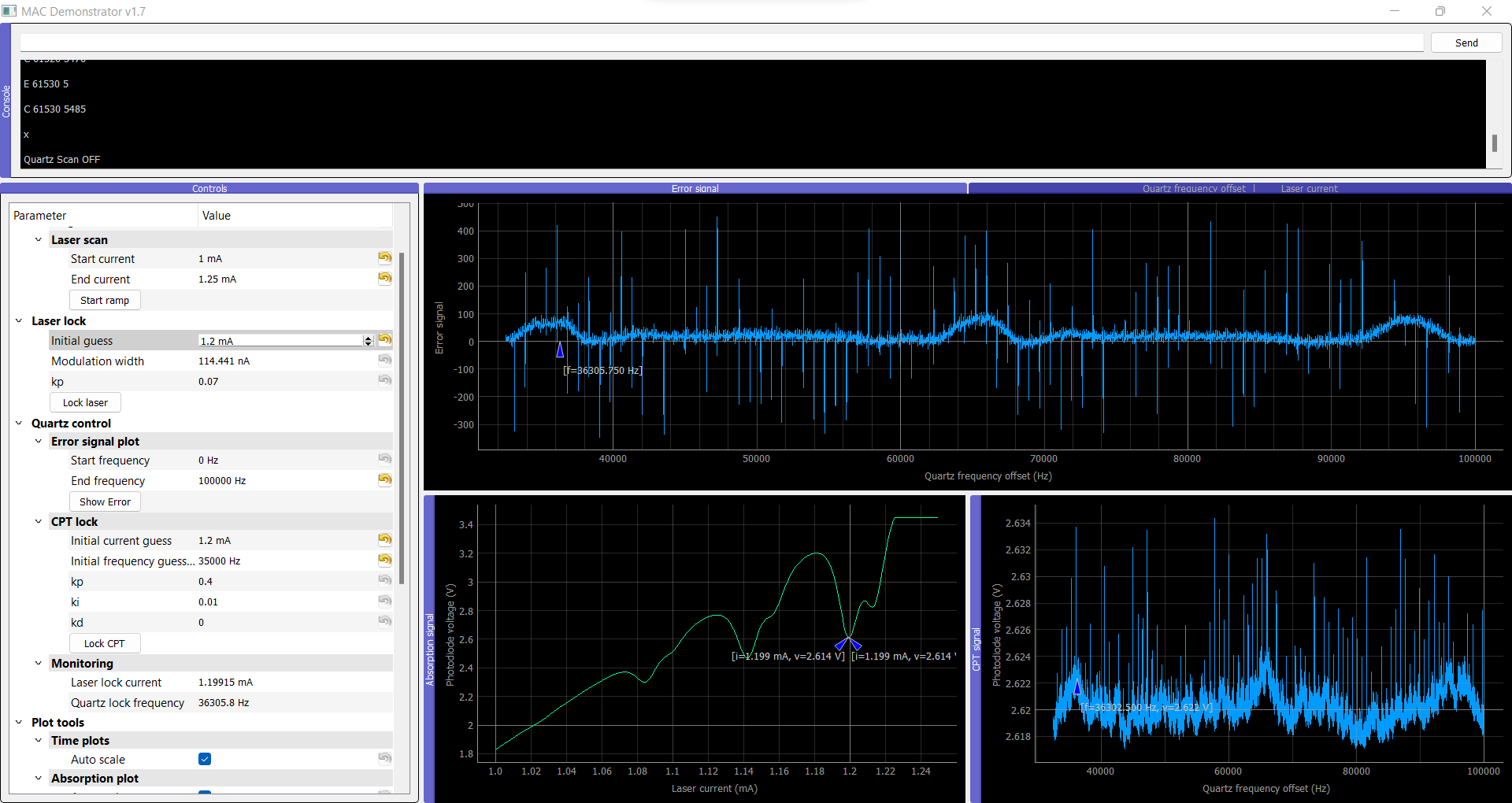
Clock 2 – PP2 – Synth 1 – TC 2 (cloned 1) and Attenuator 1:



Clock 2 – PP2 – Synth 1 – TC 2 (cloned 1) and no Attenuator:



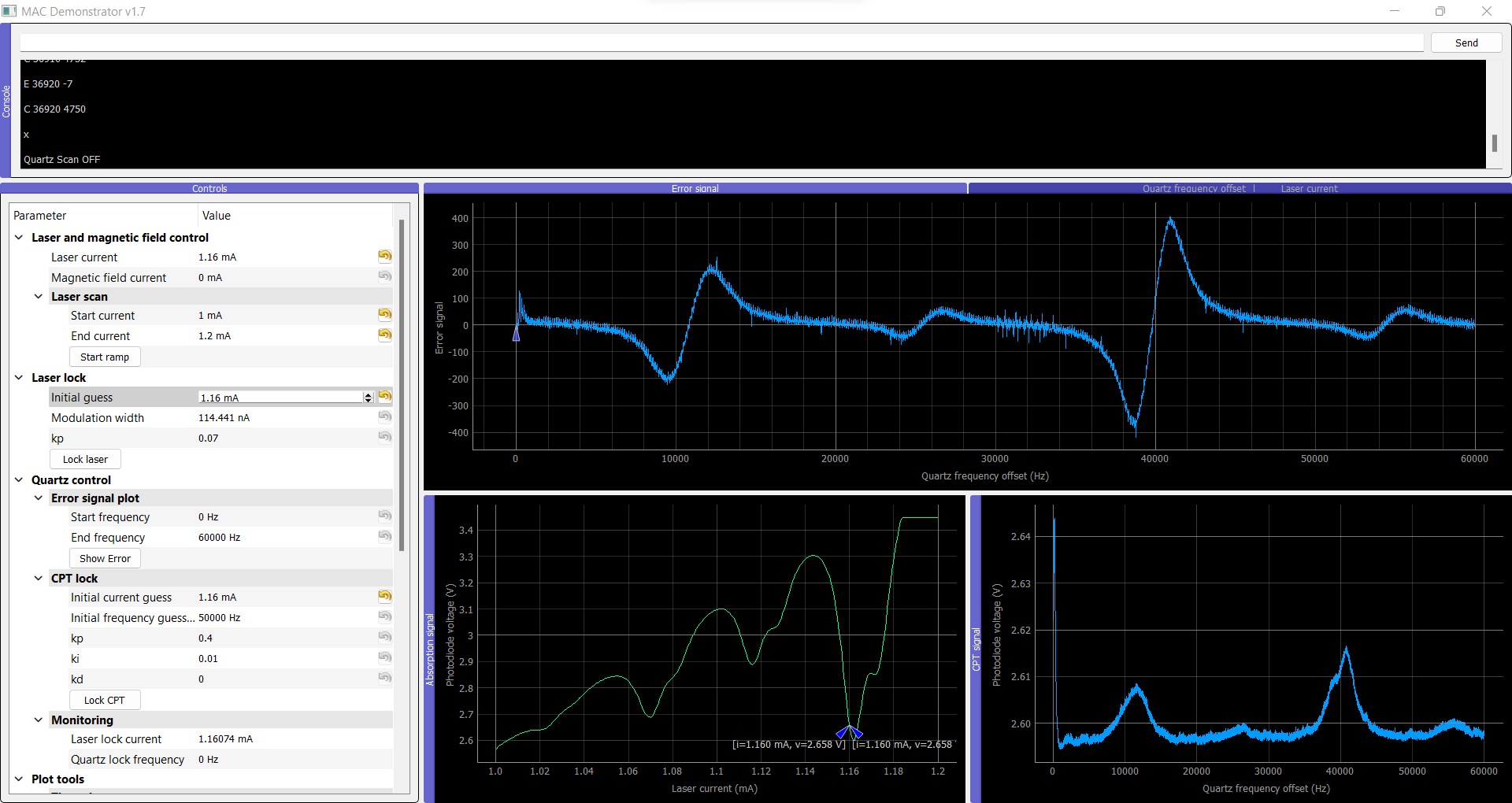
Clock 2 – PP2 – Synth 2 – TC 2 (cloned 1) and no Attenuator:



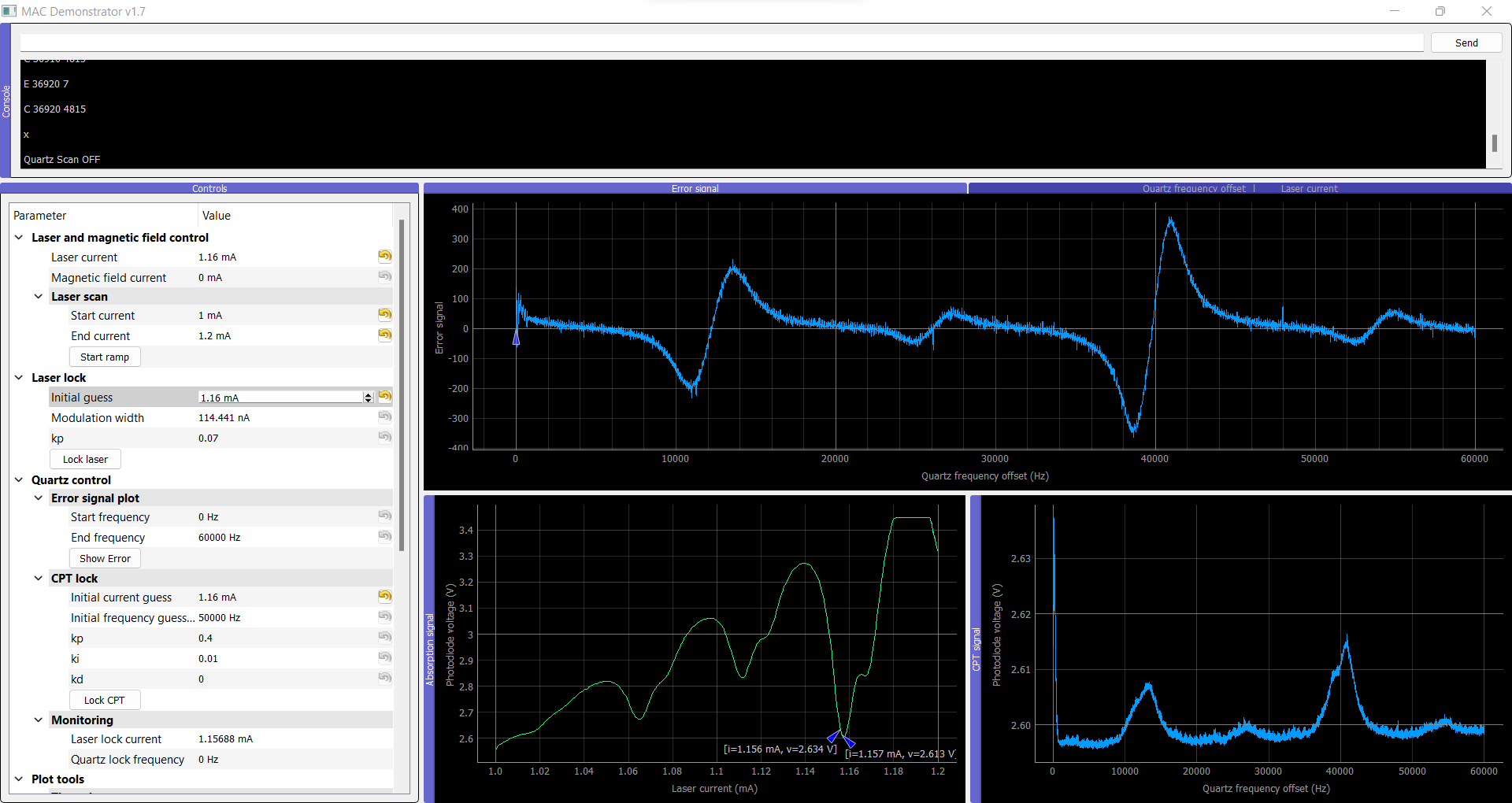
Conclusion: The biggest problem appears to be the attenuator and the synthesizer affects the signal too but only in shape (slope) and not so much in power. Temperature controller doesn’t present a big impact.

# Things to test:

Clock 1 – PP1 – Synth 1 – TC 1 and Attenuator 1:



Clock 1 – PP1 – Synth 1 – TC 1 and Attenuator 2:



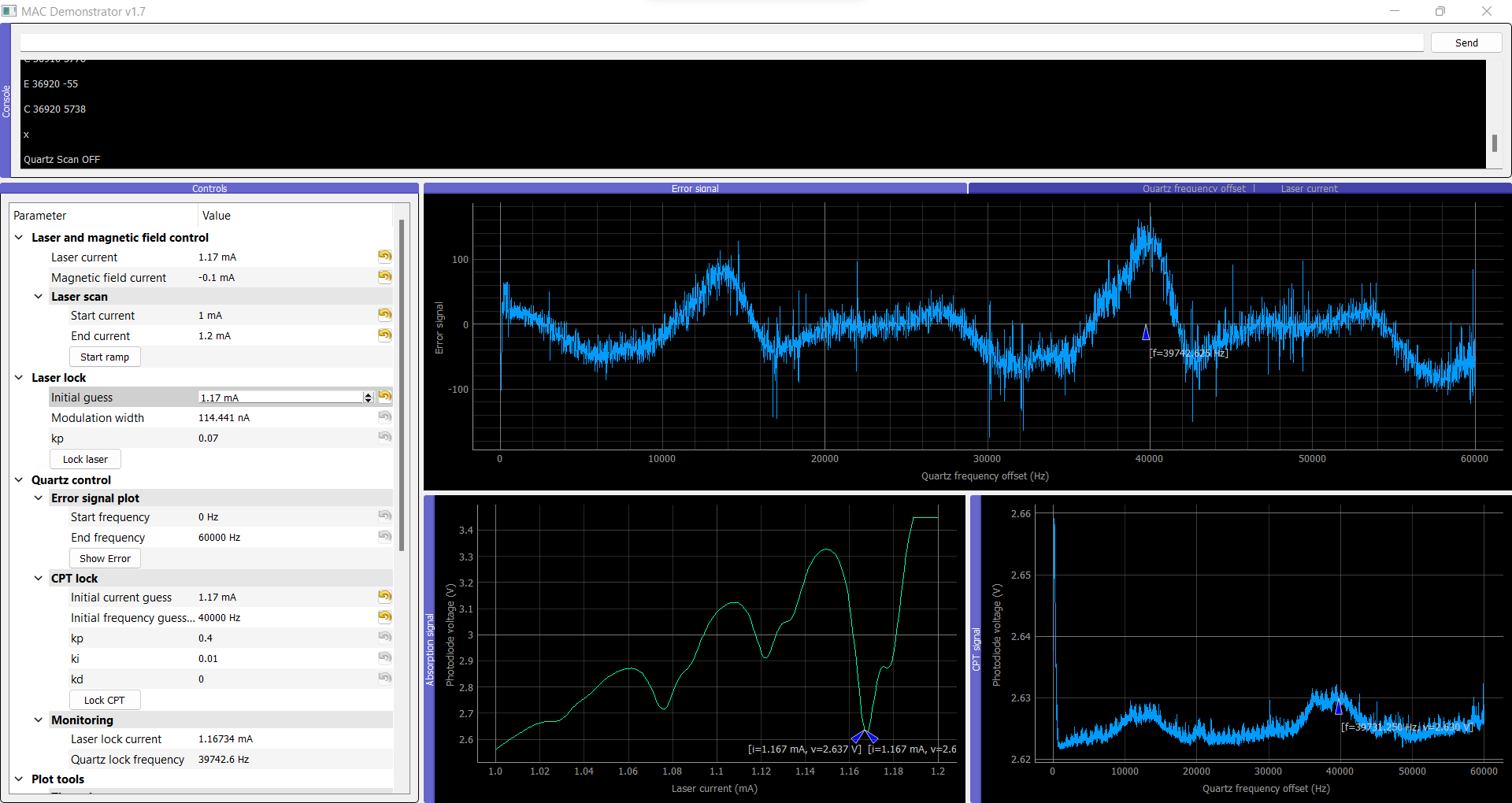
Conclusion: It’s not the attenuator problem.

Clock 1 – PP1 – Synth 1 – TC 1 and **no** Attenuator:

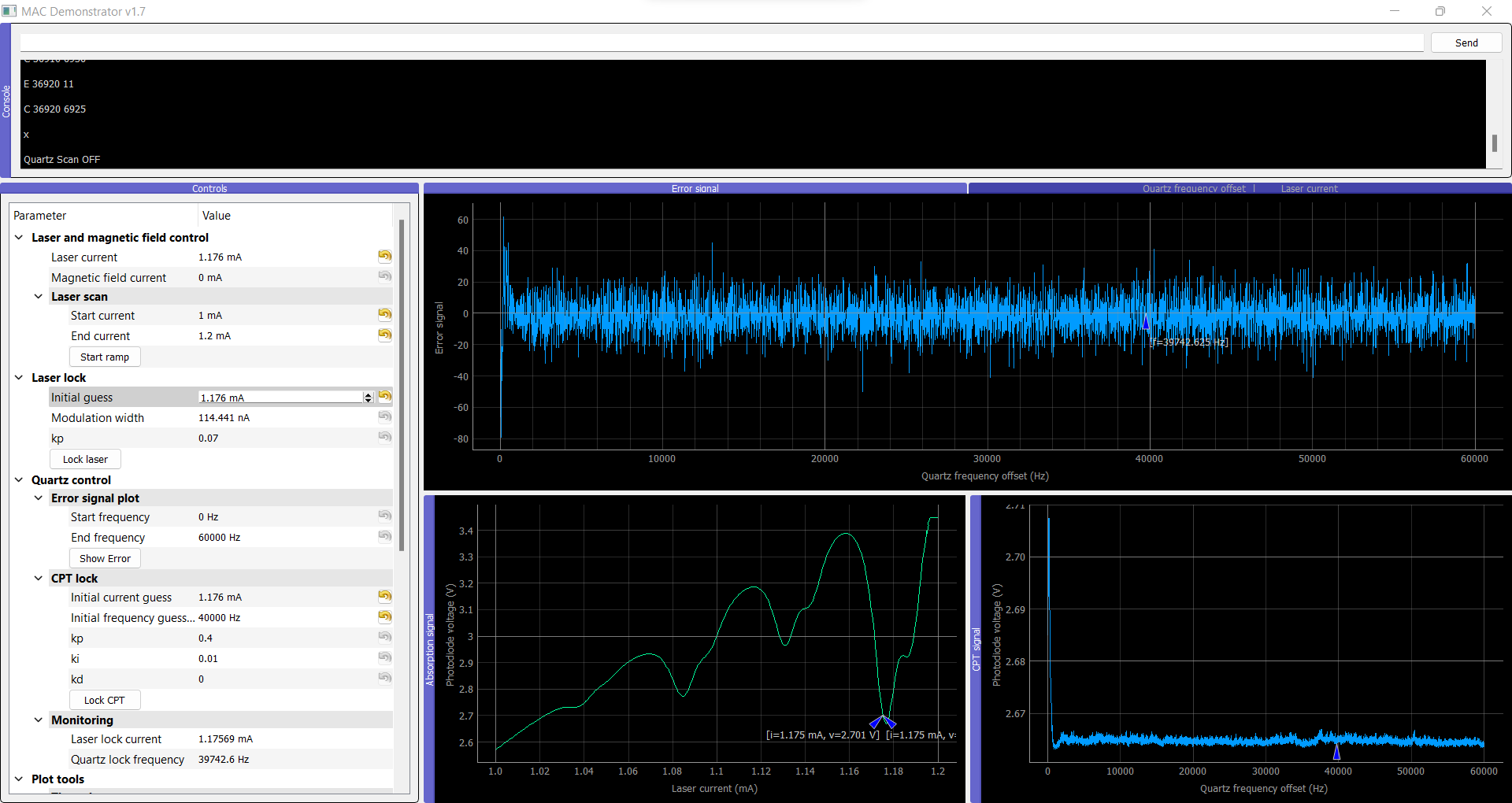


# Modifying synthesizer circuits

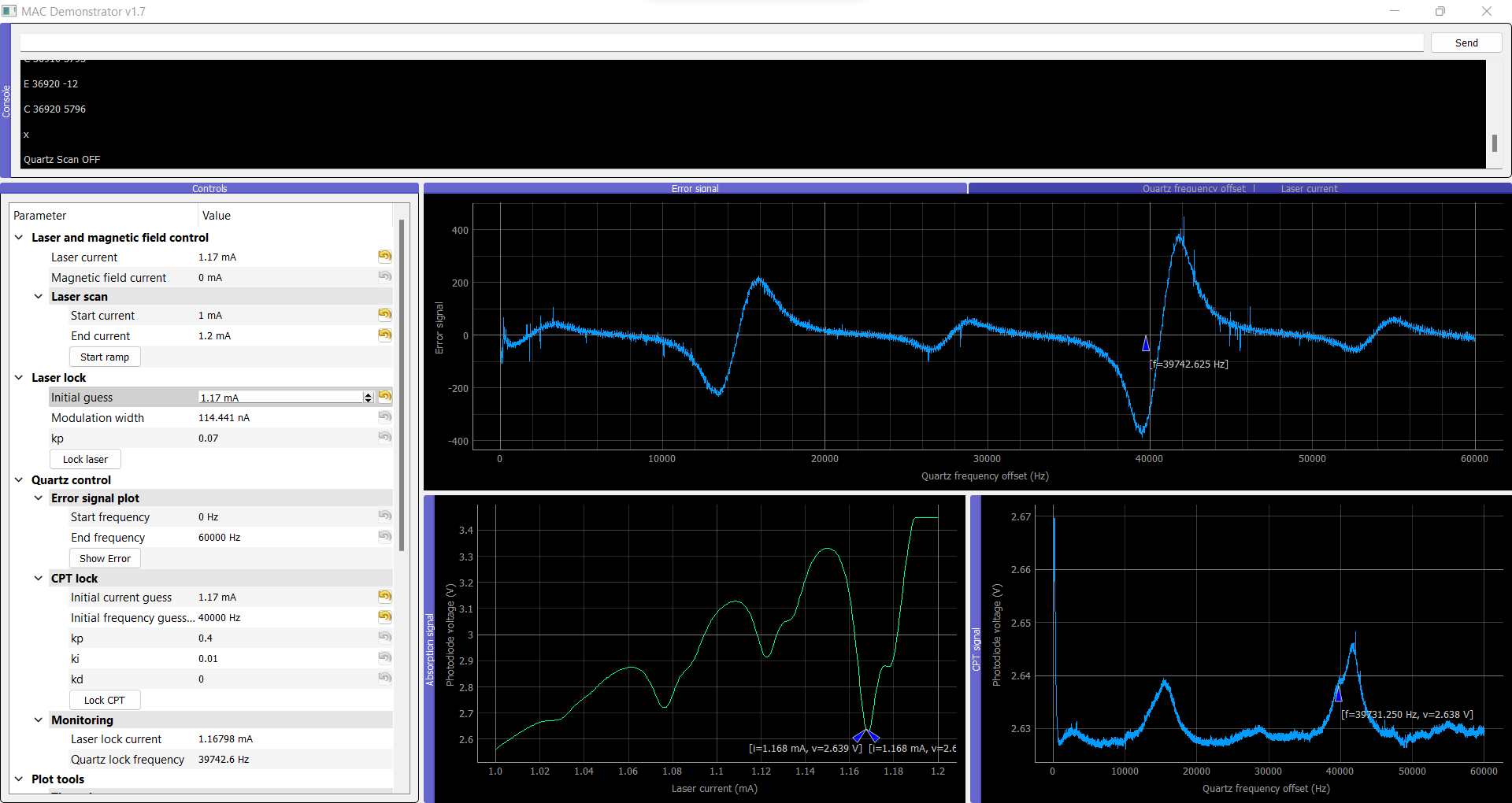
Clock 1 - Synth 2 before:



After (only resistors):

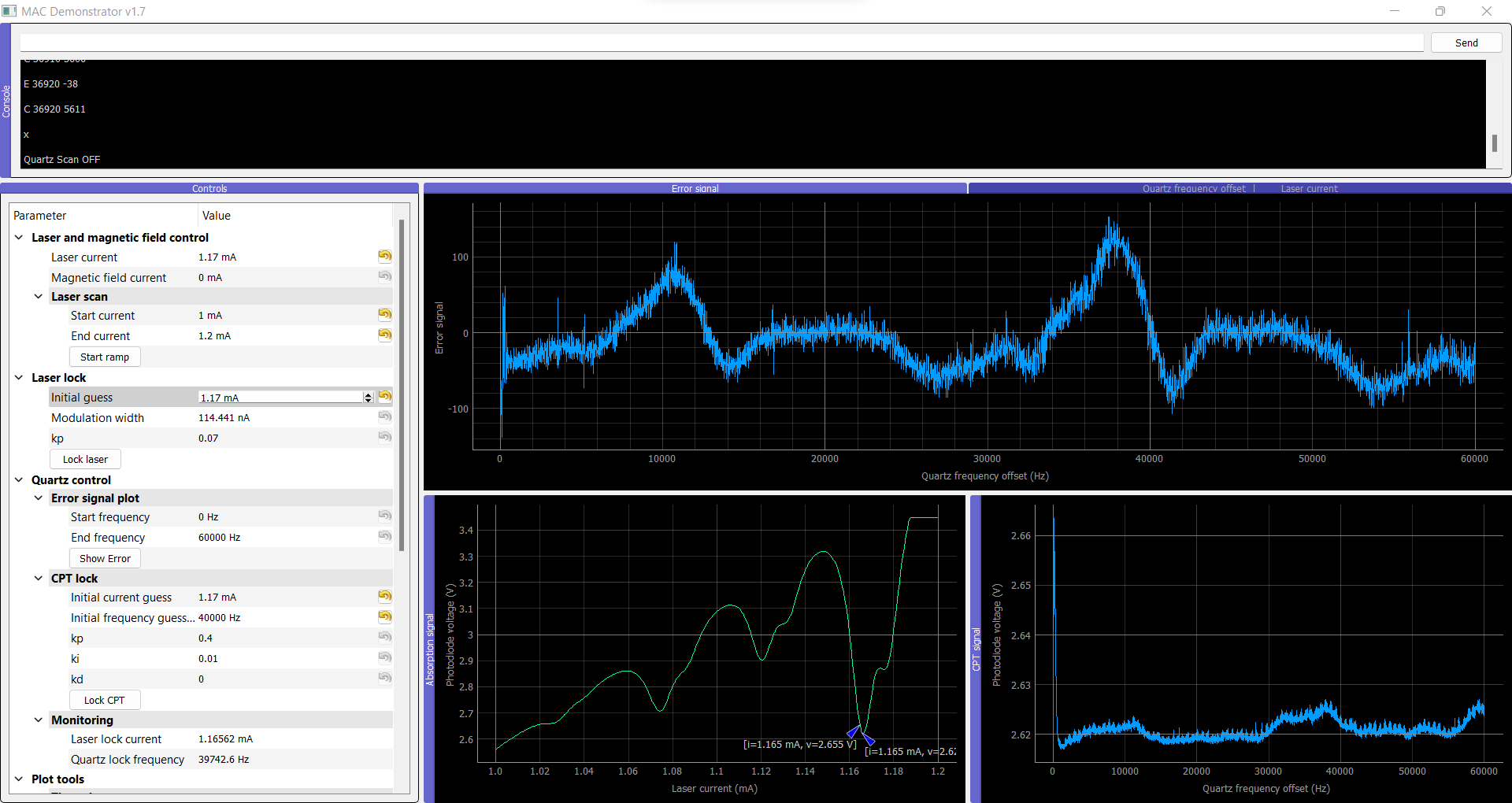


After (Capacitor and resistors):

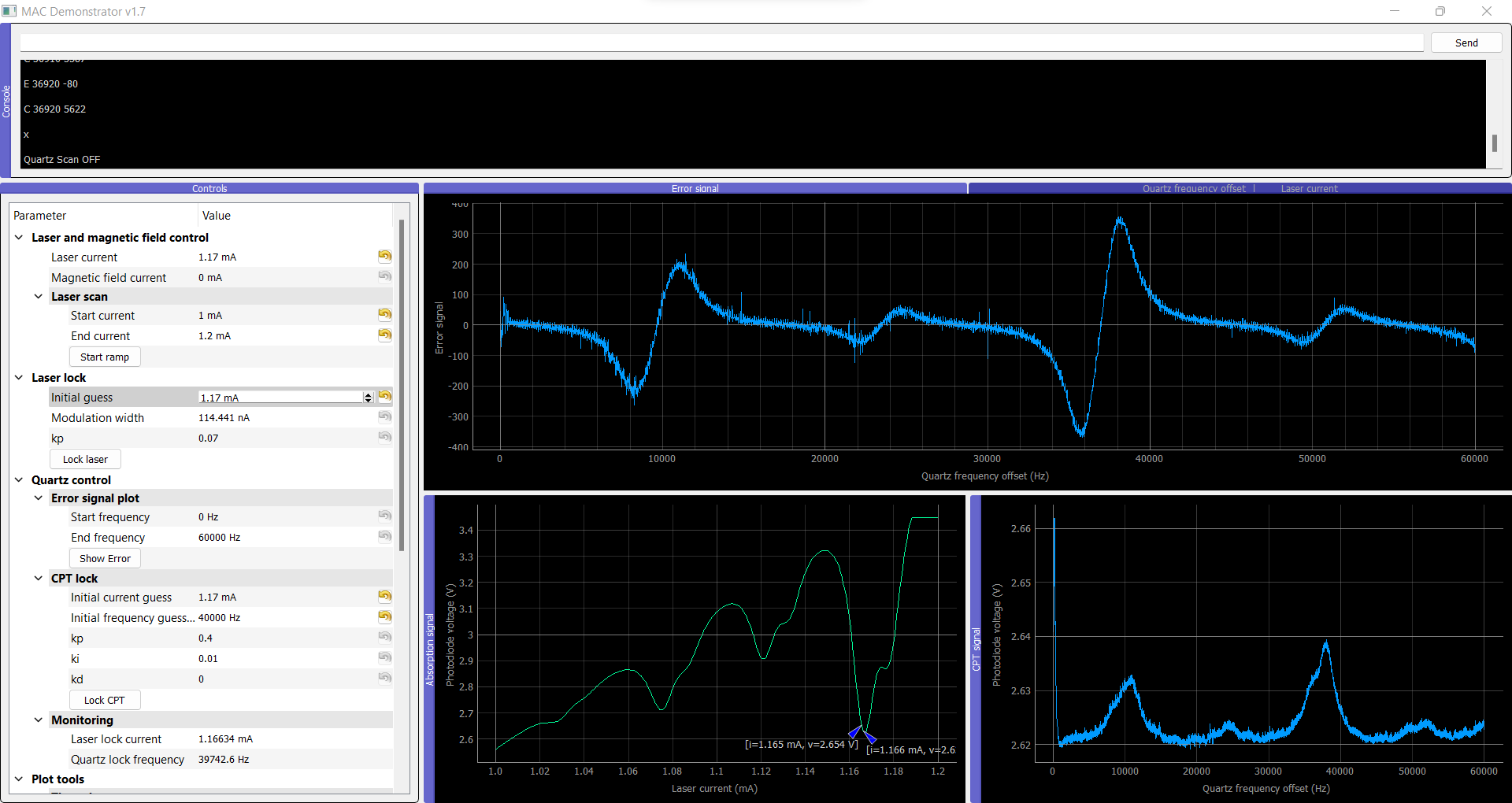


Conclusion: The synthesizer 2 now works as good as the synthesizer 1.

Clock 1 – Synthesizer 3 - before:



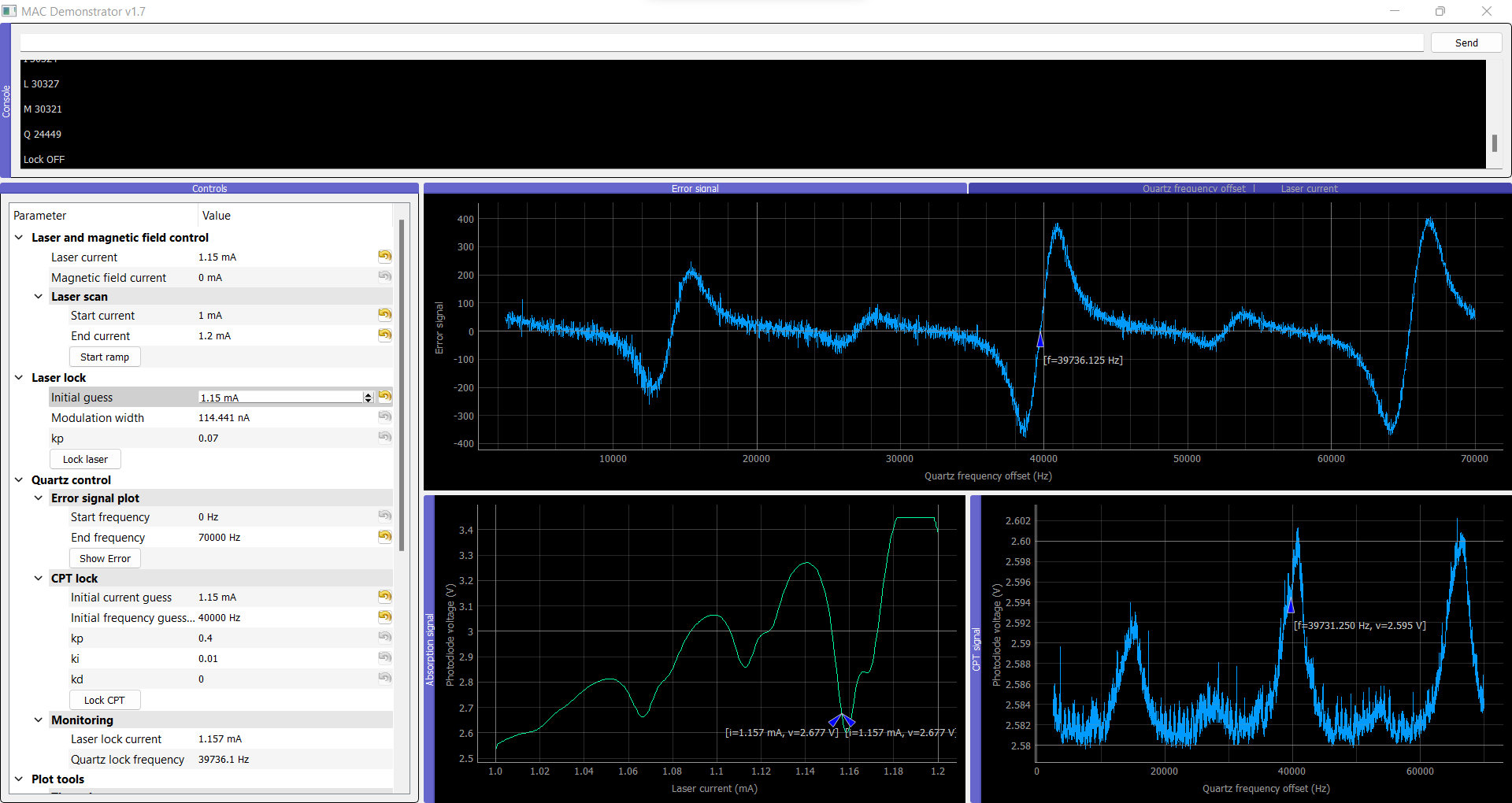
After:



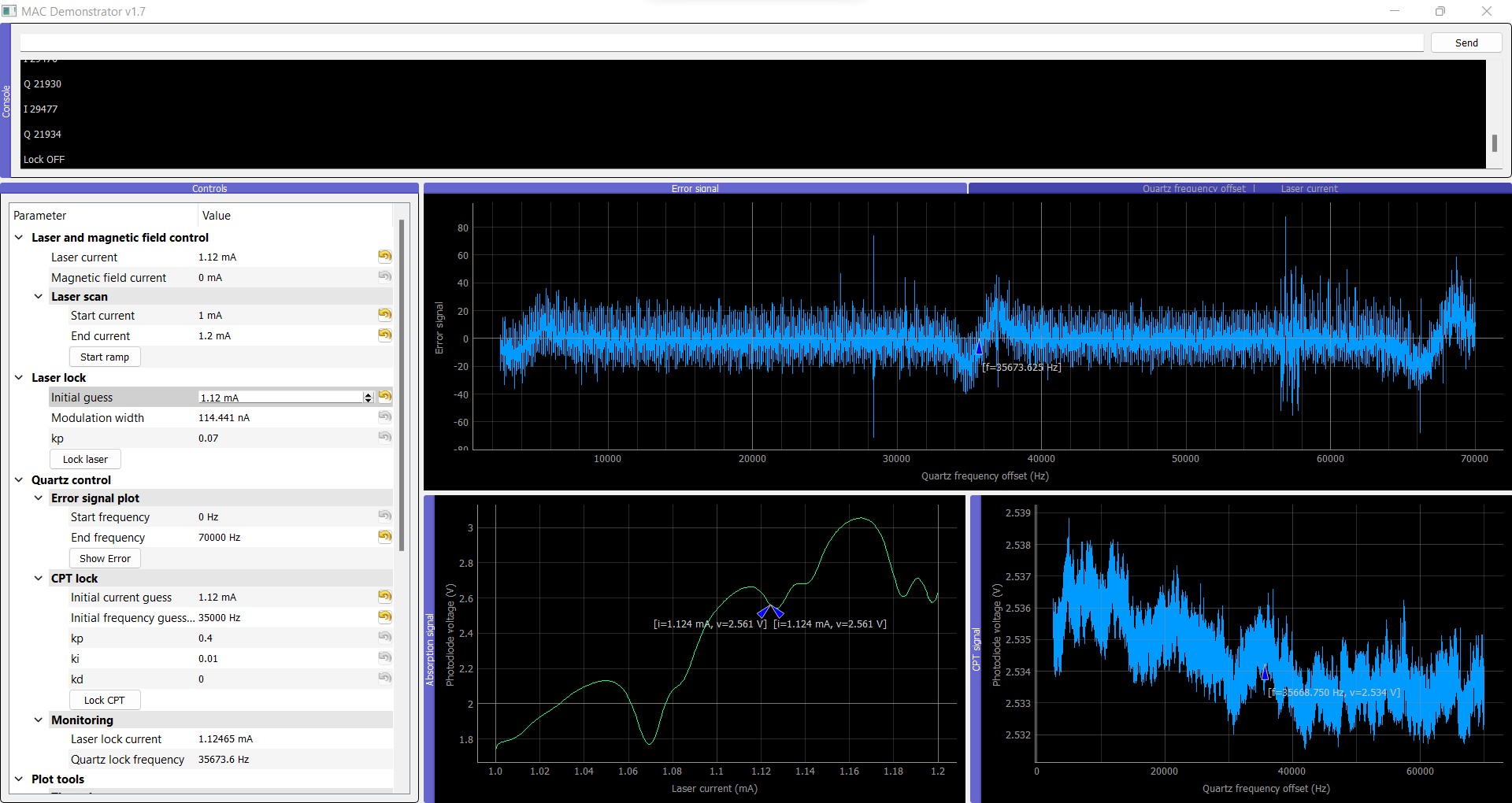
Conclusion: The synthesizer 3 now works as good as the synthesizer 1 and 2.

# Testing synthesizers in their own clocks:

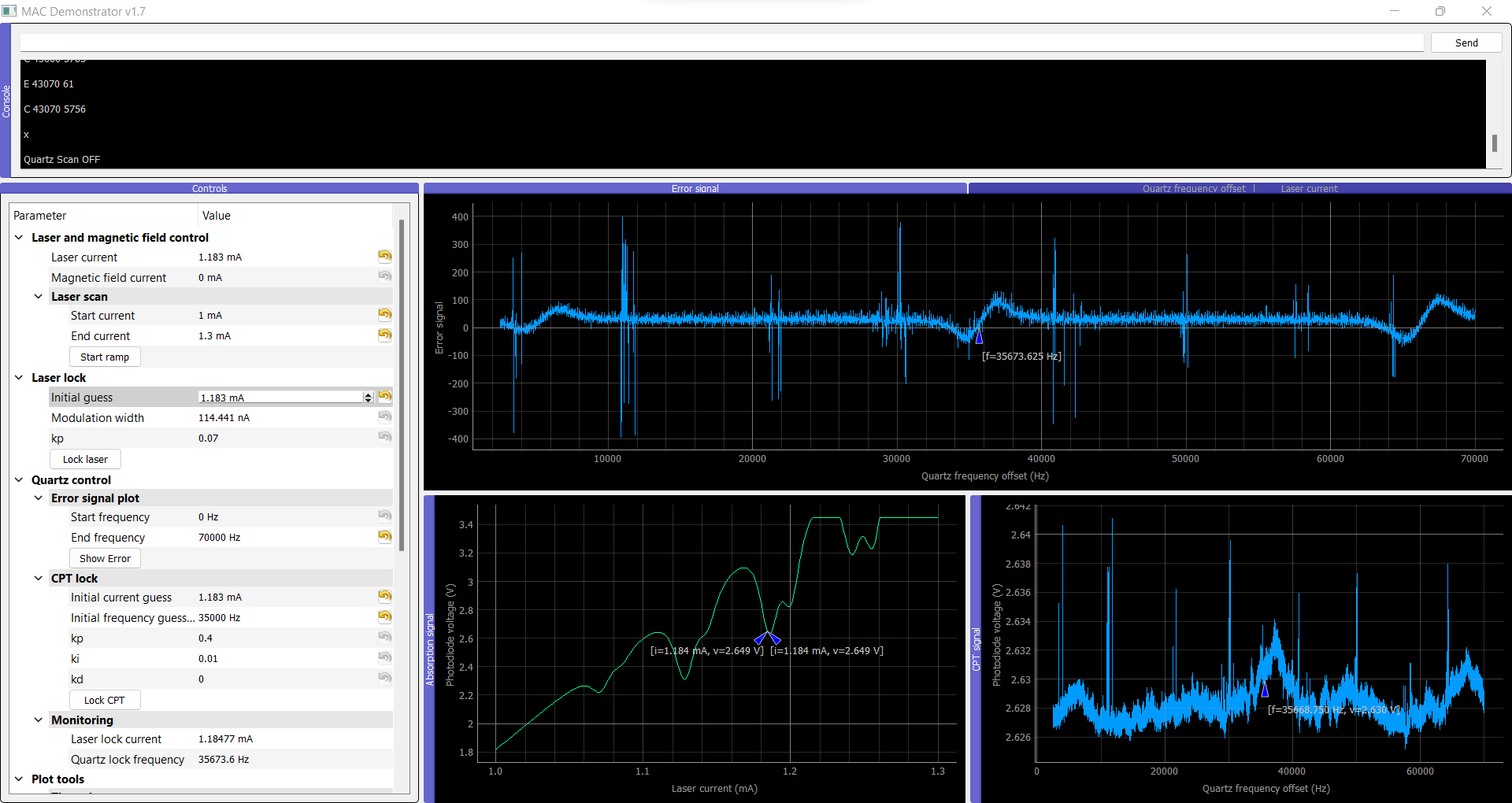
Clock 1:



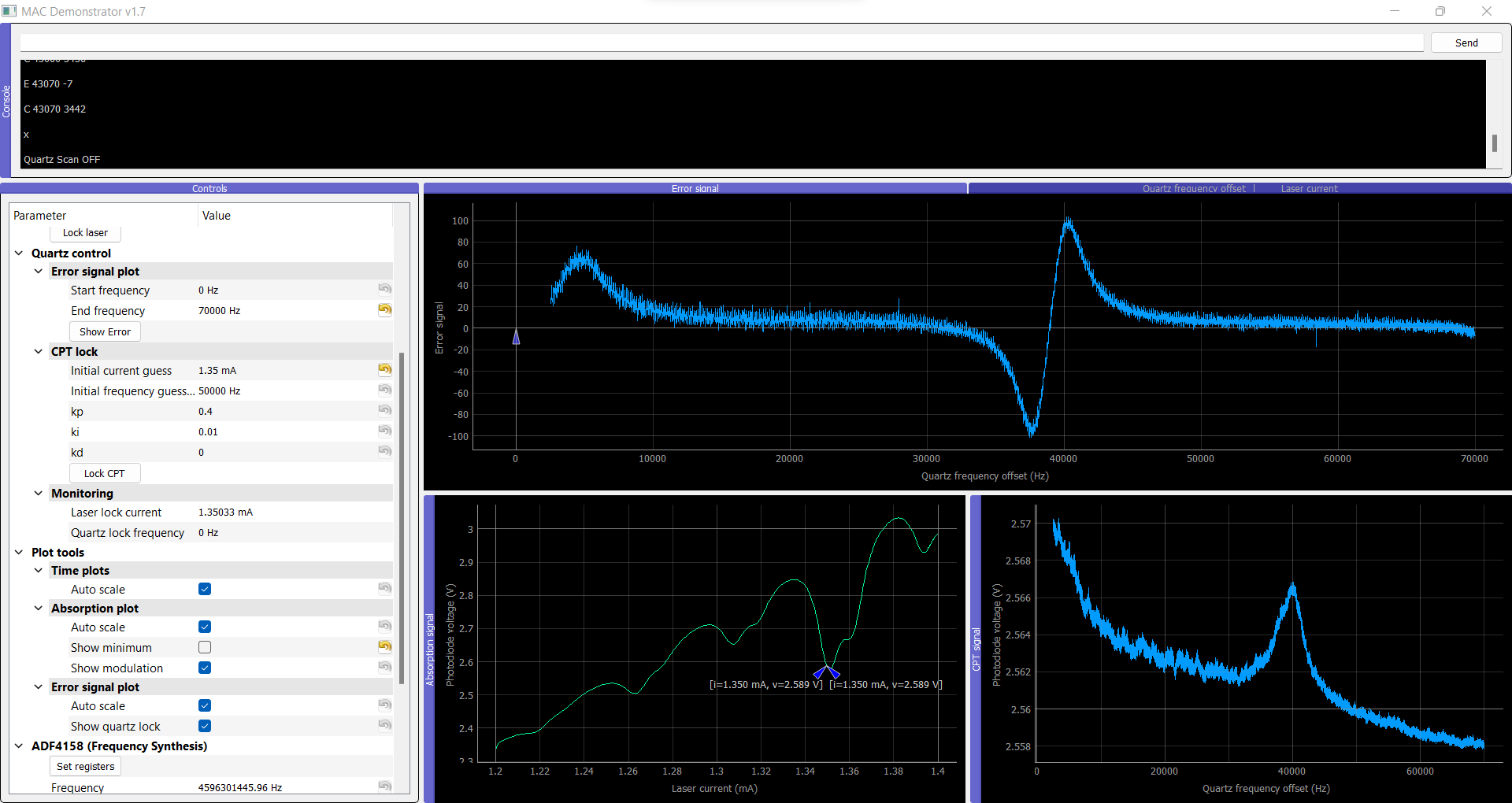
Clock 2:



No att:

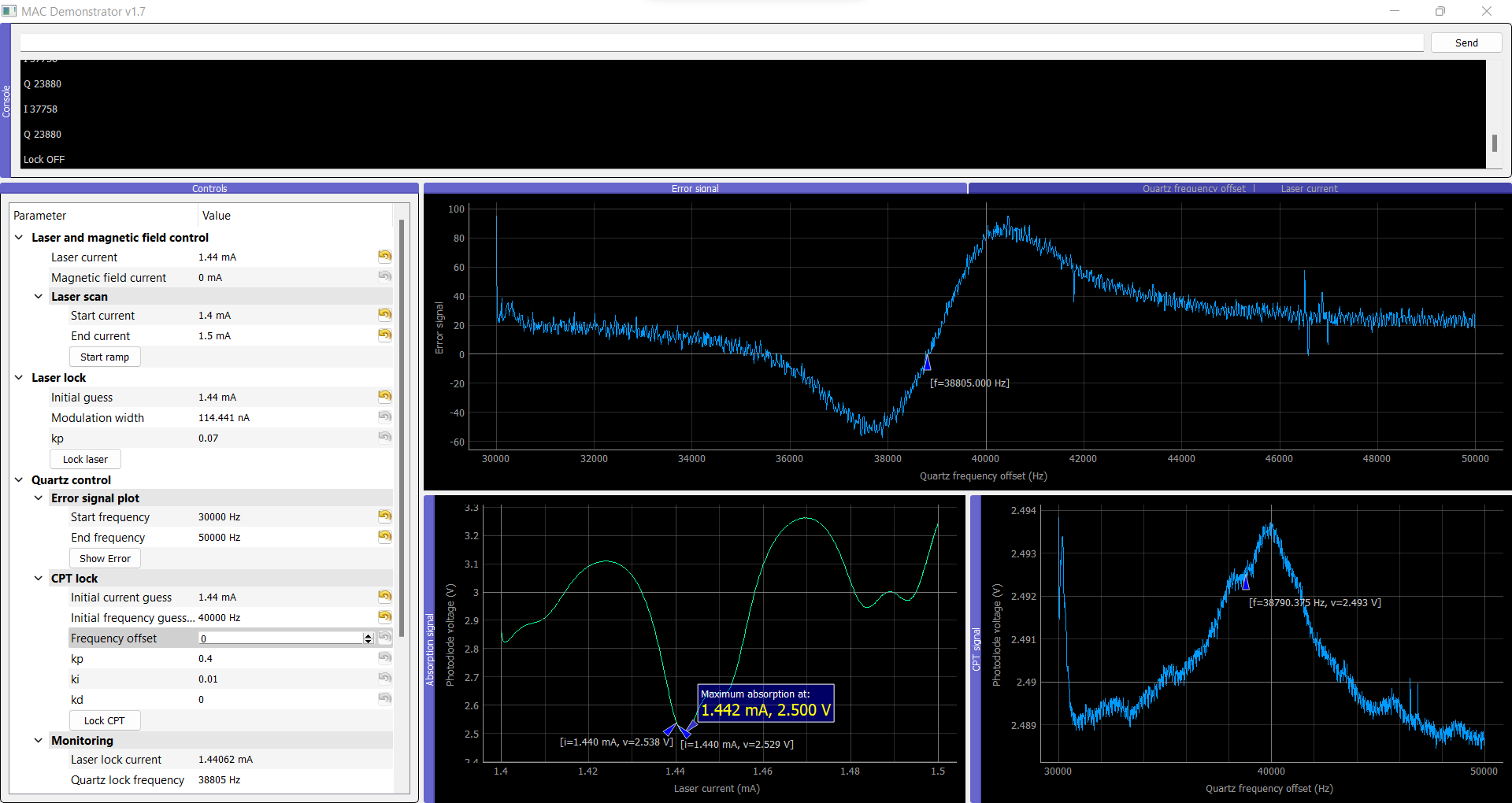


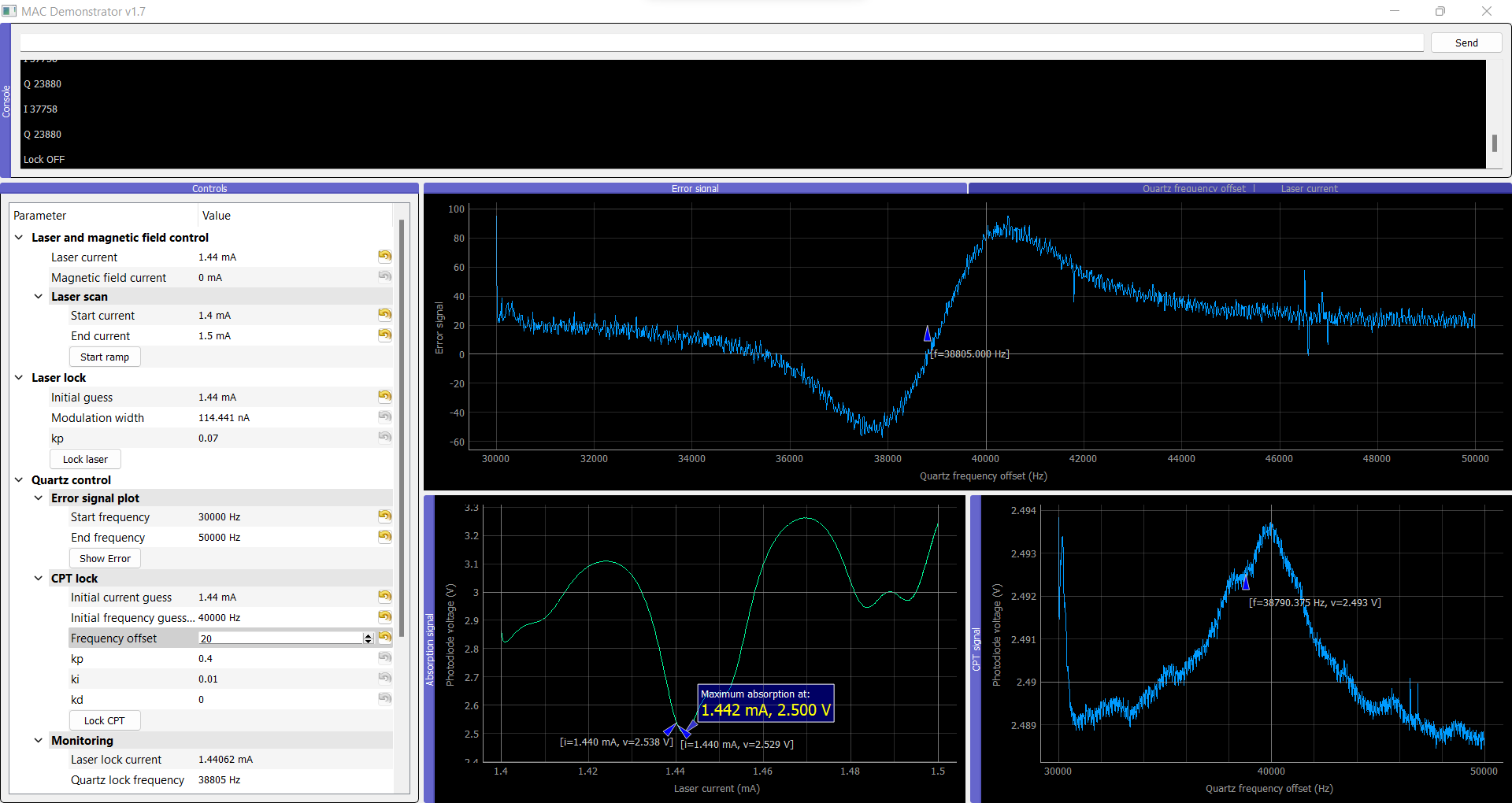
Clock 3:



# Adding Quartz error signal offset

Before:





After:

