GLIB Modules & Functionalities (v2.4.0)

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This document describes how to interact with the GLIB modules.

Contents

OptoHybrid Forward

This module forwards all its requests to the OptoHybrids.

Addressing

Module ID 4

Address 0x4ZXYYYYY

0b 0100 ZZZZ XXXX YYYY YYYY YYYY YYYY YYYY

Description

All the requests made to this module are forwarded to the OptoHybrid n°X of the GLIB. The Z parameter indicates which module on the OptoHybrid will handle the request (see *OptoHybrid Modules & Functionalities* for more information).

Tracking Data Readout

This module stores the tracking data coming from the OptoHybrids into a buffer and allows to readout the data through IPBus.

Addressing

Module ID 5
Address 0x50X0000Y
0b 0101 0000 XXXX 0000 0000 0000 0000 00YY

0	Read /write	*Data packet* A write operation will empty the FIFO
1	Read	*FIFO occupancy* Divide by 7 to compute the number of events
2	Read	*Is the FIFO full?*
3	Read	*Is the FIFO empty?*

Description

To read out data, the software must operate a FIFO read on the register. It then has to form the data packets by regrouping the 32-bits words. Writing to the register will empty the buffer which is recommended after flashing the firmware onto the GLIB or OptoHybrid.

One data packet is composed of 7x 32 bits which are formatted as follows, the highest word being read out first.

MSB - 0	“1010” & BC[11:0] & “1100” & EC[7:0] & Flags[3:0]
1	“1110” & ChipID[11:0] & Strips[127:112]
2	Strips[111:80]
3	Strips[79:48]
4	Strips[47:16]
5	Strips[15:0] & CRC[15:0]
LSB - 6	OptoHybrid BX[31:0]

Counters

This module holds all the counters of the GLIB. Writing to a given register will reset its value.

Addressing

Module ID 6
Address 0x6000000YY
0b 0110 0000 0000 0000 0000 0000 YYYY YYYY

IPBus		
0 - 4	Read	*IPBus strobes* Order: OptoHybrid 0, OptoHybrid 1, Tracking data 0, Tracking data 1, Counters
5 - 9	Read	*IPBus acknowledgments*
T1 commands		
10 - 13	Read	*T1 from AMC13* Order: LV1A, Calpulse, Resync, BC0
GTX		
14 - 15	Read	*Tracking links error*
16 - 17	Read	*Trigger links error*
18 - 19	Read	*Data packets received*

DAQ

This module is responsible for building events from OH packets and sending them to AMC13. It also does some basic checks of the data, monitors status of the FIFOs and manages the TTS state accordingly.

As soon as the data arrives from OH, it's put into Input FIFO. At the same time various checks are done on this data. Once end of event is detected, an entry is made in Event FIFO, which holds event ID, BX ID, event size and some event status flags.

All received L1As are tagged with orbit ID, BX ID and event ID and are stored in L1A FIFO. As soon as this FIFO is not empty, the main DAQ process will start waiting for data in the Event FIFOs for each enabled link. Once Event FIFOs for all links are not empty or DAV timeout is reached, the event construction and sending process begins.

End of event is detected when VFAT BC changes (this will be changed once we add OH event counter or OH Orbit+BX counter to the data stream). VFAT2 EC cannot be used for this because it's reset with BC0 signal.. Event will also be closed if there's no new data and "end of event timeout" occurs (configurable for each link)

When the data checks are performed, some global status flags are latched if an error is found. See register address table for a full list of these flags. Only a few of them are critical and are used to set TTS ERROR state, others can be read through IPBus.

More information on how this module works can be found here:
https://indico.cern.ch/event/453526/session/0/contribution/17/attachments/1169209/1688047/2015-10-13_EJ_GEM_readout_4.pdf

TTS state encoding (according to CMS standard):

0x0 **0xF**	Disconnected	Hardware failure / broken communication
0x1	Overflow Warning	Imminent buffer overflow Asserted when any FIFO is 75% full and lifted when it drains down below 60%
0x2	Out-of-Sync	Data is not synchronized. Currently this state is not used by this module, pending data analysis. In the future it could be used e.g. when L1A ID is different between OH and GLIB
0x4	Busy	Cannot accept triggers Currently this state is only used during reset. It will also be used during resync (not implemented yet)
0x8	Ready	Ready to accept triggers
0xC	Error	Any other condition that prevents this module from accepting triggers and requires a reset.

	Currently this state is set when one of the following critical errors are detected: ● Input or event FIFO overflow ● Input FIFO underflow (sign of incorrect event size in event FIFO) ● Abnormally big event detected (more than 4095 VFAT blocks corresponding to the same event)

There are 3 major groups of registers available: control, global state, OH-specific state.

Addressing

Module ID 7

Address 0x7000000YY

0b 0110 0000 0000 0000 0000 0000 0YYY YYYY

Control register			
0x0	[31:8]	RW	Input enable mask (default = 0x1) This is a bitmask telling GLIB to enable certain inputs (least significant bit is input 0). Only first is enabled by default.
0x0	[7:4]	RW	TTS Override (default = 0) When not 0, it will override the GLIB TTS state with the provided value (e.g. writing 0x8 will force GLIB to always be in TTS READY state)
0x0	[3]	RW	Reset (default = 0) Clears all FIFOs, state flags and counters. It also stops and resets all state machines (no events will be built, recorded or sent during reset) When set to 1, it will be held in reset state until 0 is explicitly written (this can be changed in the future if necessary)
0x0	[2]	RW	DAQLink Reset (default = 0) Directly connected to DAQLink module reset port. BU is advising against ever using it except for powerup, but it may clear some error conditions (like daqlink_almost_ful stuck at 1). AMC13 reset is probably required after this.
0x0	[1]	Not used	
0x0	[0]	RW	DAQ Enable (default = 0) If this is set to 0, there will be no data sent to AMC13 and TTS state will always be READY (0x8)
Global state registers			
0x1	[31:28]	R	TTS State
0x1	[27]	R	Current status: L1A FIFO is empty
0x1	[26]	R	Current status: L1A FIFO is near full (75%)
0x1	[25]	R	Current status: L1A FIFO is full

0x1	[24]	R	Current status: L1A FIFO is in underflow
0x1	[23]	R	Critical: L1A FIFO overflow occurred This bit is latched whenever L1A FIFO overflow is asserted. This means that one or more L1As were lost, so we are out-of-sync -- resync / reset is needed
0x1	[22:4]	Not used	
0x1	[3]	R	DAQLink FIFO almost full This bit comes directly from DAQLink module, indicating that its' internal buffers are full. No events will be sent when this bit is 1 (though events can still be built and stored in the Input and Event FIFOs)
0x1	[2]	R	TTC ready
0x1	[1]	R	DAQ clock locked
0x1	[0]	R	DAQLink Ready When this is 1, it means that GLIB is in good communication with AMC13. It must be 1 for GLIB to be able to send data.
0x2	[15:0]	R	8b/10b Not-in-Table error count on the AMC13 link
0x3	[15:0]	R	8b/10b Dispersion error count on the AMC13 link
0x4	[23:0]	R	L1A ID
0x5	[31:0]	R	Number of events sent to AMC13
0x6	[23:0]	RW	DAV timeout This setting controls how long DAQ will wait for individual inputs to report data before calling it timed-out (if timeout occurs a header and trailer for that chamber will still be inserted and timeout flag will be set there, though no VFAT payload will be present). Units = clock cycles @ 25MHz (current DAQLink clk frequency)
0x7	[23:0]	R	Max DAV timer This indicates the maximum amount of time that DAQ had to wait for all inputs to report data (can be used to optimize DAV timeout setting). Units = clock cycles @ 25MHz (current DAQLink clk frequency)
0x8	[23:0]	R	Last DAV timer This indicates how DAQ had to wait for all inputs to report data for the last event (mostly for debugging). Units = clock cycles @ 25MHz (current DAQLink clk frequency)
Temporary sbit debug registers			
0x9	[30:16]	R	Last sbit cluster 0 data (link 0) Top 3 bits indicate cluster size, the lower 11 bits indicate cluster address
0x9	[14:0]	R	Last sbit cluster 1 data (link 0) Top 3 bits indicate cluster size, the lower 11 bits indicate cluster address
0x10	[30:16]	R	Last sbit cluster 2 data (link 0) Top 3 bits indicate cluster size, the lower 11 bits indicate cluster address
0x10	[14:0]	R	Last sbit cluster 3 data (link 0)

			Top 3 bits indicate cluster size, the lower 11 bits indicate cluster address
0x11	[30:16]	R	Last sbit cluster 0 data (link 1) Top 3 bits indicate cluster size, the lower 11 bits indicate cluster address
0x11	[14:0]	R	Last sbit cluster 1 data (link 1) Top 3 bits indicate cluster size, the lower 11 bits indicate cluster address
0x12	[30:16]	R	Last sbit cluster 2 data (link 1) Top 3 bits indicate cluster size, the lower 11 bits indicate cluster address
0x12	[14:0]	R	Last sbit cluster 3 data (link 1) Top 3 bits indicate cluster size, the lower 11 bits indicate cluster address
0x13	[31:0]	R	Valid sbit cluster rate in Hz This is counting any valid sbit clusters on both links. Make sure you have both links connected, otherwise this will be maxed out since invalid sbit cluster must have top 2 address bits set to 1 (which is not the case when link is disconnected)
Run type and run parameters (inserted into the data stream, but don't affect DAQ otherwise)			
0xF	[27:24]	RW	Run type
0xF	[24:16]	RW	Run parameter 1
0xF	[15:8]	RW	Run parameter 2
0xF	[7:0]	RW	Run parameter 3
OH-specific state registers (addresses below are for the first OH, subsequent OHs are offset by 0x10)			
0x10	[31]	R	Current status: Event FIFO is empty
0x10	[30]	R	Current status: Event FIFO is near-full (75%)
0x10	[29]	R	Current status: Event FIFO is full
0x10	[28]	R	Current status: Event FIFO is in underflow
0x10	[27]	R	Current status: Input FIFO is empty
0x10	[26]	R	Current status: Input FIFO is near-full (75%)
0x10	[25]	R	Current status: Input FIFO is full
0x10	[24]	R	Current status: Input FIFO is in underflow
0x0	[23:16]	Not used	
0x0	[15:12]	R	Input TTS state
0x10	[11]	R	Critical: Event size overflow occurred This bit is latched if there was an event containing more than 4096 VFAT blocks. Input FIFO and Event FIFO will be out-of-sync. This might happen if end-of-event is not detected properly or for whatever reason GLIB is receiving a stream of VFAT blocks indicating that they belong to the same event (EC/BC is the same) TTS ERROR is asserted when this bit is 1
0x10	[10]	R	Critical: Event FIFO overflow occurred

			This bit is latched if Event FIFO was ever full when trying to build a new event. This means data was lost. It's not likely that this will ever be asserted because Input FIFO should overflow first. TTS ERROR is asserted when this bit is 1
0x10	[9]	R	Critical: Input FIFO underflow occurred This bit is latched if Input FIFO underflow was ever detected. This means that Event FIFO indicated that there should be more data than was stored in Input FIFO. This might happen due to overflow or some other malfunction. TTS ERROR is asserted when this bit is 1
0x10	[8]	R	Critical: Input FIFO overflow occurred This bit is latched if Input FIFO was ever full when receiving new data – this means data was lost. TTS ERROR is asserted when this bit is 1
0x10	[7]	R	Corruption: VFAT marker not detected There was at least one VFAT block not conforming to the pattern of Axxx Cxxx Exxx..... (see VFAT data format) Note that this data will still be included in the current event and sent to AMC13, but it will not be considered in end-of-event detection.
0x10	[6]	R	Corruption: VFAT block bigger than 192bits
0x10	[5]	R	Corruption: VFAT block smaller than 192bits
0x10	[4]	R	Corruption: more than 24 VFATs in event
0x10	[3]	R	OH mixed BC There was at least one event with mixed OH BX IDs (OH BX ID is reported for every VFAT block, but not sent to AMC13).
0x10	[2]	R	VFAT mixed BC There was at least one event with mixed VFAT BX IDs
0x10	[1]	R	VFAT mixed EC There was at least one event with mixed VFAT Event IDs
0x10	[0]	Not used	
0x11	[31:0]	R	Corrupted VFAT block counter This counter is incremented when a VFAT block does not conform to the pattern of Axxx Cxxx Exxx..... (see VFAT data format) Note that this data is still included in events and sent to AMC13, but it does not participate in end-of-event detection.
0x12	[23:0]	R	Current event number of the event builder This counter starts at 1 and increments with each end-of-event detection. This number should be similar to the number of events sent to AMC13 in normal operation, but it might not always be exactly the same because there's some latency between building an event and sending it. In addition, event sending could stop due to DAQ FIFO being almost full or DAQLink not being ready.

0x13	[31:16]	RW	End of event timeout (units = clock cycles @ 160MHz) If no new data was received in this amount of time, GLIB will close the current event and report it to DAQ. This is one of the two ways to close an event, the other is to get new data with different BX number.
0x17	[23:0]	R	Max end of event timer (units = clock cycles @ 160MHz) This indicates the maximum amount of time that event builder took to build and close the event. Note: this is mostly for debugging, most of the time it should be equal to "End of event timeout"
0x18	[23:0]	R	Last end of event timer (units = clock cycles @ 160MHz) This shows how long event builder took to build and close the last event. Note: this is mostly for debugging, but could be used to tune the "end of event timeout"
0x19	[31:0]	R	Debug: bits [31:0] of last received VFAT block + OH word
0x1A	[31:0]	R	Debug: bits [63:32] of last received VFAT block + OH word
0x1B	[31:0]	R	Debug: bits [95:64] of last received VFAT block + OH word
0x1C	[31:0]	R	Debug: bits [127:96] of last received VFAT block + OH word
0x1D	[31:0]	R	Debug: bits [159:128] of last received VFAT block + OH word
0x1E	[31:0]	R	Debug: bits [191:160] of last received VFAT block + OH word
0x1F	[31:0]	R	Debug: bits [223:192] of last received VFAT block + OH word

Data format

The data format consists of these main blocks (64bit words):

1. AMC header #1
2. AMC header #2
3. GEM event header
4. GEM chamber header
5. VFAT data (size of this section can vary, if not zero-suppressed then 192bits per VFAT block)
6. GEM chamber trailer
7. GEM event trailer
8. AMC trailer

This table lists the details of each section for format version 0:

AMC header #1		
[63:60]	Reserved	
[59:56]	AMC number	Slot number of the AMC (GLIB / MP7 / EC7, etc)

[55:32]	L1A ID	L1A number – basically this is like event number, but it's reset by resync
[31:20]	BX ID	Bunch crossing ID
[19:0]	Data length	Overall size of this FED event fragment in 64bit words (including all the headers and trailers)
AMC header #2		
[63:60]	Format version	Current format version = 0x0
[59:56]	Run type	Could be used to encode run types like physics, cosmics, threshold scan, latency scan, etc..
[55:48]	Run param1	
[47:40]	Run param2	
[39:32]	Run param3	
[31:16]	Orbit number	
[15:0]	Board ID	This is currently filled with 8bit long GLIB serial number (hard-coded by resistors [R38:R31])
GEM event header		
[63:40]	GEM DAV list	Bitmask indicating which inputs/chambers have data
[39:16]	Buffer status	Bitmask indicating buffer error in given inputs. The bits are asserted in case of critical buffer error: input buffer overflow, event buffer overflow, input buffer underflow, event size overflow. This error means that data in this event is most likely corrupted of out of sync (belongs to different L1A ID)
[15:11]	GEM DAV count	Number of chamber blocks
[10:4]	Not used	
[3:0]	TTS state	Debug: GLIB TTS state at the moment when this event was built. Note that there is some undefined latency between the time when this TTS state was asserted (and sent to AMC13) and when this event was built. Therefore this value is here just for debugging and likely to be scratched away from the data format.
GEM chamber header		
[63:40]	Zero suppression flags	Bitmask indicating if certain VFAT blocks have been zero suppressed
	Zero suppression flags	Bitmask indicating if certain VFAT blocks have been zero suppressed
[39:35]	Input ID	GLIB input ID (starting at 0)
[34:23]	VFAT word cnt	Size of VFAT payload in 64bit words (when not zero suppressed, one VFAT block = 192 bits = 3 words)
[22]	EvtFIFO full	Input status (critical): Event FIFO full
[21]	InFIFO full	Input status (critical): Input FIFO full
[20]	L1AFIFO full	Input status (critical): L1A FIFO full
[19]	Event size overflow	Input status (critical): Event size overflow

[18]	EvtFIFO near full	Input status (warning): Event FIFO near full (75%)
[17]	InFIFO near full	Input status (warning): Input FIFO near full (75%)
[16]	L1AFIFO near full	Input status (warning): L1A FIFO near full (75%)
[15]	Event size warn	Input status (warning): More than 24 VFATs in this chamber block
[14]	No VFAT marker	Input status (warning): No VFAT marker in one of the VFAT blocks
[13]	OOS GLIB VFAT	Input status (out-of-sync): GLIB event counter is out of sync with one or more VFAT event counters (this will be set most of the time for VFAT2 because EC resets with BC0)
[12]	OOS GLIB OH	Input status (out-of-sync): GLIB event counter is out of sync with OH event counter (currently not available, so always 0)
[11]	BX mismatch GLIB VFAT	Input status (out-of-sync): GLIB BX ID is different from one or more VFAT BX IDs
[10]	BX mismatch GLIB OH	Input status (out-of-sync): GLIB BX ID is different from one or more OH BX IDs
[9:0]	Not used	
GEM payload		
variable	VFAT data	VFAT data. Length of this section is indicated by "VFAT word cnt" field in the GEM Chamber Header and Trailer (in 64bit words). For non-zero-suppressed data there will be 192bit blocks for each VFAT (see VFAT data format). This block will always be of size indicated by "VFAT word cnt". Even if we run out of data in InFIFO for whatever reason, it will be filled with 0s to reach the desired size.
GEM chamber trailer		
[63:48]	OH CRC	CRC of OH data (currently not available – filled with 0)
[47:36]	VFAT word cnt	Same as in the header -- size of VFAT payload in 64bit words. This one actually counts the number of valid words that we just sent to AMC13 and the one in the header is what we expected to send to AMC13 (as indicated by event size in EvtFIFO). In some rare cases they might be different (e.g. after InFIFO overflow), which would indicate a severe problem. If it does happen that we run out of data in InFIFO while sending this event, the expected VFAT blocks will be substituted with the right amount of 0s, so that unpacker can find this trailer based on the "VFAT word cnt" field in the header.
[35]	InFIFO underflow	Input status (critical): Input FIFO underflow occurred while sending this event

[34]	Stuck data	Input status (warning): There was data in InFIFO or EvtFIFO when L1A FIFO was empty. This bit doesn't necessarily relate to this particular event, but indicates that stuck data was detected on this input at some point. It is latched and only resets with resync or reset.
[33:0]	Not used	
GEM event trailer		
[63:40]	Chamber timeout	This is a bitmask indicating if GLIB did not receive data from a particular input for this L1A in X amount of GTX clock cycles. X is user defined.
[39]	OOS GLIB	GLIB is out-of-sync (critical): L1A ID is different for different chambers in this event.
[38:0]	Not used	

System Control

This module exposes registers that affect the general GLIB operation

Addressing

Module ID 8
Address 0x7E00000Y
0b 0111 1110 0000 0000 0000 0000 0000 YYYY

GTX Polarity Control			
0x0	[3:0]	RW	RX Polarity This controls the GTX RX polarity of the four links (bit 0 corresponds to link 0, which connects to the top SFP)
0x0	[3:0]	RW	TX Polarity This controls the GTX TX polarity of the four links (bit 0 corresponds to link 0, which connects to the top SFP)