GLIB Modules & Functionalities

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This document describes how to interact with the GLIB modules.

# Contents

[Contents 1](#_Toc436666888)

[OptoHybrid Forward 2](#_Toc436666889)

[Addressing 2](#_Toc436666890)

[Description 2](#_Toc436666891)

[Tracking Data Readout 3](#_Toc436666892)

[Addressing 3](#_Toc436666893)

[Description 3](#_Toc436666894)

[Counters 4](#_Toc436666895)

[Addressing 4](#_Toc436666896)

[DAQ 5](#_Toc436666897)

[Addressing 6](#_Toc436666898)

# OptoHybrid Forward

This module forwards all its requests to the OptoHybrids.

## Addressing

Module ID 4

Address 0x4ZXYYYYY

0b 0100 ZZZZ XXXX YYYY YYYY YYYY YYYY YYYY

## Description

All the requests made to this module are forwarded to the OptoHybrid n°X of the GLIB. The Z parameter indicates which module on the OptoHybrid will handle the request (see *OptoHybrid Modules & Functionalities* for more information).

# Tracking Data Readout

This module stores the tracking data coming from the OptoHybrids into a buffer and allows to readout the data through IPBus.

## Addressing

Module ID 5

Address 0x50X0000Y

0b 0101 0000 XXXX 0000 0000 0000 0000 00YY

|  |  |  |
| --- | --- | --- |
| X register | Mode | Function |
| 0 | Read /write | *Data packet*  A write operation will empty the FIFO |
| 1 | Read | *FIFO occupancy*  Divide by 7 to compute the number of events |
| 2 | Read | *Is the FIFO full?* |
| 3 | Read | *Is the FIFO empty?* |

## Description

To read out data, the software must operate a FIFO read on the register. It then has to form the data packets by regrouping the 32-bits words. Writing to the register will empty the buffer which is recommended after flashing the firmware onto the GLIB or OptoHybrid.

One data packet is composed of 7x 32 bits which are formatted as follows, the highest word being read out first.

|  |  |
| --- | --- |
| MSB - 0 | “1010” & BC[11:0] & “1100” & EC[7:0] & Flags[3:0] |
| 1 | “1110” & ChipID[11:0] & Strips[127:112] |
| 2 | Strips[111:80] |
| 3 | Strips[79:48] |
| 4 | Strips[47:16] |
| 5 | Strips[15:0] & CRC[15:0] |
| LSB - 6 | OptoHybrid BX[31:0] |

# Counters

This module holds all the counters of the GLIB. Writing to a given register will reset its value.

## Addressing

Module ID 6

Address 0x6000000YY

0b 0110 0000 0000 0000 0000 0000 YYYY YYYY

|  |  |  |
| --- | --- | --- |
| Y register | Mode | Function |
| IPBus | | |
| 0 - 4 | Read | *IPBus strobes*  Order: OptoHybrid 0, OptoHybrid 1, Tracking data 0, Tracking data 1, Counters |
| 5 - 9 | Read | *IPBus acknowledgments* |
| T1 commands | | |
| 10 - 13 | Read | *T1 from AMC13*  Order: LV1A, Calpulse, Resync, BC0 |
| GTX | | |
| 14 - 15 | Read | *Tracking links error* |
| 16 - 17 | Read | *Trigger links error* |
| 18 - 19 | Read | *Data packets received* |

# DAQ

This module is responsible for building events from OH packets and sending them to AMC13. It also does some basic checks of the data, monitors status of the FIFOs and manages the TTS state accordingly.

As soon as the data arrives from OH, it’s put into Input FIFO. At the same time various checks are done on this data. Once end of event is detected, an entry is made in Event FIFO, which holds event ID, BX ID, event size and some event status flags. Another process is monitoring Event FIFO and when it detects that this FIFO is not empty, it initiates the process of constructing and sending the event to AMC13 in the standard format (more on the format later).

End of event is detected when VFAT EC changes. Though due to BC0 resetting EC in VFAT2, we use BC to look for end of event for now. Timeout-based end of event will be added in the future.

When the data checks are performed, some global status flags are latched if an error is found. See register address table for a full list of these flags. Only a few of them are critical and are used to set TTS ERROR state, others can be read through IPBus.

More information on how this module works can be found here:   
<https://indico.cern.ch/event/453526/session/0/contribution/17/attachments/1169209/1688047/2015-10-13_EJ_GEM_readout_4.pdf>

TTS state encoding (according to CMS standard):

|  |  |  |
| --- | --- | --- |
| Value | Name | Description |
| 0x0 0xF | Disconnected | Hardware failure / broken communication |
| 0x1 | Overflow Warning | Imminent buffer overflow  Asserted when any FIFO is 75% full and lifted when it drains down below 60% |
| 0x2 | Out-of-Sync | Data is not synchronized. Currently this state is not used by this module, pending data analysis. In the future it could be used e.g. when L1A ID is different between OH and GLIB |
| 0x4 | Busy | Cannot accept triggers  Currently this state is only used during reset. It will also be used during resync (not implemented yet) |
| 0x8 | Ready | Ready to accept triggers |
| 0xC | Error | Any other condition that prevents this module from accepting triggers and requires a reset.  Currently this state is set when one of the following critical errors are detected:   * Input or event FIFO overflow * Input FIFO underflow (sign of incorrect event size in event FIFO) * Abnormally big event detected (more than 4095 VFAT blocks corresponding to the same event) |

There are 3 major groups of registers available: control, global state, OH-specific state.

## Addressing

Module ID 7

Address 0x7000000YY

0b 0110 0000 0000 0000 0000 0000 0YYY YYYY

|  |  |  |  |
| --- | --- | --- | --- |
| Y register | Bits | Mode | Function |
| Control register | | | |
| 0x0 | [0] | RW | DAQ Enable (default = 0)  If this is set to 0, there will be no data sent to AMC13 and TTS state will always be READY (0x8) |
| 0x0 | [07:04] | RW | TTS Override (default = 0)  When not 0, it will override the GLIB TTS state with the provided value (e.g. writing 0x8 will force GLIB to always be in TTS READY state) |
| 0x0 | [31] | RW | Reset (default = 0)  Clears all FIFOs, state flags and counters. It also stops and resets all state machines (no events will be built, recorded or sent during reset)  When set to 1, it will be held in reset state until 0 is explicitly written (this can be changed in the future if necessary) |
| Global state registers | | | |
| 0x1 | [0] | R | DAQLink Ready  When this is 1, it means that GLIB is in good communication with AMC13. It must be 1 for GLIB to be able to send data. |
| 0x1 | [1] | R | DAQ clock locked |
| 0x1 | [2] | R | TTC ready |
| 0x1 | [3] | R | DAQ FIFO almost full  No events will be sent when this bit is 1 (though events can still be built and stored in the Input and Event FIFOs) |
| 0x1 | [31:28] | R | TTS State |
| 0x2 | [15:0] | R | 8b/10b Not-in-Table error count on the AMC13 link |
| 0x3 | [15:0] | R | 8b/10b Dispersion error count on the AMC13 link |
| 0x4 | [23:0] | R | L1A ID |
| 0x5 | [31:0] | R | Number of events sent to AMC13 |
| OH-specific state registers (addresses below are for the first OH, subsequent OHs are offset by 0x10) | | | |
| 0x10 | [0] | R | OH-VFAT out-of-sync occurred  There was at least one VFAT block with VFAT BC different from OH BX ID |
| 0x10 | [1] | R | GLIB-OH out-of-sync occurred  There was at least one OH packet with BX ID different from GLIB BX ID |
| 0x10 | [2] | R | GLIB-VFAT out-of-sync occurred  There was at least one VFAT block with BC different from GLIB BX ID |
| 0x10 | [3] | R | OH out-of-sync occurred  There was at least one event with mixed OH BX IDs (OH BX ID is reported for every VFAT block, but not sent to AMC13) |
| 0x10 | [4] | R | Corruption: more than 24 VFATs in event |
| 0x10 | [5] | R | Corruption: VFAT block smaller than 192bits |
| 0x10 | [6] | R | Corruption: VFAT block bigger than 192bits |
| 0x10 | [7] | R | Corruption: VFAT marker not detected  There was at least one VFAT block not conforming to the pattern of Axxx Cxxx Exxx…… (see VFAT data format)  Note that this data will still be included in the current event and sent to AMC13, but it will not be considered in end-of-event detection. |
| 0x10 | [8] | R | Critical: Input FIFO overflow occurred  This bit is latched if Input FIFO was ever full when receiving new data – this means data was lost.  TTS ERROR is asserted when this bit is 1 |
| 0x10 | [9] | R | Critical: Input FIFO underflow occurred  This bit is latched if Input FIFO underflow was ever detected. This means that Event FIFO indicated that there should be more data than was stored in Input FIFO. This might happen due to overflow or some other malfunction.  TTS ERROR is asserted when this bit is 1 |
| 0x10 | [10] | R | Critical: Event FIFO overflow occurred  This bit is latched if Event FIFO was ever full when trying to build a new event. This means data was lost.  It’s not likely that this will ever be asserted because Input FIFO should overflow first.  TTS ERROR is asserted when this bit is 1 |
| 0x10 | [11] | R | Critical: Event too big occured  This bit is latched if there was an event containing more than 4096 VFAT blocks. Input FIFO and Event FIFO will be out-of-sync. This might happen if end-of-event is not detected properly or for whatever reason GLIB is receiving a stream of VFAT blocks indicating that they belong to the same event (EC/BC is the same)  TTS ERROR is asserted when this bit is 1 |
| 0x10 | [24] | R | Current status: Input FIFO is in underflow |
| 0x10 | [25] | R | Current status: Input FIFO is full |
| 0x10 | [26] | R | Current status: Input FIFO is near-full (75%) |
| 0x10 | [27] | R | Current status: Input FIFO is empty |
| 0x10 | [28] | R | Current status: Event FIFO is in underflow |
| 0x10 | [29] | R | Current status: Event FIFO is full |
| 0x10 | [30] | R | Current status: Event FIFO is near-full (75%) |
| 0x10 | [31] | R | Current status: Event FIFO is empty |
| 0x11 | [31:0] | R | Corrupted VFAT block counter  This counter is incremented when a VFAT block does not conform to the pattern of Axxx Cxxx Exxx…… (see VFAT data format)  Note that this data is still included in events and sent to AMC13, but it does not participate in end-of-event detection. |
| 0x12 | [23:0] | R | Current event number of the event builder  This counter starts at 1 and increments with each end-of-event detection. This number should be similar to the number of events sent to AMC13 in normal operation, but it might not always be exactly the same because there’s some latency between building an event and sending it. In addition, event sending could stop due to DAQ FIFO being almost full or DAQLink not being ready. |
| 0x19 | [31:0] | R | Debug: bits [31:0] of last received VFAT block + OH word |
| 0x1A | [31:0] | R | Debug: bits [63:32] of last received VFAT block + OH word |
| 0x1B | [31:0] | R | Debug: bits [95:64] of last received VFAT block + OH word |
| 0x1C | [31:0] | R | Debug: bits [127:96] of last received VFAT block + OH word |
| 0x1D | [31:0] | R | Debug: bits [159:128] of last received VFAT block + OH word |
| 0x1E | [31:0] | R | Debug: bits [191:160] of last received VFAT block + OH word |
| 0x1F | [31:0] | R | Debug: bits [223:192] of last received VFAT block + OH word |