

Global Trigger firmware Specification for MP7 platform for Upgrade Phase I

Herbert Bergauer, Babak Rahbaran, Johannes Wittmann

Institute of High Energy Physics (HEPHY)

<http://www.hephy.at>

<http://globaltrigger.hephy.at>

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Revision History

Doc Rev	Description of Change	Revision Date
2.48	Fixed typo in table (33) and updated chapter (7.2.1).	2024/09/30
2.47	Added chapter "Preventing timing errors by fixing cells in Vivado" (7.1.2).	2024/09/23
2.46	Added tables for AXO (27) and TOPO (28) models.	2024/08/14
2.45	Added chapter "Calo combination conditions with more than 4 requirements" (4.4.9.2).	2024/06/18
2.44	Updated chapters "Topological Trigger" (4.4.16.3) and "CICADA Trigger" (4.4.16.4).	2024/04/10
2.43	Added chapters "Topological Trigger" (4.4.16.3) and "CICADA Trigger" (4.4.16.4). Updated 4.2.3 and 4.4.5 for new structure of CICADA data.	2024/01/04
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2.41	Updated text (non-linear η scale) in "Definitions of CICADA data" (4.4.5).	2023/10/17
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2.39	Updated "Appendices" (7.6) for "External condition patch panel".	2023/09/19
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2.36	Added chapter "Calo-Layer1 optical interface" (4.2.3).	2023/09/04
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2.30	Updated table 35.	2023/02/21
2.29	Updated text for cuts on muon index bits (4.4.4 and 4.4.6). Fixed value of η range in 4.4.2.	2023/02/20

Doc Rev	Description of Change	Revision Date
2.28	Added tables (34) and (35), removed figure "Optical link inputs to Global Trigger". Removed chapter "GTH I/Os" from "Appendices".	2023/02/09
2.27	Added table for muon charge bits(17).	2023/01/16
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2.25	Updated text "LUTs for 1/deltaR**2 used in mass over deltaR calculations" (4.4.8.6).	2023/01/09
2.24	Cleaned up text and layout.	2022/12/15
2.23	Added chapter "Handling of timing errors in synthesis" (7.1.1).	2022/12/01
2.22	Cleaned up (used "textquotesingle").	2022/11/30
2.21	Updated "Configuration of GTHs" (7.2.4).	2022/11/24
2.20	Inserted chapter "GTH I/Os" to "Appendices".	2022/10/12
2.19	Added table "Firmware versions" (2).	2022/09/27
2.18	Updated "Appendices" (7).	2022/09/26
2.17	Updated text in "LUTs for $1/\Delta R^2$ " (4.4.8), added new chapter "Muon shower bits" (4.4.11).	2022/09/13
2.16	Updated text for Final-OR-mask and veto-mask (5.5.4 and 5.5.5). Updated <code>versions.tex</code> .	2022/09/09
2.15	Updated text for "fractional prescale", reset prescaler with "start" (5.5.3).	2022/08/17
2.14	Updated text for "fractional prescale" values (5.5.3).	2022/07/11
2.13	Inserted "Description of tests" to "Appendices" (7.1).	2022/03/25
2.12	Cleaned up text and tables in section "Framework" (3). Changed links to firmware modules (git branch name set in <code>versions.tex</code>).	2022/03/23
2.11	Added "Configuration of optical input links" and "Configuration of links to AMC13 (readout)" to "Appendices" (7.3 and 7.4).	2022/02/28
2.10	Inserted "Appendices" (7) and added references.	2022/02/25
2.9	Inserted "Simulation and build of firmware" and "Testing firmware" (2.2.2 and 2.2.3).	2022/02/15
2.8.1	Bug fixed in labels. Updated labels.	2022/02/14
2.8	Inserted "Implementation in firmware" for top-of-hierarchy of VHDL code (2.2.1). Updated labels.	2022/02/11
2.7	Updated text of section "Implementation in firmware" for Framework (3.1), GTL (4.3) and FDL (5.4).	2022/02/10
2.6	Inserted references and updated text in 2.2.	2022/02/09
2.5	Updated text in "Implementation in firmware" (4.3).	2022/01/10

Doc Rev	Description of Change	Revision Date
2.4.1	Bug fixed in definition of calo eta ranges (4.4.2).	2021/11/30
2.4	Updated data structure for jets with DISP bit (4.2.1).	2021/11/17
2.3	Inserted "Calculation of look-up-tables (LUTs) for correlation cuts" (4.4.8).	2021/11/10
2.2	Removed "VHDL-Templates for VHDL-Producer".	2021/09/24
2.1	Updated (and renamed) description of "Invariant mass over delta R calculation" (see 4.4.7.6).	2021/09/14
2.0	New structure of document for firmware versions 1.12.x and higher.	2021/02/10
1.53.1	Fixed typo in section "Invariant mass calculation for three objects" 4.4.7.7 .	2020/12/03
1.53	Updated text in section "VHDL-Templates for VHDL-Producer".	2020/09/31
1.52	Inserted links to VHDL modules.	2020/09/18
1.51	Updated text in section "Correlation conditions" 4.4.15 . Description is for v1.10.0 of Global Trigger Logic.	2020/09/17
1.50	Inserted description of "Invariant mass divided by delta R calculation" (see 4.4.7.6).	2020/09/10
1.49.1	Fixed typo (unconstrained pt).	2020/09/09
1.49	Inserted text for new muon structure in sections 4.2.2 , 4.4.4 and 4.4.15.1 . Added subsections in section "VHDL-Templates for VHDL-Producer"	2020/08/04
1.48	Additional text in section for calo calo overlap remover condition module.	2020/05/25
1.47	Inserted text in section Calorimeter Overlap Remover conditions and Calo Calo Overlap Remover Correlation conditions.	2020/04/16
1.46	Updated text in sections Calorimeter conditions, Muon conditions and Correlation conditions for changes which have been done for GTL VHDL version 1.8.0 (module names without version number, "five eta cuts").	2019/08/13
1.45	Inserted "Asymmetry" and "Centrality" of "Energy sums" (GTL VHDL version 1.6.0). Therefore updated sections 4.1 , 4.2.1 , 4.4.10 added section "Centrality condition" 4.4.14 and updated Table 5	2018/08/13
1.44	Updated text in section "Global Trigger Logic" (4) according to firmware version v1.5.0 of gtl_module.vhd.	2018/02/21
1.43	Updated text in section "Framework" (3) according to firmware version v1.2.3 of frame.vhd.	2018/01/19
1.42	New "icons" ET_{miss}^{HF} and HT_{miss}^{HF} in Table 5 and Section 4 . Updated glossary.	2016/11/11

Doc Rev	Description of Change	Revision Date
1.41	Updated table " μ FDL register map" (30) and section "Register map" (5.5.7.1). Moved "List of Tables" and "List of Figures" to the end of document. Inserted link to "Scales for inputs to μ GT" (4.3). Moved section "Software reset" to section "Framework" as subsection (3.2.6). Removed empty sections "IPBus", "Firmware Configuration" and "Bibliography".	2016/11/03
1.40	Updated sections "Calo-Layer2 optical interfaces" (4.2.1) and "Energy sum quantities conditions" (4.4.10) for tower-count trigger bits. Inserted section "Towercount condition" (4.4.13).	2016/10/25
1.39	Updated section "Calo-Layer2 optical interfaces" (4.2.1) for new energy sum quantities and minimum bias trigger bits. Updated sections "Firmware" (2), "Framework" (3) and "Final Desicion Logic" (5).	2016/06/09
1.38	Updated Text in section "Muon Muon Correlation condition module".	2016/01/15
1.37	Removed "Double objects requirements condition with spatial correlation", because not used anymore in the future, replaced by Correlation conditions.	2016/01/08
1.36	Minor changes in text and updated Figure 10.	2016/01/08
1.35	Changed colour in Figure 11 and updated text for correlation conditions (see section 4.4.15).	2016/01/07
1.34	Updated Figures 10 and 9 and text in calo calo correlation condition module.	2015/12/21
1.33	Inserted drawing of VHDL structure of cuts for correlation conditions (see Figure 12).	2015/11/18
1.32	Updated muon η ranges (Table 13) and inserted correlation conditions. Created scheme for conversion of calorimeter η and φ to muon scale for calo-muon-correlation conditions.	2015/11/17
1.31	Added Text in sections calo comparator module and muon comparator module.	2015/10/08
1.30	Updated Text in section "Final Desicion Logic" (5).	2015/10/06
1.29	Updated Figure 14 and Tables 30. Remained section "Calorimeter conditions module - version 2" to "Calorimeter conditions module - version 3", section "Muon conditions module" to "Muon conditions module - version 2" and section "Muon comparators module" to "Muon comparators module - version 2".	2015/10/02
1.28	Updated text and tables of η ranges for Calorimeter objects (see 4.4.2).	2015/09/22

Doc Rev	Description of Change	Revision Date
1.27	Renewed Figures in GTL and FDL (see Figure 8, 9 and 10) and FDL(see Figure 14 and 15). Added register bits description of FDL Register map (see section 5.5.7.1).	2015/09/16
1.26	Updated text, tables and listings of section "VHDL-Templates for VHDL-Producer".	2015/09/15
1.25	Corrected calculation of muon η step width (see 4.4.4).	2015/09/10
1.24	Edited text in Table 22.	2015/08/28
1.23	Updated definition of η ranges for Calorimeter objects and Muon objects.	2015/08/20
1.22	Added section Calo Muon Correlation condition.	2015/08/19
1.21	Added section "Register map" (5.5.7.1) for μ FDL.	2015/06/26
1.20	Updated figures (8, 9 and 10) for GTL and edited section "Correlation conditions" (see 4.4.15).	2015/05/08
1.19	Added tables for calorimeter isolation-bits and for muon quality- and isolation-bits definition (12, 15 and 16). Edited section glossary and acronyms.	2015/05/07
1.18	Added text for "Energy sum conditions" (4.4.10) and updated chapters for "Calorimeter conditions" for version 2. Inserted isolation bits for electron/ γ and tau objects (4.4.2).	2015/05/06
1.17	Minor changes "Demux Lane Data" (see 3.2.2) and "Muon data" (see 4.4.4).	2014/11/06
1.16	Edited Section "Energy sum quantities conditions" (see 4.4.10).	2014/10/08
1.15	Added sections "Configuration of optical connections" (3.2.1), "Demux Lane Data" (3.2.2) and "Lane Mapping Process" (3.2.3) to framework. Removed tables of optical interfaces from gtl and referenced to tables in framework.	2014/10/07
1.14	Minor changes in "Calorimeter conditions" and "Muon conditions" .	2014/07/01
1.13	Updated with minor changes in "Muon conditions".	2014/06/17
1.12.1	Fixed bug in Figure 11.	2014/04/30
1.12	Updated section "Muon conditions".	2014/04/22
1.11	Removed section "Muon charge module" and added new section "Muon charge correlation module" (see 4.4.7.9). Edited text in section and subsections "Muon conditions definition".	2014/04/15
1.10	Changed Figure 11 and minor changes in text for anti-clockwise behaviour in φ .	2014/04/04
1.9	Added definition for "calorimeter conditions over bx", see section.	2014/03/12
1.8	Changed text of condition description in subsections Calo conditions definition and Muon conditions definition.	2014/02/12

Doc Rev	Description of Change	Revision Date
1.7	Updated calorimeter data structure in 4.2.1 .	2013/12/03
1.6	Updated muon data structure in 4.2.2	2013/12/02
1.5	Moved decription of VHDL templates for TME to "VHDL-Templates for VHDL-Producer".	2013/11/18
1.4	Subsection 4.2 added to section 4 .	2013/11/11
1.3	GTL and FDL firmware implemented for new data structure (GTL firmware version v1.0.0 [fix part of GTL], FDL firmware version v1.0.0)	2013/11/06
1.2	New framework implementation based on new object types definition. Additionally, the ROP is implemented based on production requirements.	2013/10/13
1.1	First framework implementation and ROP.	2012/07/01
1.0	Document created.	2012/02/22

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1 Global Trigger System overview

The Global Trigger System is based on MicroTCA technology and 10 Gbps optical links. A set of 6 MP7 boards (for MP7 documentation see [1], for MP7 firmware see [2]) with a FPGA of the powerful Xilinx Virtex-7 family (XC7VX690TFFG1927-2, see [3]) is available. The Global Trigger firmware is implemented on these FPGAs. Every FPGA contains a part of the VHDL representation of a L1 Menu, the partitioning is done by VHDL Producer tool. The trigger decision of every MP7 board is collected on an AMC502 board to generate the "final OR" signal which triggers the readout of the detector.

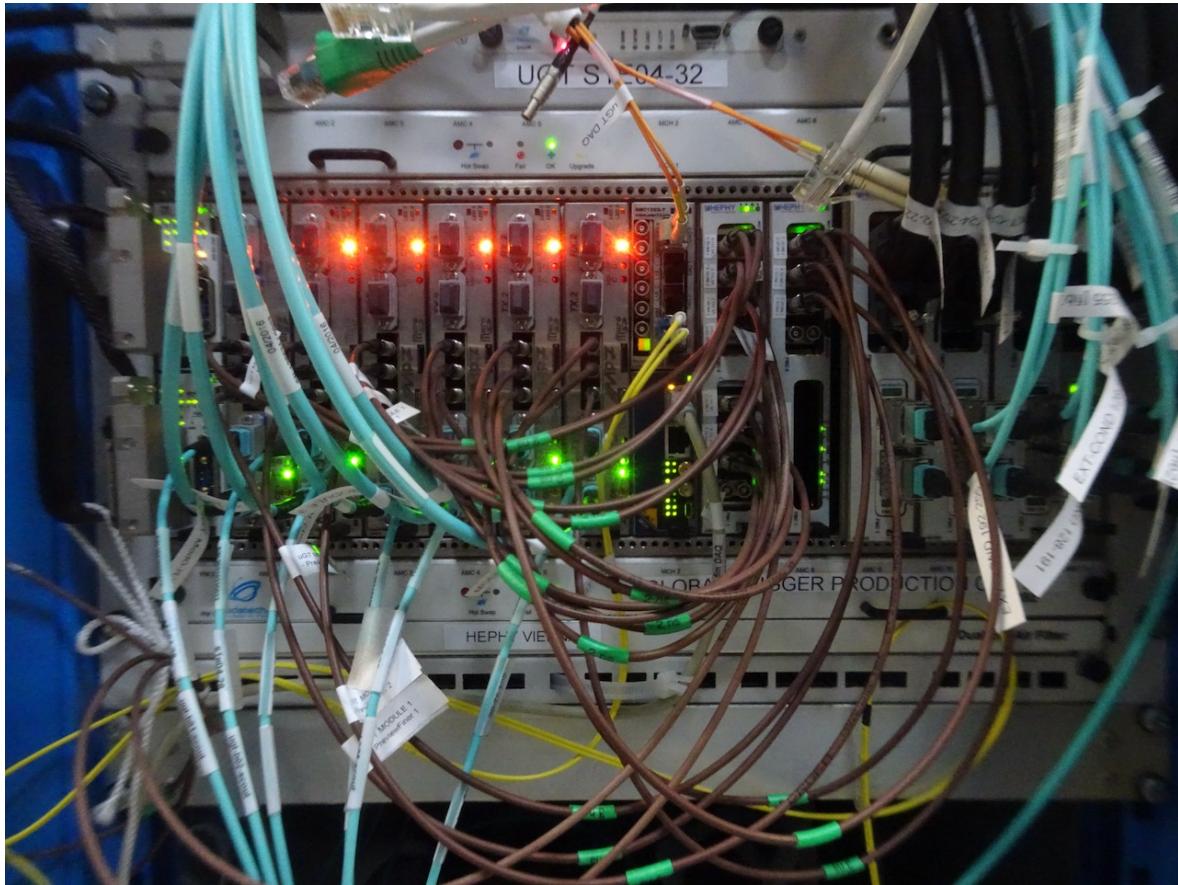


Figure 1: μ GT crate

2 Firmware overview

The figure 2 shows the architecture of μ GT payload. It consists of framework and the algorithm logic which consists of the following modules:

1. Global Trigger Logic Data Mapping
2. μ GTL

3. μ FDL

The output mux (part of framework) collects data for read-out record which are send via MP7 read-out to AMC13.

The IPBus system allows the control of hardware via a ‘virtual bus’, using a standard IP-over-gigabit-Ethernet network connection.

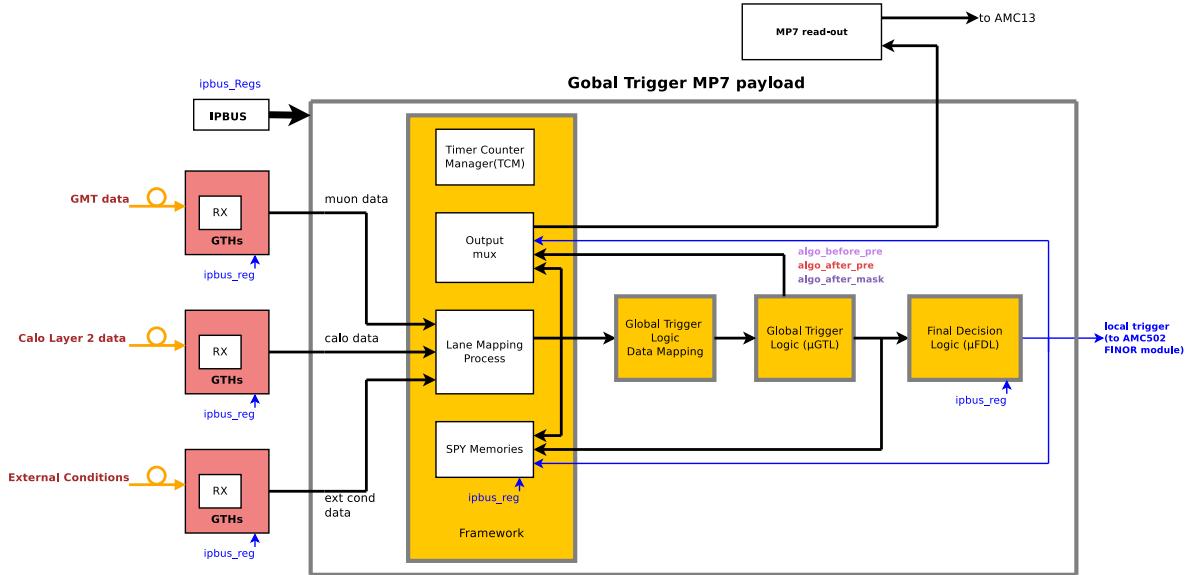


Figure 2: μ GT payload

2.1 Firmware versions

This firmware description is based on following versions:

Table 2: Firmware versions

Entity	Version
Global Trigger firmware	v1.30.0
Framework	v1.4.2
Global Trigger Logic	v1.23.0
Final Decision Logic	v1.4.1

2.2 Directory structure of Global Trigger firmware

In Global Trigger repository all files for building firmware are in directory '`firmware`' with subdirectories for synthesis configuration files ('`cfg`' and '`ucf`'), for VHDL source files ('`hdl`'), for memory files build from IPs ('`ngc`') and simulation files ('`sim`').

All definitions for VHDL code are in '[hdl/packages](#)', VHDL source files representing Global Trigger firmware are in '[hdl/payload](#)' with subdirectories (for '[gtl](#)', '[fdl](#)', '[frame](#)' and '[ipbus](#)').

2.2.1 Implementation in firmware

Top-of-hierarchy of VHDL code is '[mp7_payload.vhd](#)'.

Listing 1 contains the entity-declaration of the top-of-hierarchy file.

Listing 1: Entity declaration of mp7_payload.vhd

```
entity mp7_payload is
  port(
    clk: in std_logic; -- ipbus signals
    rst: in std_logic;
    ipb_in: in ipb_wbus;
    ipb_out: out ipb_rbus;
    clk_payload : in std_logic_vector(2 downto 0);
    rst_payload : in std_logic_vector(2 downto 0);
    clk_p: in std_logic; -- data clock
    rst_loc: in std_logic_vector(N_REGION - 1 downto 0);
    clken_loc: in std_logic_vector(N_REGION - 1 downto 0);
    ctrs: in ttc_stuff_array;
    lla: in std_logic; -- L1A input
    bc0: out std_logic;
    d: in ldata(4 * N_REGION - 1 downto 0); -- data in
    q: out ldata(4 * N_REGION - 1 downto 0); -- data out
    gpio: out std_logic_vector(29 downto 0); -- IO to mezzanine connector
    gpio_en: out std_logic_vector(29 downto 0) -- IO to mezzanine connector (
      three-state enables)
  );
end mp7_payload;
```

All the declarations for arrays ("type"), parameters ("constant") and look-up-tables ("constant") used in modules are available in '[gtl_pkg.vhd](#)' package-file.

Table 3: Explanation of Listing 1

Item	Explanation
clk	IPBus clock input.
rst	IPBus reset input.
ipb_in	IPBus data input.
ipb_out	IPBus data output.
clk_payload	clock inputs [clk_payload(0)=lhc_clock].
rst_payload	reset inputs.
clk_p	clock 240MHz.
rst_loc	not used.
clken_loc	not used.
ctrs	TTC signals input.
l1a	L1A signal input.
bc0	bunch counter reset output.
d	data input (from optical links).
q	data output (to optical links).
gpio	signal outputs to mezzanine board.
gpio_en	enable (signal) outputs to mezzanine board.

2.2.2 Simulation and build of firmware

In document '[README.md](#)' one can find instructions for setting up simulation and build environments. For simulation and building of firmware access rights to GitLab (MP7 firmware) are mandatory.

2.2.3 Testing firmware

Testing of firmware in hardware at CMS P5 (see [7.1](#)) is done with script "multiboard_function_test" ("tdf run multiboard_function_test -h"). Therefore a XML file of the L1Menu and a test vector file must be available at the crate. The firmware of the L1Menu which should be tested must be loaded into the 6 MP7 boards before testing ("tdf run uploadfw_gt -h"). For checking crate status execute "tdf run crate_status".

This testing is restricted to persons with access to μ GT crates at P5.

3 Framework

This description is for version v1.4.2 of Framework.

Remark:

with frame v1.2.3 "Delay Manager" ('dm.vhd') and "Data Source Multiplexer" ('dsmux.vhd') are removed because these features were never used in production system, only for tests. Sim-mem data not used anymore, because of removed dsmux. The reason of removing is to get more available resources.

Data from the GTH interfaces are demultiplexed (from 240 MHz clock domain to LHC clock domain, see Demux Lane Data [3.2.2](#)) and mapped to objects structure in Lane Mapping Process (LMP) for μ GTL input and SPY I memory.

3.1 Implementation in firmware

[Listing 2](#) contains the entity declaration of '[frame.vhd](#)'.

Listing 2: Entity declaration of `frame.vhd`

```
entity frame is
  generic(
    NR_LANES : positive
  );
  port(
    ipb_clk : in std_logic;
    ipb_rst : in std_logic;
    ipb_in : in ipb_wbus;
    ipb_out : out ipb_rbus;
    ctrs : in ttc_stuff_array; --mp7 ttc ctrs
    clk240 : in std_logic;
    lhc_clk : in std_logic;
    lhc_RST_o : out std_logic;
    bc0 : in std_logic;
    ec0 : in std_logic;
    oc0 : in std_logic;
    start : in std_logic;
    l1a : in std_logic;
    bcres_d : out std_logic;
    bcres_d_FDL : out std_logic;
    start_lumisection : out std_logic;
    lane_data_in : in ldata(NR_LANES-1 downto 0);
    lane_data_out : out ldata(NR_LANES-1 downto 0);
    lhc_data_2_gtl_o : out lhc_data_t;
    prescale_factor_set_index_rop : in std_logic_vector(7 downto 0);
    algo_after_gtLogic_rop : in std_logic_vector(MAX_NR_ALGOS-1 downto 0);
    algo_after_bxomask_rop : in std_logic_vector(MAX_NR_ALGOS-1 downto 0);
    algo_after_prescaler_rop : in std_logic_vector(MAX_NR_ALGOS-1 downto 0);
    local_finor_rop : in std_logic;
    local_veto_rop : in std_logic;
```

3 Framework

```
    finor_rop : in std_logic;
    local_finor_with_veto_2_spy2 : in std_logic
  );
end frame;
```

Table 4: Explanation of Listing 2

Item	Explanation
NR_LANES	number of used optical links.
ipb_clk	IPBus clock (input).
ipb_RST	IPBus reset (input).
ipb_in	IPBus data (input).
ipb_out	IPBus data (output).
ctrs	TTC control signals (input).
clk240	clock (input) 240 MHz.
lhc_clk	clock (input) (LHC clock).
lhc_RST_o	reset (output).
bc0	TTC BGo bunch counter reset (input).
ec0	TTC BGo event counter reset (input).
oc0	TTC BGo orbit counter reset (input).
start	TTC BGo start (input).
l1a	L1 access signal (input).
bcres_d	delayed bunch counter reset (output).
bcres_d_FDL	delayed bunch counter reset (output) fot μ FDL.
start_lumisection	begin of lumisection (output).
lane_data_in	data from GTHs (optical links) (input) (240MHz domain).
lane_data_out	data to GTHs (optical links) (output) (240MHz domain).
lhc_data_2_gtl_o	data to μ GTL (output) (40MHz domain).
prescale_factor_set_in	prescale factor set data (input).
algo_after_gtLogic_rop	algos after μ GTL (input).
algo_after_bxomask_rop	algos after BX mask (input).
algo_after_prescaler_rop	algos after prescaler (input).
local_finor_rop	local FINOR (input).
local_veto_rop	local VETO (input).
finor_rop	FINOR (input).
local_finor_with_veto_2_spy2	local FINOR with VETO to spy mem (input).

3.2 Main parts

The top-of-hierarchy module of framework ('`frame.vhd`') contains

- demultiplexer of lane data
- lane mapping
- spy memories
- timer counter manager
- register

3.2.1 Configuration of optical connections

The configuration of the optical connections from GMT, Calo-Layer2 and External conditions is done as described in Table 5, where frame means 32 bits data in a 240 MHz domain.

Table 5: Configuration of optical connections

link	frame					
	0	1	2	3	4	5
0	reserved	reserved	muon obj. 0 [0..31]	muon obj. 0 [32..63]	muon obj. 1 [0..31]	muon obj. 1 [32..63]
1	reserved	reserved	muon obj. 2 [0..31]	muon obj. 2 [32..63]	muon obj. 3 [0..31]	muon obj. 3 [32..63]
2	reserved	reserved	muon obj. 4 [0..31]	muon obj. 4 [32..63]	muon obj. 5 [0..31]	muon obj. 5 [32..63]
3	reserved	reserved	muon obj. 6 [0..31]	muon obj. 6 [32..63]	muon obj. 7 [0..31]	muon obj. 7 [32..63]
4	electron/ γ obj. 0	electron/ γ obj. 1	electron/ γ obj. 2	electron/ γ obj. 3	electron/ γ obj. 4	electron/ γ obj. 5
5	electron/ γ obj. 6	electron/ γ obj. 7	electron/ γ obj. 8	electron/ γ obj. 9	electron/ γ obj. 10	electron/ γ obj. 11
6	jet obj. 0	jet obj. 1	jet obj. 2	jet obj. 3	jet obj. 4	jet obj. 5
7	jet obj. 6	jet obj. 7	jet obj. 8	jet obj. 9	jet obj. 10	jet obj. 11
8	tau obj. 0	tau obj. 1	tau obj. 2	tau obj. 3	tau obj. 4	tau obj. 5
9	tau obj. 6	tau obj. 7	tau obj. 8	tau obj. 9	tau obj. 10	tau obj. 11
10	ET ETTEM MBT0HFP	HT TOWER- COUNT MBT0HFM	ET_{miss} ASYMET MBT1HFP	HT_{miss} ASYMHT MBT1HFM	ET_{miss}^{HF} ASYM- ETHF CENT[3:0]	HT_{miss}^{HF} ASYM- HTHF CENT[7:4]
11	free	free	free	free	free	free
12	external- conditions [0..31]	external- conditions [32..63]	reserved	reserved	reserved	reserved
13	external- conditions [64..95]	external- conditions [96..127]	reserved	reserved	reserved	reserved
14	external- conditions [128..159]	external- conditions [160..191]	reserved	reserved	reserved	reserved
15	external- conditions [192..223]	external- conditions [224..255]	reserved	reserved	reserved	reserved
71	0x7c/0x3c	ZDC-	ZDC+	0x0000	counter	0x0000

3.2.2 Demux Lane Data

Data from GTH interfaces are in the 240 MHz clock domain. The demultiplexing to the LHC clock domain (about 40 MHz) is done in '[demux_lane_data.vhd](#)', which is instantiated in '[frame.vhd](#)' for currently 16 input links.

3.2.3 Lane Mapping Process

In the Lane Mapping Process module data from the links are mapped to objects structure defined in '[lhc_data_pkg.vhd](#)'.

3.2.3.1 Implementation

Currently lane mapping is "fixed" in '[lmp.vhd](#)' module, see Table 6 (energy sum quantities¹: including minimum bias trigger bits, towercounts, asymmetry and centrality bits).

Table 6: Current lane mapping

lane	objects
0	muon objects 0..1
1	muon objects 2..3
2	muon objects 4..5
3	muon objects 6..7
4	electron/ γ objects 0..5
5	electron/ γ objects 6..11
6	jet object 0..5
7	jet object 6..11
8	tau object 0..5
9	tau object 6..11
10	energy sum quantities ¹
11	n/a (currently not used)
12	external-conditions [0..63]
13	external-conditions [64..127]
14	external-conditions [128..191]
15	external-conditions [192..255]
71	zdc- / zdc+

3.2.4 SPY Memory

Remark:

with frame v1.2.3 simulation memory (SIM Memory) data not useable anymore, because of removed "Data Source Multiplexer". The reason for removing "Data Source Multiplexer" is to get more available resources.

SPY memory III for ROP data is not used anymore.

Figure 3 shows the SPY memory subsystem of Framework. It is used to calibrate the system and to record results of the μ GTL and μ FDL.

3.2.4.1 Implementation

The memory subsystem consists of four three parts, which will be discussed in more detail in the following sections:

- SPY Trigger
- SPY Memory I
- SPY Memory II

3.2.4.1.1 SPY Trigger

The SPY trigger controls the SPY memories and decides when data is recorded. It can be configured and controlled using software registers 3.1 and 3.2.

Listing 3 contains the entity declaration of the '[spytrig.vhd](#)'.

Listing 3: SPY trigger interface specification

```
entity spytrig is
  port
  (
    lhc_clk      : in  std_logic;
    lhc_rst      : in  std_logic;
    orbit_nr     : in  orbit_nr_t;
    bx_nr        : in  bx_nr_t;
    sw_reg_i     : in  sw_reg_spytrigger_in_t;
    sw_reg_o     : out sw_reg_spytrigger_out_t;
    spy1_o       : out std_logic;
    spy2_o       : out std_logic
  );
end;
```

When the SPY trigger receives a "spy12" command (next or once) over the software register interface, it asserts the *spy1* and *spy2* signals for the appropriate orbit. This means that the *spy* signals go high with the bunch crossing counter reaching the value zero and stay high until it reaches zero again (overflow).

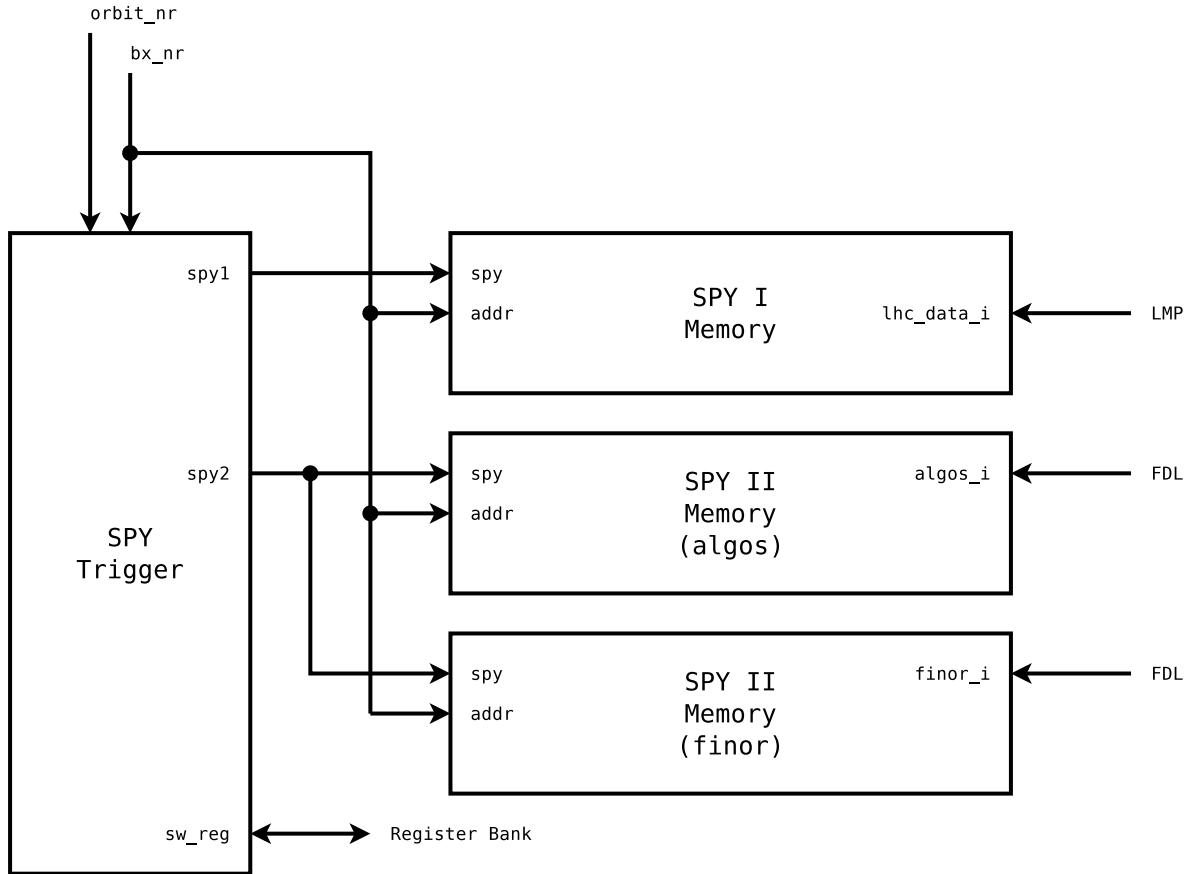


Figure 3: Memory subsystem

3.2.4.1.2 SPY memory I

SPY memory I stores data from LMP (coming from GTHs) to check the alignment of the data, for simulation and test purposes. It is composed of 72 4096x32 bits memories (to cover 3564 bunch crossings with 32 bits datawidth) for all input data. The 4096x32 memory has an input port for 32 bits data at the 40MHz clock domain and an IPBus interface to read the content. Memory address is given by bunch crossing counter (40MHz clock domain).

3.2.4.1.3 SPY memory II

SPY memory II is divided into two subcomponents, to store the "algos" and "finor" outputs of the μ FDL, where memory for "algos" has 16 4096x32 bits memories (16x32=512 algos) and "finor" is made of only one (for finor with veto). Both have the same architecture as SPY memory I.

3.2.5 Timer Counter Manager

The Timer Counter Manager (TCM) provides different counters, listed in Table 7 and a set of registers.

3.2.5.1 Counter Overview

Table 7: Counters of Timer Counter Manager

Counter	range	increase condition	reset condition	Comments
bx_nr (3.3)	0..3563	rising_edge(lhc_clk)	overflow	
event_nr (3.4)	$0..2^{32} - 1$	l1a=1 and rising_edge(lhc_clk)	BGo: event counter reset	
trigger_nr (3.5)	$0..2^{48} - 1$	l1a=1 and rising_edge(lhc_clk)	BGo: start run	
orbit_nr (3.6)	$0..2^{48} - 1$	overflow of bx_nr	BGo: orbit counter reset	
luminosity_seg_nr (3.7)	$0..2^{32} - 1$	rising_edge(orbit_nr(18))	BGo: orbit counter reset	

3.2.5.2 Counters for bunch crossing-, orbit- and luminosity segment number

The counter for bunch crossing number (*bx_nr*) is zero at startup and increased at every LHC clock cycle as depicted in figure 4. Its maximal value is 3563 (0xdeb), then it automatically overflows and starts at zero again (see figure 5). Exactly when *bx_nr* = 0, delayed BC0 (*bcres_d*) has to be asserted. Otherwise the counter is out of synchronization. If this happens, the software register *err_det* is set and the counter waits for the next *bcres_d* to synchronize again. The value of bunch crossing number can be read from "TCM Bunch Crossing Number Register" (3.3).

The counter for orbit number (*orbit_nr*) is 1 at startup and increased at every end of orbit (*bx_nr* = 3563). It is set to 1 with orbit counter reset (TTC signal *oc0*). The value of orbit number can be read from "TCM Orbit Number Register" (3.6).

The counter for luminosity segment number (*luminosity_seg_nr*) is increased, if signal *start* (TTC signal) was applied and counter for orbit number (*orbit_nr*) is greater than a given value for length of luminosity segment period (currently = 262144 [0x40000], see '[gt_mp7_core_pkg.vhd](#)'). The value of luminosity segment number can be read from "TCM Luminosity Segment Number Register" (3.7).

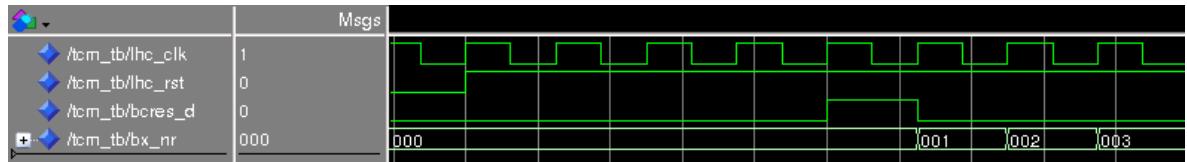


Figure 4: start of the bunch crossing number with the first *bcres_d*



Figure 5: normal operation of the bunch crossing number

3.2.5.3 Bunch crossing counter error

As stated above, `bcres_d` has to be asserted exactly when `bx_nr = 0`, otherwise the bunch crossing counter is out of sync. Then the software register `err_det` is set as depicted in figure 6. Signal `err_det` can be reset via software event register `err_det_reset_event` as depicted in figure 7.

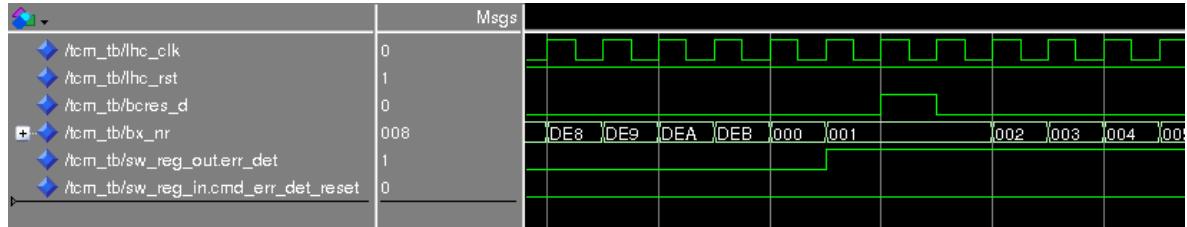


Figure 6: set of the software register `err_det` when `bc_res_d` is not asserted correctly

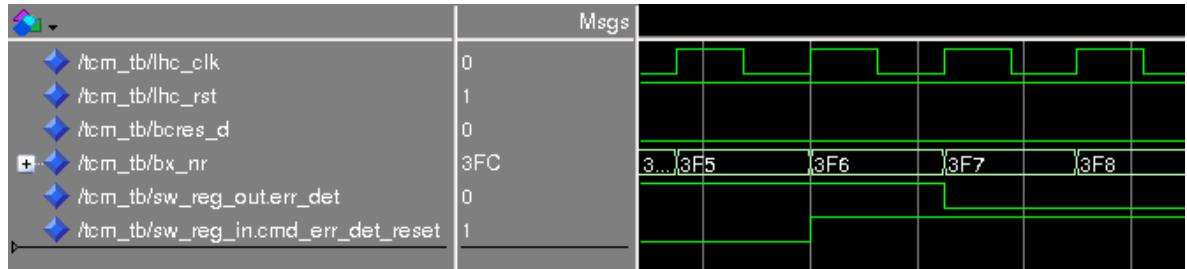


Figure 7: reset of the software register `err_det` when `err_det_reset_event` toggles

The TCM implements two additional counters (`bx_nr_chk` and `bx_nr_max`) for debugging purposes. These counters are not visible with any other module but readable via software. Counter `bx_nr_chk` has 32 bits that increased with every LHC clock cycle and set to 0 with `bcres_d`. Value `bx_nr_max` holds the highest `bx_nr_chk` ever reached (should be 3563, if the link is aligned).

3.2.5.4 Counters for event- and trigger number

The counters for event number (`event_nr`) and trigger number (`trigger_nr`) are increased with L1A signal. Event number counter is set to 0 with `ec0` signal, trigger number counter with `start` (TTC signals). The values of event number and trigger number can be read from "TCM Event Number Register" (3.4) and "TCM Trigger Number Register" (3.5).

3.2.6 Software Reset

The software reset module provides the possibility for a software reset via the software reset register `sw_reset_event`, see 3.17.

3.2.7 Registers

3.2.7.1 Register map

The register map for Framework has a base address of 0x80000000.

Table 8: Framework register map

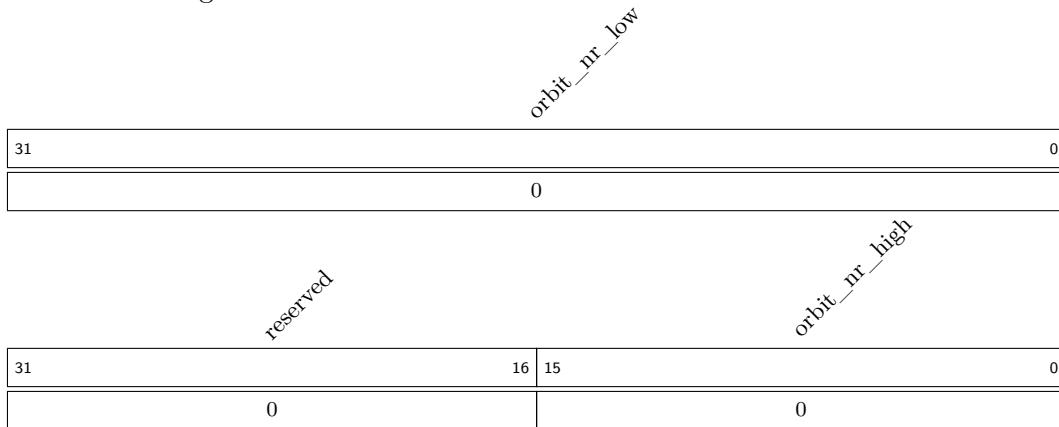
Offset	Register name	Access	Description
0x80000000	Timestamp	r	read-only register for timestamp begin of synthesis.
0x80000001	Hostname	r	4 read-only registers for hostname of synthesis platform.
0x80000009	Username	r	4 read-only registers for username of synthesis.
0x80000012	Frame version	r	read-only register for Global Trigger firmware version.
0x80000013	Build version	r	read-only register for build version of Global Trigger firmware.
0x80000800	Reset register	r/w	register for reset pulse and counter reset of counters.
0x80200000	Spy mem finor	r/w	4096 memory addresses for finor and veto.
0x80240000	Spy mem algos (0)	r/w	4096 memory addresses for algos[31:0].
0x80241000	Spy mem algos (1)	r/w	4096 memory addresses for algos[63:32].
...
0x8024F000	Spy mem algos (15)	r/w	4096 memory addresses for algos[511:480].
0x80300000	Spy mem (0)	r/w	4096 memory addresses for input data.
0x80301000	Spy mem (1)	r/w	4096 memory addresses for input data.
...
0x80347000	Spy mem (71)	r/w	4096 memory addresses for input data.
0x80700000	Spytrigger: orbit nr low	r/w	register for lower 32 bits of spy trigger orbit number.
0x80700001	Spytrigger: orbit nr high	r/w	register for higher 32 bits of spy trigger orbit number.
0x80700002	Spytrigger: control	r/w	control register for spy12.
0x80700003	Software reset	r/w	software reset register.
0x80700010	Spytrigger status	r	status register of spytrigger.
0x80700012	TCM status	r	status register of TCM.
0x80700016	TCM status: orbit nr low	r	read-only register for lower 32 bits of orbit number.

Table 8: Framework register map

Offset	Register name	Access	Description
0x80700017	TCM status: orbit_nr_high	r	read-only register for higher 32 bits of orbit number.
0x80700019	TCM status: bx_nr_max	r	read-only register for maximum Bx number.
0x8070001C	TCM status: lum_seg_nr	r	read-only register for luminosity segment number.

3.2.7.2 Register details

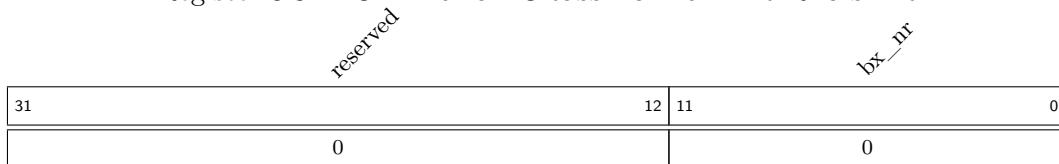
Register 3.1: SPY TRIGGER ORBIT NUMBER REGISTERS



orbit_nr_low 32 low bits of the 48 bit orbit number, used for the spy once trigger.

orbit_nr_high 16 high bits of the 48 bit orbit number, used for the spy once trigger.

Register 3.3: TCM BUNCH CROSSING NUMBER REGISTER

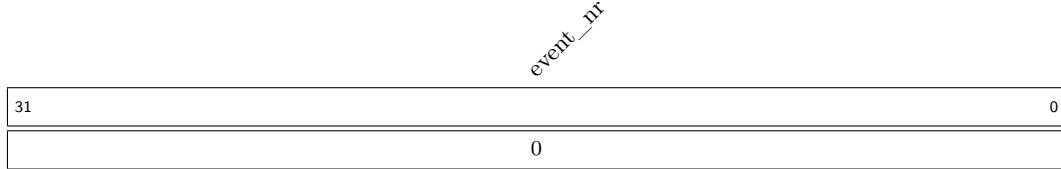


Register 3.2: SPY TRIGGER CONFIGURATION REGISTER

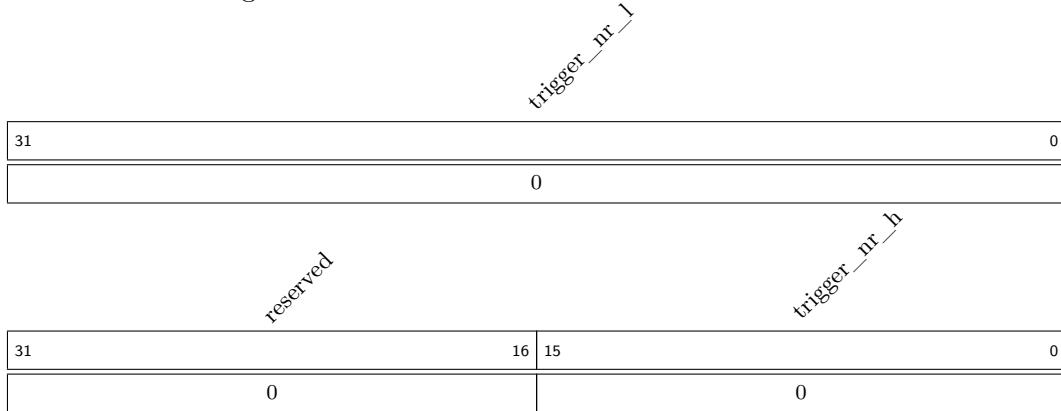
spy12_bsy	spy12_rdy	spy12_err	reserved				clr_spy12_err	clr_spy3_rdy	clr_spy12_rdy	clr_spy12_next	clr_spy12_once
31	29	27	26				6	5	4	3	1
0	0	0		0			0	0	0	0	0

- spy12_once** Triggers the recording of the selected orbit to SPY memories I and II, when written with 1.
- spy12_next** Triggers the recording of the next whole orbit to SPY memories I and II, when written with 1.
- clr_spy12_rdy** Clears the ready flag of the SPY trigger for SPY memories I and II, when written with 1.
- clr_spy3_rdy** Clears the ready flag of the SPY trigger for SPY memory III, when written with 1.
- clr_spy12_err** Clears the error flag, when written with 1.
- spy12_bsy** Indicates that the SPY trigger for SPY memories I and II is busy.
- spy12_rdy** Indicates that one orbit has been recorded in SPY memories I and II and that the SPY trigger is ready for new commands.
- spy12_err** Indicates an error condition (Set only when the selected orbit number for the spy once trigger lies in the past and can therefore not be recorded).

Register 3.4: TCM EVENT NUMBER REGISTER



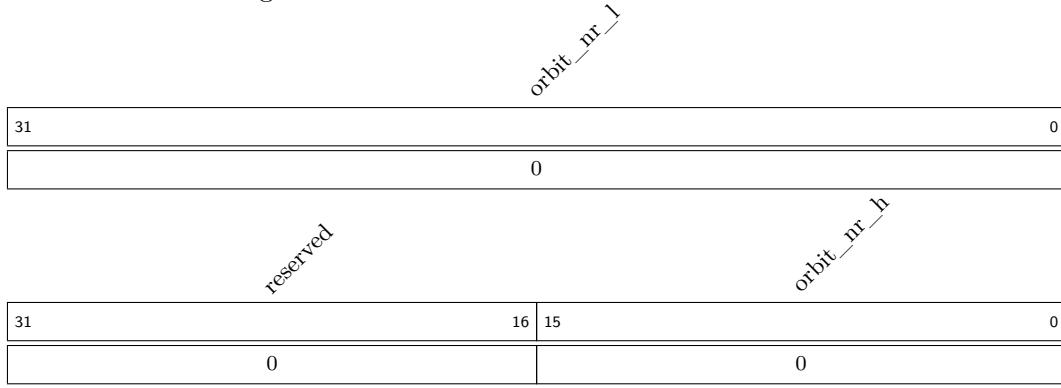
Register 3.5: TCM TRIGGER NUMBER REGISTERS



trigger_nr_l 32 low bits of the 48 bit trigger number.

trigger_nr_h 16 high bits of the 48 bit trigger number.

Register 3.6: TCM ORBIT NUMBER REGISTERS



orbit_nr_l 32 low bits of the 48 bit orbit number.

orbit_nr_h 16 high bits of the 48 bit orbit number.

Register 3.7: TCM LUMINOSITY SEGMENT NUMBER REGISTER

luminosity_seg_nr	
31	0
0	

Register 3.8: TCM BUNCH CROSSING NUMBER μ FDL REGISTER

reserved		bx_nr_d_fdl	
31	12	11	0
0		0	

Register 3.9: TCM BUNCH CROSSING NUMBER CHECK REGISTER

bx_nr_chk	
31	0
0	

Register 3.10: TCM BUNCH CROSSING NUMBER MAX REGISTER

bx_nr_max	
31	0
0	

Register 3.11: TCM_CMD_IGN_BCRE

				reserved		cnd_ign_bcres
31					1	0
	0				0	Reset

cmd_ign_bcres bcres is ignored (not checked) when this is set.

Register 3.12: TCM_ERR_DET

31						1 0	

err_det set when out of synchronization.

Register 3.13: TCM_ERR_DET_RESET_EVENT

err_det_reset_event resets err_det.

Register 3.14: TCM BGo SIGNALS

34		reserved	4	3 0
	0			0

BGo signals for simulation of BGo signals

3 Framework

Register 3.15: TCM_BGo_EVENT

The diagram illustrates the structure of the BGo_event register. It consists of a horizontal bar divided into four segments by vertical lines. The first segment on the left contains the value '31'. The second segment, labeled 'reserved', spans 11 bits. The third segment, labeled 'BGo', spans 11 bits and contains the value '0'. The fourth segment, labeled 'event', spans 11 bits and contains the value '0'. To the right of the 'event' field is a small box labeled 'Reset'.

BGo_event replaces the BGo input signals with the sw-register BGo signals for exactly one clock cycle.

Register 3.16: TCM LUMINOSITY_SEG_PERIOD_MSK

31	x	4	0	0	0	0
0						

Reset

`luminosity_seg_period_msk` `luminosity_seg_nr` is increased when the orbit_nr mod lum_seg_period_mask = 0.

Register 3.17: SOFTWARE RESET REGISTER

The diagram shows the memory map for the SW_RESET register. It consists of two horizontal rows representing memory addresses. The top row is labeled "SW_RESET" and the bottom row is labeled "Reset". The address range for the SW_RESET register is from \$0000_0000 to \$0000_0004. The bottom row shows the bit fields: bit 31 is labeled "31", bit 0 is labeled "0", and bits 1 and 0 are grouped together under the label "Reset". Above the bit 1/0 group, the label "sw_reset_event" is written diagonally. Between the two rows, the label "reserved" is written diagonally.

sw_reset_event generates a reset signal for exactly one clock cycle.

4 Global Trigger Logic

This description is for version v1.23.0 of Global Trigger Logic.

The Global Trigger Logic (μ GTL) firmware contains conditions and algorithms for trigger decision (see Figure 8).

Definitions are based on document [4].

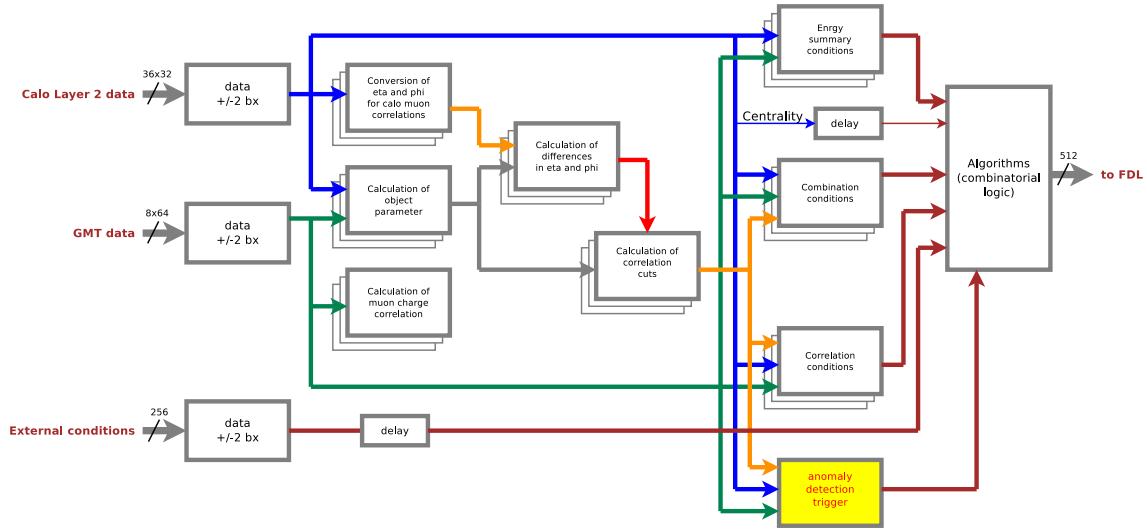


Figure 8: μ GTL firmware

4.1 μ GTL Interface

Inputs:

- Calo-Layer2 data
 - Electron/ γ objects (EG0..EG11)
 - Jet objects (JET0..JET11)
 - Tau objects (TAU0..TAU11)
 - Energy summary information:
 - * Total Et (ET)
 - * Total Et from ECAL only (ETTEM)
 - * Total calibrated Et in jets (HT)
 - * Missing Et (ET_{miss})
 - * Missing Et including HF (ET_{miss}^{HF})
 - * Missing Ht objects (HT_{miss})
 - * Missing Ht including HF (HT_{miss}^{HF})

- * "Asymmetry" information (ASYMET, ASYMHT, ASYMETHF, ASYMHTHF)
- Minimum bias HF bits (MBT0HFP, MBT0HFM, MBT1HFP and MBT1HFM; part of energy summary information data structure)
- Towercount bits (TOWERCOUNT, number of firing HCAL towers; part of energy summary information data structure)
- "Centrality" bits (CENT0..CENT7; part of energy summary information data structure)
- Global Muon Trigger data
 - Muon objects (MU0..MU7)
 - Muon shower bits (bit 61 on MU0, MU2, MU4, MU6)
- Calo-Layer1 data
 - Boosted jet objects (BJET0..BJET5)
 - Anomaly Detection Integer part
 - Anomaly Detection Decimal part
 - Heavy Ion bit(s0)
- External conditions

Outputs:

- Algorithms

4.2 Definition of optical interfaces

Remark:

All definitions for scales in the following chapters are from a CMS Detector Note: "Scales for inputs to μ GT" (see [4]).

4.2.1 Calo-Layer2 optical interface

The data structure of an electron/ γ object (bits 27..31 are not defined yet, reserved for quality, ...):

31	27	26	25	24	17	16	9	8	0
<i>qual/spare</i>	<i>iso</i>		φ		η			E_T	

The data structure of a jet object:

Remark: "D" means DISP bit (displaced jet) - "qu" means quality flags - "sp" means spare bits.

31	30	29	28	27	26	19	18	11	10	0
<i>sp</i>	<i>qu</i>	<i>D</i>		φ		η			E_T	

The data structure of a tau object (bits 27..31 are not defined yet, reserved for quality, ...):

31	27	26	25	24	17	16	9	8	0
<i>qual/spare</i>	<i>iso</i>		φ		η			E_T	

The data structure of "Total Et" (E_T) quantity [including "Total Et from ECAL only" ($E_{T\text{TEM}}$) and "minimum bias HF+ threshold 0" bits]:

31	28	27	24	23	12	11	0
<i>MBT0HFP</i>	<i>spare</i>		E_T [$E_{T\text{TEM}}$]		E_T [E_T]		

The data structure of "Total calibrated Et in jets" (HT) quantity [including "towercount" and "minimum bias HF- threshold 0" bits]:

31	28	27	25	24	12	11	0
<i>MBT0HFM</i>	<i>spare</i>		<i>TOWERCOUNT</i>		E_T		

The data structure of "Missing Et" (ET_{miss}) quantity [including "Asymmetry" ASYMET and "minimum bias HF+ threshold 1" bits]:

31	28	27	20	19	12	11	0
<i>MBT1HFP</i>		<i>ASYMET</i>		φ		E_T	

4 Global Trigger Logic

The data structure of "Missing Ht" (HT_{miss}) quantity [including "Asymmetry" ASYMHT and "minimum bias HF- threshold 1" bits]:

31	28 27	20 19	12 11	0
$MBT1HF$	$ASYMHT$	φ	E_T	

The data structure of "Missing Et including HF" (ET_{miss}^{HF}) quantity [including "Asymmetry" ASYMETHF and "Centrality" bits (3:0)]:

31	28 27	20 19	12 11	0
$[CENT3:0]$	$ASYMETHF$	φ	E_T	

The data structure of "Missing Ht including HF" (HT_{miss}^{HF}) quantity [including "Asymmetry" ASYMHTHF and "Centrality" bits (7:4)]:

31	28 27	20 19	12 11	0
$CENT[7:4]$	$ASYMHTHF$	φ	E_T	

4.2.2 Global Muon Trigger optical interface

The data structure of a muon object (64 bits):

Remark: "extrapol." means extrapolated - "qual" means quality bits - "iso" means isolation bits - "ch" means charge bits (bit 34 = charge sign, bit 35 = charge valid) - "m" means muon shower bit (on MU0 [MUS0], MU2 [MUS1], MU3 [MUS2 (two loose muon shower)], MU4 [MUSOOT0] and MU6 [MUSOOT1]; spare on MU1, MU5 and MU7) - "imp" = impact parameter.

63	62	61	60	53	52	43	42	36	35	34	33	32
<i>imp</i>	<i>m</i>			<i>unconst.pt</i>		φ (<i>out</i>)		<i>index bits</i>	<i>ch</i>	<i>iso</i>		
31				23	22	19	18	10	9			0
				η (<i>extrapol.</i>)	<i>qual</i>		p_T			φ (<i>extrapol.</i>)		

Remark: "extrapol." means extrapolated - "qual" means quality bits - "iso" means isolation bits - "ch" means charge bits (bit 34 = charge sign, bit 35 = charge valid) - "m" means muon shower bit (on MU0 [MUS0], MU2 [MUS1], MU4 [MUSOOT0] and MU6 [MUSOOT1]; spare on MU1, MU3, MU5 and MU7) - "imp" = impact parameter.

4.2.3 Calo-Layer1 optical interface

The optical link from Calo-Layer1 provides calo anomaly algorithm (CICADA) data.
Calo-Layer1 sends 6 frames in a 240MHz domain.

Anomaly Detection with an integer and a decimal part is provided.
(No Boosted Jets and no Heavy Ion bits are currently transferred !).

Overview (frame 0 ascending to 5):

31	28	27	0
AD	I	h	free
31	28	27	0
AD	I	l	free
31	28	27	0
AD	D	h	free
31	28	27	0
AD	D	l	free
31			0
			free
31			0
			free

Remark: "AD I" means Anomaly Detection Integer part, "AD D" means Anomaly Detection Decimal part, "l" means least significant bits,
"h" means most significant bits

4.3 Implementation in firmware

The firmware of μ GTL consists of two main parts:

- A top-of-hierarchy module '`gtl_module.vhd`', which contains the pipeline for $\pm 2\text{bx}$ data, the instantiations of calculators for differences in η and φ , the instantiations of conditions, the instantiations of charge correlation logic of muons and the Algorithms logic for 512 Algorithms, as well as a package file ('`gtl_pkg.vhd`') for declarations. Currently 6 AMC (MP7) boards are used to contain Algorithms.

A software tool called Trigger Menu Editor (TME) [5] is available to create a L1Menu with up to 512 Algorithms, which are partitioned by VHDL Producer [6] to the 6 MP7 boards.

The VHDL Producer creates VHDL snippets files (`algo_index.vhd`, `gtl_module_instances.vhd`, `gtl_module_signals.vhd`, `ugt_constants.vhd`) for a certain Trigger Menu.

These snippets are inserted into templates for `gtl_module.vhd` ('`gtl_module_tpl.vhd`'), `algo_mapping_rop.vhd` ('`algo_mapping_rop_tpl.vhd`') and `fdl_pkg.vhd` ('`fdl_pkg_tpl.vhd`') during simulation and synthesis (see Figure 9).

- A set of VHDL files exists for all the modules instantiated in top-of-hierarchy and the modules in the hierarchy. These files, called the "fixed part", are not influenced by VHDL Producer.

The latency of μ GTL is fixed to 5 bunch-crossings: two bunch-crossings for the pipeline of $\pm 2\text{bx}$ data, two bunch-crossings for conditions (fixed, for the conditions requested in the future, too), one bunch-crossing for the logic of Algorithms (see Figure 10).

4.3.1 Top-of-hierarchy module of μ GTL

The top-of-hierarchy module of μ GTL ('`gtl_module_tpl.vhd`') contains

- pipeline for $\pm 2\text{bx}$ data
- instantiations of charge correlation logic of muons (generated by VHDL Producer)
- instantiations of calculators for differences in η and φ (generated by VHDL Producer)
- instantiations of calculators for $\Delta\eta$ and $\Delta\varphi$ cuts (generated by VHDL Producer)
- instantiations of calculators for mass, ΔR and two-body pt cuts (generated by VHDL Producer)
- instantiations of conditions (generated by VHDL Producer)
- boolean logic for Algorithms (generated by VHDL Producer)

Listing 4 contains the entity declaration of the top-of-hierarchy module of μ GTL.

All the declarations for arrays ('type'), parameters ('constant') and look-up-tables ('constant') used in modules are available in '`gtl_pkg.vhd`' package-file.

4 Global Trigger Logic

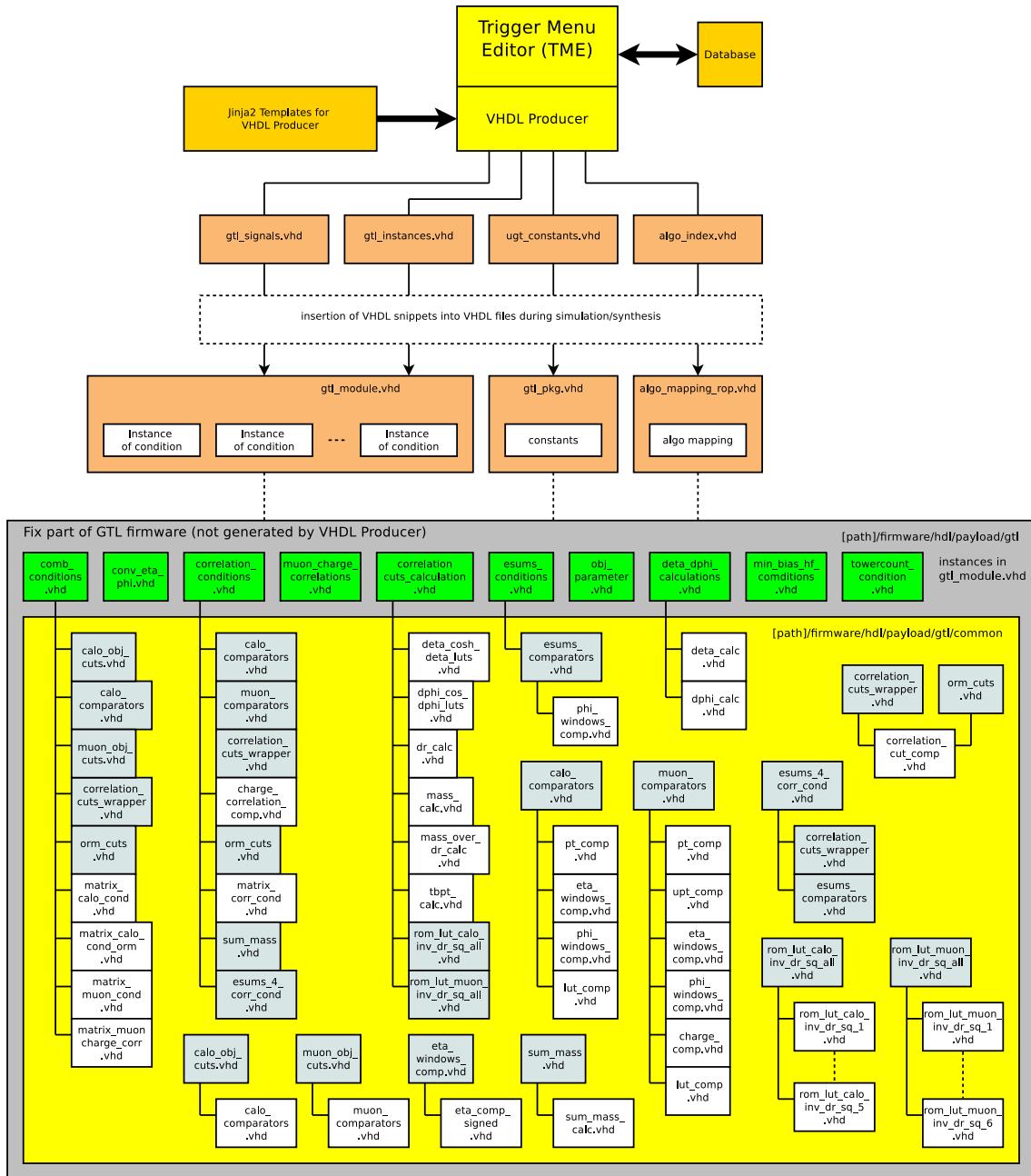


Figure 9: VHDL file generation by VHDL Producer

Table 9: Explanation of Listing 4

Item	Explanation
lhcb_clk	clock input (LHC clock).
gtl_data	input data ($\pm 2\text{bx}$ data).
algo_o	algorithms output.

Listing 4: Entity declaration of gtl_module_tpl.vhd

```
entity gtl_module is
  port(
    lhcb_clk : in std_logic;
    gtl_data : in gtl_data_record;
    algo_o : out std_logic_vector(NR_ALGOS-1 downto 0));
end gtl_module;
```

4.4 μ GTL structure

4.4.1 Data ± 2 bx

The μ GTL input data flow through a register pipeline of four stages. With those data it is possible to have conditions with objects from different bunch-crossings (within ± 2 bunch-crossings), electron/ γ for Correlation conditions.

See Figure 10 for a scheme of μ GTL pipeline structure. The data "data_p_1bx" and "data_p_2bx" occur 1 respectively 2 bunch-crossings after data for a certain bunch-crossing, therefore we got 2 bunch-crossings of latency from those data. The data "data_m_1bx" and "data_m_2bx" have no influence on latency, because coming before data for a certain bunch-crossing.

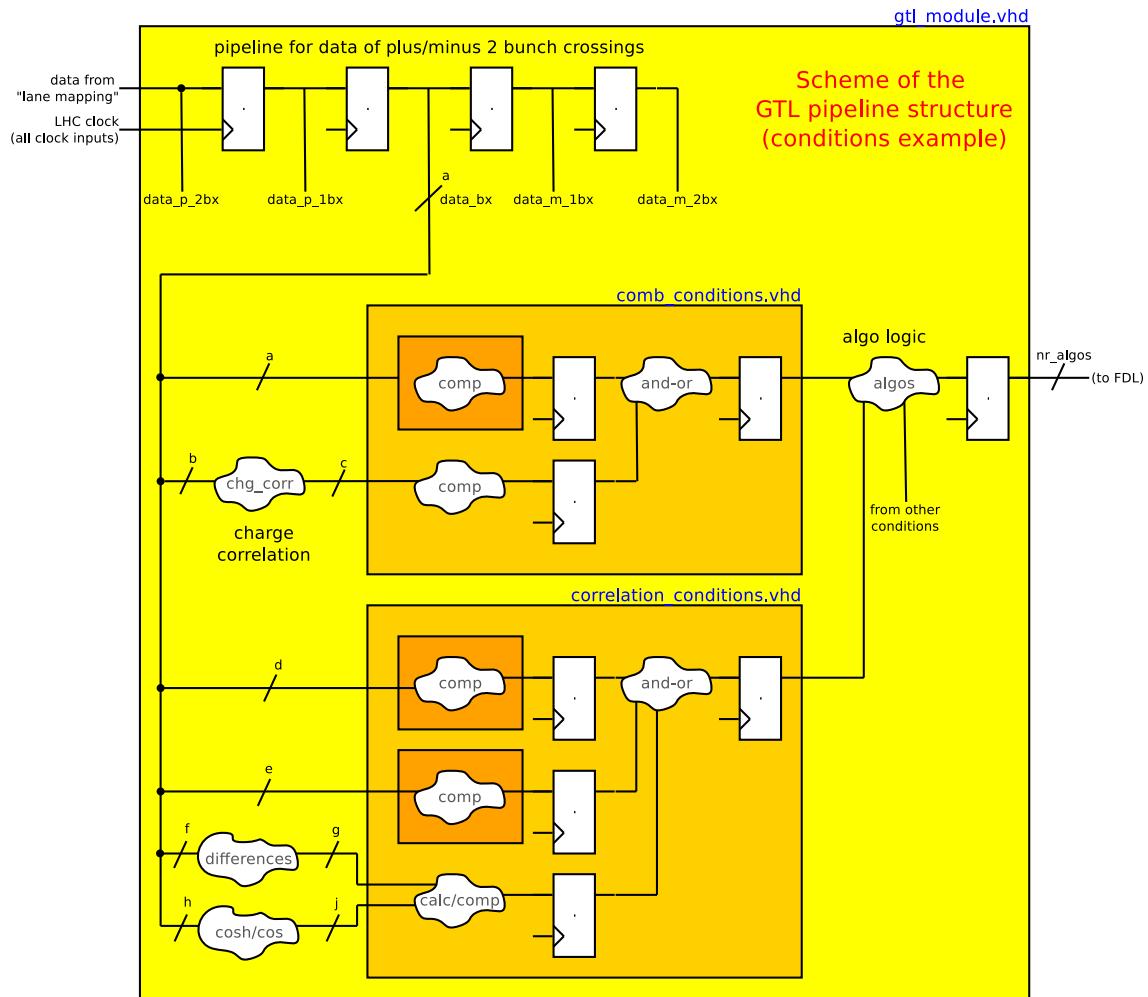


Figure 10: Scheme of μ GTL pipeline structure

4.4.2 Definitions of Calorimeter data

The calorimeter trigger processing identifies **electron/γ**, **jet** and **tau** objects and **energy sum quantities**.

See also [4.2](#).

Electron/γ:

Twelve objects are passed to the μ GT for each event.

For each selected object, the Calo-Layer2 sends parameters for p_T and for position and isolation - encoded in 32 bits:

- 9 bits p_T , range = 0..255 GeV (HW index = 0..0x1FF), step = 0.5, the highest bin will mark an overflow (HW index 0x1FF): meaning has to be defined
- 8 (7+1 sign) bits pseudo-rapidity (η) position, range = -5.0 to 5.0, step = 0.087/2, linear scale, 230 bins (HW index = 0x8D..0x72)
- 8 bits azimuth angle (φ) position, range = 2π , step $\approx 2\pi/144 (\hat{=} 2.5^\circ)$, 144 bins (HW index = 0..0x8F), HW index starting at 0° (anti-clockwise)
- 2 bits isolation
- 5 bits spare

Jet:

Twelve objects are passed to the μ GT for each event.

For each selected object, the Calo-Layer2 sends parameters: p_T , for position information, a DISP bit and quality information - encoded in 32 bits:

- 11 bits p_T , range = 0..1023 GeV (HW index = 0..0x7FF), step = 0.5, the highest bin will mark an overflow (HW index 0x7FF): meaning has to be defined
- 8 (7+1 sign) bits pseudo-rapidity (η) position, range = -5.0 to 5.0, step = 0.087/2, linear scale, 230 bins (HW index = 0x8D..0x72)
- 8 bits azimuth angle (φ) position, range = 2π , step $\approx 2\pi/144 (\hat{=} 2.5^\circ)$, 144 bins (HW index = 0..0x8F), HW index starting at 0° (anti-clockwise)
- 1 DISP bit (will be used to flag a jet as delayed / displaced based on HCAL timing and depth profiles that are indicative of a "long lived particle" (LLP) decay. If this bit is set to 1, then the jet has been tagged as a LLP jet.)
- 2 bits for "quality flags" - currently not used.
- 2 bits spare

Tau:

Twelve objects are passed to the μ GT for each event.

For each selected object, the Calo-Layer2 sends parameters for p_T and for position information and isolation - encoded in 32 bits:

- 9 bits p_T , range = 0..255 GeV (HW index = 0..0x1FF), step = 0.5, the highest bin will mark an overflow (HW index 0x1FF): meaning has to be defined
- 8 (7+1 sign) bits pseudo-rapidity (η) position, range = -5.0 to 5.0, step = 0.087/2, linear scale, 230 bins (HW index = 0x8D..0x72)
- 8 bits azimuth angle (φ) position, range = 2π , step $\approx 2\pi/144 (\approx 2.5^\circ)$, 144 bins (HW index = 0..0x8F), HW index starting at 0° (anti-clockwise)
- 2 bits isolation
- 5 bits spare

The representation of the 8 bits (called "hardware index [HW index]") in η is expected as Two's Complement notation as shown below.

Table 10: η scale of calorimeter objects

HW index	η range	η bin
0x72	114*0.087/2 to 115*0.087/2	114
...
0x01	0.087/2 to 2*0.087/2	1
0x00	0 to 0.087/2	0
0xFF	0 to -0.087/2	-1
0xFE	-0.087/2 to -2*0.087/2	-2
...
0x8D	-114*0.087/2 to -115*0.087/2	-115

The representation of the 8 bits in φ is expected as shown in Table 11.

Table 11: φ scale of calorimeter objects

HW index	φ range	φ range [degrees]	φ bin
0x00	0 to $2\pi/144$	0 to 2.5	0
0x01	$2\pi/144$ to $2*2\pi/144$	2.5 to 5.0	1
...
0x8F	$143*2\pi/144$ to 2π	357.5 to 360	143

The representation of the two bits for isolation (e/ γ and tau) is expected as shown in Table 12.

Table 12: Definition of e/γ and tau isolation bits

bits [26..25]	definition
00	not isolated
01	isolated
10	TBD
11	TBD

4.4.3 Definitions of Energy sum quantities data

See [4.2](#) for data structure.

Energy sum quantities consist of following quantities (for naming convention see [8](#)):

- ET
- HT
- ET_{miss}
- HT_{miss}
- ETTEM
- ET_{miss}^{HF}
- HT_{miss}^{HF}
- ASYMET
- ASYMHT
- ASYMETHF
- ASYMHTHF
- CENT[0..7]

Calo-Layer2 sends 6 frames (each 32 bits) with Energy sum quantities containing the following information:

- E_T , 12 bits, range = 0..2047 GeV (HW index = 0..0xFFFF), step = 0.5, the highest bin will mark an overflow (HW index 0xFFFF): meaning has to be defined
- azimuth angle (φ) position, 8 bits, range = 2π , step $\approx 2\pi/144$ ($\hat{=} 2.5^\circ$), 144 bins (HW index = 0..0x8F), HW index starting at 0° (anti-clockwise)
- "Towercount", 13 bits, range = 0..8191
- "Minimum bias", 4 bits, range = 0..15
- "Asymmetry", 8 bits, range = 0..255 (used 0..100)
- "Centrality", 8 single bits, used as signals

Frame 0: The data structure of "Total Et" (ET) quantity [including "Total Et from ECAL only" (ETTEM) and "minimum bias HF+ threshold 0" bits].

Frame 1: The data structure of "Total calibrated Et in jets" (HT) quantity [including "towercount" and "minimum bias HF- threshold 0" bits].

Frame 2: The data structure of "Missing Et" (ET_{miss}) quantity [including "Asymmetry" ASYMET and "minimum bias HF+ threshold 1" bits].

Frame 3: The data structure of "Missing Ht" (HT_{miss}) quantity [including "Asymmetry" ASYMHT and "minimum bias HF- threshold 1" bits].

Frame 4: The data structure of "Missing Et including HF" (ET_{miss}^{HF}) quantity [including "Asymmetry" ASYMETHF and "Centrality" bits (3:0)].

Frame 5: The data structure of "Missing Ht including HF" (HT_{miss}^{HF}) quantity [including "Asymmetry" ASYMHTHF and "Centrality" bits (7:4)].

4.4.4 Definitions of Muon data

Eight Muon objects are provided by Global Muon Trigger. One Muon object has a 64 bits data structure with parameters for p_T , for unconstrained p_T , for impact parameter, for position, charge, quality and isolation information (see also [4.2.2](#)):

- 10 bits azimuth angle (φ) position, range = 2π , step $\approx 2\pi/576$ ($\approx 0.625^\circ$), 576 bins (HW index = 0..0x23F), HW index starting at 0° (anti-clockwise)
- 9 bits p_T , range = 0..255 GeV (HW index = 0..0x1FF), step = 0.5, the highest bin will mark an overflow (HW index 0x1FF): meaning has to be defined
- 4 bits quality, 16 types for quality (meaning not defined yet!)
- 9 (8+1 sign) bits pseudo-rapidity (η) position, range = -2.45 to 2.45, step = 0.087/8, linear scale, 451 bins (-225..225, HW index = 0x11F..0x0E1)
- 2 bits isolation, 4 types for isolation (meaning not defined yet!)
- 1 bit charge sign, charge sign = '0' means "positive" charge, charge sign = '1' means "negative" charge
- 1 bit charge valid (= '1' means "valid")
- 7 index bits
- 10 bits azimuth angle (φ) position, raw data
- 8 bits unconstrained p_T , range = 0..255 GeV (HW index = 0..0xFF), step = 1.0, the highest bin will mark an overflow (HW index 0xFF)
- 1 hadronic (muon) shower bit
- 2 bits impact parameter

The representation of the 9 bits (called "hardware index [HW index]"') in η is expected as Two's Complement notation as shown in Table [13](#).

The central value of the bin 0 ($-0.010875/2$ to $+0.010875/2$) = 0.0, the left edge of the bins will range from $-255 \times 0.010875 - 0.010875/2 = -2.7785625$ to $+255 \times 0.010875 - 0.010875/2 = 2.7676875$. The central value of the bins will range between ± 2.773125 . The physical η range of the muon detectors is about ± 2.45 , so that not all possible η bins will be used.

The 7 index bits cover a range from 0 to 107 (e.g. index 0-17 is EMTF+ and index 90-107 is EMTF-).

The representation of the 10 bits in φ is expected as shown in Table [14](#).

The representation of the four bits for quality is expected as shown in Table [15](#).

Table 13: η scale of muon objects

HW index	η range	η bin
0x0E1	224.5*0.087/8 to 225.5*0.087/8	225
0x0E0	223.5*0.087/8 to 224.5*0.087/8	224
...
0x001	0.5*0.087/8 to 1.5*0.087/8	1
0x000	0.5*-0.087/8 to 0.5*0.087/8	0
0x1FF	0.5*-0.087/8 to 1.5*-0.087/8	-1
0x1FE	1.5*-0.087/8 to -2.5*0.087/8	-2
...
0x11F	-224.5*0.087/8 to -225.5*0.087/8	-225

Table 14: φ scale of muon objects

HW index	φ range	φ range [degrees]	φ bin
0x000	0 to $2\pi/576$	0 to 0.625	0
0x001	$2\pi/576$ to $2*2\pi/576$	0.625 to 1.250	1
...
0x23F	$575*2\pi/576$ to 2π	359.375 to 360	575

Table 15: Definition of muon quality bits

bits [22..19]	definition
0000	quality "level 0"
0001	quality "level 1"
...	...
1110	quality "level 14"
1111	quality "level 15"

The representation of the two bits for isolation is expected as shown in Table 16.

Table 16: Definition of muon isolation bits

bits [33..32]	definition
00	not isolated
01	isolated
10	TBD
11	TBD

The representation of the two bits for charge is expected as shown in Table 17.

Table 17: Definition of muon charge bits

bits [35..34]	definition
00	not valid charge
01	not valid charge
10	positive charge
11	negative charge

Muon shower bits definition is shown in Table 18.

Table 18: Definition of hadronic (muon) shower bits on bit 61 of muon objects

object	definition
0	MUS0
2	MUS1
3	MUS2 (two loose muon shower)
4	MUSOOT0
6	MUSOOT1

The representation of the two bits for impact parameter is expected as shown in Table 19.

Table 19: Definition of muon impact parameter bits

bits [63..62]	definition
00	TBD
01	TBD
10	TBD
11	TBD

4.4.5 Definitions of CICADA data

The calorimeter layer 1 trigger processing identifies **Anomaly Detection**.

See also [4.2.3](#).

The value for Anomaly Detection (of CICADA) is passed to the μ GT for each event.

The Anomaly Detection value (of CICADA) is represented by an 8 bits integer part and an 8 bits decimal part, which are combined to a 16 bits word for comparison with requested threshold ("cscore").

4.4.6 Calculation of object cuts

List of object cuts:

- p_T
- η
- index bits
- φ
- isolation
- DISP (displaced = "long lived particle" jet)
- charge
- quality
- unconstrained p_T
- impact parameter

4.4.6.1 Object cuts

The comparisons for objects cuts are done by:

A comparator between the energy (p_T) and a threshold (pt_threshold) with 'mode-selection'. Similar for unconstrained p_T .

The comparison in η is done with five "window"-comparators, so one gets max. five ranges for η . The η value (HW index) has a Two's Complement notation, the comparisons is done signed. Number of windows is given for η .

The comparison with index bits is done similar to η with five "window"-comparators. The index bits value (HW index) is in the range from 0 to 107. Number of windows is given for index bits.

The comparison in φ is done with two "window"-comparators, so one gets two ranges for φ . The comparisons is done unsigned. Number of windows is given for φ .

There are two cases how the limits of one "window"-comparator could be set (see also Figure 11):

- Upper limit is less than lower limit $\Rightarrow \varphi$ range between the limits, including the φ bin with value = 0 (HW index).
- Upper limit is greater/equal than lower limit $\Rightarrow \varphi$ range between the limits, not including the φ bin with value = 0 (HW index).

```
phi_comp_w1 <= '1' when phi_w1_upper_limit < phi_w1_lower_limit and  
    (phi <= phi_w1_upper_limit or phi >= phi_w1_lower_limit) else  
    '1' when phi_w1_upper_limit >= phi_w1_lower_limit and  
    (phi <= phi_w1_upper_limit and phi >= phi_w1_lower_limit)  
    else '0';
```

Only one of the required ranges ("windows") must be fulfilled by η and φ values ("or").

The comparisons for isolation, quality and impact parameter are done with LUTs.
 The comparison for charge is done with requested charge.
 If DISP bit is set to 1, then the jet has been tagged as a "long lived particle" (LLP) jet. A one bit requirement is given for DISP for comparison.

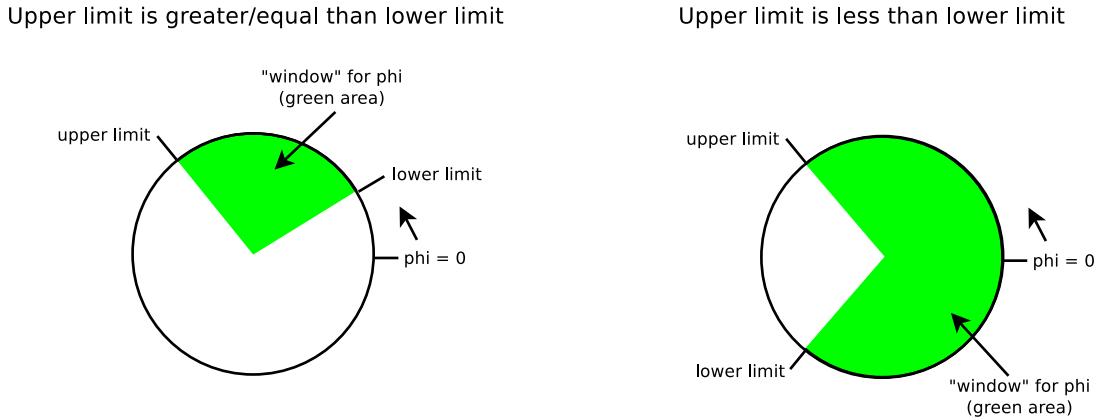


Figure 11: Setting the limits for "window"-comparators for φ

The comparison of isolation (for electron/ γ , tau and muon) is done with a LUT (Table 20). [To ignore quality comparison, all bits in the LUT have to be '1'.]

The comparison of impact parameter is done with LUT (Table 21). [To ignore quality comparison, all bits in the LUT have to be '1'.]

The comparison of quality is done with LUT (Table 22). [To ignore quality comparison, all bits in the LUT have to be '1'.]

Charge valid and charge sign bits must be equal to the requested charge.

Table 20: LUT contents for isolation comparison

LUT content (4 bits)	isolation (2 bits)	trigger
X"0"	xx	no trigger
X"1"	00	trigger on isolation bits = 00
X"2"	01	trigger on isolation bits = 01
X"3"	00 or 01	trigger on isolation bits = 00 or 01
X"4"	10	trigger on isolation bits = 10
X"5"	00 or 10	trigger on isolation bits = 00 or 10
X"6"	01 or 10	trigger on isolation bits = 01 or 10
X"7"	00 or 01 or 10	trigger on isolation bits = 00 or 01 or 10
X"8"	11	trigger on isolation bits = 11
X"9"	00 or 11	trigger on isolation bits = 00 or 11
X"A"	01 or 11	trigger on isolation bits = 01 or 11
X"B"	00 or 01 or 11	trigger on isolation bits = 00 or 01 or 11
X"C"	10 or 11	trigger on isolation bits = 10 or 11
X"D"	00 or 10 or 11	trigger on isolation bits = 00 or 10 or 11
X"E"	01 or 10 or 11	trigger on isolation bits = 01 or 10 or 11
X"F"	00 or 01 or 10 or 11	trigger on isolation bits = 00 or 01 or 10 or 11 (= "ignore" isolation)

Table 21: LUT contents for impact parameter comparison

LUT content (4 bits)	impact parameter (2 bits)	trigger
X"0"	xx	no trigger
X"1"	00	trigger on impact parameter bits = 00
X"2"	01	trigger on impact parameter bits = 01
X"3"	00 or 01	trigger on impact parameter bits = 00 or 01
X"4"	10	trigger on impact parameter bits = 10
X"5"	00 or 10	trigger on impact parameter bits = 00 or 10
X"6"	01 or 10	trigger on impact parameter bits = 01 or 10
X"7"	00 or 01 or 10	trigger on impact parameter bits = 00 or 01 or 10
X"8"	11	trigger on impact parameter bits = 11
X"9"	00 or 11	trigger on impact parameter bits = 00 or 11
X"A"	01 or 11	trigger on impact parameter bits = 01 or 11
X"B"	00 or 01 or 11	trigger on impact parameter bits = 00 or 01 or 11
X"C"	10 or 11	trigger on impact parameter bits = 10 or 11
X"D"	00 or 10 or 11	trigger on impact parameter bits = 00 or 10 or 11
X"E"	01 or 10 or 11	trigger on impact parameter bits = 01 or 10 or 11
X"F"	00 or 01 or 10 or 11	trigger on impact parameter bits = 00 or 01 or 10 or 11 (= "ignore" impact parameter)

Table 22: LUT contents for quality comparison of muon objects

LUT content (16 bits)	quality bits (4 bits)	trigger
X"0000"	xxxx	no trigger
X"0001"	0000	trigger on quality "level 0"
X"0002"	0001	trigger on quality "level 1"
X"0003"	0001 or 0000	trigger on quality "level 1" or "level 0"
X"0004"	0010	trigger on quality "level 2"
...
X"8000"	1111	trigger on quality "level 15"
X"C000"	1111 or 1110	trigger on quality "level 15" or "level 14"
...
X"FFFF"	xx	trigger on all quality "levels" (= "ignore")

4.4.7 Calculation of correlation cuts

The following cuts are used for two objects correlations:

- $\Delta\eta$ (DETA).
- $\Delta\varphi$ (DPHI).
- ΔR (DR).
- charge correlation (only for muon).
- Cuts for mass (MASS) of following mass types:
 - Invariant mass.
 - Invariant mass with unconstrained pt (for muons only).
 - Invariant mass over ΔR .
 - Transverse mass.
- Two-body pt.

There is one mass cut for correlations with three objects:

- Invariant mass for three objects (MASS).

The generation of look-up-tables (LUTs) for calculations of correlation cuts is described in chapter "Calculation of look-up-tables (LUTs) for correlation cuts" (see [4.4.8](#)).

4.4.7.1 Calculation of $\Delta\eta$

The calculation of $\Delta\eta$ of two objects is done with formula:

$$\Delta\eta = \text{abs}(\eta_1 - \eta_2)$$

where η_1 and η_2 are represented in signed hardware indices.

4.4.7.2 Calculation of $\Delta\varphi$

The calculation of $\Delta\varphi$ of two objects is done with formula:

$$\Delta\varphi = \text{abs}(\varphi_1 - \varphi_2) \text{ with } (" \varphi \text{ full bin range} " - \Delta\varphi) \text{ when } (\Delta\varphi > " \varphi \text{ half bin range} ").$$

where φ_1 and φ_2 are represented in unsigned hardware indices.

4.4.7.3 ΔR calculation

The calculation of ΔR of two objects is done with formula:

$$\Delta R = \sqrt{(\eta_1 - \eta_2)^2 + (\varphi_1 - \varphi_2)^2}.$$

The calculation of ΔR^2 in VHDL (no square root in VHDL) is done by adding the square of $\Delta\eta$ and $\Delta\varphi$ LUT values.

4.4.7.4 Invariant mass calculation

The calculation of *invariant mass of two objects* is done with formula:

$$M = \sqrt{2pt_1pt_2(\cosh(\eta_1 - \eta_2) - \cos(\varphi_1 - \varphi_2))}.$$

The calculation of $\frac{M^2}{2}$ in VHDL (no square root in VHDL) is done by multiplying LUT values of pt1, pt2 and the difference of $\cosh(\Delta\eta)$ and $\cos(\Delta\varphi)$.

4.4.7.5 Transverse mass calculation

The calculation of *transverse mass of two objects* is done with formula:

$$M = \sqrt{2pt_1pt_2(1 - \cos(\varphi_1 - \varphi_2))}.$$

Calculation similar to "Invariant mass calculation".

4.4.7.6 Invariant mass over ΔR calculation

The formulas for *invariant mass over ΔR of two objects* are:

$$M = \sqrt{2pt_1pt_2(\cosh(\eta_1 - \eta_2) - \cos(\varphi_1 - \varphi_2))}.$$

$$\Delta R = \sqrt{(\eta_1 - \eta_2)^2 + (\varphi_1 - \varphi_2)^2}.$$

The calculation of *invariant mass over ΔR of two objects* is done with $\frac{M^2}{2} \times (1/\Delta R^2)$ (no square root in VHDL).

A direct calculation of $1/\Delta R^2$ is not possible in firmware (VHDL code), therefore the implementation of the calculation is done by LUTs. In the hardware the values of these LUTs are stored in "large" ROMs, which was realized using the Block RAMs (BRAMs) of the Virtex chip.

Due the limited number of available BRAMs there are some restrictions for creating algorithms with *invariant mass over ΔR* :

- Objects must have the same type (e.g.: "muon muon", "eg eg", ...)
- Objects must be of same bx
- Resolution of $\Delta\eta$ and $\Delta\varphi$:
 - Full resolution for calos (max. eta bins=230, max. dphi bins=72)
 - Half resolution only for muons (max. eta bins=226, max. dphi bins=144)
- If $1/\Delta R^2=0$ ($\Delta\eta=0$ and $\Delta\varphi=0$) then correlation cut *invariant mass over ΔR* is true
- The values of LUTs are only valid for current definitions and restrictions. Every change might cause a recalculation of the values and a regeneration of IPs (representing LUTs in BRAMs) in Vivado (firmware generation tool)

The values of LUTs in firmware are listed in coe files of ROMs (created by same scripts mentioned above), currently 5 ROMs for "calo calo" and 6 ROMs for "muon muon" (see

'lut_calor_inv_dr_sq_rom1.coe', etc. and 'lut_muon_inv_dr_sq_rom1.coe', etc.). The addresses of the BRAMs are given by $\Delta\eta$ and $\Delta\varphi$. All ROMs for calos have 4096 addresses, for muons 8192 addresses. The data width of ROMs is different depending on the highest LUT value in ROM. Because of these different data widths, the partitioning of several ROMs was done to save BRAM resources. Currently 873 BRAMs (36kb) are available per Virtex chip. Following numbers of BRAMs (36kb) are needed for:

- "calo calo": 660
- "muon muon": 672

Currently one calculation of *invariant mass over ΔR* of "calo calo" or "muon muon" is possible in one Virtex chip, but one can have some algorithms containing *invariant mass over ΔR* with different thresholds, but with same objects and same bx. A description of calculation of $1/\Delta R^2$ with python scripts one can find in '[scripts/.../README.md](#)'.

4.4.7.7 Invariant mass calculation for three objects

The calculation of *invariant mass calculation for three objects* is done by calculating the invariant mass for all two-object combinations and take the sum of the three invariant masses of the two-object combinations.

4.4.7.8 Two-body pt calculation

The calculation of *two-body pt* is done with formula:

$$pt = \sqrt{pt_1^2 + pt_2^2 + 2pt_1pt_2(\cos(\varphi_1)\cos(\varphi_2) + \sin(\varphi_1)\sin(\varphi_2))}$$

The calculation of pt^2 in VHDL (no square root in VHDL) is using LUTs for pt_1 , pt_2 , $\cos(\varphi)$ and $\sin(\varphi)$.

4.4.7.9 Muon charge correlation

For definition of muon charge, see [4.4.4](#).

In the muon charge correlation module (['muon_charge_correlations.vhd'](#)), the charge correlations are made for different muon conditions types. The module is instantiated in the top-of-hierarchy module (['gt1_module.vhd'](#)) and not inside of a muon conditions module. The charges of objects (number of objects depends on muon condition type) are compared to get "like sign charge" ("LS") or "opposite sign charge" ("OS"), "LS" means that the charges (charge sign) of objects are the same, "OS" means that at least one object has different charge than the others. This information is used in all instantiated muon conditions. There is no charge correlation for single type conditions.

In all cases the "charge valid" bit of the objects must be set.

In TME [5] one can select "LS", "OS" or ignore for charge correlation in muon conditions.

Table 23: Muon charge correlation - Double Muon

x x	I ignore (charge x = +, -, I)
+	LS both positive muons
- -	LS both negative muons
+ -	OS two muons of opposite sign (a pair)
- +	OS two muons of opposite sign (a pair)

Table 24: Muon charge correlation - Triple Muon

x x x	I ignore (charge x = +, -, I)
+	LS three muons of positive charge
- - -	LS three muons of negative charge
- + +	OS a pair plus a positive muon
+ - +	OS a pair plus a positive muon
+ + -	OS a pair plus a positive muon
+ - -	OS a pair plus a negative muon
- + -	OS a pair plus a negative muon
- - +	OS a pair plus a negative muon

Table 25: Muon charge correlation - Quad Muon

x x x x	I ignore (charge x = +, -, I)
+	LS four muons of positive charge
- - - -	LS four muons of negative charge
- + + +	OS a pair plus two positive muons
+ - + +	OS a pair plus two positive muons
+ + - +	OS a pair plus two positive muons
+ + + -	OS a pair plus two positive muons
+ + - -	OS two pairs
+ - + -	OS two pairs
+ - - +	OS two pairs
- - + +	OS two pairs
- + - +	OS two pairs
- + + -	OS two pairs
+ - - -	OS a pair plus two negative muons
- + - -	OS a pair plus two negative muons
- - + -	OS a pair plus two negative muons
- - - +	OS a pair plus two negative muons

4.4.8 Calculation of look-up-tables (LUTs) for correlation cuts

LUTs are defined as a VHDL "constant" in '`gtl_pkg.vhd`' (VHDL package file). The values of precision and step size are given by "scale_set" in XML file of a L1 menu.

Overview of precision types for correlation cuts (an example for electron/ γ electron/ γ correlation):

- *EG-EG-Delta* relevant for DeltaEta and DeltaPhi LUTs
- *EG-EG-MassPt* relevant for pt and unconstrained pt LUTs (used in mass and two-body pt calculations)
- *EG-EG-Math* relevant for $\cos(\Delta\phi)$ and $\cosh(\Delta\eta)$ LUTs (used in mass calculations)
- *EG-EG-InverseDeltaRMath* relevant for $1/\Delta R$ LUTs (used in mass over deltaR calculations)
- *EG-EG-TwoBodyPtMath* relevant for $\cos(\Phi)$ and $\sin(\Phi)$ LUTs (used in two-body pt calculations)
- *EG-EG-DeltaOverlapRemoval* is obsolete, used EG-EG-Delta (same scales for η and φ)
- *EG-EG-Mass* currently not used
- *EG-EG-TwoBodyPt* is obsolete, used EG-EG-MassPt

Overview of precision names (example for "MassPt"):

EG-EG-MassPt
EG-JET-MassPt
EG-TAU-MassPt
JET-JET-MassPt
JET-TAU-MassPt
EG-ETM-MassPt
JET-ETM-MassPt
TAU-ETM-MassPt
EG-HTM-MassPt
JET-HTM-MassPt
TAU-HTM-MassPt
EG-ETMHF-MassPt
JET-ETMHF-MassPt
TAU-ETMHF-MassPt
EG-MU-MassPt
JET-MU-MassPt
TAU-MU-MassPt
MU-MU-MassPt
MU-ETM-MassPt
MU-HTM-MassPt
MU-ETMHF-MassPt

4.4.8.1 LUTs for p_T and unconstrained p_T used in mass and two-body p_T calculations

The values of p_T or unconstrained p_T LUT are calculated by building the half difference of maximum and minimum value of a bin, adding minimum value, rounding at precision position after decimal point and multiplying with $10^{\text{precision}}$ to get integer values.

The address input of the LUT for p_T or unconstrained p_T is the value of hardware index of p_T or unconstrained p_T .

The precision values in XML file are given by (an example for electron/ γ electron/ γ correlation):

```
<scale>
<object>PRECISION</object>
<type>EG-EG-MassPt</type>
...
<n_bits>1</n_bits>
</scale>
```

VHDL names of p_T and unconstrained p_T LUTs:

```
EG_PT_LUT (used also for tau)
JET_PT_LUT
ETM_PT_LUT (used also for  $HT_{\text{miss}}$  and  $ET_{\text{miss}}^{HF}$ )
MU_PT_LUT
MU_UPT_LUT
```

4.4.8.2 LUTs for delta eta

The values of the LUT for $\Delta\eta$ are calculated by multiplying $\Delta\eta$ in hardware indices with η step size, rounding at precision position after decimal point and multiplying the result with $10^{\text{precision}}$ to get integer values.

The address of the LUT is the value of $\Delta\eta$ in hardware indices.

The precision value in XML file is given by (an example for electron/ γ electron/ γ correlation):

```
<scale>
<object>PRECISION</object>
<type>EG-EG-Delta</type>
...
<n_bits>3</n_bits>
</scale>
```

where $<\text{n_bits}>$ is the precision value and $<\text{type}>$ represents a precision name.

The η ($=\Delta\eta$) step size in XML file is given by (an example for electron/ γ):

```
<scale>
<object>EG</object>
<type>ETA</type>
...

```

```
<step>+4.34999999999997E-02</step>
...
</scale>
```

VHDL names of $\Delta\eta$ LUTs:

```
CALO_CALO_DIFF_ETA_LUT
CALO_MU_DIFF_ETA_LUT
MU_MU_DIFF_ETA_LUT
```

4.4.8.3 LUTs for delta phi

The values of the LUT for $\Delta\varphi$ are calculated by multiplying $\Delta\varphi$ in hardware indices with φ step size, rounding at precision position after decimal point and multiplying the result with $10^{\text{precision}}$ to get integer values.

The address of the LUT is the value of $\Delta\varphi$ in hardware indices.

The precision values of $\Delta\varphi$ are identical with $\Delta\eta$.

The φ ($=\Delta\varphi$) step size in XML file is given by (an example for electron/ γ):

```
<object>EG</object>
<type>PHI</type>
...
<step>+4.3633231299858237E-02</step>
...
</scale>
```

VHDL names of $\Delta\varphi$ LUTs:

```
CALO_CALO_DIFF_PHI_LUT
CALO_MU_DIFF_PHI_LUT
MU_MU_DIFF_PHI_LUT
```

4.4.8.4 LUTs for $\cosh(\Delta\eta)$ used in mass calculations

The values in the LUT for $\cosh(\Delta\eta)$ are calculated by multiplying $\Delta\eta$ in hardware indices with η step size, calculating cosine hyperbolic, rounding at "Math" precision position after decimal point and multiplying the result with $10^{\text{precision}}$ to get integer values.

The address of the LUT for $\cosh(\Delta\eta)$ is the value of $\Delta\eta$ in hardware indices.

For calo muon correlations one has to use the muon step size.

The precision values in XML file are given by (an example for electron/ γ electron/ γ correlation):

```
<scale>
<object>PRECISION</object>
<type>EG-EG-Math</type>
```

```
...
<n_bits>3</n_bits>
</scale>
used for cosh( $\Delta\eta$ ) and cos( $\Delta\varphi$ ).
```

VHDL names of cosh($\Delta\eta$) LUTs:

```
CALO_CALO_COSH_DETA_LUT
CALO_MUON_COSH_DETA_LUT
MU_MU_COSH_DETA_LUT
```

4.4.8.5 LUTs for cos(delta phi) used in mass calculations

The values in the LUT for cos($\Delta\varphi$) are calculated by multiplying $\Delta\varphi$ in hardware indices with φ step size, calculating cosine, rounding at "Math" precision position after decimal point and multiplying the result with $10^{\text{precision}}$ to get integer values.

The address of the LUT for cos($\Delta\varphi$) is the value of $\Delta\varphi$ in hardware indices. For calo muon correlations one has to use the muon step size.

VHDL names of cos($\Delta\varphi$) LUTs:

```
CALO_CALO_COS_DPHI_LUT
CALO_MUON_COS_DPHI_LUT
MU_MU_COS_DPHI_LUT
```

4.4.8.6 LUTs for 1/deltaR**2 used in mass over deltaR calculations

The calculation of $1/\Delta R^2$ is done by multiplying $\Delta\eta$ in hardware indices with η step size, making the square, doing the same for $\Delta\varphi$, adding the squares, inverting the sum, rounding at "InverseDeltaRMath" precision position after decimal point and multiplying the result with $10^{\text{precision}}$ to get integer values. The address of the two-dimensional LUT for $1/\Delta R^2$ consists of values of $\Delta\eta$ and $\Delta\varphi$ in hardware indices.

The precision values in XML file are given by (an example for electron/ γ electron/ γ correlation):

```
<scale>
<object>PRECISION</object>
<type>EG-EG-InverseDeltaRMath</type>
...
<n_bits>5</n_bits>
</scale>
```

Precision names for "InverseDeltaRMath":

```
EG-EG-InverseDeltaRMath
JET-JET-InverseDeltaRMath
TAU-TAU-InverseDeltaRMath
MU-MU-InverseDeltaRMath
```

The LUTs are located in BRAMs.

For calo-calо mass over deltaR 5 ROMs are needed to represent the LUT. The content of the LUT one can see in '[lut_calo_inv_dr_sq_rom1.coe](#)' (and so on).

For muon-muon mass over deltaR 6 ROMs are needed to represent the LUT. The content of the LUT one can see in '[lut_muon_inv_dr_sq_rom1.coe](#)' (and so on).

The access to a certain ROM depends on the values of $\Delta\eta$ and $\Delta\varphi$ (see '[description_rom_lut_calо_inv_dr_sq.txt](#)' and '[rom_lut_calо_inv_dr_sq_all.vhd](#)', respectively

'[description_rom_lut_muon_inv_dr_sq.txt](#)' and '[rom_lut_muon_inv_dr_sq_all.vhd](#)').

The calculation of values for LUTs is done by python script '[one_over_dr_sq_calc.py](#)'.

Calculated values one can see in '[emulator_lut_calо_one_over_dr_sq_calc.txt](#)' and '[emulator_lut_muon_one_over_dr_sq_calc.txt](#)'.

4.4.8.7 LUTs for $\cos(\varphi)$ used in two-body pt calculations

The values in the LUT for $\cos(\varphi)$ are calculated by building the half difference of maximum and minimum value of a φ bin, adding minimum value, calculating cosine, rounding at "Two-BodyPtMath" precision position after decimal point and multiplying the result with $10^{\text{precision}}$ to get integer values.

The precision values in XML file are given by (an example for electron/ γ electron/ γ correlation):

```
<scale>
<object>PRECISION</object>
<type>EG-EG-TwoBodyPtMath</type>
...
<n_bits>3</n_bits>
</scale>
```

used for $\cos(\varphi)$ and $\sin(\varphi)$.

VHDL names of $\cos(\varphi)$ LUTs:

```
CALO_COS_PHI_LUT
MUON_COS_PHI_LUT
```

4.4.8.8 LUTs for $\sin(\varphi)$ used in two-body pt cuts

The values in the LUT for $\sin(\varphi)$ are calculated by building the half difference of maximum and minimum value of a φ bin, adding minimum value, calculating sine, rounding at "Two-BodyPtMath" precision position after decimal point and multiplying the result with $10^{\text{precision}}$ to get integer values.

VHDL names of $\sin(\varphi)$ LUTs:

```
CALO_SIN_PHI_LUT
MUON_SIN_PHI_LUT
```

4.4.9 Combination conditions

4.4.9.1 Combination conditions definition

A condition consists of input data and a set of requirements, which contain the requirements to be complied. The requirements are called "object cuts".

The requirement list contains:

thresholds for p_T , ranges for η and φ , LUTs for isolation, LUTs for quality, requested charges, thresholds for unconstrained p_T , a LUT for impact parameter. The condition is complied, if every comparison between object parameters and requirements is valid for the following object cuts (only for requested cuts):

For Calorimeter input data:

- p_T greater-equal (or equal) threshold
- η in range
- φ in range
- iso LUT

For Muon input data:

- p_T greater-equal (or equal) threshold
- η in range
- φ in range
- iso LUT
- requested charge
- quality LUT
- unconstrained p_T greater-equal (or equal) threshold
- impact parameter LUT

There are different types of conditions implemented, depending of how many objects have to comply the requirements.

- "Quad objects requirements condition": this condition type consists of requirements for 4 different trigger objects of the same object type. For each object the requirements can be different. To fulfill this condition, there must exist at least one set of 4 different objects, each of which fulfills at least one of the requirements.
- "Triple objects requirements condition": this condition type consists of requirements for 3 different trigger objects of the same object type. For each object the requirements can be different. To fulfill this condition, there must exist at least one set of 3 different objects, each of which fulfills at least one of the requirements.

- "Double objects requirements condition": this condition type consists of requirements for 2 different trigger objects of the same object type. For each object the requirements can be different. To fulfill this condition, there must exist at least one set of 2 different objects, each of which fulfills at least one of the requirements.²
- "Single object requirement condition": this condition type consists of one requirement for one trigger object of a given object type. To fulfill this condition, there must exist at least one object which fulfills the requirement.

The values of the requirements are given by VHDL Producer for every Trigger Menu. The input data objects have to be of same type and same bunch-crossing.

With "Double objects requirements condition" a correlation cut of "two-body pt" can be required (calorimeter and muon objects).

Additionally charge correlation cuts with "Double objects requirements condition", "Triple objects requirements condition" and "Quad objects requirements condition" of muon objects can be required.

4.4.9.2 Calo combination conditions with more than 4 requirements

The possibility of a combination condition for more than 4 requirements (up to 12) is implemented, but there are some restrictions:

- only for calo objects (Electron/ γ , Jet and Tau)
- all requirements must have the same threshold and bx
- no cuts allowed for such conditions

Providing this type of conditions is based on the decreasing pt values of the calo objects. In VHDL producer the number of requirements and the common threshold is given to VHDL code. A pt comparision of the object given by the number of requirements with the threshold is made for a combination condition for more than 4 requirements.

²"Double objects requirements condition with spatial correlation" not used anymore, replaced by Correlation conditions

4.4.10 Energy sum quantities conditions

4.4.10.1 Energy sum quantities conditions module (including Asymmetry conditions)

A comparator between E_T and a threshold (et_threshold) and, depending on object type, a comparison in φ with two "window"-comparators is done in this module. The value for E_T threshold, the 'mode-selection' for the E_T comparator and the limits for the "window"-comparators are given in the generic interface list of the module. The selection whether a comparison in φ is part of the condition is done with the value of the generic parameter 'obj_type' ('ETM_TYPE', 'ETMHF_TYPE', 'HTM_TYPE' and 'HTMHF_TYPE' force a comparison). The comparison in φ is done in the same way as for calorimeter conditions. Additionally the data structure of input data (data_i in port interface list) is provided as a record in this list. The output signal of the module is in high state, if all comparisons are true.

Data for Asymmetry trigger are received on 4 frames on bits 27..20 (8 bits). For every type a comparision with an 8-bit threshold (greater-equal [or equal]) is done. Asymmetry data are interpreted as counts.

For the entity declaration of '[esums_conditions.vhd](#)', see Listing 5.

Table 26: Explanation of Listing 5

Item	Explanation
et_ge_mode	"mode-selection" for the E_T comparator. Valid strings are "true" and "false" (type is boolean), "true" means comparator works on greater/equal, "false" means equal (for tests only)
obj_type	valid strings are "ETT_TYPE", "HTT_TYPE", "ETM_TYPE", "HTM_TYPE" and "ETMHF_TYPE".
et_threshold	threshold value for comparison in E_T . The size of the std_logic_vector depends on the number of E_T bits.
phi_full_range	boolean to set full range of φ .
phi_w1_upper_limits	"upper limit" of "window"-comparator 1 for φ .
phi_w1_lower_limits	"lower limit" of "window"-comparator 1 for φ .
phi_w2_ignore	boolean to ignore "window"-comparator 2 for φ .
phi_w2_upper_limits	"upper limit" of "window"-comparator 2 for φ .
phi_w2_lower_limits	"lower limit" of "window"-comparator 2 for φ .
clk	clock input (LHC clock).
data_i	input data, structure defined in obj_type.
condition_o	output of condition (routed to Algorithms logic, see 4.4.18).

Listing 5: Entity declaration of esums_conditions.vhd

```
entity esums_conditions is
  generic (
    et_ge_mode : boolean;
    obj_type : natural := ETT_TYPE; -- ett=0, ht=1, etm=2, htm=3
    et_threshold: std_logic_vector(MAX_ESUMS_TEMPLATES_BITS-1 downto 0);
    phi_full_range : boolean;
    phi_w1_upper_limit: std_logic_vector(MAX_ESUMS_TEMPLATES_BITS-1 downto 0)
    ;
    phi_w1_lower_limit: std_logic_vector(MAX_ESUMS_TEMPLATES_BITS-1 downto 0)
    ;
    phi_w2_ignore : boolean;
    phi_w2_upper_limit: std_logic_vector(MAX_ESUMS_TEMPLATES_BITS-1 downto 0)
    ;
    phi_w2_lower_limit: std_logic_vector(MAX_ESUMS_TEMPLATES_BITS-1 downto 0)
  );
  port(
    clk : in std_logic;
    data_i : in std_logic_vector(MAX_ESUMS_BITS-1 downto 0);
    condition_o : out std_logic
  );
end esums_conditions;
```

4.4.11 Muon shower bits

Muon shower bits MUS0 (MUon Shower, bit 61 on MU0), MUS1 (bit 61 on MU2), MUS2 (two loose muon shower - bit 61 on MU3), MUSOOT0 (MUon Shower Out Of Time, bit 61 on MU4), MUSOOT1 (bit 61 on MU6) (see [4.4.4](#) and Table [18](#)) can be selected by TME [5] to an algo or combined with other conditions to an algo.

4.4.12 Minimum bias trigger conditions

Data for Minimum bias trigger are received on the 4 MSBs of 4 frames used for Energy sum quantities (see [4.4.10](#)).

- MBT0HFP: "minimum bias HF+ threshold 0" bits
- MBT0HFM: "minimum bias HF- threshold 0" bits
- MBT1HFP: "minimum bias HF+ threshold 1" bits
- MBT1HFM: "minimum bias HF- threshold 1" bits

In minimum bias trigger conditions module there is a comparision with a 4-bit threshold (greater-equal [or equal]).

4.4.13 Towercount condition

Data for Towercount trigger (number of firing HCAL towers) are received on frame HT (see [4.4.10](#)) on bits 24..12 (13 bits) of HT data structure.

In towercount condition module there is a comparision with a 13-bit threshold (greater-equal [or equal]).

4.4.14 Centrality condition

Centrality bits used as a signals for triggers (similar to external signals).

4.4.15 Correlation conditions

The correlation conditions contain a combination of two "Single object requirement conditions" of two object types or one "Double objects requirement condition" of objects of the same type. In addition with object cuts there are correlation cuts for $\Delta\eta$, $\Delta\varphi$, ΔR , mass, mass divided by ΔR and "two-body pt".

The correlation condition of "Invariant mass for three objects" contains one "Triple objects requirement condition" of objects of the same type with one object cut for mass.

List of correlation cuts in [4.4.7](#).

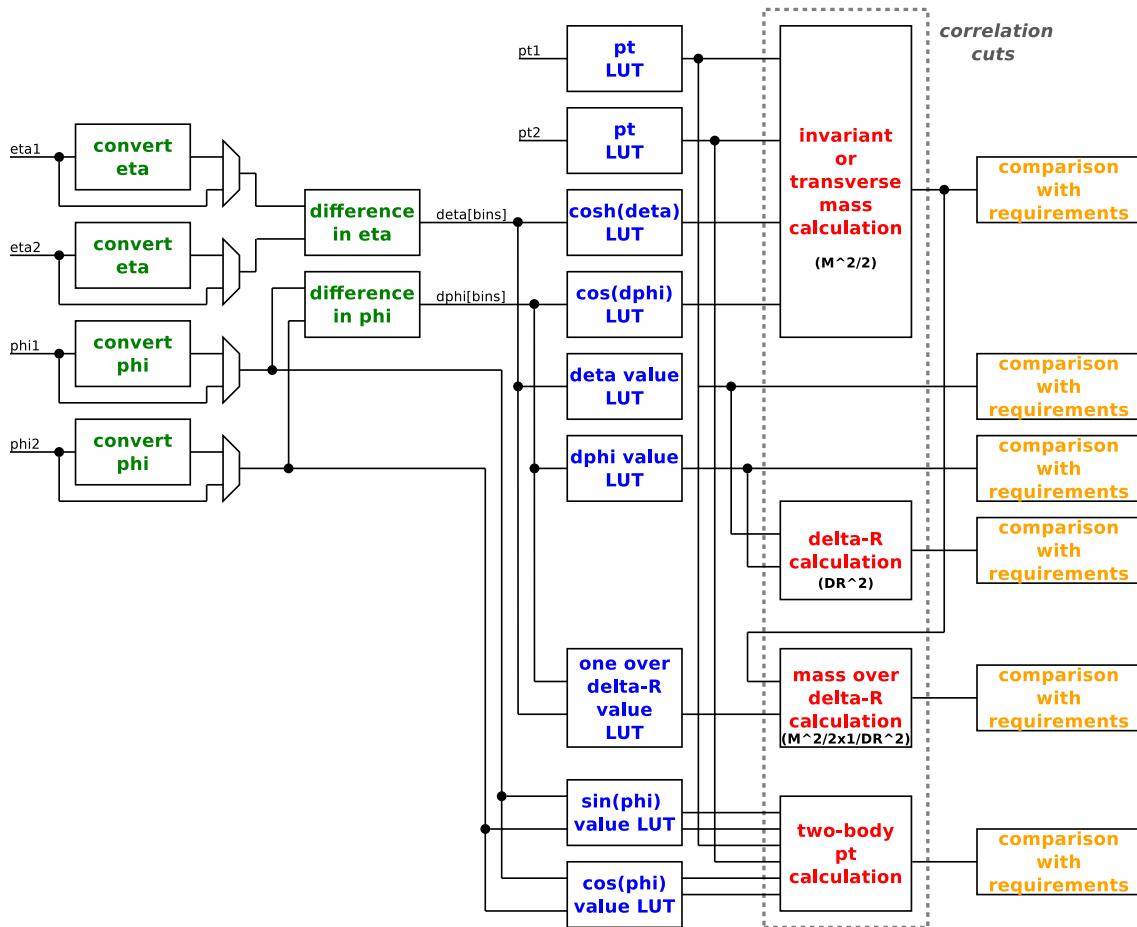


Figure 12: VHDL structure of cuts for correlation conditions

Overview of correlation cuts in conditions

The following list gives an overview of possible correlation cuts in conditions:

- Calo conditions:
 - two-body pt (for double condition)
- Calo conditions overlap removal:

- $\Delta\eta$ overlap removal
- $\Delta\varphi$ overlap removal
- ΔR overlap removal
- two-body pt (for double condition)
- Muon conditions:
 - charge correlation
 - two-body pt (for double condition)
- Calo calo correlation condition with calo overlap removal:
 - $\Delta\eta$ overlap removal
 - $\Delta\varphi$ overlap removal
 - ΔR overlap removal
 - $\Delta\eta$
 - $\Delta\varphi$
 - ΔR
 - invariant mass
 - two-body pt
- Calo calo correlation condition:
 - $\Delta\eta$
 - $\Delta\varphi$
 - ΔR
 - invariant mass
 - two-body pt
- Calo calo correlation condition for invariant mass divided by ΔR :
 - invariant mass divided by ΔR
- Calo calo correlation condition mass with three objects:
 - invariant mass with three objects
- Calo muon correlation condition:
 - $\Delta\eta$
 - $\Delta\varphi$
 - ΔR
 - invariant mass
 - two-body pt
- Calo esums correlation condition:

- $\Delta\varphi$
- transverse mass
- two-body pt
- Muon muon correlation condition:
 - charge correlation
 - $\Delta\eta$
 - $\Delta\varphi$
 - ΔR
 - invariant mass or invariant mass unconstraint pt
 - two-body pt
- Muon muon correlation condition for invariant mass divided by ΔR :
 - charge correlation
 - invariant mass divided by ΔR
- Muon muon correlation condition mass with three objects:
 - charge correlation
 - invariant mass with three objects
- Muon esums correlation condition:
 - $\Delta\varphi$
 - transverse mass
 - two-body pt

4.4.15.1 Correlation condition module

As described in section Correlation conditions (4.4.15), correlations of two object types are available. Therefore several correlations (objects 1-objects 2) are possible:

- Correlation condition with calorimeter objects electron/ γ -electron/ γ , electron/ γ -jet, electron/ γ -tau, jet-jet, jet-tau and tau-tau.
- Correlation condition with calorimeter objects and energy sum quantities (ET_{miss} , ET_{miss}^{HF} and HT_{miss} only)
electron/ γ -etm, jet-etm, tau-etm, electron/ γ -htm, jet-htm, tau-htm, electron/ γ -etmhf, jet-etmhf and tau-etmhf.
- Correlation condition with calorimeter objects and muons objects electron/ γ -muon, jet-muon and tau-muon.
- Correlation condition with muon objects

- Correlation condition with muon objects and energy sum quantities (ET_{miss} , ET_{miss}^{HF} and HT_{miss} only)
muon-etm, muon-etmhf and muon-htm.

There are two correlations for mass with three objects:

- Correlation condition for mass with three objects with calorimeter objects (same type, same bunch-crossing)
- Correlation condition for mass with three objects with muon objects

In correlation condition with calorimeter and muons objects we have different scales of calorimeter and muon objects in η and φ , therefore LUTs for conversion of the calorimeter bins to muon bins are used (in '[gtl_pkg.vhd](#)': e.g. EG_ETA_CONV_2_MUON_ETA_LUT and EG_PHI_CONV_2_MUON_PHI_LUT).

Remark:

The center value of bins are used as reference value for conversion. The content of EG_ETA_CONV_2_MUON_ETA_LUT is calculated with formular:

"converted-calо-eta[bin] = calо-eta[bin] $\times 4 + 2$ ",

of EG_PHI_CONV_2_MUON_PHI_LUT with formular:

"converted-calо-phi[bin] = calо-phi[bin] $\times 4 + 2$ ".

Definitions of scales (see Tables [10](#), [11](#), [13](#) and [14](#)):

- Calorimeter objects:
 - η bin width = $\frac{0.087}{2}$ (bin 0 from 0.0 to $\frac{0.087}{2}$)
 - ϕ bin width = $\frac{2\pi}{144}$ (bin 0 from 0.0 to $\frac{2\pi}{144}$)
- Muon objects:
 - η bin width = $\frac{0.087}{8}$ (bin 0 from $0.5 \times \frac{-0.087}{8}$ to $0.5 \times \frac{+0.087}{8}$)
 - ϕ bin width = $\frac{2\pi}{576}$ (bin 0 from 0.0 to $\frac{2\pi}{576}$)

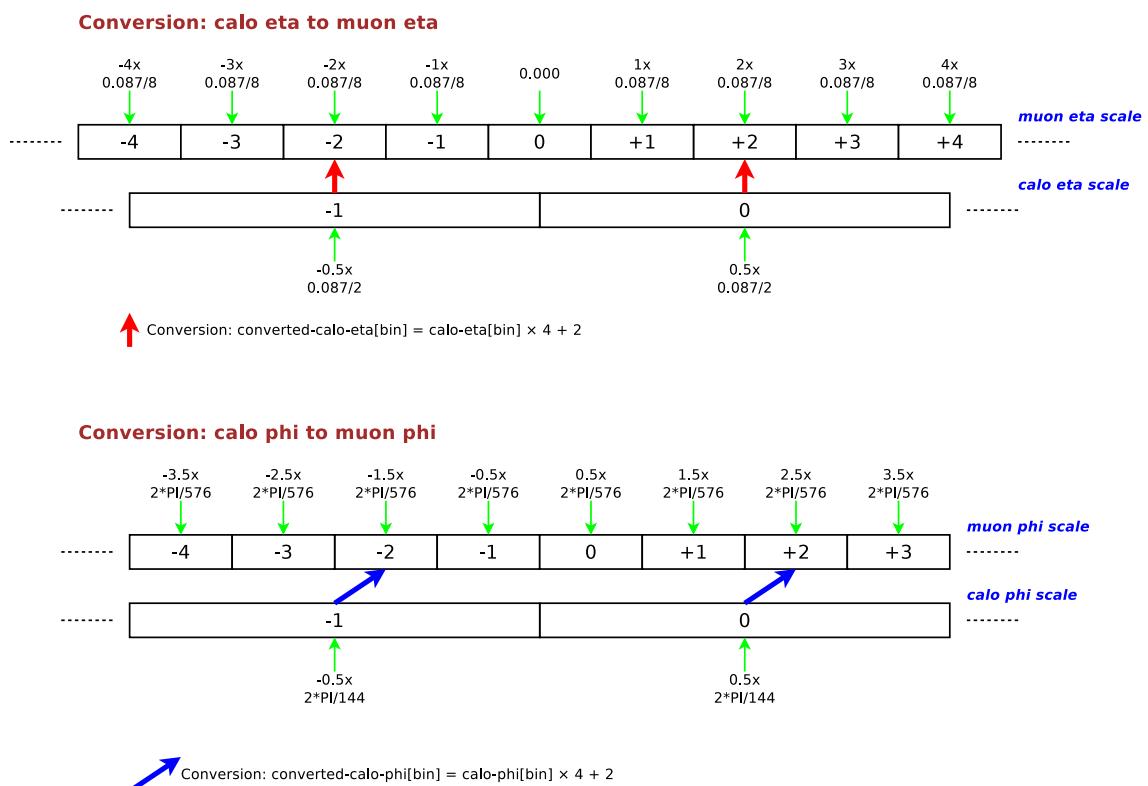


Figure 13: Conversion of calorimeter η and φ to muon scales

4.4.16 ML Triggers

4.4.16.1 Anomaly Detection Trigger

The possibility of implementing "Anomaly Detection Trigger" (ADT) is foreseen in this version of μ GTL. The VHDL code of HLS generated files is given by "Anomaly Detection Trigger" group in directory `anomaly_detection` with `axol1tl_v3.vhd` as top module. In `adt_wrapper.vhd` module `axol1tl_v3.vhd` is instantiated and a comparison of the output of `axol1tl_v3.vhd` ("anomaly_score") with a given threshold is implemented to get an "Anomaly Detection Trigger". The "anomaly_score" consists of 18 bits, currently. "Anomaly Detection Trigger" can use all input objects of μ GT, except CICADA data and external condition inputs, for calculating the "anomaly_score" value.

4.4.16.2 AXOL1TL Trigger

The possibility of implementing "AXOL1TL Trigger" (AXO) is foreseen in this version of μ GTL. The VHDL of HLS generated files code is given by "Anomaly Detection Trigger" group in `axol1tl_trigger`. Because of the possibility using different models for "AXOL1TL Trigger" (see Table 27), directories for the models are foreseen. The directories are named `model_<model name>`, e.g. `model_v3` with `axol1tl_v3.vhd` as top module. In `axol1tl_v3_wrapper.vhd` module `axol1tl_v3.vhd` is instantiated and a comparison of the output of "score" with a given threshold is implemented to get an "AXOL1TL Trigger". The "score" consists of 18 bits, currently. "AXOL1TL Trigger" can use all input objects of μ GT, except CICADA data and external condition inputs, for calculating the "score" value.

Table 27: AXOL1TL models

Key	Description	Status
v1	first version (docu missing)	implemented
v2	-	not implemented
v3	AXOL1TL v3	implemented
v4	current version (docu missing)	implemented

4.4.16.3 Topological Trigger

Similar to "AXOL1TL Trigger" a "Topological Trigger" is part of this version. The VHDL code of HLS generated files is given by "Anomaly Detection Trigger" group in `topo_trigger`. Because of the possibility using different models for "Topological Trigger" (see Table 28), directories for the models are foreseen. The directories are named `model_<model name>`, e.g. `model_hh_ele_v1` with `topo_hh_ele_v1.vhd` as top module. In `topo_hh_ele_v1_wrapper.vhd` module `topo_hh_ele_v1.vhd` is instantiated and a comparison of the output of "score" with a given threshold is implemented to get an "Topological Trigger". The "score" consists of 16 bits, currently. "Topological Trigger" can use all input objects of μ GT, except CICADA data and external condition inputs, for calculating the "score" value.

Table 28: TOPO models

Key	Description	Status
base_v1	version used for TOPO tests (docu missing)	implemented
hh_ele_v1		not implemented yet
hh_had_v1		not implemented yet
hh_mu_v1		not implemented yet

4.4.16.4 CICADA Trigger

The Anomaly Detection value of CICADA is represented (currently) by an 8 bits integer part (cicada_integer_precision) and an 8 bits decimal part (cicada_decimal_precision), which are combined to a 16 bits word for comparison with requested threshold ("cscore"). In TME [5] the threshold can be selected with predefined values for the decimal part ($x/2^{**\text{cicada_decimal_precision}}$, for all x from 0 to $2^{**\text{cicada_decimal_precision}}$) and values from 0 to cicada_integer_precision for the integer part. In VHDL Producer a function converts the threshold to integer for "cscore" value. In VHDL module `cicada_condition.vhd` this "cscore" value is used. The trigger decision is made by comparison of 16 bits Anomaly Detection value of CICADA with "cscore". CICADA data are received in μ GT at input link 11 from Calo-Layer1 system (see chapter 4.2.3).

4.4.17 External Conditions

Maximal 256 External Conditions are possible in Global Trigger. They are provided as inputs in the Algorithms logic of μ GTL. External Conditions will include the "Technical Trigger" of the legacy system.

4.4.18 Algorithms logic

The outputs of all the instantiated conditions are combined in the Algorithms logic with boolean algebra given by TME for every single Algorithm. These Algorithms are registered and provided as inputs for Final Decision Logic.

5 Final Desicion Logic

This description is for version v1.4.1 of Final Desicion Logic.

The Final Desicion Logic (μ FDL) firmware contains algo-bx-masks, suppression of algos caused by calibration trigger, prescalers, veto-masks and rate-counters ("before prescalers", "after prescalers" and "post dead time") for each Algorithm and the local Final-OR- and veto-logic.

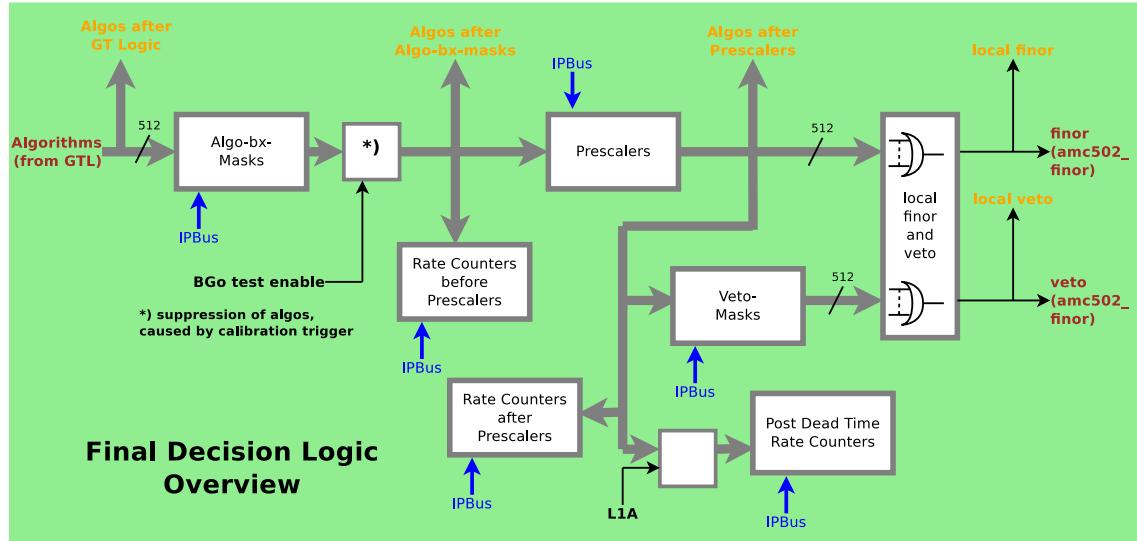


Figure 14: μ FDL firmware

5.1 μ FDL Interface

Inputs:

- Algorithms from μ GTL
- IPBus interface (for registers, counters and memories)
- LHC clock
- Reset signal
- BC0, BGo test-enable, L1A
- Begin of lumi-section

Outputs:

- Prescale factor set index to Readout-Process

- Algorithms after GTLogic to Readout-Process
- Algorithms after algo-bx-masks to Readout-Process
- Algorithms after prescalers to Readout-Process
- Algorithms after Final-OR-masks to Readout-Process
- Local Final-OR to Readout-Process
- Local veto to Readout-Process
- Local Final-OR with veto to Readout-Process
- Local Final-OR to mezzanine
- Local veto to mezzanine
- Local Final-OR with veto to mezzanine

5.2 MP7 Final-OR hardware solution

The firmware of μ FDL in this document is based on a hardware configuration with maximum 6 μ GT modules.

5.3 Data flow

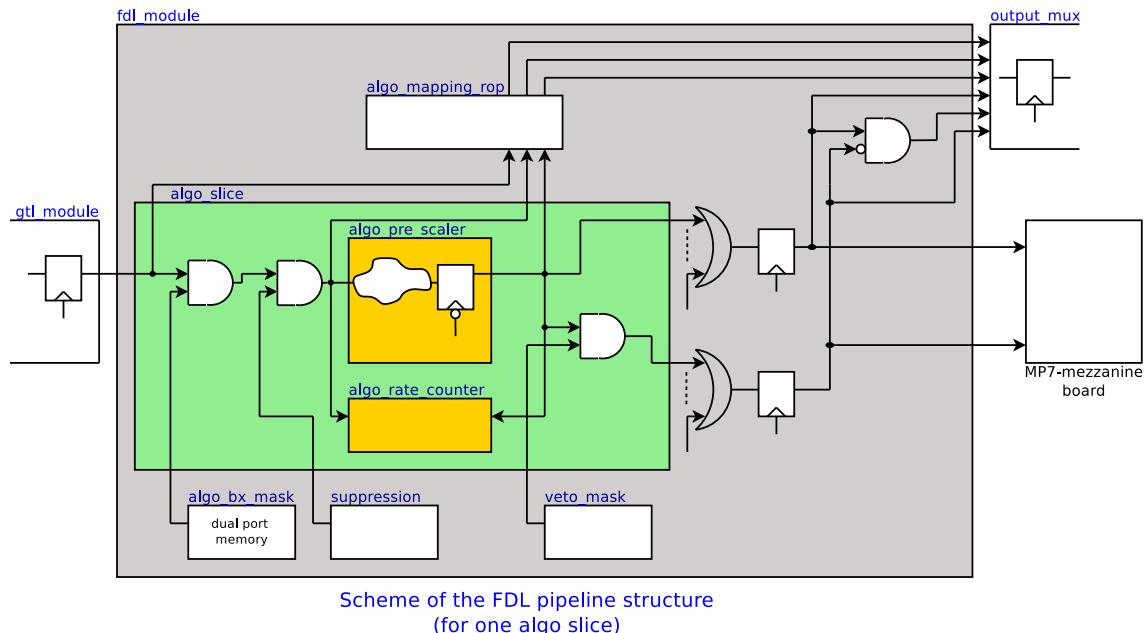


Figure 15: μ FDL pipeline

Every Algorithm, in total 512 coming from μ GTL, passes a algo-bx-mask, the logic for suppression of algos caused by calibration trigger (5.17) and a prescaler, which reduces the trigger rate by a given factor. The factor has a precision of two digits after comma ("fractional prescale factor"). Prescaled Algorithms signals are combined to a local final-or-signal (Final-OR). For every Algorithm there is a rate-counter before prescaler and after prescaler, which are incremented by LHC clock if the Algorithm is true. In addition there are post-dead-time counters, one for each Algorithm, which are incremented, if the Algorithm and the L1A-signal are true at the same bunch-crossing. Algorithms after GTLogic, after algo-bx-masks, after prescalers, the local Final-OR- and local Veto-signal are provided for read-out-record.

If there are not enough firmware resources in one μ GT board, more boards could be used. Therefore the 512 Algorithms are partitioned by TME. TME will set the number of Algorithms as constant in the package module '[gt1_pkg.vhd](#)'. This means μ GTL and μ FDL firmware considered as a unit for synthesis. In the case of more μ GT boards, the local Final-OR and local veto are routed via a mezzanine board on MP7 (located on "General Purpose I/O connector") to the FINOR-AMC502 module, where the total Final-OR is created and send to TCDS.

A mapping for Algorithms is provided, to give flexibility for setting the index of Algorithms:

- creating a mapping instance (algo_mapping_rop.vhd) by VHDL Producer, this component will be instantiated in fix part of FDL, and new calculation will done each time over TME.
- TME delivers just the number of Algorithms, which will be built on each card.
- from FDL point of view, FDL see incremented number of Algorithms indexes, e.g. 0, 1, 2, which is e.g. 69, 200, 300.
- TME should take care of assignment of each Algorithm to a number, that means if in card 1 algo_59 is defined, nobody allows to produce the same number again.

5.4 Implementation in firmware

The entity declaration of '`fdl_module.vhd`' is shown in 5.3.

Listing 6 contains the entity declaration of '`fdl_module.vhd`'.

Listing 6: Entity declaration of `fdl_module.vhd`

```
entity fdl_module is
    generic(
        SIM_MODE : boolean := false; -- if SIM_MODE = true, "algo_bx_mask" is
        given by "algo_bx_mask_sim".
        PRESCALE_FACTOR_INIT : ipb_regs_array(0 to MAX_NR_ALGOS-1);
        MASKS_INIT : ipb_regs_array(0 to MAX_NR_ALGOS-1);
        PRESCALE_FACTOR_SET_INDEX_WIDTH : positive := 8;
        PRESCALE_FACTOR_SET_INDEX_REG_INIT : ipb_regs_array(0 to 1) := (others =>
            X"00000000");
        L1A_LATENCY_DELAY_INIT : ipb_regs_array(0 to 1) := (others => X"00000000"
            );
        CNTRL_REG_INIT : ipb_regs_array(0 to 1) := (others => X"00000000");
    -- Input flip-flops for algorithms of fdl_module.vhd - used for tests of
    -- fdl_module.vhd only
        ALGO_INPUTS_FF: boolean := false
    );
    port(
        ipb_clk           : in std_logic;
        ipb_RST           : in std_logic;
        ipb_in            : in ipb_wbus;
        ipb_out           : out ipb_rbus;
    --
    -- =====
        lhc_clk           : in std_logic;
        lhc_RST           : in std_logic;
        bcres             : in std_logic;
        test_en           : in std_logic;
        l1a               : in std_logic;
        begin_lumi_section : in std_logic;
        algo_i             : in std_logic_vector(NR_ALGOS-1 downto 0);
        bx_nr_out         : out std_logic_vector(11 downto 0);
        prescale_factor_set_index_rop : out std_logic_vector(
            PRESCALE_FACTOR_SET_INDEX_WIDTH-1 downto 0);
        algo_after_gtLogic_rop   : out std_logic_vector(MAX_NR_ALGOS-1 downto 0);
        algo_after_bxomask_rop   : out std_logic_vector(MAX_NR_ALGOS-1 downto
            0);
        algo_after_prescaler_rop : out std_logic_vector(MAX_NR_ALGOS-1
            downto 0);
        local_finor_rop      : out std_logic;
        local_veto_rop       : out std_logic;
        finor_2_mezz_lemo    : out std_logic; -- to LEMO
        finor_preview_2_mezz_lemo : out std_logic; -- to LEMO
        veto_2_mezz_lemo     : out std_logic; -- to LEMO
        finor_w_veto_2_mezz_lemo : out std_logic; -- to tp_mux.vhd
        local_finor_with_veto_o : out std_logic; -- to SPY2_FINOR
    -- HB 2016-03-02: v0.0.21 - algo_bx_mask_sim input for simulation use with
    -- MAX_NR_ALGOS (because of global index).
        algo_bx_mask_sim     : in std_logic_vector(MAX_NR_ALGOS-1 downto 0)
```

5 Final Desicion Logic

```
) ;  
end fdl_module;
```

Table 29: Explanation of Listing 6

Item	Explanation
SIM_MODE	switch for simulation mode.
PRESCALE_FACTOR_INIT	init value for prescale factor.
MASKS_INIT	init value for BX mask.
PRESCALE_FACTOR_SET_INDEX_WIDTH	width of prescale factor set index.
PRESCALE_FACTOR_SET_INDEX_REG_INIT	init value prescale factor set index register.
L1A_LATENCY_DELAY_INIT	init value of L1A latency delay.
CNTRL_REG_INIT	init value control register.
ALGO_INPUTS_FF	switch for algos input flip-flops.
ipb_clk	IPBus clock input.
ipb_RST	IPBus reset input.
ipb_in	IPBus data input.
ipb_out	IPBus data output.
lhc_clk	clock input (LHC clock).
lhc_RST	reset input.
bcres	TTC BGo bunch counter reset input.
test_en	TTC BGo test enable input.
l1a	L1A input.
begin_lumi_section	begin of lumisection input.
algo_i	algos input.
bx_nr_out	bunch crossing number output.
prescale_factor_set_index	prescale factor set data output.
algo_after_gtLogic_rop	algos after GTL output.
algo_after_bxomask_rop	algos after BX mask output.
algo_after_prescaler_rop	algos after prescaler output.
local_finor_rop	local FINOR output.
local_veto_rop	local VETO output.
finor_2_mezz_lemo	FINOR to MP7 mezzanine board and via LEMO connection to FINOR board.
finor_preview_2_mezz_lemo	FINOR preview to MP7 mezzanine board and via LEMO connection to FINOR preview board.
veto_2_mezz_lemo	VETO to MP7 mezzanine board and via LEMO connection to FINOR board.
finor_w_veto_2_mezz_lemo	FINOR with VETO to MP7 mezzanine board and via LEMO connection to FINOR board.
local_finor_with_veto_o	local FINOR with VETO output.
algo_bx_mask_sim	algo-bx-mask input for simulation.

5.5 Main parts

The top-of-hierarchy module (`'fdl_module.vhd'`) contains

- version registers
- a command pulse register
- prescalers for all Algorithms
- registers for prescale factors
- register for prescale factor set index
- rate-counters for all Algorithms, finor, veto, L1A and post-dead-time
- read only registers for rate-counter values
- algo-bx-masks for all Algorithms
- Final-OR-masks for all Algorithms
- veto-masks for all Algorithms
- the Final-OR-logic

5.5.1 Algo-bx-masks

Every Algorithm passes a logic where at every bunch-crossing of the orbit the Algorithm is enabled (or not). The algo-bx-masks are implemented as dual-port memories and loaded at the begin of run. The size of the algo-bx-masks memory is number of bunch-crossings per orbit for address length and number of Algorithms for data-depth (3564 [4096] x 512 bits). The address (bx-number) of the memory for masking the Algorithm is delivered by an address-counter for algo-bx-masks memory, which is reseted with a delay-able bres signal, to get the correct relations between Algorithms and masks from memory.

5.5.2 Rate-counters

Every Algorithm has rate-counters with 32 bits, because of the length of one luminosity segment period. There are counters before and after prescalers and post-dead-time counters (5.1, 5.3 and 5.4). The counters before and after prescalers are incremented, if the Algorithm signal is in high state and a positive edge of LHC clock occur. The post-dead-time counters are incremented, if the Algorithm signal, delayed by L1A latency delay (5.12), is in high state, a L1A signal and a positive edge of LHC clock occur. The content of a counter is updated into a register (for reading the counter value) and is set to 0 at the begin of a luminosity segment period. So there is one luminosity segment period time to read the registers with the counter values by software. In addition there are rate-counters for Final-OR-signal, Veto-signal and L1A-signal implemented (5.11, 5.14 and 5.13). All counters count the occurrancy of the signal in one luminosity segment.

5.5.3 Prescalers

Every Algorithm has a prescaler with a prescale factor of 24 bits (5.2). The prescaler reduces the trigger-rate per Algorithm with a factor. So a factor of 2 lets every second trigger request of this Algorithm pass, a factor of 3 every third request and so on. A prescale factor of 1 lets all triggers pass while a factor of 0 inhibits all trigger requests of the corresponding Algorithm. Since 2019 the logic allows also for fractional prescale factor values. Prescale factors are listed in integer or float format in prescale tables. The precision of the fractional prescale factor values in the current implementation is 2 (2 digits after decimal point). Software multiplies the fractional prescale factor with $10^{\text{precision}}$ (i.e., currently by 100) and loads it into a register. At the beginning of a new “luminosity section” (“lumi section”) the factor is updated if during the preceding lumi section the update was requested by software. For this, in the “command pulses” register (5.10) the value of “request update factor pulse” is first set to 1 and then back to 0. The prescaler then uses the updated factor. A register for the “prescale factor set index” (5.6) contains a value which represents a certain set of prescale factors (commonly referred to as “prescale column” in CMS). The content of this register can be seen in the Readout-record, too. The “prescale factor set index” is loaded into the register by software and updated at the beginning of the next lumi section (5.15 and 5.16).

5.5.3.1 Prescaler logic

With each trigger request of the Algorithm, a counter is incremented by $10^{\text{precision}}$ as long as the incremented counter is less than the prescale factor. If the incremented counter is greater or equal than the prescale factor, the trigger request of the prescaled Algorithm is forwarded to the Final Decision Logic (for one clock cycle) and the prescale factor is subtracted from the incremented counter during the next clock cycle.

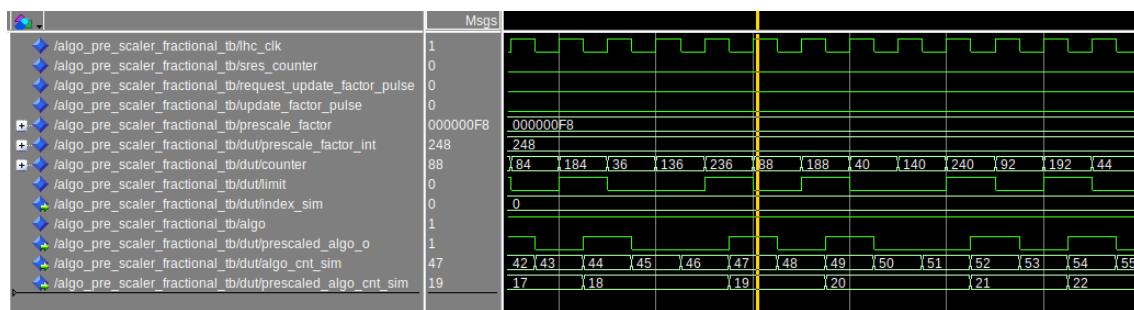


Figure 16: Fractional prescaler

In Figure (16) one can see the simulation of a fractional prescaler. In this example the fractional prescale factor is 2.48 and the signal “prescale factor int” shows this value multiplied by $10^{\text{precision}}$, i.e., currently by 100 (so, 248). The signal “algo” is always true, in other words, without prescale this Algorithm would be firing (sending a trigger request) in every bunch crossing. Signal “prescaled algo o” shows when the trigger request of the prescaled Algorithm is allowed to pass. Signals “algo cnt sim” and “prescaled algo cnt sim” show the number of this Algorithm’s trigger requests before and after the prescale logic. At the cursor point a factor $47/19 (\approx 2.4737)$ is reached. With “algo cnt sim” reaching higher numbers, on average

the effective prescale factor gets closer and closer to the requested value of 2.48. The prescaler is reseted with B-Go "start" signal, at the begin of a run.

5.5.4 Finor-masks

Every Algorithm passes a Final-OR-mask, which enables the Algorithm for Final-OR. The Final-OR-masks are implemented as registers (5.5) and loaded at the begin of a run.

Configuration of Final-OR-masks is done by a "run settings key" (e.g. UGT_RS_KEYS => ugt_rs_algo_finor_mask_empty/v4)

5.5.5 Veto-masks

Every Algorithm passes a veto-mask, if at least one Algorithm, which is enabled by veto-mask, becomes high state, then Final-OR is disabled as long as the Algorithm is in high state. The veto-masks are implemented as registers (5.5) and loaded at the begin of a run.

Configuration of veto-masks is done by a "run settings key" (e.g. UGT_RS_KEYS => ugt_rs_algo_finor_veto_all_zero/v2)

5.5.6 Finor

The Final-OR-signal is a disjunction of all Algorithms passed the Final-OR-bx-masks. An Algorithm enabled by veto-mask, disables the Final-OR. This is done on the FINOR-AMC502 module.

5.5.7 Registers and memories

All registers and memories are 32 bits wide. (Definition of addresses is shown in Table 30.)

- Dual-port memories for the algo-bx-masks are implemented. For each Algorithm there is a mask bit at every bunch crossing of one orbit. Therefore in total memories of 4096 x 512 bits are implemented. Because of the 32 bit data interface, 16 memories each with a size of 4096 x 32 bits are instantiated.
- Read-only registers for the value of rate-counters (before and after prescalers, post-dead-time counters) are implemented, 512 registers, one for every Algorithm. Rate-counter value has 32 bits.
- Registers for prescale factor of the prescalers are implemented, 512 registers, one for every Algorithm. A prescale factor value has 24 bits.
- Registers for masks (Final-OR- and veto-masks) are implemented, 512 registers.
- One register for prescale factors set index is implemented. This register contains a value, which is unique for a given set of prescale factors. The content of this register is part of Readout-record.
- One register for command pulses is implemented. One bit of this register (bit 0) is used for "setting the request signal for updating prescale factors high", which enables, that the prescale factors and the prescale factor set index are loaded at the begin of a luminosity segment period. (Other bits are not defined yet.)
- One control register is implemented (the content has to be defined).
- 32 register for L1 Trigger Menu name for μ GTL is implemented.
- 4 register for L1 Trigger Menu UUID for μ GTL is implemented.
- One register for L1 Trigger Menu compiler version is implemented.
- One register for μ FDL firmware version is implemented.
- One register for μ GTL firmware (fixed code) version is implemented.

5.5.7.1 Register map

The register map for μ FDL has a base address of 0x90000000.

Remark:

Register "SVN revision number" is used for firmware version of Framework VHDL code (SVN revision number is obsolete).

Table 30: μ FDL register map

Offset	Register name	Access	Description
0x90000000	Algo BX masks (0)	r/w	4096 memory addresses of algo-bx-masks for Algorithms 0-31.
0x90001000	Algo BX masks (1)	r/w	4096 memory addresses of algo-bx-masks for Algorithms 32-63.
...
0x9000F000	Algo BX masks (15)	r/w	4096 memory addresses of algo-bx-masks for Algorithms 480-511.
0x90010000	Rate counter before prescaler (5.1)	r	512 read-only registers for rate-counter values before prescalers.
0x90010200	Prescale factors (5.2)	r/w	512 registers for prescale factors.
0x90010400	Rate counter after prescaler (5.3)	r	512 read-only registers for rate-counter values after prescalers.
0x90010600	Rate counter post-dead-time (5.4)	r	512 read-only registers for post-dead-time rate-counter values.
0x90010800	Masks (5.5)	r/w	512 registers for Final-OR-masks and veto-masks. Bit 0 = Final-OR-mask, bit 1 = veto-mask.
0x90091880	Prescale factors set index (5.6)	r/w	Register for prescale factors set index.
0x900918C0	L1tm name	r	32 registers for L1 Trigger Menu name for μ GTL.
0x900918E0	L1tm uuid	r	4 registers for L1 Trigger Menu UUID for μ GTL.
0x900918E4	L1tm compiler (5.7) version	r	Register for L1 Trigger Menu compiler version.
0x900918E5	GTL FW version (5.8)	r	Register for firmware version of μ GTL VHDL code.
0x900918E6	FDL FW version (5.9)	r	Register for firmware version of μ FDL VHDL code.
0x900918E7	L1tm FW uuid	r	4 registers for L1 Trigger Menu FW UUID for μ GTL.
0x900918EB	SVN revision number	r	Register for firmware version of framework VHDL code.
0x900918EC	L1tm uuid hash	r	Register for L1 Trigger Menu UUID hash for μ GTL.

Table 30: μ FDL register map

Offset	Register name	Access	Description
0x900918ED	L1tm FW uuid hash	r	Register for L1 Trigger Menu FW UUID hash for μ GTL.
0x900918EE	Module ID	r	Register for Module ID of L1 Trigger Menu.
0x90091900	Command Pulses (5.10)	r/w	Register for command pulses (request_update_factor_pulse).
0x90091980	Rate counter finor (5.11)	r	One read-only registers for finor rate-counter value.
0x90092200	L1A latency delay (5.12)	r/w	Register for L1A latency delay value (used for post-dead-time counter).
0x90093000	Rate counter L1A (5.13)	r	One read-only registers for L1A rate-counter value.
0x90094000	Rate counter veto (5.14)	r	One read-only registers for veto rate-counter value.
0x90095000	Current prescale set index (5.15)	r	Read-only register for prescale factors set index, which was "updated" with begin of current lumi-section ("prescale_factors_set_index_reg_updated(0)" in VHDL).
0x90095001	Previous prescale set index (5.16)	r	Read-only register for prescale factors set index, which was "updated" with begin of previous lumi-section for monitoring "prescale_factors_set_index_reg_updated(1)" in VHDL.
0x90096000	Calibration trigger gap (5.17)	r/w	Register for begin and end (in Bx) of calibration trigger gap.

Register 5.1: RATE COUNTER BEFORE PRESCALER

		rate_counter_before_prescaler
31	0	
0		Reset

rate_counter_before_prescaler Rate counter before prescaler. Counts the occupancy of an algo (given by register address) in one luminosity segment.

Register 5.2: PRESCALE FACTOR

		prescale_factor
31	24	
0		1
		Reset

prescale_factor Prescale factor of an algo (given by register address). Prescale factor = 0 means "disable alg". The factor has a precision of two digits after comma, therefore values in register are equal to factor * 100 (e.g.: factor=1.00 => 100 [0x64]).

Register 5.3: RATE COUNTER AFTER PRESCALER

		rate_counter_after_prescaler
31	0	
0		Reset

rate_counter_after_prescaler Rate counter after prescaler. Counts the occupancy of an algo (given by register address) in one luminosity segment.

Register 5.4: RATE COUNTER POST-DEAD-TIME

rate_counter_postdeadtime	
31	0
0	Reset

rate_counter_postdeadtime Rate counter post-dead-time. Counts the occupancy of an algo (given by register address) and L1A at the same bx in one luminosity segment.

Register 5.5: MASKS

reserved		veto_mask finor_mask	
31		2 1 0	
0		0 1	Reset

veto_mask Selection of a veto (by an algo, given by register address) for veto-or.

finor_mask Selection of an algo (given by register address) for final-or.

Register 5.6: PRESCALE FACTORS SET INDEX

reserved		prescale_factor_set_index	
31		8 7 0	
0		0	Reset

prescale_factor_set_index Index for a certain set of prescale factors.

Register 5.7: L1TM COMPILER VERSION							
reserved	major			minor		revision	
31	24	23		16	15	8	7 0
0		0			0	0	Reset

major Major version of VHDL producer.

minor Minor version of VHDL producer.

revision Revision version of VHDL producer.

Register 5.8: GTL FW VERSION							
reserved	major			minor		revision	
31	24	23		16	15	8	7 0
0		0			0	0	Reset

major Major version of GTL firmware.

minor Minor version of GTL firmware.

revision Revision version of GTL firmware.

Register 5.9: FDL FW VERSION							
reserved	major			minor		revision	
31	24	23		16	15	8	7 0
0		0			0	0	Reset

major Major version of FDL firmware.

minor Minor version of FDL firmware.

revision Revision version of FDL firmware.

Register 5.10: COMMAND PULSES REGISTER

The diagram shows the memory map for the `request_update_factor_pulse` register. It consists of a 32-bit register divided into four fields: a 5-bit `reserved` field at address 31, a 24-bit `request_update_factor` field at address 0, and a 1-bit `Reset` control field at address 0.

31	request_update_factor				
	reserved				
0					
	Reset				

request_update_factor_pulse A sequence of applying 1 followed by 0 generates the "request update factors pulse". (Updating is done at the next "begin of luminosity segment".)

Register 5.11: RATE COUNTER FINOR

31	0	0
		rate counter finor
		Reset

rate_counter_finor Rate counter finor. Counts the occurrancy of finor in one luminosity segment.

Register 5.12: L1A LATENCY DELAY

Register 0x12: L1A LATENCY DELAY			
29	reserved	6 5	0
0		0	Reset

l1a_latency_delay L1A latency delay value (used for post-dead-time counter).

Register 5.13: RATE COUNTER L1A

rate_counter_l1a	
31	0
0	Reset

rate_counter_l1a Rate counter L1A. Counts the occurrancy of L1A in one luminosity segment.

Register 5.14: RATE COUNTER VETO

rate_counter_veto	
31	0
0	Reset

rate_counter_veto Rate counter veto. Counts the occurrancy of veto in one luminosity segment.

Register 5.15: CURRENT PRESCALE SET INDEX

prescale_factor_set_index_updated	
reserved	
31	0
0	0
	Reset

prescale_factor_set_index_updated Index for a certain set of prescale factors, which was "updated" with begin of current lumi-section.

Register 5.16: PREVIOUS PRESCALE SET INDEX

31	reserved								8	7	0
0								0	Reset		

prescale_factor_set_index_updated Index for a certain set of prescale factors, which was "updated" with begin of previous lumi-section.

Register 5.17: CALIBRATION TRIGGER GAP

31	28	27	reserved								16	15	12	11	0
0								0	begin_calibration_trigger_gap		end_calibration_trigger_gap		reserved		0

begin_calibration_trigger_gap Begin of calibration trigger gap (in Bx).

end_calibration_trigger_gap End of calibration trigger gap (in Bx).

6 Readout process

Data for readout are collected in '`output_mux.vhd`' (part of '`frame.vhd`'). The readout record contains:

- algorithm outputs of μ GTL (algo_after_gtLogic)
- algorithms after bunch crossing mask (algo_after_bxmask)
- algorithms after prescale logic (algo_after_prescaler)
- finor and veto bits
- prescale factor index
- bunch counters
- hash values for menu name and firmware UUID

and in addition all input data at AMC #1.

For details see [7.4](#).

The readout process of Global Trigger data is done via GTH transmitter of MP7 to AMC13.

For details of readout record structure see [\[8\]](#).

7 Appendices

7.1 Description of simulation, synthesis and hardware tests

Workflow for simulation and synthesis of firmware is described in [README](#) file.

List of useful TDF routines and commands for hardware tests:

- Check crate status

```
$ tdf run crate_status
```
- Enable TTC signals on AMC13 for all MP7 modules

```
$ tdf run ttc_enable
```
- Check lock of BC0 and LHC clock

```
$ tdf unittest <module> default
```
- Reset module

```
$ tdf mp7butler reset <module> -clksrc external -clkcfg default-ext
```
- Load firmware to scansd card on all MP7 modules [and load it into FPGAs]

```
$ tdf run uploadfw_gt <tar file path> [-rebootfpga]
```
- Load firmware from scansd card into FPGAs

```
$ tdf run loadfw_gt <fw build nr> <nr modules>
```
- Compare hardware results with test vector pattern (for a certain firmware build)

```
$ tdf run multiboard_function_test -h
```
- Setup links (GTHs)

```
$ tdf mp7butler rxmrgts <module> -e <links>
```
- Align links (GTHs)

```
$ tdf mp7butler rxalign <module> -e <links> [-to-bx <alignment point>]
```
- Check minipods

```
$ tdf mp7butler minipods <module>
```
- ... (other routines are available in /nfshome0/ugtdev/software/tdf/etc/routines)

7.1.1 Handling of timing errors in synthesis

Sometimes synthesis finish with timing errors on modules and no bit files are generated for those modules. Most of the time the errors are low or not relevant and can be ignored. In this case generation of a bit file could be done on the platform of synthesis with the following command in an environment where vivado is running (see [README](#)):

- Generate bit file

```
$ vivado -mode batch -source <local path to mp7_ugt_legacy>/  
scripts/vivado_write_bitstream.tcl -tclargs  
<path to synth dir> <module number>
```

7.1.2 Preventing timing errors by fixing cells in Vivado

Timing errors always occur in "readout" region. Therefore nodes and locations (of the nodes) are taken from an utilization of an implementation without errors (0x1192, module 0) and a constraints file was created which contains those information ('[constraints_fixed_cells.tcl](#)'). A Vivado TCL-script ('[vivado_fix_cells.tcl](#)') contains the sequence to fix cells in Vivado. It is executed by Vivado batch mode during synthesis (between "ipbb synth" and "ipbb impl").

7.2 Configuration of GTHs

The FPGA on MP7 board receives and transmits data via GTH transceivers.

7.2.1 ZDC 5G scheme

ZDC data are provided on a 5 GHz link. Figure 17 shows ZDC 5G link connection to μ Gt system.

Remark: Connection with **ZDC** is made on **MP7 in slot 1** (link 71), only!

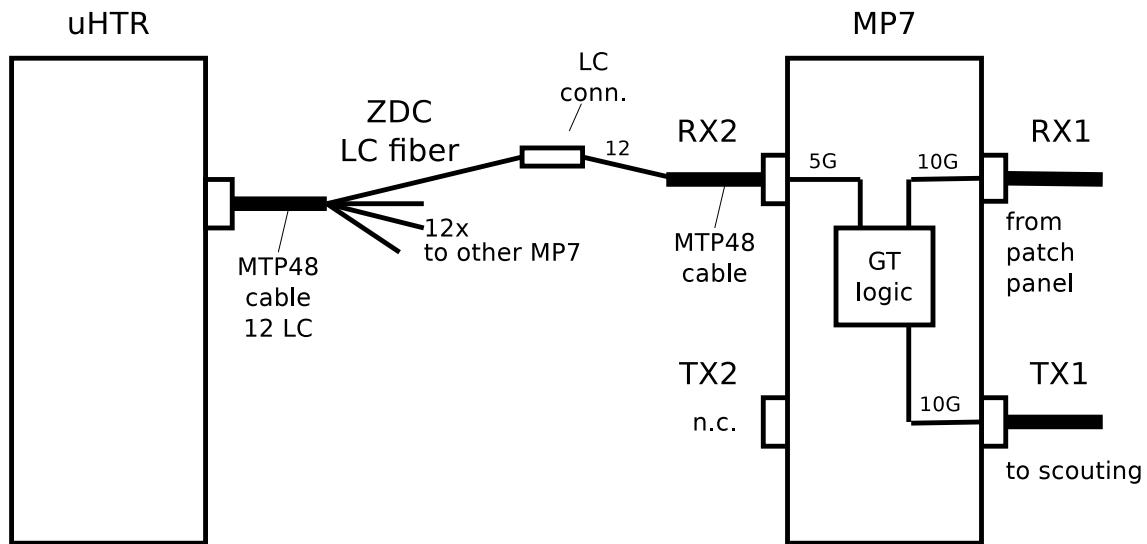


Figure 17: ZDC 5G link connection

7.2.2 GTH input connections

Table 31 contains the GTH input connections from MP7 MTP48 front connectors³:

Table 31: GTH input connections

MTP48	minipod	quad	GTH ch.	GTH	MP7 ch.	pp	lane	data
RX1/1	rx3/0	118	X1Y35	10G	0x00	1	0	muon
RX1/2	rx3/1		X1Y34	10G	0x02	2	1	muon
RX1/3	rx3/2		X1Y33	10G	0x04	3	2	muon
RX1/4	rx3/3		X1Y32	10G	0x06	4	3	muon
RX1/5	rx3/4	117	X1Y31	10G	0x08	5	4	eg
RX1/6	rx3/5		X1Y30	10G	0x0A	6	5	eg
RX1/7	rx3/6		X1Y29	10G	0x0C	7	6	jet
RX1/8	rx3/7		X1Y28	10G	0x0E	8	7	jet
RX1/9	rx3/8	116	X1Y27	10G	0x10	9	8	tau
RX1/10	rx3/9		X1Y26	10G	0x12	10	9	tau
RX1/11	rx3/10		X1Y25	10G	0x14	11	10	esums
RX1/12	rx3/11		X1Y24	10G	0x16	12	11	CICADA
RX1/13	rx4/0	115	X1Y23	10G	0x18	13	12	external conditions
RX1/14	rx4/1		X1Y22	10G	0x1A	14	13	external conditions
RX1/15	rx4/2		X1Y21	10G	0x1C	15	14	external conditions
RX1/16	rx4/3		X1Y20	10G	0x1E	16	15	external conditions
RX1/17	rx4/4	114	X1Y19	10G	0x20	17	16	free
RX1/18	rx4/5		X1Y18	10G	0x22	18	17	free
RX1/19	rx4/6		X1Y17	10G	0x24	19	18	free
RX1/20	rx4/7		X1Y16	10G	0x26	20	19	free
RX1/21	rx4/8	113	X1Y15	10G	0x28	21	20	free
RX1/22	rx4/9		X1Y14	10G	0x2A	22	21	free
RX1/23	rx4/10		X1Y13	10G	0x2C	23	22	free
RX1/24	rx4/11		X1Y12	10G	0x2E	24	23	free
RX1/25	rx5/0	112	X1Y11	10G	0x30	nc	24	-
RX1/28	rx5/3		X1Y10	10G	0x32	nc	25	-
RX1/26	rx5/1		X1Y09	10G	0x34	nc	26	-
RX1/27	rx5/2		X1Y08	10G	0x36	nc	27	-
RX1/30	rx5/5	111	X1Y07	x	0x38	nc	28	-
RX1/29	rx5/4		X1Y06	x	0x3A	nc	29	-

³"ch." means "channel", "pp conn." means "optical patch panel connector number"

Table 31: GTH input connections

MTP48	minipod	quad	GTH ch.	GTH	MP7 ch.	pp	lane	data
RX1/31	rx5/6		X1Y05	x	0x3C	nc	30	-
RX1/32	rx5/7		X1Y04	x	0x3E	nc	31	-
RX1/33	rx5/8	110	X1Y03	x	0x40	nc	32	-
RX1/34	rx5/9		X1Y02	x	0x42	nc	33	-
RX1/35	rx5/10		X1Y01	x	0x44	nc	34	-
RX1/36	rx5/11		X1Y00	x	0x46	nc	35	-
RX2/26	rx2/1	210	X0Y00	x	0x48	nc	36	-
RX2/25	rx2/0		X0Y01	x	0x4A	nc	37	-
RX2/28	rx2/3		X0Y02	x	0x4C	nc	38	-
RX2/27	rx2/2		X0Y03	x	0x4E	nc	39	-
RX2/30	rx2/5	211	X0Y04	x	0x50	nc	40	-
RX2/29	rx2/4		X0Y05	x	0x52	nc	41	-
RX2/31	rx2/7		X0Y06	x	0x54	nc	42	-
RX2/32	rx2/6		X0Y07	x	0x56	nc	43	-
RX2/33	rx2/8	212	X0Y08	x	0x58	nc	44	-
RX2/35	rx2/10		X0Y09	x	0x5A	nc	45	-
RX2/34	rx2/9		X0Y10	x	0x5C	nc	46	-
RX2/36	rx2/11		X0Y11	x	0x5E	nc	47	-
RX2/14	rx1/1	213	X0Y12	x	0x60	nc	48	-
RX2/13	rx1/0		X0Y13	x	0x62	nc	49	-
RX2/16	rx1/3		X0Y14	x	0x64	nc	50	-
RX2/15	rx1/2		X0Y15	x	0x66	nc	51	-
RX2/18	rx1/5	214	X0Y16	x	0x68	nc	52	-
RX2/17	rx1/4		X0Y17	x	0x6A	nc	53	-
RX2/20	rx1/7		X0Y18	x	0x6C	nc	54	-
RX2/19	rx1/6		X0Y19	x	0x6E	nc	55	-
RX2/22	rx1/9	215	X0Y20	x	0x70	nc	56	-
RX2/21	rx1/8		X0Y21	x	0x72	nc	57	-
RX2/23	rx1/10		X0Y22	x	0x74	nc	58	-
RX2/24	rx1/11		X0Y23	x	0x76	nc	59	-
RX2/2	rx0/1	216	X0Y24	x	0x78	nc	60	-
RX2/1	rx0/0		X0Y25	x	0x7A	nc	61	-
RX2/4	rx0/3		X0Y26	x	0x7C	nc	62	-
RX2/3	rx0/2		X0Y27	x	0x7E	nc	63	-
RX2/6	rx0/5	217	X0Y28	x	0x80	nc	64	-

Table 31: GTH input connections

MTP48	minipod	quad	GTH ch.	GTH	MP7 ch.	pp	lane	data
RX2/5	rx0/4		X0Y29	x	0x82	nc	65	-
RX2/8	rx0/7		X0Y30	x	0x84	nc	66	-
RX2/7	rx0/6		X0Y31	x	0x86	nc	67	-
RX2/10	rx0/9	218	X0Y32	5G	0x88	nc	68	-
RX2/9	rx0/8		X0Y33	5G	0x8A	nc	69	-
RX2/11	rx0/10		X0Y34	5G	0x8C	nc	70	-
RX2/12	rx0/11		X0Y35	5G	0x8E	nc	71	ZDC

7.2.3 GTH output connections

Table 32 contains the GTH output connections to MP7 MTP front connectors:

Table 32: GTH output connections

MTP48	minipod	quad	GTH ch.	GTH	MP7 ch.	pp	lane	data
TX1/1	tx3/0	118	X1Y35	10G	0x01	nc	0	-
TX1/2	tx3/1		X1Y34	10G	0x03	nc	1	-
TX1/3	tx3/2		X1Y33	10G	0x05	nc	2	-
TX1/4	tx3/3		X1Y32	10G	0x07	nc	3	-
TX1/5	tx3/4	117	X1Y31	10G	0x09	nc	4	-
TX1/6	tx3/5		X1Y30	10G	0x0b	nc	5	-
TX1/7	tx3/6		X1Y29	10G	0x0d	nc	6	-
TX1/8	tx3/7		X1Y28	10G	0x0f	nc	7	-
TX1/9	tx3/8	116	X1Y27	10G	0x11	nc	8	-
TX1/10	tx3/9		X1Y26	10G	0x13	nc	9	-
TX1/11	tx3/10		X1Y25	10G	0x15	nc	10	-
TX1/12	tx3/11		X1Y24	10G	0x17	nc	11	-
TX1/13	tx4/0	115	X1Y23	10G	0x19	nc	12	-
TX1/14	tx4/1		X1Y22	10G	0x1b	nc	13	-
TX1/15	tx4/2		X1Y21	10G	0x1d	nc	14	-
TX1/16	tx4/3		X1Y20	10G	0x1f	nc	15	-
TX1/17	tx4/4	114	X1Y19	10G	0x21	nc	16	readout (AMC13)
TX1/18	tx4/5		X1Y18	10G	0x23	nc	17	readout (AMC13)
TX1/19	tx4/6		X1Y17	10G	0x25	nc	18	readout (AMC13)
TX1/20	tx4/7		X1Y16	10G	0x27	nc	19	readout (AMC13)
TX1/21	tx4/8	113	X1Y15	10G	0x29	nc	20	readout (AMC13)
TX1/22	tx4/9		X1Y14	10G	0x2b	nc	21	readout (AMC13)
TX1/23	tx4/10		X1Y13	10G	0x2d	nc	22	readout (AMC13)
TX1/24	tx4/11		X1Y12	10G	0x2f	nc	23	readout (AMC13)
TX1/25	tx5/0	112	X1Y11	10G	0x31	nc	24	readout (AMC13)
TX1/26	tx5/1		X1Y10	10G	0x33	nc	25	readout (AMC13)
TX1/27	tx5/2		X1Y09	10G	0x35	nc	26	-
TX1/28	tx5/3		X1Y08	10G	0x37	nc	27	-
TX1/29	tx5/4	111	X1Y07	10G	0x39	nc	28	scouting
TX1/30	tx5/5		X1Y06	10G	0x3b	nc	29	scouting
TX1/31	tx5/6		X1Y05	10G	0x3d	nc	30	scouting
TX1/32	tx5/7		X1Y04	10G	0x3f	nc	31	scouting

Table 32: GTH output connections

MTP48	minipod	quad	GTH ch.	GTH	MP7 ch.	pp	lane	data
TX1/33	tx5/8	110	X1Y03	x	0x41	nc	32	-
TX1/34	tx5/9		X1Y02	x	0x43	nc	33	-
TX1/35	tx5/10		X1Y01	x	0x45	nc	34	-
TX1/36	tx5/11		X1Y00	x	0x47	nc	35	-
TX2/26	tx2/1	210	X0Y00	x	0x49	nc	36	-
TX2/25	tx2/0		X0Y01	x	0x4b	nc	37	-
TX2/28	tx2/3		X0Y02	x	0x4d	nc	38	-
TX2/27	tx2/2		X0Y03	x	0x4f	nc	39	-
TX2/30	tx2/5	211	X0Y04	x	0x51	nc	40	-
TX2/29	tx2/4		X0Y05	x	0x53	nc	41	-
TX2/32	tx2/7		X0Y06	x	0x55	nc	42	-
TX2/31	tx2/6		X0Y07	x	0x57	nc	43	-
TX2/34	tx2/8	212	X0Y08	x	0x59	nc	44	-
TX2/33	tx2/10		X0Y09	x	0x5b	nc	45	-
TX2/35	tx2/9		X0Y10	x	0x5d	nc	46	-
TX2/36	tx2/11		X0Y11	x	0x5f	nc	47	-
TX2/14	tx1/1	213	X0Y12	x	0x61	nc	48	-
TX2/13	tx1/0		X0Y13	x	0x63	nc	49	-
TX2/16	tx1/3		X0Y14	x	0x65	nc	50	-
TX2/15	tx1/2		X0Y15	x	0x67	nc	51	-
TX2/18	tx1/5	214	X0Y16	x	0x69	nc	52	-
TX2/17	tx1/4		X0Y17	x	0x6b	nc	53	-
TX2/20	tx1/7		X0Y18	x	0x6d	nc	54	-
TX2/19	tx1/6		X0Y19	x	0x6f	nc	55	-
TX2/22	tx1/9	215	X0Y20	x	0x71	nc	56	-
TX2/21	tx1/8		X0Y21	x	0x73	nc	57	-
TX2/23	tx1/10		X0Y22	x	0x75	nc	58	-
TX2/24	tx1/11		X0Y23	x	0x77	nc	59	-
TX2/2	tx0/1	216	X0Y24	x	0x79	nc	60	-
TX2/1	tx0/0		X0Y25	x	0x7b	nc	61	-
TX2/4	tx0/3		X0Y26	x	0x7d	nc	62	-
TX2/3	tx0/2		X0Y27	x	0x7f	nc	63	-
TX2/6	tx0/5	217	X0Y28	x	0x81	nc	64	-
TX2/5	tx0/4		X0Y29	x	0x83	nc	65	-
TX2/8	tx0/7		X0Y30	x	0x85	nc	66	-

Table 32: GTH output connections

MTP48	minipod	quad	GTH ch.	GTH	MP7 ch.	pp	lane	data
TX2/7	tx0/6		X0Y31	x	0x87	nc	67	-
TX2/10	tx0/9	218	X0Y32	x	0x89	nc	68	-
TX2/9	tx0/8		X0Y33	x	0x8b	nc	69	-
TX2/11	tx0/10		X0Y34	x	0x8d	nc	70	-
TX2/12	tx0/11		X0Y35	x	0x8f	nc	71	-

7.2.4 Data on GTHs

In Table 33 configuration of GTHs [7] for Global Trigger is shown⁴.

Table 33: Configuration of GTHs

Objects	Link	MGT	GTHE2	RX	TX
MU0..MU1	0	118	X1Y35	x	
MU2..MU3	1	118	X1Y34	x	
MU4..MU5	2	118	X1Y33	x	
MU6..MU7	3	118	X1Y32	x	
EG0..EG5	4	117	X1Y31	x	
EG6..EG11	5	117	X1Y30	x	
JET0..JET5	6	117	X1Y29	x	
JET6..JET11	7	117	X1Y28	x	
TAU0..TAU5	8	116	X1Y27	x	
TAU6..TAU11	9	116	X1Y26	x	
ESUMS	10	116	X1Y25	x	
CICADA	11	116	X1Y24	x	
EXT_COND[0:63]	12	115	X1Y23	x	
EXT_COND[64:127]	13	115	X1Y22	x	
EXT_COND[128:191]	14	115	X1Y21	x	
EXT_COND[192:255]	15	115	X1Y20	x	
free	16	114	X1Y19	x	
free	17	114	X1Y18	x	
free	18	114	X1Y17	x	
free	19	114	X1Y16	x	
free	20	113	X1Y15	x	
free	21	113	X1Y14	x	
free	22	113	X1Y13	x	
free	23	113	X1Y12	x	
ALGO_AFTER_GTLOGIC[0:191]	16	114	X1Y19		x
ALGO_AFTER_GTLOGIC[192:383]	17	114	X1Y18		x
ALGO_AFTER_GTLOGIC[383:511]	18	114	X1Y17		x
ALGO_AFTER_BXMASK[0:191]	19	114	X1Y16		x
ALGO_AFTER_BXMASK[192:383]	20	113	X1Y15		x
ALGO_AFTER_BXMASK[383:511]	21	113	X1Y14		x

⁴"MGT" means "MGT_BANK", "GTHE2" means "GTHE2_CHANNEL", "RX" means "GTH receiver", "TX" means "GTH transmitter"

Table 33: Configuration of GTHs

Objects	Link	MGT	GTHE2	RX	TX
ALGO_AFTER_BXMASK[0:191]	22	113	X1Y13		x
ALGO_AFTER_BXMASK[192:383]	23	113	X1Y12		x
ALGO_AFTER_BXMASK[383:511]	24	112	X1Y11		x
Bunchcounters, ...	25	112	X1Y10		x
SCOUTING	28	111	X1Y07		x
SCOUTING	29	111	X1Y06		x
SCOUTING	30	111	X1Y05		x
SCOUTING	31	111	X1Y04		x
ZDC	71	218	X0Y35	x	

7.3 Configuration of optical input links

Tables 34 and 35 show the configuration of optical links to Global Trigger.

Links 0..3 contain muon data from GMT, links 4..10 data from Calo-Layer2, link 11 data from Calo-Layer1 and links 12..15 external conditions from AMC502 boards.

Input data of links 0-12 (channels 0x00-0x18) are part of the readout record of AMC #1.

Table 34: Overview optical input links (part 1)

	link									
	0	1	2	3	4	5	6	7	8	9
ch. ->	0x00	0x02	0x04	0x06	0x08	0x0a	0x0c	0x0e	0x10	0x12
frame										
0	free	free	free	free	EG0	EG6	JET0	JET6	TAU0	TAU6
1	MU0 eta raw on bits [21:13] MU1 eta raw on bits [30:22]	MU2 eta raw on bits [21:13] MU3 eta raw on bits [30:22]	MU4 eta raw on bits [21:13] MU5 eta raw on bits [30:22]	MU6 eta raw on bits [21:13] MU7 eta raw on bits [30:22]	EG1	EG7	JET1	JET7	TAU1	TAU7
2	MU0 [31:00]	MU2 [31:00]	MU4 [31:00]	MU6 [31:00]	EG2	EG8	JET2	JET8	TAU2	TAU8
3	MU0 [63:32]	MU2 [63:32]	MU4 [63:32]	MU6 [63:32]	EG3	EG9	JET3	JET9	TAU3	TAU9
4	MU1 [31:00]	MU3 [31:00]	MU5 [31:00]	MU7 [31:00]	EG4	EG10	JET4	JET10	TAU4	TAU10
5	MU1 [63:32]	MU3 [63:32]	MU5 [63:32]	MU7 [63:32]	EG5	EG11	JET5	JET11	TAU5	TAU11

Table 35: Overview optical input links (part 2)

	link						
	10	11	12	13	14	15	71
ch. ->	0x14	0x16	0x18	0x1a	0x1c	0x1e	0x8e
frame							
0	ET, ETTEM, MBT0HFP	CICADA AD INT MSB on bits [31:28]	ExtCond [31:0]	ExtCond [95:64]	ExtCond [159:128]	ExtCond [223:192]	ZDC frame 0 0x7c/0x3c
1	HT, TOWERCOUNT, MBT0HFM	CICADA AD INT LSB on bits [31:28]	ExtCond [63:32]	ExtCond [127:96]	ExtCond [191:160]	ExtCond [255:224]	ZDC- 10 bits
2	ET _{miss} , ASYMET, MBT1HFP	CICADA AD DEC MSB on bits [31:28]	free	free	free	free	ZDC+ 10 bits
3	HT _{miss} , ASYMHT, MBT1HFM	CICADA AD DEC LSB on bits [31:28]	free	free	free	free	ZDC frame 3 0x0000
4	ET _{miss} ^{HF} , ASYMETHF, CENT[3:0]	free	free	free	free	free	ZDC counter 12 bits
5	HT _{miss} ^{HF} , ASYMHTHF, CENT[7:4]	free	free	free	free	free	ZDC frame 5 0x0000

7.4 Configuration of links to AMC13 (readout)

Table 36 shows the configuration of links from Global Trigger to AMC13 (readout). Links 16..24 contains algo data (after GTL, after BX mask and after prescalers), link 25 contains several counter values (currently not in readout record).

Table 36: Outputs to AMC13

	link									
	0	1	2	3	4	5	6	7	8	9
ch. ->	0x21	0x23	0x25	0x27	0x29	0x2b	0x2d	0x2f	0x31	0x33
frame										
0	algo_ after_ gtlogic [31:0]	algo_ after_ gtlogic [223:192]	algo_ after_ gtlogic [415:384]	algo_ after_ bxmask [31:0]	algo_ after_ bxmask [223:192]	algo_ after_ bxmask [415:384]	algo_ after_ prescaler [31:0]	algo_ after_ prescaler [223:192]	algo_ after_ prescaler [415:384]	tcm bunch counter
1	algo_ after_ gtlogic [63:32]	algo_ after_ gtlogic [255:224]	algo_ after_ gtlogic [447:416]	algo_ after_ bxmask [63:32]	algo_ after_ bxmask [255:224]	algo_ after_ bxmask [447:416]	algo_ after_ prescaler [63:32]	algo_ after_ prescaler [255:224]	algo_ after_ prescaler [447:416]	mp7 ttc bunch counter tcm
2	algo_ after_ gtlogic [95:64]	algo_ after_ gtlogic [287:256]	algo_ after_ gtlogic [479:448]	algo_ after_ bxmask [95:64]	algo_ after_ bxmask [287:256]	algo_ after_ bxmask [479:448]	algo_ after_ prescaler [95:64]	algo_ after_ prescaler [287:256]	algo_ after_ prescaler [479:448]	bunch counter for FDL
3	algo_ after_ gtlogic [127:96]	algo_ after_ gtlogic [319:288]	algo_ after_ gtlogic [511:480]	algo_ after_ bxmask [127:96]	algo_ after_ bxmask [319:288]	algo_ after_ bxmask [511:480]	algo_ after_ prescaler [127:96]	algo_ after_ prescaler [319:288]	algo_ after_ prescaler [511:480]	spare
4	algo_ after_ gtlogic [159:128]	algo_ after_ gtlogic [351:320]	32 bit hash of menu name	algo_ after_ bxmask [159:128]	algo_ after_ bxmask [351:320]	spare	algo_ after_ prescaler [159:128]	algo_ after_ prescaler [351:320]	veto + finor [0]	spare
5	algo_ after_ gtlogic [191:160]	algo_ after_ gtlogic [383:352]	32 bit hash of firmware uuid	algo_ after_ bxmask [191:160]	algo_ after_ bxmask [383:352]	spare	algo_ after_ prescaler [191:160]	algo_ after_ prescaler [383:352]	precale factor index [1]	spare

[0]: In this field, the finor and veto information is stored (1 bit each):

"00000000000000000000000000" & "0000000" & local_veto & "0000000" & local_finor.

The local_finor & local_veto are the values from the local MP7 uGT module.

[1]: In this field, the 8 bit prescale factor index is stored:

"00000000000000000000000000" & prescale_factor_index.

7.5 Optical patch panel

Figure 18 shows the connections on Global Trigger patch panels for optical links.

fiber cabling 28.2.2022																	
uGT Patchpanel #1: for production crate																	
MP7 slot1 & slot2 (modules 0 & 1)						MP7 slot3 & slot4 (modules 2 & 3)						MP7 slot5 & slot6 (modules 4 & 5)					
Fiber inputs @ uGT																	
Mu0	E00	Tau0	ExtCond0	Mu0	E00	Tau0	ExtCond0	Mu0	E00	Tau0	ExtCond0
Mu1	E01	Tau1	ExtCond1	Mu1	E01	Tau1	ExtCond1	Mu1	E01	Tau1	ExtCond1
Mu2	ext0	spare	ExtCond2	Mu2	ext0	spare	ExtCond2	Mu2	ext0	spare	ExtCond2
Mu3	ext1	spare	ExtCond3	Mu3	ext1	spare	ExtCond3	Mu3	ext1	spare	ExtCond3
Note that chips is marked by plastic clip & yellow strain relief														Note that chips is marked by plastic clip & yellow strain relief			
uGT Patchpanel #3: for test crate														Note that chips is marked by plastic clip & yellow strain relief			
Fiber inputs @ uGT																	
Mu0	E00	Tau0	ExtCond0	Mu0	E00	Tau0	ExtCond0	Mu0	E00	Tau0	ExtCond0
Mu1	E01	Tau1	ExtCond1	Mu1	E01	Tau1	ExtCond1	Mu1	E01	Tau1	ExtCond1
Mu2	ext0	spare	ExtCond2	Mu2	ext0	spare	ExtCond2	Mu2	ext0	spare	ExtCond2
Mu3	ext1	spare	ExtCond3	Mu3	ext1	spare	ExtCond3	Mu3	ext1	spare	ExtCond3
Note that chips is marked by plastic clip & yellow strain relief														Note that chips is marked by plastic clip & yellow strain relief			
SOT Strip														new Sydes fibre			

Figure 18: Global Trigger patch panels for optical links

Figure 19 shows the LC connectors on Global Trigger patch panels.

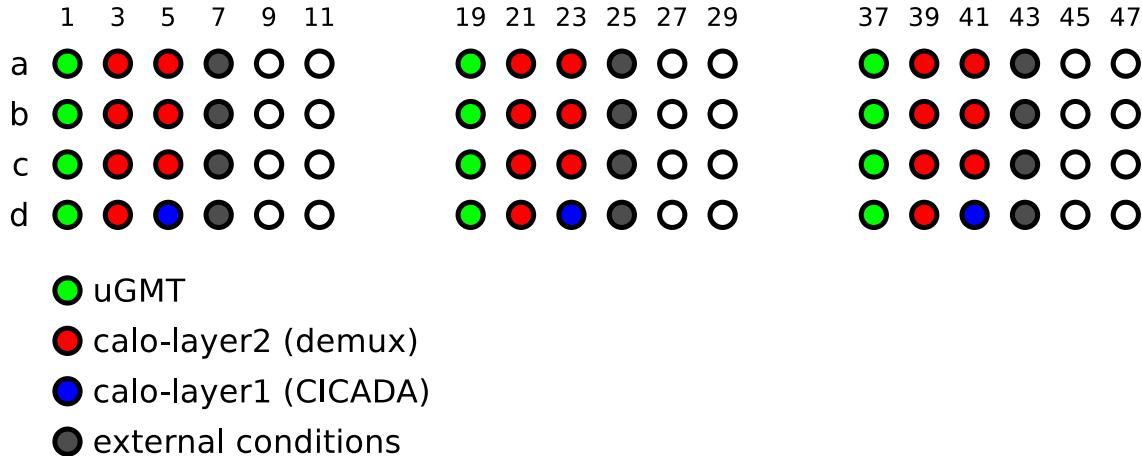


Figure 19: LC connectors on Global Trigger patch panels

The following Table 37 contains the optical patch panel ("uGT Patchpanel #1") connections for production crate⁵:

⁵"source" means "source of MTP48 cable to uGT", "uGMT" means "microTCA Global Muon Trigger module", "calo-layer2 (demux)" means "Calo-Layer2 demux module", "ext_cond" means "External condition AMC502 module", "fibre" means "fibre number of a MTP48 cable", "LC" means "LC number of optical patch panel", "MP7 slot" means "destination MP7 slot number of microTCA crate".

Table 37: uGT Patchpanel #1 (for production crate)

LC	source	fiber	data	MP7 slot
1/a	uGMT	1	MU0..MU1	1..2
1/b	uGMT	2	MU2..MU3	1..2
1/c	uGMT	3	MU4..MU5	1..2
1/d	uGMT	4	MU6..MU7	1..2
3/a	calo-layer2 (demux)	4b	EG0..EG5	1..2
3/b	calo-layer2 (demux)	4a	EG6..EG11	1..2
3/c	calo-layer2 (demux)	3b	JET0..JET5	1..2
3/d	calo-layer2 (demux)	3a	JET6..JET11	1..2
5/a	calo-layer2 (demux)	2b	TAU0..TAU5	1..2
5/b	calo-layer2 (demux)	2a	TAU6..TAU11	1..2
5/c	calo-layer2 (demux)	1b	ESUMS	1..2
5/d	calo-layer1		CICADA	1..2
7/a	ext_cond	Mod0 EXT0	ExtCond[0..63]	1..2
7/b	ext_cond	Mod0 EXT1	ExtCond[64..127]	1..2
7/c	ext_cond	Mod0 EXT2	ExtCond[128..191]	1..2
7/d	ext_cond	Mod0 EXT3	ExtCond[192..255]	1..2
19/a	uGMT	5	MU0..MU1	3..4
19/b	uGMT	6	MU2..MU3	3..4
19/c	uGMT	7	MU4..MU5	3..4
19/d	uGMT	8	MU6..MU7	3..4
21/a	calo-layer2 (demux)	12b	EG0..EG5	3..4
21/b	calo-layer2 (demux)	12a	EG6..EG11	3..4
21/c	calo-layer2 (demux)	11b	JET0..JET5	3..4
21/d	calo-layer2 (demux)	11a	JET6..JET11	3..4
23/a	calo-layer2 (demux)	10b	TAU0..TAU5	3..4
23/b	calo-layer2 (demux)	10a	TAU6..TAU11	3..4
23/c	calo-layer2 (demux)	9b	ESUMS	3..4
23/d	calo-layer1		CICADA	3..4
25/a	ext_cond	Mod1 EXT0	ExtCond[0..63]	3..4
25/b	ext_cond	Mod1 EXT1	ExtCond[64..127]	3..4
25/c	ext_cond	Mod1 EXT2	ExtCond[128..191]	3..4
25/d	ext_cond	Mod1 EXT3	ExtCond[192..255]	3..4
37/a	uGMT	9	MU0..MU1	5..6
37/b	uGMT	10	MU2..MU3	5..6
37/c	uGMT	11	MU4..MU5	5..6
37/d	uGMT	12	MU6..MU7	5..6

Table 37: uGT Patchpanel #1 (for production crate)

LC	source	fiber	data	MP7 slot
39/a	calo-layer2 (demux)	8b	EG0..EG5	5..6
39/b	calo-layer2 (demux)	8a	EG6..EG11	5..6
39/c	calo-layer2 (demux)	7b	JET0..JET5	5..6
39/d	calo-layer2 (demux)	7a	JET6..JET11	5..6
41/a	calo-layer2 (demux)	18b	TAU0..TAU5	5..6
41/b	calo-layer2 (demux)	18a	TAU6..TAU11	5..6
41/c	calo-layer2 (demux)	17b	ESUMS	5..6
41/d	calo-layer1		CICADA	5..6
43/a	ext_cond	Mod2 EXT0	ExtCond[0..63]	5..6
43/b	ext_cond	Mod2 EXT1	ExtCond[64..127]	5..6
43/c	ext_cond	Mod2 EXT2	ExtCond[128..191]	5..6
43/d	ext_cond	Mod2 EXT3	ExtCond[192..255]	5..6

The following Table 38 contains the optical patch panel ("uGT Patchpanel #3") connections for test crate⁵:

Table 38: uGT Patchpanel #3 (for test crate)

LC	source	fiber	data	MP7 slot
1/a	uGMT	13	MU0..MU1	5..6
1/b	uGMT	14	MU2..MU3	5..6
1/c	uGMT	15	MU4..MU5	5..6
1/d	uGMT	16	MU6..MU7	5..6
3/a	calo-layer2 (demux)	16b	EG0..EG5	5..6
3/b	calo-layer2 (demux)	16a	EG6..EG11	5..6
3/c	calo-layer2 (demux)	15b	JET0..JET5	5..6
3/d	calo-layer2 (demux)	15a	JET6..JET11	5..6
5/a	calo-layer2 (demux)	14b	TAU0..TAU5	5..6
5/b	calo-layer2 (demux)	14a	TAU6..TAU11	5..6
5/c	calo-layer2 (demux)	13b	ESUMS	5..6
5/d	calo-layer1		CICADA	5..6
7/a	ext_cond	Mod3 EXT0	ExtCond[0..63]	5..6
7/b	ext_cond	Mod3 EXT1	ExtCond[64..127]	5..6
7/c	ext_cond	Mod3 EXT2	ExtCond[128..191]	5..6
7/d	ext_cond	Mod3 EXT3	ExtCond[192..255]	5..6
19/a	uGMT	17	MU0..MU1	1..2

Table 38: uGT Patchpanel #3 (for test crate)

LC	source	fiber	data	MP7 slot
19/b	uGMT	18	MU2..MU3	1..2
19/c	uGMT	19	MU4..MU5	1..2
19/d	uGMT	20	MU6..MU7	1..2
21/a	calo-layer2 (demux)	26	EG0..EG5	1..2
21/b	calo-layer2 (demux)	25	EG6..EG11	1..2
21/c	calo-layer2 (demux)	28	JET0..JET5	1..2
21/d	calo-layer2 (demux)	27	JET6..JET11	1..2
23/a	calo-layer2 (demux)	30	TAU0..TAU5	1..2
23/b	calo-layer2 (demux)	29	TAU6..TAU11	1..2
23/c	calo-layer2 (demux)	32	ESUMS	1..2
23/d	calo-layer1		CICADA	1..2
25/a	ext_cond	Mod4 EXT0	ExtCond[0..63]	1..2
25/b	ext_cond	Mod4 EXT1	ExtCond[64..127]	1..2
25/c	ext_cond	Mod4 EXT2	ExtCond[128..191]	1..2
25/d	ext_cond	Mod4 EXT3	ExtCond[192..255]	1..2
37/a	uGMT	21	MU0..MU1	3..4
37/b	uGMT	22	MU2..MU3	3..4
37/c	uGMT	23	MU4..MU5	3..4
37/d	uGMT	24	MU6..MU7	3..4
39/a	calo-layer2 (demux)	34	EG0..EG5	3..4
39/b	calo-layer2 (demux)	33	EG6..EG11	3..4
39/c	calo-layer2 (demux)	35	JET0..JET5	3..4
39/d	calo-layer2 (demux)	36	JET6..JET11	3..4
41/a	calo-layer2 (demux)	14	TAU0..TAU5	3..4
41/b	calo-layer2 (demux)	13	TAU6..TAU11	3..4
41/c	calo-layer2 (demux)	16	ESUMS	3..4
41/d	calo-layer1		CICADA	3..4
43/a	ext_cond	Mod5 EXT0	ExtCond[0..63]	3..4
43/b	ext_cond	Mod5 EXT1	ExtCond[64..127]	3..4
43/c	ext_cond	Mod5 EXT2	ExtCond[128..191]	3..4
43/d	ext_cond	Mod5 EXT3	ExtCond[192..255]	3..4

7.6 External condition patch panel

The connections of external conditions (technical trigger) on patchpanel are listed below. Currently only AMC502 slot 12 is used for conversion to optical, therefore only 64 bits (of 256) are possible.

- Patch panel #0:
 - CON0:
 - * RJ45 #1: BPTX - TRIG 4 beamgas
(1-2: BPTX_BeamGas_Ref1_VME, 3-4: BPTX_BeamGas_Ref2_VME, 5-6: BPTX_BeamGas_B1_VME, 7-8: BPTX_BeamGas_B2_VME)
 - * RJ45 #2: BPTX - TRIG0 LOGS0
(1-2: ZeroBias_BPTX_AND_VME, 3-4: BPTX_B1_VME, 5-6: BPTX_B2_VME, 7-8: BPTX_OR_VME)
 - * RJ45 #3: BPTX - TRIG1 LOGS1
(1-2: BPTX_AND_Ref1_VME, 3-4: BPTX_B1NotB2_VME, 5-6: BPTX_B2NotB1_VME, 7-8: BPTX_NotOR_VME)
 - * RJ45 #4: empty
 - * RJ45 #5: BPTX - FST COL BCH / TECH TRG
(1-2: BPTX_AND_Ref3_VME, 3-4: BPTX_OR_Ref3_VME, 5-6: BPTX_RefAND_VME, 7-8: BPTX_FirstCollidingBunch_VME)
 - * RJ45 #6: BPTX - TRIG2 PRECOLL
(1-2: BPTX_AND_Ref4_VME, 3-4: BPTX_OR_Ref4_VME, 5-6: BPTX_LastCollisionInTrain, 7-8: BPTX_FirstCollisionInTrain)
 - * RJ45 #7: empty
 - * RJ45 #8: empty
 - CON1: (AMC502 slot 11 not used currently)
 - * all empty
 - CON2: (AMC502 slot 10 not used currently)
 - * all empty
 - CON3: (AMC502 slot 9 not used currently)
 - * all empty
- Patch panel #1:
 - CON0:
 - * RJ45 #1: HCAL - HCAL Laser
(1-2: HCAL_LaserMon_1, 3-4: HCAL_LaserMon_2, 5-6: HCAL_LaserMon_3, 7-8: HCAL_LaserMon_4)
 - * RJ45 #2: ZDC - reserved for ZDC
(1-2: ZDC1nM, 3-4: not used, 5-6: not used, 7-8: ZDC1nP)
 - * RJ45 #3: TOTEM - TOT trigger to CMS
(1-2: TOTEM_1, 3-4: TOTEM_2, 5-6: TOTEM_3, 7-8: TOTEM_4)
 - * RJ45 #4: ZDC - reserved for ZDC
(1-2: ZDC2nM, 3-4: not used, 5-6: not used, 7-8: ZDC2nP)
 - * RJ45 #5: empty

- * RJ45 #6: ZDC - reserved for ZDC
(1-2: ZDC3nM, 3-4: not used, 5-6: not used, 7-8: ZDC3nP)
- * RJ45 #7: CASTOR (obsolete)
(1-2: CASTOR_1, 3-4: CASTOR_2, 5-6: CASTOR_3, 7-8: CASTOR_4)
- * RJ45 #8: empty
- CON1: (AMC502 slot 11 not used currently)
 - * all empty
- CON2: (AMC502 slot 10 not used currently)
 - * all empty
- CON3: (AMC502 slot 9 not used currently)
 - * all empty

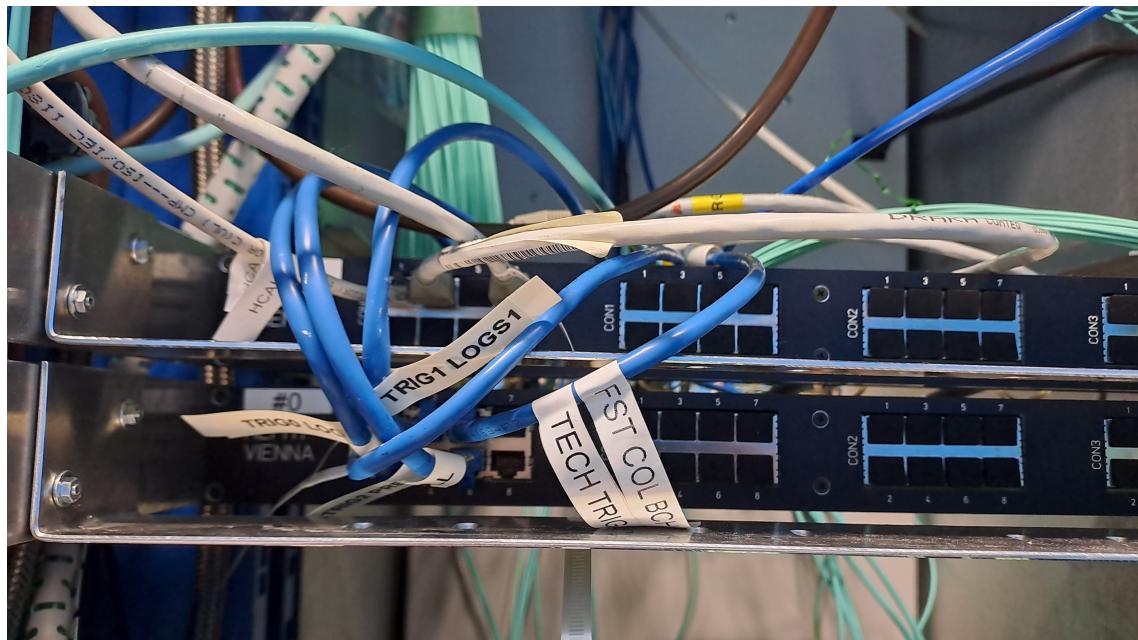


Figure 20: External condition patch panel (picture date: September 12, 2023)

8 Glossary

electron/ γ = electron/gamma objects over Calo-Layer2 (VHDL: eg)

jet = jet objects over Calo-Layer2 (VHDL: jet)

tau = tau objects over Calo-Layer2 (VHDL: tau)

muon = muon objects over μ GMT (VHDL: muon)

ET = Scalar sum of transverse energy components over Calo-Layer2 (VHDL: ett)

ETTEM = Scalar sum of transverse energy components from ECAL only over Calo-Layer2
(VHDL: ettem)

MBTxHFy = Minimum bias HF bits (VHDL: MBT0HFP, MBT0HFM, MBT1HFP, MBT1HFM)

HT = Magnitude of the vectorial sum of transverse energy of jets (hadronic) over Calo-Layer2
(VHDL: htt)

TOWERCOUNT = tower counts (VHDL: towercount)

ET_{miss} = 2-vector sum of transverse energy over Calo-Layer2 (VHDL: etm)

HT_{miss} = Missing Total transverse energy of jets over Calo-Layer2 (VHDL: htm)

ET_{miss}^{HF} = 2-vector sum of transverse energy including HF over Calo-Layer2 (VHDL: etmhf)

HT_{miss}^{HF} = Missing Total transverse energy of jets including HF over Calo-Layer2 (VHDL:
htmhf)

ASYMET = Asymmetry of ET over Calo-Layer2 (VHDL: asymet)

ASYMHT = Asymmetry of HT over Calo-Layer2 (VHDL: asymht)

ASYMETHF = Asymmetry of ET including HF over Calo-Layer2 (VHDL: asymethf)

ASYMHHTF = Asymmetry of HT including HF over Calo-Layer2 (VHDL: asymhthf)

CENTx = Centrality bits [7:0] over Calo-Layer2 (VHDL: cent7, cent6, ...)

p_T = transverse momentum of muon objects(VHDL: pt)

E_T = energy of calorimeter objects (VHDL: et)

η = pseudo-rapidity position (VHDL: eta)

φ = azimuth angle position (VHDL: phi)

isolation = isolation information (VHDL: iso)

quality = quality information (VHDL: qual)

charge = charge information of muon objects (VHDL: ch)

unconstrained p_T = transverse momentum of muon objects (VHDL: `upt`)

impact parameter = impact parameter information of muon objects (VHDL: `ip`)

hadronic shower = hadronic shower (muon shower [mus]) information, on bit 61 of MU0, MU2, MU3, MU4 and MU6 (VHDL: `mus0`, `mus1`, `mus2`, `musoot0`, `musoot1`)

DISP = displaced bit of jet objects (VHDL: `disp`)

index bits = index bits of muon objects - currently not used

9 Acronyms

AMC13 AMC board in uTCA crate for several features (readout, ...)

DAQ Data Acquisition

FDL Final Decision Logic Module

GCT Calorimeter Trigger Layer-2

GMT Global Muon Trigger

GT Global Trigger

GTL Global Trigger Logic Module

ROP Readout Process Module

TCM Timing Counter Manager Module

TCDS Trigger, Control and Distribution System

TDF Test and Development Framework

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