# FPGA Implementation of the Fast Fourier Transform

Garrett Massman and Cory Walker

December 2, 2014

# Introduction

In this project we implemented a fast Fourier transform algorithm on a Xilinx FPGA using VHDL. The primary motivation of our project was to digitally analyze musical signals, but the use cases for an FFT chip far surpass that specific use case.

As a very general overview, our completed device functions by sampling an analog signal for a set amount of time and storing the data into an input buffer in BRAM. Next, the signal is is processed using an FT controller and a complex ALU and stored in an output buffer. Finally, a microcontroller can then read the output buffer over a standard SPI protocol. From there the processed frequency domain data can be sent to a computer for further processing or any other device.

# Theory

To understand the discrete Fourier transform, one must first analyze its analogous continuous time form. This is written most simply as

$$X(j\omega) = \int_{-\infty}^{\infty} x(t)e^{-j\omega t} \, dt$$

which defines the transform of a continuous time signal $f(t)$. Without getting into too many details, it defines the signal as a combination of sinusoids, making it a very useful tool for real world applications.

The discrete Fourier transform (DFT) is simply a reduction of the continuous Fourier transform into a discrete sample space. In other words, if we let $x_n$ represent a sampled version of the continuous time function $x(t)$ with a total of $N$ samples, we can replace the integral with a summation over the series, as shown below.

$$X_k = \sum_{n=0}^{N-1} x_n e^{\frac{-j2\pi kn}{N}}$$

As with the continuous time case, this series gives us a glimpse into the component elements of our original signal. However, it is rather costly to

compute, requiring a time complexity of $O(N^2)$. For each value $X_k$, a series of values from $n = 0$ to $N-1$ must be generated and summed, using up valuable computer resources. Thus, calculating the DFT in this way is very inefficient, so we instead turn to the Fast Fourier transform.

In order to perform this operation more quickly, we utilized the Cooley-Tukey FFT algorithm implemented through the Xilinx CoreGen FFT module. One requirement is that our input is strictly a power of 2. That is because the algorithm works by recursively finding the FFT of smaller and smaller sample sizes of $x_n$, which arises from the fact that the transform itself is periodic. The transform function can be broken into the sum of its even and odd components,

$$X_k = \sum_{m=0}^{N/2-1} x_{2m} e^{-\frac{2\pi i}{N}(2m)k} + \sum_{m=0}^{N/2-1} x_{2m+1} e^{-\frac{2\pi i}{N}(2m+1)k}$$

This equation can further be simplified by making the substitutions

$$E_k = \sum_{m=0}^{N/2-1} x_{2m} e^{-\frac{2\pi i}{N}(2m)k} \qquad\qquad O_k = \sum_{m=0}^{N/2-1} x_{2m+1} e^{-\frac{2\pi i}{N/2}mk}$$

giving us

$$X_k = E_k + e^{-\frac{2\pi i}{N}k} O_k$$

The expression $e^{-\frac{2\pi i}{N}k}$ is commonly called the *twiddle factor*. Furthermore, because of the periodicity of the transform, we can calculate respective even and odd components simultaneously

$$E_k = E_{k+\frac{N}{2}} \qquad\qquad O_k = O_{k+\frac{N}{2}}$$

## Motivation

The FFT is a very common operation used in many digital signal processing tasks. Digital signal processors are usually very highly tuned to perform a series of dedicated tasks quickly, and have very little flexability in the way of general purpose usage. This is both a blessing and a curse, as they rarely need to be reprogrammed, but are also limited to the range of tasks they

can accomplish. High end DSPs utilize parallelism to complete mathematical calculations quickly. Because of their dedicated nature, DSPs also tend to be rather costly, upwards of $32 for a SHARC model chip from Analog Electronics.

FPGAs are primarily a large collection of configurable logic blocks that can be wired together to run in parallel, so why not try and use one in place of an expensive DSP? By taking the heavy computations off of a typical CPU and putting the burden onto an FPGA, the processor could be freed up to execute any number of instructions until the final computations are complete. This hybrid model has actually become quite popular in the past several years, and several products such as some of Intel's Xeon chips have FPGAs integrated onboard. This can offset the costs for companies who formerly may have been inclined to build expensive ASICs and instead shift their focus onto a new platform. A parallel CPU/FPGA integrated system is beyond the scope of this project, but instead a simple model using a Digilent Basys board and an Arduino are built to illustrate the principles.

## System Overview

A critical task in building our FFT device was converting an arbitrary waveform into the SPI signal input that the FPGA expected. This requires the use of a fast analog to digital converter. The Xilinx Spartan 3E FPGA does not come with an onboard ADC. Because of this, a large percentage of the work was actually electronics work done outside of the FPGA:
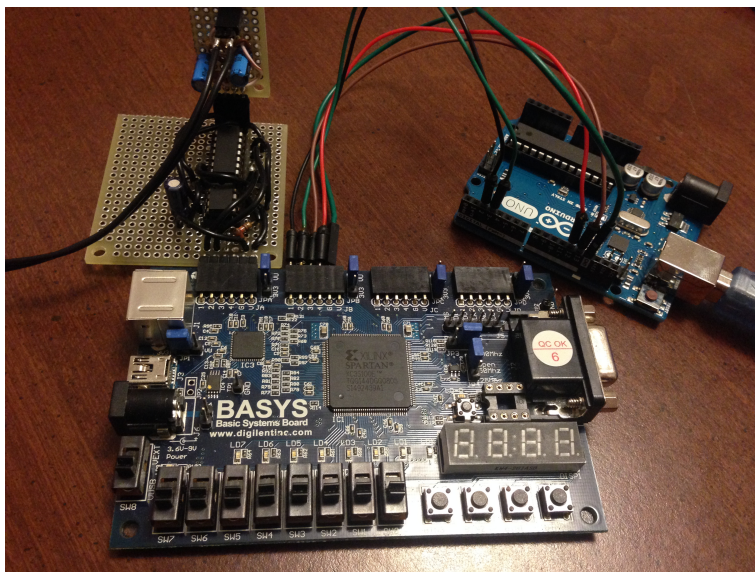
Figure 1: Full system including ADC PMOD and audio signal module.

These external components condition the signal and then send the digital signal into the FPGA at the right voltage level. In addition, the FPGA's output buffer must be read out by an Arduino microcrontroller and sent to a computer with the right software to parse and display the output. We call these external components macro-components and we call the FPGA internal blocks micro-components.

# Macro-Component Descriptions

The required components external to the FPGA are as follows:
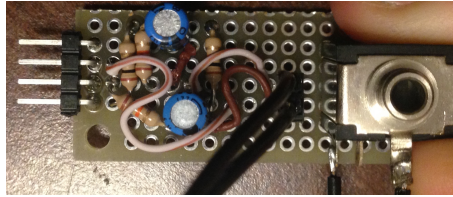
## Audio signal module



Figure 2: Audio signal circuit board with audio connector

The audio signal module tailors the input audio signal for conversion with the ADC. Traditional audio signals are centered around 0 V and are in the negative voltage range half the time. This module biases the signal by 2.5 V, allowing for a 5 V variation peak to peak in the audio signal without any clipping. This module also provides filtering capacitors that remove most of the supply rail noise that may be present.
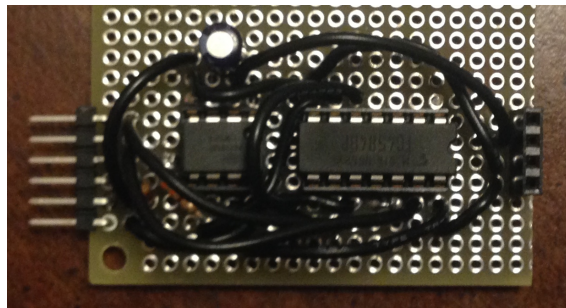
## ADC PMOD



Figure 3: ADC PMOD circuit board

The ADC PMOD accepts any input analog input and converts it to a SPI bus that the FPGA can read. The analog signal is fed into the onboard ADS7818 chip. Unfortunately, this chip operates at 5 V but the FPGA operates at 3.3 V. Because of this, there is a voltage divider to drop the voltage down to the FPGA. For FPGA output to be read by the ADS7818, we added a Schmitt inverter IC wired as a Schmitt trigger to act as a level converter.

## Arduino

The Arduino functions as a means of getting the processed information out of the FPGA's BRAM. The Arduino turned out to be the main bottleneck in terms of framerate to the computer's display. We had to push the SPI and serial write functions outside of recommended bounds to get a fluid framerate on the computer display. The full software is available in the `arduino/osc_binary_spi` directory of the source code repository.

## Computer software

The computer software for this project is divided into two components. The first component is the Python module that facilitates the reading and decoding of the data from the serial port. It will read out 512 complex numbers and, optionally, compute the magnitude of each of those numbers. The second component is the actual display. It will use the Python module to read the device and it uses Tkinter to display the plot on the screen.

# Micro-Component Descriptions

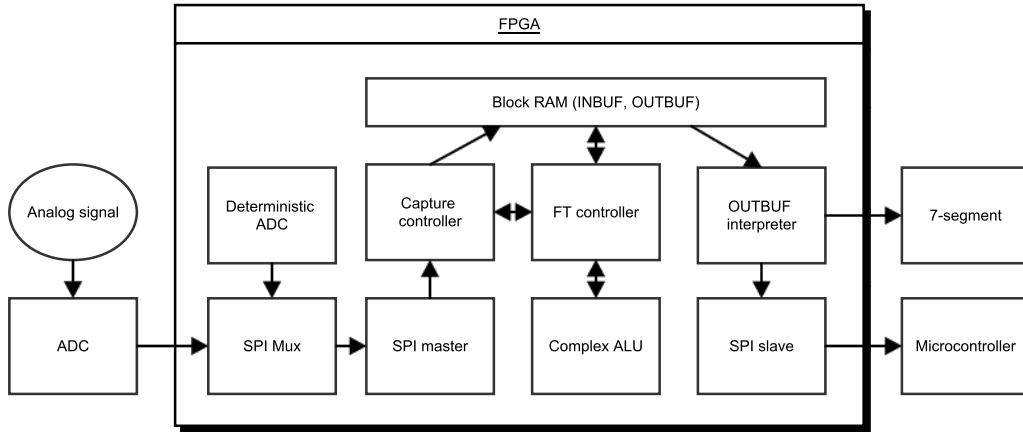The final block diagram of our device is as follows:



Figure 4: Block diagram of the FFT chip

All of the blocks inside the FPGA device are referred to as micro-components.

TODO: DESCRIPTION OF EACH COMPONENT HERE

# Steps Taken

# Simulation Results

# Results

# Roadblocks

# Future Improvements

# Conclusion

# Appendix

# References

[1] Doin, Jonny. *SPI Master/Slave Interface.* OpenCores, 16 May 2011. Web. 13 Sept. 2014. <`http://opencores.org/project,spi_master_slave`>.

[2] Reynwar, Ben. *FFT on an FPGA.* FFT on an FPGA. N.p., n.d. Web. 13 Sept. 2014. <`http://www.reynwar.net/ben/docs/fft_dit/index.html`>.

[3] Roberts, Michael J. *Signals and Systems: Analysis Using Transform Methods and MATLAB.* New York: McGraw Hill, 2012. Print.

[4] Satoh, Keiichi, Jubee Tada, Kenta Yamaguchi, and Yasutaka Tamura. *Complex Multiplier Suited for FPGA Structure.* Computers and Communications (2008): 341-44. Web. 13 Sept. 2014.

[5] Wikipedia contributors. *Cooley–Tukey FFT algorithm.* Wikipedia, The Free Encyclopedia. Wikipedia, The Free Encyclopedia, 27 Jun. 2014. Web. 13 Sep. 2014.

[6] Wikipedia contributors. *Discrete Fourier transform.* Wikipedia, The Free Encyclopedia. Wikipedia, The Free Encyclopedia, 2 Sep. 2014. Web. 13 Sep. 2014.