CMPE 2020A TEST 3: Open book open notes.

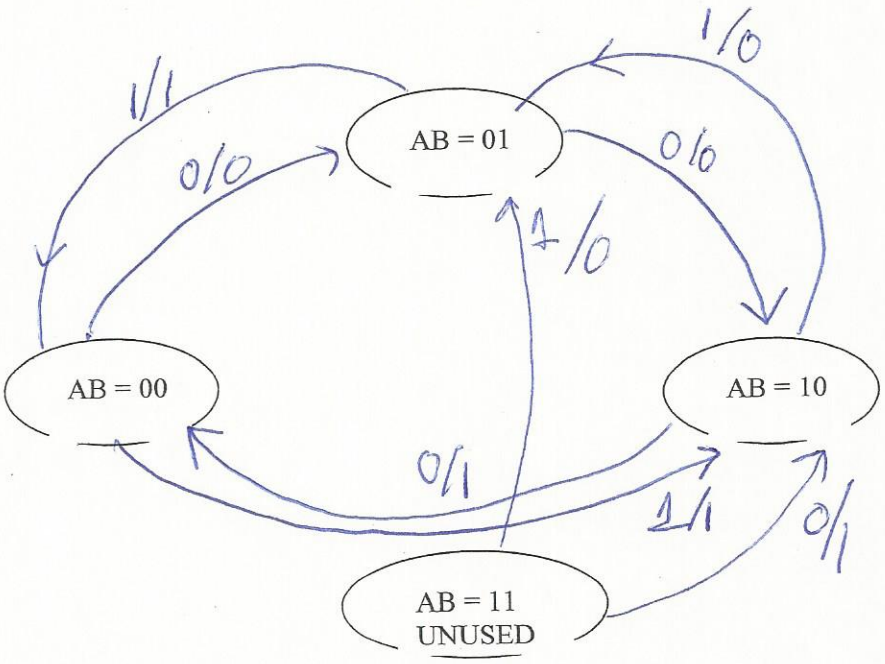
NAME:
GT ID #:

SOLUTIONS

Prob 1 (10 points):
The state transition table of a 3-state FSM (2 flip flops) is given below. The state AB = 11 is unused.

Present State = A(t),B(t)		Input = I	Next State = A(t+1), B(t+1)		Output=Z
0	0	0	0	1	0
0	0	1	1	0	1
0	1	0	1	0	0
0	1	1	0	0	1
1	0	0	0	0	1
1	0	1	0	1	0
1	1	0	X (1)	X (0)	X (1)
1	1	1	X (0)	X (1)	X (0)

(a) Draw its state transition diagram below.



(b) You are to design a finite state machine that realizes the above state transition diagram/state transition with D flip flops. Below, fill in the K-maps for D(A), D(B) and Z (see figure on next page) and write the miminal Boolean expressions for the same. *Make sure that the machine is not caught in a self-loop* if it starts up in the state AB=11.

A \ BI	00	01	11	10
0	0	1	0	1
1	0	0	X	X

D(A) = $\bar{A}\bar{B}I + B\bar{I}$

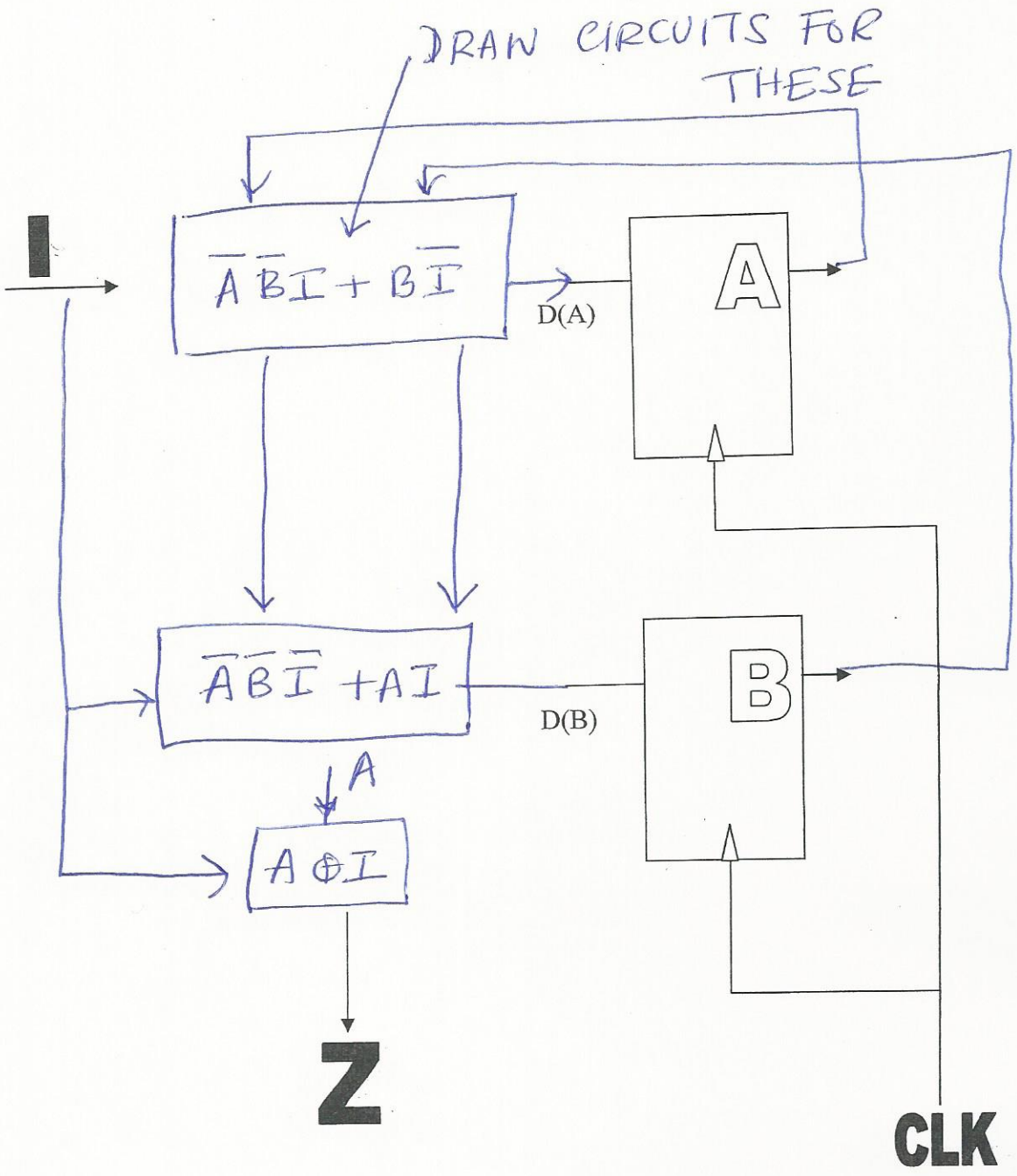
A \ BI	00	01	11	10
0	1	0	0	0
1	0	1	X	X

D(B) = $\bar{A}\bar{B}\bar{I} + AI$

A \ BI	00	01	11	10
0	0	1	0	0
1	1	0	X	X

Z = $\bar{A}I + A\bar{I}$

(c) Draw a circuit diagram for the finite state machine showing all logic, FSM input and output and the two D flip flops corresponding to A and B.



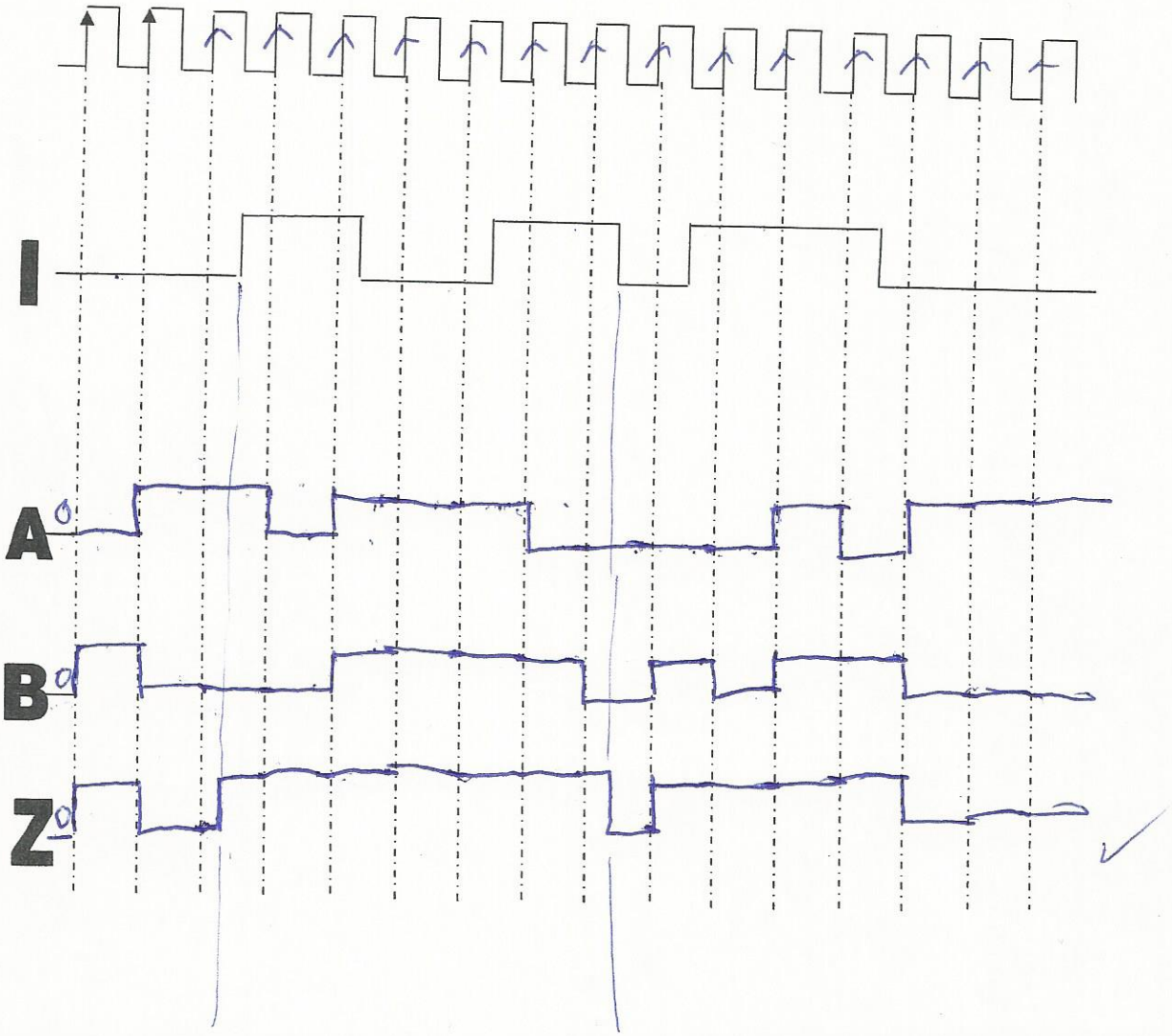
Prob 2. (10 points)
A FSM has two flip flops with outputs A and B and inputs D(A) and D(B) respectively (as in the previous problem, part (c)). The FSM has an input I and one output Z (as in the previous problem). The equations for the FSM are given below. The flip flops are **positive edge** triggered.

$D(A) = (A + B) \oplus I$ ($\oplus$ = XOR, XOR = exclusive OR)

$D(B) = \overline{A} \oplus B$ (note again, D(B) = ((A bar) XOR B) !)

$Z = B + I$

Initially, at t=0, A(0) = B(0) = 0.
Draw the waveforms for the outputs of the flip flops corresponding to A and B and the output Z below, given the waveform for the input I.



Prob 3 (10 points)

Consider the following truth table of 4 input variables.

W	X	Y	Z	F = f(W,X,Y,Z)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

WY = 00

XZ	F
00	0
01	1
10	1
11	0

$F = X \oplus Z$

WY = 01

XZ	F
00	1
01	0
10	0
11	0

$F = \overline{(X+Z)}$

WY = 10

XZ	F
00	1
01	1
10	1
11	0

$F = \overline{X \cdot Z}$

WY = 11

XZ	F
00	0
01	1
10	0
11	0

$F = \overline{X}Z$

You are to realize this truth table using a 4-to-1 mux with control signals connected to W and Y (see Figure) and additional logic whose inputs are driven by the signals X and Z. Please draw your circuit (additional logic) below and show all steps.