ECE 410, Spring 2017
Introduction to VLSI Design

Lecture: MWF, 11:30 12:20, Room 2243 EB

Instructor: Dr. Fathi M. Salem, Office: 2308D EB, Email: salem@egr.msu.edu

Office Hrs.: M Tu W 1:00-2: p.m. or via D2L- email appointments

TA & Lab (NO LAB THE FIRST TWO WEEKS)

TA: Patrick O'hara (Email: oharapa1@msu.edu)

TA Office Hours: Lab times plus other times to be announced

Reserved Labs in rm 2314 (Th.: 3-6pm), and rm 2200 EB (Th.: 7-9). They are RESEVED for the labs of ECE 410 students during this semester.

LAB Room 2314 EB/2200 EB* (Unix Machines)

*OPEN LAB CONCEPT: You may work on your assignments in any available UNIX lab, at any time you wish. The Lab times are when the TA will be available to answer your questions.

Course Website: This Semester, we will use the D2Lmanagement website via (https://d2l.msu.edu). We may have a direct class website as well.

Prerequisite: ECE 230, 302, and 303

Recommended Text: (Not required but recommended. I will ask the Main Library to have a copy of reserve)
J. Uyemura, Introduction to VLSI Circuits and Systems, Wiley, 2002. ISBN 0-471-12704-3.

From The Catalog Description:

Integrated circuit design fundamentals. Design specifications: functionality, performance, reliability, manufacturability, testability, cost. Standards, silicon compilers, foundries. Design layout rules, rule checking. Circuit extraction, simulation, verification. Team-based design.

Attendance and Conduct in Class:

"Students are expected to attend class and be bright and cheerful with lots of questions and ideas." It will be hard to do well in this class without attending the lectures, taking quizzes, homework and Exams. It is the student's responsibility to get notes and handouts for any missed class. Lecture notes, HWs, and handouts have and will be posted on D2L frequently.

Grading:

35% Two Midterm Exams (Exam I:15%, Exam II: 20%) (Dates: Friday, 02/17/17 and Friday, 03/31/17)
15% Homework *
5% Quizzes (or Check-ins)*
20% Lab Assignments (Lab 1-7)*
25% (Labs 8-10) Group Lab Project (15%) and final project Lab demo (10%)*
**** must obtain a passing grade of 60% or better to pass the course***

The Final Exam on Thursday, May 4, 2017, 10-noon-- this time may be used for team project presentations. There will be an in-lab test of skills learned in lab assignments and the design project demo. There will be up to ten homework

assignments. Homework assignments will be due weekly turned in before class on the due date. Approximately 5-10, 5-minute quizzes/Check-ins may be given during class on random days.

Lab Assignments and Lab Project:

Lab Assignments using Cadence VLSI design software (available in all Engineering UNIX labs) will be an integral part of this course. ***There are no set lab times***, but the UNIX lab in EB 1312 (tentative) has been reserved for ECE410 during several 3-hour blocks. During these times the TA will be available to help answer questions. Details of each assignment will be posted on the course via the class website or D2L. Each student will have a UNIX class directory at ***/classes/ece410/username***.

Each Lab Assignment will have specific deliverables which must be turned-in by 10 pm on Thursday of the week due. There will be approximately 8 lab assignments (possibly 6 individual and 2 group) and a 2-part group lab project with a report. Lab assignments will be assigned and due weekly with a brief lab report required for each lab. Grades will be evaluated by your TA and are 80% based on the quality of your work and 20% on the completeness of your report. The lab project will be done in 3-4 person groups and grades will be assigned according to the following breakdown.

10% Proposal 20% Phase A 30% Phase B 15% Individual 25% Report

Other Policies:

- Cheating in any form will not be tolerated! This includes copying homework, copying circuit design files, cheating on exams, or any other form of unethical behavior.
- There is no makeup for missed quizzes. If you have an excusable absence and notify the instructor by email before class begins, missed quizzes will not count against your grade.
- Homework can be done in groups but must be turned in individually. Direct copying of homework will result in a zero-point score for all people involved.
- Homework must be turned in at the beginning of class on the date it is due (generally Mondays). ***No late homework will be accepted.***
- Lab Assignment must be turned-in by 10pm on Thursday of the week due. Timestamps on CAD files will be checked to ensure work was completed on time.
- Makeup exams will only be allowed for written excused absences and only when the instructor is informed before the exam. Makeup exams will be oral exams given after the exam date.