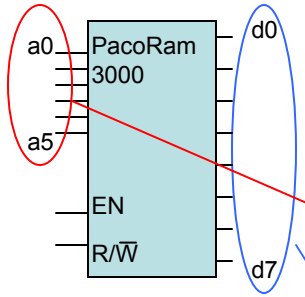
Designing a memory bank



- Suppose we're working with this chip

- What is the memory capacity?

- First, look at the number of address lines

- 6 address lines implies 2^6=64 addresses in the chip

- Now look at the number of data lines

- 8 data lines implies 8 bits (1 byte) per address

- Hence, this chip can hold 64 bytes of memory

- Typically the chip will be labeled 64 x 8, meaning 64 addresses, 8 bits per address.

Problem:

Design a memory bank with 256 bytes of memory
using the PacoRam3000 chips and decoders

- First question: How many memory chips we need?

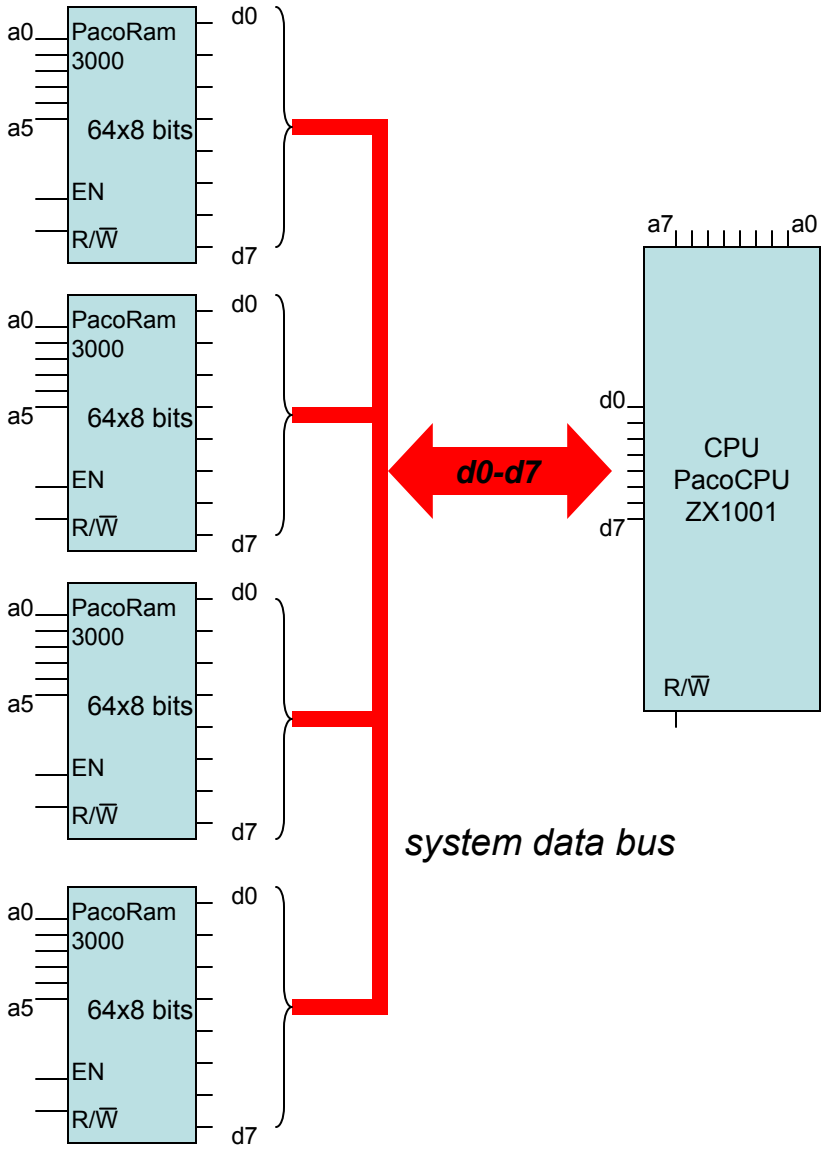
  4 – 64 bytes * 4 = 256 bytes

- What type of decoder will we use?

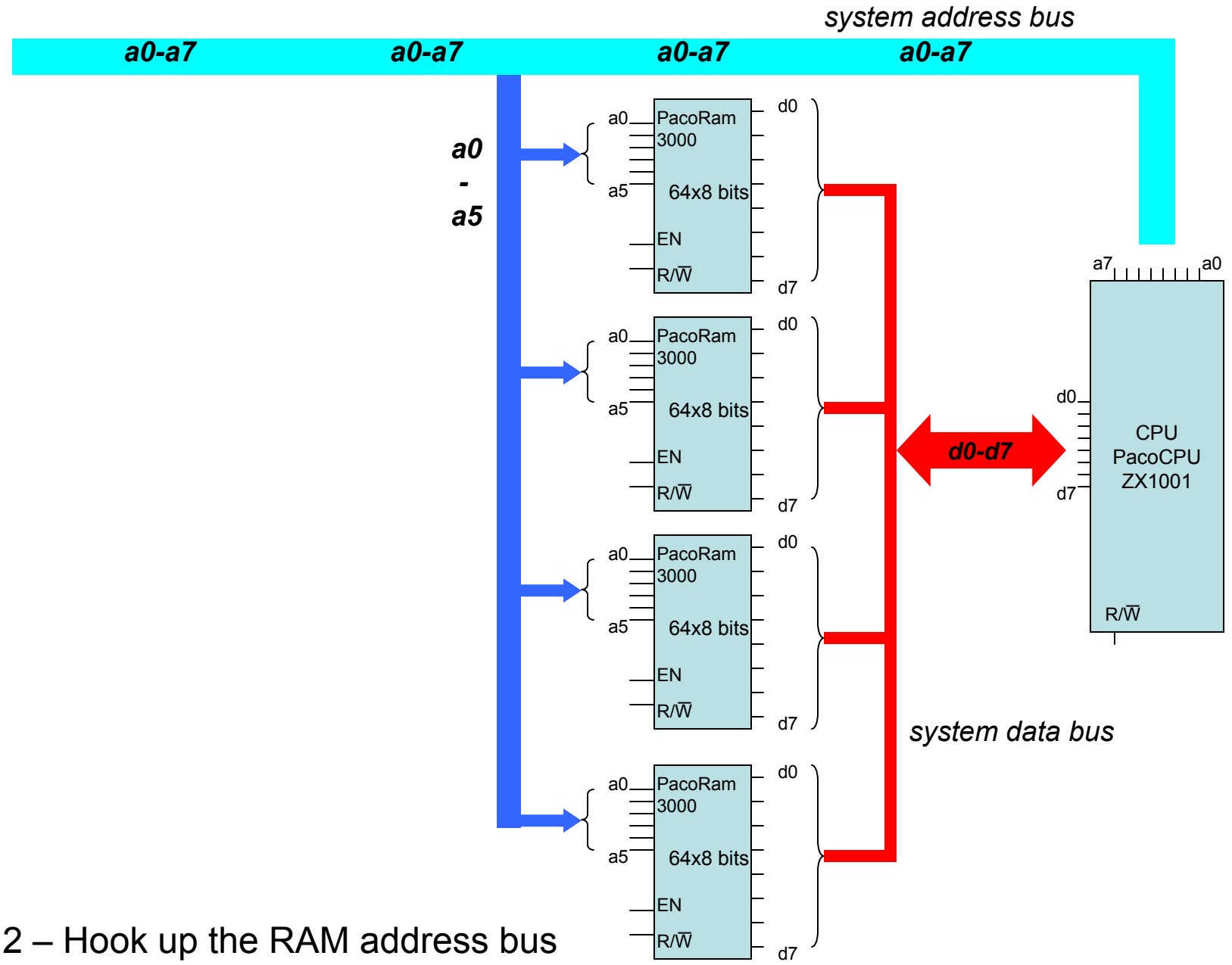
  A 2 to 4 decoder, 2 selection lines, 4 output lines

Memory bank design

1 – Hook up the data bus

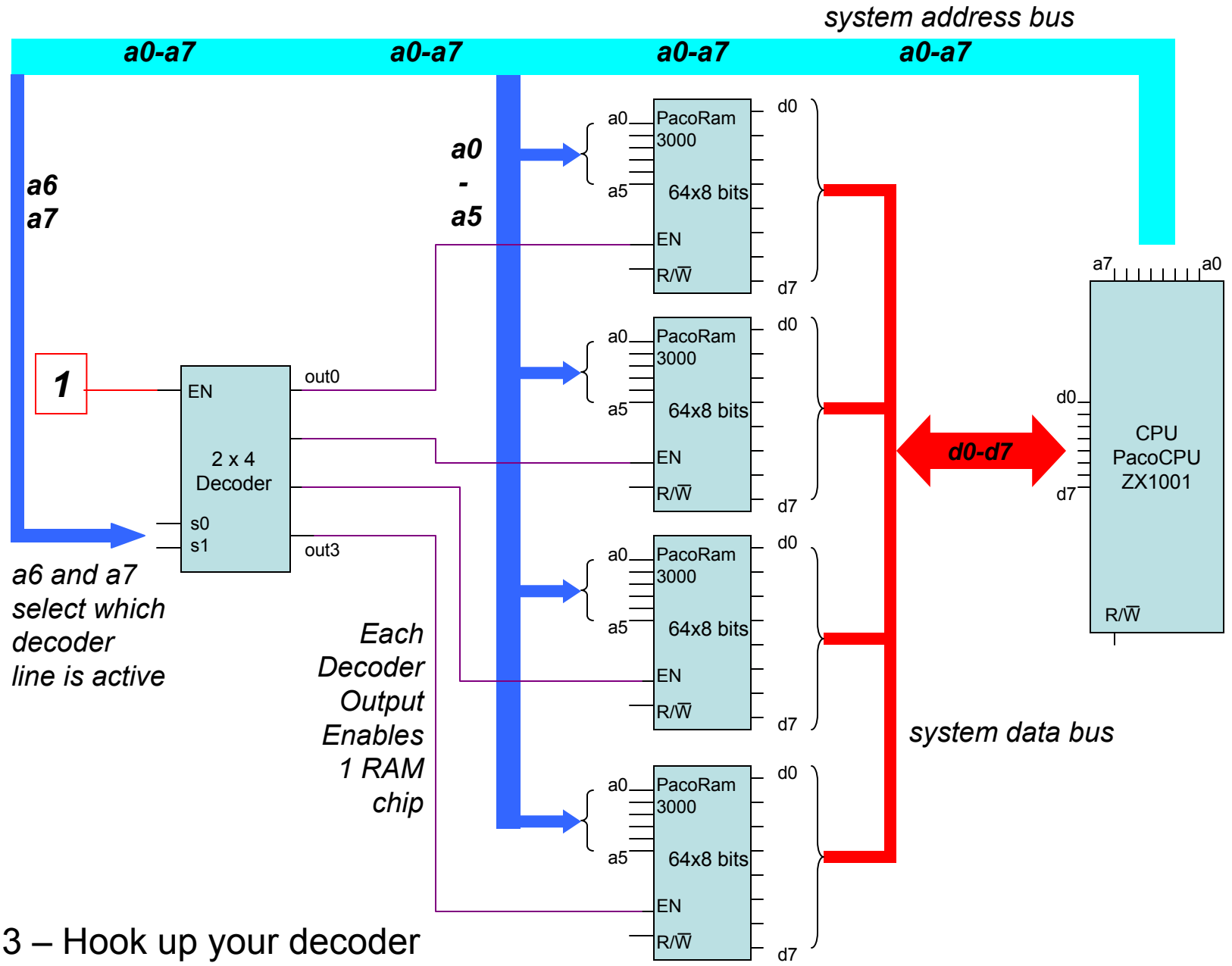


Memory bank design



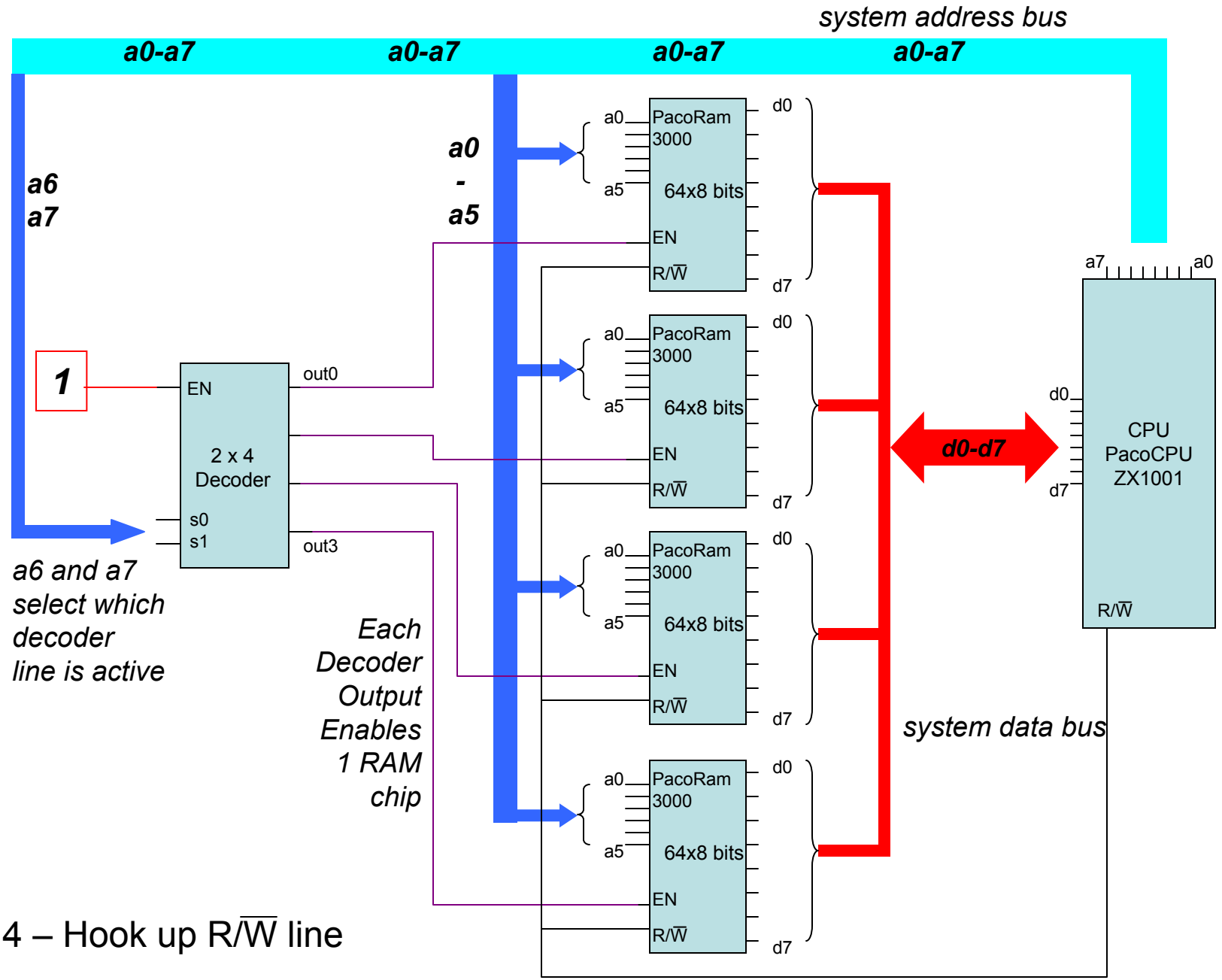
2 – Hook up the RAM address bus

Memory bank design



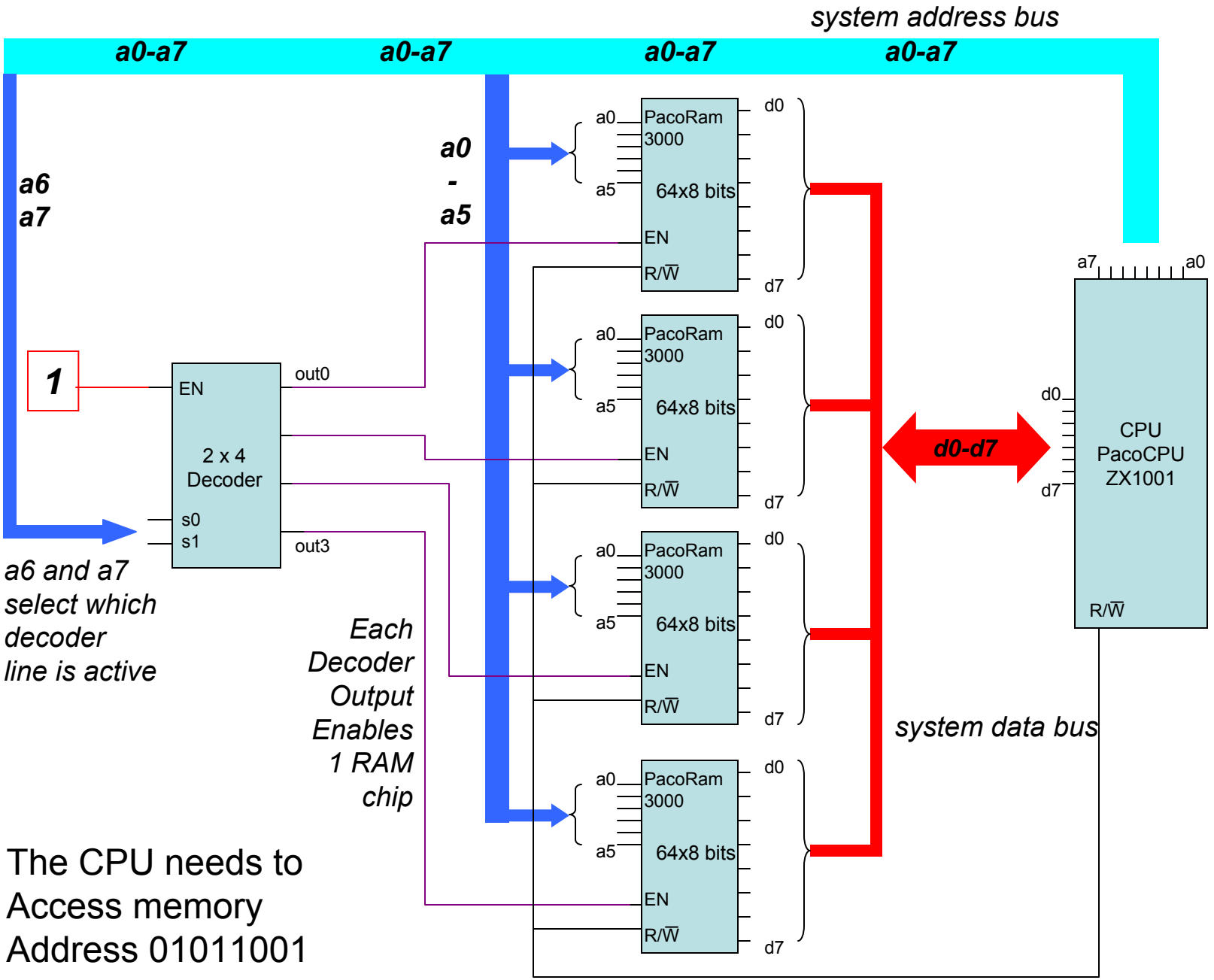
3 – Hook up your decoder

Memory bank design

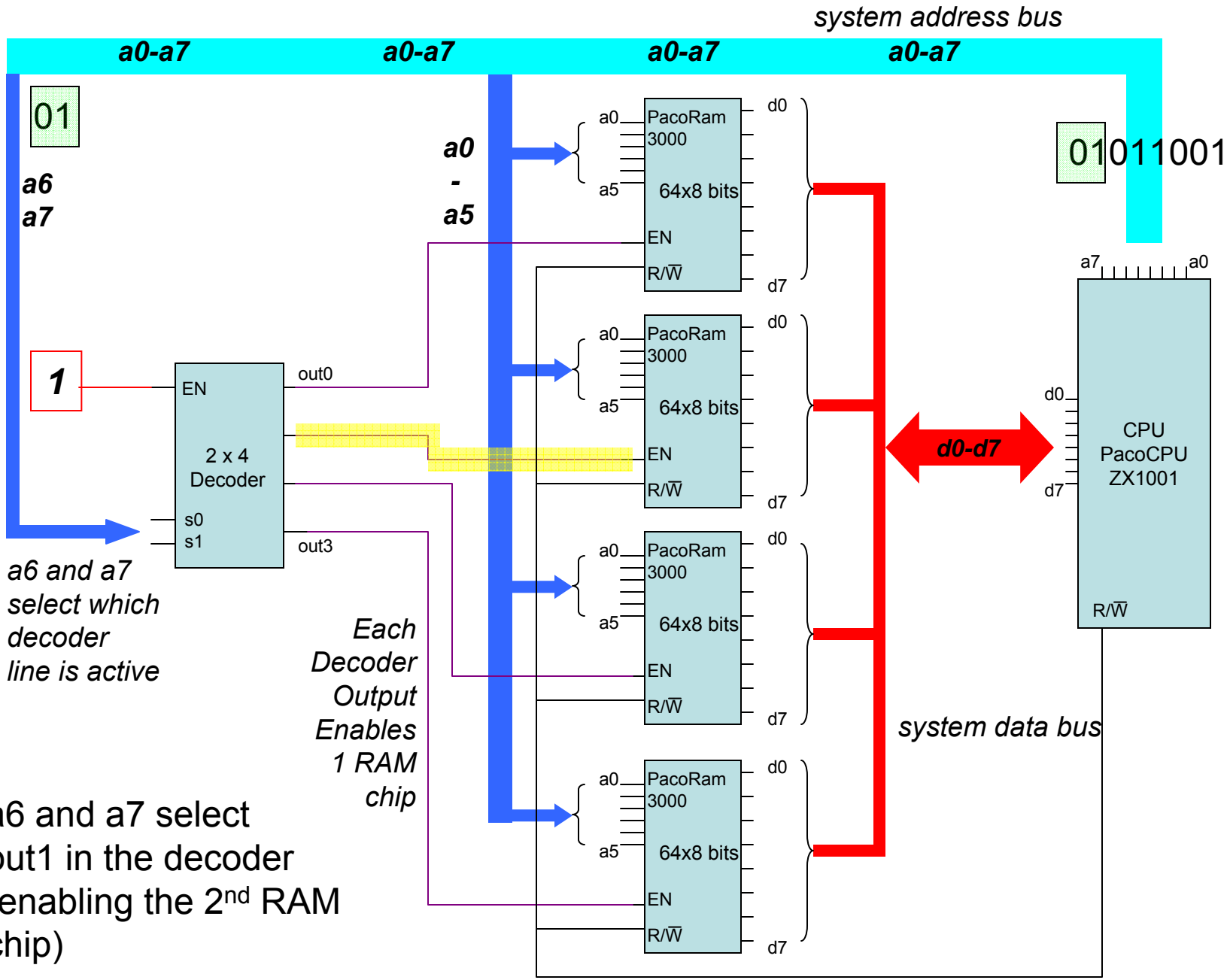


4 – Hook up R/$\overline{W}$ line

Memory bank operation

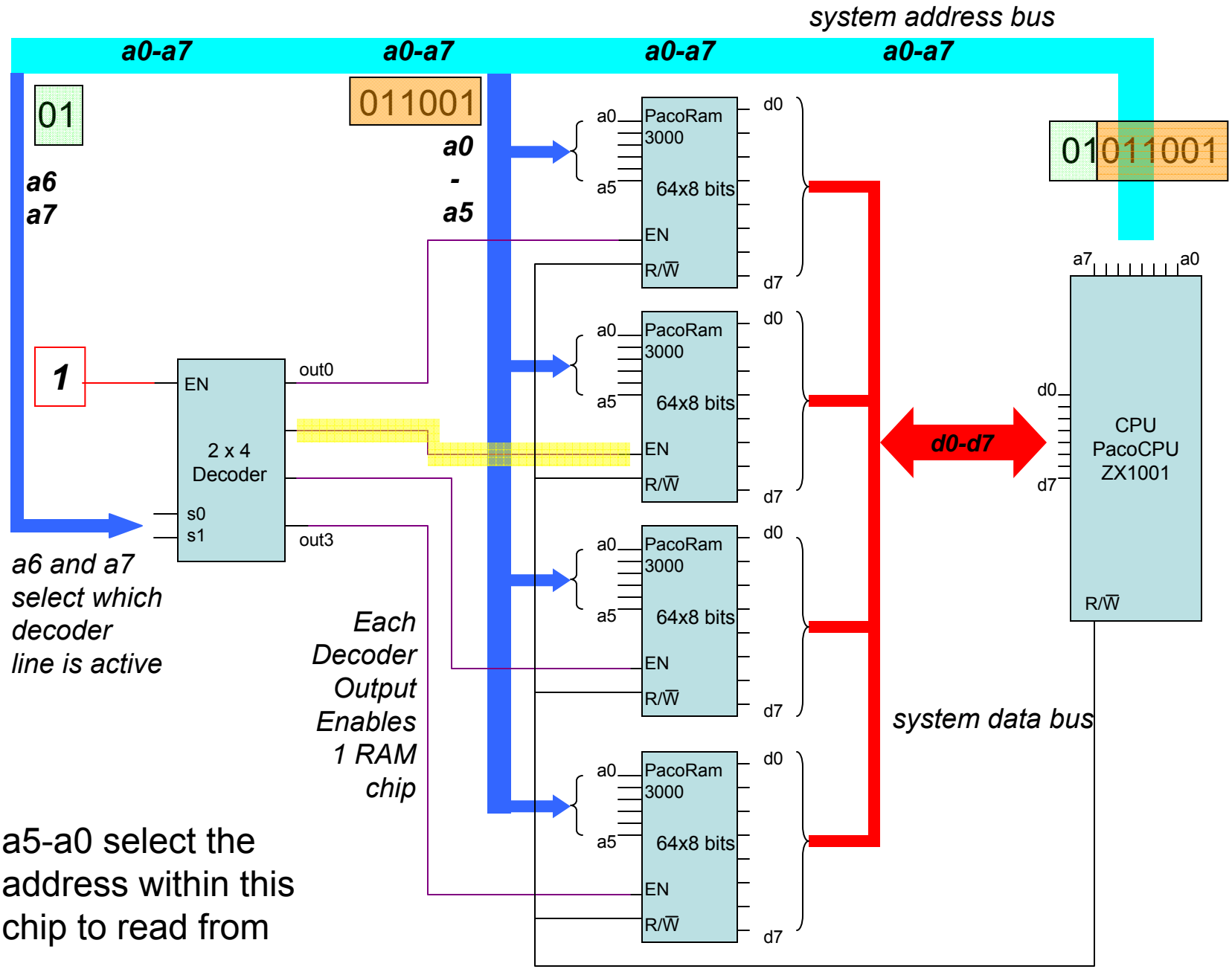


Memory bank operation

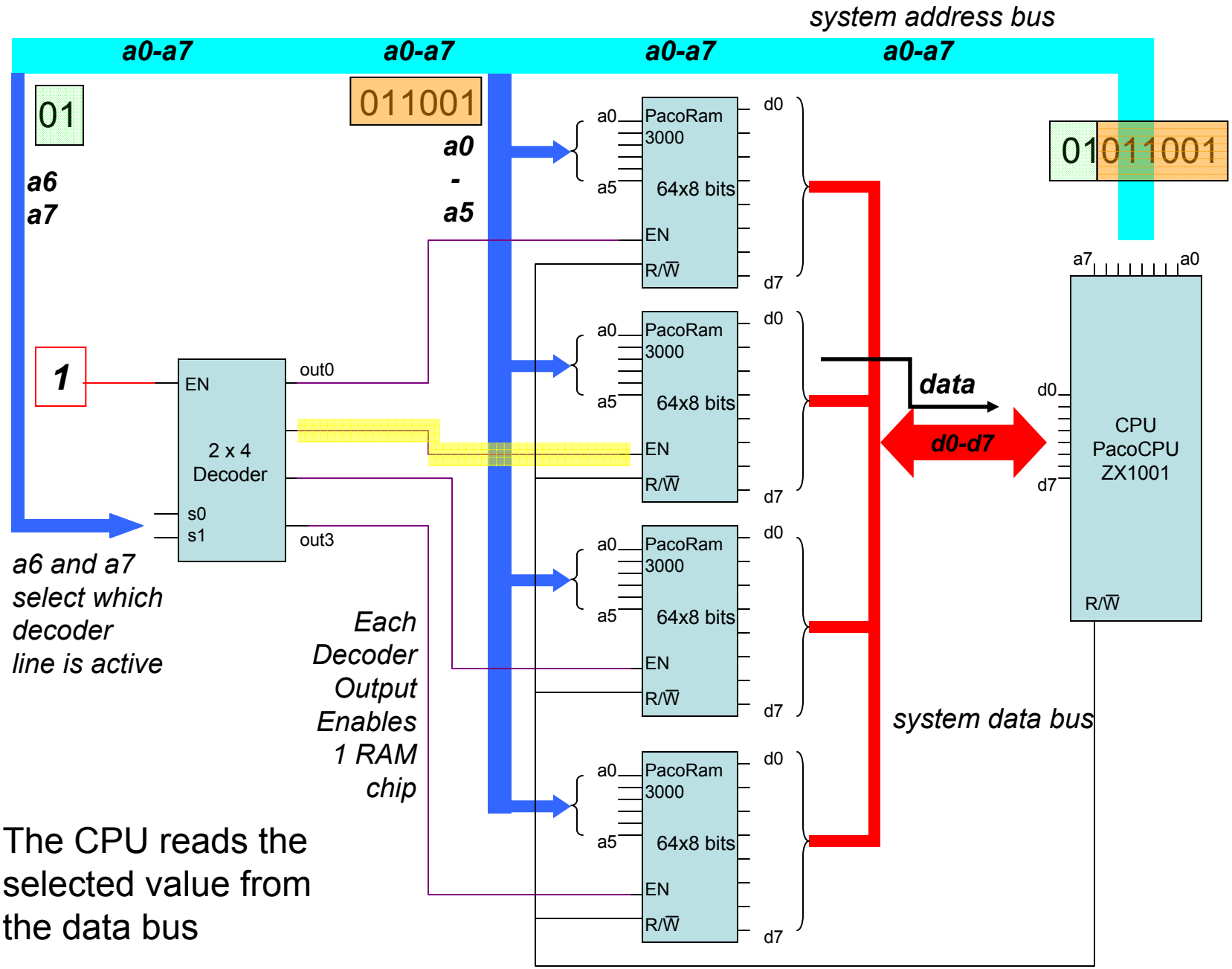


a6 and a7 select out1 in the decoder (enabling the 2nd RAM chip)

Memory bank operation

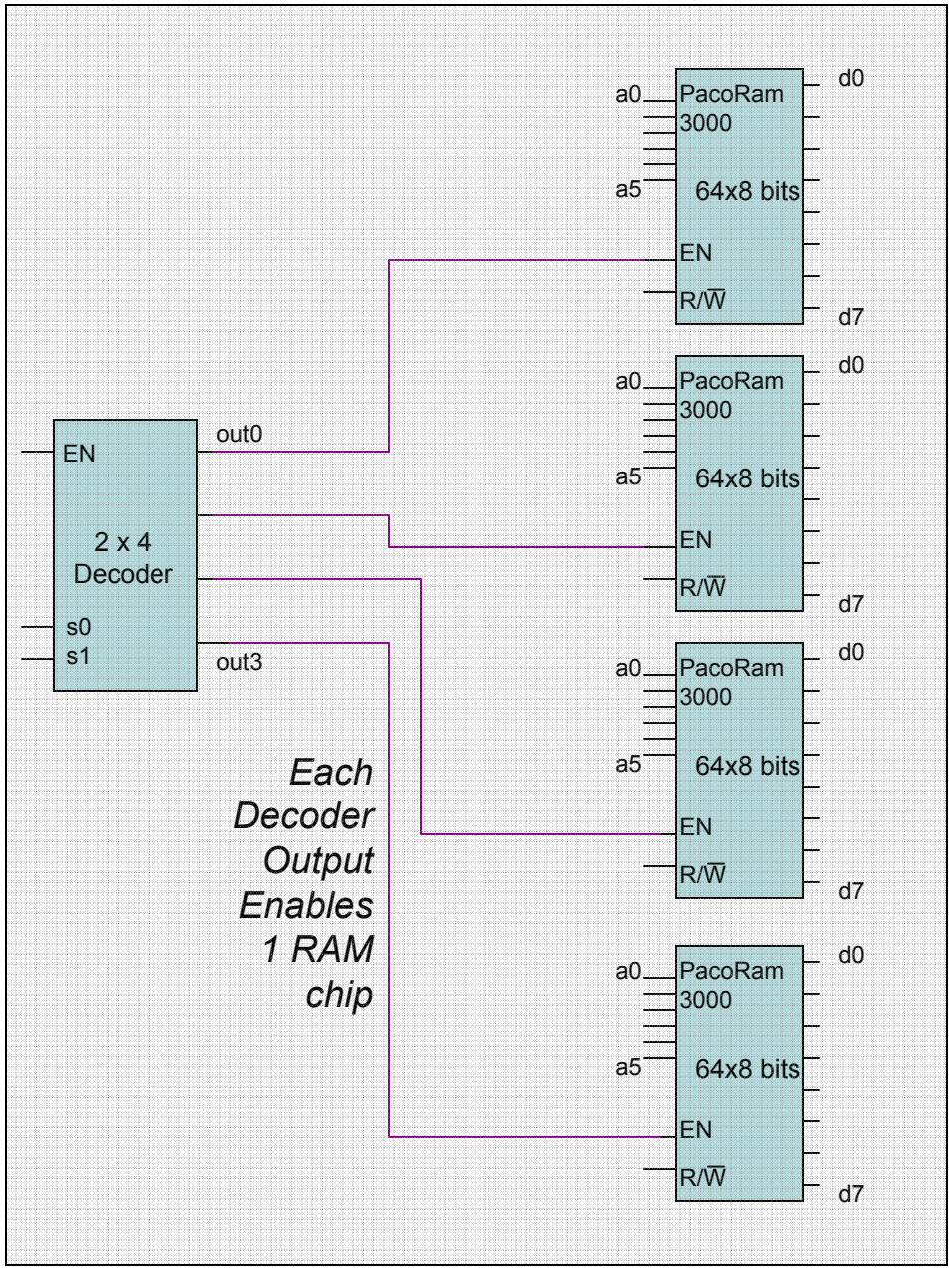


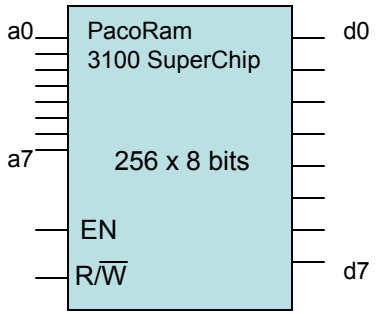
Memory bank operation



The CPU reads the selected value from the data bus

Memory bank – expanding with more decoders





As long as I have available address lines, I can keep adding more memory