The due date for this assignment is: Fri. Feb. 13, at 12 noon (at the B58 drop box)

Name (last, first):

Student No.:

I certify that I have read the UTSC policy on academic honesty and plagiarism, and that all work I am providing with this assignment is my own.

Student signature: _____

Note: There is a 3 marks penalty for failing to complete the above section.

Part	Marks
1	/ 10
2	/ 30
3	/ 35
Bonus	/ 3
Total	/ 75

CSC B58 – Winter 2015
Assignment 2 – Memory Circuits and Memory Banks

This assignment is intended to help you practice with the different modes of binary data representation and manipulation. You will also review your understanding of how computer memory is organized at the physical level: How it is wired to a processor, how different locations are addressed and accessed, and how you can design a memory bank from scratch.

Learning Objectives – after completing this assignment you should be able to:

Build a memory bank of a specified capacity using memory components with smaller storage size

Explain how addressing works within a memory bank.

Determine, given the memory address of some variable, in which chip within the memory bank it is stored

Understand the operation of circuits with flip-flops, and how outputs from these circuits change over time

Skills Developed:

Designing memory banks at the level of discrete components and address/data connections

Understanding timing diagrams and thinking about circuits with feedback

References:

Your lecture notes on simple circuits, decoders, latches, flip-flops, and timing diagrams.

Your course instructor and/or TA! (did I mention we are happy to help?)

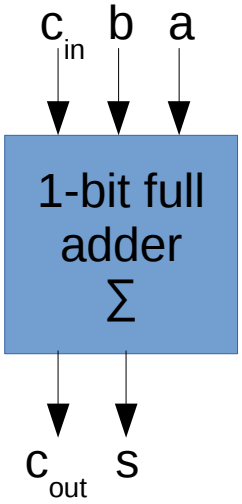
Part 1 – Binary arithmetic

a) (10 marks): Design a 3-***bit binary multiplier.*** The circuit takes the following inputs:

Input number A (a2 a1 a0)
Input number B (b2 b1 b0)

And produces as output the multiplication of both (how many bits?)

You can use as building blocks 1-bit full adders as shown below:



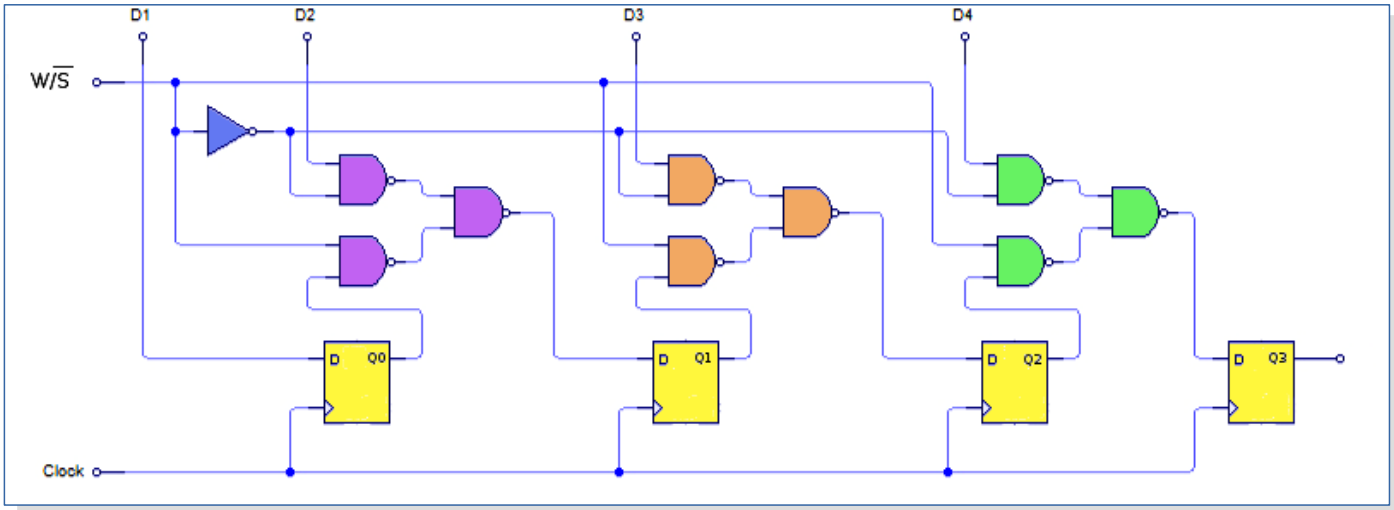
You will need to add some additional gates, but you do not have to Draw any components of the full adders. Use boxes just like the above.

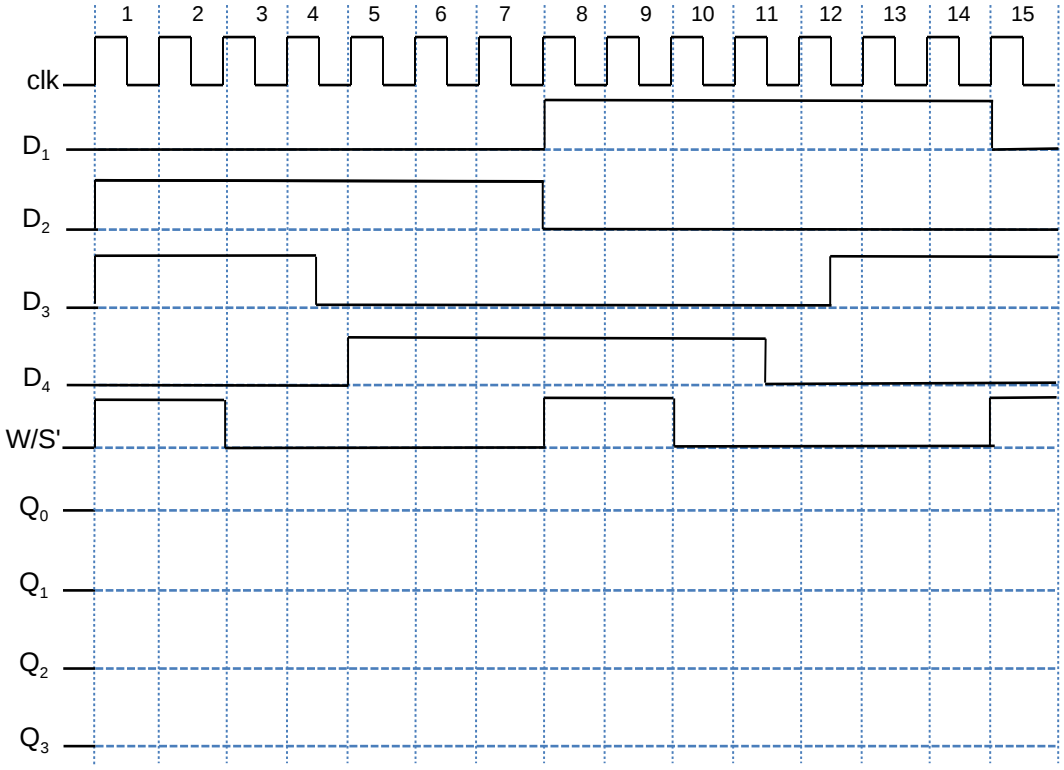
Be sure to annotate your circuit and explain to your TA clearly how it works!

Attach any written work for this part immediately after this page

Part 2 – Circuits with Feedback (Flip-Flops)

a) (3 marks per clock): Complete the timing diagram for the circuit shown below





Clk	Q3 Q2 Q1 Q0
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	

Record the values for Q3, Q2, Q1, and Q0 on the table at the right-hand side of the timing diagram. Q3-Q0 are initially all zero.

Attach any written work for this part immediately after this page

Part 3 – Memory Banks

a) (20 marks total) Design a memory bank under the following conditions:

- The CPU has 9 address lines, and 16 data lines
- You have memory chips with a capacity of 256 bytes, and 8 data lines
- Your memory bank must have a capacity of 1024 bytes

1) (5 marks) Show a simple block for the CPU with the correct number of address and data lines, as well as any ***control signals*** needed to operate the memory bank. ***What is the maximum memory capacity of this CPU (in bytes)?***

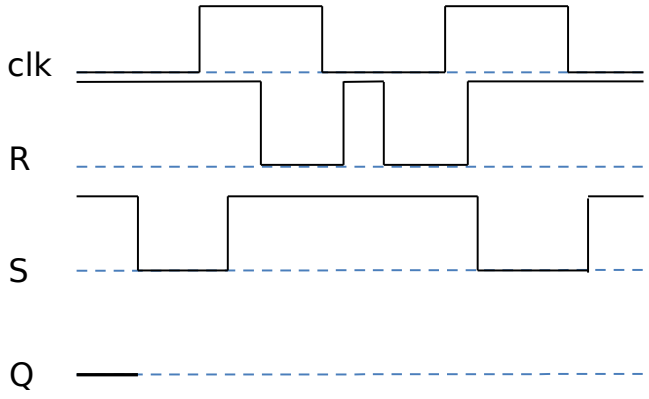
2) (5 marks) Show a simple block for the RAM chip with the correct number of addresses and data lines as well as any control inputs that will be used to connect and operate the memory bank. ***How many of these chips will you need for your memory bank?***

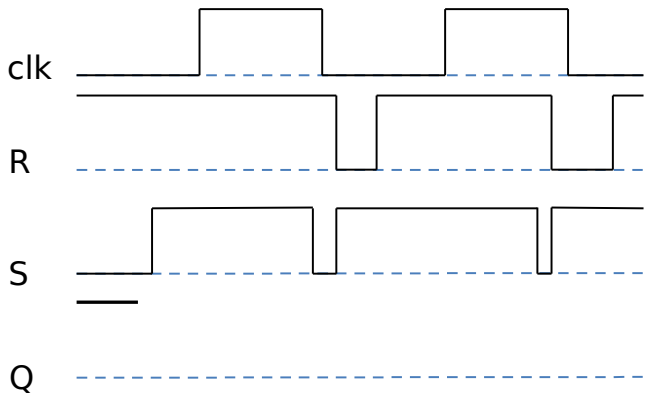
3) (10 marks) Create the memory bank. Be sure to draw a clean diagram with all address, data, and control lines clearly shown, and if you use other components (such as decoders or multiplexers) be sure to ***explain to your TA why they are there and what they do.***

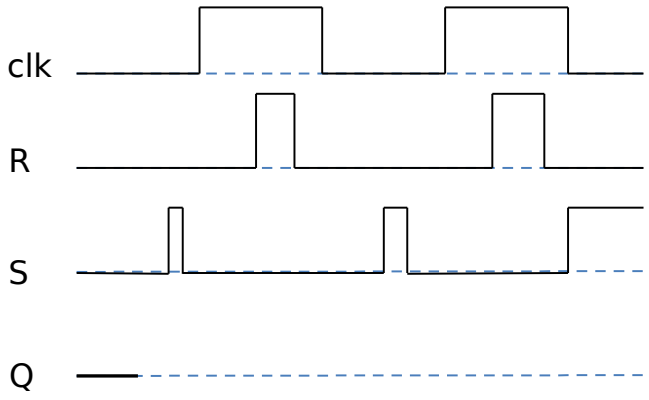
Attach any written work for this part immediately after this page

Part 3 – Memory Banks (cont.)

c) (5 marks each) Analyze and complete the timing diagrams below assuming an R-S flip-flop. State ***the final value for the output Q.*** The dotted lines are at "0". The initial value for Q is given in each diagram.







Attach any written work for this part immediately after this page

Bonus: (3 marks)
Complete this section after you have solved the rest of your assignment
- there are no right answers! - this is for feedback only, and will remain confidential.

Self evaluation: This section is meant to help you find topics that are giving you trouble. Focus your studying on these topics.

I will look at this also, to see what topics are giving most people trouble, we will devote more time to these topics during tutorials, and if necessary, use tutorials for reviewing that material

1.- How difficult did you find converting numbers between binary and decimal formats?
very easy / easy / tricky / hard

2.- How well do you understand 2's complement arithmetic (how to get the 2's complement) and how to use if in arithmetic operations)?
very well / well / partially / not at all

3.- Did the timing-diagram exercise make you think carefully about flip-flops and how they work?
definitely / somewhat / not at all

4.- How confident are you at this point that you understand how computer memory is organized at the physical level?
very confident / somewhat confident / not confident (it's unclear to me)

5.- How useful was this assignment in helping you achieve the learning goals stated on P1?
very useful / somewhat useful / not useful at all
(if not useful, please give a brief comment of why, and what would have helped you achieve these learning goals – use the back of the page as needed)

6.- What topic or concept would you like to see a review of (either in lecture or tutorial)?