

RV1126/RV1109

Hardware Design Guide

Release Version: V1.1
Release Date: 2020-6-24

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Preface

Overview

This document presents the key points of hardware design and notices for RV1126/RV1109 processor, aiming to help customers shorten the product design time, improving product design stability and reducing fault rate. Please refer to the requirements of this guide for hardware design, and use the relevant core templates released by Rockchip. If you need to modify for special reasons, please strictly follow the design rule of high-speed-digital-circuit and Rockchip Schematic&PCB checklist requirements.

Chipset Model

This document is suitable for the following chipset models: RV1126 and RV1109.

Intended Audience

This document (this guide) is mainly intended for:

- Hardware development engineers
- Technical support engineers
- Test engineers

Revision History

This revision history recorded description of each version, and any updates of previous versions are included in the latest one.

Version No	Author	Revision Date	Revision Description	Remark
V1.0	Li Yanhong	2020-04-09	The initial release version	
V1.1	Li Yanhong	2020-06-24	V1.1 Update points: 1. Add A7-JTAG_M1 introduction. 2. Add power-on sequence introduction 3. Add DDR template list table 4. Add logic/ARM/NPU/VEPU max current 5. Add usb circuit for improving compability 6. Correct Audio DSM reference circuit 7. Add DDR signals Layout Requirements table 8. Add FLASH/eMMC signals Layout Requirements table 9. Add SDMMC0/SDIO signals Layout Requirements table 10. Add RGMII signals Layout Requirements table 11. Add MIPI/RGB/LCDC signals Layout Requirements table 12. Add USB signals Layout Requirements table	

Acronyms

Acronyms include the abbreviations of commonly used phrases in this document:

ARM	Central processing unit	中央处理器
NPU	Neural network Processing Unit	神经网络处理器
VPU	Video Processing Unit	视频处理器
PMU	Power Management Unit	电源管理单元
PMIC	Power Management IC	电源管理芯片
DDR	Double Data Rate	双倍速率同步动态随机存储器
eMMC	Embedded Multi Media Card	内嵌式多媒体存储卡
FSPI	Flexible Serial Peripheral Interface	灵活串行外设接口
SPI	Serial Peripheral Interface	串行外设接口
SDMMC	Secure Digital Multi Media Card	安全数字多媒体存储卡
SDIO	Secure Digital Input and Output Card	安全数字输入/输出卡
SD Card	Secure Digital Memory Card	安全数码卡
TF Card	Micro SD Card(Trans-flash Card)	外置记忆卡
I2C	Inter-Integrated Circuit	内部整合电路(两线式串行通讯总线)
I2S	Inter-IC Sound	集成电路内置音频总线
ACODEC	digital audio codec	数字音频编解码器
PDM	Pulse density modulation	脉冲密度调制
USB	Universal Serial Bus	通用串行总线
UART	Universal Asynchronous Receiver/ Transmitter	通用异步收发传输器
PWM	Pulse width modulation	脉冲宽度调制
TSADC	Temperature sensing a / D converter	温度感应模数转换器
SARADC	successive approximation register Analog to digital converter	逐次逼近寄存器型模数转换器
CAN	Controller Area Network	控制器局域网络
MIPI	Mobile Industry Processor Interface	移动产业处理器接口
LVDS	Low-Voltage Differential Signaling	低电压差分信号
SubLVDS	Sub- Low-Voltage Differential Signaling	低摆幅差分信号技术
RGB	RGB color mode is a color standard in industry	RGB色彩模式，是工业界的一种颜色标准
ISP	Image Signal Processing	Figure像信号处理
JTAG	Joint Test Action Group	联合测试行为组织定义的一种国际标准测试协议（IEEE 1149.1兼容）
LDO	Low Drop Out Linear Regulator	低压差线性稳压器
Rockchip	Rockchip Electronics Co.,Ltd.	瑞芯微电子股份有限公司

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1 System Introduction

1.1 Overview

RV1126 and RV1109 are high performance processor SoCs specific for visual processing, which can be widely used in smart door lock, smart doorbell, network camera, drive recorder, game interaction, network living broadcast and other intelligent related industries.

The package of RV1126 is completely compatible with RV1109, they are with the same pin signal definition. The main difference is the computing ability of ARM, NPU, ISP, etc. Please refer to the following table or chipset datasheet. The description of the interface function of these two chipset is no longer strictly different from each other in this document, both of them called RV11XX.

RV1126 integrates NEON and FPU based on quad core Arm Cortex-A7 32 bit kernel. RV1109 integrates NEON and FPU based on dual core Arm Cortex-A7 32 bit kernel. Each core has a 32KB I-cache, 32KB D-cache and 512KB shared second level buffer. Embedded NPU supports INT8/INT16 mix operation and with strong computing ability. Besides, due to the great compatibility, so much network models such as TensorFlow/MXNet/PyTorch/Caffe etc. can be easily converted.

RV11XX also introduces a new generation of completely hardware based image signal processor and post processor. The chipset directly integrates many algorithm accelerators, which can be used for IPC and CVR products, such as HDR, 3A (AE, AF, AWB), LSC, 3DNR, 2DNR, sharpen, dehaze, fisheye correction, gamma calibration, characteristic detection and other functions. The chipset integrates two MIPI CSI (or LVDS/SubLVDS) and one DVP interfaces, and supports multi-camera application. For other interfaces, please refer to the following description or datasheet.

Chipset spec	RV1126	RV1109
ARM	Quad core A7*1.5GHz	Dual core A7*1.5GHz
NPU	2.0 Tops	1.2 Tops
ISP	14M Pixel	5M Pixel

Figure 1-1 Differences between RV1126 and RV1109

1.2 Block Diagram of the Chipset

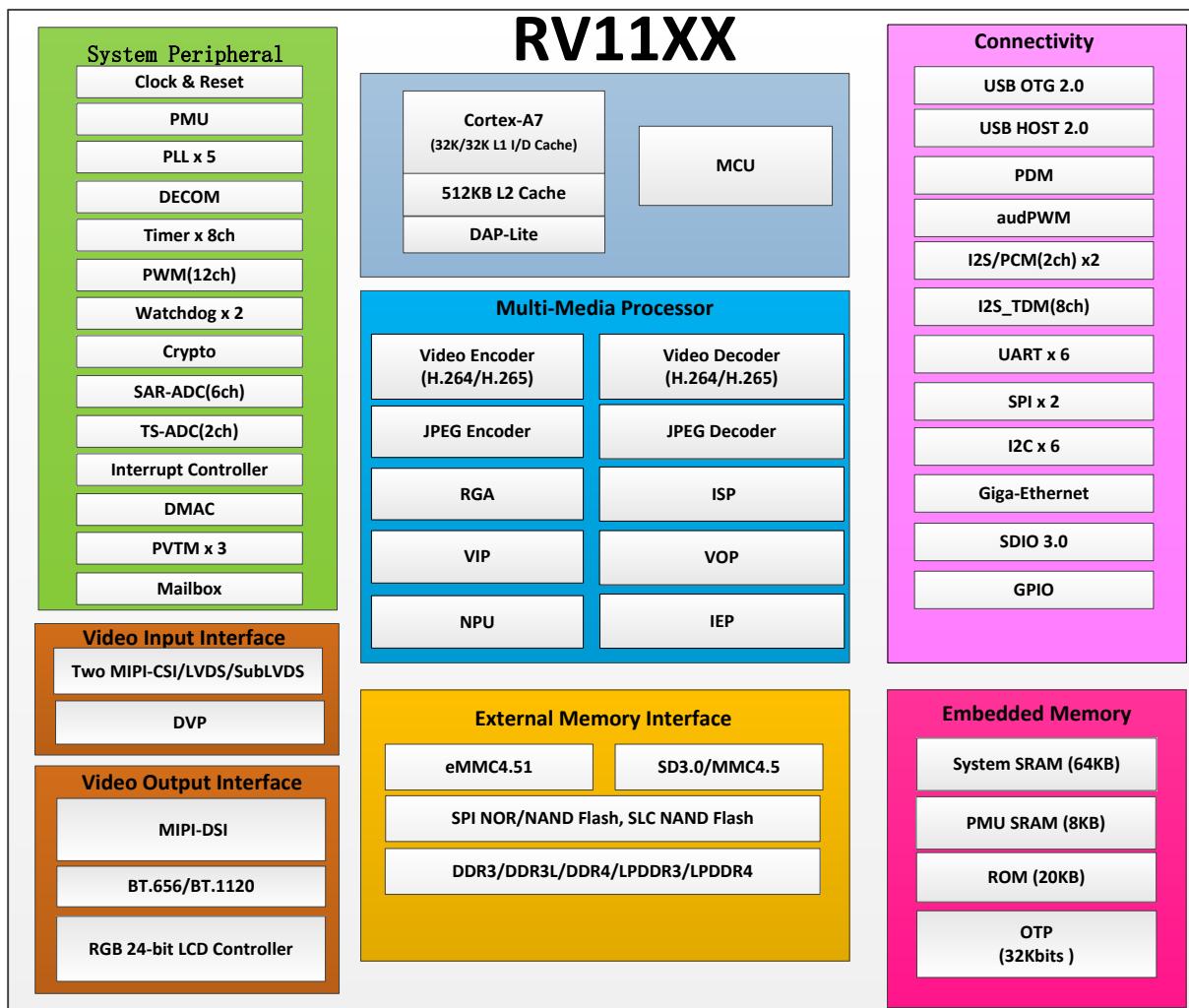


Figure 1-2 RV11XX block diagram

1.3 Application Block Diagram

1.3.1 Typical Application Block Diagram (PMIC Solution)

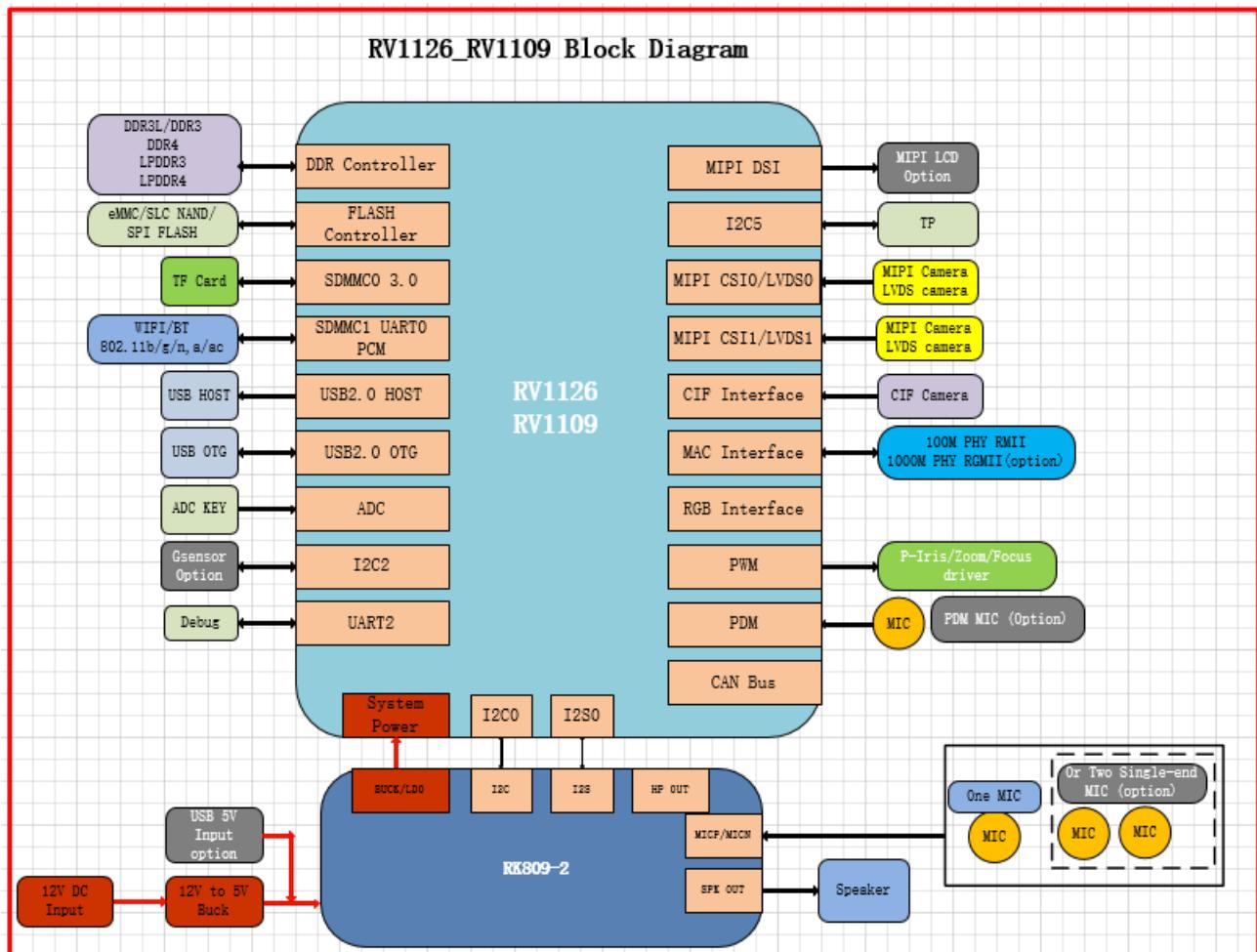


Figure 1-3 RV11XX typical application block diagram (PMIC solution)

The figure above is the application block diagram of RV11XX with the PMIC chipset RK809-2. Please refer to the reference design schematic released by RK for more details.

2 Schematic Design Recommendation

2.1 Minimum System Design

2.1.1 Clock Circuit

The internal feedback circuit of RV11XX chipset and external 24MHz crystal oscillator circuit form the system clock circuit. The recommended crystal connection and component parameters as shown in Figure 2-1.

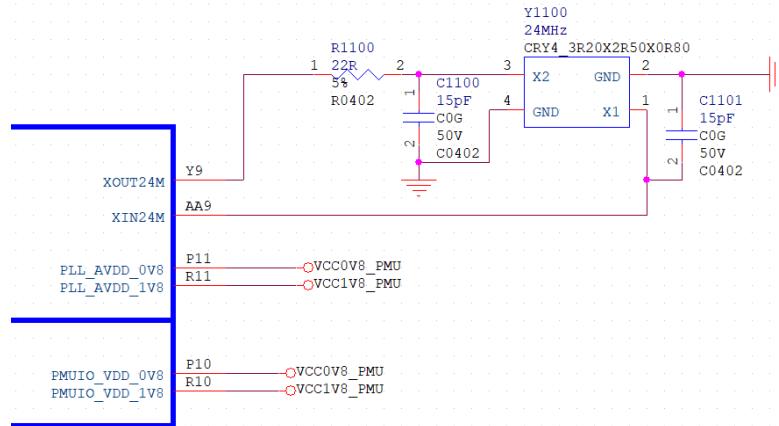


Figure 2-1 RV11XX crystal circuit



Note

The capacitances used should be matched with the load capacitance of the crystal oscillator and NPO material is recommended. It is recommended to use 4Pin SMT crystal oscillator, with 2 GND pins fully connected with ground to enhance ESD anti-interference ability of the system clock. Select 24MHz with 20ppm frequency offset.

When the 24MHz system clock is active crystal, it inputs from pin XIN24M, pin XOUT24M is left unconnected, and the clock amplitude is $1.8V \pm 10\%$. The clock parameters are shown as table 2-1 below:

Table 2-1 The 24MHz digital clock source

Parameters	Spec		Description
	Min.	Max.	
Frequency	24.000000		MHz
Frequency tolerance	+/-20		ppm
Clock amplitude	$1.8V \pm 10\%$		V
Operating temperature	-20	70	°C
ESR	/	40	Ohm

The 32.768KHz clock required by RV11XX during standby state can be provided by PVTM inside PMU, and also can be input externally. The 32.768KHz clock signal can be obtained from PMIC or external RTC clock source, and then go into pin AA3 as shown below.

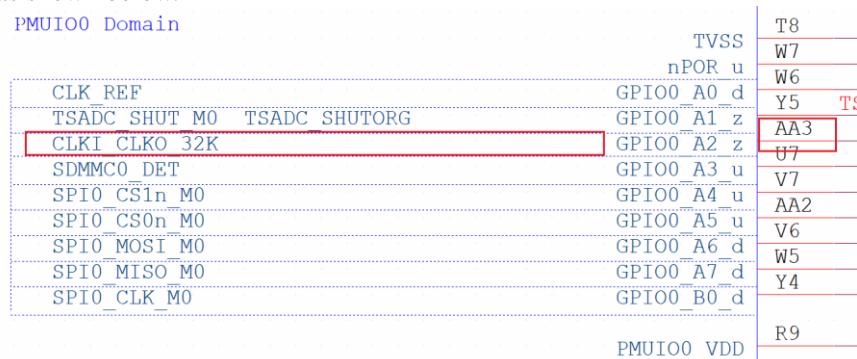


Figure 2-2 RV11XX clock input in standby state

The external 32.768KHz RTC clock parameters are shown as table 2-2 below:

Table 2-2 The 32.768KHz clock requirements

Parameters	Spec			Description
	Min.	Max.	Unit	
Frequency	32.768000		kHz	
Frequency tolerance	+/-30		ppm	
Clock amplitude	PMUIO0_VDD ±10%		V	
Operating temperature	-20	70	°C	
Duty ratio	50		%	

2.1.2 Reset Function

RV11XX hardware reset is implemented by nPOR pin, low active, and the minimum pulse width time is 100 cycles of 24MHz clock (at least 4us), to ensure SoC operation stably and normally.

It is recommended to connect a 100nF capacitor in parallel to the reset signal, and place it close to the pins of the chipset, to enhance the anti-interference ability and avoid system reset caused by false triggering. The power management chip matched with RV11XX is RK809-2, which has fixed power up sequence and reset operation to ensure reliable reset. The level of IO power domain of NPOR pin should keep consistent with the pull up level of RESET pin, as shown in figure 2-3 and 2-4.

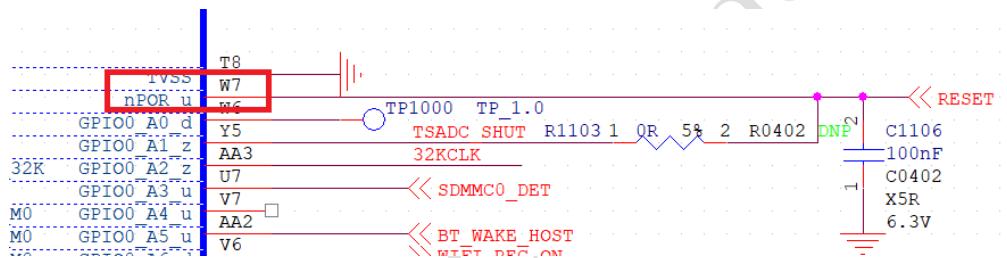


Figure 2-3 Reset pin of RV11XX

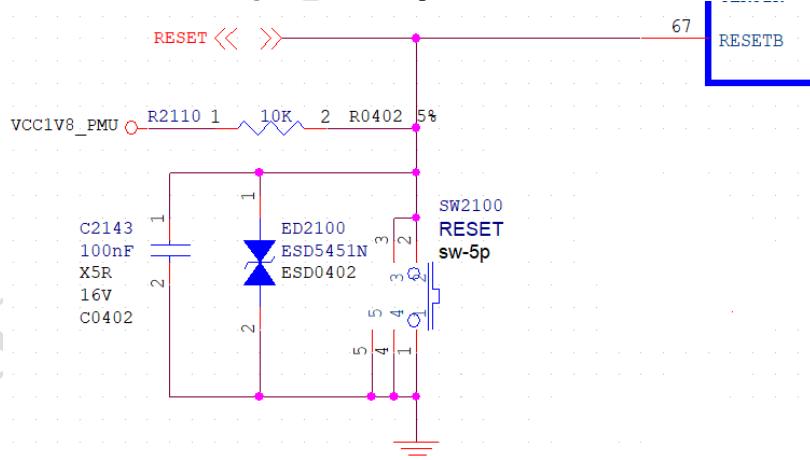


Figure 2-4 Reset pin of RK809-2

2.1.3 System Boot Sequence

RV11XX supports multi system boot sequences. After system reset, the boot code integrated inside the chipset will automatically judge and load according to the following sequence:

- SPI FLASH
 - Nand FALSH
 - eMMC FLASH
 - SDMMC CARD
 - USB OTG

2.1.4 System Initialization Configuration Signal

There are two signals PIN Y8 FLASH_VOL_SEL and PIN U7 SDMMC0_DET of RV11XX which will affect the system boot configuration. When the system reset is released, the chipset will configure the default functions of the corresponding modules according to the input level of these two pins.

PIN Y8 FLASH_VOL_SEL is used to configure the VCCIO1_VDD power domain level of the memory interface IO, to ensure the level match with the configuration in the boot code. If the level of external memory interface IO is 1.8V, this pin must be kept high during reset. Conversely, if the level of the memory interface IO is 3.3V, this pin must be kept low during reset (FLASH_VOL_SEL pin can be unconnected as it is pull down inside the chipset). The boot level state of PIN Y8 should match with the actual power supply of the memory interface, to avoid the risk of system stability.

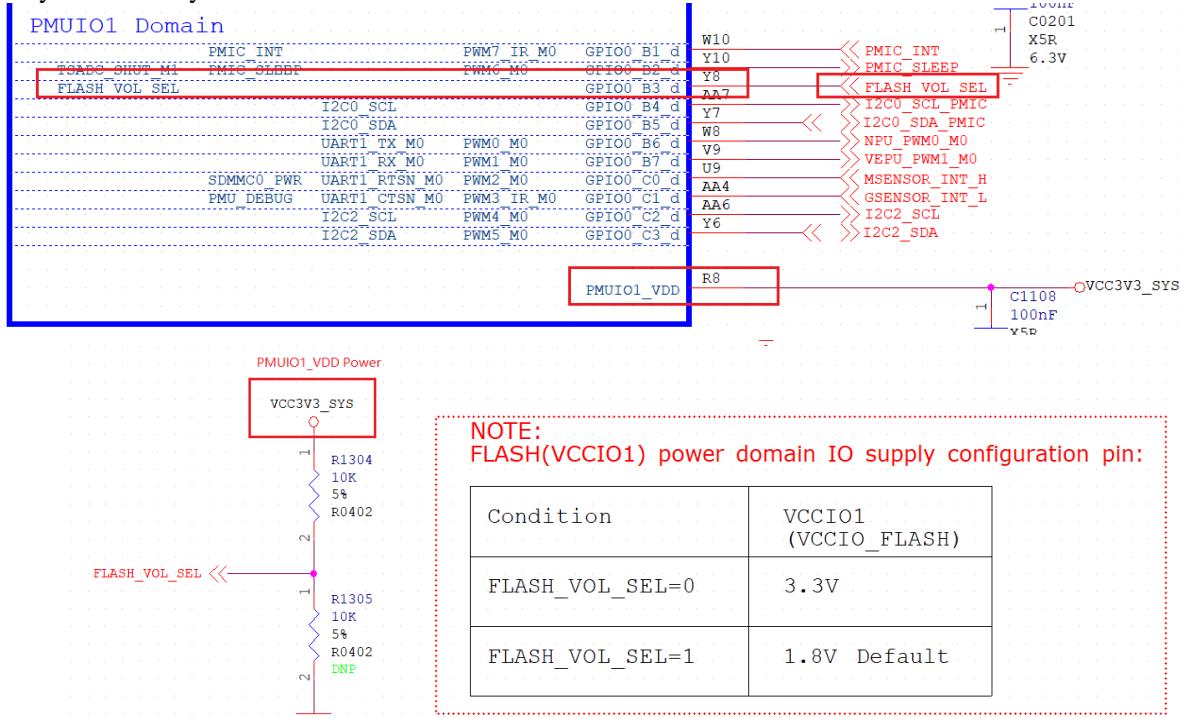


Figure 2-5 FLASH_VOL_SEL function

PIN U7 SDMMC0_DET is used to configure the default functions for system boot. When high level is detected, switch to JTAG function. When low level is detected (normal insertion state of SD card), switch to SDMMC function. This function is mainly convenient for the system bottom layer debugging without disassembling after the device with SD card function is assembled.

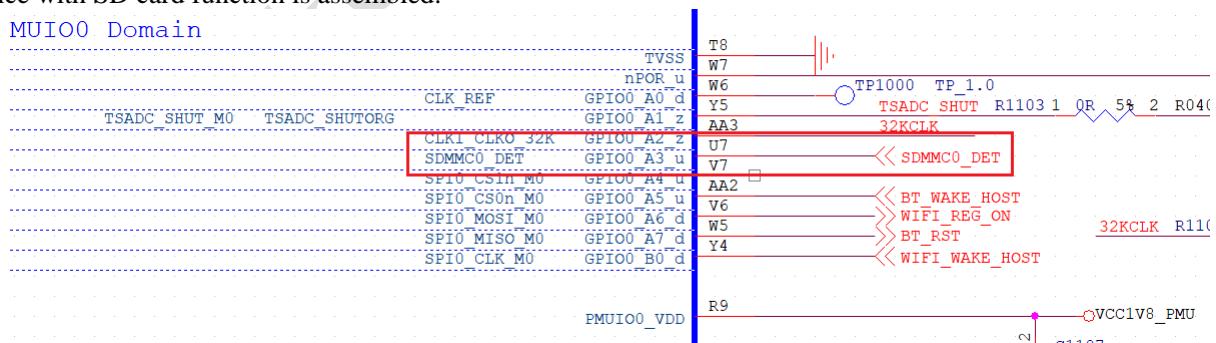


Figure 2-6 SDMMC0/DEBUG reused control pins

Pin T8 TVSS pin state determines the mode of RV11XX, 0 grounded means normal function mode, while 1 means test mode.

Pin configurations are shown as the following table:

Table 2-3 System initialization configuration signal description

Signal name	Internal pull up/down	Description
FLASH_VOL_SEL	Pull down	FLASH(VCCIO1) power domain level configuration pins: 0: IO level mode is 3.3V (default) 1: IO level mode is 1.8V
SDMMC0_DET	Pull up	Control signal selection of JTAG pin reuse:

		0: is recognized as SD card insert, SDMMC/JTAG/UART pin is reused as SDMMC output. 1: is not recognized as SD card insert, SDMMC/JATG/UART pin is reused as JTAG function (default).
TVSS	NA	Function mode and test mode selection: 0: function mode, connected to GND. 1: test mode.

2.1.5 JTAG Debug circuit

The A7_JTAG interface of RV11XX chipset is compliant with IEEE1149.1 standard. PC can connect with DSTREAM emulator by SWD mode (Two-line mode) to debug ARM core inside the SoC. The MCU_JTAG of RV11XX chipset is compliant with IEEE1149.1 standard. PC can debug MCU inside the SoC by four-line mode. As described in previous section, when PIN U7 SDMMC0_DET pin is high (is high by default), it will switch to A7_JTAG function by default during system boot. The pins corresponding to JTAG-A7 function are:

Table 2-4 JTAG Debug interface signal

Pins	Signal name	Description
V13	A7_JTAG_TCK_M0	Cortex-A7 JTAG interface clock input/SWD interface clock input
U13	A7_JTAG_TMS_M0	Cortex-A7 JTAG interface TMS input/SWD interface data ou
W13	MCU_JTAG_TRSTn	MCU JTAG reset signal
V13	MCU_JTAG_TCK	MCU JTAG interface TCK input
U13	MCU_JTAG_TMS	MCU JTAG mode selection input signal
AA13	MCU_JTAG_TDO	MCU JTAG interface TDO output
Y13	MCU_JTAG_TDI	MCU JTAG interface TDI input

The A7-JTAG is also been multiplexed in VCCIO5 power domain, It's name is A7-JTAG_M1. The A7-JTAG_M1 is multiplexed with UART2_M1. UART2 debug function is by default during system boot. If UART2_RX_M1 is pulled down for a while, it will swich to A7_JTAG function.

Table 2-5 A7-RV1126/RV1109RV11XX JTAG-M1 interface signal

Pins	Signal name	Description
G18	A7_JTAG_TCK_M1/UART2_TX_M1	Cortex-A7 JTAG interface clock input/SWD interface clock input
H16	A7_JTAG_TMS_M1/UART2_RX_M1	Cortex-A7 JTAG interface TMS input/SWD interface data out



Note

MCU_JTAG_TCK and A7_JTAG_TCK_M0 reuse the same pin V13, which is A7_JTAG_TCK_M0 function by default.

MCU_JTAG_TMS and A7_JTAG_TMS_M0 reuse the same pin U13, which is A7_JTAG_TMS_M0 function by default. So if A7-JTAG function is needed, please use these two pins.

The JTAG connection method and standard connector pin definition are shown as below:

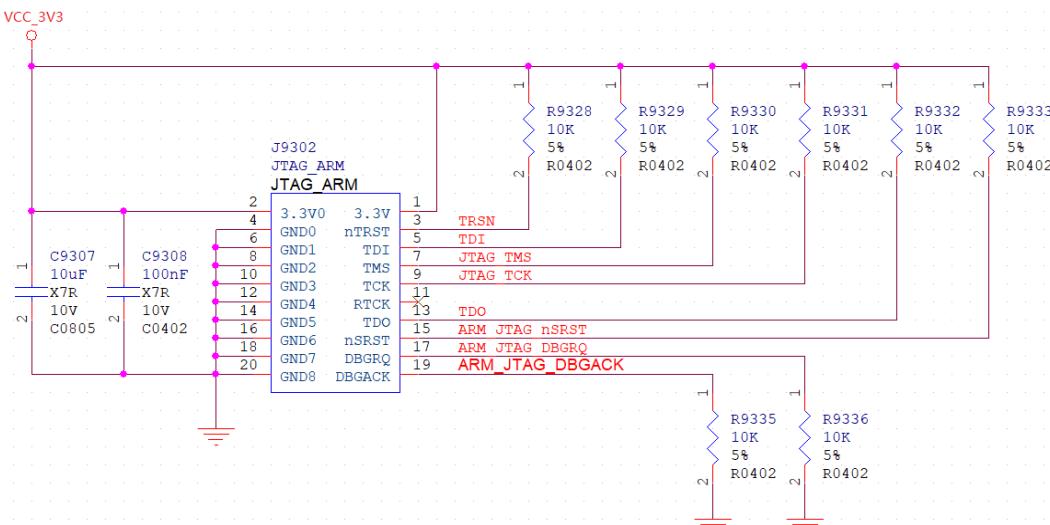


Figure 2-7 JTAG connection method

2.1.6 System Power Introduction

- PLL power supply: PLL_AVDD_0V8,PLL_AVDD_1V8
- OSC power supply: PMUIO_VDD_0V8,PLL_AVDD_1V8
- ARM power supply: ARM_VDD
- LOGIC power supply: LOGIC_VDD
- NPU power supply: NPU_VDD
- Encode power supply: VEPU_VDD
- DDR power supply: VCC_DDR
- PMU GPIO:PMUIO_VDD_0V8,PMUIO_VDD_1V8,PMUIO0_VDD, PMUIO1_VDD
- The power supply of OTP and ADC: ADC_AVDD_1V8
- IO PAD PVT power supply: VCCIO_VDD_1V8
- USB power supply: USB_AVDD_0V8,USB_AVDD_1V8,USB_AVDD_3V3
- MIPI DSI power supply: MIPI_DSI_TX0_AVDD_0V8,MIPI_DSI_TX0_AVDD_1V8
- MIPI CSI power supply: MIPI_CSI_RX0_AVDD_0V8,MIPI_CSI_RX1_AVDD_0V8, MIPI_CSI_RX0_AVDD_1V8, MIPI_CSI_RX1_AVDD_0V8

2.1.7 Power on sequence Introduction

Power on sequence as follow fig:

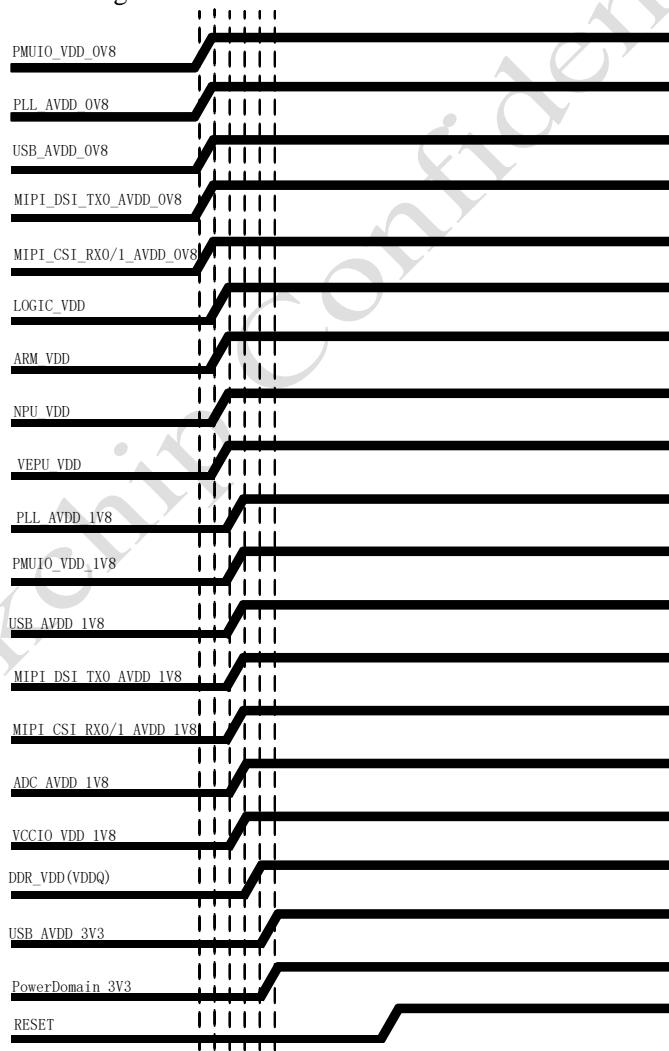


Figure 2-8 Power on sequence

- Digital VDD need to according the sequence:
PMUIO_VDD_0V8/PLL_AVDD_0V8→LOGIC_VDD/ARM_VDD/NPU_VDD/VEPU_VDD
(Note: The power on sequence of ARM_VDD/NPU_VDD/VEPU_VDD is OK before or after LOGIC_VDD)
 - USB power on
USB_AVDD_0V8→USB_AVDD_1V8→USB_AVDD_3V3
- The rise up time of all these three power: $T_{up} > 200\mu s$. The step time of all these three power: $T_d > 0\mu s$.

- MIPI DSI/CSI power on
MIPI_DSI_TX0_AVDD_0V8/ MIPI_CSI_RX0_AVDD_0V8/MIPI_CSI_RX1_AVDD_0V8- \rightarrow
MIPI_DSI_TX0_AVDD_1V8/ MIPI_CSI_RX0_AVDD_1V8/MIPI_CSI_RX1_AVDD_1V8, The
step time Td>0us.
- DDR PHY power on
PLL_AVDD_1V8 \rightarrow VCC_DDR (VDDQ)

(Note: The power on sequence of VCC_DDR is the same as PLL_AVDD_1V8 or after
PLL_AVDD_1V8)

Summary:

The requirement of power on sequence:

0.8V(all the 0.8Vpower) \rightarrow LOGIC_VDD/ARM_VDD/NPU_VDD/VEPU_VDD \rightarrow 1.8V(all the
1.8V power) \rightarrow VCC_DDR \rightarrow 3.3V(all the 3.3V power)

The rise up time of all power: Tup>200us, The step time of all power Td>0us.

2.1.8 Power Management (PMU) Interface Introduction

The power management (PMU) module of RV11XX can enable control of the nonconstant power supply module, receive the key signal/rising edge signal to control power up and down, and receive the wake-up signal output by the peripheral device, so as to realize the standby and awake functions of products.

- The power supply pins PMUIO0_VDD, PMUIO1_VDD, PMUIO_VDD_0V8 and PMUIO_VDD_1V8 of the PMU module are constant power supply.
- PMUIO0_VDD and PMUIO1_VDD represent the IO level of the respective power domain, which can be connected to 1.8V or 3.3V.
- The pinW7 is reset pin of nPOR (as described in section 2.1.2), low active.
- Pin W10 is PMIC_INT function, which can receive interrupt information returned by PMIC.
- Pin Y10 is PMIC_SLEEP function, which is used to control nonconstant power supply. When the system enters standby state, this pin will output a high-level sleep indication signal. According to the configuration of the software dts file, some power supplies will be turned off, and some power supplies will be lowered. When the system is resumed, PMIC_SLEEP restores low-level output state and power output of each channel will be restored.
- Pin Y5 is TSADC_SHUT function, which is used to control nPOR and can be connected to RESET through a OR resistor. When the chip temperature is over the set temperature, there will output a low-level signal from this pin, used to reset RV11XX and RK809-2, and control the power to be powered off and powered on again, and reset the entire system while the register is cleared.

2.1.9 Power Solution in Standby State

The RV11XX system power supply is designed with low power consumption. In the standby state, it can be divided into a constantly power supply area and power off in standby area. The two parts are independently powered, as shown in the following figure.

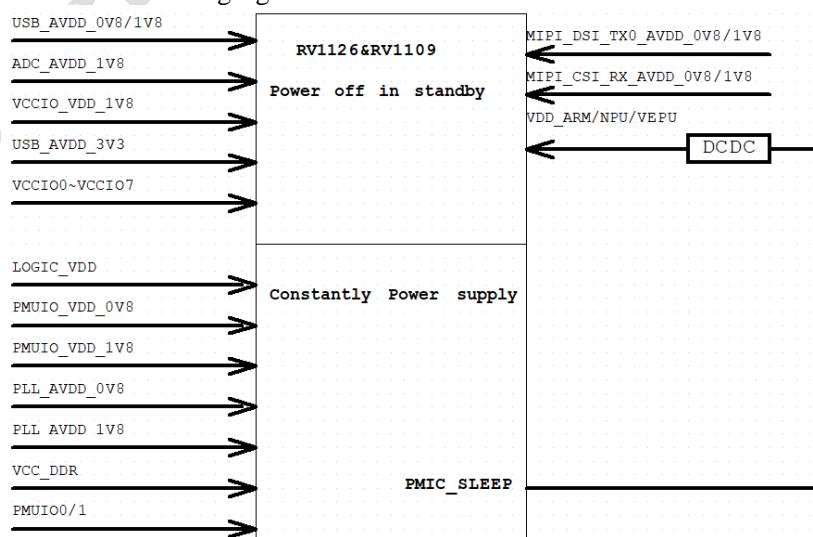


Figure 2-9 Power solution in standby state

Keep the following four groups of power supplies in the standby state without turning off:

- DDR: VCC_DDR, provide power for DDR self-refresh;

- PMU: PMUIO0/1_VDD, PMUIO_VDD_0V8 and PMUIO_VDD_1V8, provide IO power supply corresponding PMU power domain and PMU internal hardware logic power supply;
- PLL: PLL_AVDD_0V8&PLL_AVDD_1V8, provide power to PLL and OSC for work

**Note**

If there is any group of VCCIO continuous power during standby, VCCIO_VDD_1V8 should not be powered off.

2.1.10 DDR Circuit Design

2.1.10.1 DMC Introduction

DMC includes DDR Protocol Controller (PCTL) and DDRPHY, they are complete memory interface solutions for DDR memory subsystem.

The RV11XX DDR controller interface supports JEDEC SDRAM standard interface with following features:

- Support DDR3/DDR3L/DDR4/LPDDR3/LPDDR4, etc.
- Supports up to 2 RANKs and 4GB capacity;
- Support 32-bit and 16-bit DDR data bus width;
- Low power consumption modes, such as Power Down and SDRAM self-refresh;

2.1.10.2 DDR Topology Structure and Connection Mode

For the convenience of PCB layout, different DDR layouts with different bit widths take different line sequences. Please refer to the released "RV1126_RV1109_Template" for detailed line sequence and layout.

Table 2–6 DDR Template

DDR type	Template name	description
DDR3	RV1126_RV1109_Template_DDR3P216 DD4_V10_20200617	Layer: 4 DDR number: Support 1pcs or 2 pcs DDR chips.If only use 1pcs DDR chip, please use lane0 and lane2. DDR layout: double side
DDR3	RV1126_RV1109_Template_DDR3P216 SD4_V10_20200619	Layer: 4 DDR number: Support 1pcs or 2 pcs DDR chips.If only use 1pcs DDR chip, please use lane0 and lane2. DDR layout: Single side
DDR3	RV1126_RV1109_Template_DDR3P216 DD6_V10_20200325	Layer:6 DDR number: Only support 2 pcs DDR chips. DDR layout: double side
DDR3	RV1126_RV1109_Template_DDR3P416 DD6_V10_20200423	Layer:6 DDR number: Support 4 pcs DDR chips. DDR layout: double side
DDR4	RV1126_RV1109_Template_DDR4P216 DD6_V10_20200325	Layer: 6 DDR number: Support 1pcs or 2 pcs DDR chips.If only use 1pcs DDR chip, please use lane0 and lane2. DDR layout: double side
LPDDR3	RV1126_RV1109_Template_LP3S178P1 32SD6_V10_20200325	Layer: 6 DDR number: Support 1pcs 178 balls LPDDR3 chip
LPDDR4	RV1126_RV1109_Template_LP4S200P1 32SD6_V10_20200325	Layer: 6 DDR number: Support 1pcs 200 balls LPDDR4 chip

**Note**

The layout of DDR is completely copied from "RV1126_RV1109_Template". For the related design files, please refer to the hardware part of the release package. If customers design their own DDR template, please make sure to double check with RK.

Take LPDDR3 as an example:

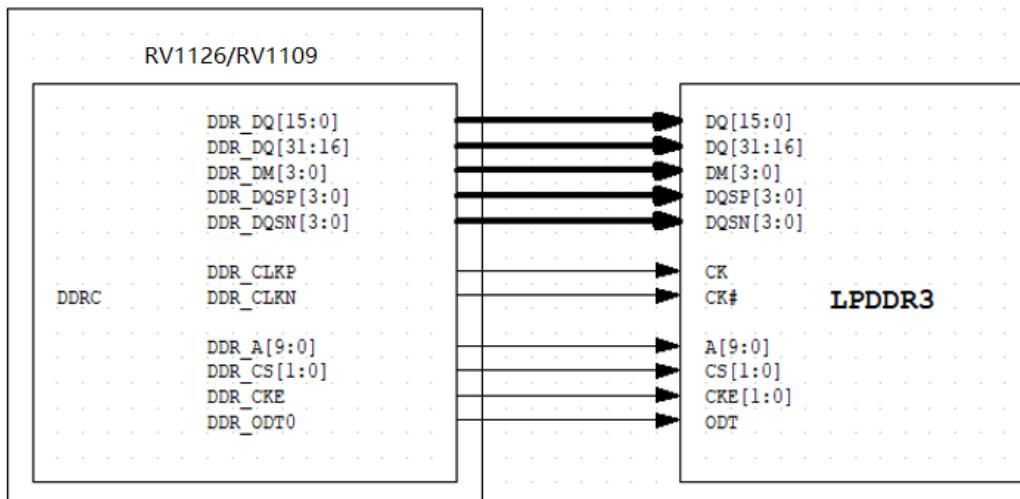


Figure 2-10 LPDDR3 Topological connection mode

Matching design suggestions:

- DQ and DQS bidirectional signals: DQ and DQS_P/N signals in the RV11XX application are all point-to-point topologies, just connect directly.
- Differential clock: please two 49.9ohm resistors across the boundary near the end of the DDR.

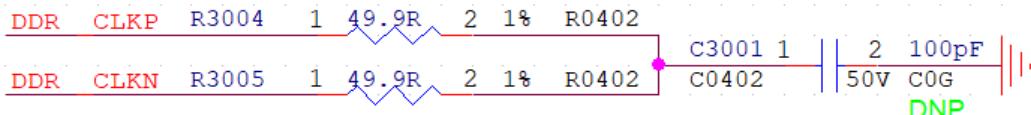


Figure 2-11 DDR_CLK series resistances

- Address signal and command: For example, when designing two 16bit DDR, the T-type topology address and command can be directly connected. The address and command signal of the fly-by topology sometimes have series resistances. The resistances value are based on simulation and test. At present, the DDR3 fly-by template of 4 layers connect 49.9 Ohm resistors in series.
- The external resistance ZQ selects 240ohm, with accuracy 1%.

2.1.10.3 DDR Power up Sequence Requirement

There is only one group of power supply of RV11XX DDR controller:

- DDRIO_VDD: I/O power supply for DDR controller

SDRAM include two groups of power supplies, please refer to JEDEC standards for power-on sequence:

- The power-up sequence of DDR3 SDRAM is shown below:

1. Apply power (RESET# is recommended to be maintained below $0.2 \times VDD$; all other inputs may be undefined). RESET# needs to be maintained for minimum 200 us with stable power. CKE is pulled "Low" anytime before RESET# being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp, $VDD > VDDQ$ and $(VDD - VDDQ) < 0.3$ volts.
 - VDD and VDDQ are driven from a single power converter output, AND
 - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
 - Vref tracks VDDQ/2.

OR

- Apply VDD without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

Figure 2-12 DDR3 SDRAM Power up Sequence

- The power-up sequence of LPDDR3 SDRAM is shown in the figure below:

After...	Applicable Conditions
Ta is reached	V_{DD1} must be greater than $V_{DD2} - 200mV$
	V_{DD1} and V_{DD2} must be greater than $V_{DDCA} - 200mV$
	V_{DD1} and V_{DD2} must be greater than $V_{DDQ} - 200mV$
	V_{Ref} must always be less than all other supply voltages

Figure 2-13 LPDDR3 SDRAM power up sequence

- The power-up sequence of DDR4 SDRAM is shown in the figure below:

1. Apply power (RESET_n is recommended to be maintained below $0.2 \times VDD$; all other inputs may be undefined). RESET_n needs to be maintained for minimum 200us with stable power. CKE is pulled "Low" anytime before RESET_n being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to V_{DD} min must be no greater than 200ms; and during the ramp, $V_{DD} \geq V_{DDQ}$ and $(V_{DD} - V_{DDQ}) < 0.3$ volts. VPP must ramp at the same time or earlier than VDD and VPP must be equal to or higher than VDD at all times.
 - V_{DD} and V_{DDQ} are driven from a single power converter output, AND
 - The voltage levels on all pins other than $V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ}$ must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side. In addition, V_{TT} is limited to TBDV max once power ramp is finished, AND
 - VrefCA tracks TBD.
 - or
 - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}
 - Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} & VrefCA.
 - Apply VPP without any slope reversal before or at the same time as VDD.
 - The voltage levels on all pins other than $V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ}$ must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.

Figure 2-14 DDR4 SDRAM power up sequence

- The power-up sequence of LPDDR4 SDRAM is shown in the figure below:

The following sequence shall be used to power up the LPDDR4 device. Unless specified otherwise, these steps are mandatory. Note that the power-up sequence of all channels must proceed simultaneously.

1. While applying power (after Ta), RESET_n is recommended to be LOW ($\leq 0.2 \times VDD2$) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table 4. VDD1 must ramp at the same time or earlier than VDD2. VDD2 must ramp at the same time or earlier than VDDQ.

Table 4 — Voltage Ramp Conditions

After	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ - 200mV

NOTE 1 Ta is the point when any power supply first reaches 300mV.

NOTE 2 Voltage ramp conditions in Table 4 apply between Ta and power-off (controlled or uncontrolled).

NOTE 3 Tb is the point at which all supply and reference voltages are within their defined ranges.

NOTE 4 Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.

NOTE 5 The voltage difference between any of Vss and Vssq pins must not exceed 100mV.

Figure 2-15 LPDDR4 SDRAM power up sequence

2.1.10.4 DDR Support List

The maximum working frequency of RV11XX DDR interface supports up to 1066MHz. For the DDR support list, please refer to the document "RK DDR Support List", which can be downloaded on our redmine platform: https://redmine.rockchip.com.cn/projects/fae/documents?tdsourcetag=s_pcim_aiomsg

2.1.11 eMMC Circuit Design

2.1.11.1 eMMC Controller Introduction

The RV11XX eMMC interface supports eMMC 4.51 and is compatible with 4.41 with the following features:

- Compatible with standard INAND interface;

- Support three data bus widths of 1-bit, 4-bit and 8-bit;
- The maximum rate is 150MB/s;

2.1.11.2 eMMC Topology and Connection Mode

eMMC interface supports interface pull-up and pull-down and matching design recommendations as shown in Table 2-5:

Table 2-7 eMMC interface design

signal	Internal pull up/down	Connection method	Description(chipset)
eMMC_DQ[7:0]	pull up	direct connection, D0 external pull-up with a 4.7K resistor	eMMC data send and receive
eMMC_CLK	pull up	connection a 22ohm resistor in series	eMMC clock send
eMMC_CMD	pull up	direct connection, external pull-up with 4.7K resistor	eMMC command send and receive

2.1.11.3 eMMC Power up Sequence Requirement

The eMMC controller of RV11XX belongs to VCCIO1_VDD power domain:

- VCCIO1_VDD: The I/O power supply of eMMC controller. Pay attention to that this power supply should match the level configuration of FLASH_VOL_SEL mentioned above.

The eMMC have two power supplies, please refer to JEDEC standard for power-on sequence:

- VCC and VCCQ have no power-on sequence requirements;
- VCC and VCCQ should be powered on before the CMD command of RV1126/RV1109RV11XX is sent, and maintain a stable operating voltage;
- After the eMMC enters sleep mode, RV1126/RV1109RV11XX can turn off the VCC power supply to reduce power consumption;
- Before the eMMC waking up from sleep mode, the VCC power supply must be powered on and maintain a stable operating voltage;

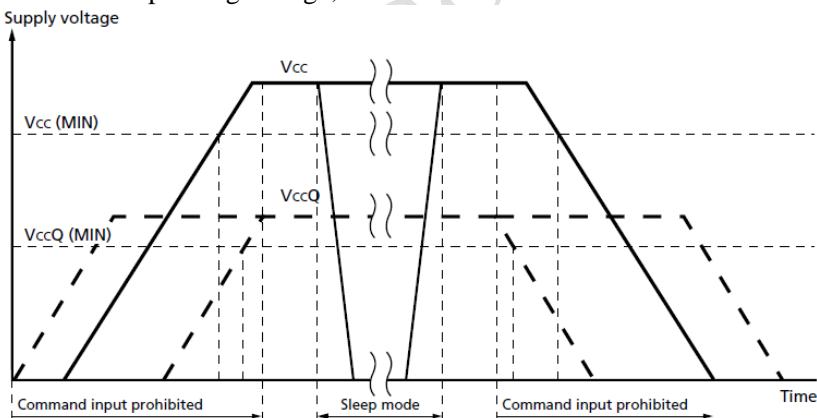


Figure 2-16 eMMC power up and power down sequence

2.1.11.4 eMMC Support List

For RV11XX eMMC support list, please refer to the document "RK eMMCSupportList", which can be downloaded on our redmine platform:

https://redmine.rockchip.com.cn/projects/fae/documents?tdsourcetag=s_pctim_aiomsg

2.1.12 SLC NAND Flash Circuit Design

2.1.12.1 NAND Controller Introduction

NANDC supports the following features:

- Only supports SLC FLASH, does not support MLC, TLC Nand Flash;
- Supports 8-bit data width asynchronous flash interface.
- Only single chip select devices are supported.
- Support 16-bit BCH/ECC.

2.1.12.2 NAND Topology and Connection Mode

Table 2-8 lists the recommendation for pull-up and pull-down and matching design of NAND interface.

Table 2-8 NAND Flash interface design

Signal	Internal pull up/down	Connection mode	Description(chipset)
Flash_DQ[7:0]	pull up	direct connection	NAND FLASH data
Flash_CS0n	pull up	direct connection	CS signal of NAND FLASH
Flash_WRn	pull up	direct connection	NAND FLASH Write enable
Flash_CLE	pull down	direct connection	NAND FLASH command latch enable
Flash_ALE	pull down	direct connection	NAND FLASH address latch enable
Flash_RDYn	pull up	direct connection, pull up with a 4.7K resistance	NAND FLASH Ready/busy
Flash_RDn	pull up	direct connection	NAND FLASH Read enable
Flash_WPn	pull down	direct connection	NAND FLASH Write protect

2.1.12.3 NAND Power-on Sequence Requirements

NAND Flash controller of RV11XX chip belongs to VCCIO1_VDD power domain:

- VCCIO1_VDD: for I/O power of NAND Flash controller, please pay attention to match the level configuration of FLASH_VOL_SEL mentioned above.

NAND Flash have two power supplies, please refer to JEDEC standard for power-on sequence:

Once V_{CC} and V_{CCQ} reach the V_{CC} minimum and V_{CCQ} minimum values, respectively, listed in Table 5 and power is stable, the R/B_n signal shall be valid after RB_valid_Vcc and shall be set to one (Ready) within RB_device_ready, as listed in Table 16. R/B_n is undefined until 50 μ s has elapsed after V_{CC} has started to ramp. The R/B_n signal is not valid until both of these conditions are met.

Parameter	Raw NAND	EZ NAND
RB_valid_Vcc	10 μ s	250 μ s
RB_device_ready	1 ms	2 ms

Table 16 R/B_n Power-on Requirements

During power-on, V_{CCQ} shall be less than or equal to V_{CC} at all times. Figure 19 shows V_{CCQ} ramping after V_{CC} , however, they may ramp at the same time.

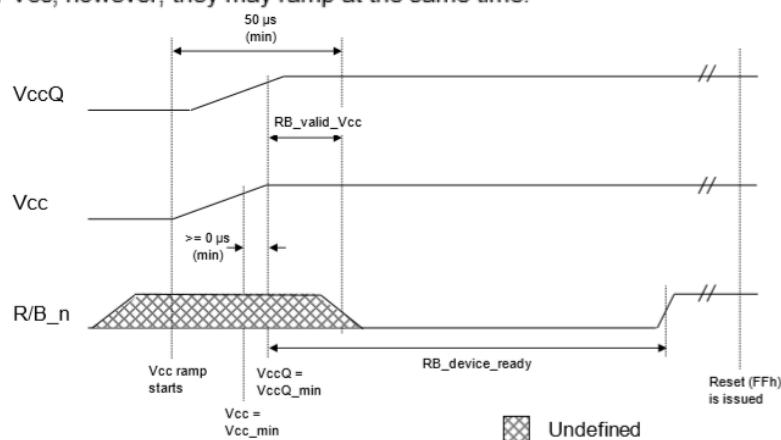


Figure 19 R/B_n Power-On Behavior

Ready/Busy is implemented as an open drain circuit, thus a pull-up resistor shall be used for termination. The combination of the pull-up resistor and the capacitive loading of the R/B_n circuit determines the rise time of R/B_n.

Figure 2-17 NAND FLASH power-on sequence

2.1.12.4 Flash Support List

For RV11XX NAND Flash support list, please refer to the document "RK SpiNor and SLC NAND Support List", which can be downloaded on our redmine platform:

https://redmine.rockchip.com.cn/projects/fae/documents?tdsourcetag=s_pctim_aiomsg

2.1.13 FSPI Circuit Design

2.1.13.1 FSPI Controller Introduction

FSPI is a flexible serial peripheral interface host controller and external devices interfaces. FSPI supports the following features:

- Support serial NOR and NAND FLASH;
- Support SDR mode, support single/dual/four-line mode;
- Support 2 chip selects

VCCIO1_VDD: I/O power supply of SPI Flash controller, please pay attention to match the level configuration of FLASH_VOL_SEL mentioned above.

2.1.13.2 FSPI Topology and Connection Mode

Table 2-9 shows the recommendation of pull-up and pull down and match design of FSPI interface.

Table 2-9 FSPI interface design

Signal	Internal pull up/down	Connection method	Description(chipset)
FSPI_DQ0/SI	pull up	direct connection	Data0 of SPI FLASH
FSPI_DQ1/SO	pull up	direct connection	Data1 of SPI FLASH
FSPI_DQ2/WP#	pull up	direct connection, pull up to VCC with a 10K resistance	Data2 of SPI FLASH
FSPI_DQ3/HOLD#	pull down	direct connection, pull up to VCC with a 10K resistance	Data3 of SPI FLASH
FSPI_CS0n/CS1n	pull down	direct connection	CS signal of SPI FLASH
FSPI_CLK	pull up	direct connection with a 22ohm resistance in series	Clock signal of SPI FLASH

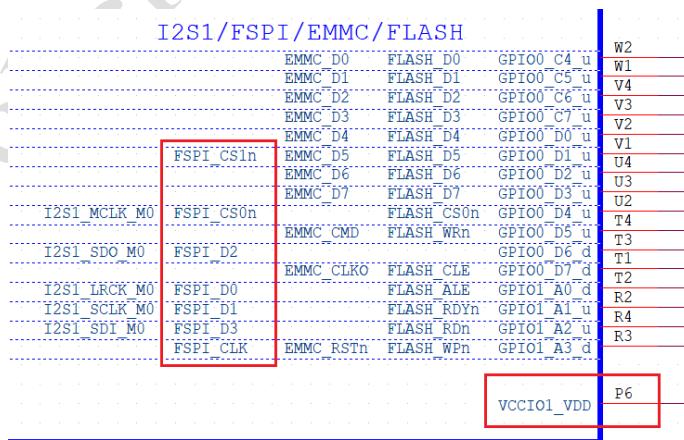


Figure 2-18 RV11XX FSPI Control module



Note

As shown in Figure 2-16, FSPI_CSIN is reused with EMMC_D5, and other pins of FSPI are not reused with EMMC. In a certain application case, EMMC and SPI FLASH can be used at the same time.

2.2 Power Supply Design Recommendations

For design parameters of RV11XX power supply, please refer to the Electrical Performance Parameters section of "Rockchip RV1126 Datasheet". RV11XX takes PMIC RK809-2 as power supply solution. If other power supply solution are used, please refer to 2.1.7 power supply timing sequence for power-on sequence.

2.2.1 PMIC RK809-2 Solution Introduction

2.2.1.1 RK809-2 Block Diagram

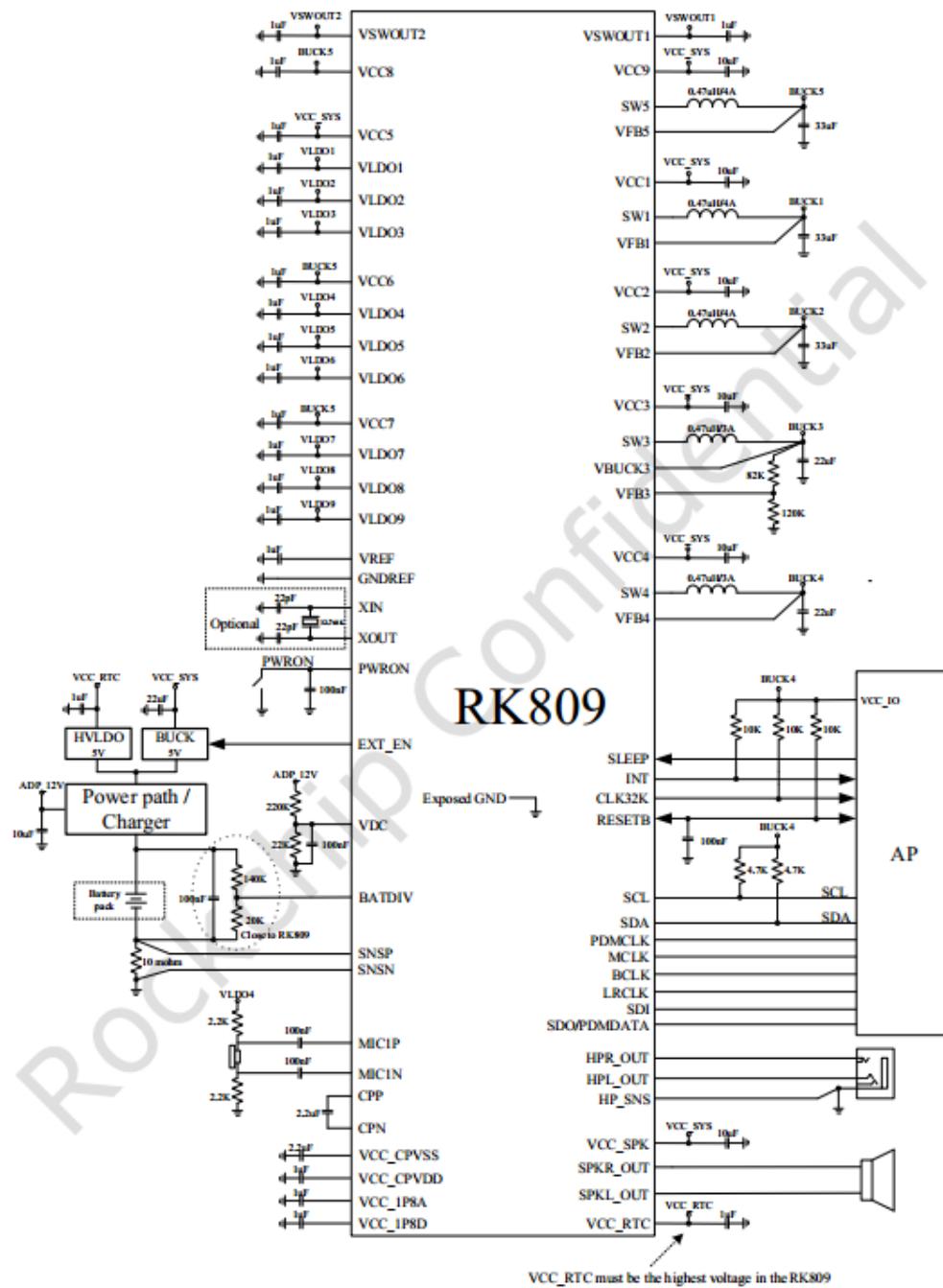


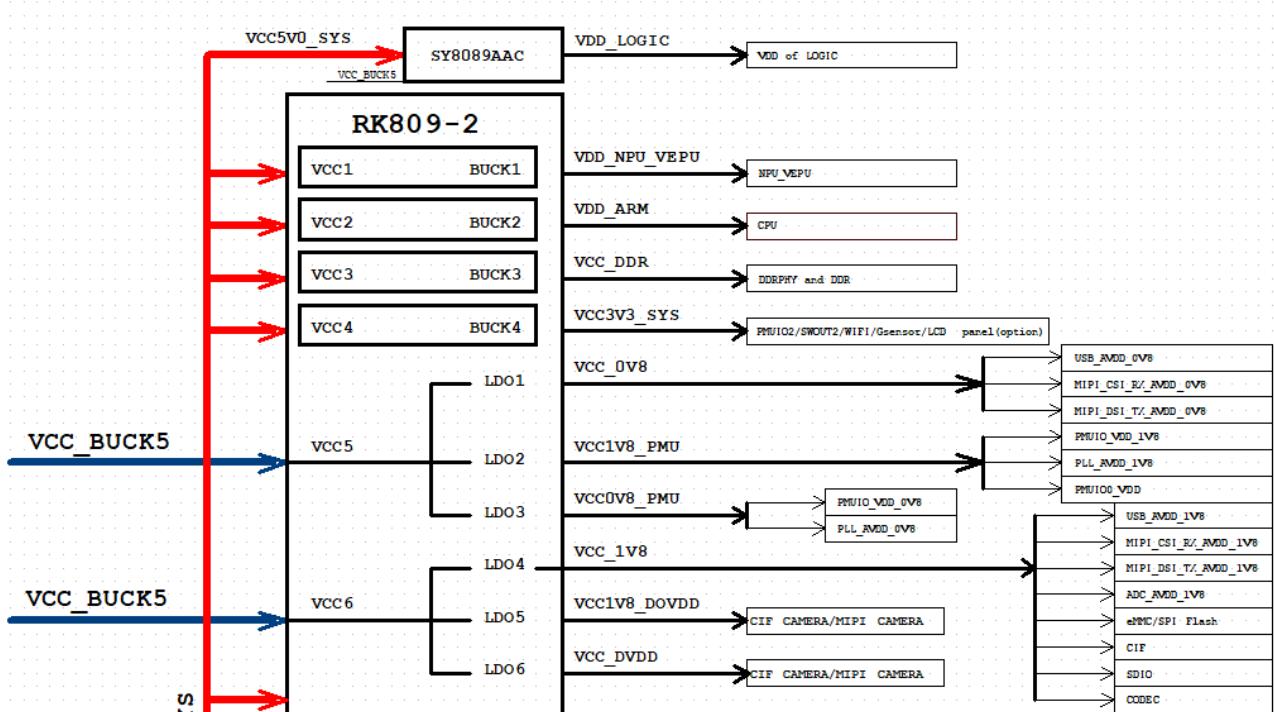
Figure 2-19 RK809-2 block diagram

2.2.1.2 RK809-2 Features

- Power input range is from 2.7V to 5.5V
- Precision fuel gauge with two independent battery voltage and current ADCs
- Built-in real-time clock (RTC)
- Low standby current of 16uA (at 32KHz clock frequency)

- Earphone driver output in real time
- 1.3W Class D amplifier without filter inductor
- Fixed and programmable power supply boot sequence control
- Built-in high-performance audio codec
 - ◆ Built-in independent PLL
 - ◆ Support microphone input
 - ◆ Both DAC and ADC support I2S digital input
 - ◆ Support ALC, limiter and noise gate
 - ◆ Supports programmable digital and analog gain
 - ◆ Support 16bits-32bits bit rate
 - ◆ Sampling rate up to 192kHz
 - ◆ The software supports two working mode configurations of master and slave
 - ◆ Supports 3 I2S formats (standard, left aligned, right aligned)
 - ◆ Support PDM mode (external input PCLK)
- Power channels:
 - ◆ Channel 1: synchronous step-down DC-DC converter, 2.5A max
 - ◆ Channel 2: synchronous step-down DC-DC converter, 2.5A max
 - ◆ Channel 3: synchronous step-down DC-DC converter, 1.5A max
 - ◆ Channel 4: synchronous step-down DC-DC converter, 1.5A max
 - ◆ Channel 5: synchronous step-down DC-DC converter, 2.5A max
 - ◆ Channel 6-7, 9-14: low dropout linear regulator, 500mA max
 - ◆ Channel 8: low noise, high power supply rejection ratio low dropout linear regulator, 100mA max
 - ◆ Channel 15: switch, 3A max
 - ◆ Channel 16: Switch, 1.5A max
- package: 7mmx7mm QFN68

2.2.1.3 RV11XX+RK809-2 Power Tree



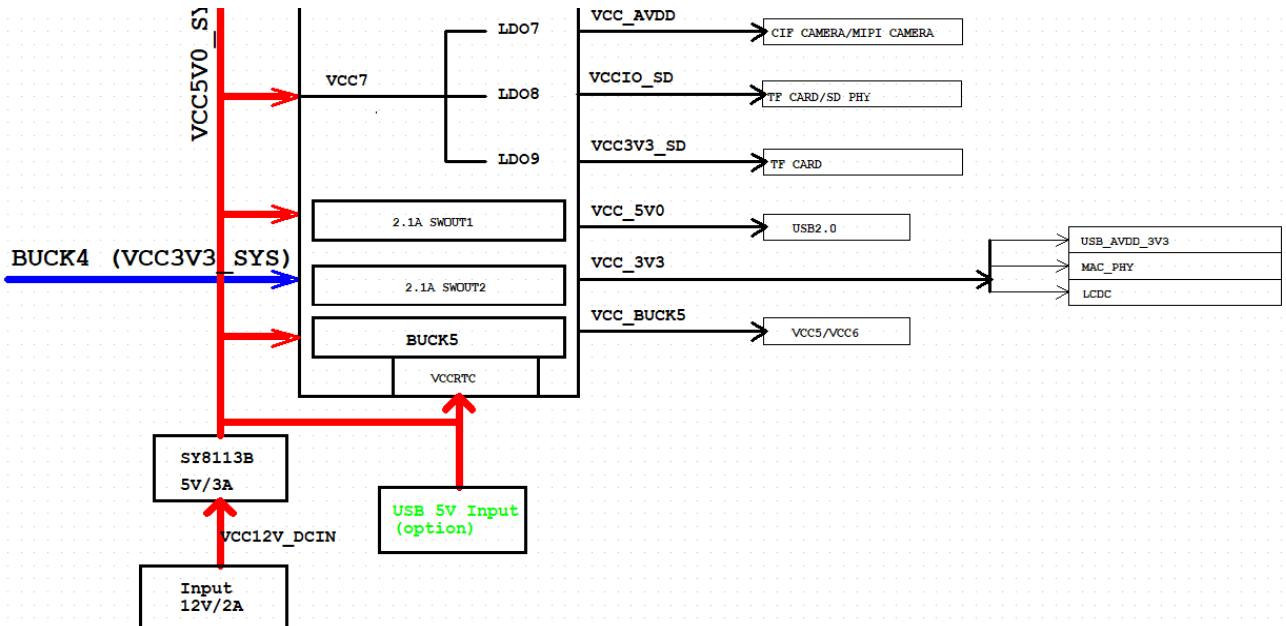


Figure 2-20 RK809-2 Power framework

The reference power on sequence of RK809-2 and discrete BUCK

Power Name	PMIC Channel	Time (step=2ms)	Default voltage	Supply Limit	Default ON/OFF	Sleep ON/OFF	Peak Current
VCC_BUCK5	RK809-2 BUCK5	Slot: 1	2.2V	2.5A	ON	ON	
VCC0V8_PMU	RK809-2 LDO3	Slot: 2	0.8V	0.1A	ON	ON	
VCC_0V8	RK809-2 LDO1	Slot: 2	0.8V	0.4A	ON	OFF	
VDD_ARM	RK809-2 BUCK2	Slot: 2	0.8V	2.5A	ON	OFF	0.73A@1.8GHz
VDD_NPU	RK809-2 BUCK1	Slot: 2	0.8V	2.0A	ON	OFF	1.34A@934MHz
VDD_VEPU	RK809-2 BUCK1	Slot: 2	0.8V	2.0A	ON	OFF	0.77A@700MHz
VDD_LOGIC	Ext(SY8089AAC)	Slot 1+3ms	0.8V	2.5A	ON	ON	1.75A
VCC_DDR	RK809-2 BUCK3	Slot: 3	1.5V	1.5A	ON	ON	
VCC1V8_PMU	RK809-2 LDO2	Slot: 3	1.8V	0.4A	ON	ON	
VCC_1V8	RK809-2 LDO4	Slot: 3	1.8V	0.4A	ON	OFF	
VCC3V3_SYS	RK809-2 BUCK4	Slot: 4	3.3V	1.5A	ON	ON	
VCC_3V3	RK809-2 SWOUT2	Slot: 4	3.3V	1.5A	ON	OFF	
VCCIO_SD	RK809-2 LDO8	Slot: 4	3.3V	0.4A	ON	OFF	
VCC3V3_SD	RK809-2 LDO9	Slot: 4	3.3V	0.4A	ON	OFF	
VCC1V8_DVDD	RK809-2 LDO5		1.8V	0.4A	OFF	OFF	
VCC_DVDD	RK809-2 LDO6		1.2V	0.4A	OFF	OFF	
VCC_AVDD	RK809-2 LDO7		2.8V	0.4A	OFF	OFF	
VCC5V0_HOST	RK809-2 SWOUT1		5V	2.1A	ON	OFF	
RESET	RK809-2	sent out Reset signal for soc(SLOT:5(10ms))					

NOTE: VCC_DVDD and VCC_AVDD according to camera sensor voltage

Figure 2-21 RK809-2 Power sequence

2.2.1.4 Note on RK809-2

- The recommended value of the matching capacitance of the 32.768 crystal is 22pF. Customers can fine-tune this parameter according to the specifications of the crystal they used;



Note

In order to reduce power consumption, the crystal oscillation of PMIC RTC is relatively weak. The oscillation signal cannot be measured with a common oscilloscope on XOUT or XIN pin, or it will stop vibration as soon as an oscilloscope probe touches. To measure 32.768k, please test the CLK32K pin. VCC_RTC must be the first power supply, which should be the highest one of the input power supplies to RK809-2

- VCC_RTC must be the first power supply, which should be the highest one of the input power supplies to RK809-2;
- The output capacitors of BUCK1 and BUCK2 should be greater than 22uF to guarantee good decoupling effect, especially in high current and heavy loading cases, it is better to increase output decoupling capacitor value;
- RK809-2 supports built-in USB OTG power supply function, with short circuit protection function

- and 1.0-1.5A configurable output current limited;
- The boot logic directly controlled by input power supply is as follows: when there is a power input, the primary DCDC step-down outputs VCC5V0_SYS and VCC_RTC. When the power supply inputting to VDC after passing through the external voltage divider circuit and is greater than 0.55V. The PMIC starts to work and output voltage;
- Power on and off logic controlled by buttons is as follows: PWRON pin has a built-in pull-up resistors to pull up to VCCRTC, and it will automatically power on when the low level is detected for more than 500ms; if the PWRON pin is pulled down for more than 6s after start, it will be forced to shut down (It is usually used for forced shutdown and restart after system crash); during standby and awake operations, the low level of PWRON pin should be maintained for more than 20ms.
- Basic conditions for RK809-2 work:
 - ◆ VCC_RTC power supply;
 - ◆ VCC5V0_SYS power supply,
 - ◆ One of the following three conditions is detected, RK809-2 automatically turns on: PWRON pin is low and maintains 500mS; VDC level exceeds 0.55V; internal RTC Alarm is enabled by default and the time is up.
 - ◆ Turn on power-up process, each timing interval is 2mS, it will continue to the next sequence after the previous sequential voltage output meets the requirements, until all timing sequence finishing power-up, and release reset to complete the power-up process;
- If RK809-2 detects one of the following two situations, it will automatically shut down:
 - ◆ I2C writes DEVICE_OFF=1;
 - ◆ PWRON pin is low more than 6s
- After the RK809-2 starts the power-off process, it will pull down the reset after 1 RTC clock cycle (after about 30.5us), and then turn off all power outputs at the same time after 2ms to complete the power-off process;

2.2.1.5 RK809-2 Design Instructions

For detailed design instructions of RK809-2, please refer to RK PMIC design document "AN_RK809_V1.1_20200310".

2.2.2 Power Design Recommendations

The capacitance value and quantity of LOGIC, ARM, NPU, VEPU, PLL, DDR are required to refer to the reference design strictly.

2.2.2.1 PLL Power Supply Design

PLL power supply of RV11XX:

Table 2–10 PLL Power supply

Power supply	Standby state
PLL	PLL_AVDD_0V8, PLL_AVDD_1V8

There are two power supplies for PLL, they are PLL_AVDD_0V8 and PLL_AVDD_1V8. Decoupling capacitors should be used in the design and placed close to the pins. It is recommended to use LDO to supply power for PLL separately. Especially when DDR operating frequency is high, a stable PLL power supply will help to improve working stability of SOC. Note that the decoupling capacitors should be placed near the pins.

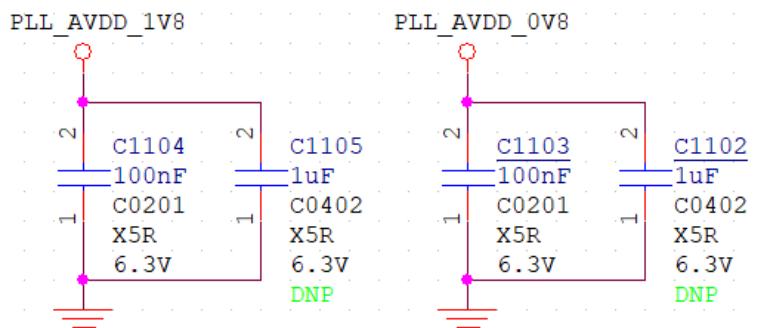


Figure 2-22 RV11XX PLL Power

2.2.2.2 ARM Power Design

The typical value of RV11XX ARM power supply is 0.8V, and the actual voltage will be controlled according to the SDK dynamic voltage regulation parameters. The higher the frequency, the higher the voltage. It is designed according to the reference design. It is not recommended to combine with other power sources .It requires that the power supply capacity is not less than 1A when selecting the power chip. Please do not delete the capacitors in the reference schematic. Place the large capacitor on the back of the RV11XX chip as much as possible during layout (please place it close to the chip when is single-sided SMT). The capacitances are shown in the following figure:

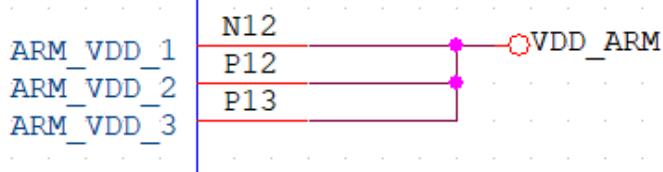


Figure 2-23 RV11XX VDD_ARM power

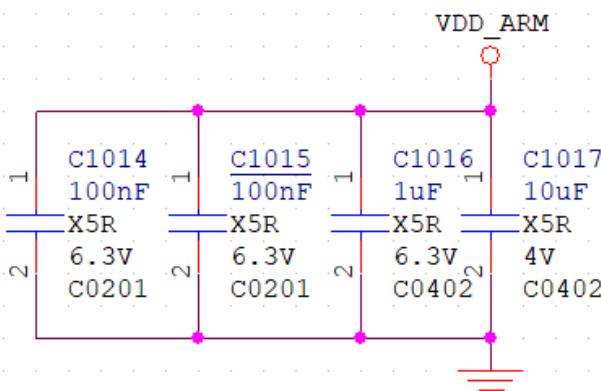


Figure 2-24 Decoupling capacitors of RV11XX VDD_ARM Power supply

2.2.2.3 LOGIC Power Design

The typical value of RV11XX LOGIC power supply is 0.8V. Dynamic voltage regulation is not allowed. It is not recommended to combine with other power supply. Please design according to the reference drawing .It requires that the power supply capacity is not less than 2A when selecting the power chip. Please do not delete the capacitors in the reference schematic. Place the large capacitors on the back of RV11XX chip as much as possible during layout (please place them close to the chip when is single-sided SMT). The capacitances are shown in the following figure:

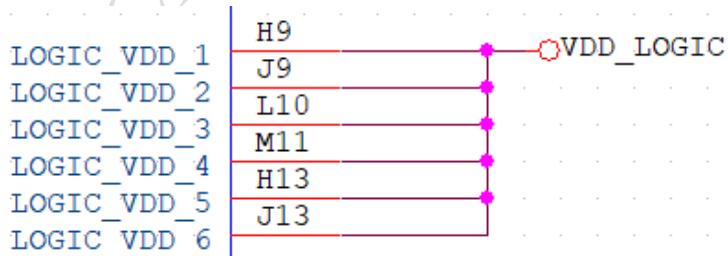


Figure 2-25 RV11XX VDD_LOGIC Power supply

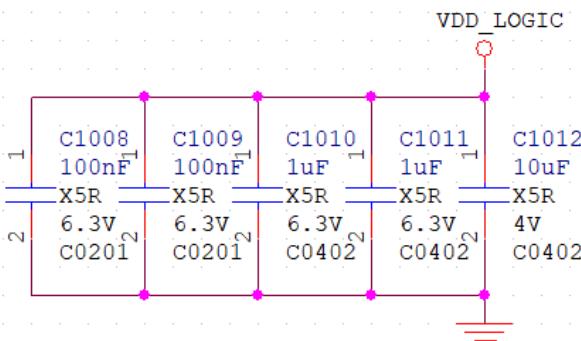


Figure 2-26 Decoupling capacitors of RV11XX VDD_LOGIC power supply

2.2.2.4 NPU Power Design

The typical value of the RV11XX NPU power supply is 0.8V, and the actual voltage is controlled according to the SDK dynamic voltage regulation parameters. NPU and vepu power supply can be combined according to the actual product situation. It requires that the power supply capacity is not less than 2A when selecting the power chip. Please do not delete the capacitors in the reference schematic. Place the large capacitors on the back of the RV11XX chip as much as possible during layout (please place them close to the chip when is single-sided SMT). The capacitances are shown in the following figure:

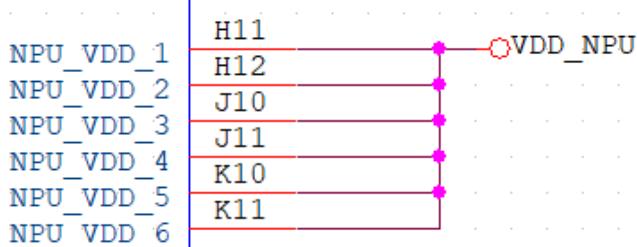


Figure 2-27 RV11XX VDD_NPU Power supply

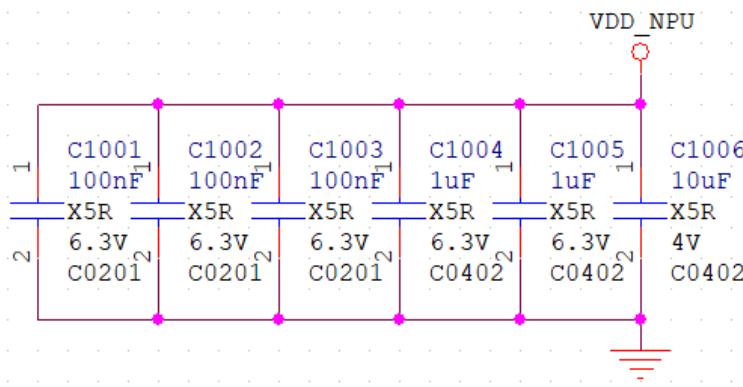


Figure 2-28 Decoupling capacitors of RV11XX VDD_NPU power supply

2.2.2.5 VEPU Power Design

The typical value of RV11XX VEPU power supply is 0.8V, and the actual voltage is controlled according to the SDK dynamic voltage regulation parameters. NPU and vepu power supply can be combined according to the actual product situation. It requires that the power supply capacity is not less than 1.0A when selecting the power chip. Please do not delete the capacitors in the reference schematic. Please place large capacitors on the back of the RV11XX chip during layout (please place them close to the chip when is single-sided SMT) to avoid large power ripple caused by large load. The capacitor is shown in the following figure:

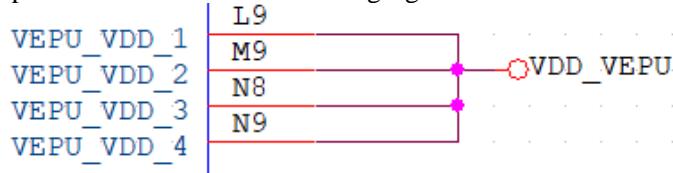


Figure 2-29 RV11XX VDD_VEPU power

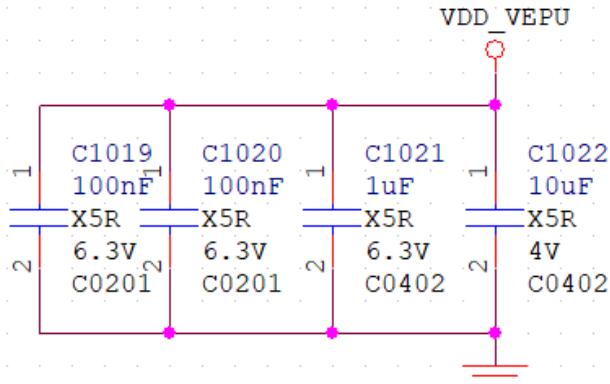


Figure 2-30 Decoupling capacitors of chip VDD_VEPU power

2.2.2.6 Dynamic Voltage Regulation

The ARM/NPU/VEPU power supply of RX11XX should add dynamic voltage regulation function in the following way:

- If it is powered by RK809-2, PMIC can be used for dynamic voltage regulation;
- If ARM, NPU and VEPU are powered by separate power supplies, dynamic voltage regulation can output 0~3.3V different voltage DC level through PWM waveform output pin and RC filter. The DC level is added to the feedback voltage input of DCDC through resistance network to realize DC-DC output voltage regulation. The PWM frequency and duty cycle can be changed through RV11XX related registers, and finally the output voltage of the DC-DC will be dynamically adjusted.

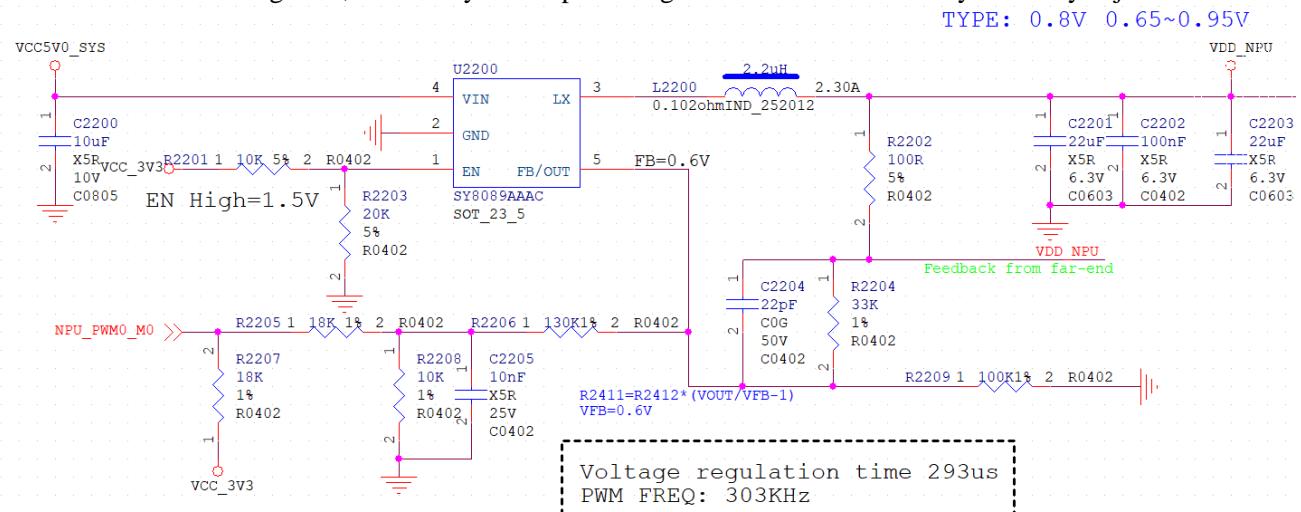


Figure 2-31 PWM Voltage Regulation

Please pay attention to the following items in the design:

- The DC voltage value error of VCC_3V3 power supply should not exceed $\pm 50\text{mV}$.
- The calculated value is a reference value. The actual resistance value can be around the calculated value, but should be as close as possible.
- The accuracy of all resistors is 1%.
- It is required that the selected DC-DC reference voltage Vref is less than 0.65V, and the accuracy tolerance of DCDC Vref should not exceed 2%.

2.2.2.7 DDR Power Design

- The DDR controller interface of RV11XX chip supports DDR3/DDR3L/DDR4/LPDDR3/LPDDR4.
- The typical voltage value of DDR3 is 1.5V, the typical voltage value of DDR3L is 1.35V, the typical voltage value of LPDDR3 is 1.2V, the typical voltage value of DDR4 is 1.2V, and the typical voltage value of LPDDR4 is 1.1V. The power supply of DDR and the DDR IO power of RV11XX are required to be in the same power network. Please do not delete the capacitors in the reference schematic.
- The RV11XX DDR controller integrates a Vref circuit, which can supply VREF voltage to the controller or DDR. According to the different states of different DDR in application, the VREF voltage value will be dynamically adjusted in software driver. Please place a 1nF decoupling capacitor next to each reference power pin.
- Vref_CA is generated by VCC_DDR through a voltage divider resistor, and the resistance accuracy is 1%.

For example: Vref_CA at the LPDDR3 SDRAM end can be generated by a resistor divider circuit, and $V_{ref_CA} = V_{CC_DDR}/2$, and Vref_DQ needs to be adjusted according to ODT strategy, and the corresponding Vref voltage can be adjusted according to the driving strength and ODT value. At 800MHz frequency, the driving strength of the chip is 34.3ohm, and the ODT of SDRAM is 240ohm, so when ODT is enabled, the SDRAM $V_{ref} = 0.56 * V_{CC_DDR}$ is calculated according to the formula. This voltage can be directly provided by Pin M6.

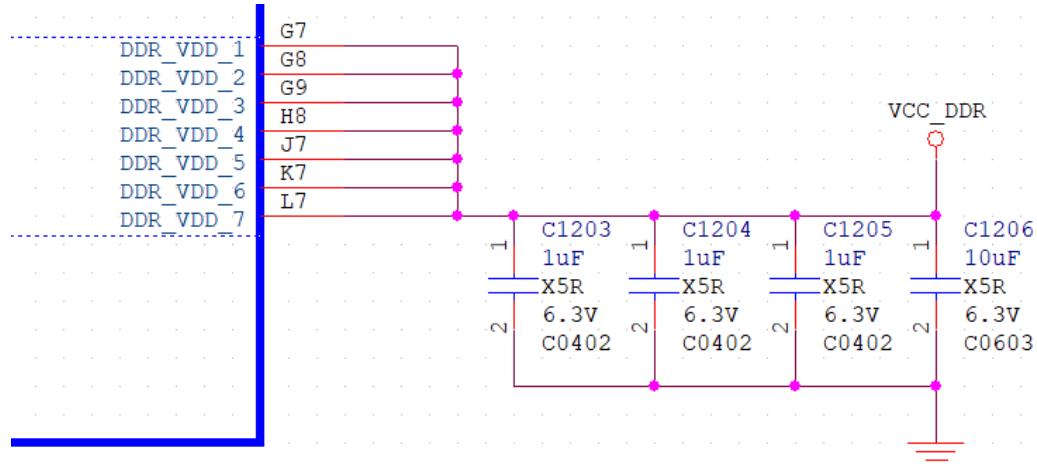


Figure 2-32 RV11XX VCC_DDR power

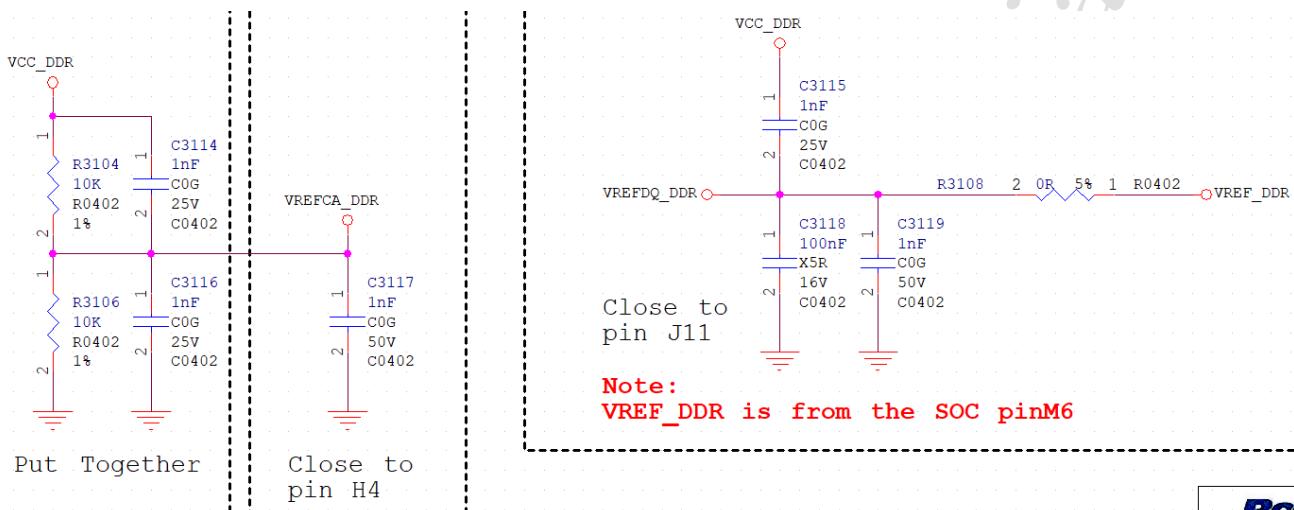


Figure 2-33 VREF power supply design of LPDDR3 SDRAM



Note

About the Vref_DQ design of different DDR:

DDR4 Vref_DQ can be adjusted by the software in the component. When the ODT function of DDR3/DDR3L is enabled, it will be internally pulled up and down at the same time. $Vref_DQ = Vref_CA = VCC_DDR/2$; LPDDR4 has no Vref voltage; so only LPDDR3 needs to adjust Vref_DQ separately

2.2.2.8 GPIO Power Design

In RV11XX, the GPIO type is configurable to 1.8V/3.3V.

In RV11XX, there are two types of GPIO, one type of GPIO provides 4 levels of adjustable driving strength, and the other type of GPIO provides 16 levels of adjustable driving strength. Depending on different types of GPIO, the initial default driving strength are also different. Please refer to chip TRM for configuration modification, or refer to Table 3 "Pin Control Registers" and Table 4 "Pin Default Status" in the "RV1126_RV1109_PINOUT_EN" document.

- The name of IO power pin, such as VCCIO1_VDD, the level of the VCCIO1 power domain supports 3.3V/1.8V. The pin names of other IO power are: VCCIO2_VDD, VCCIO3_VDD, VCCIO4_VDD, VCCIO5_VDD, VCCIO6_VDD, VCCIO7_VDD.
- VCCIO1/2/3/4/5/6/7_VDD support 3.3V/1.8V.
- VCCIO_VDD_1V8 is the common power supply in VCCIO1/2/3/4/5/6/7 power domain. As long as the GPIO in VCCIO1~VCCIO7 power domain is used, this pin must be powered.
- IO level of PMUIO0 power domain (pin name is PMUIO0_VDD): support 3.3V/1.8V.
- IO level of PMUIO1 power domain (pin name is PMUIO1_VDD): support 3.3V/1.8V.
- PMUIO_VDD_1V8 is the common power supply of PMUIO0 and PMUIO1 power domains and

- must be supply with 1.8V.
- PMUIO0_VDD_0V8 is the common power supply for PMUIO and PMUIO1 power domains and must be supply with 0.8V.
- It is recommended to place a 100nF decoupling capacitor on each power supply pin of the power domain and place it close to the power supply pin. For detailed design, please refer to the reference schematic of RV11XX chipset.
- The actual IO level should be consistent with the interface level of the connected chip.

Table 2–11 GPIO Power pins description

Power domain	GPIO Type	Pin name	Description
PUMIO0/PMUIO1	0.8V	PMUIO_VDD_0V8	0.8V logic power for PMUIO0/PMUIO1 domain (group).
	1.8V	PUMIO_VDD_1V8	1.8V power for PMUIO0/PMUIO1 domain (group).
PUMIO0	1.8V/3.3V	PMUIO0_VDD	1.8V or 3.3V IO supply for this GPIO domain (group).
PMUIO1	1.8V/3.3V	PMUIO1_VDD	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO1~VCCIO7	1.8V	VCCIO_VDD_1V8	1.8V power for all VCCIO domain (group).
VCCIO1	1.8V/3.3V	VCCIO1_VDD	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO2	1.8V/3.3V	VCCIO2_VDD	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO3	1.8V/3.3V	VCCIO3_VDD	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO4	1.8V/3.3V	VCCIO4_VDD	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO5	1.8V/3.3V	VCCIO5_VDD	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO6	1.8V/3.3V	VCCIO6_VDD	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO7	1.8V/3.3V	VCCIO7_VDD	1.8V or 3.3V IO supply for this GPIO domain (group).

2.2.3 Power Peak Current Table

The following table is RV11XX peak current evaluation results, for reference only. The test conditions are as follows:

Table 2–12 RV11XX peak current table

Power Supply	Voltage			Max Current value (mA)	Remark
	Min(V)	Typical(V)	Max(V)		
ARM_VDD	TBD	0.8V	TBD	730	
LOGIC_VDD	TBD	0.8V	TBD	1750	
VEPU_VDD	TBD	0.8V	TBD	770	
NPU_VDD	TBD	0.8V	TBD	1340	
DDR_VDD	TBD	TBD	TBD	TBD	Depends on the type of DDR

2.3 Peripheral Interface Design Recommendations

2.3.1 SDMMC Interface

The SDMMC interface controller integrated in RV11XX, supports SD V3.0 and MMC V4.51 protocols, as shown in the figure:

- The SDMMC controller is powered by a separate power domain;
- SDMMC is reused with UART2, JTAG and other functions by SDMMC0_DET for function selection. For details, please refer to section 2.1.4;
- VCCIO2_VDD is IO power, which requires external 3.3V power supply (SD 2.0 mode) or 3.3V/1.8V adjustable power supply (SD 3.0 mode);
- SDMMC_DATA, SDMMC_CMD and SDMMC_CLK connect a 22ohm resistor in series. If the

traces are so short, the resistors can be deleted.

- For ESD devices, please select models with junction capacitance less than 1p
- The decoupling capacitors of 3.3V power supply of the TF card are placed close to the card connector.

NOTE:

Place the SDMMC0_CLK resistor closed to SOC for better signal quality if long trace.
The resistor can be deleted if trace is short.

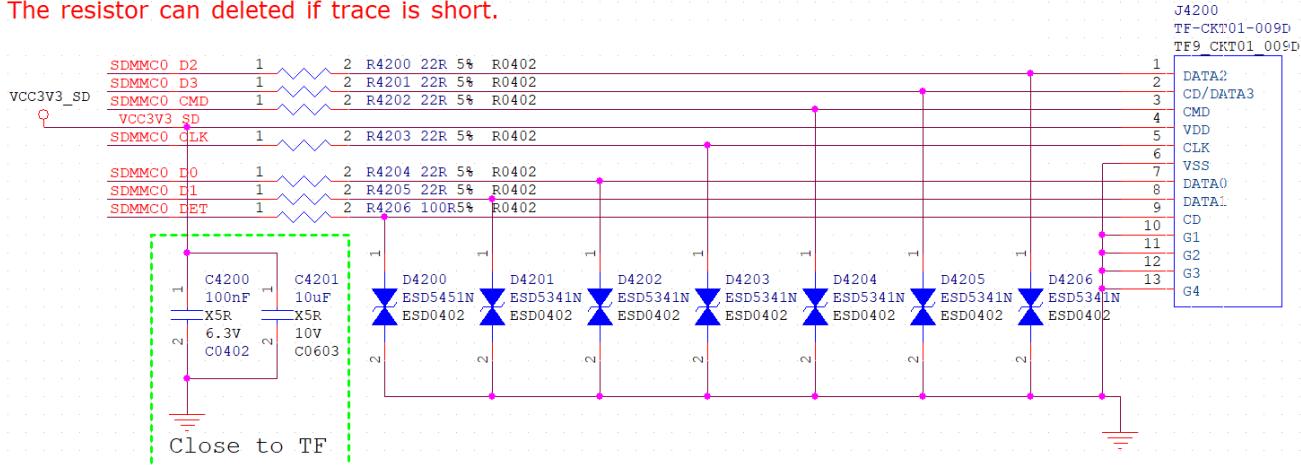


Figure 2-34 RV11XX TF Card

Table 2-11 shows the recommended pull-up and down and matching design of the SDMMC interface:

Table 2-13 SDMMC interface design

Signal	Internal pull up/down	Connection mode	Description(chipset)
SDMMC_DQ[3:0]	pull up	Connect a 22ohm resistor in series which can be deleted when the trace is short	SD data send/receive
SDMMC_CLK	pull up	Connect a 22ohm resistor in series	SD clock send
SDMMC_CMD	pull up	Connect a 22ohm resistor in series which can be deleted when the trace is short	SD command send/receive

2.3.2 SDIO Interface

RV11XX supports WIFI/BT module with SDIO 3.0 interface. Please pay attention to that the power supply of RV11XX SDIO must be consistent with the IO level of the module.

The pull-up and down and matching design recommendations for SDIO interface are shown in the following table:

Table 2-14 RV11XX SDIO interface design

Signal	Internal pull up/down	Connection mode	Description(chipset)
SDIO_DQn[0:3]	pull up	Connect a 22ohm resistor in series which can be deleted when the trace is short	SDIO data send/receive
SDIO_CLK	pull down	Connect a 22ohm resistor in series	SDIO clock send
SDIO_CMD	pull down	Connect a 22ohm resistor in series which can be deleted when the trace is short	SDIO command send/receive

Please refer to the reference schematic for WIFI/BT module design.

2.3.3 Ethernet Interface

- The RV11XX chipset has a built-in GMAC controller, provides RMII interface and RGMII interface, and is compatible with the complete Ethernet interface of the Ethernet physical layer.
- 10/100/1000M Ethernet controller:
 - Support RGMII interface with 10/100/Mbps data transmission rate;
 - Support RMII interface with 10/100 Mbps data transmission rate;
 - Support full-duplex and half-duplex operation;

- Support TCP segment offload (TSO) and UDP segment offload (UFO) network acceleration
- The RGMII function pin is reused in two power domains. The power domain of RGMII_M0 is VCCIO6, and the power domain of RGMII_M1 is VCCIO5 (Note that some pins in this power domain with no GPIO function). Only one group of interfaces can be used at a time. The GMAC power supply VCCIO5 or VCCIO6 can be powered by 1.8V or 3.3V, which must be consistent with the IO level of PHY.
- On RGMII interface send-receive signal line, TX_CLK and RX_CLK are 125MHz. In order to achieve a transmission rate of 1000Mbps, the TXdata and RXdata signal lines are sampled on both sides of the clock. The data enable signals (RGMII_TXEN, RGMII_RXDV) must be enabled before the data is sent validly.
- Reset: RGMII uses GPIO to control the reset mode of PHY. You can also use RC hardware reset circuit. Note that if RC hardware reset circuit is used, the power of PHY must be controllable. GPIO is used to control by default.
- The control and status information transmitted between MAC layer and PHY is the MDIO interface, the clock MDC signal and the data MDIO signal. Noted that the MDIO signal should be pulled up.
- The rules and connection mode of 10/100M are similar to 1000M, except that RGMII_CLK=50M; it should be noted that 10/100M PHY_CRS_DV is connected to RGMII_RXDV, not MAC_CRS pin.
- The RGMII interface can be connected to different Ethernet PHYs to achieve 100M/1000M network functions. For detailed design, please refer to the design document from PHY vendor.

The clock solutions that RMII can provide are shown below:

- First: the external crystal provides a 25MHz clock signal to the Ethernet PHY. The PHY returns a 125MHz clock signal to the RGMII_CLK pin. Note that the PHY and GMAC controller levels must be consistent.
- Second: CLK_OUT_ETHERNET pin provides 25MHz clock signal to Ethernet PHY, and then PHY returns a 125MHz clock signal to RGMII_CLK pin. Note that the PHY and RGMII controller levels must be consistent.
- Third: The CLK_OUT_ETHERNET pin provides a 25MHz clock signal to the Ethernet PHY. The controller outputs a 125MHz clock signal as RGMII_TXCLK. There is no need to return the clock signal from the PHY and the RGMII_CLK pin is useless.
- Fourth: the external crystal provides a 25MHz clock signal to the Ethernet PHY. The controller outputs a 125MHz clock signal as RGMII_TXCLK. There is no need to return the clock signal from the PHY. The RGMII_CLK pin is useless.

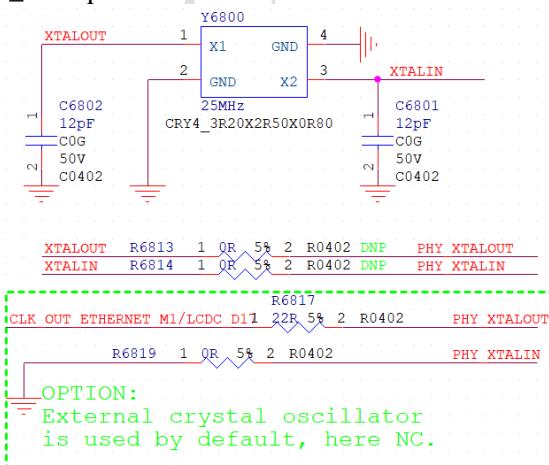


Figure 2-35 RV11XX GMAC Clock circuit

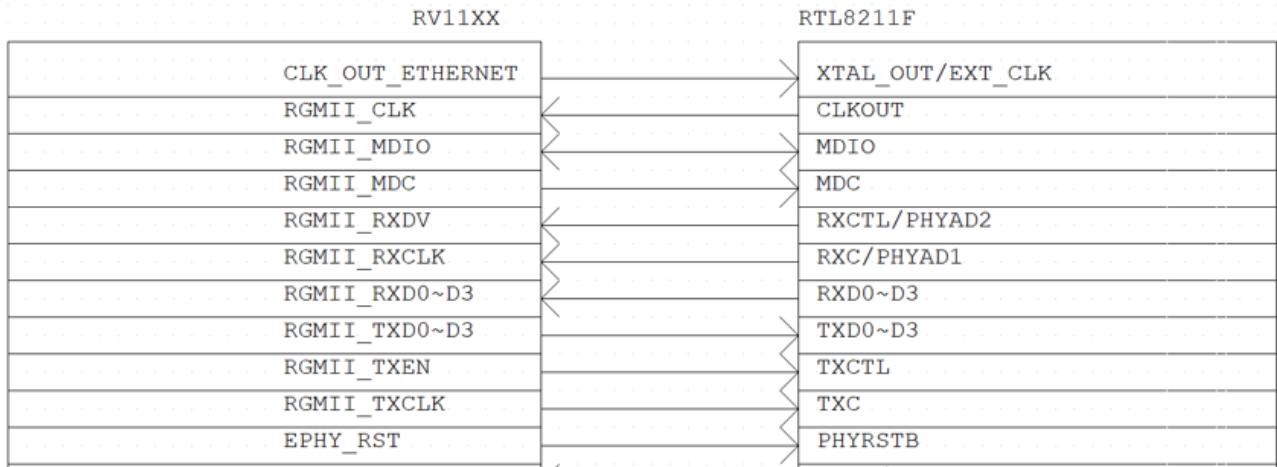


Figure 2-36 RV11XX RGMII signal connection diagram

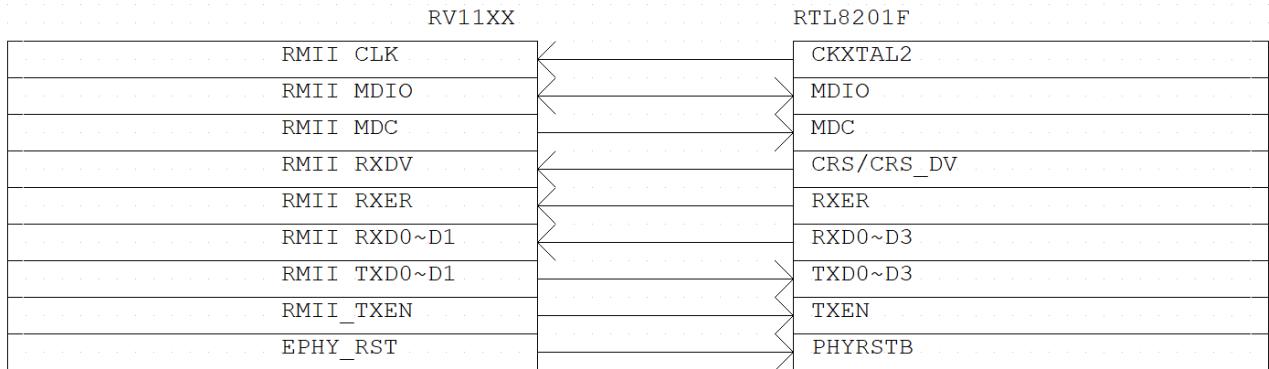


Figure 2-37 RV11XX RMII signal connection diagram

Table 2-15 RV11XX RGMII Interface design

Signal	Internal pull up/down	Connection method	Description(chipset)
CLK_OUT_ETHERNET	pull down	Connect 22ohm resistor in series	Output reference clock to PHY
RGMII_CLK	pull down	Connect 22ohm resistor in series	MAC clock output or external input a clock
RGMII_MDIO	pull down	Connect 22ohm resistor in series	MDIO data
RGMII_MDC	pull down	Connect 22ohm resistor in series	MDIO clock
RGMII_CRS	pull down	Connect 22ohm resistor in series	Physical CRS signal, generally this pin is not needed, just reserved
RGMII_COL	pull down	Connect 22ohm resistor in series	Detected physical collision, generally this pin is not needed, just reserved
RGMII_RXER	pull down	Connect 22ohm resistor in series	MAC receiving error, this pin is usually used by 100MPHY
RGMII_RXDV	pull down	Connect 22ohm resistor in series	RMII RX data validity and carrier detection signal, some 100M phy CRS_DV function pin is connected to RXDV pin (see pin definition of PHY for details).
RGMII_RXCLK	pull down	Connect 22ohm resistor in series	GMAC receive clock
RGMII_RXD0~D3	pull down	Connect 22ohm resistor in series	GMAC receive data
RGMII_TXD0~D3	pull down	Connect 22ohm resistor in series	GMAC send data
RGMII_TXEN	pull down	Connect 22ohm resistor in series	GMAC TX data valid signal
RGMII_TXCLK	pull down	Connect 22ohm	GMAC send clock

		resistor in series	
--	--	--------------------	--

Note:

Please refer to the reference schematic for the circuit design of the Ethernet PHY.

- Place RX_DATA、RX_DV、RX_CLK series resistor close to the master
- Place TX_DATA、TX_EN、TX_CLK series resistance close to PHY

2.3.4 VI Interface

2.3.4.1 MIPI-CSI/LVDS/Sub-LVDS Interface

The RV11XX has two MIPI-CSI/LVDS/Sub-LVDS inputs and a built-in ISP processor. The MIPI-CSI/LVDS/Sub-LVDS are multiplexed pins. The three functions of MIPI-CSI/LVDS/Sub-LVDS cannot be used at the same time, only one of them can be used at a time.

The differential interface inputs one differential clock signals and 4 differential data signals, supporting 2lane MIPI RX and 4lane MIPI RX inputs

- When it is 4Lane MIPI RX, MIPI_RX_CLKP/N samples MIPI_RX_D0P/N, MIPI_RX_D1P/N, MIPI_RX_D2P/N, MIPI_RX_D3P/N;
- When it is 2In the MIPI RX, MIPI_RX_CLKP/N samples MIPI_RX_D0P/N and MIPI_RX_D1P/N;
- To improve MIPI-CSI performance, please place the decoupling capacitors of the controller power supply close to the pins.
- PinW21 MIPI_CSI_CLK1 and Pin V21 MIPI_CSI_CLK0 can provide clock signal for MIPI/LVDS camera.



Figure 2-38 RV11XX MIPI-CSI/LVDS/sub-LVDS module

2.3.4.2 Parallel Interface Input

There is one VICAP controllers in RV11XX. The VIACAP function pins are named CIF_D0~D15, CIF_HSYNC, CIF_VSYNC, CIF_CLKOUT, CIF_CLKIN.

If the VICAP pins are reused in two power domains: VCCIO6 and VCCIO5 power domains, only one group can be used at a time. In the actual product design, the corresponding power supply should be selected according to the actual IO power supply requirement of the product Camera (1.8V or 3.3V), and must be consistent with I2C pull-up level, otherwise it will cause camera to work abnormally or not work. For multiplexed pins, please refer to the released "RV1126_RV1109_PINOUT".

The parallel VICAP controller interface supports RAWData, BT1120, BT656, BT601 format data, and the interface

rate can reach 148.5MHz.

- When the connected signal is RAWdata, the connection should be aligned from the high bit of VICAP. For example, 12bit RawData corresponds to CIF_D15~D4 from the high bit.
- When the connected signal is BT1120, 8bit data is connected to Y, 8bit data is connected to UV, and only supporting internal synchronization.
- When the connected signal is BT656 or BT601, the high bits of VICAP are connected in order.
- CIF_CLKOUT outputs clock signal to peripherals.
- CIF_CLKIN accepts the clock signal input from peripherals.

The correspondence between CIF interface BT1120 and 12bit/10bit/8bit:

Correspondence CIF data and BT1120/12bit/10bit/8bit CIF				
16bit CIF data	BT1120	12bit CIF camera	10bit CIF camera	8bit CIF camera
CIF_D0	BT1120_D0			
CIF_D1	BT1120_D1			
CIF_D2	BT1120_D2			
CIF_D3	BT1120_D3			
CIF_D4	BT1120_D4	D0		
CIF_D5	BT1120_D5	D1		
CIF_D6	BT1120_D6	D2	D0	
CIF_D7	BT1120_D7	D3	D1	
CIF_D8	BT1120_D8	D4	D2	D0
CIF_D9	BT1120_D9	D5	D3	D1
CIF_D10	BT1120_D10	D6	D4	D2
CIF_D11	BT1120_D11	D7	D5	D3
CIF_D12	BT1120_D12	D8	D6	D4
CIF_D13	BT1120_D13	D9	D7	D5
CIF_D14	BT1120_D14	D10	D8	D6
CIF_D15	BT1120_D15	D11	D9	D7

Figure 2-39 RV11XX CIF interface

2.3.5 VO Interface

RV11XX chipset has a built-in video controller and supports RGB/BT1120/MIPI DSI four video output modes, with the resolution of 1080P@60fps. And the RGB/BT1120 signal is in the VCCIO5_VDD power domain

2.3.5.1 MIPI-DSI

MIPI-DSI controller, a 4 lane MIPI-DSI interface, with the rate of 1Gbps per lane.

Pay attention to the following items in the design:

- Please place the decoupling capacitors of the controller power supply close to the pins for MIPI-DSI performance
- Please refer to differential clocks for the four differential data samples.
- For detailed schematic design, please refer to the released schematic.

Table 2-16 RV11XX MIPIDSI interface design

Signal	Connection mode	Remark
MIPI_DSI_TX0_CLKP	direct connection	MIPI DSI CLKP
MIPI_DSI_TX0_CLKN	direct connection	MIPI DSI CLKN
MIPI_DSI_TX0_D0P	direct connection	MIPI DSI data0P
MIPI_DSI_TX0_D0N	direct connection	MIPI DSI data0N
MIPI_DSI_TX0_D1P	direct connection	MIPI DSI data1P
MIPI_DSI_TX0_D1N	direct connection	MIPI DSI data1N
MIPI_DSI_TX0_D2P	direct connection	MIPI DSI data2P
MIPI_DSI_TX0_D2N	direct connection	MIPI DSI data2N
MIPI_DSI_TX0_D3P	direct connection	MIPI DSI data3P
MIPI_DSI_TX0_D3N	direct connection	MIPI DSI data3N

2.3.5.2 Parallel VO Interface Design

Parallel VO (video output) interface of RV11XX supports BT1120 and RGB output.

The RGB output is used to connect LCD screen and supports 6/8bit serial RGB and 16bit, 18bit, 24bit parallel RGB.

Table 2-17 Signal interface mode and corresponding pins

Signal interface mode	Corresponding pins
-----------------------	--------------------

BT1120TX	DATA: LCDC_DATA[15:0] Y[0:7]:LCDC_DATA[8:15] Cb[0:7]:LCDC_DATA[0:7] CLOCK:LCDC_CLK
6bit Serial RGB	DATA: LCDC_DATA[5:0] CLOCK:LCDC_CLK Hsync:LCDC_HSYNC Vsync:LCDC_VSYNC DE:LCDC_DEN
8bit Serial RGB	DATA: LCDC_DATA[7:0] CLOCK:LCDC_CLK Hsync:LCDC_HSYNC Vsync:LCDC_VSYNC DE:LCDC_DEN
16bit Parallel RGB(RGB565)	R[4:0]: LCDC_DATA[15:11] G[5:0]: LCDC_DATA[10:5] B[4:0]: LCDC_DATA[4:0] CLOCK:LCDC_CLK Hsync:LCDC_HSYNC Vsync:LCDC_VSYNC DE:LCDC_DEN
18bit Parallel RGB(RGB666)	R[5:0]: LCDC_DATA[17:12] G[5:0]: LCDC_DATA[11:6] B[5:0]: LCDC_DATA[5:0] CLOCK:LCDC_CLK Hsync:LCDC_HSYNC Vsync:LCDC_VSYNC DE:LCDC_DEN
24bit Parallel RGB(RGB888)	R[7:0]: LCDC_DATA[23:16] G[7:0]: LCDC_DATA[15:8] B[7:0]: LCDC_DATA[7:0] CLOCK:LCDC_CLK Hsync:LCDC_HSYNC Vsync:LCDC_VSYNC DE:LCDC_DEN

Table 2-18 Design requirements for parallel VO signals

Signal	Designing
BT1120_CLK	Connect a 22R resistor in series with RV11XX
BT1120_DATA	direct connection
LCDC_CLK	Connect a 22R resistor in series with RV11XX
LCDC_DATA	direct connection

2.3.6 SPI Interface

2.3.6.1 SPI Controller Introduction

There are two SPI controllers in RV11XX chipset: SPI0 (2CS) and SPI1 (2CS).

Both SPI0 and SPI1 support master and slave modes. SPI0 and SPI1 have three groups of multiplexed relationship respectively. The remark with "_M0/1/2" suffix in the schematic is the multiplexing number of the corresponding function. Note that due to the limitation of the controller, this kind of multiplexing function can only be used by one group from the multiplexing relationship. You have to allocate resources well on applications. Please refer to the released "RV1126_RV1109_PINOUT" document for prophase design.

Table 2-19 SPI Multiplex interface

Signal	Corresponding power domain	Signal	Corresponding power domain

SPI0_M0	PMUIO0_VDD	SPI1_M0	VCCIO6_VDD
SPI0_M1	VCCIO4_VDD	SPI1_M1	VCCIO2_VDD
SPI0_M2	VCCIO5_VDD	SPI1_M2	VCCIO5_VDD

2.3.6.2 SPI Topology and Connection Mode

SPI interface pull-up and down and matching design recommendations are shown in the table below

Table 2–20 RV11XX SPI interface design

Signal	Connection method	Description(chipset)
SPI_MOSI	direct connection	SPI data output
SPI_MISO	direct connection	SPI data input
SPI_CLK	Connect a 22ohm resistor in series	SPI clock signal
SPI_CS0	direct connection	SPI Chip select signal 0
SPI_CS1	direct connection	SPI Chip select signal 1

2.3.7 USB

There are two USB 2.0 interfaces in RV11XX chipset, OTG_DM/DP supports OTG mode, HOST_DM/DP only supports HOST mode.

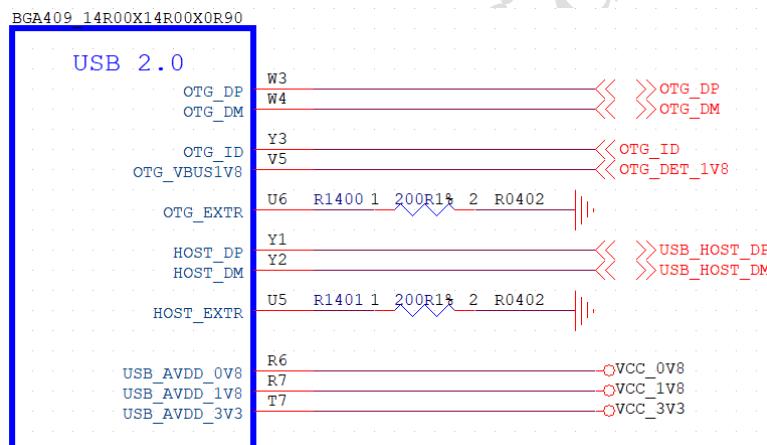


Figure 2-40 RV11XX USB module

Pay attention to the following items in the design:

- The USB OTG interface is the system firmware flashing port by default, which should be reserved during the debugging process;
- USB_ID is internally pulled up to USB_AVDD_1V8, so OTG is Device mode by default;
- OTG_VBUS1V8 uses an 18K resistor and a 10K resistor to divide VCC5V0_USB for input detection. The detection voltage is from 1.62V to 2.08V, and when high level is detected indicates that an USB is inserted.
- Please select a 200ohm resistor with 1% accuracy for the reference resistance of USB controller. Please do not change the resistor, because it is related to USB amplitude and the quality of the eye diagram.

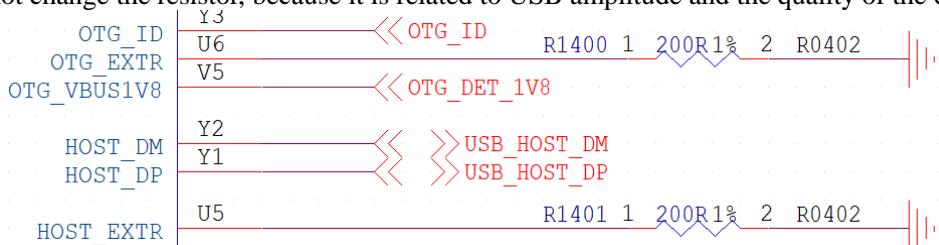


Figure 2-41 RV11XX USB controller reference resistor

- To improve the USB performance, please place decoupling capacitors of the controller power supply close to the pins;

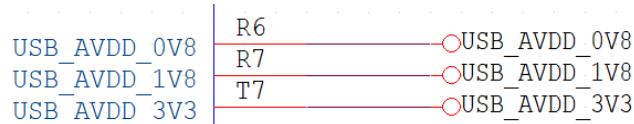


Figure 2-42 RV11XX USB controller power supply

- To control electromagnetic radiation, setting a common mode choke on the signal line can take in consideration. During debugging and testing process, choose a 2.2R resistor or a common mode choke according to the actual situation.

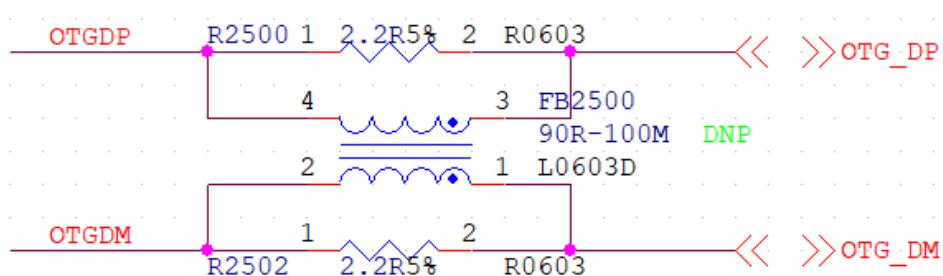


Figure 2-43 RV11XX USB reserved the common mode choke

- In order to improve usb compatible, please add this circuit. And please note that USB_CTRL must connecte to GPIO0_C1 (SOC pinAA4).

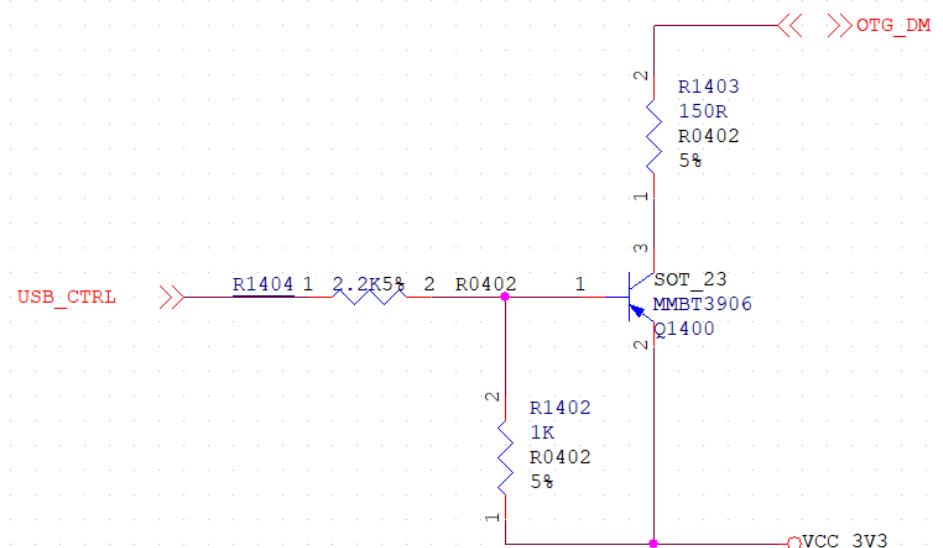


Figure 2-44 RV11XX usb compatible improving

- There must be ESD protection measures on the USB2.0 signal. The parasitic capacitance of the ESD device should be less than 1pF. The ESD device should be placed close to the USB.
- The pull-up and down and matching design recommendations for USB2.0 interface are shown in the table below.

Table 2-21 RV11XX USB2.0 interface design

Signal	Connection mode	Description
OTG_DP/DM	Connect a 2.2ohm resistor in series	USB OTG input/output
OTG_ID	direct connection (Internal 1.8V pull-up)	USB OTG ID recognition, used when it is Micro-B interface
OTG_VBUS1V8	Resistance voltage division detection	USB OTG insertion detection
OTG_EXTR	200ohm resistor grounded	USB PHY configuration reference resistance, 200ohm grounded
HOST_DP/DM	Connect a 2.2ohm resistor in series	USB HOST input/output
HOST_EXTR	200ohm resistor grounded	USB PHY configuration reference resistance, 200ohm grounded

2.3.8 SARADC

RV11XX chip takes ADC_IN0 of SARADC as key input sampling interface. Under the condition that the system has already flashed the firmware, if ADC_IN0 is kept low (0V) during system start, RV11XX enters the Rockusb flashing mode, you can update the firmware via a PC in this state.

In RV11XX, SARADC sampling ranges from 0 to 1.8V, with 10 bits sampling accuracy. The key array is in parallel, and the input key value can be adjusted by increasing or decreasing the keys and adjusting the ratio of the voltage-dividing resistance, so as to realize multi-key input to meet customer product requirements. In the design, it is recommended that the sampling value of any two keys must be greater than +/-35, that is, the center voltage difference must be greater than 123mV.

Pay attention to the following items in the design:

- Place the decoupling capacitors of the controller power supply close to the pins;
- The ADC is an analog signal, which must be properly routed. The distance from other signals should follow the 3W principle.
- When the SARADC is connected with a key, ESD protection and anti-shake function are needed.

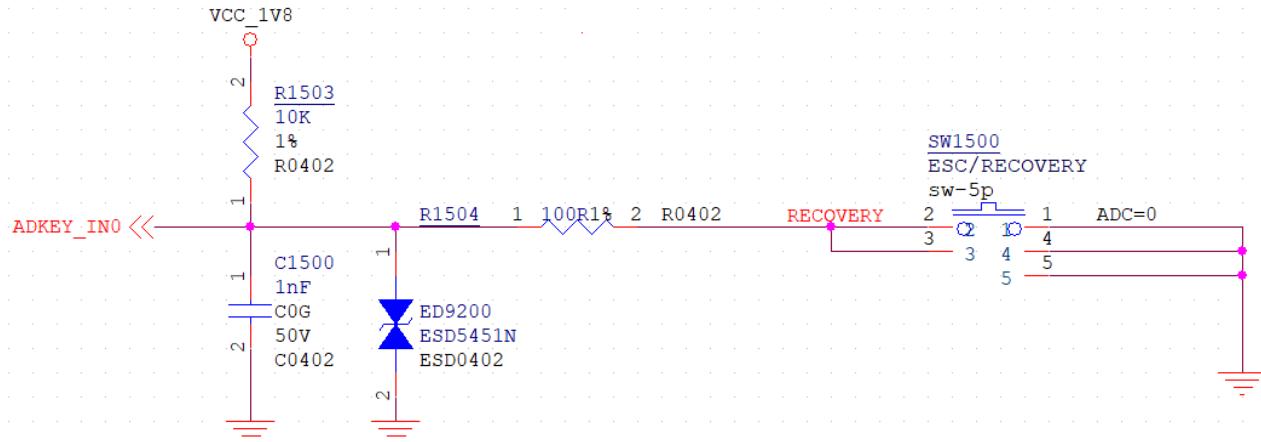


Figure 2-45 SARADC_KEY

2.3.9 UART and Debug

The RV11XX integrates 6 UART interfaces, similar to other interfaces, and considering the diversity of products, the UART controller has also been multiplexed. The mark with "_M0/1/2" Suffix in the schematic is the multiplexed number of the corresponding function, it is better to allocate resources in the design.

The UART controller supports the following functions:

- Support 6 independent UART controllers: UART0-UART5 are all including two 64-byte FIFOs for data reception and transmission;
- In addition to support 115.2Kbps, 460.8Kbps, 921.6Kbps, 1.5Mbps, 3Mbps, 4Mbps, support automatic flow control.
- Supports programmable baud rate, even with non-integer clock dividers, standard asynchronous communication bits (start, stop, and parity check).
- Supports interrupt-based or DMA-based modes
- Support 5-8 bits width transmission

Introduction to UART0~UART5:

- UART0 in the reference design is used to connect to BT, belonging to VCCIO3 power domain, and the IO level should be consistent with the level of the BT module.
- UART1 is multiplexed in two different power domains, UART1_M0 is in the PMUIO1 power domain, and UART1_M1 is in the VCCIO3 power domain. Only one application can be selected during design.
- UART2 is reused in two different power domains, UART2_M0 is in the VCCIO2 power domain, and UART2_M1 is in the VCCIO5 power domain. Only one application can be selected in the design. The figure below shows the location of the UART2_M1 interface. The default function is debugging interface. Please try to keep it consistent with our design. It can be connected an UART to USB transfer board for debugging in the product. Please refer to the document "RV1126_RV1109_PINOUT" for the location of UART2_M0. When debugging, please select the port number according to actual connection. The default baud rate of the debug log output is 1.5M. Do not check the flow control RTS/CTS. In product design, it is recommended to use UART to USB chip for transfer, and FT232RL is recommended.

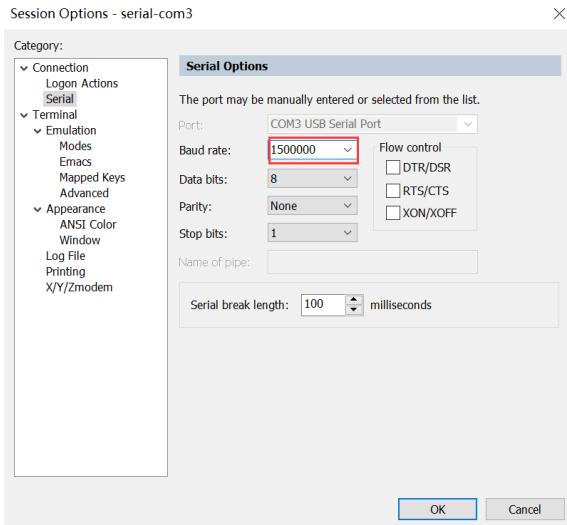


Figure 2-46 RV11XX Serial port configuration

- UART3 is reused in 3 different power domains, UART3_M0 is reused with VCCIO6 power domain, UART3_M1 is reused with VCCIO2 power domain, UART3_M2 is reused with VCCIO5 power domain, choose one of them according to the actual application.
- UART4 is reused in 3 different power domains, UART4_M0 is reused with VCCIO6 power domain, UART4_M1 is reused with VCCIO5 power domain, UART4_M2 is reused with VCCIO4 power domain, choose one of them according to the actual application.
- UART5 is reused in 3 different power domains, UART5_M0 is reused with VCCIO6 power domain, UART5_M1 is reused with VCCIO5 power domain, UART5_M2 is reused with VCCIO4 power domain, choose one of them according to the actual application.

Table 2-22 UART multiplexed table

Signal	Corresponding power domain	Signal	Corresponding power domain
UART0	VCCIO3_VDD	UART3_M2	VCCIO5_VDD
UART1_M0	PMUIO1_VDD	UART4_M0	VCCIO6_VDD
UART1_M1	VCCIO3_VDD	UART4_M1	VCCIO5_VDD
UART2_M0	VCCIO2_VDD	UART4_M2	VCCIO4_VDD
UART2_M1	VCCIO5_VDD	UART5_M0	VCCIO6_VDD
UART3_M0	VCCIO6_VDD	UART5_M1	VCCIO5_VDD
UART3_M1	VCCIO2_VDD	UART5_M2	VCCIO4_VDD

Table 2-23 RV11XX UART pull up and down and matching design

Signal	Connection mode	Description(chipset)
UART_RX	direct connection	UART data input
UART_TX	direct connection	UART data output
UART_CTSn	direct connection	UART allows to send signals
UART_RTSn	direct connection	UART request to send signal

2.3.10 I2C

Inter-Integrated Circuit (I2C) is a two-line (SCL and SDA) bidirectional serial bus that provides an efficient and simple way for information exchange between devices. The I2C bus controller supports the master-slave mode as a bridge between AMBA protocol and general I2C bus system.

I2C controller supports the following functions

- Support 5 independent I2C: I2C0/1/3/4/5
- Support I2C bus master mode
- Software programmable clock frequency and transmission rate up to 400Kbit/sec
- Support 7-bit and 10-bit addressing mode

I2C is also multiplexing. The mark with the "_M0/1/2" suffix in the schematic is the multiplexing number of the corresponding function.

Introduction to I2C0~I2C5:

- I2C0 belongs to PMUIO1 power domain. In the reference design, I2C0 is used to connect to PMIC by default.
- I2C1 belongs to the VCCIO4 power domain, which is used to connect to camera by default in the reference design.
- The I2C3 pins are reused in 3 power domains: I2C3_M0 belongs to the VCCIO6 power domain, I2C3_M1 belongs to the VCCIO5 power domain, and I2C3_M2 belongs to the VCCIO4 power domain, and choose one of them according to the actual application situation.
- The I2C4 pins are reused in two power domains. I2C4_M0 belongs to the VCCIO5 power domain, and I2C4_M1 belongs to the VCCIO7 power domain. Choose one group according to the actual applications.
- The I2C5 pins are reused in three power domains: I2C5_M0 belongs to the VCCIO5 power domain, I2C5_M1 belongs to the VCCIO6 power domain, and I2C5_M2 belongs to the VCCIO7 power domain. Choose one of them according to the actual applications.

Table 2-24 I2C multiplexed table

Signal	Corresponding power domain	Signal	Corresponding power domain
I2C0	PMUIO1_VDD	I2C4_M0	VCCIO5_VDD
I2C1	VCCIO4_VDD	I2C4_M1	VCCIO7_VDD
I2C2	PMUIO1_VDD	I2C5_M0	VCCIO5_VDD
I2C3_M0	VCCIO6_VDD	I2C5_M1	VCCIO6_VDD
I2C3_M1	VCCIO5_VDD	I2C5_M2	VCCIO7_VDD
I2C3_M3	VCCIO4_VDD		

2.3.11 PWM

Pulse width Modulation (PWM) technology is widely used in product design, and is often used in applications such as controlling servo motors or digital-to-analog conversion. RV11XX integrates 3 PWM controllers, each controller has 4 channels, so there are 12 PWM channels available.

The pulse width modulation module supports the following features:

- Support capture mode.
- Support continuous mode or single sending mode.
- Support second-level frequency division.
- Available low-power modes, reduce power consumption when the channel is inactive.

PWM3, PWM7, PWM11 can be used for infrared receiving and decoding applications, and a special hardware decoder is integrated inside the chip with higher efficiency.

The pins of PWM0~PWM11 have two groups of multiplexing relationships, which are reused in different power domains. For example, PWM0_M0 and PWM0_M1 actually belong to the same PWM, but are multiplexed on different pins, so only one of them can be selected at a time. PWM0~PWM11 are independent and do not affect each other.

For the location of PWM_M0/PWM_M1, please refer to the document "RV1126_RV1109_PINOUT".

2.3.12 CAN Bus

CAN (Controller Area Network) bus is a widely used field bus, which allows microcontrollers and devices to communicate with each other in applications without a host. CAN bus has great application prospects in the fields of industrial measurement and control and industrial automation, especially the measurement and control communication applications in the automobile.

The CAN interface of RV11XX is multiplexed in two different power domains, please choose one of them according to the actual application, as shown in the following figure.

Table 2-25 RV11XX CAN Bus interface design

Signal	Connection method	Description(chipset)
CAN_RXD	direct connection	CAN Bus data input
CAN_TXD	direct connection	CAN Bus data output

2.3.13 Audio Circuit

RV11XX provides three groups of standard I2S interfaces, they all support master or slave mode, with the highest sampling rate to 192kHz and the bit rate from 16bits to 32bits. RV11XX also supports a group of PDM digital audio interfaces which support up to 8 channels of PDM format audio input and the highest sampling rate to 192kHz, the bit rate from 16bits to 32bits.

2.3.13.1 I2S0/TDM/PCM

The I2S0 controller contains three functions: I2S/PCM/TDM function, all of them will be called I2S0 below. The I2S0 interface contains independent 8-channel output and 8-channel input. In order to meet the different sampling rate requirements of playback and recording, the bit clock and frame clock provide two groups accordingly(SCLKTX|LRCKTX, SCLKRX|LRCKRX); Note that, For the case where SDOx and SDIx only refer to one group of bit/frame clocks, SCLKTX|LRCKTX is preferentially used as their common clock.

I2S0 interface supports master-slave working mode, and is configurable in software; supports 3 I2S formats (regular, left-aligned, right-aligned); supports 4 PCM formats (early, late1, late2, late3); I2S and PCM, TDM mode cannot be used at the same time.

It should be noted that the I2S0 pins are reused in two different power domains. The mark with the "_M0/1/2" suffix in the schematic is the multiplex number of the corresponding function. I2S0_M0 belongs to the VCCIO7 power domain, and the default setting is VCC_1V8. I2S0_M1 belongs to the VCCIO6 power domain, and the default voltage is also VCC_1V8. I2S0_M0 and I2S0_M1 cannot be used at the same time, in other words, only one of them can be used at a time. If the I2S peripheral IO level is 3.3V, the power supply of the corresponding power domain needs to be adjusted to match the level of the related IO.

I2S0 interface pull-up and down and matching design recommendations, and the relationship between I2S0, PCM, TDM are shown in the following table.

Table 2–26 RV11XX I2S0 interface design

Signal	Internal pull up/down	Connection mode	Description(chipset)
I2S0_MCLK	pull down	Connect a 22ohm resistor in series	I2S0 system clock output
I2S0_SCLK_TX (PCM_CLK) (TDM_CLK)	pull down	Connect a 22ohm resistor in series	I2S0 continuous serial clock (TX, associated with SDOx)
I2S0_LRCK_TX (PCM_SYNC) (TDM_FSYNC)	pull down	Connect a 22ohm resistor in series	I2S0 frame clock for channel selection (TX, associated SDOx)
I2S0_SDO0 (PCM_OUT) (TDM_SDO0)	pull down	Connect a 22ohm resistor in series	I2S0 serial data 0 output
I2S0_SDO1_SD13	pull down	Connect a 22ohm resistor in series	I2S0 serial data 1 output, or serial data input 3
I2S0_SDO2_SD12	pull down	Connect a 22ohm resistor in series	I2S0 serial data 2 output, or serial data input 2
I2S0_SDO3_SD11	pull down	Connect a 22ohm resistor in series	I2S0 serial data 3 output, or serial data input 1
I2S0_SCLK_RX	pull down	22ohm resistor in series	I2S0 continuous serial clock (RX, associated SDIx)
I2S0_LRCK_RX	pull down	Connect a 22ohm resistor in series	I2S0 frame clock for channel selection (RX, associated SDIx)
I2S0_SD10 (PCM_IN) (TDM_IN)	pull down	Connect a 22ohm resistor in series	I2S0 serial data 0 input

2.3.13.2 I2S1/I2S2

The I2S1/I2S2 controller includes I2S and PCM functions.

I2S2 supports 2-channel output and 2-channel input. In the reference design, is connected to the PCM interface of the BT module by default, and it is used as the communication port of the Bluetooth call function under the HFP protocol.

I2S1/2 supports 2 channels input and 2 channels output; supports master-slave working mode, and is software configurable; supports 3 I2S formats (regular, left aligned, right aligned); supports 4 PCM formats (early, late1, late2, late3); I2S and PCM, TDM mode cannot be used at the same time.

The I2S1 pins are reused in three different power domains. The mark with the "_M0/1/2" suffix in the schematic is the multiplexed number of the corresponding function. I2S1_M0 belongs to the VCCIO1 power domain, I2S1_M1 belongs to the VCCIO4 power domain, and I2S1_M2 belongs to the VCCIO5 power domain, and choose one of them according to the actual application.

The I2S2 pins are reused in two different power domains. The mark with the "_M0/1" suffix in the schematic is the multiplexed number of the corresponding function. I2S2_M0 belongs to the VCCIO3 power domain, and I2S2_M1 belongs to the VCCIO5 power domain. Choose one of them according to the actual application.

Please refer to the "RV1126_RV1109_PINOUT" document for the detailed location.

Table 2-27 RV11XX I2S1/2 interface design

Signal	Internal pull down	Connection method	Description(chipset)
I2S1/2_MCLK	pull down	Connect a 22ohm resistor in series	I2S1 system clock output
I2S1/2_SCLK (PCM_CLK)	pull down	Connect a 22ohm resistor in series	I2S1 continuous serial clock
I2S1/2_LRCK (PCM_SYNC)	pull down	Connect a 22ohm resistor in series	I2S1 frame clock for channel selection clock
I2S1/2_SDO (PCM_OUT)	pull down	Connect a 22ohm resistor in series	I2S1 serial data 0 output
I2S1/2_SDI (PCM_IN)	pull down	Connect a 22ohm resistor in series	I2S1 serial data 0 input

2.3.13.3 PDM Interface

RV11XX provides one PDM digital audio interfaces, supports up to 8 channels of PDM format audio input, the highest sampling rate is 192kHz, the bit rate is from 16bits to 32bits, supports PDM master receiving mode.

The PDM pins are reused in two different power domains. The symbol with the "_M0/1" suffix in the schematic is the multiplexed number of the corresponding function. PDM_M0 belongs to the VCCIO7 power domain, and PDM_M1 belongs to the VCCIO6 power domain. Choose one of them according to the actual application.

When taking PDM MIC as audio collection, in order to simplify the processing of recording audio data by software, it is recommended to use PDM interface for recovery. In this way, for the common applications case of 2-6 PDM MIC recordings and 1-2 recovery channels, only the whole 4-8 channel recording audio will complete input, without additional splicing processing in the software.

If you need to connect one 8-channel PDM MIC input, only I2S interface can be used as sampling for recovery channel. The software needs to do additional audio splicing process to meet the algorithm's data synchronization requirements.

Table 2-28 RV11XX PDM interface design

Signal	Internal pull up/down	Connection method	Description(chipset)
PDM_CLK0	pull down	Connect a 22ohm resistor in series	PDM clock 0
PDM_CLK1	pull down	Connect a 22ohm resistor in series	PDM clock 1 , the same origin as PDM clock 0
PDM_SDI0	pull down	Connect a 22ohm resistor in series	PDM data 0 input
PDM_SDI1	pull down	Connect a 22ohm resistor in series	PDM data 1 input
PDM_SDI2	pull down	Connect a 22ohm resistor in series	PDM data 2 input
PDM_SDI3	pull down	Connect a 22ohm resistor in series	PDM data 3 input

2.3.13.4 Audio PWM Interface

RV11XX has built-in Audio PWM function, supports converting PCM format to PWM format, supports 2x/4x/8x/16x oversampling linear interpolation, supports 8/9/10/11 bit maskable L/R channel PWM output. It is

suitable for applications such as prompt sounds with low sound quality requirements, and applications with higher requirements and no high-performance audio DAC are recommended to use Audio DSM.

AUDPWM has two group of reused pins. The mark with the "_M0/1" suffix in the schematic is the multiplexed number of the corresponding function. The power domains of AUDPWM_M0 and AUDPWM_M1 are both VCCIO7, and chose one of them according to the actual applications.

2.3.13.5 Audio DSM Interface

RV11XX has built-in Audio DSM function, which supports to change direct stream digital encoding of PCM data into a 1-bit signal stream, providing oversampling of more than 128x, and upsampling interpolation of 16x/32x/64x. In a design without a high-performance audio DAC but requires audio output, audio signal will output by AUDDSM going through a first-order RC low-pass filtering, and the audio quality can be optimized to the maximum when using a differential output.

Design the external first-order RC low-pass filter and parameters selection:

- 1) The circuit is as follows:

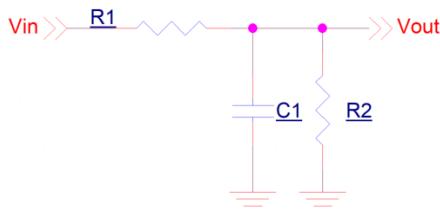


Figure 2-47 RV11XX Audio filter circuit

- 2) Vin is output from Audio DSM, with the maximum peak-to-peak value close to the power supply voltage of VCCIO7. This amplitude may exceed the input range of some audio amplifiers, resulting in serious distortion. After adding R2 in the circuit to divide the voltage, it is convenient for Vout to match the input range of the power amplifier to avoid distortion
- 3) Parameters selection:

R1 connecting to AUDSM output in series is selected in the range of 1Kohm~10Kohm, the accuracy of R1 and R2 is 1%, and the low-pass cut-off frequency of the filters:

$$f_{(-3dB)} = \frac{R_1 + R_2}{2\pi R_1 R_2 C_1} \dots \text{formula (1)}$$

Change to:

$$C_1 = \frac{R_1 + R_2}{2\pi R_1 R_2 f_{(-3dB)}} \dots \text{formula (2)}$$

According to VCCIO7 and the input range of the audio power amplifier to get the voltage division ratio of R1 and R2, supposing that the ratio of the voltage of VCCIO7 to the input voltage of the power amplifier is n, then:

$$R_2 = \frac{R_1}{n-1} \dots \text{formula (3)}$$

After taking formula (3) into formula (2), you will get

$$C_1 = \frac{n}{2\pi R_1 f_{(-3dB)}} \dots \text{formula (4)}$$

For example, if the power supply voltage of VCCIO7 is 3.3V and the input amplitude of the audio power amplifier is 0.5 Vpp, then n=6.6 can be obtained. It is generally recommended that $f_{(-3dB)}$ is in the range of 22KHz~40KHz, if $f_{(-3dB)} = 33\text{KHz}$ here, take R1=5.6 Kohm, calculated by formula (3) and formula (4):

$$R_2 = \frac{R_1}{n-1} = \frac{5.6}{6.6-1} = 1(\text{Kohm})$$

$$C_1 = \frac{n}{2\pi R_1 f_{(-3dB)}} = \frac{6.6}{2\pi \times 5.6 \times 33 \times 10^6} \approx 5.6(\text{nF})$$

Audio AUDDSM reference design is shown below:

Speaker

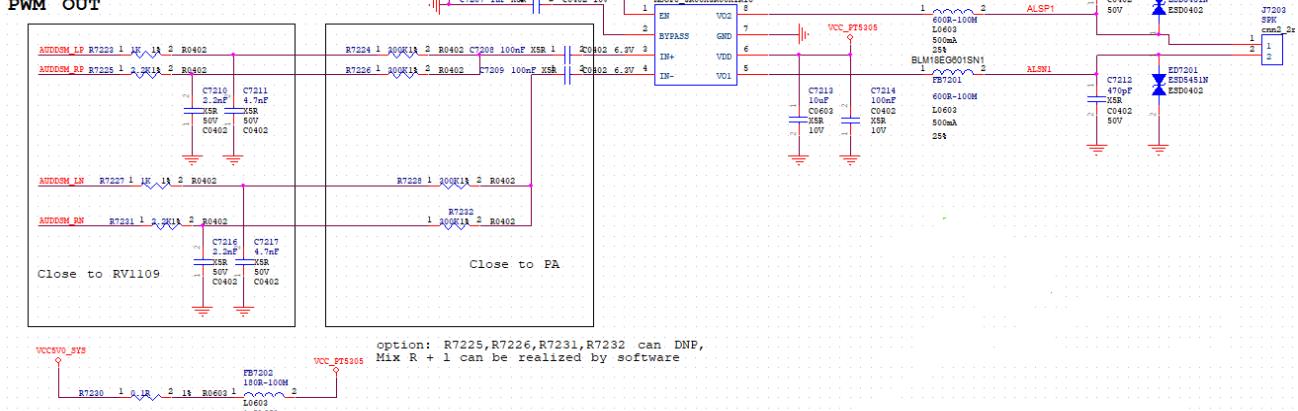


Figure 2-48 RV11XX Audio AUDDSM reference design

2.3.13.6 Codec Solution of RV11XX and RK809-2

RK809-2 chip integrates Codec and connects to RV11XX through I2S interface

PMIC RK809-2 CODEC

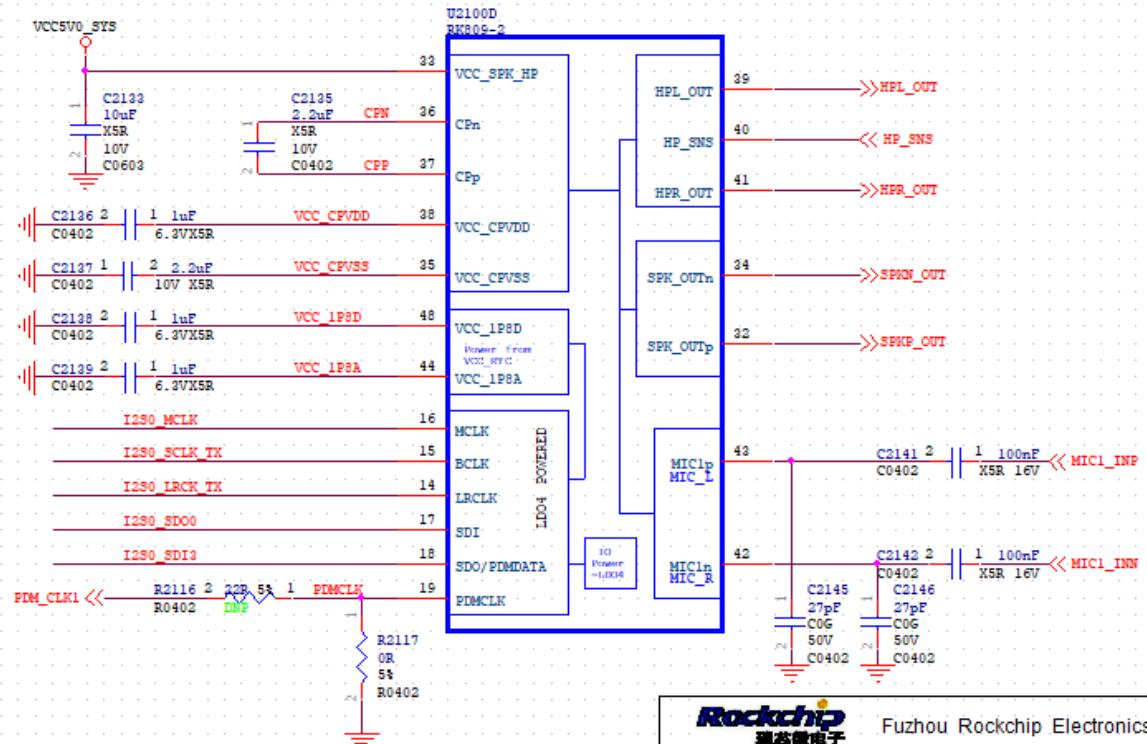


Figure 2-49 RK809-2 Codec circuit

RK809-2 HP_SNS is used for audio ground loop compensation. It is required to connect the GND to the earphone socket when wiring, to improve the isolation of the left and right channels. In addition, note that HPR/HPL is not a differential signal which should be grounded to avoid interference from other signals or mutual interference.

Codec built-in mono filter-free speaker drive circuit, which will provide 1.3W@8ohm driving capability, meet the low-power and mono applications, and save additional external power amplifier costs.

SPK

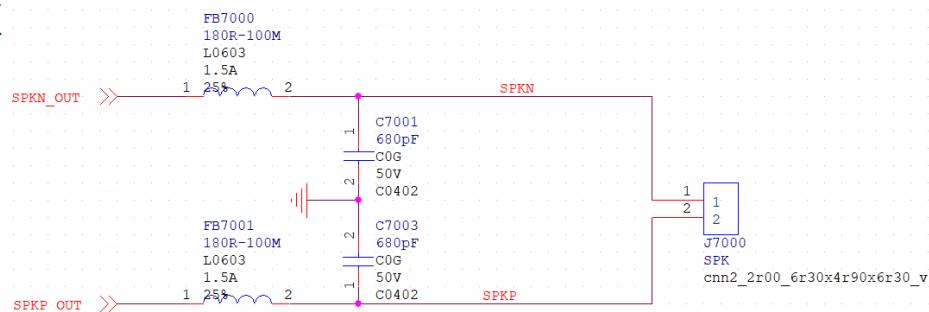


Figure 2-50 Speaker output circuit

RK809-2 integrates two MIC inputs, which can be configured as a differential MIC input or two single-ended MIC inputs. Which can be chose according to actual needs on product. Three solutions are provided in the reference design.

Solution 1: If the product does not have duplex calls or interrupt and wake-up requirements, a low-cost solution with differential MIC+ mono speakers can be used. As shown in the following figure, MIC is an analog small signal trace, and please pay attention to protection.

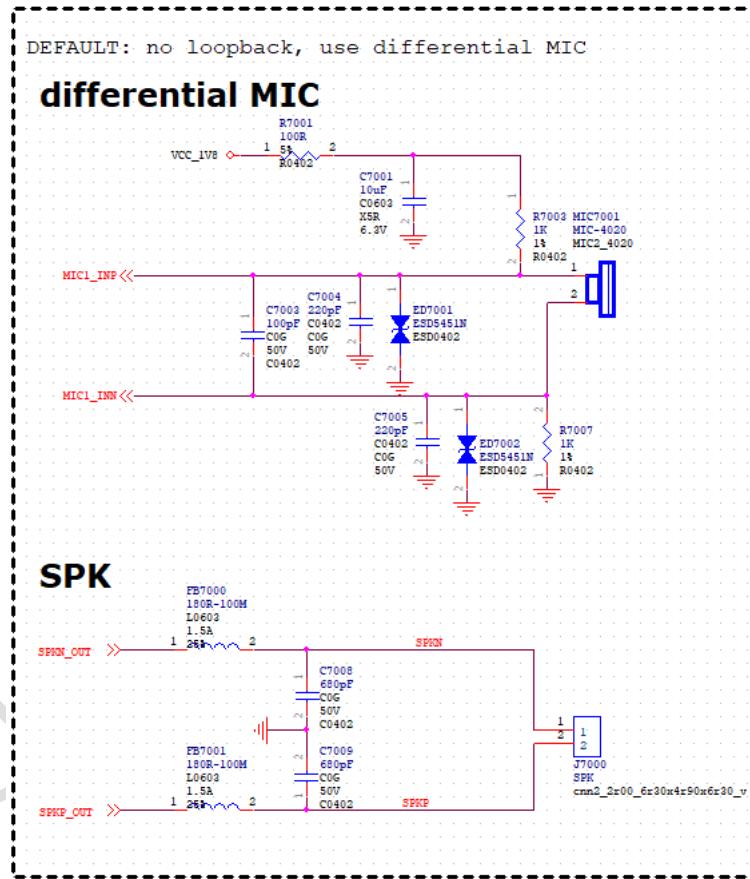


Figure 2-51 MIC solution 1

Solution 2: If the product has a call or interrupt and wake-up requirements, a recovery circuit needs to be added. A low-cost solution is recommended to use single-ended MIC + single-ended recovery. The solution is often used in IPC products, and the recovery function is frequently used for the processing of sidetone cancellation during calls. The single-ended MIC and the recovery traces are easily interfere. Please pay attention to surrounding by ground and avoid large current and interference areas on the board.

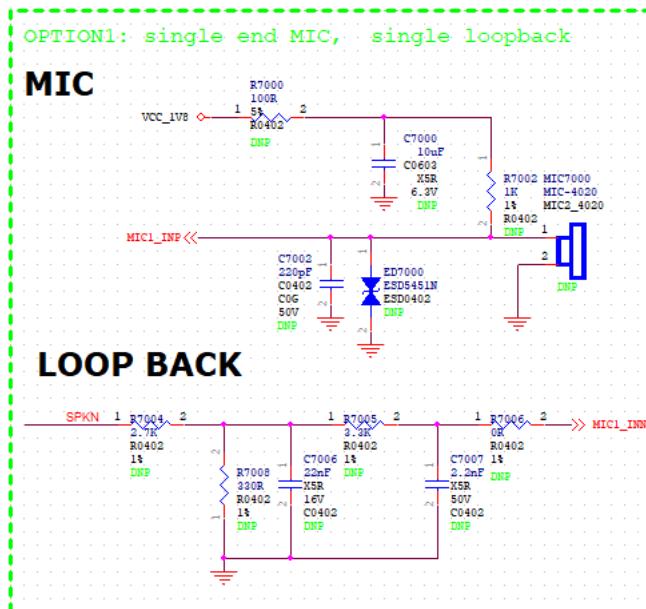


Figure 2-52 MIC solution 2

Solution 3: If the product has duplex calls or interrupt and wake-up requirement from a long distance, for high-end products, PDM MIC+ differential recovery solution are recommended. The number of PDM MIC is selected according to the actual needs of the algorithm and products, such as 2MIC, 4MIC, etc. If the output power of the speaker output part such as RK809 cannot meet the product requirement, and an analog or digital power amplifier can be added externally, it is not going to describe more details here.

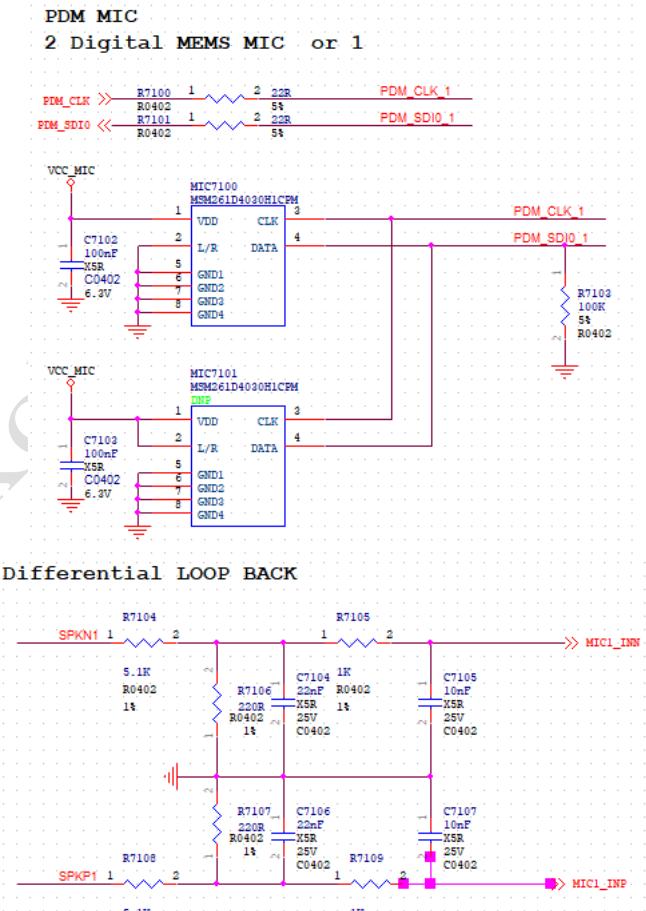


Figure 2-53 MIC solution 3

3 PCB Design

3.1 Power Supply and Filter Capacitors Design



Note

The power supplies below the controller includes the type, number and layout of filter capacitors for ARM, NPU, VEPU, LOGIC, PLL, MIPI, etc. Please follow the reference design.

- Filter capacitor group under the controller for ARM: 10uF+1uF+100nF*2
- Filter capacitor group under the controller for NPU: 10uF+1uF*2+100nF*3
- Filter capacitor group under the controller for VEPU: 10uF+1uF+100nF*2
- Filter capacitor group under the controller for LOGIC: 10uF+1uF*2+100nF*2
- Filter capacitor group under the controller for DDRIO: 10uF+1uF*3+100nF. Please keep the same as the reference design. The value and quantity of capacitors at other locations may be different.

For the location of the filter capacitors, please refer to the released "RV1126_RV1109_Template".

PLL power design:

PLL filter capacitors are placed near the ball position of the PLL power supply.

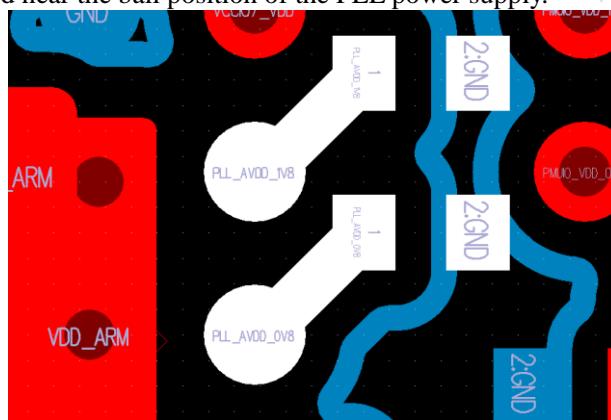


Figure 3-1 PLL Filter capacitors design

3.2 Crystal Oscillator PCB Design

The whole XIN and XOUT signal traces should be surround by ground and ensure that these signals have a complete reference ground, and no high-speed signals can pass under the crystal circuit. The crystal is placed near the controller.

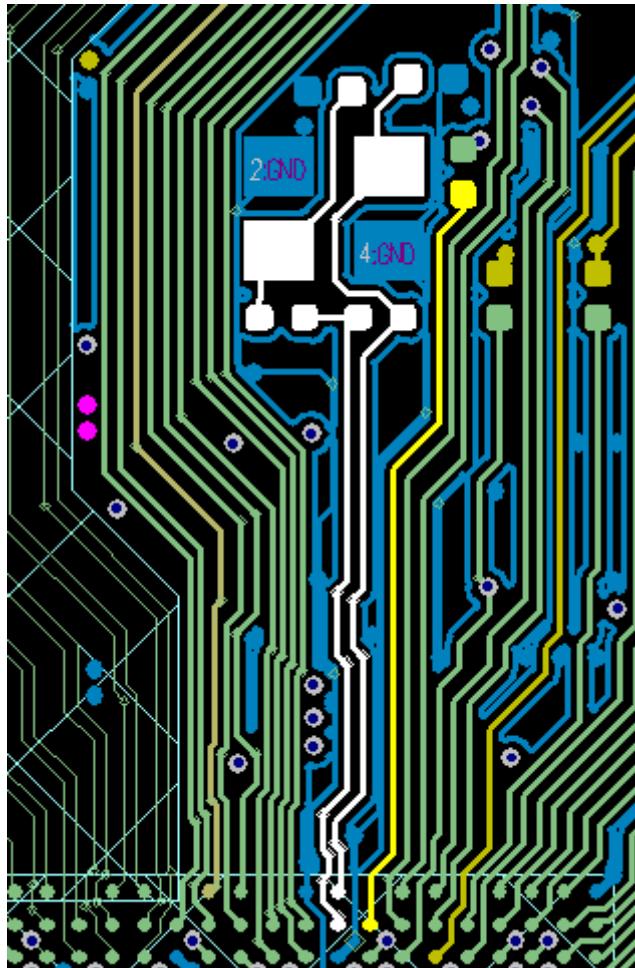


Figure 3-2 Crystal oscillator design

3.3 DDR PCB Design

DDR signal design requirements are as follows

Please refer to “RV1126_RV1109_Template”for details.

Table 3-1 [RV1126/RV1109](#)DDR3/DDR4/LPDDR4 Layout Requirements

Parameter	Requirement
single-ended impedance	50 Ohm $\pm 10\%$
Differential impedance	100 Ohm $\pm 10\%$
DQ to DQS matching (within a byte)	under 30mil
DM to DQS matching (within a byte)	under 30mil
(Command /Address) to CLK matching	under 60mil
DQS_P to DQS_N matching (within a byte)	under 12mil
CLK_P to CLK_N matching	under 12mil
DQS to CLK matching	under 900mil
Byte-to-byte spacing	≥ 2 times the width of the trace
DQ to DQ spacing within a byte	≥ 2 times the width of the trace
DQ to DQS spacing within a byte	Recommend ≥ 3 times the width of the trace At least 2 times the width of the trace
(Command /Address) to (Command /Address) spacing	≥ 2 times the width of the trace
CLK to all others spacing	Recommend ≥ 3 times the width of the trace At least 2 times the width of the trace

Table 3–2 LPDDR3 Layout Requirements

Parameter	Requirement
single-ended impedance	$50\Omega \pm 10\%$
Differential impedance	$100\Omega \pm 10\%$
DQ to DQS matching (within a byte)	under 30mil
DM to DQS matching (within a byte)	under 30mil
(Command /Address) to CLK matching	under 30mil
DQS_P to DQS_N matching (within a byte)	under 12mil
CLK_P to CLK_N matching	under 12mil
DQS to CLK matching	under 900mil
Byte-to-byte spacing	≥ 2 times the width of the trace
DQ to DQ spacing within a byte	≥ 2 times the width of the trace
DQ to DQS spacing within a byte	Recommend ≥ 3 times the width of the trace At least 2 times the width of the trace
(Command /Address) to (Command /Address) spacing	≥ 2 times the width of the trace
CLK to all others spacing	Recommend ≥ 3 times the width of the trace At least 2 times the width of the trace

3.4 FLASH/eMMC Circuit Design

FLASH signal design requirements are as follows:

- Avoid signal traces crossing the power supply division area, and keep the integrity of signal reference layer;
- The length of FSPI CS and data traces is based on the length of FSPI_CLK trace, and the error is controlled within 300mil.
- NAND FLASH signal traces should be controlled within 200 mils.
- Package + PCB signal length should not exceed 4inches.

Table 3–3 SFC Layout Requirements

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock matching	<300mil
Max trace length	<4 inches
The minimum spacing of SFC Signals	At least 2 times the width of SFC trace.

Table 3–4 NAND FLASH Layout Requirements

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock matching	<200mil
Max trace length	4 inches
The minimum spacing of NAND FLASH Signals	Recommend 2 times the width of FLASH trace.

The eMMC signal design requirements are as follows:

- Avoid signal traces crossing the power supply division area, and keep the integrity of signal reference layer;
- The length of eMMC_DATA and eMMC_CMD traces are based on the length of eMMC_CLK trace, and the error should be controlled within 120mil.
- The length of the package + PCB traces should not exceed 4 inches.

Table 3–5 eMMC Layout Requirements

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock matching	<120mil
Max trace length	<4 inches
The minimum spacing of eMMC Signals	At least 2 times the width of eMMC trace.

The minimum spacing between eMMC and other Signals	Recommend 3 times the width of eMMC trace. At least 2 times the width of eMMC trace.
--	---

3.5 SPI PCB Design

SPI signal design requirements are as follows:

- Avoid signal traces crossing the power supply division area, and keep the integrity of signal reference layer;
- The length of FSPI_CS and data traces is based on the length of FSPI_CLK trace, and the error is controlled within 300mil.

Table 3–6 SPI Layout Requirements

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock matching	<300mil
Max trace length	<6 inches

3.6 SDMMC0/SDIO PCB Design

SDMMC0/SDIO signal design requirements are as follows:

- The length of SDMMC0_DATA/SDIO_DATA and SDMMC0_CMD/SDIO_CMD traces are based on the length of SDMMC0_CLK/SDIO_CLK traces, and the error is controlled within 120mil.
- The signal takes GND as the reference layer and keeps the integrity of the reference layer.
- SDMMC0 is connected to TF card, and choose ESD devices with junction capacitances less than 1pF.
- The length of the package + PCB line should not exceed 4 inches.

Table 3–7 SDMMC/SDIO Layout Requirements

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock matching	<120mil
Max trace length	<4 inches
The minimum spacing of SDMMC Signals	At least 2 times the width of SDMMC trace.

3.7 RGMII Signal PCB Design

RGMII signal design requirements are as follows:

- Avoid signal traces crossing the power supply division area, and keep the integrity of signal reference layer;
- The length of RGMII_TXD and RGMII_TX_EN traces are based on the length of TX_CLK traces, and the error is controlled within 120mil;
- The length of RGMII_RXD and RGMII_RX_DV traces are based on the length of RX_CLK traces, and the error is controlled within 120mil;
- The length of MDI0+, MDI0-, MDI1+, MDI1-, MDI2+, MDI2-, MDI3+, MDI3-, differential pairs are controlled within 10mil, and differential impedance is controlled within $100\text{ohm} \pm 10\%$;
- The shorter the RGMII line, the better;
- Place RJ45 close to PHY;
- CLK signal should be surrounded by ground.
- The length of the package + PCB should not exceed 5 inches.

Table 3–8 RGMII Layout Requirements

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
(TXD0,TXD1,TXD2,TXD3,TXEN) to TXCLK matching	<120mil
(RXD0,RXD1,RXD2,RXD3,RXDV) to RXCLK matching	<120mil

Max trace length	<5 inches
The minimum spacing of RGMII Signals	At least 2 times the width of RGMII trace.
The minimum spacing between RGMII and other Signals	Recommend 3 times the width of RGMII trace. At least 2 times the width of RGMII trace.

3.8 Video Input PCB Design

MIPI RX signal design requirements are as follows:

- The differential signal takes GND as a reference layer and keeps the integrity of the reference layer;
- The length of PCB trace is recommended to be within 7.2 inches, the equal length of the differential pair P/N is controlled within 24 mil, take the sampling differential clock as reference between pairs, and the equal length is controlled within 42 mil (use the package+PCB together to control equal length).
- The differential impedance of the PCB trace of the MIPI RX differential pair is controlled within $100\Omega \pm 10\%$.
- When the differential signal passes through connectors, the neighbouring differential signal pair should be isolated by GND pin.
- To improve the performance of MIPI-CSI, please place the decoupling capacitors of the controller power supply close to the pins;
- The distance between the differential pair and other signals should follow the 3W principle.

Parallel CIF interface signal design requirements are as follows::

- Avoid signal traces crossing the power supply division area, and keeps the integrity of the reference layer;
- Keep the distance between neighbouring signal traces following "3W" principle;
- The line length of CIF_DATA, CIF_HSYNC, and CIF_VSYNC are based on the line length of CIF_CLKOUT and CIF_CLKIN, and the error is controlled within $\pm 50\text{mil}$.

3.9 Video Output PCB Design

MIPI TX signal design requirements are as follows:

- The differential signal takes GND as a reference layer and keeps the integrity of the reference layer;
- The differential impedance of the PCB trace of the MIPI TX differential pair is controlled within $100\Omega \pm 10\%$.
- If using FPC connection, it is recommended that the total length of PCB+FPC does not exceed 6 inches.
- The equal length of the differential pair P/N should be controlled within 24 mils, with CLK as equal length between pairs, which should be controlled within 42 mils.

Table 3–9 MIPI Layout Requirements

Parameter	Requirement
Trace Impedance	$100\Omega \pm 10\%$ differential
Max intra-pair skew	<24mil
Data to clock matching	<42mil
Max trace length	<6 inches
Maximum allowed via	4
Minimum pair to pair spacing	Recommend >3 times the width of MIPI trace. At least 2 times the width of MIPI trace . Try to increase Spacing between pairs whenever it is possible.
The minimum spacing between MIPI and other Signals	Recommend >3 times the width of MIPI trace. At least 2 times the width of MIPI trace .

Video output BT1120 and LCDC signal design requirements are as follows:

Table 3–10 BT1120 Layout Requirements ($\leq 74.25\text{Mhz}$)

Parameter	Requirement
-----------	-------------

Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock matching	<180mil
Max trace length	<5 inches
The minimum spacing of LCDC Signals	Recommend 2 times the width of LCDC trace.

Table 3–11 BT1120 Layout Requirements (148.5Mhz)

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock matching	<180mil
Max trace length	<4 inches
The minimum spacing of LCDC Signals	Recommend 2 times the width of LCDC trace.

Table 3–12 LCDC Layout Requirements ($\leq 74.25\text{Mhz}$)

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock matching	<180mil
Max trace length	<5 inches
The minimum spacing of LCDC Signals	Recommend 2 times the width of LCDC trace.

Table 3–13 LCDC Layout Requirements (148.5Mhz)

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock matching	<180mil
Max trace length	<3 inches
The minimum spacing of LCDC Signals	Recommend 2 times the width of LCDC trace.

3.10 USB PCB Design

USB signal design requirements are as follows:

- The error of the trace length in the differential signal group is controlled within $\pm 30\text{mil}$, and the differential impedance is controlled within $90\text{ohm} \pm 10\%$.
- The differential signal takes GND as a reference layer and keeps the integrity of the reference layer;
- The length of the USB2.0 differential signal trace of RV11XX should not exceed 6inch, and the number of vias should not exceed 6. A GND via should be placed near the USB signal via to obtain better signal quality.
- Avoid closing to other signals, and ensure that the distance to other signals is greater than 20mil.
- The REXT resistor needs to be placed close to the controller.
- The parasitic capacitances of ESD devices are recommended to be less than 1pF.

Table 3–14 USB 2.0 Layout Requirements

Parameter	Requirement
Trace Impedance	$90\Omega \pm 10\%$ differential
Max intra-pair skew	<30mil
Max trace length on carrier board	<6 inches
Maximum allowed via	Recommend less than 4 vias Cannot exceed 6 vias

4 Thermal Design Recommendations

4.1 Thermal Simulation Results

For Reliability and operability issues, the absolute maximum junction temperature must be less than 125 °C.



Note

The thermal resistance is the reference value under the condition of no external heat dissipation on the PCB. The actual temperature is related to the design, size, thickness, materials and other physical factors of the board.

4.1.1 The Result Overview

Thermal resistance simulation results are as follows

Table 4-1 Chip thermal resistance simulation report

Parameter	Symbol	Typical	Unit
Junction-to-ambient thermal resistance	θ_{JA}	33.3	(°C/W)
Junction-to-board thermal resistance	θ_{JB}	7.3	(°C/W)
Junction-to-case thermal resistance	θ_{JC}	3.7	(°C/W)

4.1.2 PCB Description

The PCB structure for thermal resistance simulation is as follows:

Table 4-2 The PCB structure for thermal resistance simulation

PCB	PCB Dimension (L x W)	45 x 45mm
	PCB Thickness	1.6mm
	Number of Cu Layer	4-layers

4.1.3 Terms interpretation

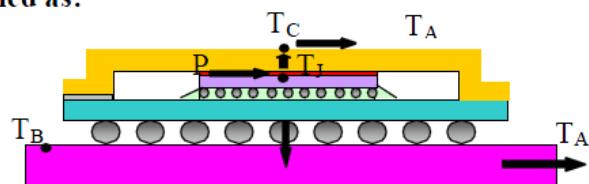
The terms in this chapter are as follows:

- T_J : maximum junction temperature;
- T_A : environment temperature;
- T_C : the maximum temperature of the package case
- T_B : the maximum temperature of the PCB combination surface;
- P: total input power

The thermal parameter can be define as following

1. Junction to ambient thermal resistance, θ_{JA} , defined as:

$$\theta_{JA} = \frac{T_J - T_A}{P}; \quad (1)$$



Thermal Dissipation of EHS-FCBGA

Figure 4-1 θ_{JA} definition

2. Junction to case thermal resistance, θ_{JC} , defined as:

$$\theta_{JC} = \frac{T_J - T_C}{P}; \quad (2)$$

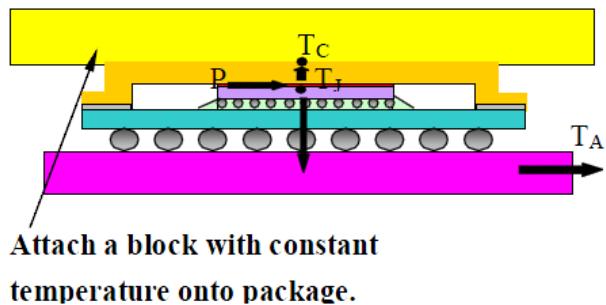


Figure 4-2 θ_{JC} definition

3. Junction to board thermal resistance, θ_{JB} , defined as:

$$\theta_{JB} = \frac{T_J - T_B}{P}; \quad (3)$$

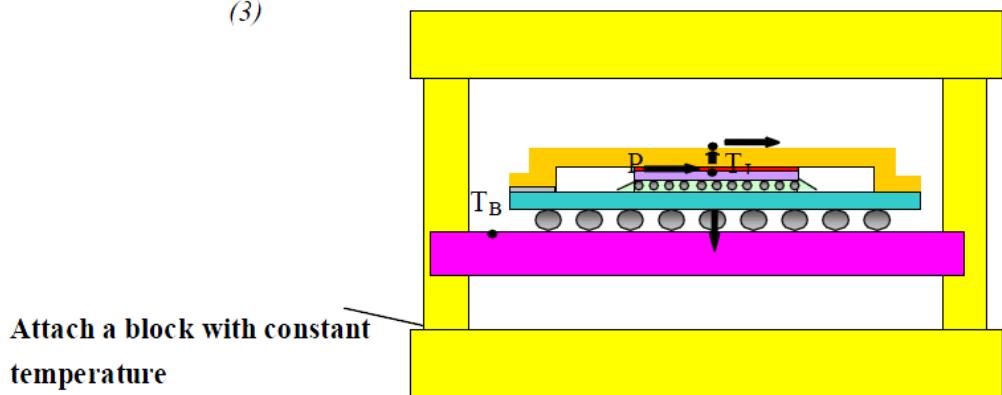


Figure 4-3 θ_{JB} definition

4.2 Thermal Control Solution inside the Chipset

4.2.1 Thermal Control Strategy

The thermal control frame “Linux Generic Thermal System Drivers” is defined in Linux kernel. Which can control system temperature through different strategies. Currently, the commonly used 3 strategies are showed as follows:

- Power_allocator: introduce PID (percentage-integral-differential) control to dynamically allocate power for modules according to current temperature, and convert power to frequency, so as to achieve the effect of limiting frequency by temperature.
- Step_wise: limit frequency step by step according to current temperature.
- Userspace: do not limit frequency.

There is a T-sensor inside the chipset to detect internal temperature, taking Power_allocator strategy by default, the working statuses as below:

- When the temperature is over the set value:
 - As the temperature trend increases, the maximum frequency allowed will decrease;
 - As the temperature trend decreases, the maximum frequency allowed will increase;
- When the temperature decreases to the set value:
 - The maximum frequency allowed is the default value and is not controlled by thermal;
- The software will trigger restart when the chipset is still over temperature (such as poor heat dissipation) after frequency reduction. When the chipset cannot be restarted due to deadlock or other causes, which causes the chipset to exceed a certain temperature, the otp_out inside the chip will be triggered to PMIC and shut down directly. Fore detailed temperature depends on the final software strategy settings.



Note

Temperature tendency is achieved by comparing the neighbouring two values captured. When device temperature is not over the threshold value, capture one temperature per second; when device temperature is over the threshold value, capture temperature every 20 ms and limit the frequency.

4.2.1.1 Temperature Control Configuration

The system SDK can provide temperature control strategies for ARM, NPU, and VEPU respectively. Please refer to “Rockchip thermal development guide” for detailed configurations.

5 ESD/EMI Protection Design

5.1 Overview

This chapter provides ESD/EMI protection design suggestion for product design to help customers to improve anti-static and anti-electromagnetic interference ability of products.

5.2 Terms Interpretation

Terms of this chapter are explained as below:

- ESD: Electro-Static discharge
- EMI: Electromagnetic Interference: including conduction interference and radiation interference.

5.3 ESD Protection

- Ensure reasonable mold design; reserve anti ESD components for ports and connectors.
- Protect and isolate sensitive components in PCB layout.
- Try best to put the chipset and core components in the center of PCB layout. If not able to put them in the center, need to ensure that the shielding cover has 2mm distance at least from the board edge and is connected to GND safely.
- PCB layout is based on function module and signal flow direction, sensitive components should be mutually independent, and it is better to isolate the parts that are easy to produce interference;
- Place ESD components reasonably. Generally place at the source, that is, place ESD components in the junction or electrostatic discharge.
- Components layout should be away from the board edge and keep some distance from the connectors.
- Make sure good inner and outer ground loops to ensure the smoothness of the electrostatic loop in PCB design, to avoid the generation of large potential differences caused by static electricity and abnormal system control;
- Do not go through the edge of surface layer and make as many ground holes as possible.
- Isolate signal from ground if necessary.
- Expose GND copper of the PCB as much as possible, in order to well connect the complete machines with the conductive structural parts during assembly and enhance electrostatic discharging effect.

5.4 EMI Protection

- Electromagnetic interference has three factors: interference sources, coupling channels and sensitive devices. We have no way to deal with sensitive equipment, so EMI problem can only start with interference sources and coupling channels. The best way to resolve EMI issues is to eliminate interference source. If cannot eliminate, try to cut off coupling channels or avoid antenna effect.
- It is difficult to eliminate interference source on PCB. We can take actions such as filtering, grounding, balancing, resistance controlling, improving signal quality (e.g. termination connection) etc. Generally several methods will be applied together, but the basic requirement is good grounding.
- The commonly used EMI materials include shielding cover, special filter, resistor, capacitor, inductor, magnetic bead, common mode choke/magnetic ring, wave-absorbing material, spread frequency device

etc.

- The rules to select filters: if the load (receiver) is high resistance (normal single port signal interface is high resistance, such as SDIO, RBG, CIF etc.), select capacitive filter components and parallel connect to circuit; if the load (receiver) is low resistance (such as power output interface), select inductive filter component and serial connect to circuit. After using the filter device, the signal quality cannot exceed its SI permission. Differential interface usually uses common mode choke to suppress EMI.
- The shielding measures on PCB should have good grounding, otherwise it will cause radiation leakage or form antenna effect. The shielding of connectors should comply with relevant technical standards.
- The use of the spread spectrum function of the core device: if the radiated interference can clarify the frequency point and the generation source, the spread energy of the related clock can be used to reduce the radiated energy. If the design requirements can be met In principle, the smaller the spread spectrum amplitude, the better, to reduce risk;
- EMI has the same high requirement as ESD on layout. The ESD Layout requirements described above are mostly suitable for EMI protection. Besides, add the following requirements:
 - Try best to ensure the integrality signal and reference surface.
 - Differential line should in equal length and be tight coupling to ensure the symmetry of the differential signal, minimize the misplacement of differential signals to avoid EMI problems caused by phase mismatch;
 - Components with metal shell such as plug-in electrolytic capacitors should avoid coupling interference signals to radiate. Also need to avoid component interference signals coupling from shell to other signal lines.

6 Soldering Process

6.1 Overview

RV1126/RV1109 chipset are ROHS certified products, that is, they are all Lead-free products. This chapter regulates basic temperature settings of each period when customers use the chipset SMT. It mainly introduces process control when using RV1126/RV1109 chipset reflow soldering: lead-free process and mixed process.

6.2 Terms Interpretation

Terms in this chapter are explained below:

- Lead-free: Lead-free process;
- Pb-free: Pb-free process, all devices (main board, all ICs, resistors and capacitors, etc.) are lead-free devices, and the lead-free solder paste are used in the pure lead-free process;
- Reflow profile: reflow soldering
- Restriction of Hazardous Substances (ROHS) : instructions for restricting use of certain hazardous components in electrical and electronic equipment;
- Surface Mount Technology (SMT) ;
- Sn-Pb: Sn-Pb mixing process refers to using lead solder paste and a mixed soldering process with both lead-free BGA and lead IC;

6.3 Reflow Soldering Requirements

6.3.1 Solder Paste Composition Requirements

The proportion of Solder alloy and flux is 90%: 10%; volume ratio: 50%: 50%, solder paste refrigerating temperature is 2~10°C, the temperature should be returned to normal temperature before use, and the return time should be 3~4 hours and the time should be recorded.

The solder paste needs to be stirred before brushing, manual stirring for 3 to 5 minutes or mechanical stirring for 3 minutes. After stirring, it will flow naturally.

6.3.2 SMT Profile

Since RK chipset are made of environmental protection materials, Pb-Free process is recommended. The reflow profile shown below is only recommended for JEDEC J-STD-020D process requirements, and customers need to

adjust according to actual production conditions.

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time at liquidous (t_L)	60-150 seconds	60-150 seconds
Peak package body temperature (T_p)*	See classification temp in Table 4.1	See classification temp in Table 4.2
Time (t_p)** within 5 °C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Figure 6-1 Reflow profile classification

Package Thickness	Volume mm ³ <350	Volume mm ³ 350 - 2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Figure 6-2 Standard for heat resistance of lead-free process device packages

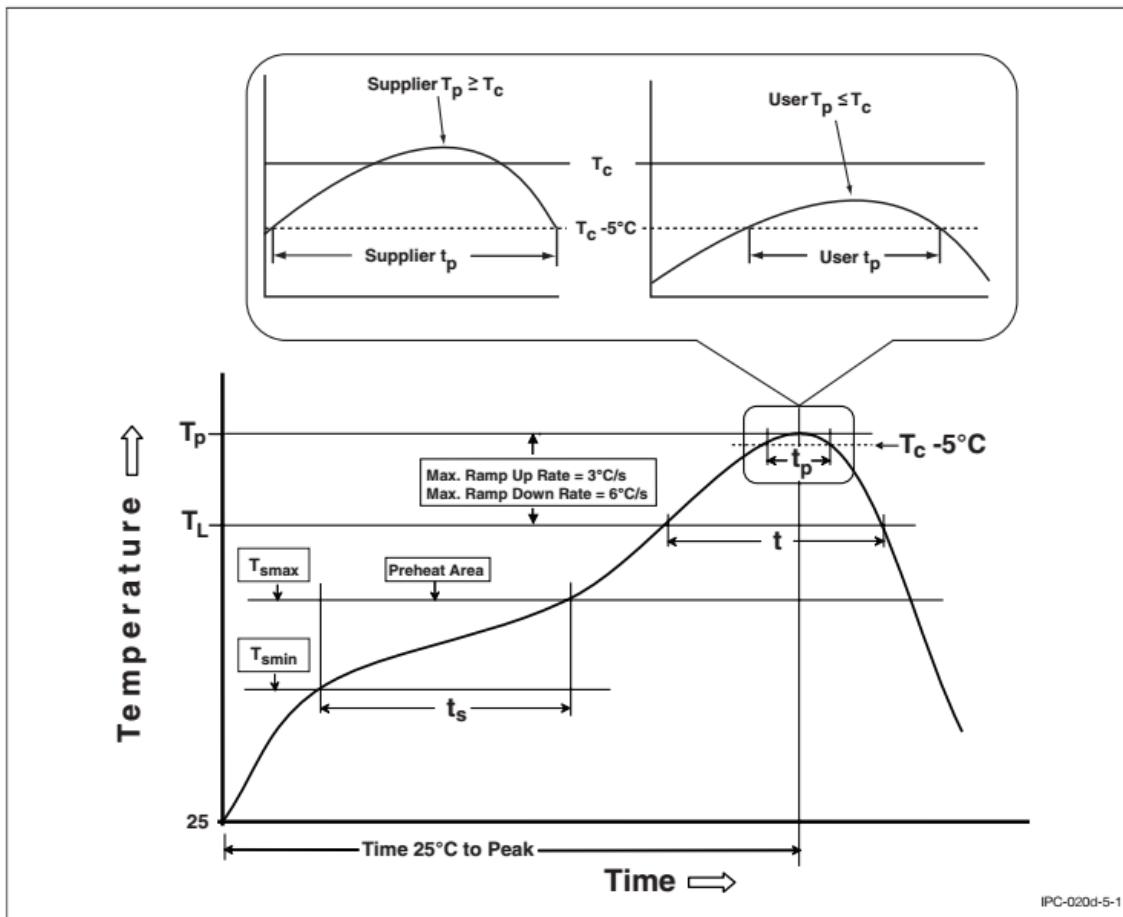


Figure 6-3 Lead-free reflow profile

6.3.3 SMT Recommendation Profile

The SMT profile recommended by RK is shown in Figure 6-4:

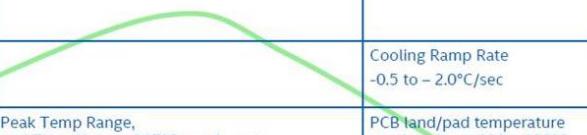
Step 1 Board Preheat	Step 2 Soak Time	Step 3 Peak Reflow & Time Above 220 °C	Step 4 Cool Down
Start with solder joint temp \leq 40°C	After nozzle is lowered prior to peak reflow (Soak Time: Paste dependant; consult paste manufacturer)	Solder Joint Temp 230 – 250°C Above \geq 217°C 60 – 90 sec Max delta-t of solder joint temperature at peak reflow \leq 10°C	Substrate MAX Temperature \leq 260°C Die Peak Temperature \leq 300°C
Rising Ramp Rate 0.5 – 2.5° C/ Sec.	Solder Joint Temp: 200 to 220°C		Cooling Ramp Rate -0.5 to – 2.0°C/sec
Board Preheat Solder Joint Temp: 125 – 150°C	Critical Ramp Rate (205 to 215°C): 0.35 – 0.75°C/sec.	Peak Temp Range, and Time Above \geq 217°C spec's met.	PCB land/pad temperature needs to be at 100 – 130°C \pm 5°C when removing board from rework machine bottom heater at end of component removal operation or \leq 80°C when using stand alone PCB Pre-Heater for PCB land/pad site dress operation.
Preheat with bottom heater, before nozzle is lowered	Nozzle has lowered to reflow component	Nozzle is down during peak reflow	Nozzle raises to home position when solder joint reaches peak temp range

Figure 6-4 Lead-free reflow soldering process recommended profile parameters

7 Packages and storage conditions

7.1 Overview

This chapter introduces the storage and directions for chipset usage to ensure the safety and correct usage of products.

7.2 Terms Interpretation

Terms in this chapter are explained below:

- Desiccant: a material used to adsorb moisture
- Floor life: the maximum time products are allowed to be exposed to environment, from before unpacking moisture barrier bag to reflow soldering;
- HIC: Humidity Indicator Card
- MSL: Moisture Sensitivity Level
- MBB: Moisture Barrier Bag
- Rebake: to bake again
- Solder Reflow
- Shell Life
- Storage environment

7.3 Moisture Packages

The dry vacuum package material of product is shown as follows:

- Desiccant;
- Six-point humidity card;
- Moisture barrier bag: aluminum foil, silver opaque, with a mark of moisture sensitivity level;



Figure 7-1 Chipset dry vacuum package

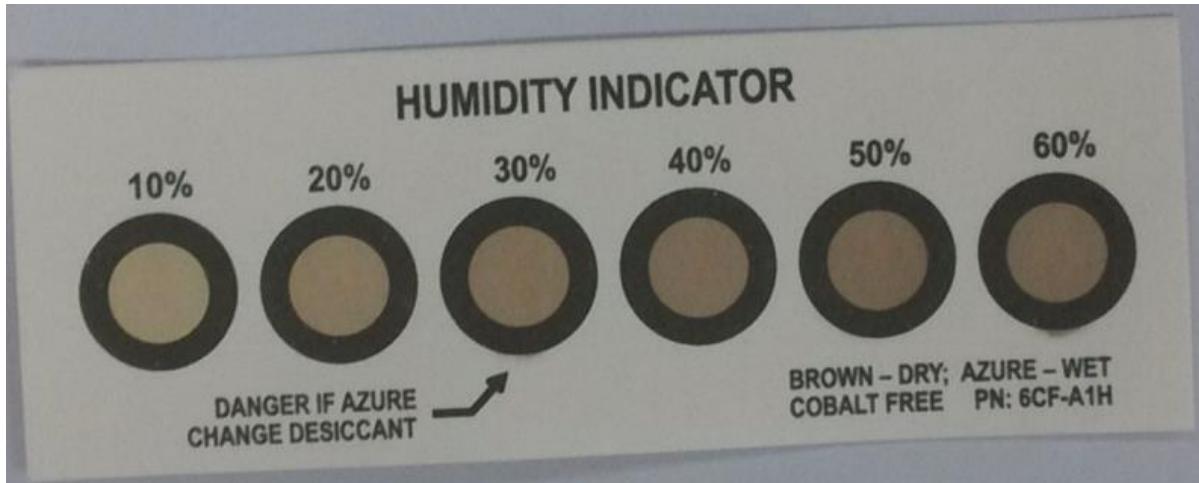


Figure 7-2 Six-point humidity card

7.4 Product Storage

7.4.1 Storage Environment

The product is stored in vacuum packaging, and the storage period can reach 12 months when the temperature is $\leq 40^{\circ}\text{C}$ and the relative humidity is $<90\%$.

7.4.2 Exposure Time

For environmental conditions: $<30^{\circ}\text{C}$ and humidity 60%, please refer to Table 7-1 below.

The MSL level of RV1126/RV1109 chipset is 3 and is very sensitive to humidity. If package is not used in time after unpacking, and if it is not baked and directly SMT after being left for a long time, there will be a high probability of chip failure.

Table 7-1 Moisture Sensitivity Levels (MSL)

MSL等级	Exposure time	
	Factory environmental conditions: $\leq 30^{\circ}\text{C}/60\% \text{RH}$	
1	Unlimited at $\leq 300^{\circ}\text{C}/85\% \text{RH}$	
2	1 year	
2a	4 weeks	
3	168 hours	
4	72 hours	
5	48 hours	
5a	24 hours	
6	Please bake before use, and reflow within the time limit specified on the table.	

7.5 Usage of Moisture Sensitive Products

After RV1126/RV1109 chipset packages are opened, it must meet the following conditions before reflow soldering:

- Continuous or cumulative exposure time is within 168 hours, and factory environment is $\leq 30^{\circ}\text{C}/60\% \text{RH}$;
- Stored in $<10\%$ RH environment;

Chips must be baked to remove internal moisture under the following conditions to avoid layered or popcorn problems during reflow:

- When humidity indicator card is at $23 \pm 5^{\circ}\text{C}$, $>10\%$ points have changed color. (Please refer to humidity indicator cards for color change);
- Does not meet the specifications of 2a or 2b;

Please refer to Table 7-2 below for the time for chip re-baking:

Table 7-2 RV11XX chipset Re-bake reference table

Package Body	MSL	High Temp Bake @125°C +10/-0°C		Medium Temp Bake @90°C +8/-0°C		Low Temp Bake @40°C +5/-0°C	
		Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h	Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h	Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h
Thickness ≤1.4mm	3	9 hours	7 hours	33 hours	23 hours	13 days	9 days



Note

The table shows the minimum baking time necessary after damp.
Low temperature baking is preferred.