RV1126_RV1109_BATTERY_IPC_SMARTBELL_REF_V10

Quick start solution

RV1126_RV1109 Main difference		
	RV1126	RV1109
CPU	Quad A7	Dual A7
NPU	2.0Tops	1.2Tops
ISP	14M Pixel	5M Pixel

Reference Design Main Functions Introduction	
Power	Discrete Power
RAM	EMMC/SLC NAND FLASH/SPI FLASH
ROM	DDR3L/DDR3/LPDDR3/LPDDR4
Interface	SDMMC/SDIO/CIF/MIPI_DSI/MIPI_CSI0/ MIPI_CSI1/I2S/USB/ADC

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Project:	RV1126_RV1109_REF				
File:	00.Cover Page				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	1 of 34

Index and Notes

Table of Content

Note

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

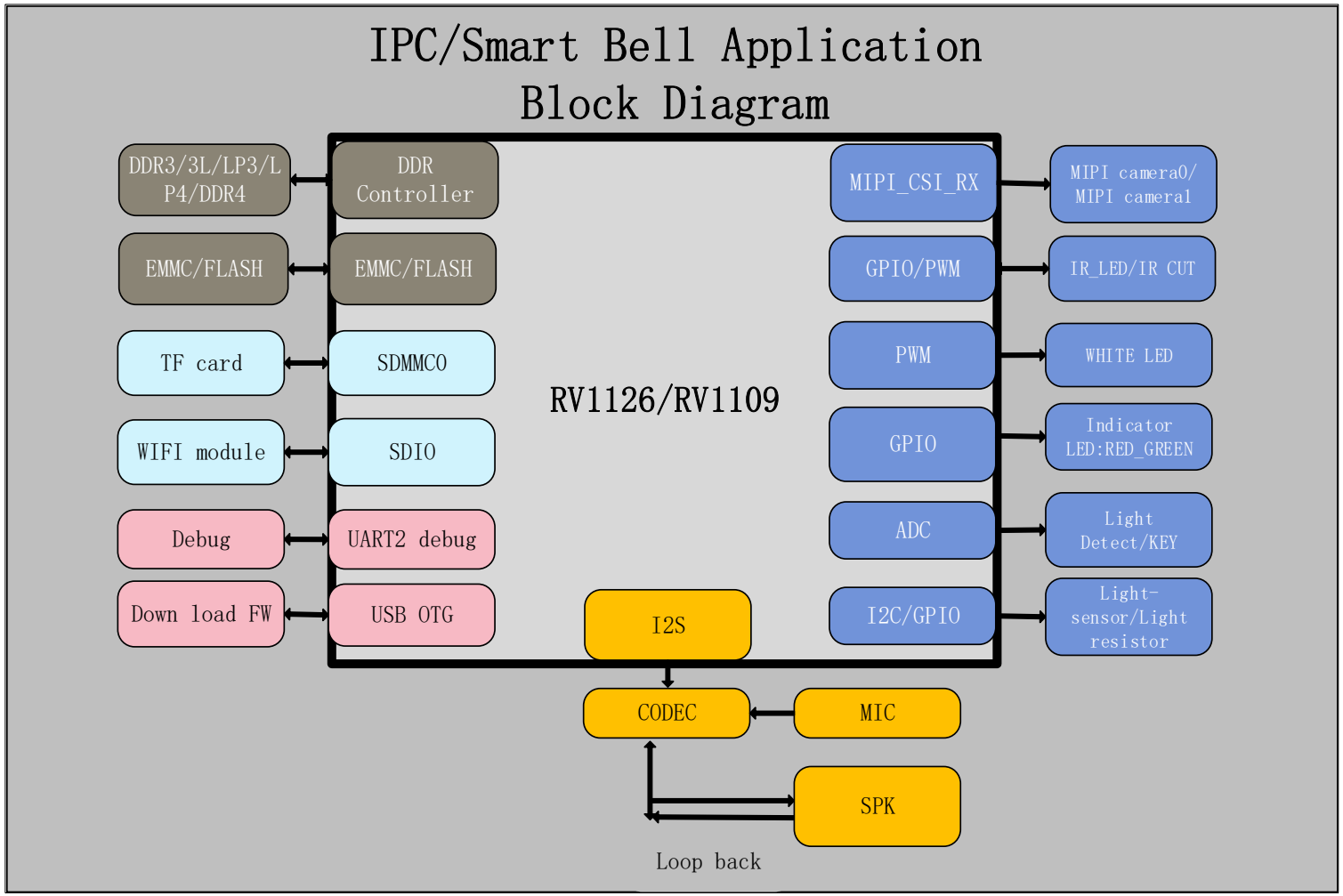
{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Graphic Description

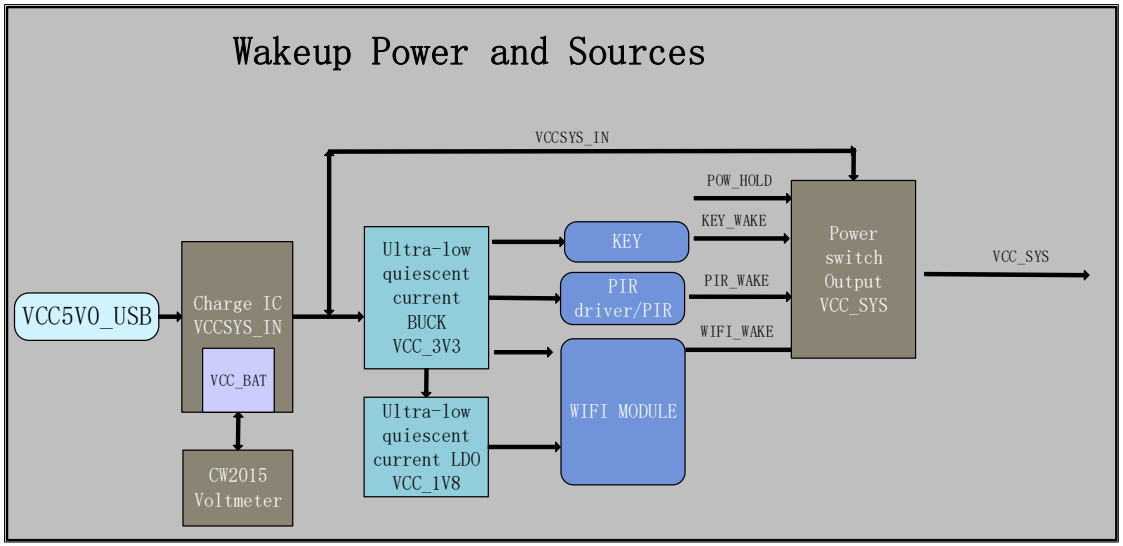
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	01.Index and Notes				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	2 of 34

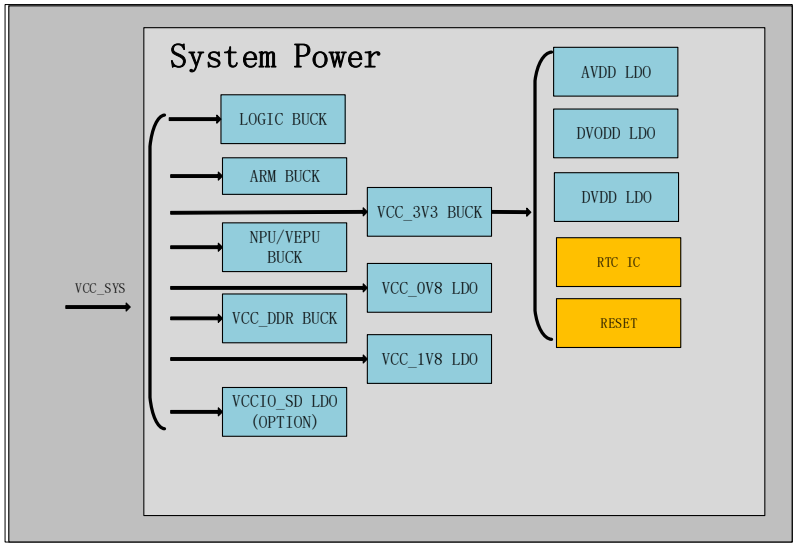
Revision History

Version	Date	Author	Change Note	Approved
V1.0	2020.07.13	Liyh	RV1126_RV1109_BATTERY_IPC_SMARTBELL_REF_V10	



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	03.Block Diagram				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	4 of 34





The reference power on sequence of discrete power

Power Name	Power Channel	Time Slot	Default voltage	Supply Limit	Peak Current
VCC_0V8	LDO	Slot: 1	0.8V	0.5A	
VDD_LOGIC	BUCK	Slot: 2	0.8V	2.0A	1.75A
VDD_ARM	BUCK	Slot: 2	0.8V	1.0A	0.73A
VDD_NPU_VEPU	BUCK	Slot: 2	0.8V	3.0A	2.11A
VCC_1V8	LDO	Slot: 3	1.8V	2.0A	
VCC_DDR	BUCK	Slot: 4	1.2V	0.4A	
VCC_3V3	BUCK	Slot: 5	3.3V	2.0A	
VCCIO_SD	LDO(option)		3.3V	0.5A	
VCC1V8_DOVDD	LDO		1.8V	0.5A	
VCC1V2_DVDD	LDO		1.2V	0.5A	
VCC2V8_AVDD	LDO		2.8V	0.5A	
RESET					

NOTE:VCC_DVDD and VCC_AVDD according to camera sensor voltage

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Project:	RV1126_RV1109_REF				
File:	04.Power Sequence				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	5 of 34

I2C MAP

Port	Bus Name	Domain	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Slave Bus Capability	Note
I2C0	I2C0_SCL I2C0_SDA	PMUIO1	VCC_3V3	BM8563	Read:0A3H, Write: 0A2H		
				CW2015	Read:0XC5, Write: 0XC4		
I2C1	I2C1_SCL I2C1_SDA	VCCIO4	VCC_1V8	MIPI Camera			
				CIF Camera			
I2C4	I2C4_SCL_M1 I2C4_SDA_M1	VCCIO7	VCC_3V3	ES8311	0x18		
I2C5	I2C5_SCL_M0 I2C5_SDA_M0	VCCIO5_VDD	VCC_3V3	CM32181A3OP	0x48		

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Project:	RV1126_RV1109_REF				
File:	05.I2C MAP				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	6 of 34

IO Power Domain Map

IO Domain	IO Group	Support of IO Voltage		Default Actual assigned IO Domain Voltage		Notes
		1.8V	3.3V	Net Name of Power Supply	Voltage	
PMUIO0	***GPIO0A***	✓	✓	*VCC_1V8*	*1.8V*	
PMUIO1	***GPIO0BC***	✓	✓	*VCC_3V3*	*3.3V*	
VCCIO1	***GPIO0CD/GPIO1A***	✓	✓	*VCCIO_FLASH*	*1.8V*	*GPIO0_B3/FLASH_VOL_SEL pin defined as a set pin for VCCIO1.*
VCCIO2	***GPIO1AB***	✓	✓	*VCCIO_SD*	*3.3V*	
VCCIO3	***GPIO1BCD***	✓	✓	*VCC_1V8*	*1.8V*	
VCCIO4	***GPIO1D/GPIO2A***	✓	✓	*VCC_1V8*	*1.8V*	
VCCIO5	***GPIO2ABCD/GPIO3A***	✓	✓	*VCC_3V3*	*3.3V*	
VCCIO6	***GPIO3ABC***	✓	✓	*VCC_1V8*	*1.8V*	
VCCIO7	***GPIO3D/GPIO4A***	✓	✓	*VCC_3V3*	*3.3V*	

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Project:	RV1126_RV1109_REF				
File:	06.IO Power Domain Map				
Date:	Monday, July 13, 2020			Rev:	V1.0
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Power

U1000N
RV1126_RV1109
BGA409_14R00X14R00X0R90

NPU/LOGIC/VEPU/ARM Power

NPU_VDD_1	H11	VDD_NPU_VEPU
NPU_VDD_2	H12	
NPU_VDD_3	J10	
NPU_VDD_4	J11	
NPU_VDD_5	K10	
NPU_VDD_6	K11	
LOGIC_VDD_1	H9	VDD_LOGIC
LOGIC_VDD_2	J9	
LOGIC_VDD_3	L10	
LOGIC_VDD_4	M11	
LOGIC_VDD_5	H13	
LOGIC_VDD_6	J13	
VEPU_VDD_1	L9	VDD_NPU_VEPU
VEPU_VDD_2	M9	
VEPU_VDD_3	N8	
VEPU_VDD_4	N9	
ARM_VDD_1	N12	VDD_ARM
ARM_VDD_2	P12	
ARM_VDD_3	P13	

Supply for VCCIO1~7 Power

VCCIO_VDD_1V8	H14	VCC_1V8

C1000 100nF X5R 6.3V C0402

NOTE:
If any power domain of vccio 1 ~ vccio 7 is used,
then VCCIO_ VDD_ 1V8 must be connected to 1.8V power supply

VDD_NPU_VEPU

C1006 10uF X5R 4V C0402
C1005 1uF X5R 6.3V C0402
C1004 1uF X5R 6.3V C0402
C1003 100nF X5R 6.3V C0201
C1002 100nF X5R 6.3V C0201
C1001 100nF X5R 6.3V C0201

For NPU Power

VDD_NPU_VEPU

C1019 10uF X5R 4V C0402
C1018 1uF X5R 6.3V C0402
C1017 100nF X5R 6.3V C0201
C1016 100nF X5R 6.3V C0201

For VEPU Power

VDD_ARM

C1015 10uF X5R 4V C0402
C1014 1uF X5R 6.3V C0402
C1013 100nF X5R 6.3V C0201
C1012 100nF X5R 6.3V C0201

VDD_LOGIC

C1011 10uF X5R 4V C0402
C1009 1uF X5R 6.3V C0402
C1010 1uF X5R 6.3V C0402
C1007 100nF X5R 6.3V C0201
C1008 100nF X5R 6.3V C0201

GND

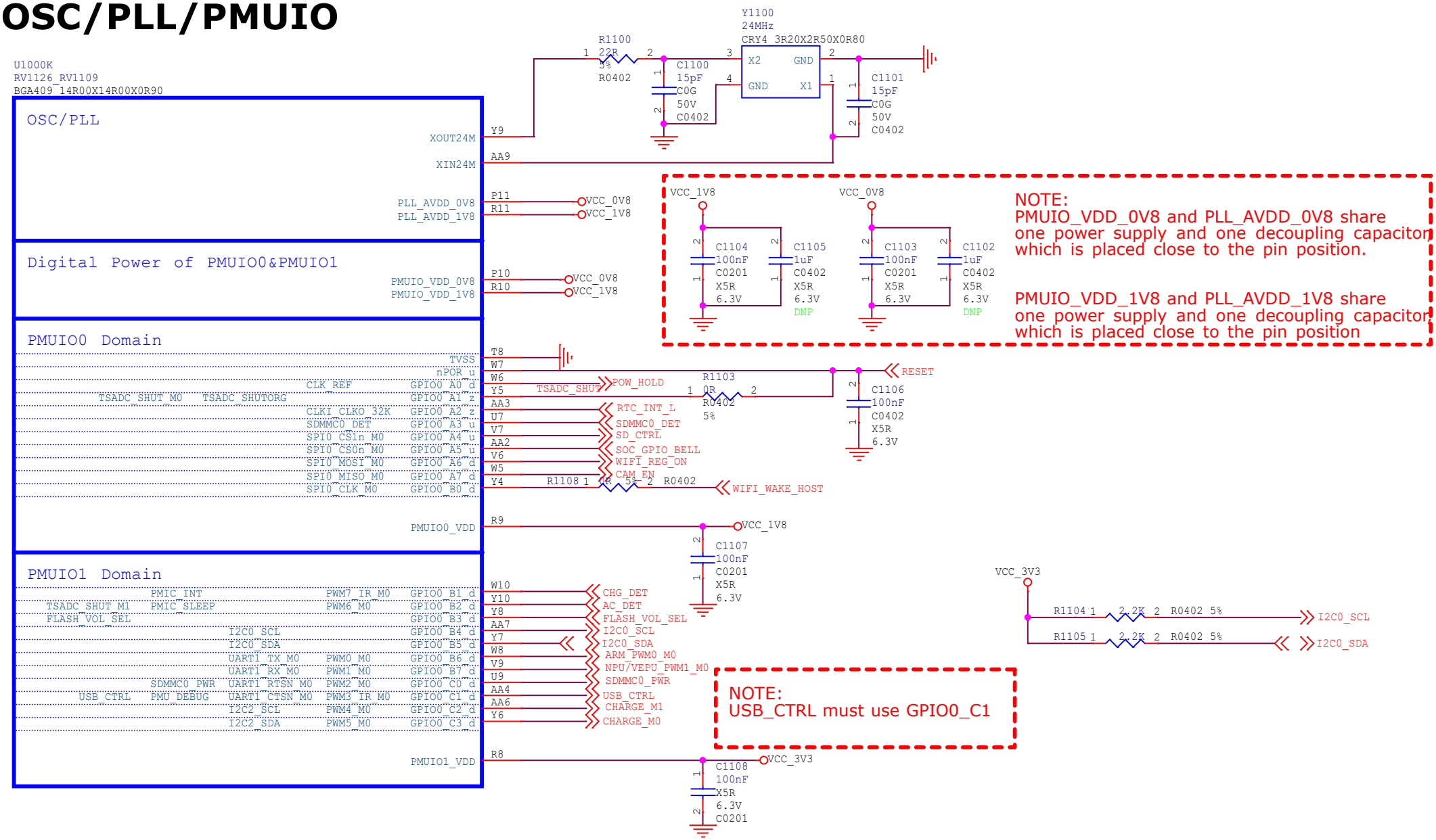
U1000O
RV1126_RV1109
BGA409_14R00X14R00X0R90

VSS/AVSS

A1	VSS_1		VSS_53	K9	
A21	AVSS_2		VSS_54	K12	
B12	VSS_3		VSS_55	K13	
C3	VSS_4		VSS_56	K14	
C5	VSS_5		VSS_57	L2	
C7	VSS_6		VSS_58	L5	
C10	VSS_7		VSS_59	L6	
C12	VSS_8		VSS_60	L11	
D9	VSS_9		VSS_61	L12	
D12	VSS_10		VSS_62	L13	
D18	AVSS_11		VSS_63	L14	
E4	VSS_12		VSS_64	L16	
E6	VSS_13		VSS_65	M3	
E8	VSS_14		VSS_66	M5	
E9	VSS_15		VSS_67	M7	
E10	VSS_16		VSS_68	M8	
E11	VSS_17		VSS_69	M10	
E12	VSS_18		VSS_70	M12	
F3	VSS_19		VSS_71	M13	
F5	VSS_20		VSS_72	M14	
F7	VSS_21		VSS_73	M16	
F8	VSS_22		VSS_74	N5	
F9	VSS_23		VSS_75	N6	
F10	VSS_24		VSS_76	N7	
F11	VSS_25		VSS_77	N10	
F12	VSS_26		VSS_78	N11	
F13	VSS_27		VSS_79	N13	
F14	AVSS_28		VSS_80	N14	
F15	AVSS_29		VSS_81	N16	
G2	VSS_30		VSS_82	P5	
G5	VSS_31		VSS_83	P7	
G6	VSS_32		VSS_84	P8	
G10	VSS_33		VSS_85	P9	
G11	VSS_34		VSS_86	P14	
G12	VSS_35		VSS_87	P16	
G13	VSS_36		VSS_88	R1	
G16	AVSS_37		VSS_89	R5	
G17	AVSS_38		VSS_90	R12	
H4	VSS_39		VSS_91	R13	
H5	VSS_40		VSS_92	R14	
H6	VSS_41		VSS_93	T6	
H7	VSS_42		VSS_94	T9	
H10	VSS_43		VSS_95	T10	
H15	VSS_44		VSS_96	T14	
J5	VSS_45		VSS_97	T17	
J6	VSS_46		VSS_98	V17	
J12	VSS_47		VSS_99	W9	
J14	VSS_48		VSS_100	W14	
J16	VSS_49		VSS_101	AA1	
K5	VSS_50		VSS_102	AA10	
K6	VSS_51		VSS_103	AA21	
K8	VSS_52				

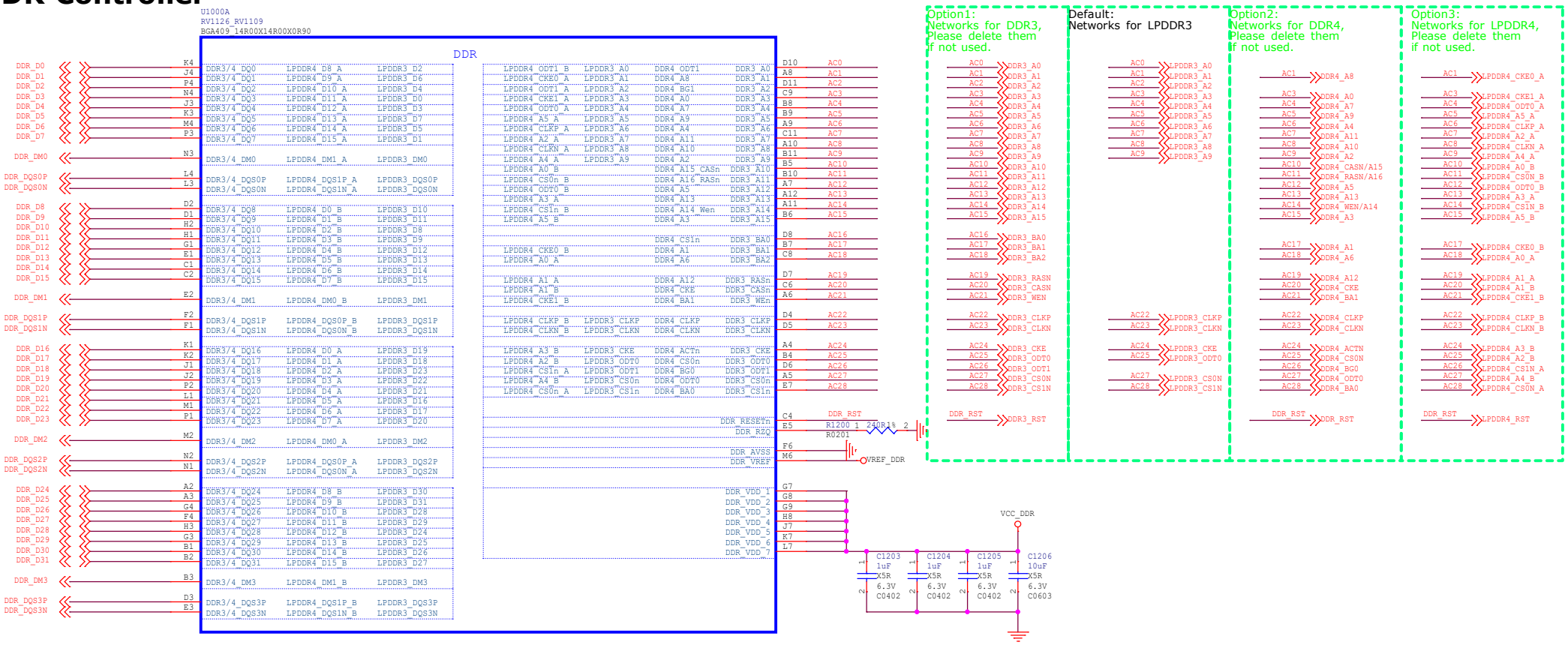
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd			
Project:	RV1126_RV1109_REF			
File:	10.RV1126/1109_Power/GND			
Date:	Monday, July 13, 2020		Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by: <Checker>	Sheet:	8 of 34

OSC/PLL/PMUIO



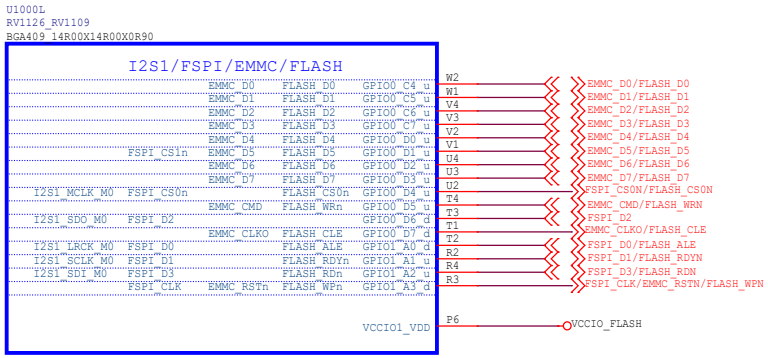
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	11.RV1126/1109_OSC/PLL/PMUIO				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	9 of 34

DDR Controller

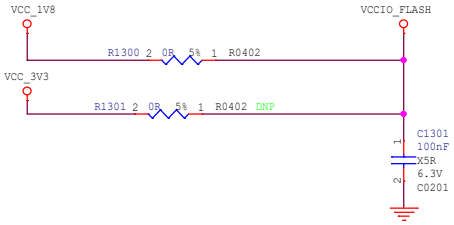


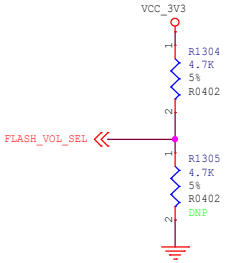
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RV1126_RV1109_REF		
File:	12.RV1126/1109_DRAM Controller		
Date:	Monday, July 13, 2020	Rev:	V1.0
Designed by: Yanhong.Li	Reviewed by: <Checker>	Sheet:	10 of 34

EMMC/FLASH



NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.

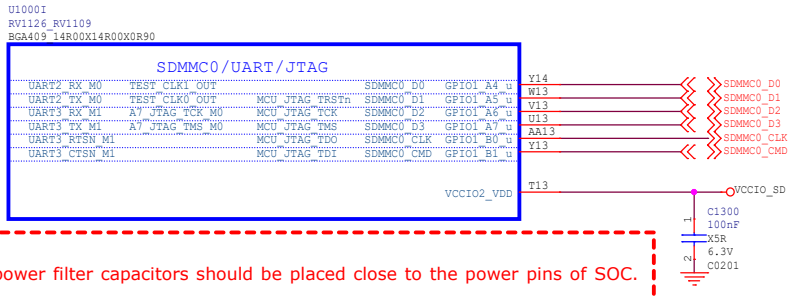




NOTE:
FLASH(VCCIO1) power domain IO supply configuration pin:

Condition	VCCIO1 (VCCIO_FLASH)
FLASH_VOL_SEL=0	3.3V
FLASH_VOL_SEL=1	1.8V Default

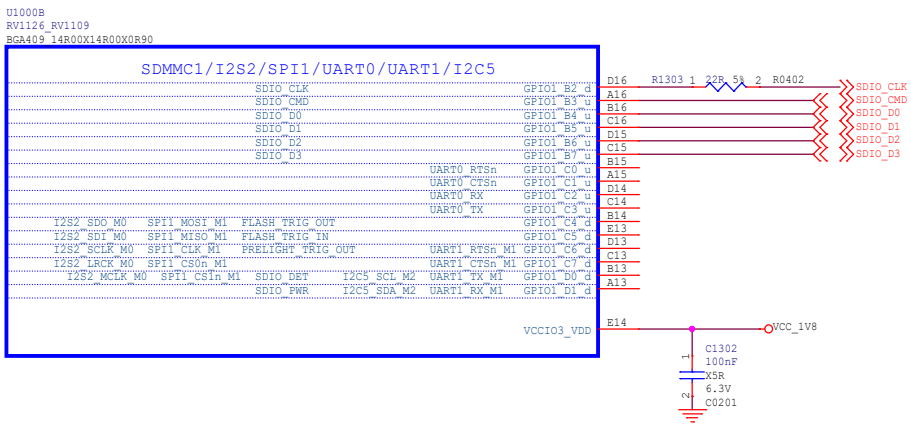
SDMMC0/JTAG



NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.

If SD card is not used,please reserve MCU JTAG interface

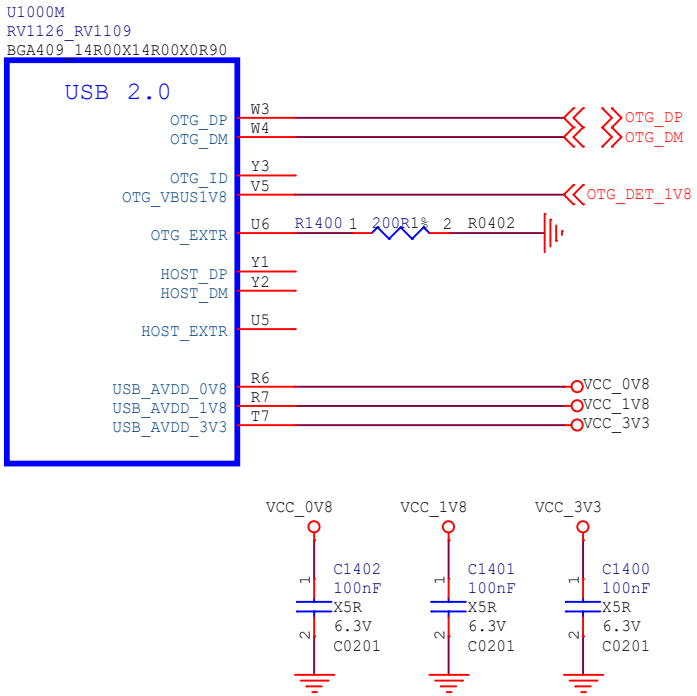
SDMMC1/UART/I2S2



NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	13.RV1126/1109_Flash/SD				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	11 of 34

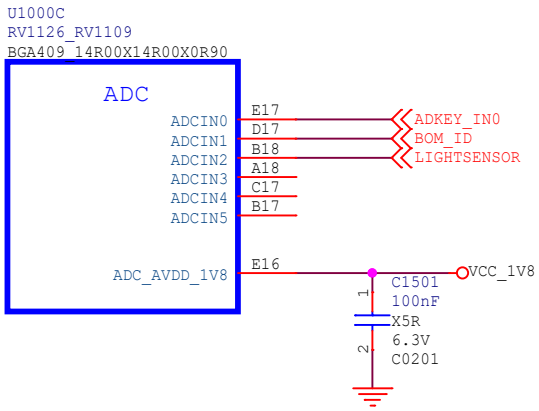
USB Controller

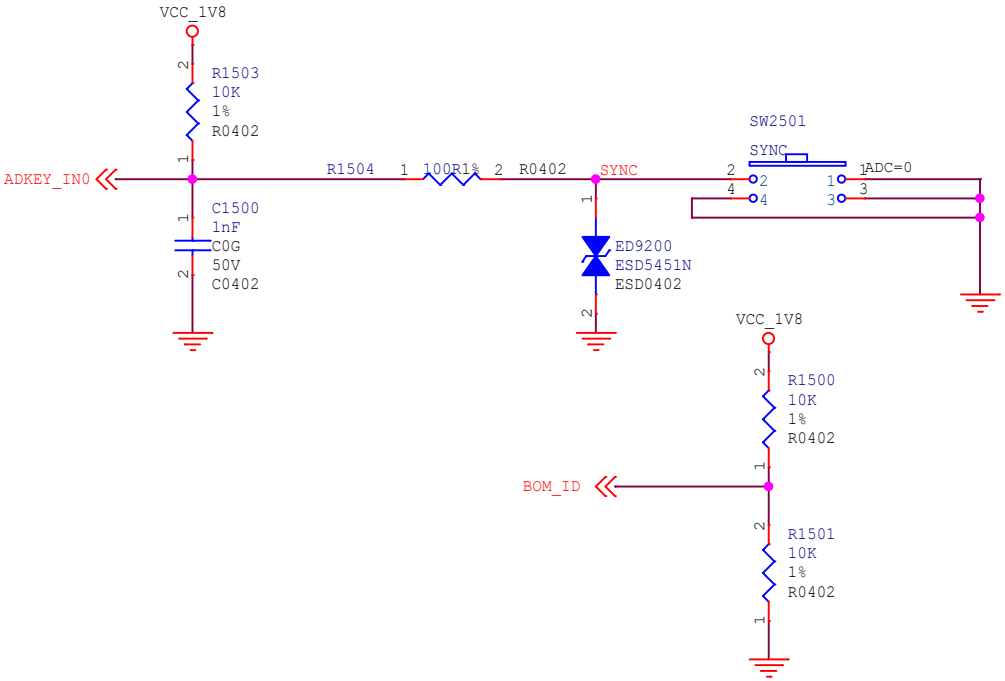


USB2.0 design rules:
1. Max intra-pair skew <4ps
2. Max trace length<6inchs
3. Max allowed via <6
4. Trace impedance 90ohm+/-10%
5. The distance between other signals follows the 3W rule.

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	14.RV1126/1109_USB Controller				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	12 of 34

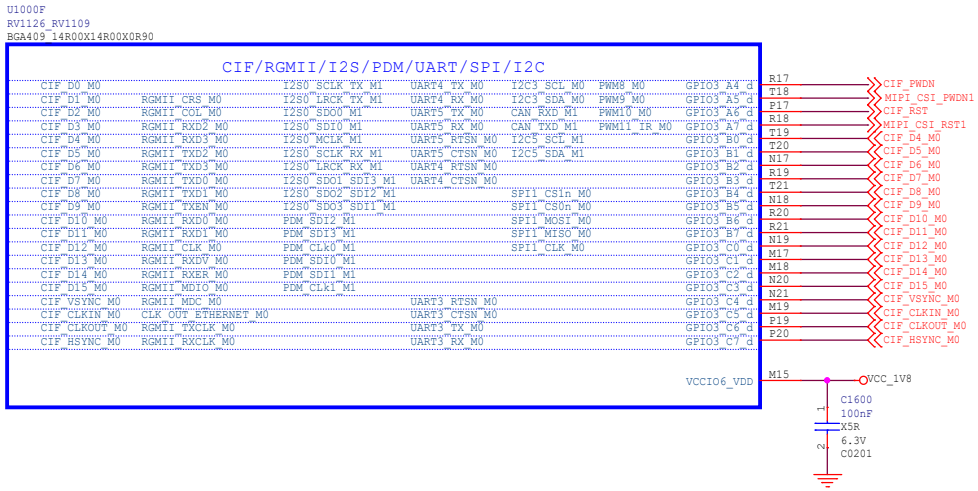
SARADC





Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	15.RV1126/1109_SARADC				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	13 of 34

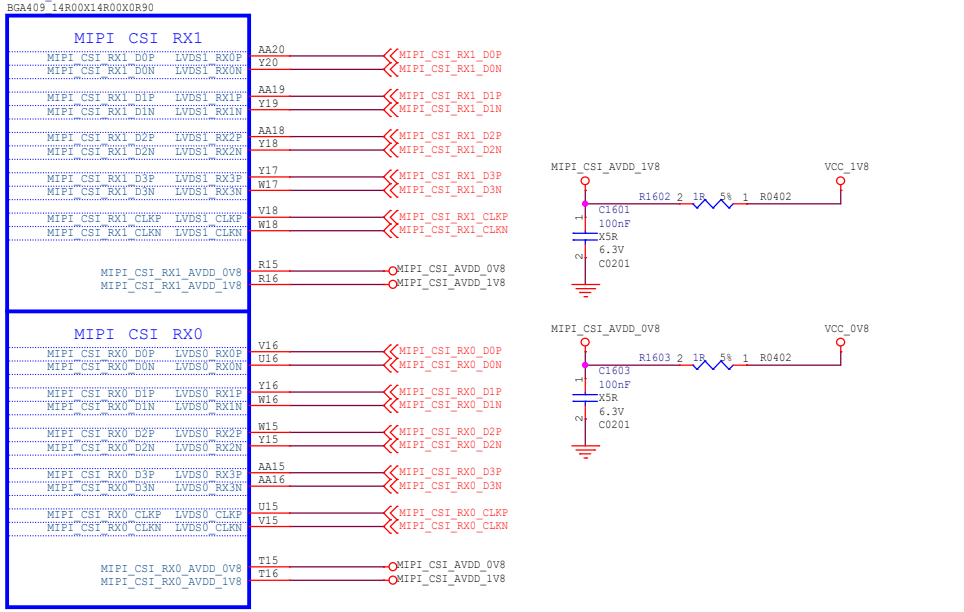
CIF Interface



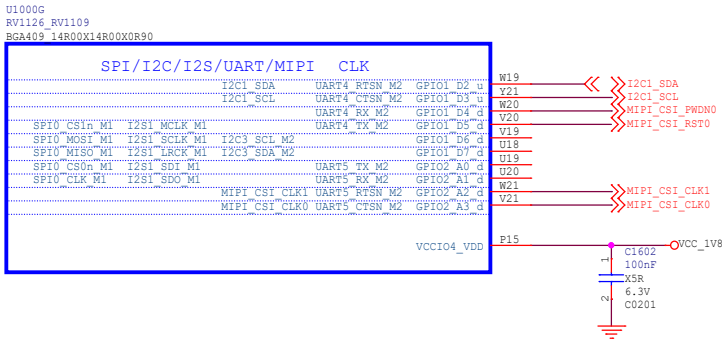
BT1120 RX	DATA:CIF_DATA[15:0] Y[0:7]:CIF_DATA[8:15] Cb[0:7]:CIF_DATA[0:7] CLOCK:CIF_CLKIN
12bit CIF camera	CameraCIF[12:0]:CIF_DATA[15:4] XCLK:CIF_CLKOUT PCLK:CIF_CLKIN HSYNC:CIF_HSYNC VSYNC:CIF_VSYNC
10bit CIF camera	CameraCIF[10:0]:CIF_DATA[15:6] XCLK:CIF_CLKOUT PCLK:CIF_CLKIN HSYNC:CIF_HSYNC VSYNC:CIF_VSYNC
8bit CIF camera	CameraCIF[8:0]:CIF_DATA[15:8] XCLK:CIF_CLKOUT PCLK:CIF_CLKIN HSYNC:CIF_HSYNC VSYNC:CIF_VSYNC

MIPI-CSI Interface

MIPI_CSI_RX0 and MIPI_CSI_RX1 power pins are adjacent, so they share a decoupling capacitor
All the power filter capacitors should be placed close to the power pins of SOC.

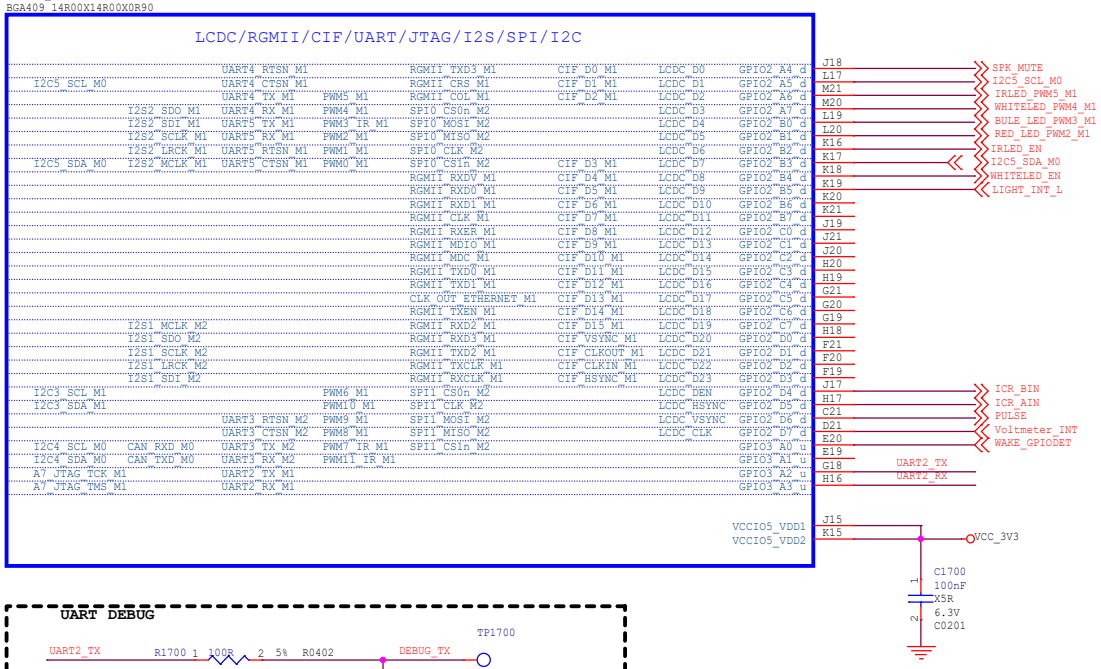


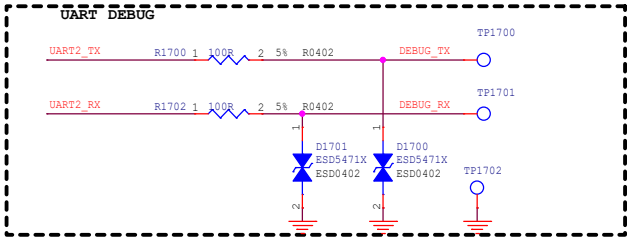
I2C/SPI/MIPI-CLK



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	16.RV1126/1109_VideoInput				
Date:	Tuesday, July 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	14 of 34

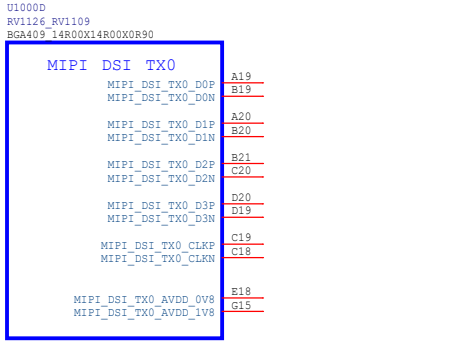
LCDC/RGMII/PWM





BT1120 TX	DATA:LCDC_DATA[15:0] Y[0:7]:LCDC_DATA[8:15] Cb[0:7]:LCDC_DATA[0:7] CLOCK:LCDC_CLK
6bit Serial RGB	DATA:LCDC_DATA[5:0] CLOCK:LCDC_CLK HSYNC:LCDC_HSYNC VSYNC:LCDC_VSYNC DE:LCDC_DEN
8bit Serial RGB	DATA:LCDC_DATA[7:0] CLOCK:LCDC_CLK HSYNC:LCDC_HSYNC VSYNC:LCDC_VSYNC DE:LCDC_DEN
16bit Parallel RGB(RGB656)	R[4:0]:LCDC_DATA[15:11] G[5:0]:LCDC_DATA[10:5] B[4:0]:LCDC_DATA[4:0] CLOCK:LCDC_CLK HSYNC:LCDC_HSYNC VSYNC:LCDC_VSYNC DE:LCDC_DEN
18bit Parallel RGB(RGB666)	R[5:0]:LCDC_DATA[17:12] G[5:0]:LCDC_DATA[11:6] B[5:0]:LCDC_DATA[5:0] CLOCK:LCDC_CLK HSYNC:LCDC_HSYNC VSYNC:LCDC_VSYNC DE:LCDC_DEN
24bit Parallel RGB(RGB888)	R[7:0]:LCDC_DATA[23:16] G[7:0]:LCDC_DATA[15:8] B[7:0]:LCDC_DATA[7:0] CLOCK:LCDC_CLK HSYNC:LCDC_HSYNC VSYNC:LCDC_VSYNC DE:LCDC_DEN

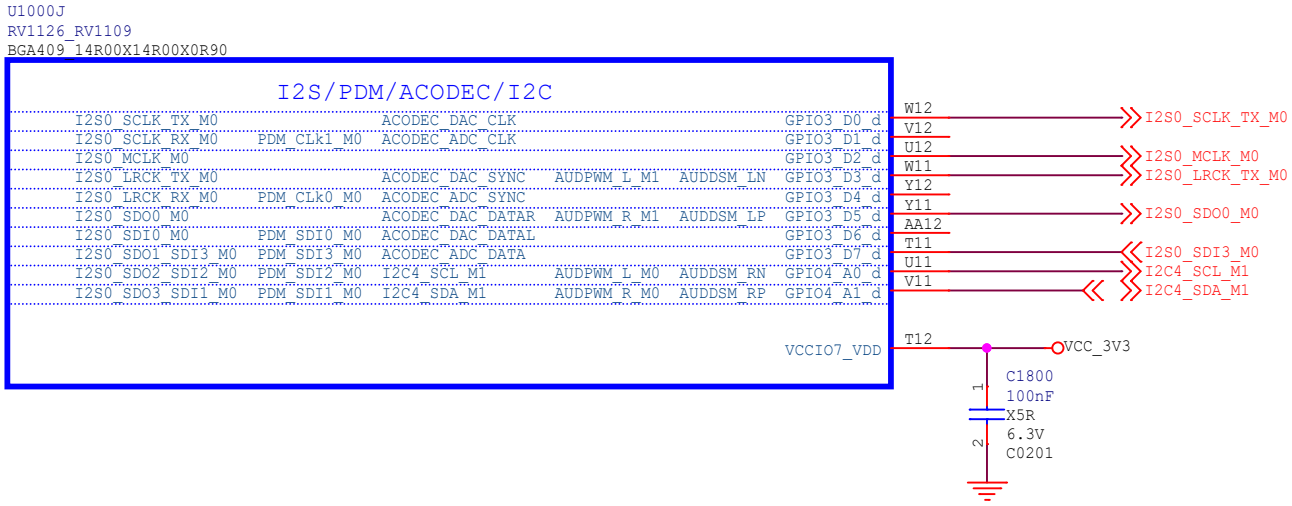
MIPI-DSI Interface



If use MIPI DSI ,E18 connct to VCC_0V8,
G15 connect to VCC_1V8

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	17.RV1126/1109_VideoOutput Interface				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	15 of 34

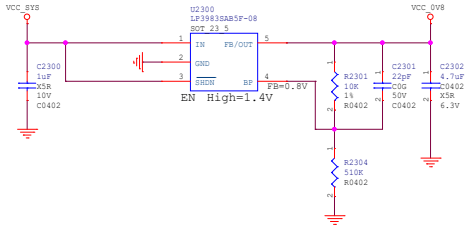
Audio Interface



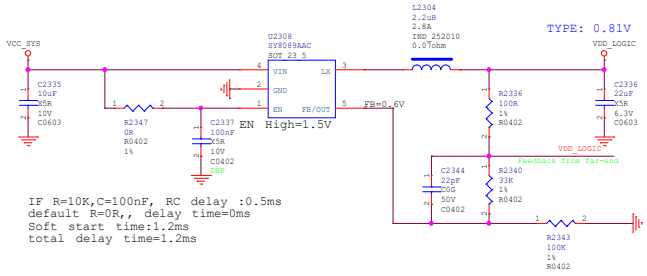
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	18.RV1126/1109_Audio				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	16 of 34

Discrete Power

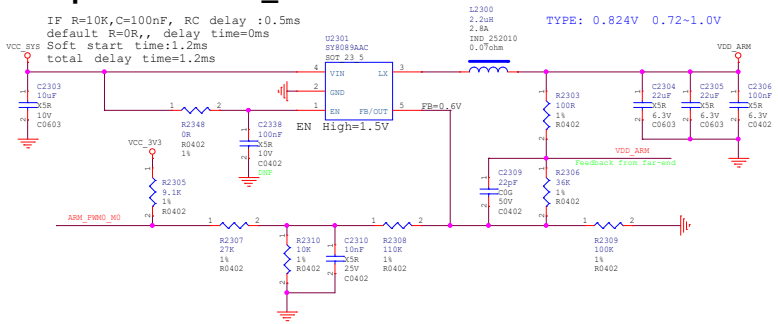
Power Sequence: 1 VCC_0V8



Power Sequence: 2 VDD_LOGIC

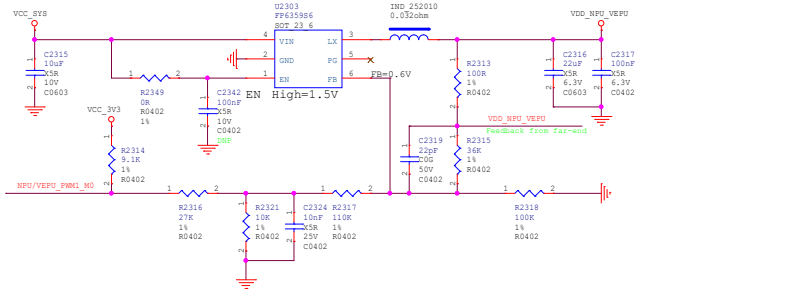


Power Sequence: 2 VDD_ARM

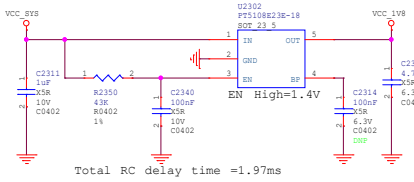


Power Sequence: 2 VDD_NPU_VEPU

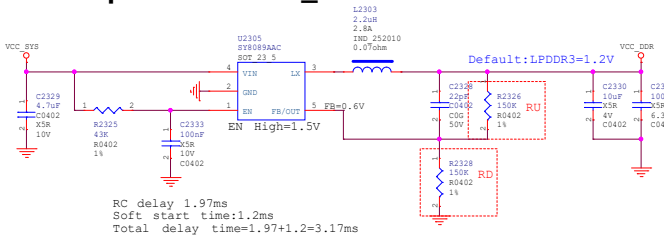
NOTE:
1. The ripple of VPP for NPU_VEPU need to <80mV
FP635986:
1. Load transient is better than some BUCK.
2. 3A Peak load current.



Power Sequence: 3 VCC_1V8

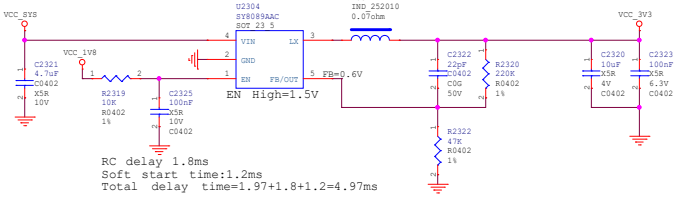


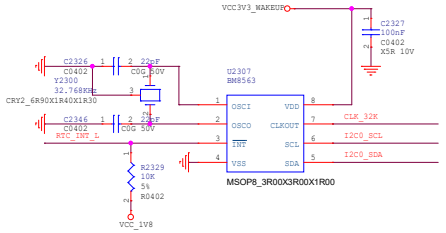
Power Sequence: 4 VCC_DDR

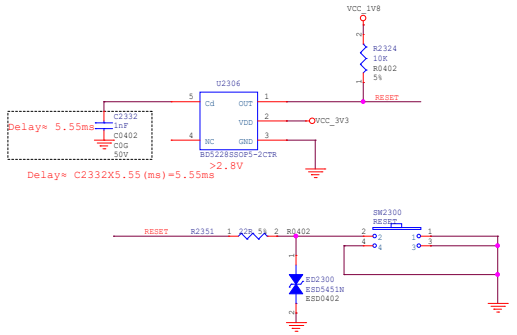


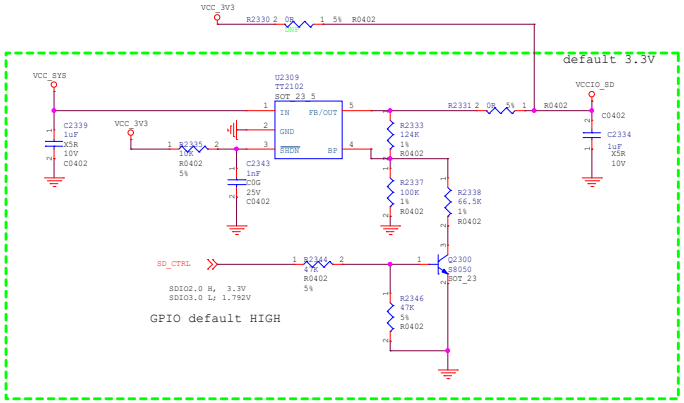
DDR Type	VCC_DDR Voltage	RU	RD
DDR3L	1.35V	150K	120K
DDR3	1.5V	150K	100K
DDR4	1.2V	150K	150K
LPDDR3	1.2V	150K	150K
LPDDR4	1.1V	150K	180K

Power Sequence: 5 VCC_3V3









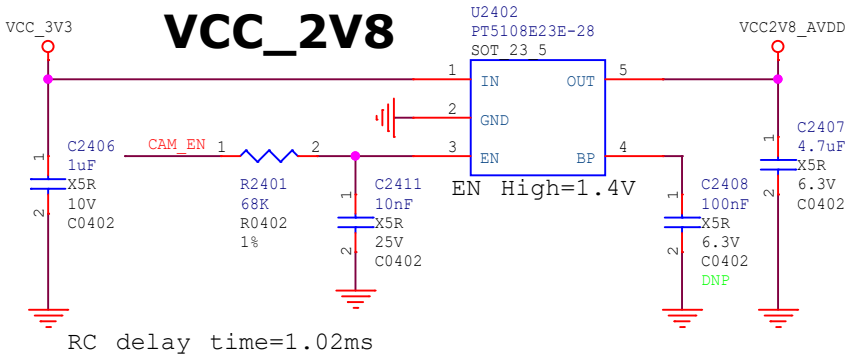
Rockchip Electronics Co., Ltd			
Project:	RV1126_RV1109_REF		
File:	23.Discrete Power for System		
Date:	Wednesday, July 15, 2020	Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>
		Sheet:	17 of 34

Discrete Power for Camera

CAM_EN

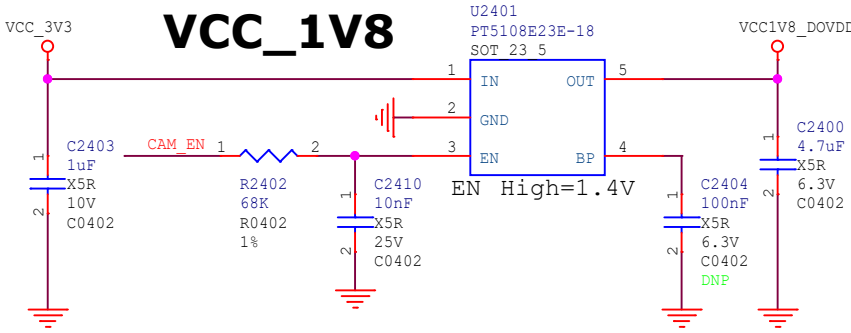
NOTE:
The power on sequence is adjusted according to the camera.

VCC_2V8



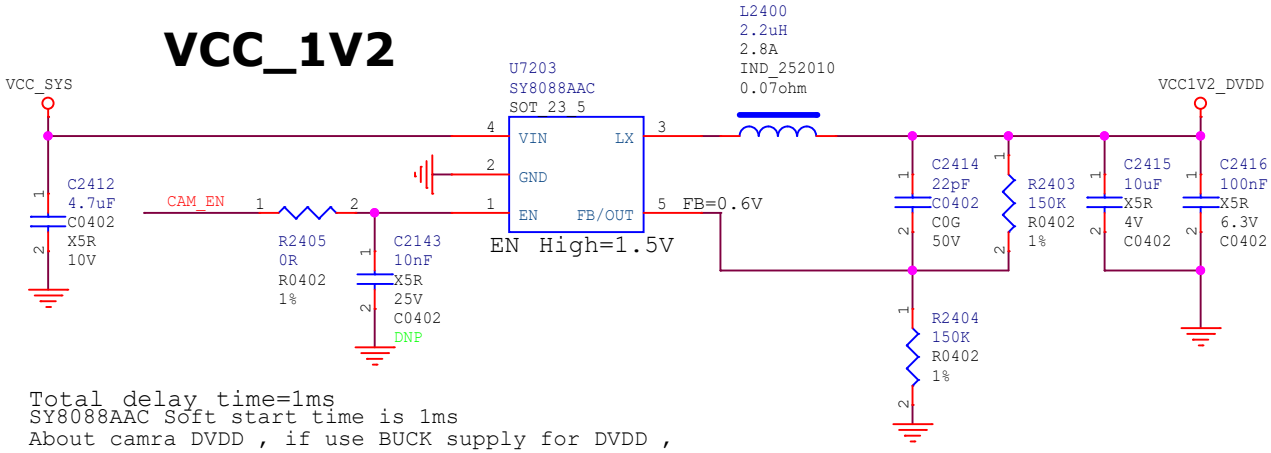
RC delay time=1.02ms

VCC_1V8



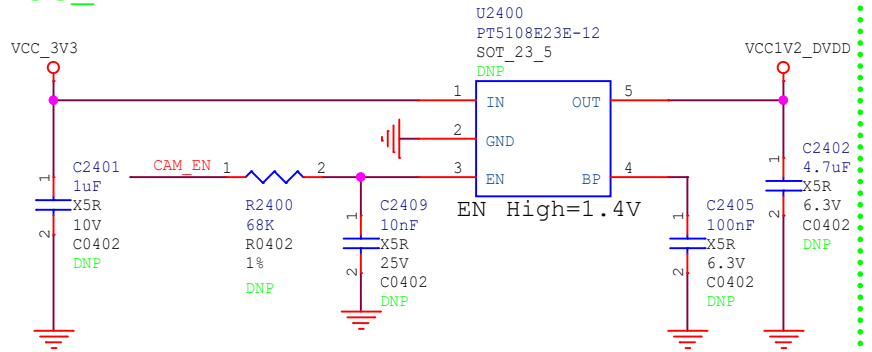
RC delay time=1.02ms

VCC_1V2



Total delay time=1ms
SY8088AAC Soft start time is 1ms
About camra DVDD , if use BUCK supply for DVDD ,
it will cost less power consumption.

Option: VCC_1V2

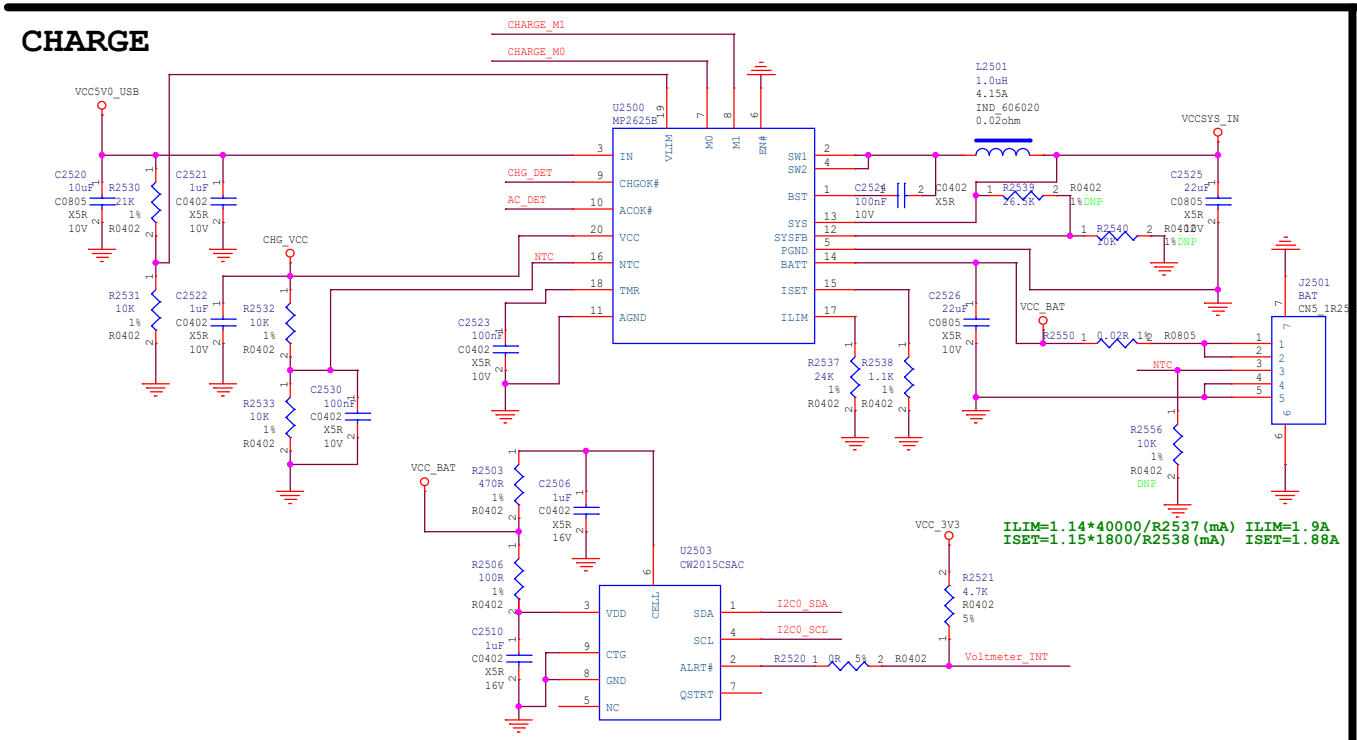


RC delay time=1.02ms

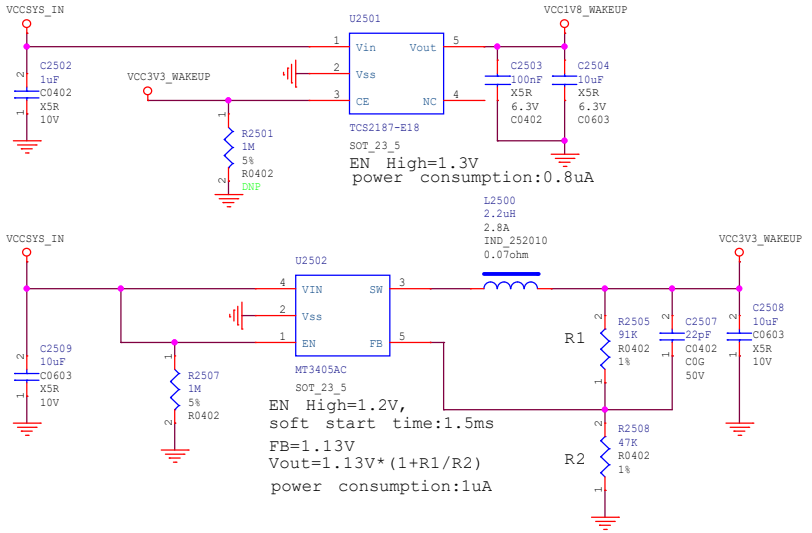
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	24.Discrete Power for Camera				
Date:	Wednesday, July 15, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	18 of 34

Wake up Power

CHARGE

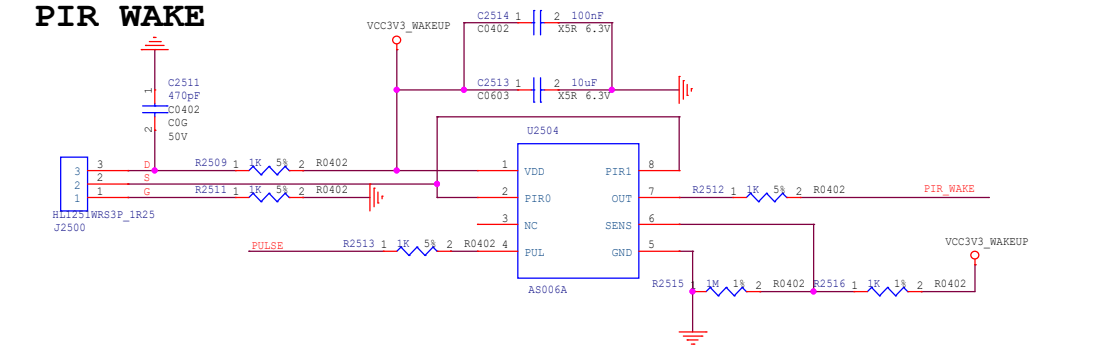


Power always on

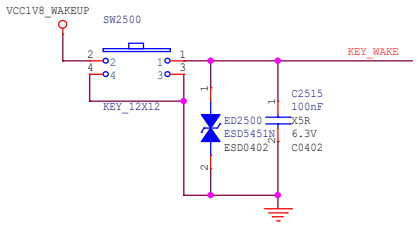


power on sequence of WIFI AP6201BM/AP6203BM: 3V3--->1V8

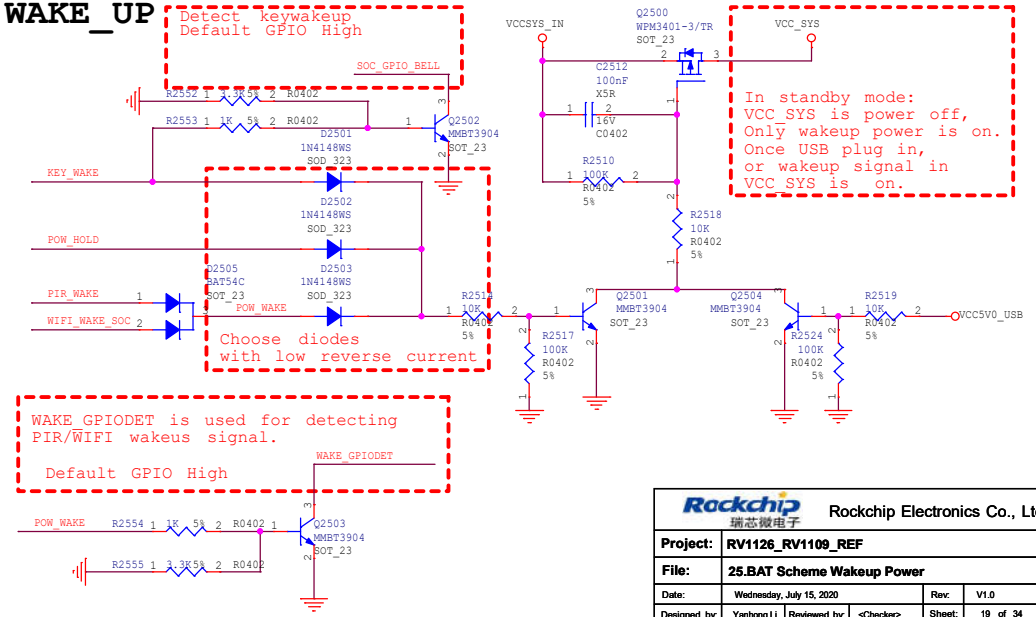
PIR WAKE



KEY WAKE



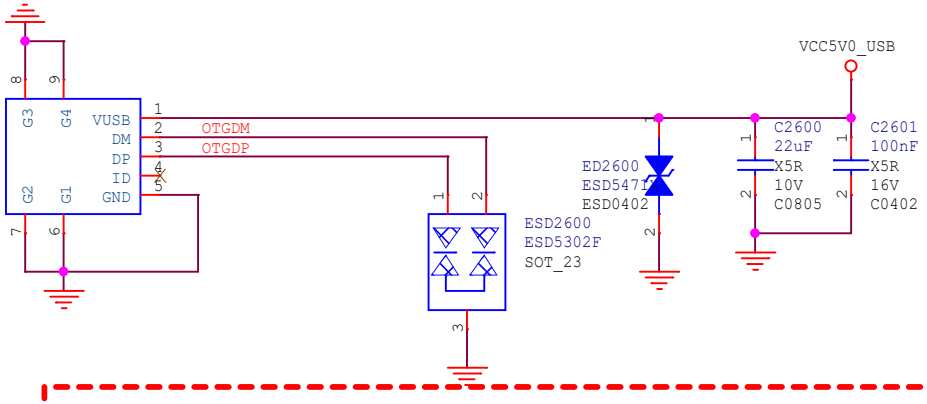
WAKE_UP

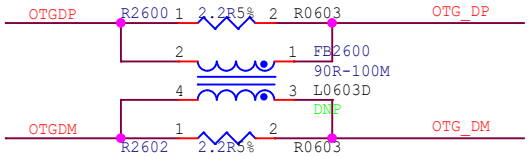


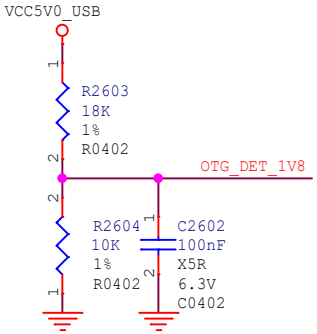
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	25.BAT Scheme Wakeup Power				
Date:	Wednesday, July 15, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	19 of 34

USB2.0 OTG

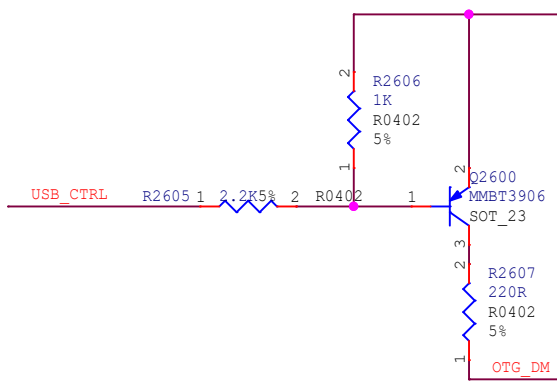
J2600
USB20_micro
USB20Micro5_MU05_10MGF_T

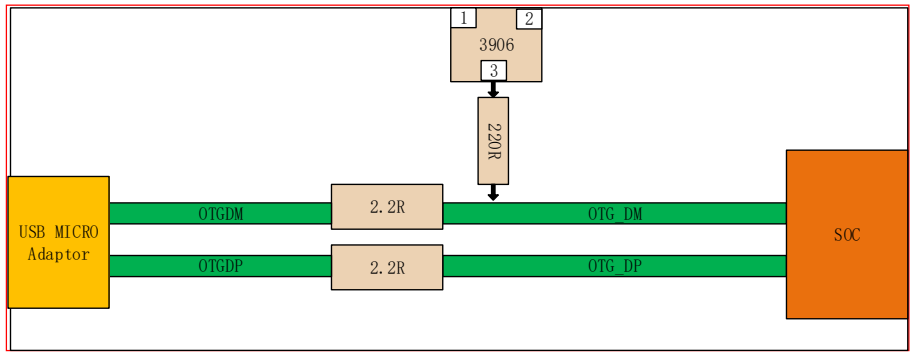






This circuit is used to improve usb compatibility.
Note:
These components are close to R2602 to avoid long branches.

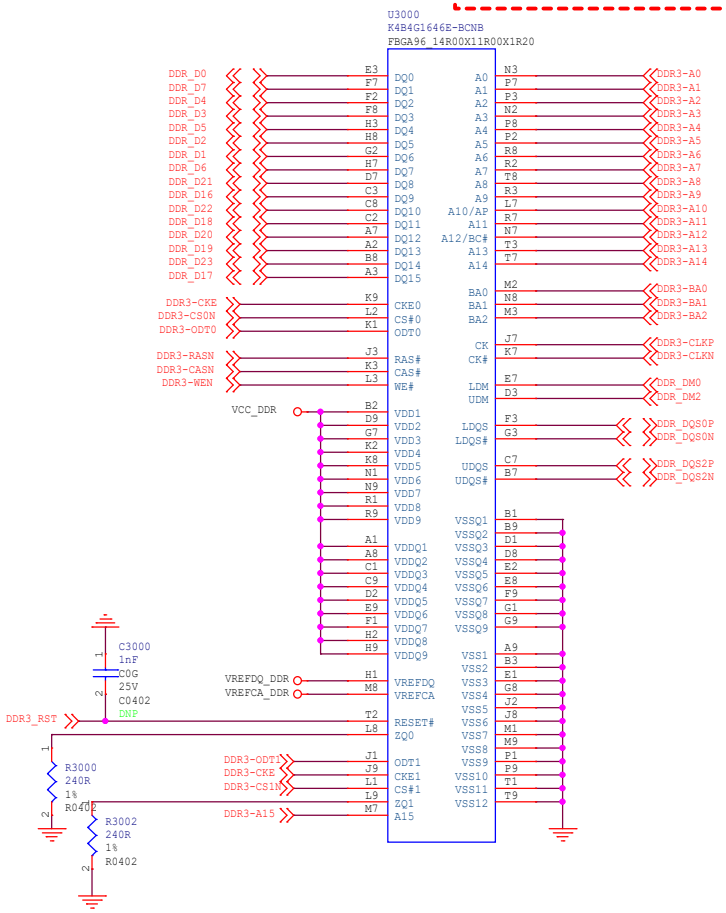


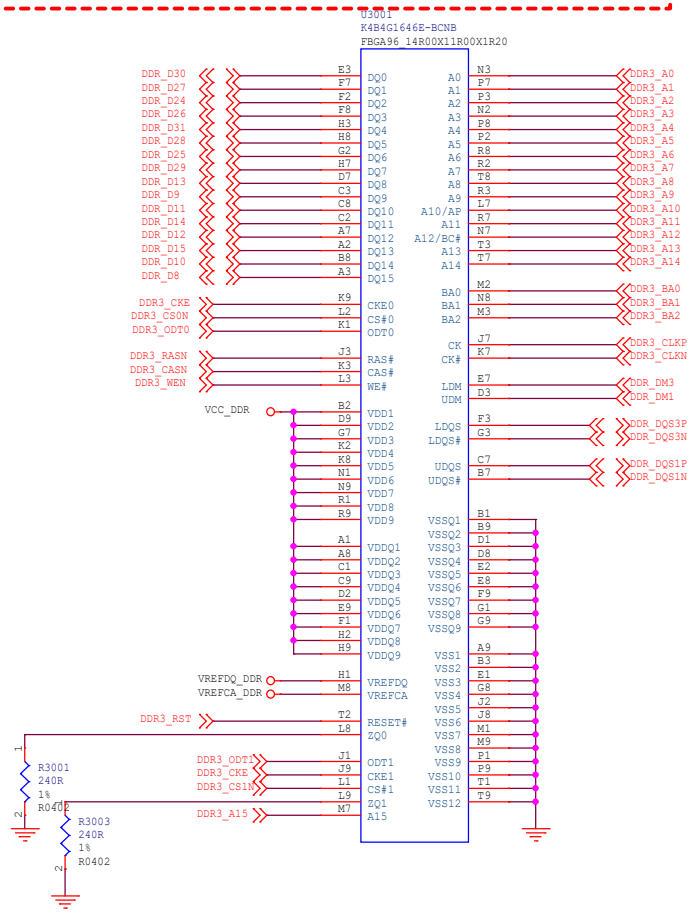


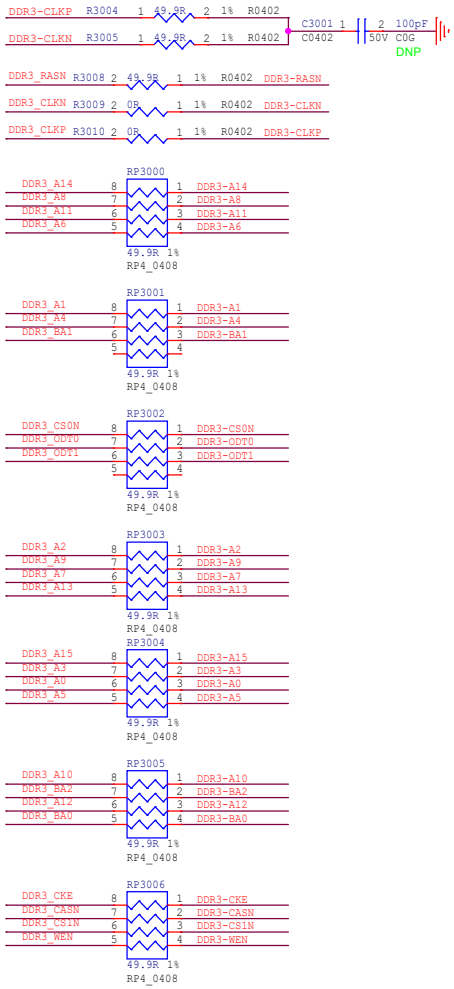
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	26.USB OTG				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	20 of 34

DDR3/DDR3L 2x16bit

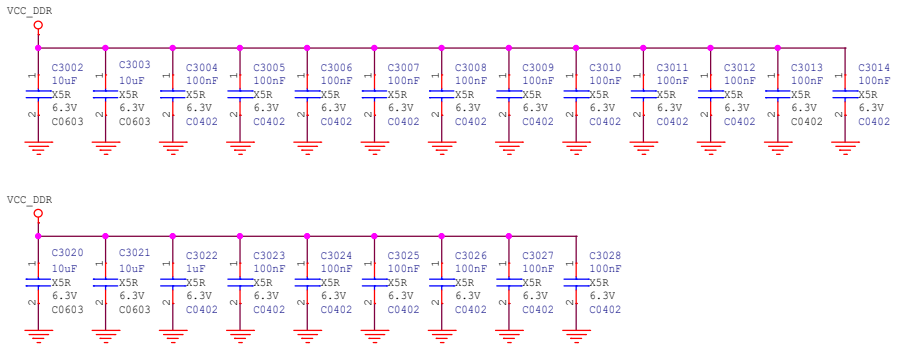
Note:
This is DDR template<RV1126_RV1109_Template_DDR3P216SD4_V10_20200619>. 4 layers PCB.
If only need one pcs DDR, please must use U3000(lane0,lane2).
If need other template, please apply to RK.

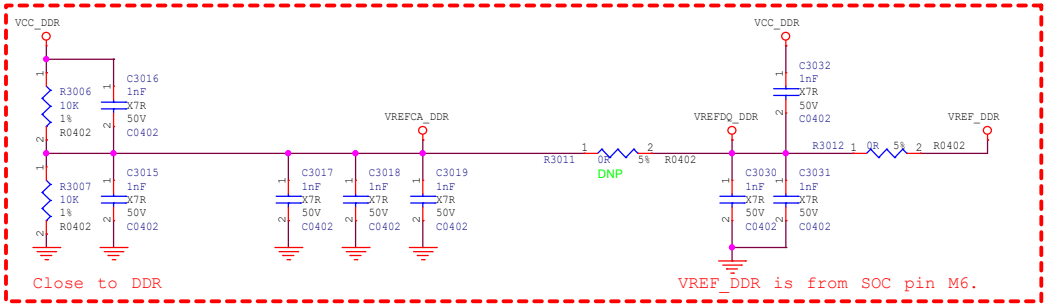






Note:All the Power filter capacitors should be placed close to the power pins of DDR3





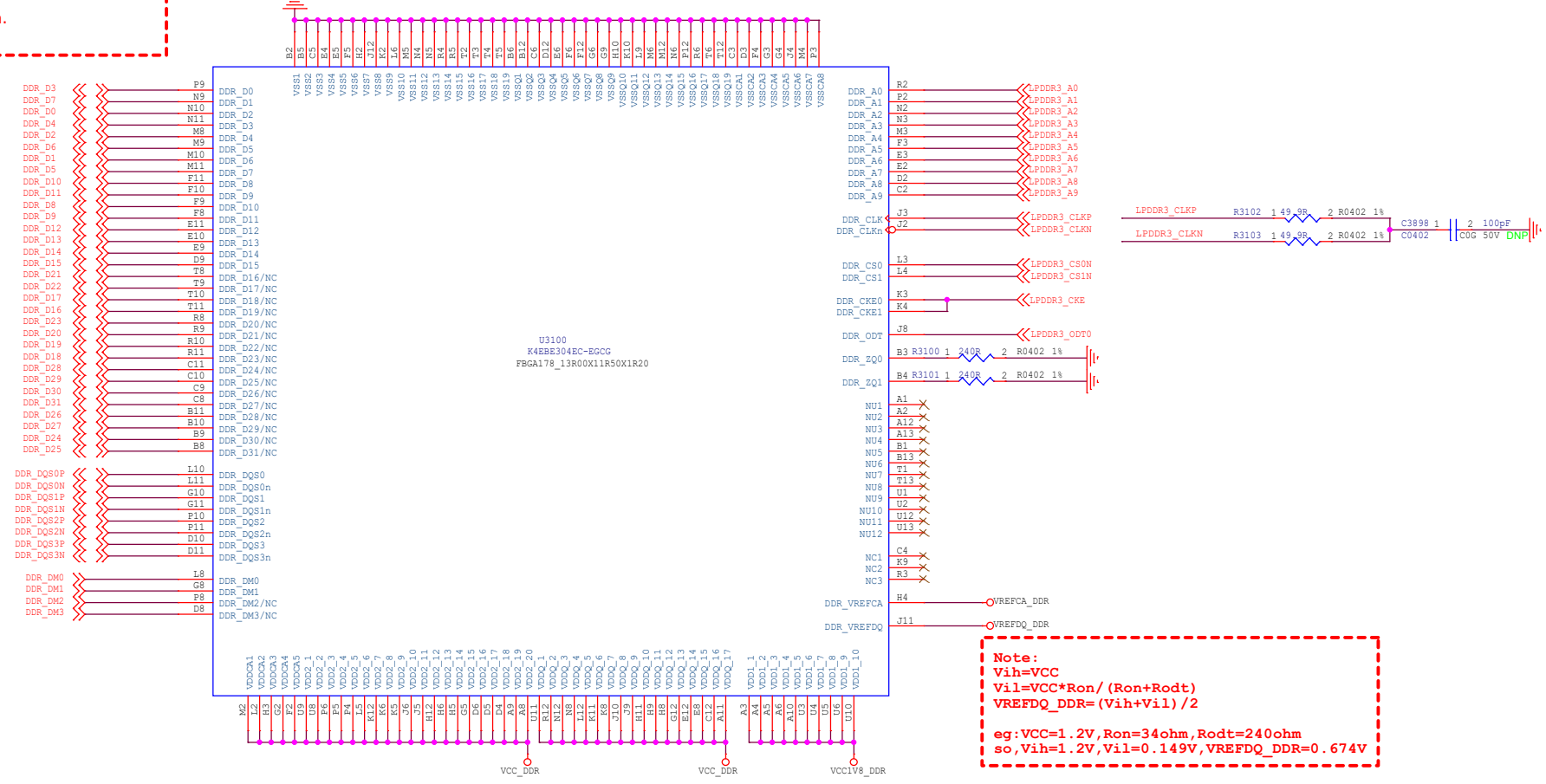
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	30.DRAM_DDR3_96P_2X16bit				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	21 of 34

LPDDR3 1x32bit

NOTE:
The sequence of DQ shall be done according to the template and shall not be adjusted or changed

Refer to the latest AVL for parts selection.

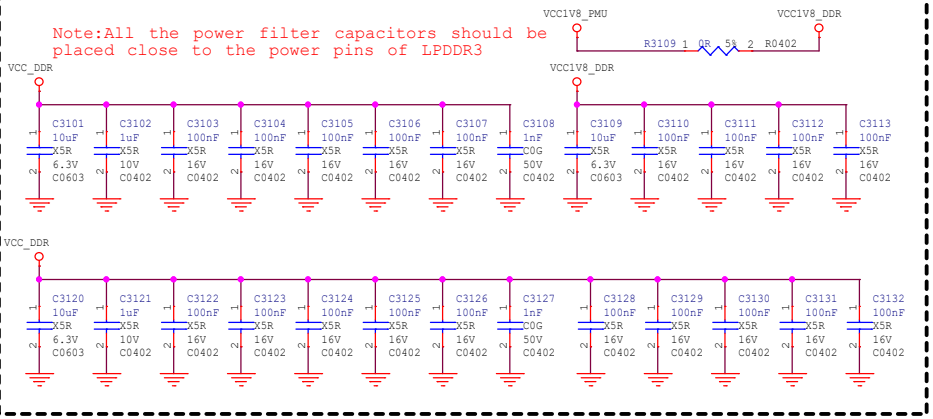
Note:
This is DDR template<RV1126_RV1109_Template_LP3S178P132SD6_V10_20200325>. Six layers PCB.

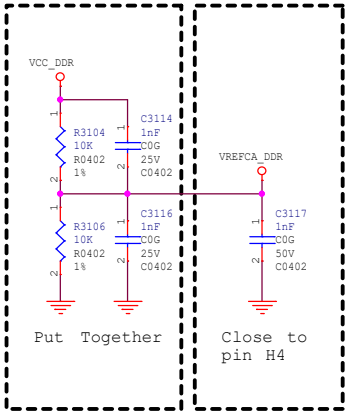


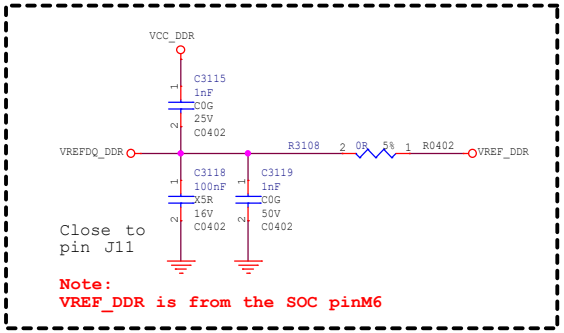
Note:
Vih=VCC
Vil=VCC*Ron/(Ron+Rodt)
VREFDQ_DDR=(Vih+Vil)/2

eg:VCC=1.2V,Ron=34ohm,Rodt=240ohm
so,Vih=1.2V,Vil=0.149V,VREFDQ_DDR=0.674V

Note:All the power filter capacitors should be placed close to the power pins of LPDDR3





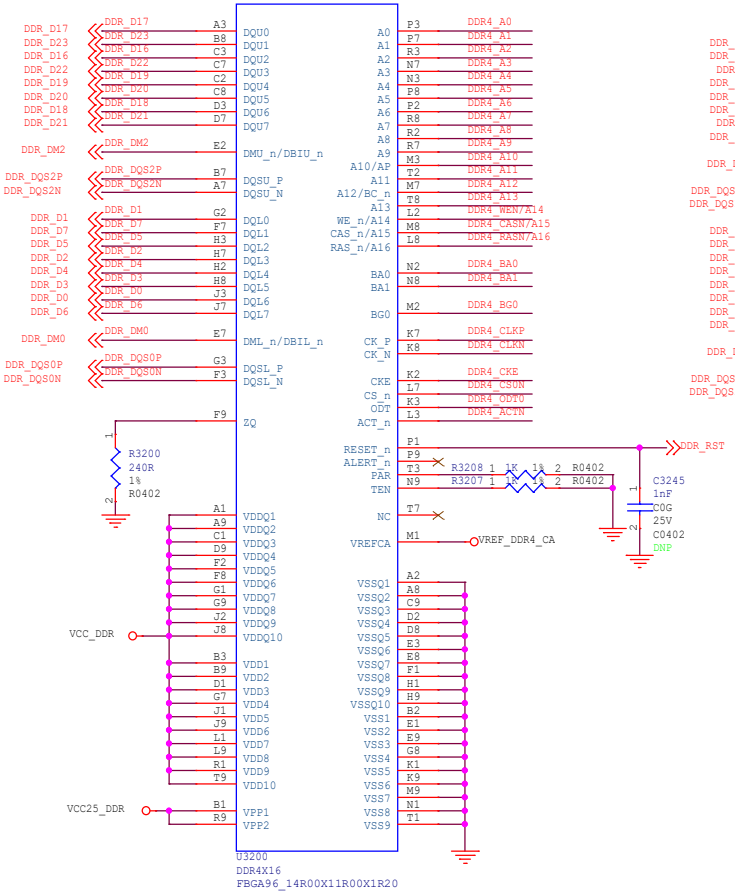


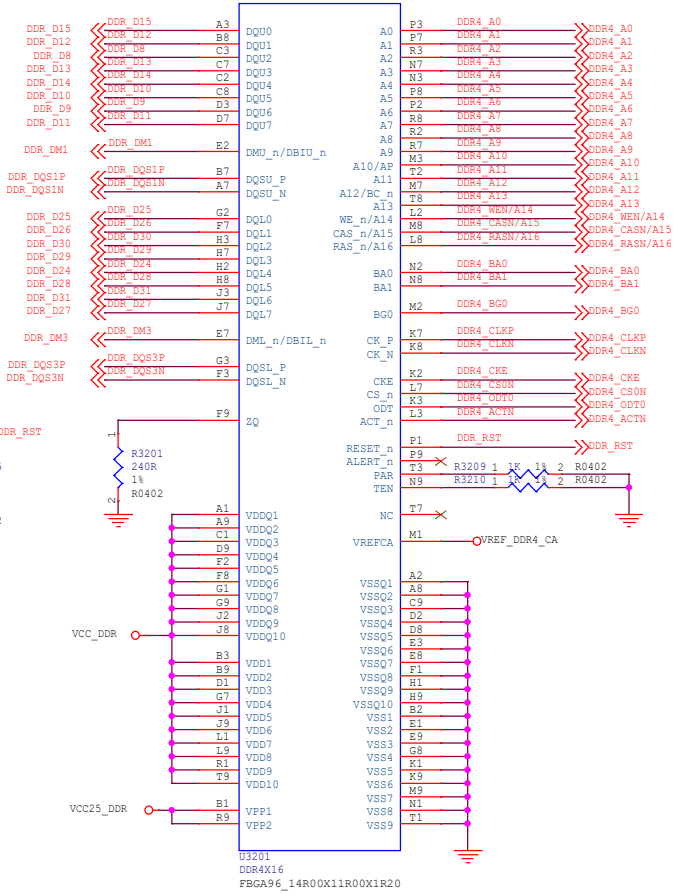
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	31. DRAM_LPDDR3_32 bit				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	22 of 34

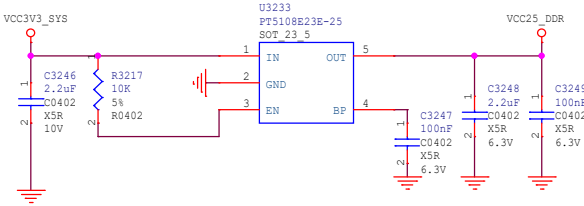
DDR4 2x16bit

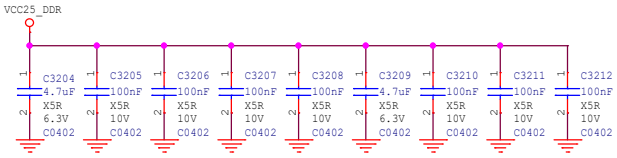
NOTE:
The sequence of DQ shall be done according to the template and shall not be adjusted or changed
Refer to the latest AVL for parts selection.

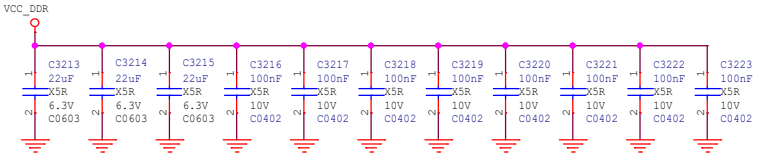
Note:
This is DDR template<RV1126_RV1109_Template_DDR4P216DD6_V10_20200325>.Six layers PCB.
If only need one pcs DDR, please must use U3200(lane0,lane2).

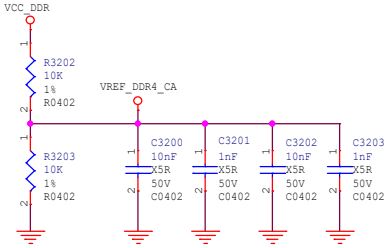


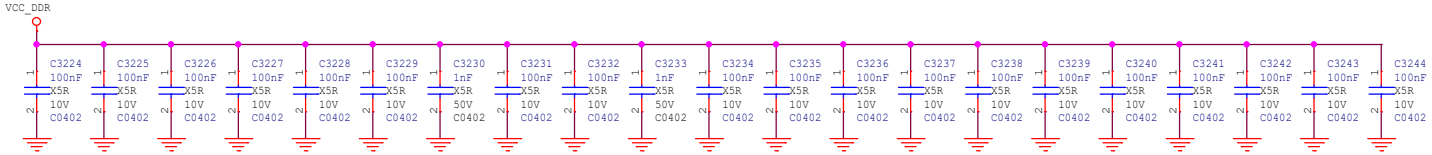










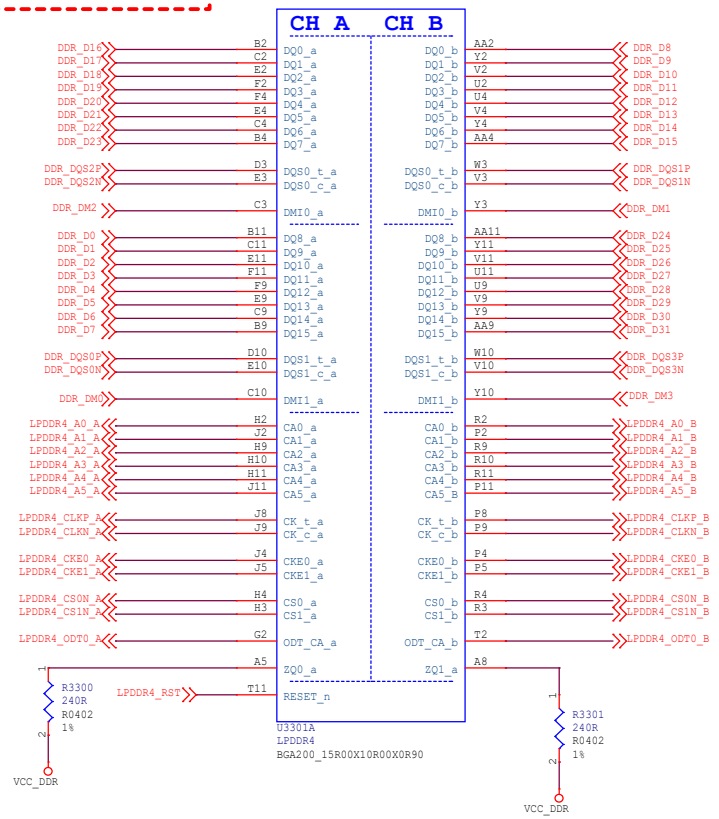


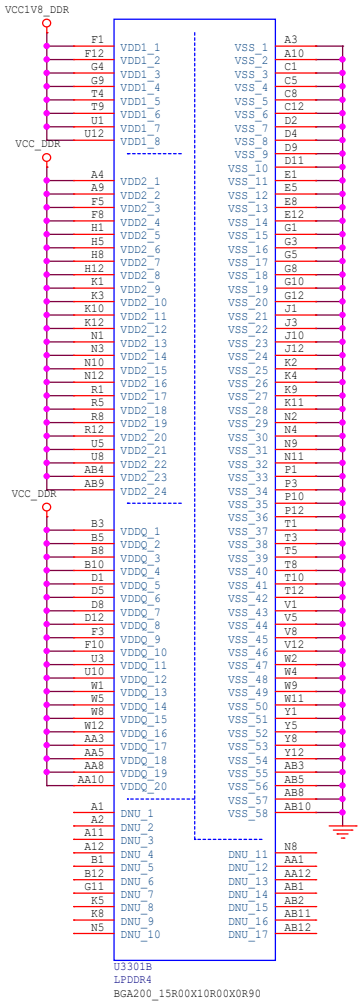
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	31. DRAM_LPDDR3_32 bit				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	23 of 34

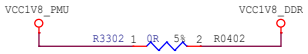
LPDDR4 1x32bit

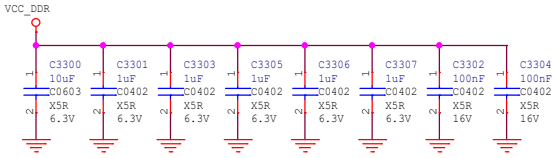
NOTE:
The sequence of DQ shall be done according to the template and shall not be adjusted or changed
Refer to the latest AVL for parts selection.

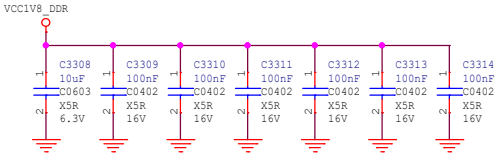
Note:
This is DDR template<RV1126_RV1109_Template_LP4S200P132SD6>. Six layers PCB.
If only need one pcs DDR, please must use U3200(lane0,lane2).

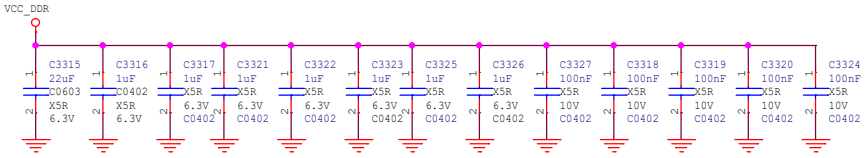








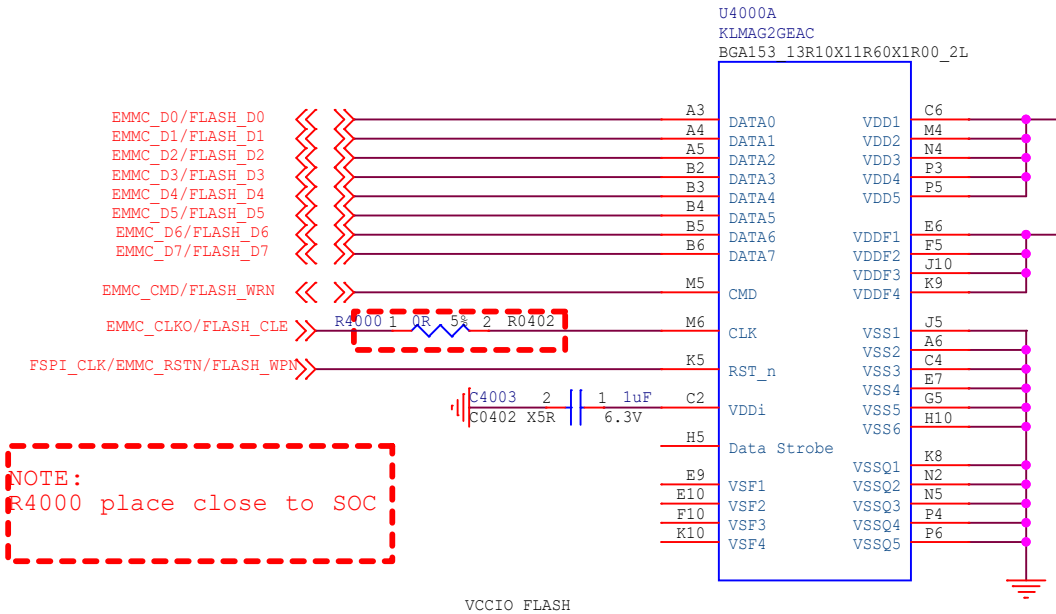




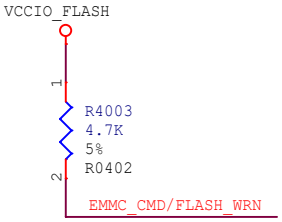
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	33.DRAM_LPDDR4_32 bit				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	24 of 34

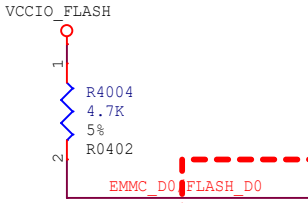
eMMC

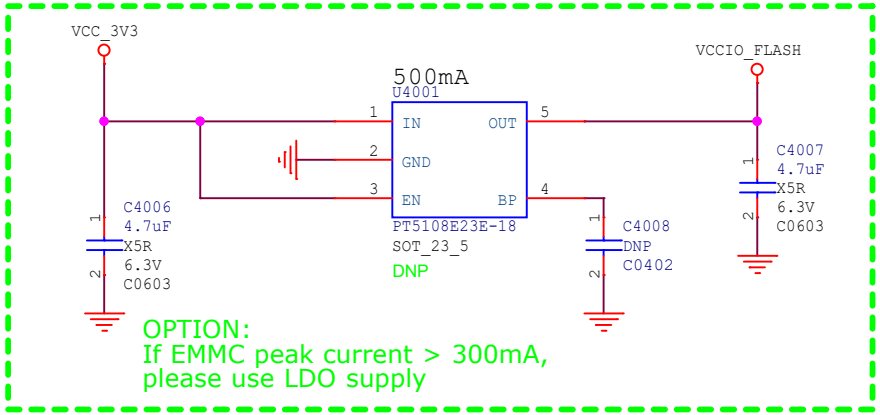
NOTE:
Refer to the latest AVL for parts selection.
NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.

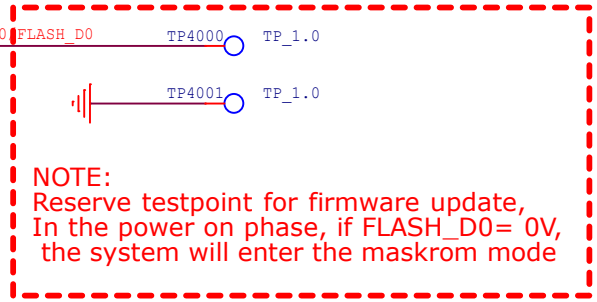


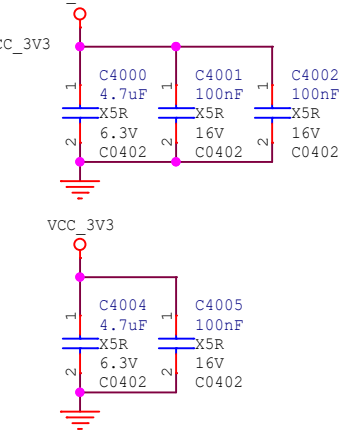
NOTE:
R4000 place close to SOC

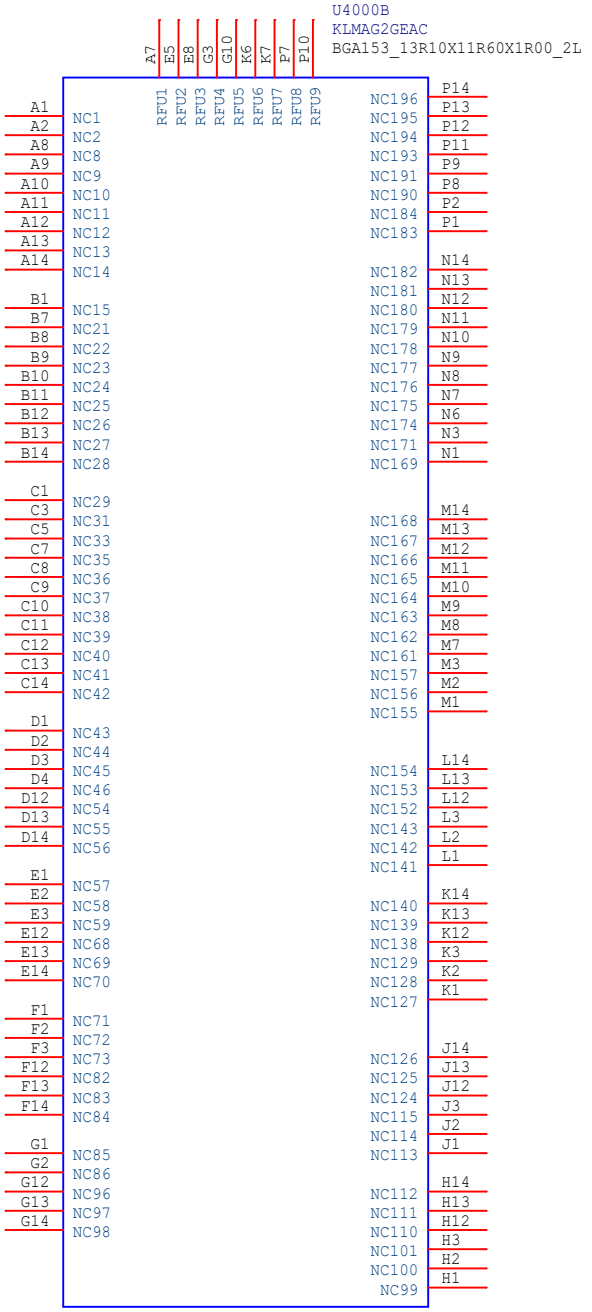








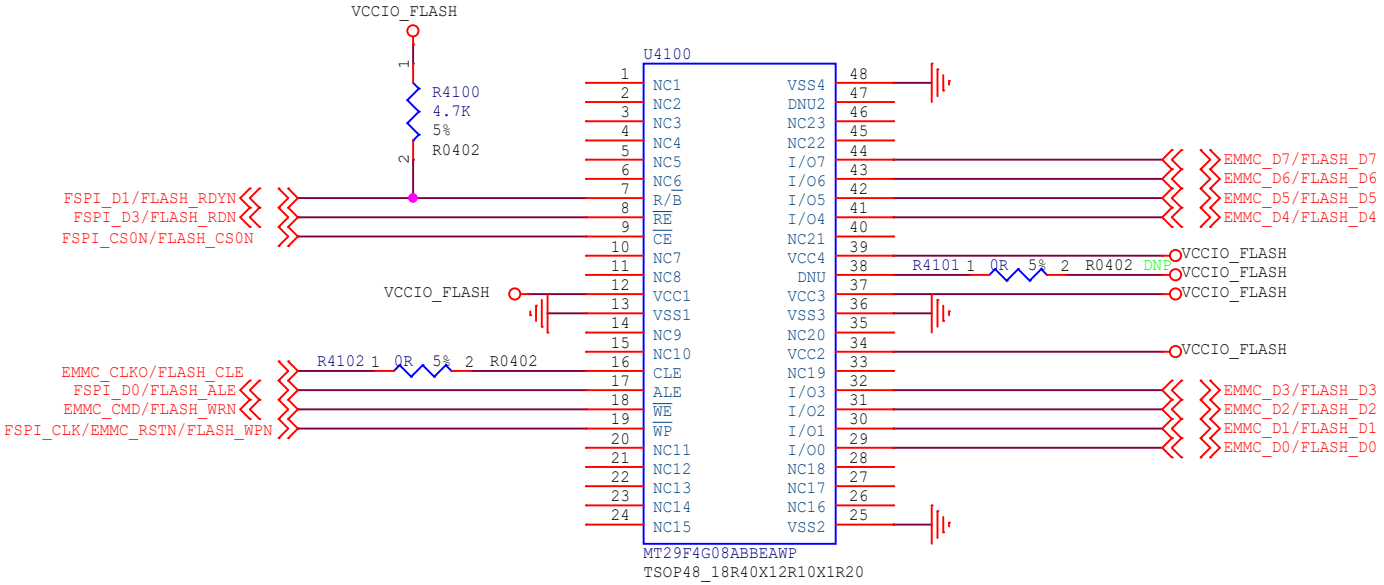


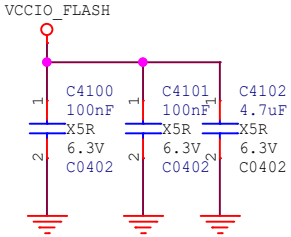


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	40.Flash-eMMC Flash				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	25 of 34

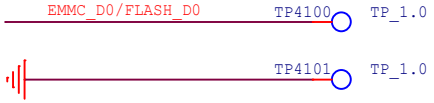
NAND FLASH

NOTE:
Refer to the latest AVL for parts selection.
Only support SLC NAND





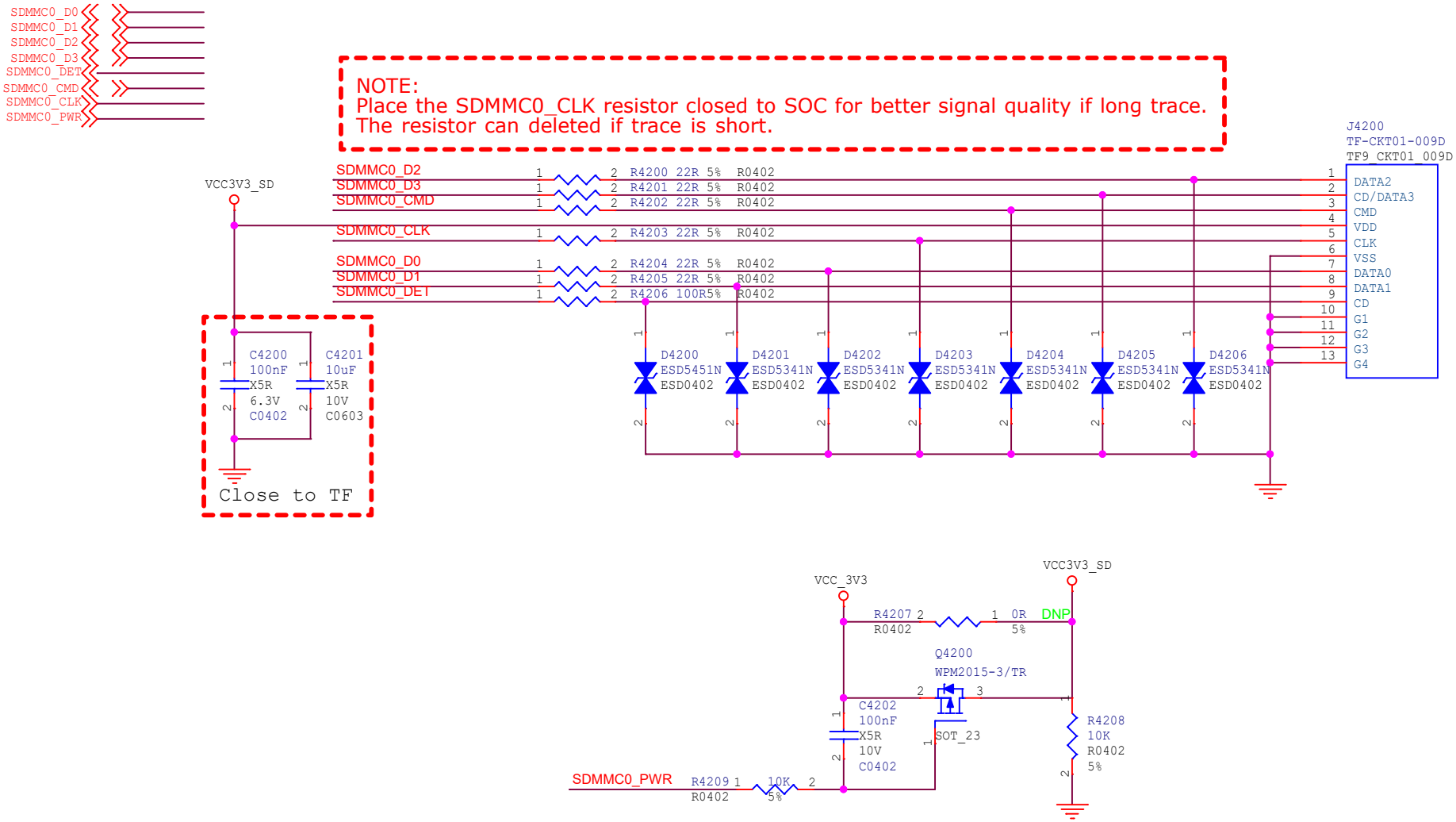
NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.



NOTE:
Reserve testpoint for firmware update,
In the power on phase, if FLASH_D0= 0V,
the system will enter the maskROM mode

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	41.Flash-Nand Flash				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	26 of 34

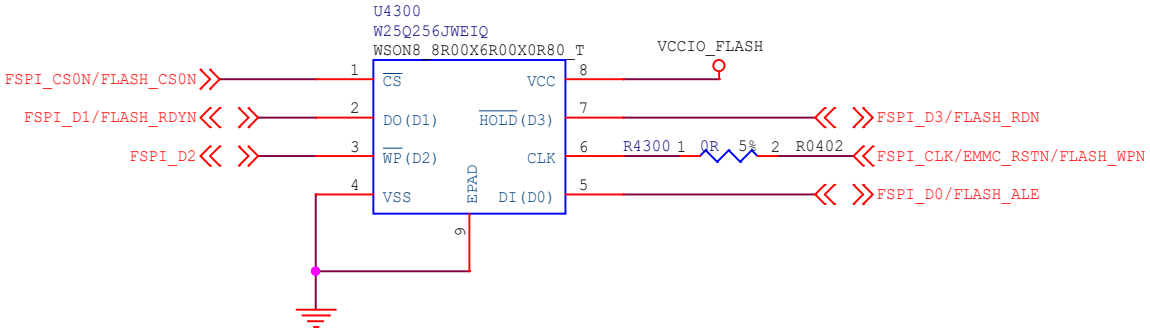
TF CARD

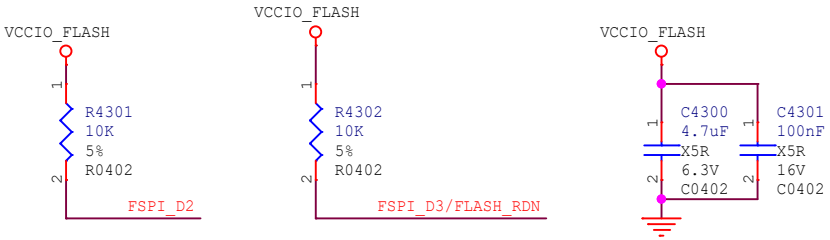


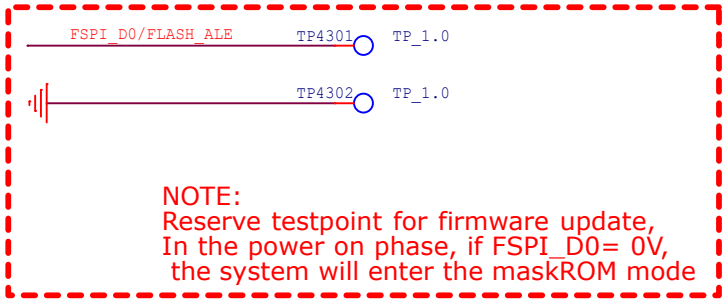
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	42.Flash-Micro-SD Card				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	27 of 34

SPI_Flash

NOTE:
Refer to the latest AVL for parts selection.

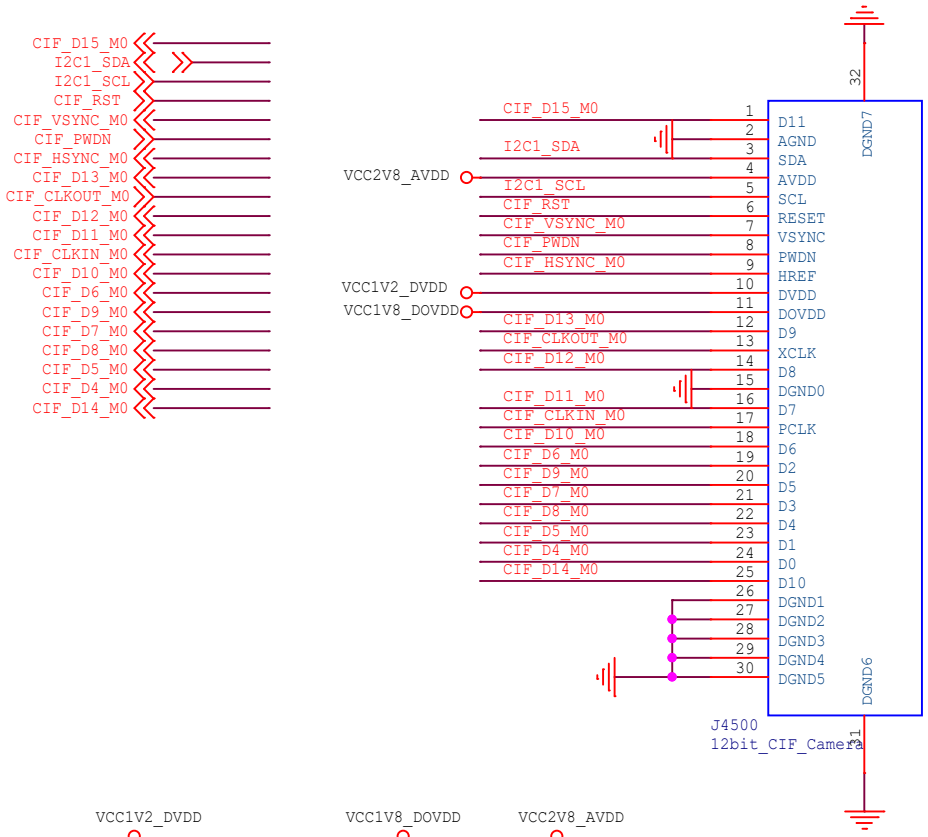






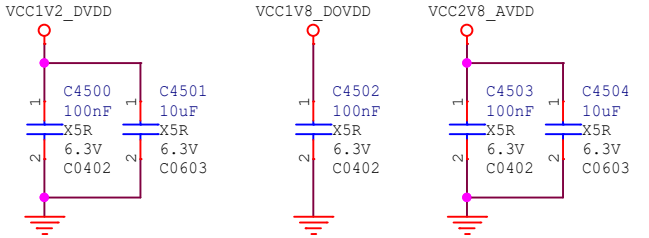
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	43.Flash-SPI Flash				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	28 of 34

CIF Camera Interface

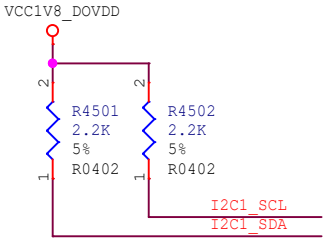


Correspondence CIF data and BT1120/12bit/10bit/8bit CIF				
16bit CIF data	BT1120	12bit CIF camera	10bit CIF camera	8bit CIF camera
CIF_D0	BT1120_D0			
CIF_D1	BT1120_D1			
CIF_D2	BT1120_D2			
CIF_D3	BT1120_D3			
CIF_D4	BT1120_D4	D0		
CIF_D5	BT1120_D5	D1		
CIF_D6	BT1120_D6	D2	D0	
CIF_D7	BT1120_D7	D3	D1	
CIF_D8	BT1120_D8	D4	D2	D0
CIF_D9	BT1120_D9	D5	D3	D1
CIF_D10	BT1120_D10	D6	D4	D2
CIF_D11	BT1120_D11	D7	D5	D3
CIF_D12	BT1120_D12	D8	D6	D4
CIF_D13	BT1120_D13	D9	D7	D5
CIF_D14	BT1120_D14	D10	D8	D6
CIF_D15	BT1120_D15	D11	D9	D7

NOTE:
According to the current of the actual camera module, evaluate whether the current output by LDO can meet the requirement of two cameras using at the same time. If not, please add LDO to supply power



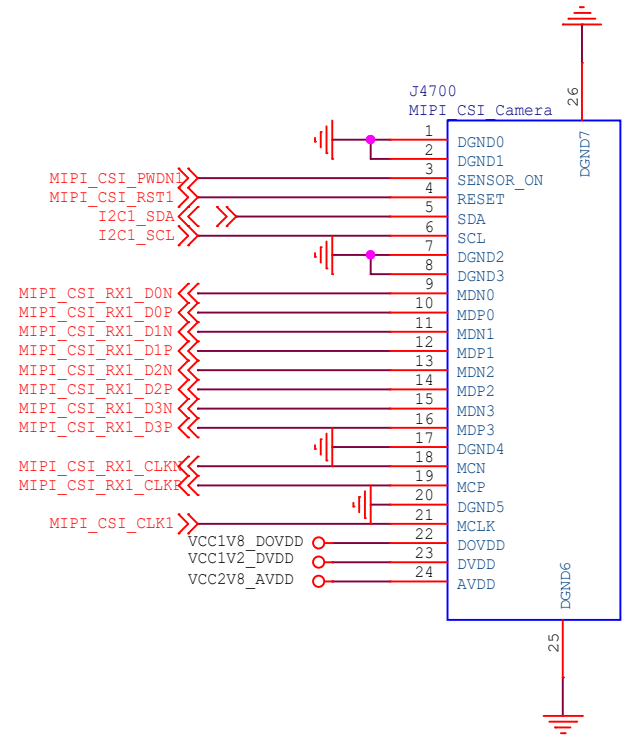
NOTE:
There is also a group of pull-up for I2C1 on page 47. Select one group.



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	45.VI-Camera_CIF				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	29 of 34

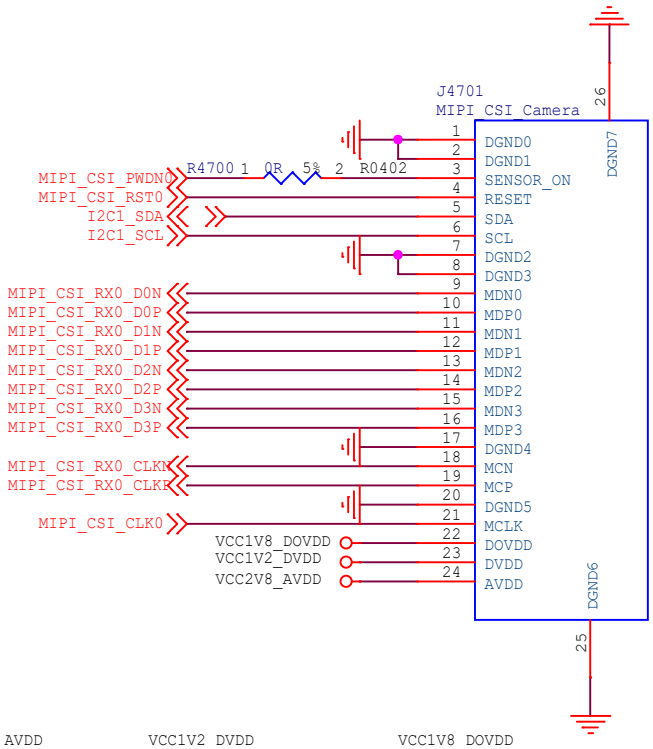
DEFAULT: MIPI_CSI Interface
LVDS interface and mipicsi interface share pins,
only one of them can be selected at the same time.

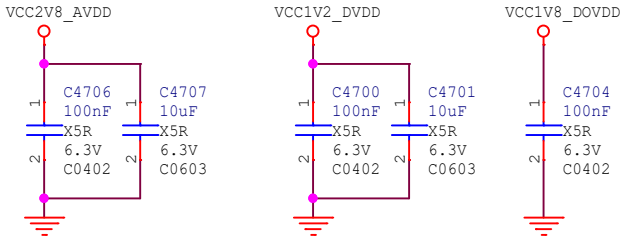
MIPI-CSI_RX1 Interface

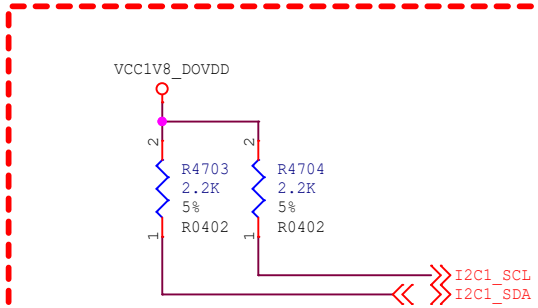


NOTE:
1. According to the current of the actual camera module, evaluate whether the current output by LDO can meet the requirement of two cameras using at the same time.
2.If not, please add LDO to supply power.
3. If the I2C addresses of the two cameras are the same, use another set of I2C.
4.LVDS RX interfaces are pin to pin with MIPI_CSI_RX

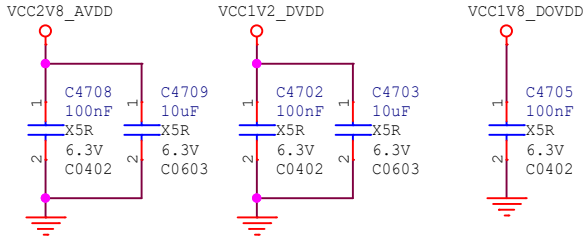
MIPI-CSI_RX0 Interface



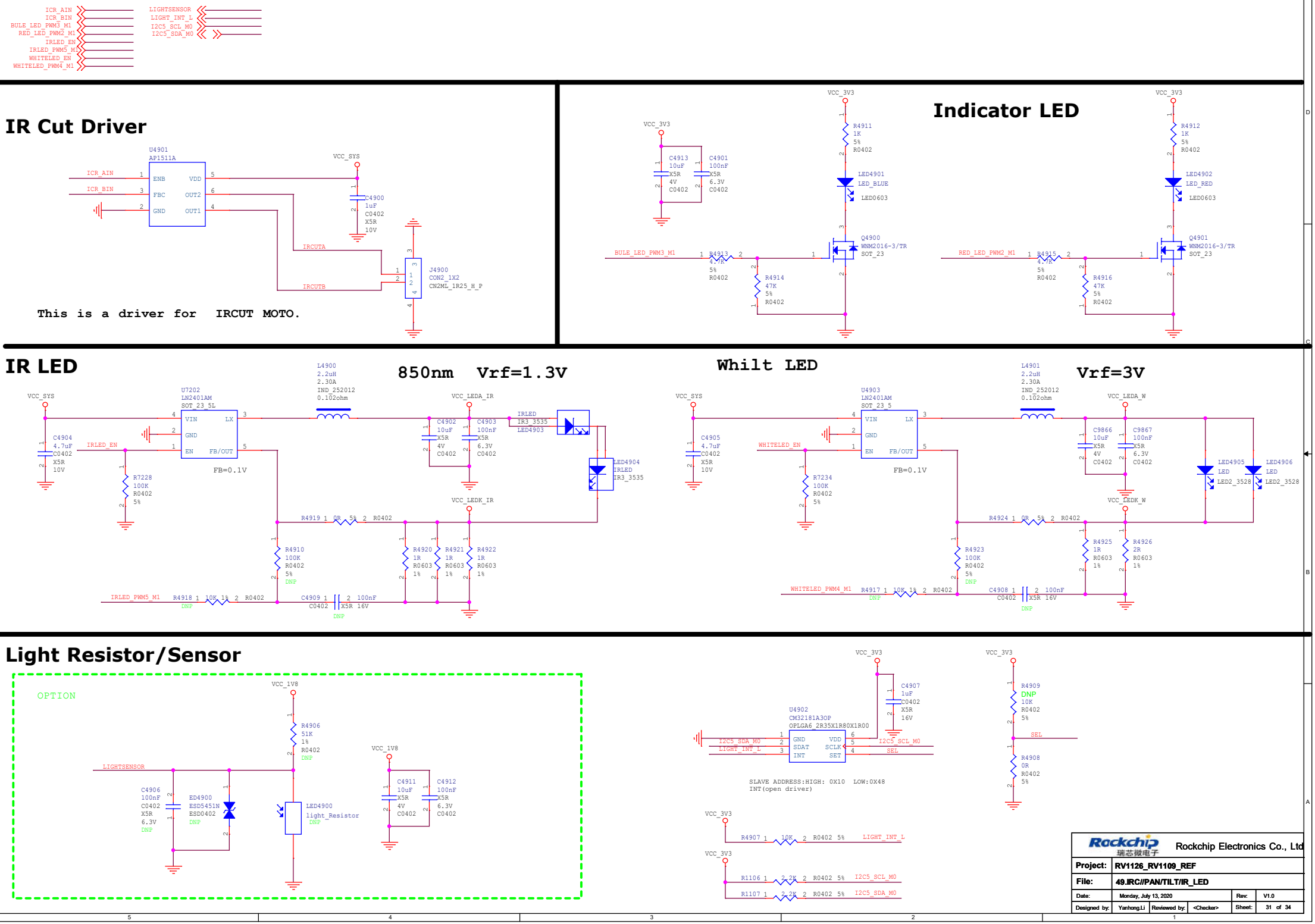




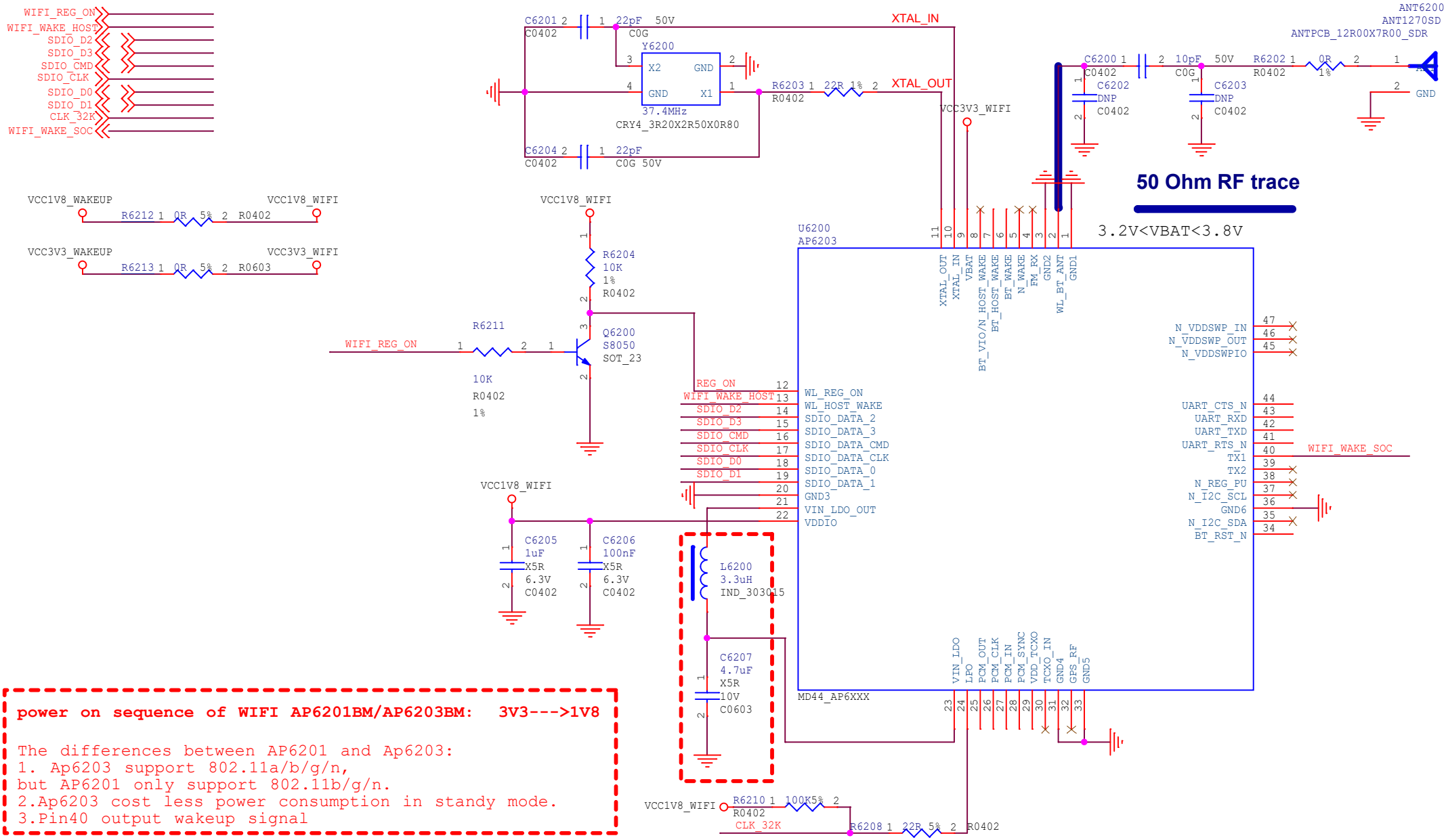
NOTE:
There is also a group of pull-up for I2C1 on page 45.
Select one group.



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	47.VI-Camera_MIPI-CSI				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	30 of 34


ICR_AIN
ICR_BIN
BULE_LED_PWM3_M1
RED_LED_PWM2_M1
IRLED_EN
IRLED_PWM5_M1
WHITELED_EN
WHITELED_PWM4_M1
LIGHTSENSOR
LIGHT_INT_L
I2C5_SCL_M0
I2C5_SDA_M0
IR Cut Driver
U4901
AP1511A
ENB
FBC
GND
VDD
OUT2
OUT1
VCC_SYS
C4900
1uF
C0402
X5R
10V
IRCUTA
IRCUTB
J4900
CON2_1X2
CN2ML_1R25_H_P
This is a driver for IRCUT MOTO.
Indicator LED
VCC_3V3
C4913
10uF
X5R
4V
C0402
C4901
100nF
X5R
6.3V
C0402
R4911
1K
5%
R0402
LED4901
LED_BLUE
LED0603
Q4900
WNM2016-3/TR
SOT_23
BULE_LED_PWM3_M1
R4913
4.7K
R4914
47K
R4912
LED4902
LED_RED
Q4901
RED_LED_PWM2_M1
R4915
R4916
IR LED
850nm Vrf=1.3V
L4900
2.2uH
2.30A
IND_252012
0.102ohm
U7202
LN2401AM
SOT_23_5L
VIN
LX
GND
EN
FB/OUT
FB=0.1V
VCC_LEDA_IR
VCC_LEDK_IR
C4902
10uF
C4903
100nF
C4904
4.7uF
IRLED_EN
R7228
100K
IRLED
IR3_3535
LED4903
LED4904
R4919
0R
R4910
R4920
R4921
R4922
1R
R0603
1%
IRLED_PWM5_M1
R4918
10K
C4909
DNP
Whilt LED
Vrf=3V
L4901
U4903
LN2401AM
SOT_23_5
C4905
WHITELED_EN
R7234
VCC_LEDA_W
VCC_LEDK_W
C9866
C9867
LED4905
LED4906
LED
LED2_3528
R4924
R4923
R4925
R4926
WHITELED_PWM4_M1
R4917
C4908
Light Resistor/Sensor
OPTION
VCC_1V8
R4906
51K
LIGHTSENSOR
C4906
ED4900
ESD5451N
ESD0402
LED4900
light_Resistor
C4911
C4912
U4902
CM32181A3OP
OPLGA6_2R35X1R80X1R00
GND
SDAT
INT
VDD
SCLK
SET
C4907
SEL
R4909
R4908
SLAVE ADDRESS:HIGH: 0X10 LOW:0X48
INT(open driver)
R4907
LIGHT_INT_L
R1106
2.2K
R1107
Rockchip
瑞芯微电子
Rockchip Electronics Co., Ltd
Project: RV1126_RV1109_REF
File: 49.IRC//PAN/TILT/IR_LED
Date: Monday, July 13, 2020
Rev: V1.0
Designed by: Yanhong.Li
Reviewed by: <Checker>
Sheet: 31 of 34

Battery Solution: WIFI Module wake up



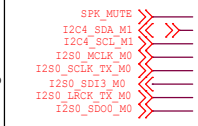
power on sequence of WIFI AP6201BM/AP6203BM: 3V3--->1V8

The differences between AP6201 and Ap6203:
1. Ap6203 support 802.11a/b/g/n,
but AP6201 only support 802.11b/g/n.
2.Ap6203 cost less power consumption in standy mode.
3.Pin40 output wakeup signal

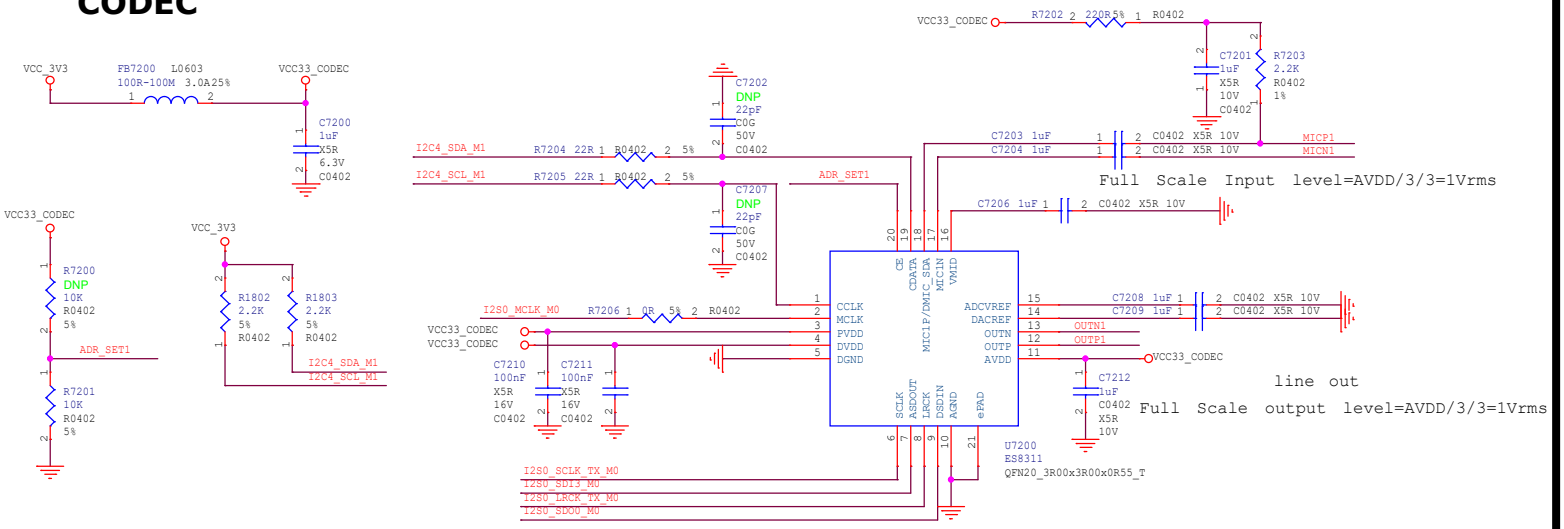
WIFI module		Crystal
AP6201	1T1R802.11b/g/n WIFI+BT5.0	37.4MHz
AP6203	1T1R802.11a/b/g/n WIFI+BT5.0	37.4MHz

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	62.WIFI Wakeup Function				
Date:	Tuesday, July 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	32 of 34

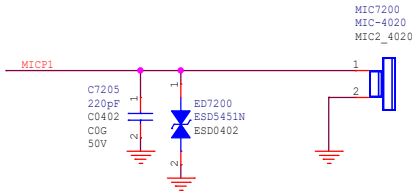
Audio Port



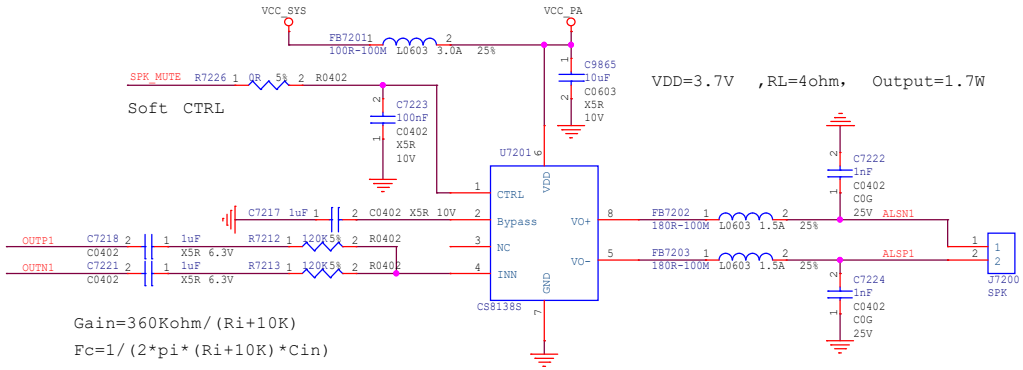
CODEC



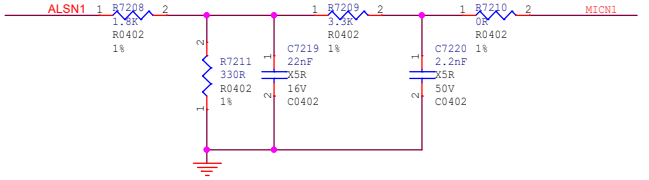
MIC



SPK



LOOP BACK



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_REF				
File:	72.Audio Port2				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	33 of 34

M9900
MARK

M9901
MARK

M9902
MARK

M9903
MARK

M9904
MARK

M9905
MARK

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	**RV1126_RV1109_REF**				
File:	**99.MARK/HOLE**				
Date:	Monday, July 13, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	34 of 34