RV1126_RV1109 Reference Design

RV1126_RV1109_IPC_ENTRANCEGATE_REF_V13

RV1126_RV1109 Main difference		
	RV1126	RV1109
CPU	Quad A7	Dual A7
NPU	2.0Tops	1.2Tops
ISP	14M Pixel	5M Pixel

Reference Design Main Functions Introduction	
Power	RK809-2 +1DCDC or Discrete Power
RAM	EMMC/SLC NAND FLASH/SPI FLASH
ROM	DDR3L/DDR3/LPDDR3/LPDDR4
Interface	SDMMC/SDIO/MAC/LCD/CIF/MIPI_DSI/MIPI_CSI0/ MIPI_CSI1/LVDS0/LVDS1/I2S/PDM/USB/ADC

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	00.Cover Page				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	1 of 54

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Index and Notes

Note

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Graphic Description

Note

Option

Description

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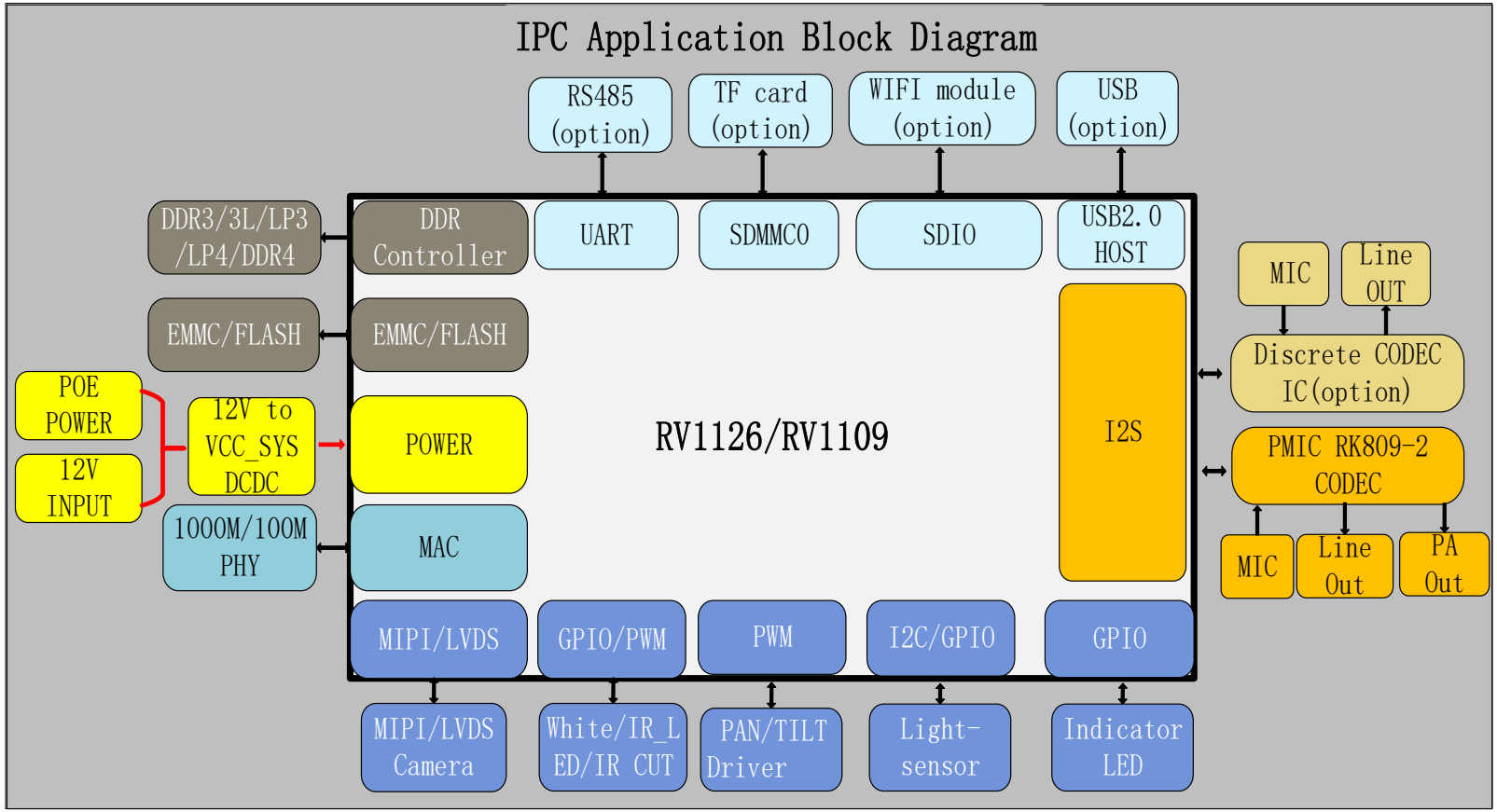
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	01.Index and Notes				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	2 of 54

Revision History

Version	Date	Author	Change Note	Approved
V1.0	2020.04.09	Liyh	IPC REF Design V1.0 for RV1126_RV1109	
V1.1	2020.06.26	Liyh	IPC REF Design V1.1 for RV1126_RV1109 Update: 1.Add usb circuit for improving compability 2.Replace DDR3 template 3.Update some notes	
V1.2	2020.11.02	Liyh	IPC REF Design V1.2 for RV1126_RV1109 Update: 1. Add discrete power solution. 2. Add the discrete CODEC IC solution. 3. Change the IRCUT, PAN/TILT Driver.	
V1.3	2021.01.20	Liyh	IPC and Entrance gate REF Design V1.3 for RV1126_RV1109 Update: 1. Add the funtions of Entrance gate 2. The voltage of logic is raised to 0.825v. 3. Add ADC ES7202 to realize the following two functions: 1). Realize the function of single differential mic and differential loopback for RK809-2 power solution. 2). Realize the function of double differential mic and differential loopback for RK809-2 power solution. 4.The reference drawing of Entrance gate and IPC are combined into one schematic.The previously released reference schematic of Entrance gate will stop updating. For the Entrancel gate solution, please refer to this schematic. 5.Add a page of schematic instructions to explain that IPC and gate solution can select the corresponding schematic quickly.	



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	03.IPC Block Diagram				
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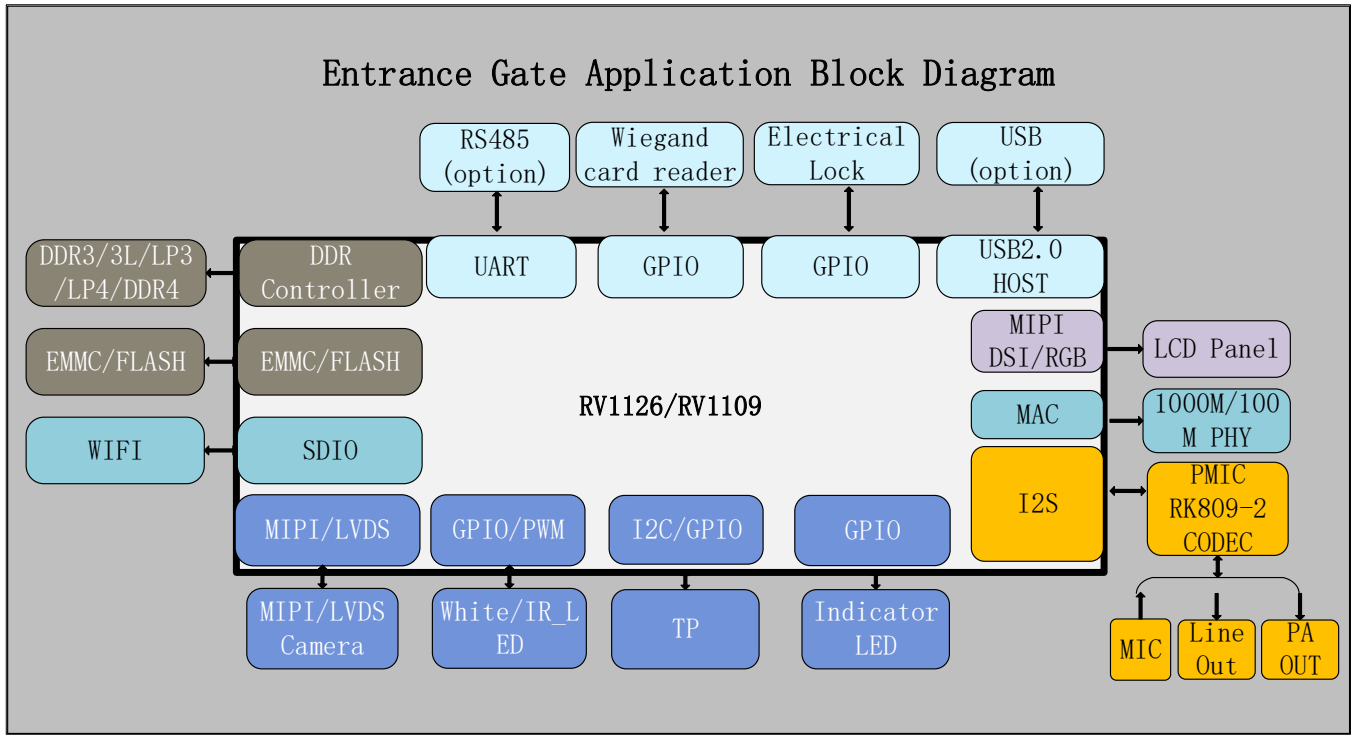
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	4 of 54



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	04.Entrancegate Block Diagram				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
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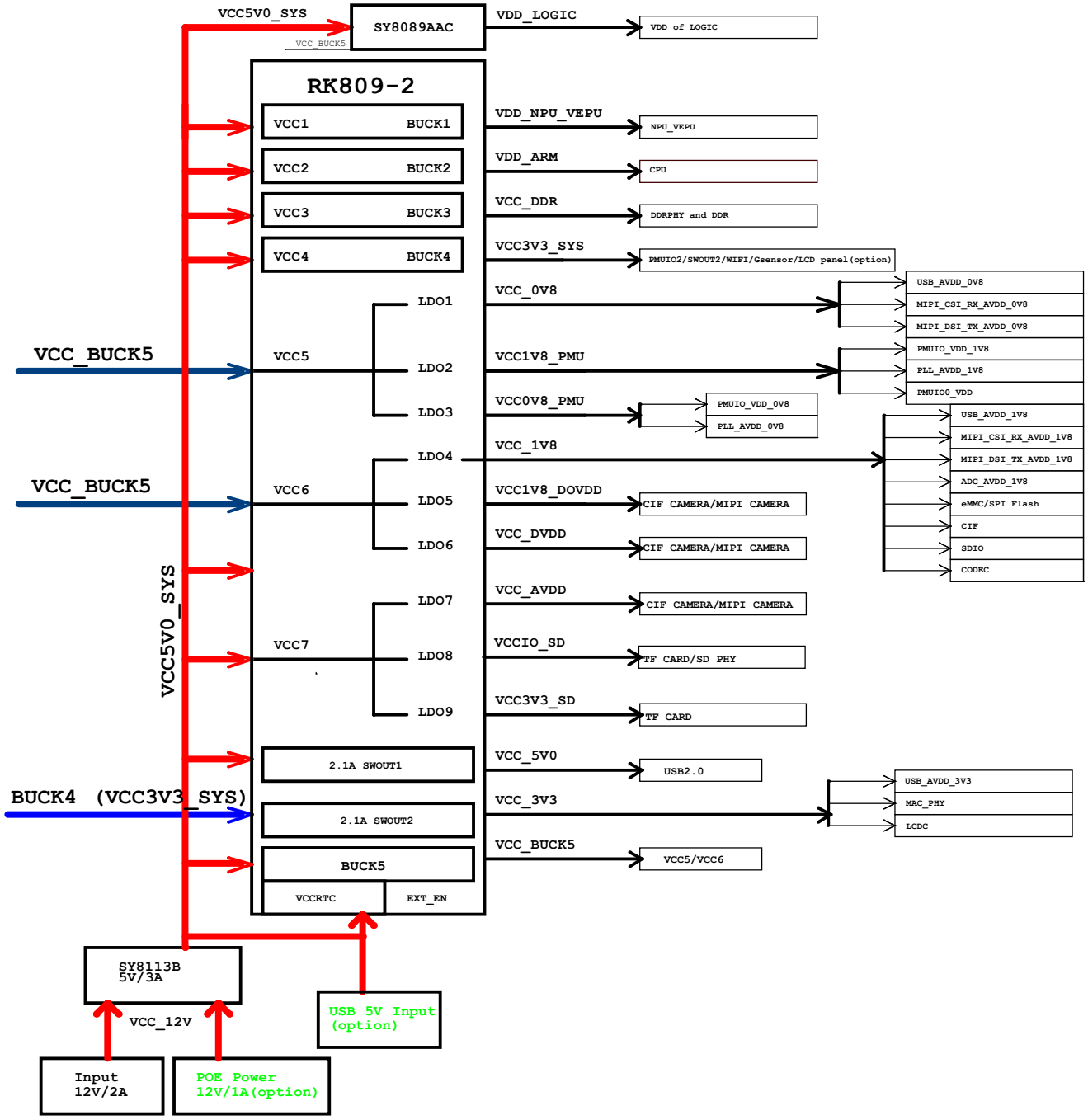
PMIC Power Diagram



The reference power on sequence of RK809-2 and discrete BUCK

Power Name	PMIC Channel	Time (step=2ms)	Default voltage	Supply Limit	Default ON/OFF	Sleep ON/OFF	Peak Current
VCC_BUCK5	RK809-2 BUCK5	Slot: 1	2.2V	2.5A	ON	ON	
VCC0V8_PMU	RK809-2 LDO3	Slot: 2	0.8V	0.1A	ON	ON	
VCC_0V8	RK809-2 LDO1	Slot: 2	0.8V	0.4A	ON	OFF	
VDD_ARM	RK809-2 BUCK2	Slot: 2	0.8V	2.5A	ON	OFF	0.73A@1.8GHz
VDD_NPU	RK809-2 BUCK1	Slot: 2	0.8V	2.0A	ON	OFF	1.34A@934MHz
VDD_VEPU	RK809-2 BUCK1	Slot: 2	0.8V	2.0A	ON	OFF	0.77A@700MHz
VDD_LOGIC	Ext(SY8089AAC)	Slot 1+3ms	0.8V	2.5A	ON	ON	1.75A
VCC_DDR	RK809-2 BUCK3	Slot: 3	1.5V	1.5A	ON	ON	
VCC1V8_PMU	RK809-2 LDO2	Slot: 3	1.8V	0.4A	ON	ON	
VCC_1V8	RK809-2 LDO4	Slot: 3	1.8V	0.4A	ON	OFF	
VCC3V3_SYS	RK809-2 BUCK4	Slot: 4	3.3V	1.5A	ON	ON	
VCC_3V3	RK809-2 SWOUT2	Slot: 4	3.3V	1.5A	ON	OFF	
VCCIO_SD	RK809-2 LDO8	Slot: 4	3.3V	0.4A	ON	OFF	
VCC3V3_SD	RK809-2 LDO9	Slot: 4	3.3V	0.4A	ON	OFF	
VCC1V8_DOVDD	RK809-2 LDO5		1.8V	0.4A	OFF	OFF	
VCC_DVDD	RK809-2 LDO6		1.2V	0.4A	OFF	OFF	
VCC_AVDD	RK809-2 LDO7		2.8V	0.4A	OFF	OFF	
VCC5V0_HOST	RK809-2 SWOUT1		5V	2.1A	ON	OFF	
RESET	RK809-2 sent out Reset signal for soc(SLOT:5(10ms))						

NOTE:VCC_DVDD and VCC_AVDD according to camera sensor voltage

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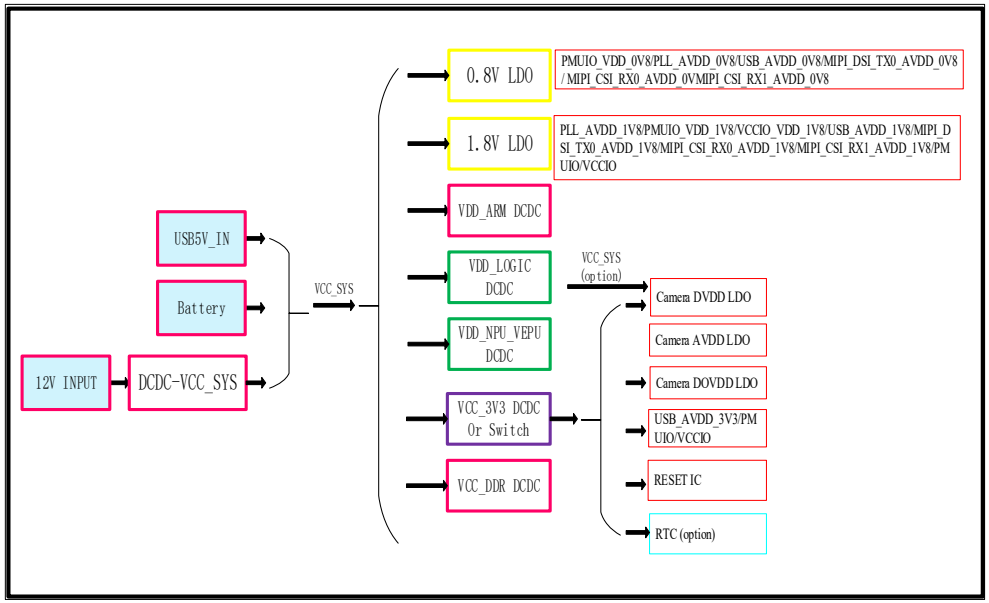
Project:	RV1126_RV1109_IPC_ENTRANCEGATE						
File:	05.PMIC Power Diagram						
Date:	Wednesday, January 20, 2021			Rev:	V1.3		
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	6 of 54		

Power Diagram



The reference power on sequence of discrete power

Power Name	Power Channel	the requirement of power on sequence	Default voltage	Supply Limit	Peak Current
VCC_0V8	LDO	1	0.8V	0.5A	
VDD_LOGIC	BUCK	2	0.8V	2.0A	1.75A
VDD_ARM	BUCK	2	0.8V	1.0A	0.73A
VDD_NPU_VEPU	BUCK	2	0.8V	3.0A	2.11A
VCC_1V8	LDO	3	1.8V	0.5A	
VCC_DDR	BUCK	4	1.1V/1.2V/1.35V/1.5V	2.0A	
VCC_3V3	BUCK or Switch	5	3.3V	2.0A	
VCC1V8_DOVDD	LDO		1.8V	0.5A	
VCC1V2_DVDD	LDO		1.2V	0.5A	
VCC2V8_AVDD	LDO		2.8V	0.5A	
RESET					

NOTE:VCC_DVDD and VCC_AVDD according to camera sensor voltage

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Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	06.Discrete Power Diagram				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	7 of 54

I2C MAP

Port	Pin Name	Domain	Bus Name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Slave Bus Capability	Note
I2C0	I2C0_SCL/GPIO0_B4_u I2C0_SDA/GPIO0_B5_u	PMUIO1	I2C0_SCL_PMIC I2C0_SDA_PMIC	VCC3V3_SYS	RK809-2	0x20		PMIC
I2C1	I2C1_SCL/GPIO1_D3_u I2C1_SDA/GPIO1_D2_u	VCCIO4	I2C1_SCL I2C1_SDA	VCC1V8_DOVDD				CIF camera
								MIPI camera
I2C2	I2C2_SCL/GPIO0_C2_d I2C2_SDA/GPIO0_C3_d	PMUIO1	I2C2_SCL I2C2_SDA	VCC3V3_SYS	RTC			
I2C4	I2C4_SCL_M1/GPIO4_A0_d I2C4_SDA_M1/GPIO4_A1_d	VCCIO7	I2C4_SCL I2C4_SDA	VCC_3V3/VCC_1V8	3.3V:ES8311 1.8V:ES7202			
I2C5	I2C5_SCL_M0/GPIO2_A5_d I2C5_SDA_M0/GPIO2_B3_d	VCCIO5	I2C5_SCL I2C5_SDA	VCC_3V3	MS32006 CM32181A3OP			

IO Power Domain Map

IO Domain	IO Group	Support of IO Voltage		Default Actual assigned IO Domain Voltage			Notes
		1.8V	3.3V	Net Name of Power Supply	Power Source	Voltage	
PMUIO0	***GPIO0A***	✓	✓	*VCC1V8_PMU*	*RK809-2_LDO2*	*1.8V*	
PMUIO1	***GPIO0BC***	✓	✓	*VCC3V3_SYS*	*RK809-2_BUCK4*	*3.3V*	
VCCIO1	***GPIO0CD/GPIO1A***	✓	✓	*VCCIO_FLASH*	*RK809-2_LDO4*	*1.8V*	*GPIO0_B3/FLASH_VOL_SEL pin defined as a set pin for VCCIO1 voltage.*
VCCIO2	***GPIO1AB***	✓	✓	*VCCIO_SD*	*RK809-2_LDO8*	*3.3V*	
VCCIO3	***GPIO1BCD***	✓	✓	*VCCIO3_VDD*	*RK809-2_LDO4*	*1.8V*	
VCCIO4	***GPIO1D/GPIO2A***	✓	✓	*VCCIO4_VDD*	*RK809-2_LDO4*	*1.8V*	
VCCIO5	***GPIO2ABCD/GPIO3A***	✓	✓	*VCCIO5_VDD*	*RK809-2_SWOUT2*	*3.3V*	
VCCIO6	***GPIO3ABC***	✓	✓	*VCCIO6_VDD*	*RK809-2_LDO4*	*1.8V*	
VCCIO7	***GPIO3D/GPIO4A***	✓	✓	*VCCIO7_VDD*	*RK809-2_LDO4*	*1.8V*	

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Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	08.IO Power Domain Map				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	9 of 54

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Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	09.Schematic instructions				
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Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	10 of 54

Power

U1000N
RV1126/RV1109
BGA409 14R00X14R00X0R90

NPU/LOGIC/VEPU/ARM Power

NPU_VDD_1	H11	VDD_NPU_VEPU
NPU_VDD_2	H12	
NPU_VDD_3	J10	
NPU_VDD_4	J11	
NPU_VDD_5	K10	
NPU_VDD_6	K11	
LOGIC_VDD_1	H9	VDD_LOGIC
LOGIC_VDD_2	J9	
LOGIC_VDD_3	L10	
LOGIC_VDD_4	M11	
LOGIC_VDD_5	H13	
LOGIC_VDD_6	J13	
VEPU_VDD_1	L9	VDD_NPU_VEPU
VEPU_VDD_2	M9	
VEPU_VDD_3	N8	
VEPU_VDD_4	N9	
ARM_VDD_1	N12	VDD_ARM
ARM_VDD_2	P12	
ARM_VDD_3	P13	

Supply for VCCIO1~7 Power

VCCIO_VDD_1V8 — H14

VCCIO_VDD_1V8 — R1000 (3.3R, R0402, 1%) — VCC_1V8

C1000 1nF X5R 25V C0201

NOTE:
If any power domain of vccio 1 ~ vccio 7 is used,
then VCCIO_ VDD_ 1V8 must be connected to 1.8V power supply

VDD_NPU_VEPU

C1006 10uF X5R 4V C0402
C1005 1uF X5R 6.3V C0402
C1004 1uF X5R 6.3V C0402
C1003 100nF X5R 6.3V C0201
C1002 100nF X5R 6.3V C0201
C1001 100nF X5R 6.3V C0201

For NPU Power

VDD_NPU_VEPU

C1019 10uF X5R 4V C0402
C1018 1uF X5R 6.3V C0402
C1017 100nF X5R 6.3V C0201
C1016 100nF X5R 6.3V C0201

For VEPU Power

VDD_ARM

C1015 10uF X5R 4V C0402
C1014 1uF X5R 6.3V C0402
C1013 100nF X5R 6.3V C0201
C1012 100nF X5R 6.3V C0201

VDD_LOGIC

C1011 10uF X5R 4V C0402
C1009 1uF X5R 6.3V C0402
C1010 1uF X5R 6.3V C0402
C1007 100nF X5R 6.3V C0201
C1008 100nF X5R 6.3V C0201

GND

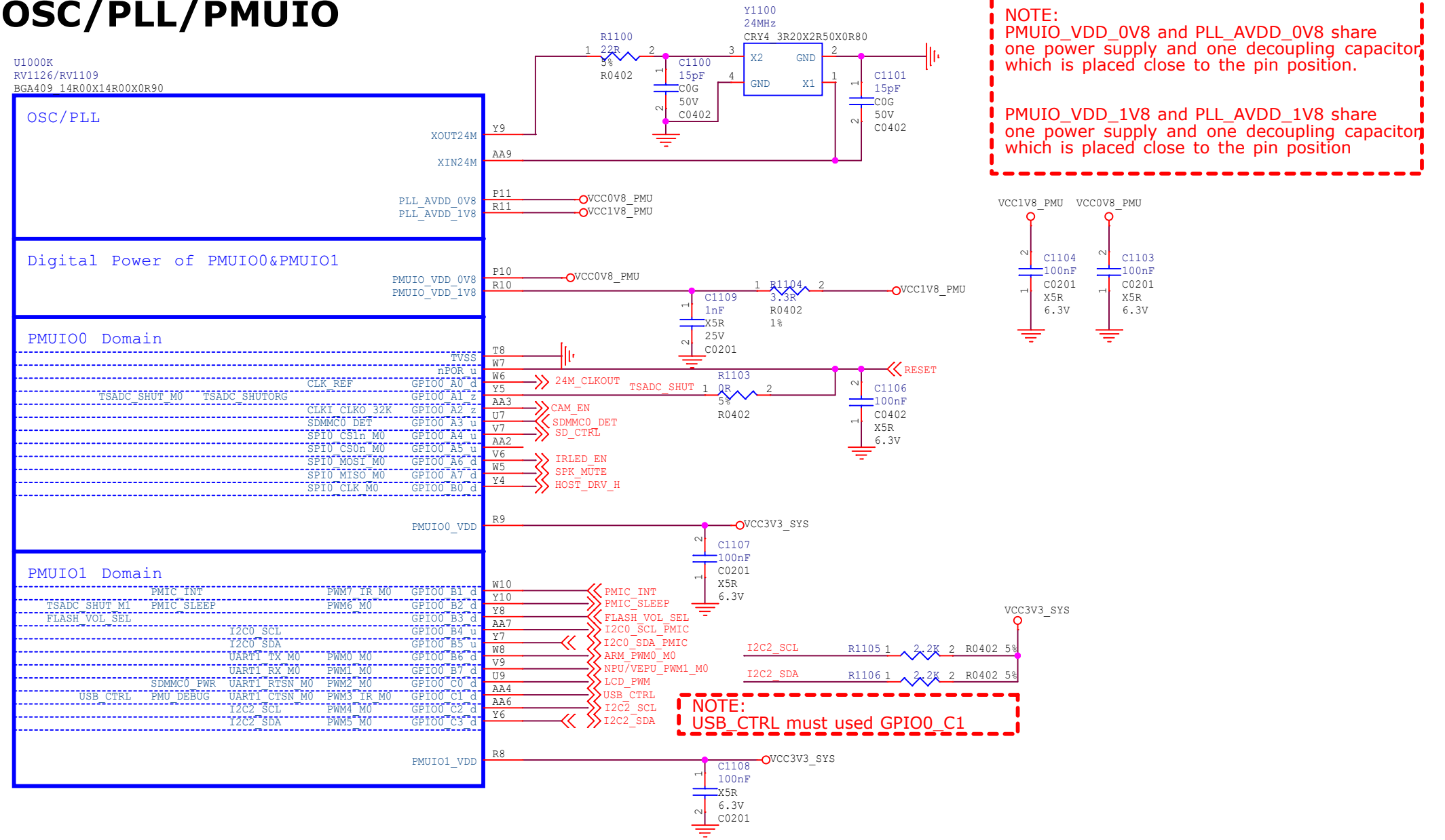
U1000O
RV1126/RV1109
BGA409 14R00X14R00X0R90

VSS/AVSS

A1	VSS_1	VSS_53	K9		
A21	AVSS_2	VSS_54	K12		
B12	VSS_3	VSS_55	K13		
C3	VSS_4	VSS_56	K14		
C5	VSS_5	VSS_57	L2		
C7	VSS_6	VSS_58	L5		
C10	VSS_7	VSS_59	L6		
C12	VSS_8	VSS_60	L11		
D9	VSS_9	VSS_61	L12		
D12	VSS_10	VSS_62	L13		
D18	AVSS_11	VSS_63	L14		
E4	VSS_12	VSS_64	L16		
E6	VSS_13	VSS_65	M3		
E8	VSS_14	VSS_66	M5		
E9	VSS_15	VSS_67	M7		
E10	VSS_16	VSS_68	M8		
E11	VSS_17	VSS_69	M10		
E12	VSS_18	VSS_70	M12		
F3	VSS_19	VSS_71	M13		
F5	VSS_20	VSS_72	M14		
F7	VSS_21	VSS_73	M16		
F8	VSS_22	VSS_74	N5		
F9	VSS_23	VSS_75	N6		
F10	VSS_24	VSS_76	N7		
F11	VSS_25	VSS_77	N10		
F12	VSS_26	VSS_78	N11		
F13	VSS_27	VSS_79	N13		
F14	AVSS_28	VSS_80	N14		
F15	AVSS_29	VSS_81	N16		
G2	VSS_30	VSS_82	P5		
G5	VSS_31	VSS_83	P7		
G6	VSS_32	VSS_84	P8		
G10	VSS_33	VSS_85	P9		
G11	VSS_34	VSS_86	P14		
G12	VSS_35	VSS_87	P16		
G13	VSS_36	VSS_88	R1		
G16	AVSS_37	VSS_89	R5		
G17	AVSS_38	VSS_90	R12		
H4	VSS_39	VSS_91	R13		
H5	VSS_40	VSS_92	R14		
H6	VSS_41	VSS_93	T6		
H7	VSS_42	VSS_94	T9		
H10	VSS_43	VSS_95	T10		
H15	VSS_44	VSS_96	T14		
J5	VSS_45	VSS_97	T17		
J6	VSS_46	VSS_98	V17		
J12	VSS_47	VSS_99	W9		
J14	VSS_48	VSS_100	W14		
J16	VSS_49	VSS_101	AA1		
K5	VSS_50	VSS_102	AA10		
K6	VSS_51	VSS_103	AA21		
K8	VSS_52				

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	10.RV1126/1109_Power/GND				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	11 of 54

OSC/PLL/PMUIO

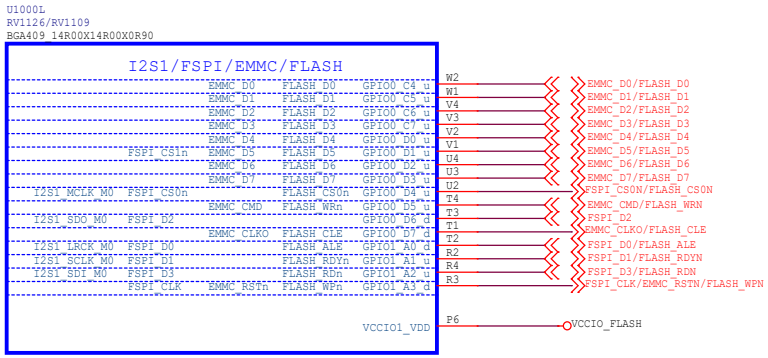


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	11.RV1126/1109_OSC/PLL/PMUIO				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	12 of 54

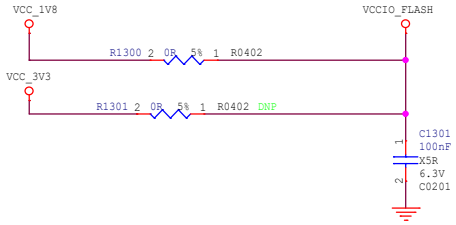
DDR Controller

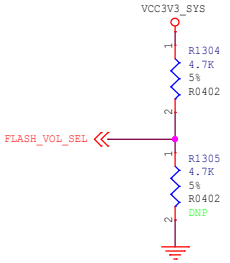
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RV1126_RV1109_IPC_ENTRANCEGATE
File:	12.RV1126/1109_DRAM Controller
Date: Wednesday, January 20, 2021	Rev: V1.3
Designed by: Yanhong.Li / Reviewed by: <Checker>	Sheet: 13 of 54

EMMC/FLASH



NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.

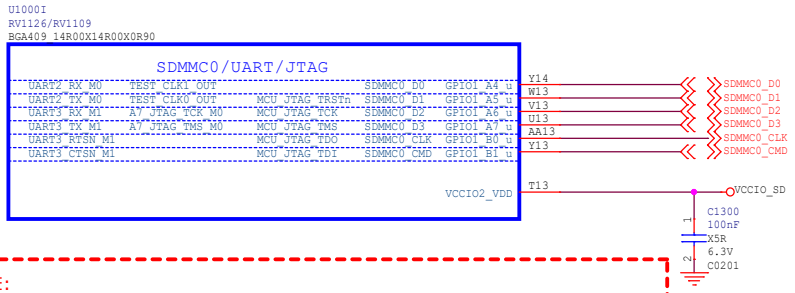




NOTE:
FLASH(VCCIO1) power domain IO supply configuration pin:

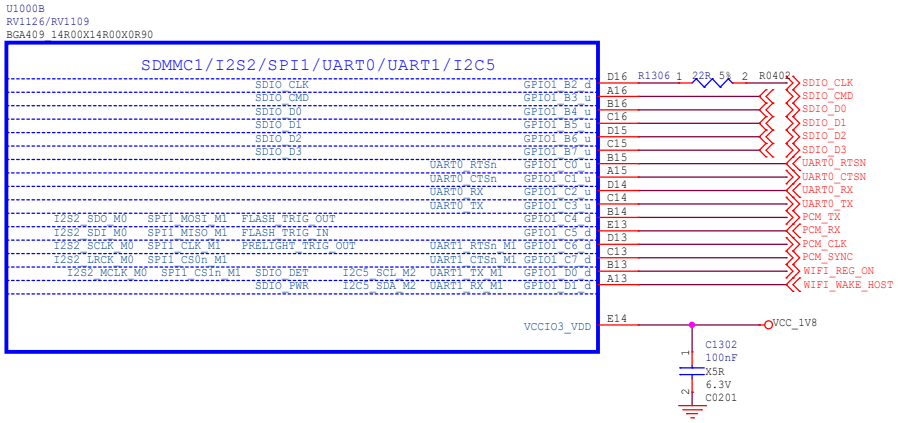
Condition	VCCIO1 (VCCIO_FLASH)
FLASH_VOL_SEL=0	3.3V
FLASH_VOL_SEL=1	1.8V Default

SDMMC0/JTAG



NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.
If SD card is not used,please reserve MCU JTAG interface

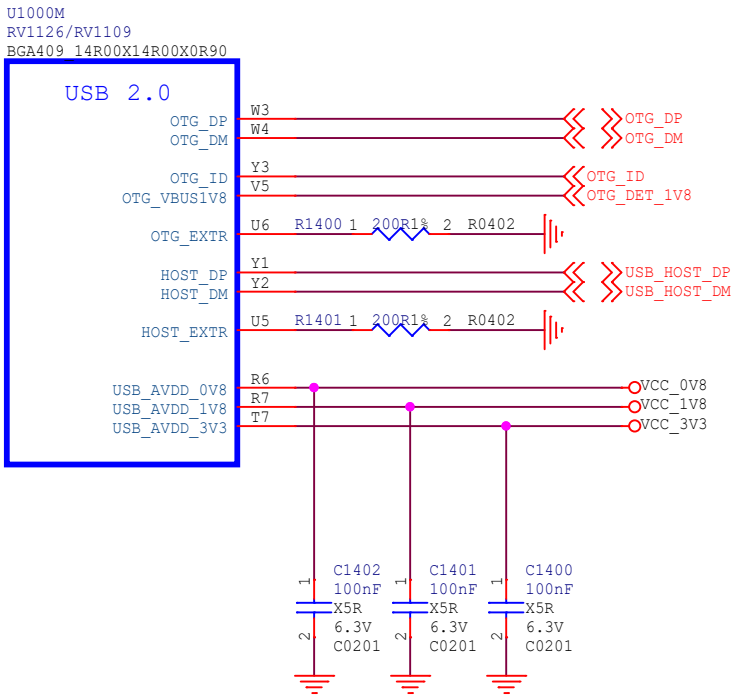
SDMMC1/UART/I2S2



NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.

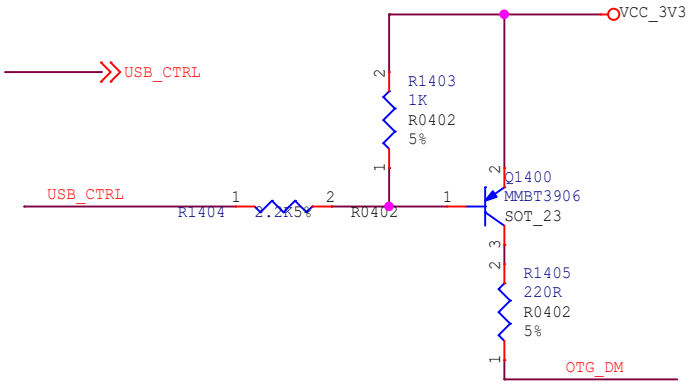
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	13.RV1126/1109_Flash/SD				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	14 of 54

USB Controller



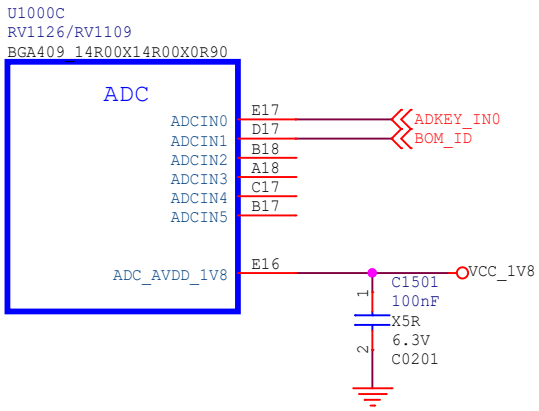
USB2.0 design rules:
1. Max intra-pair skew <4ps
2. Max trace length<6inchs
3. Max allowed via <6
4. Trace impedance 90ohm+/-10%
5. The distance between other signals follows the 3W rule.

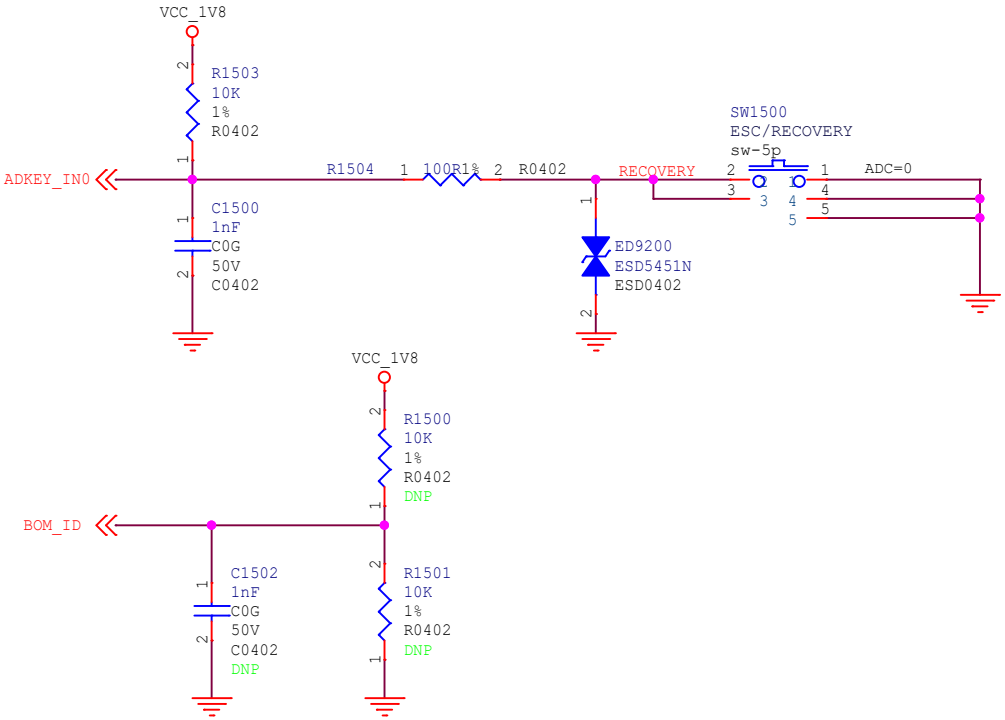
This circuit is used to improve usb compatibility.
Note:
These components are close to R2502 to avoid long branches.



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	14.RV1126/1109_USB Controller				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	15 of 54

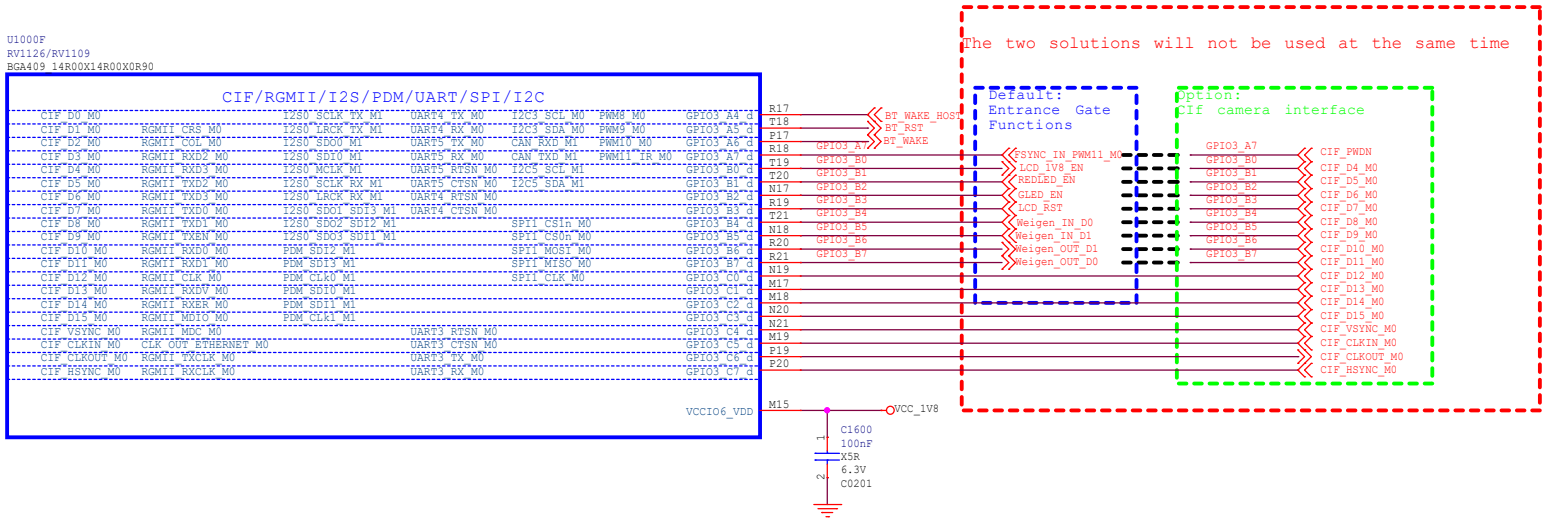
SARADC





Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	15.RV1126/1109_SARADC				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	16 of 54

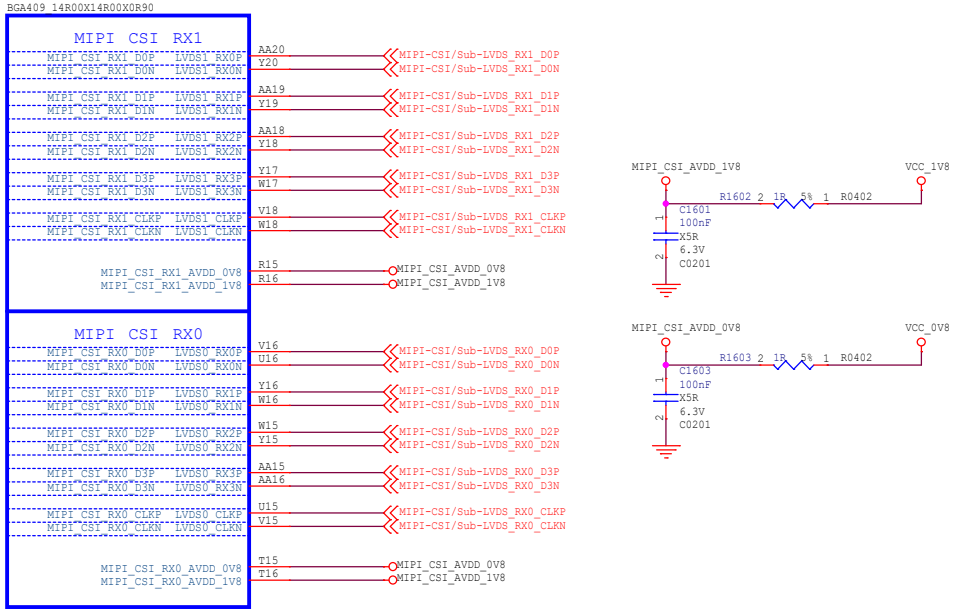
CIF Interface



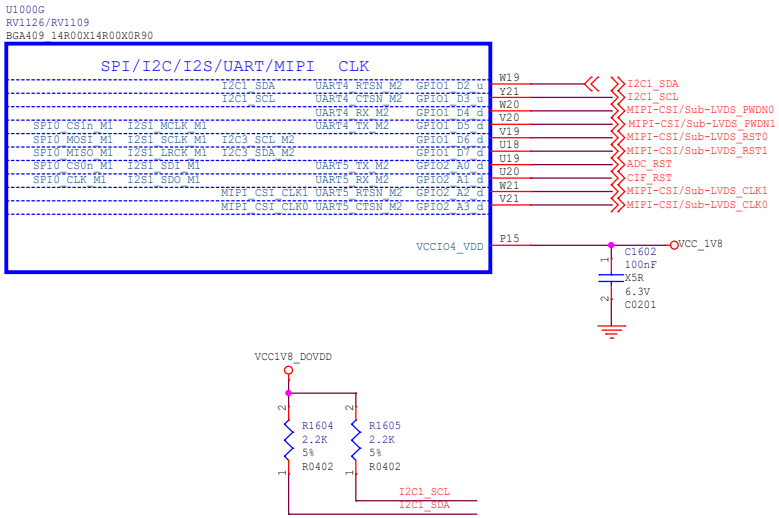
BT1120 RX	DATA:CIF_DATA[15:0] Y[0:7]:CIF_DATA[8:15] Cb[0:7]:CIF_DATA[0:7] CLOCK:CIF_CLKIN
12bit CIF camera	CameraCIF[11:0]:CIF_DATA[15:4] XCLK:CIF_CLKOUT PCLK:CIF_CLKIN HSYNC:CIF_HSYNC VSYNC:CIF_VSYNC
10bit CIF camera	CameraCIF[9:0]:CIF_DATA[15:6] XCLK:CIF_CLKOUT PCLK:CIF_CLKIN HSYNC:CIF_HSYNC VSYNC:CIF_VSYNC
8bit CIF camera	CameraCIF[7:0]:CIF_DATA[15:8] XCLK:CIF_CLKOUT PCLK:CIF_CLKIN HSYNC:CIF_HSYNC VSYNC:CIF_VSYNC

MIPI-CSI Interface

MIPI_CSI_RX0 and MIPI_CSI_RX1 power pins are adjacent, so they share a decoupling capacitor
All the power filter capacitors should be placed close to the power pins of SOC.

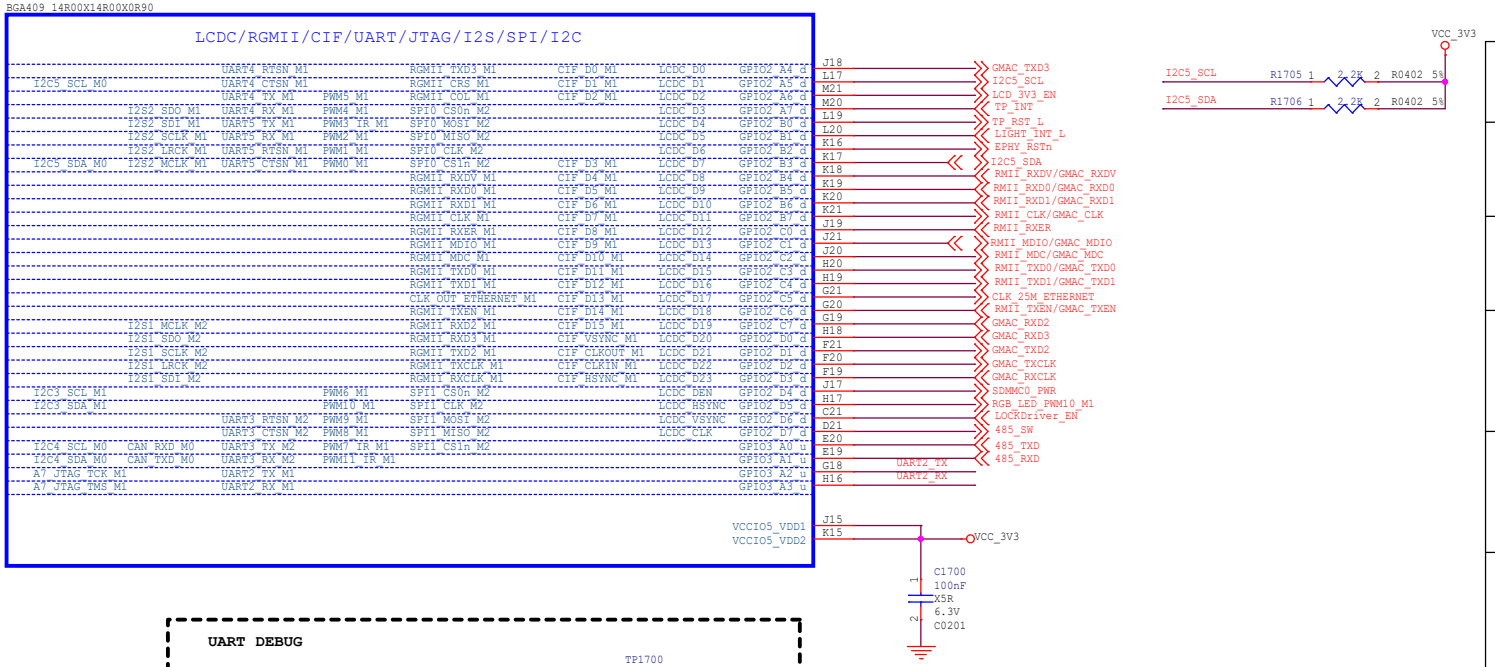


I2C/SPI/MIPI-CLK

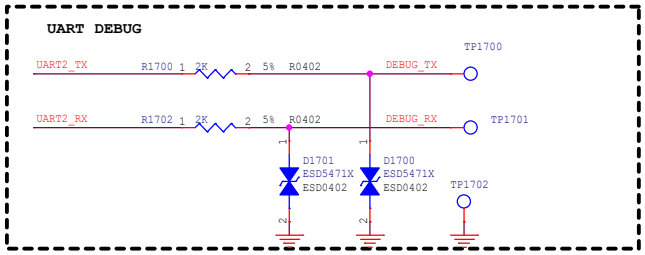


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RV1126_RV1109_IPC_ENTRANCEGATE
File:	16.RV1126/1109_VideoInput
Date:	Wednesday, January 20, 2021
Rev:	V1.3
Designed by:	Yanhong.Li
Reviewed by:	<Checker>
Sheet:	17 of 54

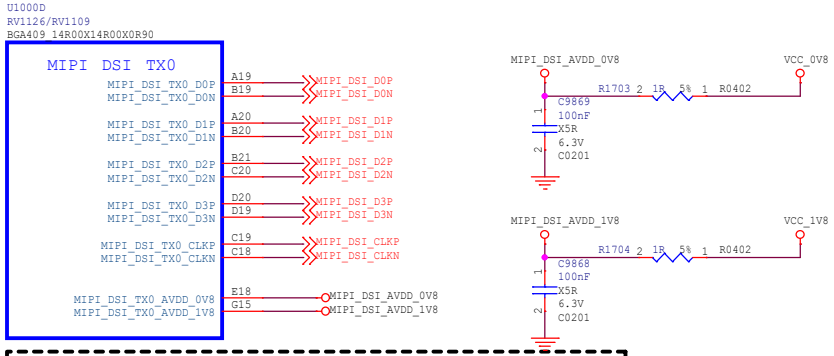
LCDC/RGMII/PWM



BT1120 TX	DATA:LCDC_DATA[15:0] Y[0:7]:LCDC_DATA[8:15] Cb[0:7]:LCDC_DATA[0:7] CLOCK:LCDC_CLK
6bit Serial RGB	DATA:LCDC_DATA[5:0] CLOCK:LCDC_CLK HSYNC:LCDC_HSYNC VSYNC:LCDC_VSYNC DE:LCDC_DEN
8bit Serial RGB	DATA:LCDC_DATA[7:0] CLOCK:LCDC_CLK HSYNC:LCDC_HSYNC VSYNC:LCDC_VSYNC DE:LCDC_DEN
16bit Parallel RGB(RGB565)	R[4:0]:LCDC_DATA[15:11] G[5:0]:LCDC_DATA[10:5] B[4:0]:LCDC_DATA[4:0] CLOCK:LCDC_CLK HSYNC:LCDC_HSYNC VSYNC:LCDC_VSYNC DE:LCDC_DEN
18bit Parallel RGB(RGB666)	R[5:0]:LCDC_DATA[17:12] G[5:0]:LCDC_DATA[11:6] B[5:0]:LCDC_DATA[5:0] CLOCK:LCDC_CLK HSYNC:LCDC_HSYNC VSYNC:LCDC_VSYNC DE:LCDC_DEN
24bit Parallel RGB(RGB888)	R[7:0]:LCDC_DATA[23:16] G[7:0]:LCDC_DATA[15:8] B[7:0]:LCDC_DATA[7:0] CLOCK:LCDC_CLK HSYNC:LCDC_HSYNC VSYNC:LCDC_VSYNC DE:LCDC_DEN



MIPI-DSI Interface



If use MIPI DSI ,E18 connct to VCC_0V8, G15 connect to VCC_1V8.
Otherwise, E18 and G15 don't need to supply power.

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	17.RV1126/1109_VideoOutput Interface				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	18 of 54

Audio Interface

U1000J
RV1126/RV1109
BGA409_14R00X14R00X0R90

I2S/PDM/ACODEC/I2C

I2S0_SCLK_TX_M0		ACODEC_DAC_CLK			GPIO3_D0_d	W12
I2S0_SCLK_RX_M0	PDM_CLK1_M0	ACODEC_ADC_CLK			GPIO3_D1_d	V12
I2S0_MCLK_M0					GPIO3_D2_d	U12
I2S0_LRCK_TX_M0		ACODEC_DAC_SYNC	AUDPWM_L_M1	AUDDSM_LN	GPIO3_D3_d	W11
I2S0_LRCK_RX_M0	PDM_CLK0_M0	ACODEC_ADC_SYNC			GPIO3_D4_d	Y12
I2S0_SDO0_M0		ACODEC_DAC_DATAR	AUDPWM_R_M1	AUDDSM_LP	GPIO3_D5_d	Y11
I2S0_SDI0_M0	PDM_SDI0_M0	ACODEC_DAC_DATAL			GPIO3_D6_d	AA12
I2S0_SDO1_SDI3_M0	PDM_SDI3_M0	ACODEC_ADC_DATA			GPIO3_D7_d	T11
I2S0_SDO2_SDI2_M0	PDM_SDI2_M0	I2C4_SCL_M1	AUDPWM_L_M0	AUDDSM_RN	GPIO4_A0_d	U11
I2S0_SDO3_SDI1_M0	PDM_SDI1_M0	I2C4_SDA_M1	AUDPWM_R_M0	AUDDSM_RP	GPIO4_A1_d	V11
					VCCIO7_VDD	T12

I2S0_SCLK_TX_M0
PDM_CLK1
I2S0_MCLK_M0
I2S0_LRCK_TX_M0
PDM_CLK0_M0
I2S0_SDO0_M0
I2S0_SDI0_M0
PDM_SDI3_M0
I2C4_SCL_M1
I2C4_SDA_M1

VCC_1V8
R1800 2 0R 5% 1 R0402

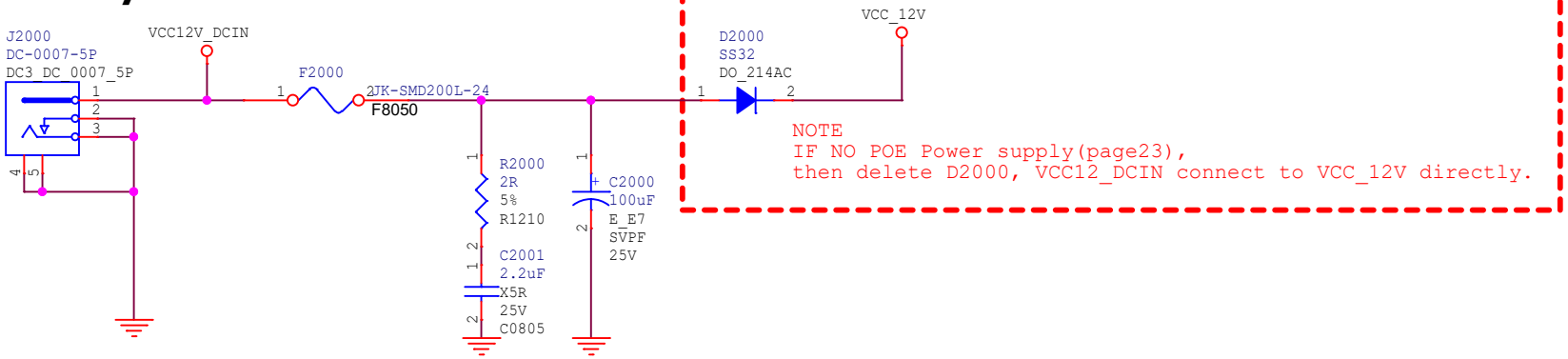
VCC_3V3
R1801 2 0R 5% 1 R0402 DNP

C1800
100nF
X5R
6.3V
C0201

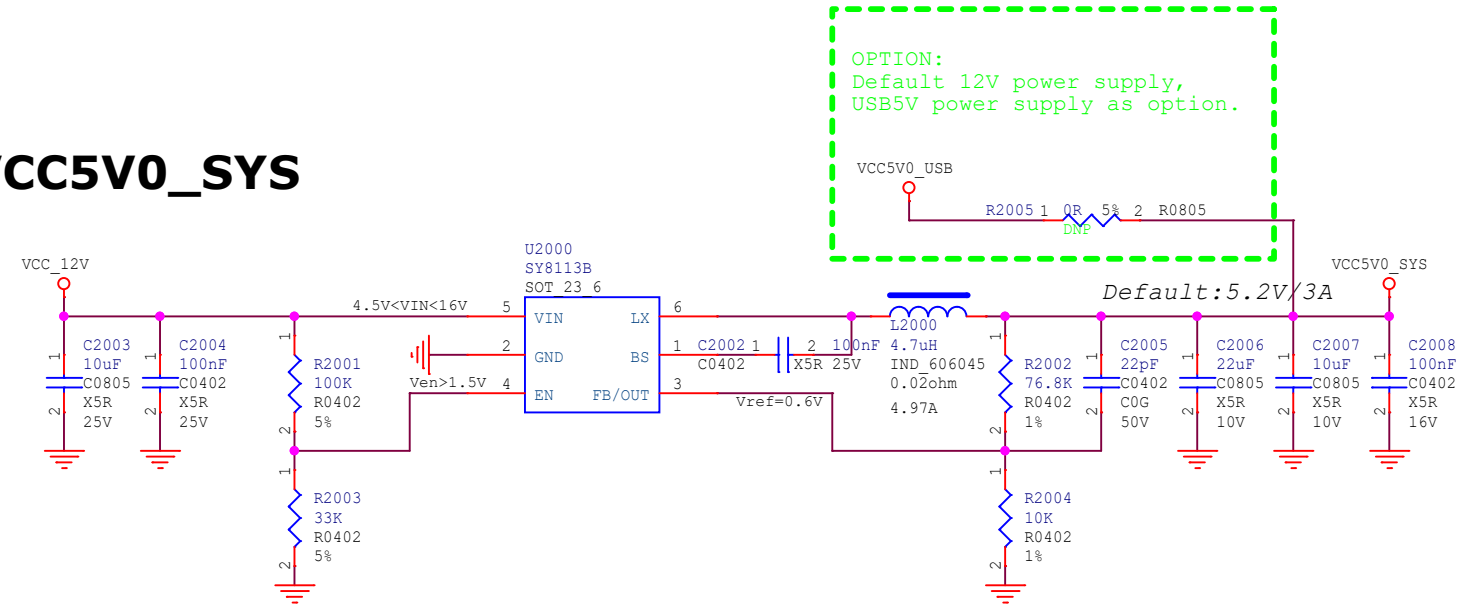
NOTE:
If the audio of RK809-2 is used, then R1800=0R, R1801=DNP
If the audio of ES8311 is used,then R1800=DNP,R1801=0R.

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	18.RV1126/1109_Audio				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	19 of 54

12V/2A DCIN



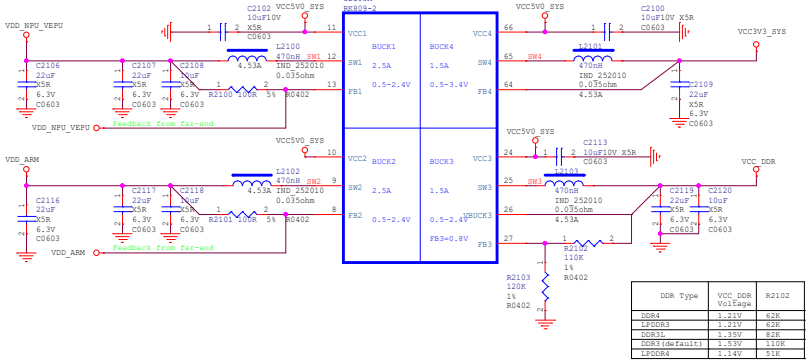
VCC5V0_SYS



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	20.Power_DC IN				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	20 of 54

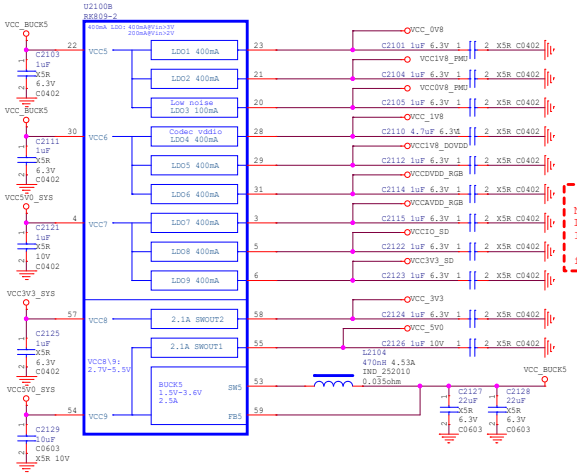
PMIC rk809-2 is recommended for the following solutions:
1) Rk1109 / rv1126 needs to be in standby mode;
2) There are more peripherals and solutions that need more power, such as those that require sd3.0 and screen functions.

PMIC RK809-2 DCDC



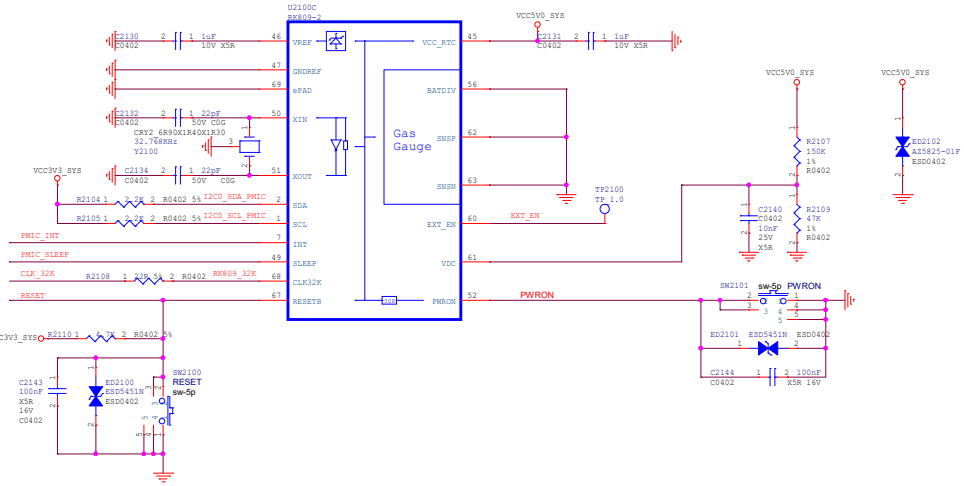
DDR Type	VCC_DDR Voltage	R2102
DDR4	1.21V	62K
LPDDR3	1.21V	62K
DDR3L	1.35V	82K
DDR3(default)	1.53V	110K
LPDDR4	1.14V	51K

PMIC RK809-2 LDO

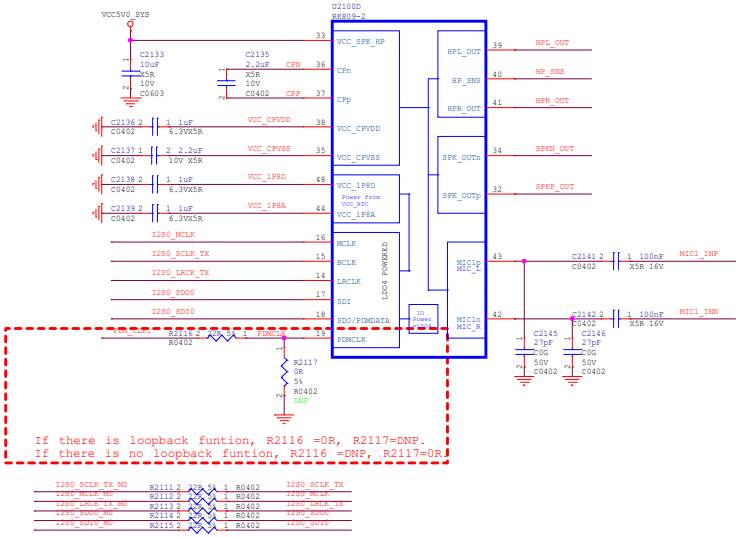


NOTE:
LDO8 and LDO9 output 3.3V default.
If there isn't SD card function, LDO8 and LDO9 can be used for other function .

PMIC RK809-2 Managerment

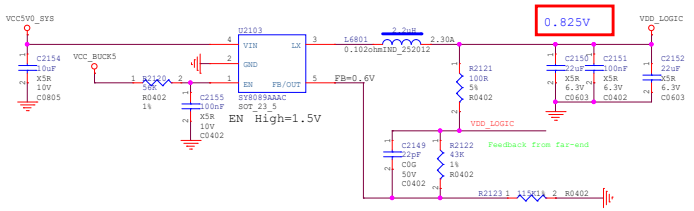


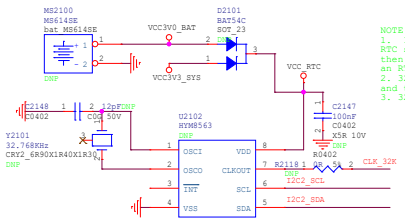
PMIC RK809-2 CODEC



If there is loopback funtion, R2116 =0R, R2117=DNP.
If there is no loopback funtion, R2116 =DNP, R2117=0R.

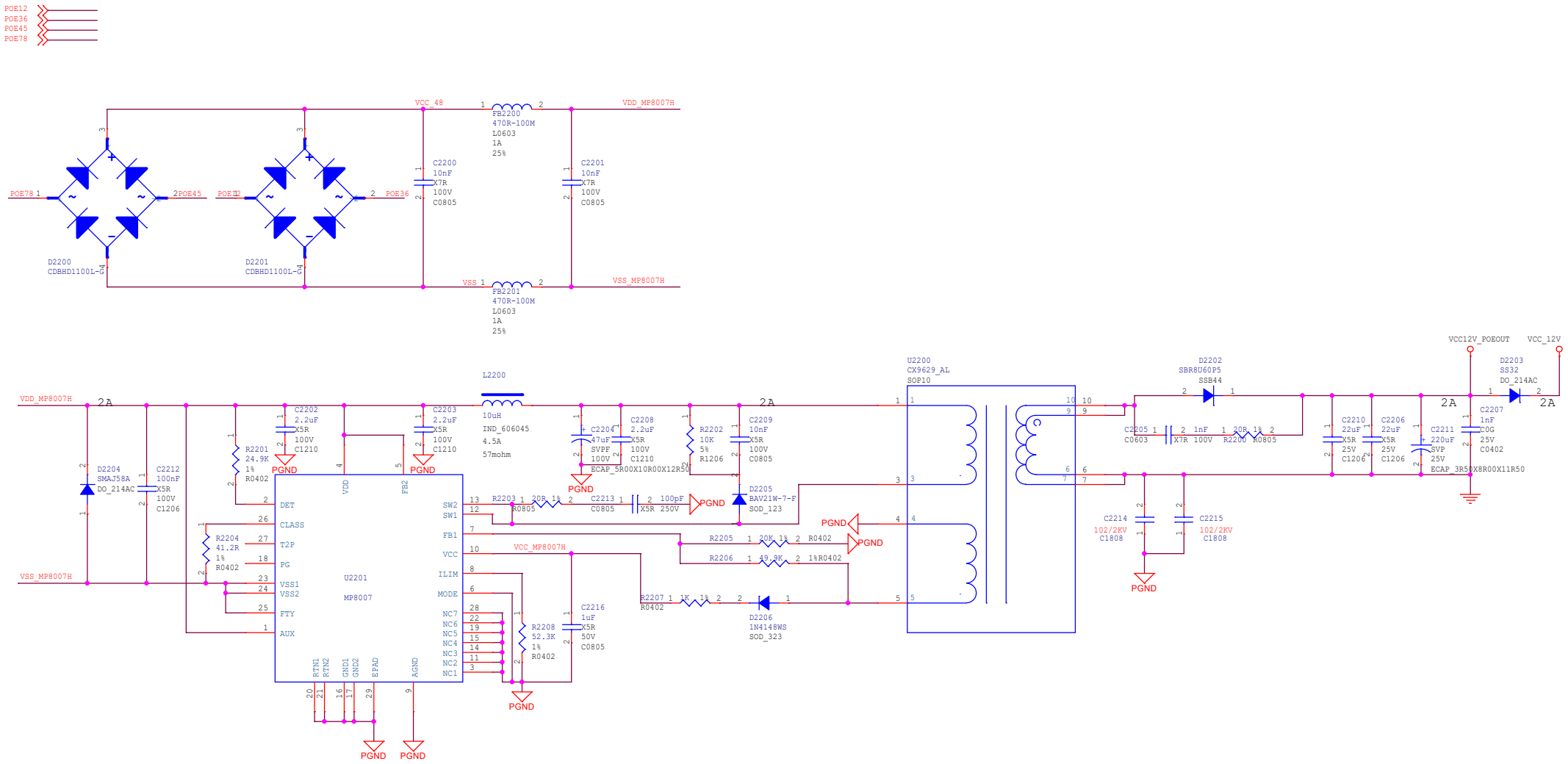
VDD_LOGIC





NOTE:
1. IPC: after the system is powered off, RTC still need to work, then it is necessary to add an RTC IC ,and use battery to power the RTC.
2. 32K crystal is connected to RTC, and the 32K crystal of rk809-2 can be DNP.
3. 32kclk signal can only be output from RTC.

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RV1126_RV1109_IPC_ENTRANCEGATE		
File:	21.Power_PMIC		
Date:	Wednesday, January 20, 2021	Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by: <Checker>	Sheet: 21 of 54



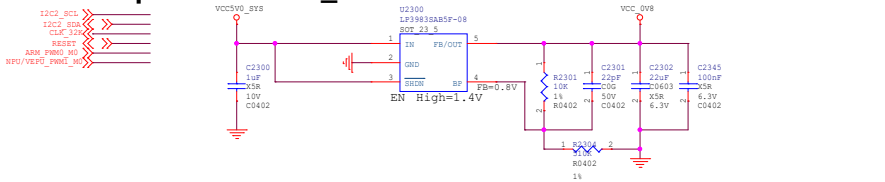
Class	Max Input Power to PD(W)	Classification Current(mA)	R2204(Rclass)
0	12.95	2	578R
1	3.84	10.55	110R
2	6.49	18.7	62R
3	12.95	28.15	41.2R
4	25.5	40.4	28.7R

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	23.POE Power(option)				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	22 of 54

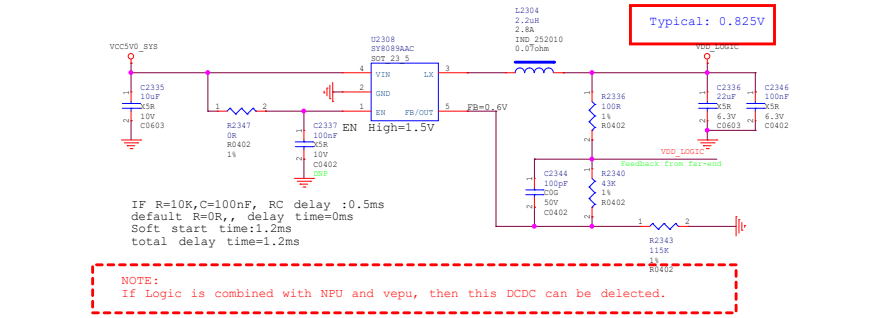
Discrete Power

Discrete power supply is recommended for the following solutions:
1) Less peripheral equipment and less power supply
2) Small PCB space
3) The following discrete power supply solutions can reduce some devices according to the actual products,
Please read the notes on the power supply below.

Power Sequence: 1 VCC_0V8

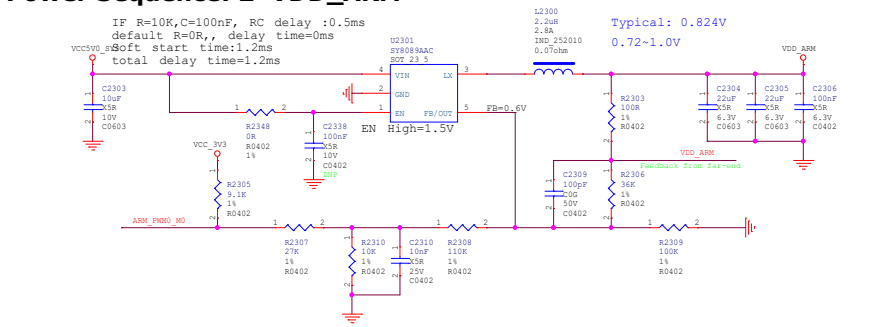


Power Sequence: 2 VDD_LOGIC

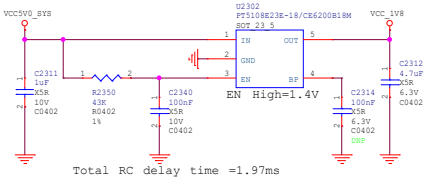


NOTE:
If Logic is combined with NPU and vepu, then this DCDC can be delected.

Power Sequence: 2 VDD_ARM

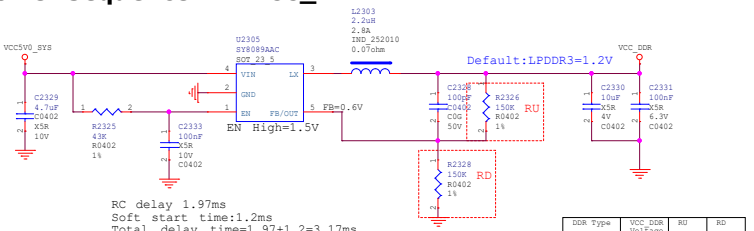


Power Sequence: 3 VCC_1V8



Total RC delay time =1.97ms

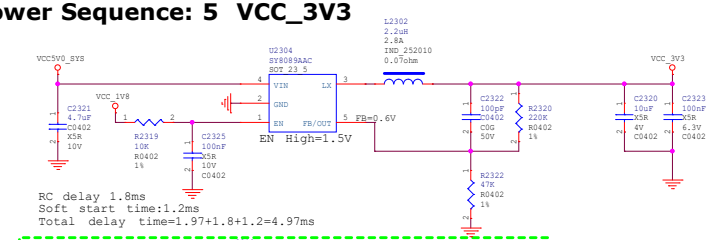
Power Sequence: 4 VCC_DDR



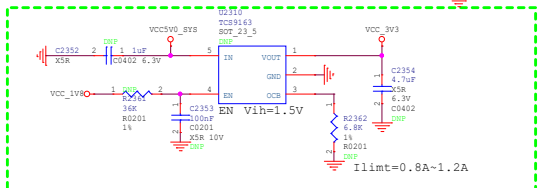
RC delay 1.97ms
Soft start time:1.2ms
Total delay time=1.97+1.2=3.17ms

DDR Type	VCC_DDR Voltage	RU	RD
DDR3L	1.35V	150K	120K
DDR3	1.5V	150K	100K
DDR4	1.2V	150K	150K
LPDDR3	1.2V	150K	150K
LPDDR4	1.1V	150K	180K

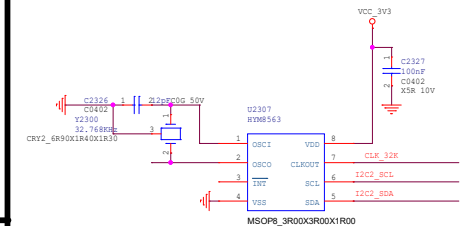
Power Sequence: 5 VCC_3V3

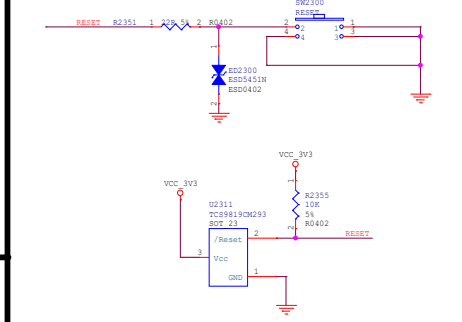


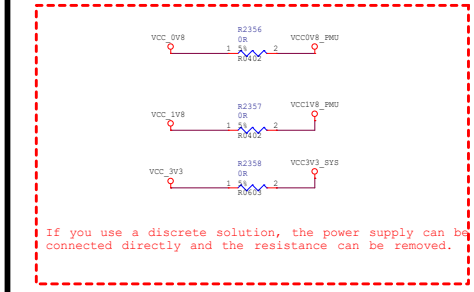
RC delay 1.8ms
Soft start time:1.2ms
Total delay time=1.97+1.8+1.2=4.97ms



NOTE:
Only when VCC5V0_SYS is 3.3V, the tcs9163 switch can be used.
then U2304 can be delected.





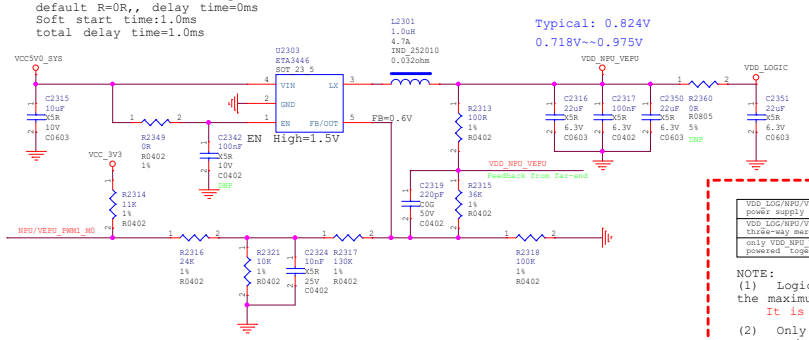


If you use a discrete solution, the power supply can be connected directly and the resistance can be removed.

Power Sequence: 2 VDD_NPU_VEPU

NOTE:
Recommend ETA3446 for better ripple.

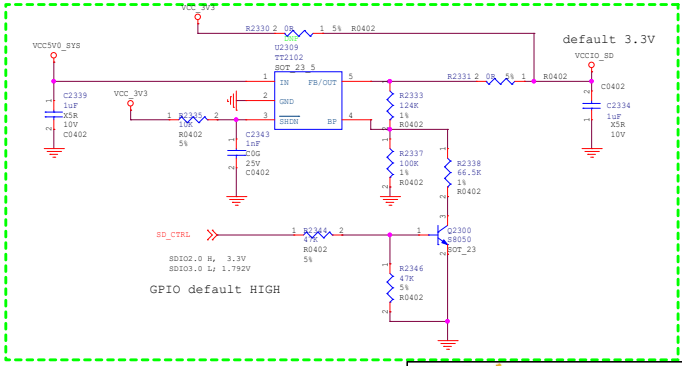
IF R=10K,C=100nF, RC delay :0.5ms
default R=0R,, delay time=0ms
Soft start time:1.0ms
total delay time=1.0ms



VDD_LOG/NPU/VEPU power supply selection	R2314	R2316	R2317	R2360	Voltage range	NOTE
VDD_LOG/NPU/VEPU three-way merge	24K	12K	330K	0R	0.72V~0.88V	(1)
only VDD_NPU_VEPU is powered together	11K	24K	130K	NC	0.715V~0.975V	(2)

NOTE:
(1) Logic is combined with NPU and vepu:
the maximum voltage is only 0.88v, which makes the frequency of NPU not run very high.
It is only suitable for rv1109 and rv1126 without NPU high performance.

(2) Only NPU is combined with vepu:
It is only suitable for rv1109 and rv1126 .



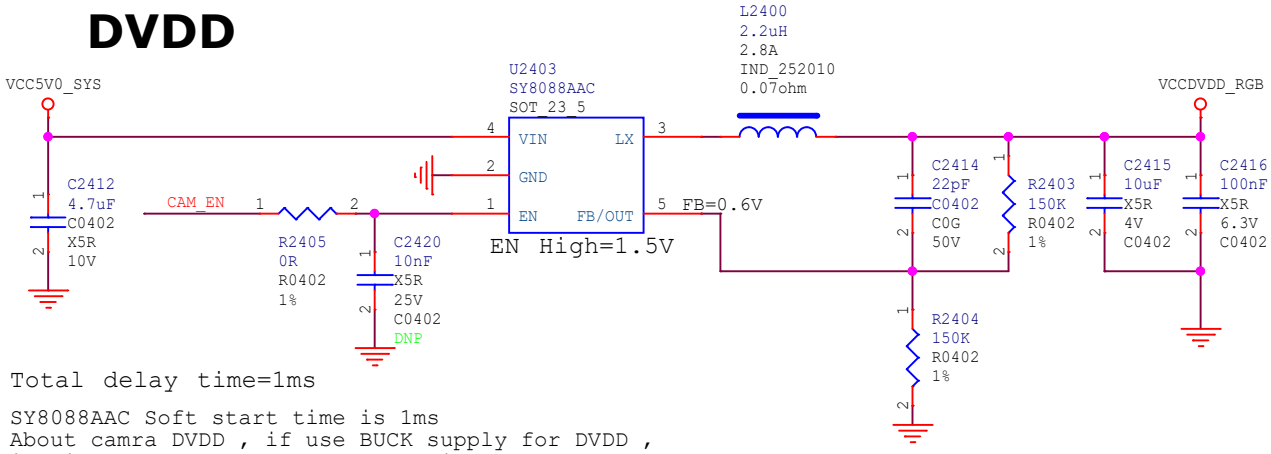
Rockchip 瑞芯微电子 Rockchip Electronics Co., Ltd

Project:	RV1126_RV1109_IPC_ENTRANCEGATE
File:	23.Discrete Power for System
Date:	Monday, January 25, 2021
Rev:	V1.3
Designed by:	Yanhong.Li
Reviewed by:	<Checker>
Sheet:	23 of 54

Discrete Power for Camera

CAM_EN

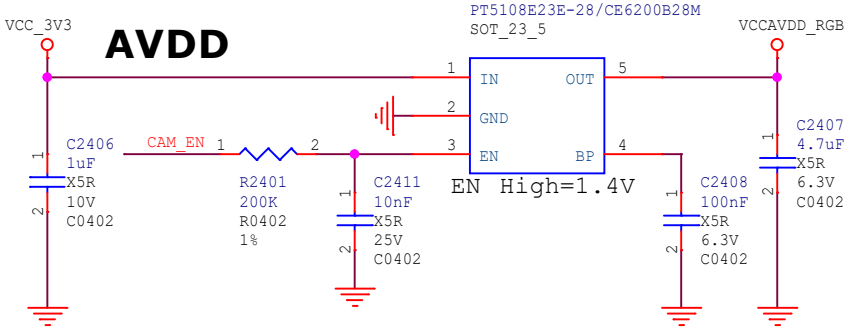
DVDD



Total delay time=1ms

SY8088AAC Soft start time is 1ms
About camra DVDD , if use BUCK supply for DVDD ,
it will cost less power consumption.

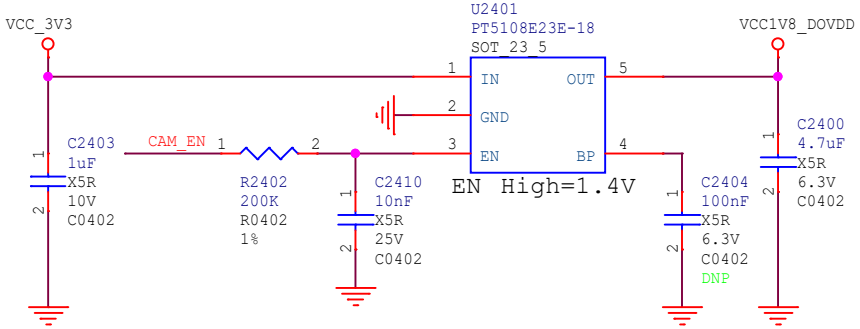
AVDD



RC delay time=1.02ms

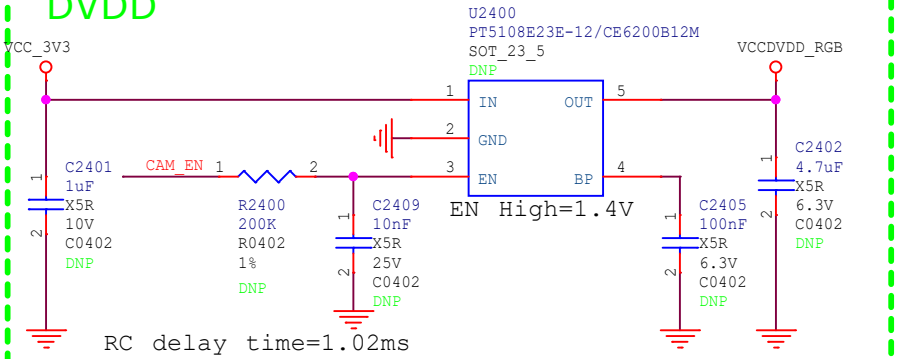
Total delay time=1ms

VCC1V8_DOVDD



RC delay time=1.02ms

Option: DVDD



RC delay time=1.02ms

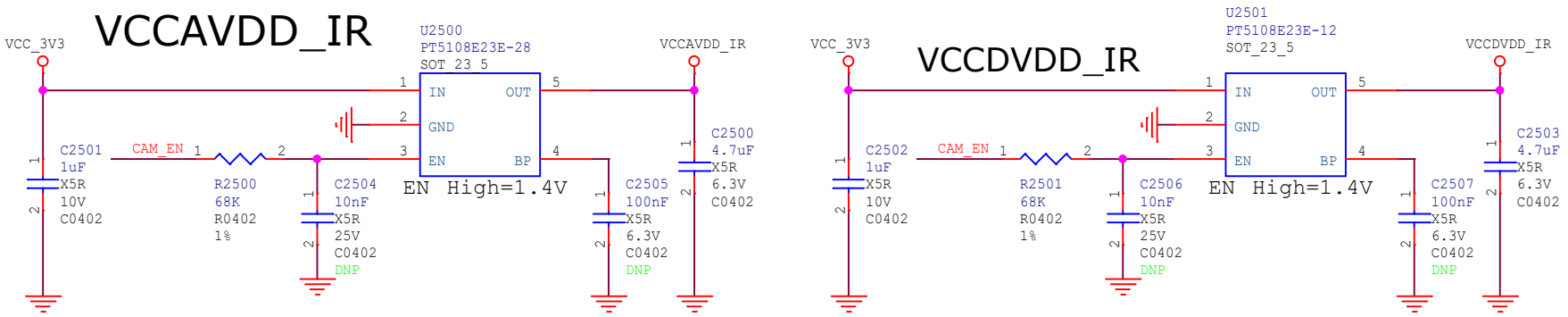
NOTE:
It's recommended to use DCDC for the DVDD and AVDD of camera for saving power consumption of battery solution.

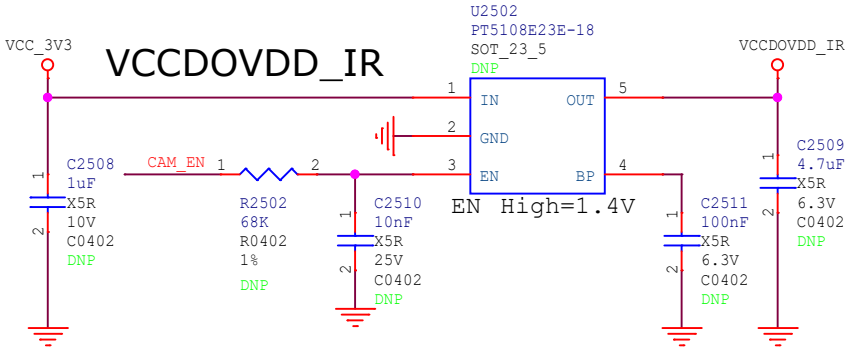
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	Discrete Power for Camera				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	24 of 54

Entrance Gate Solution:
Power of IRCamera

CAM_EN

NOTE:
The power on sequence is adjusted according to the camera.

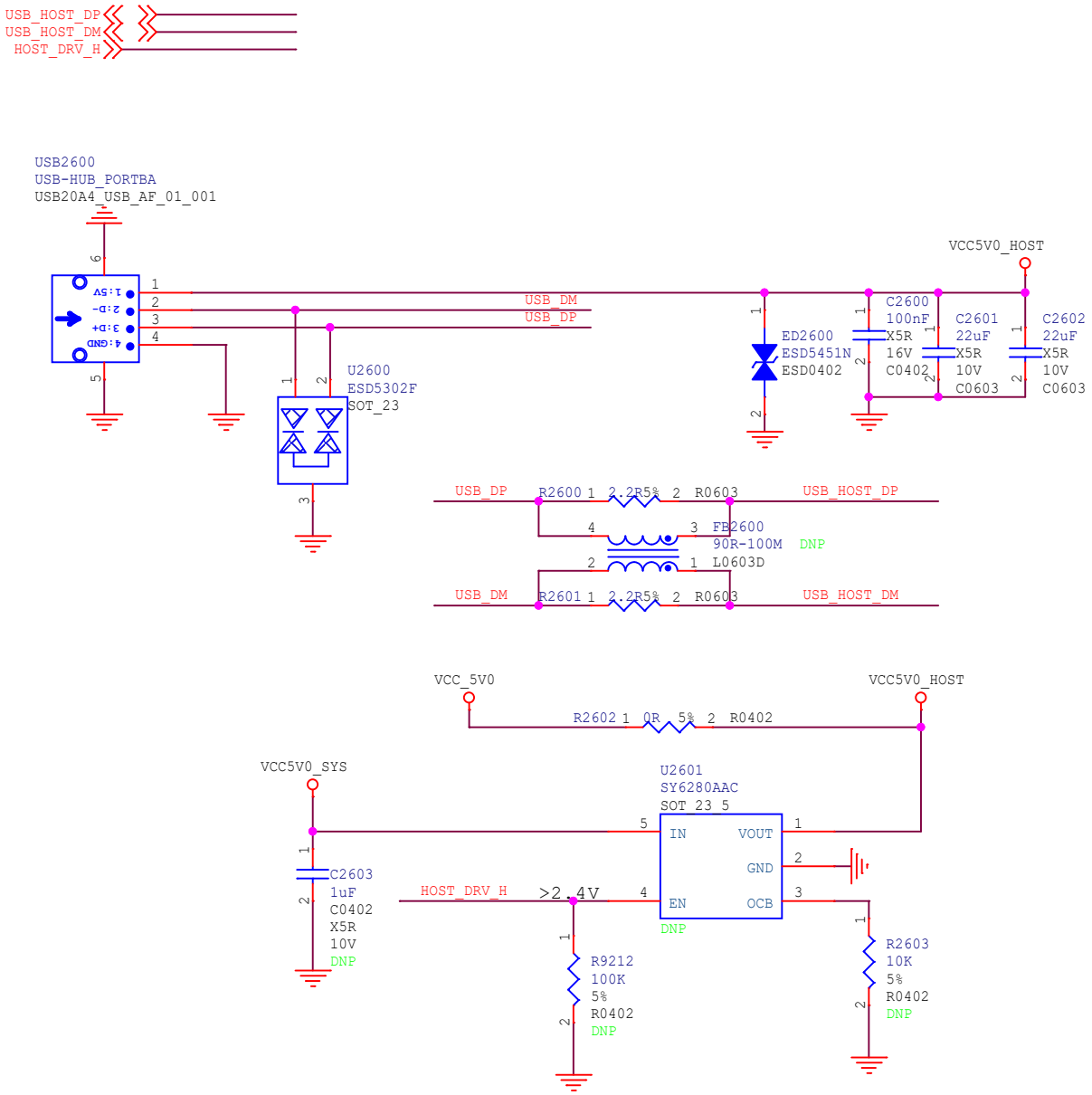




OPTION:
It is used for the camera mudules that the power of DOVDD are separated.

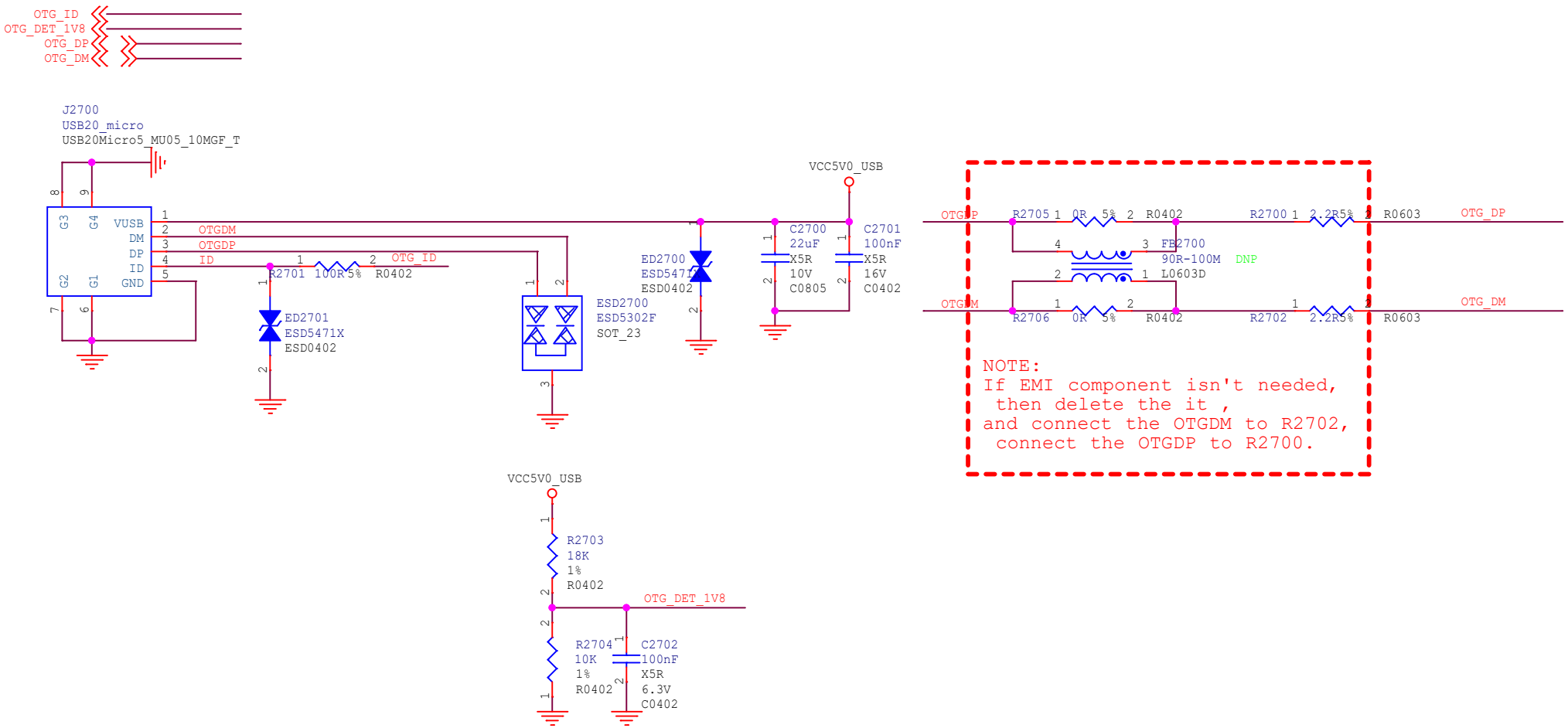
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	25.Power of IRCamera(GATE)				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	25 of 54

USB HOST



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	26.USB Host				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	26 of 54

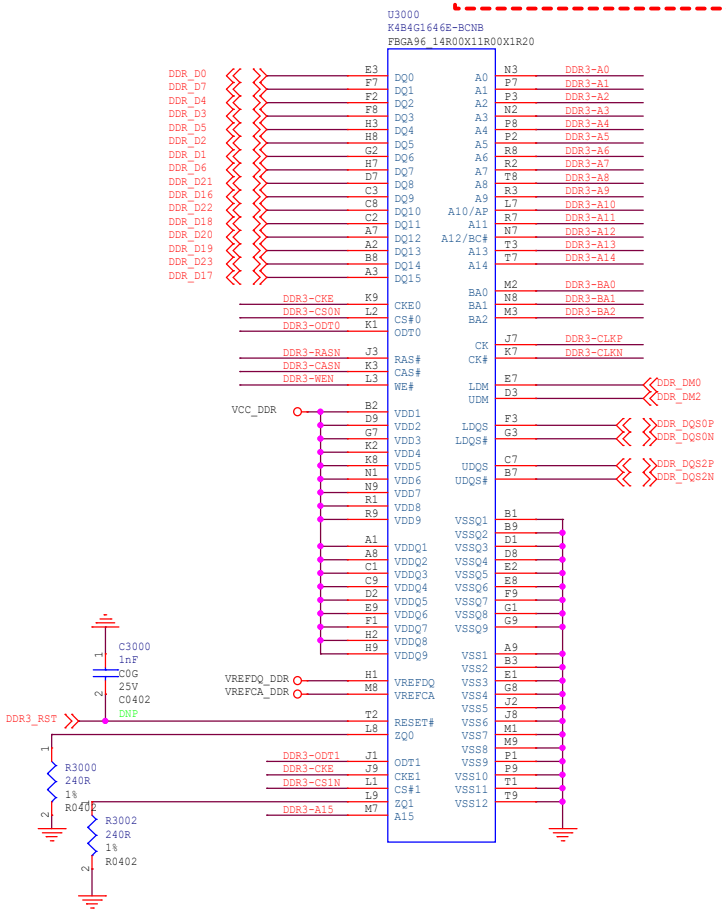
USB2.0 OTG

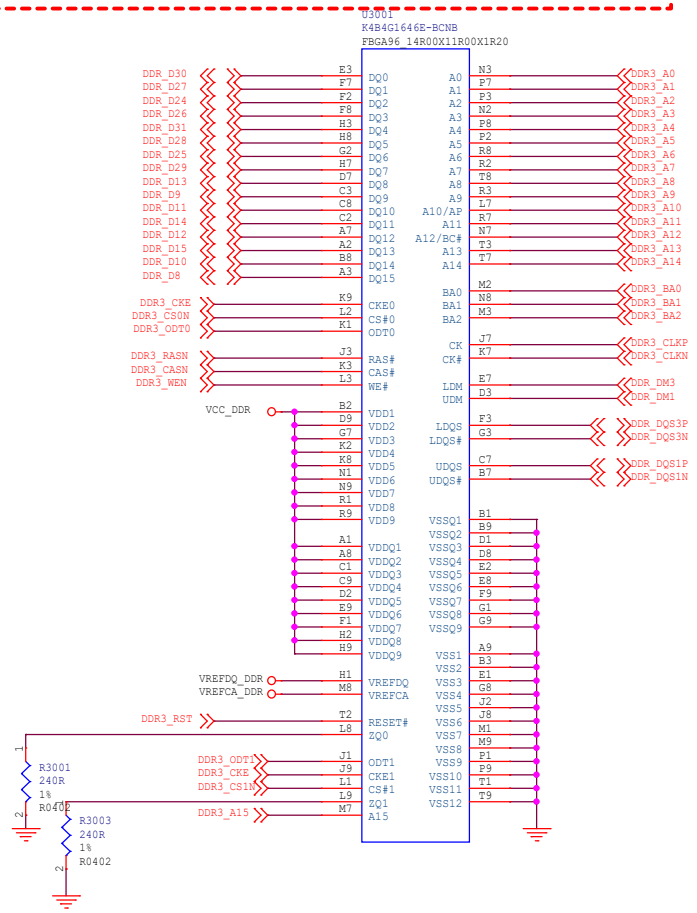


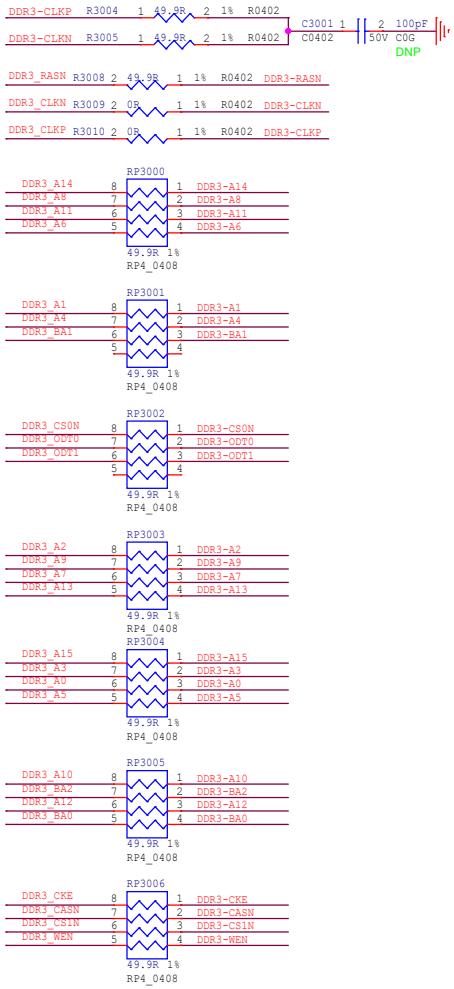
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	27.USB OTG				
Date:	Monday, January 25, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	27 of 54

DDR3/DDR3L 2x16bit

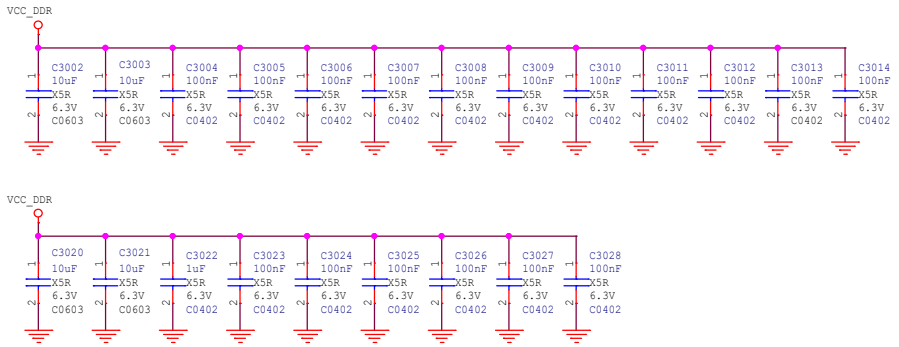
Note:
This is DDR template<RV1126_RV1109_Template_DDR3P216SD4_V10_20200619>. 4 layers PCB.
If only need one pcs DDR, please must use U3000(lane0,lane2).
If need other template, please apply to RK.

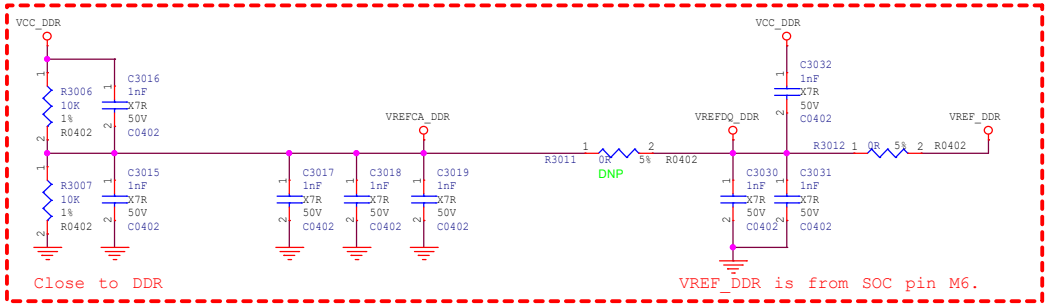






Note:All the Power filter capacitors should be placed close to the power pins of DDR3





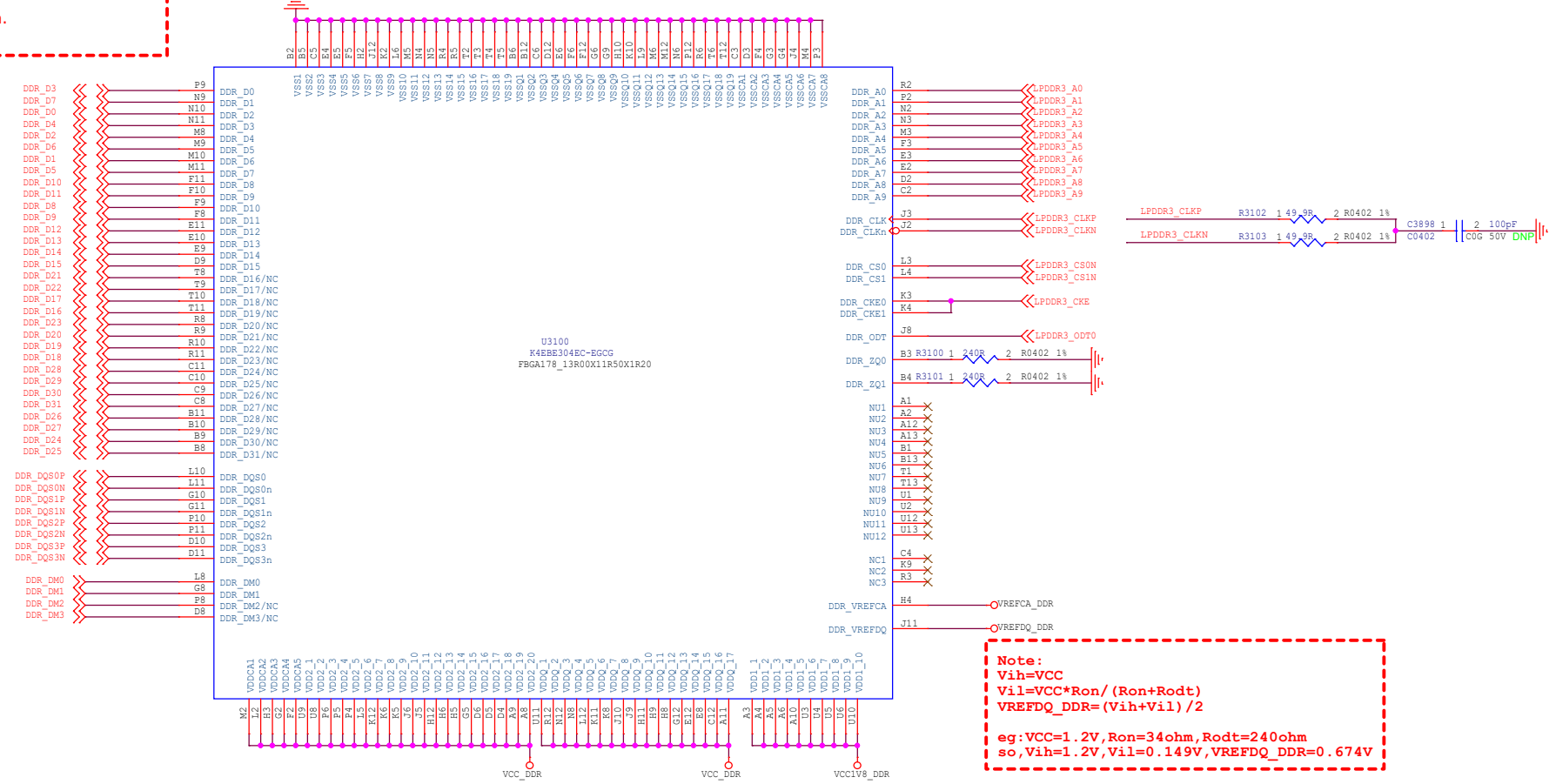
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	30.DRAM_DDR3_96P_2X16bit				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	28 of 54

LPDDR3 1x32bit

NOTE:
The sequence of DQ shall be done according to the template and shall not be adjusted or changed

Refer to the latest AVL for parts selection.

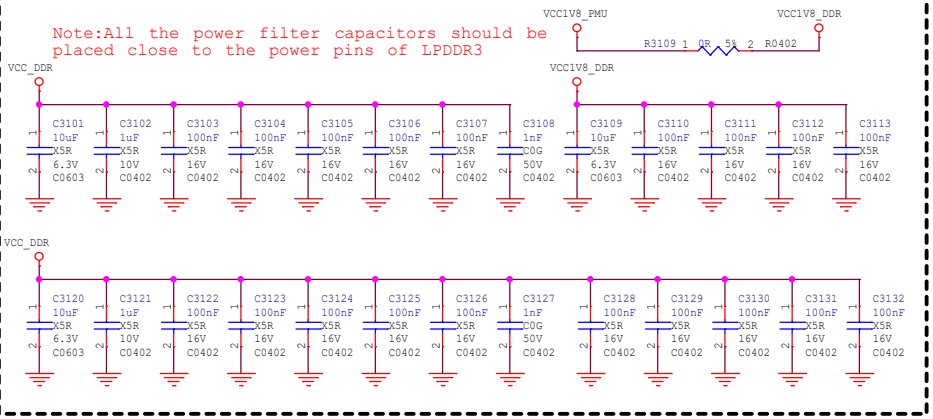
Note:
This is DDR template<RV1126_RV1109_Template_LP3S178P132SD6_V10_20200325>. Six layers PCB.

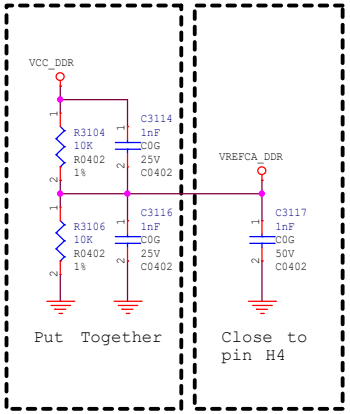


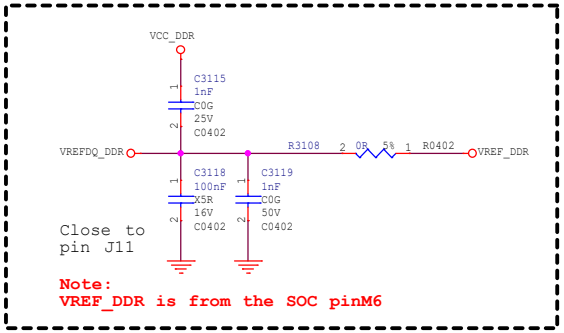
Note:
Vih=VCC
Vil=VCC*Ron/(Ron+Rodt)
VREFDQ_DDR=(Vih+Vil)/2

eg:VCC=1.2V,Ron=34ohm,Rodt=240ohm
so,Vih=1.2V,Vil=0.149V,VREFDQ_DDR=0.674V

Note:All the power filter capacitors should be placed close to the power pins of LPDDR3







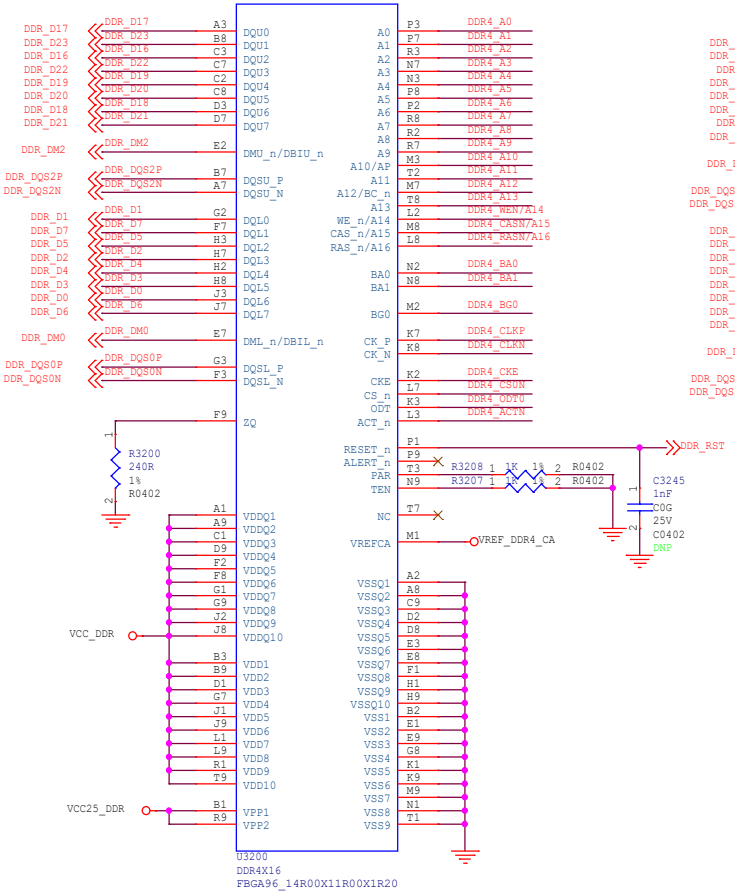
Note:
VREF_DDR is from the SOC pinM6

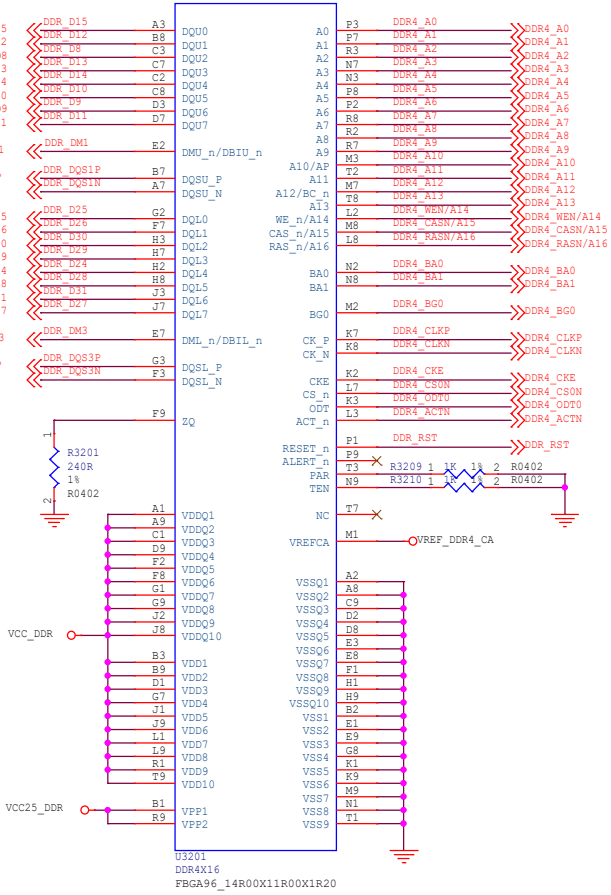
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	31. DRAM_LPDDR3_32 bit				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	29 of 54

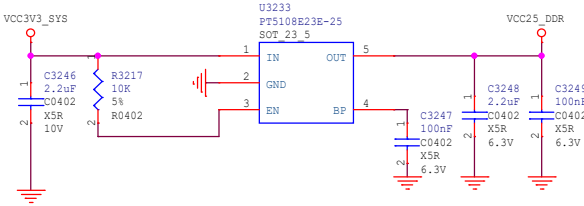
DDR4 2x16bit

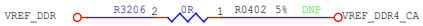
NOTE:
The sequence of DQ shall be done according to the template and shall not be adjusted or changed
Refer to the latest AVL for parts selection.

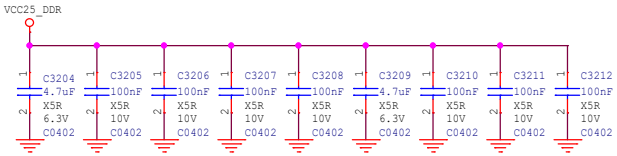
Note:
This is DDR template<RV1126_RV1109_Template_DDR4P216DD6_V10_20200325>.Six layers PCB.
If only need one pcs DDR, please must use U3200(lane0,lane2).

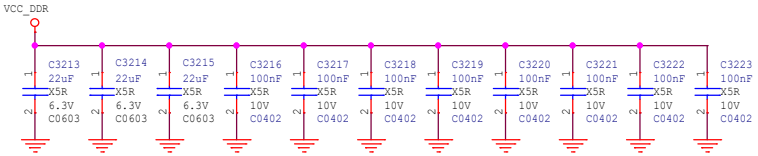


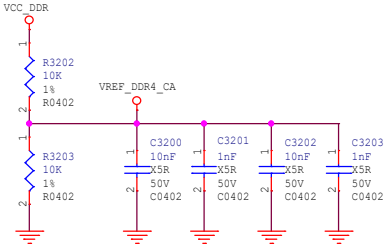


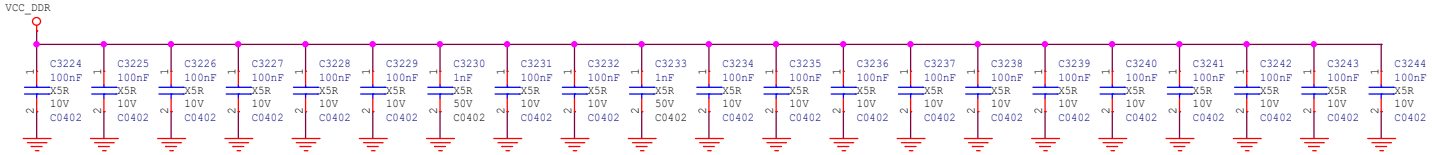










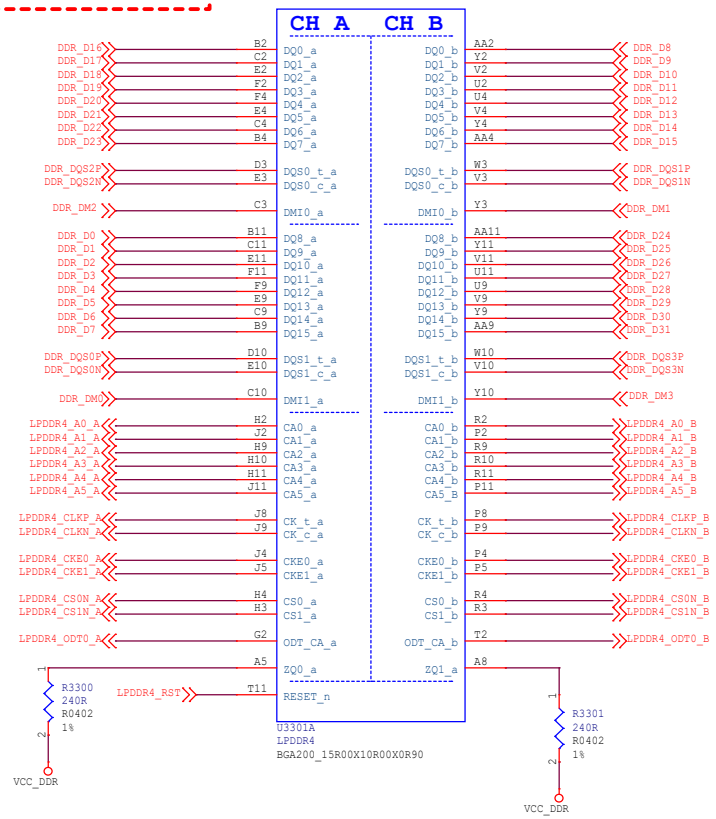


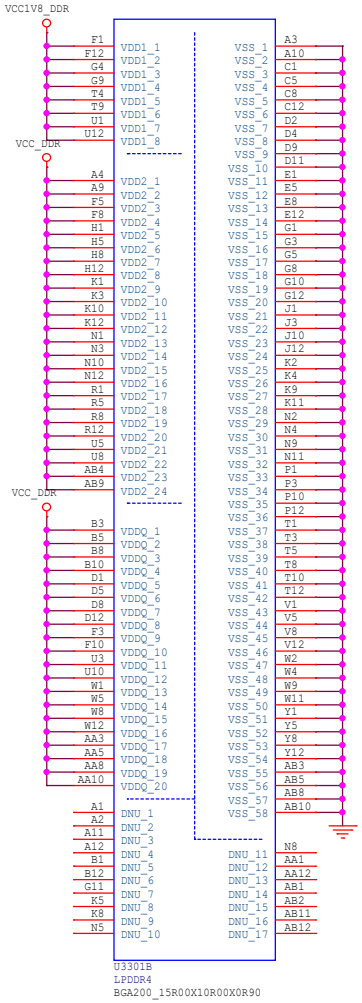
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	31. DRAM_LPDDR3_32 bit				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	30 of 54

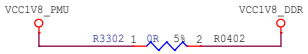
LPDDR4 1x32bit

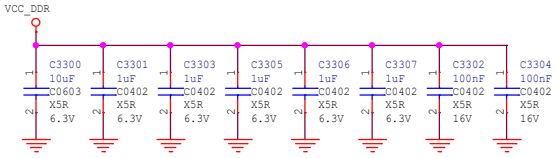
NOTE:
The sequence of DQ shall be done according to the template and shall not be adjusted or changed
Refer to the latest AVL for parts selection.

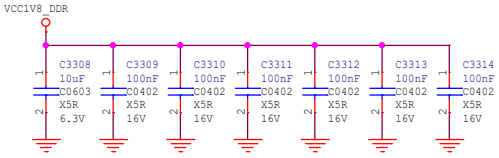
Note:
This is DDR template<RV1126_RV1109_Template_LP4S200P132SD6>. Six layers PCB.
If only need one pcs DDR, please must use U3200(lane0,lane2).

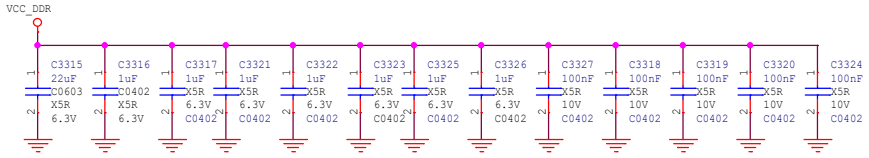








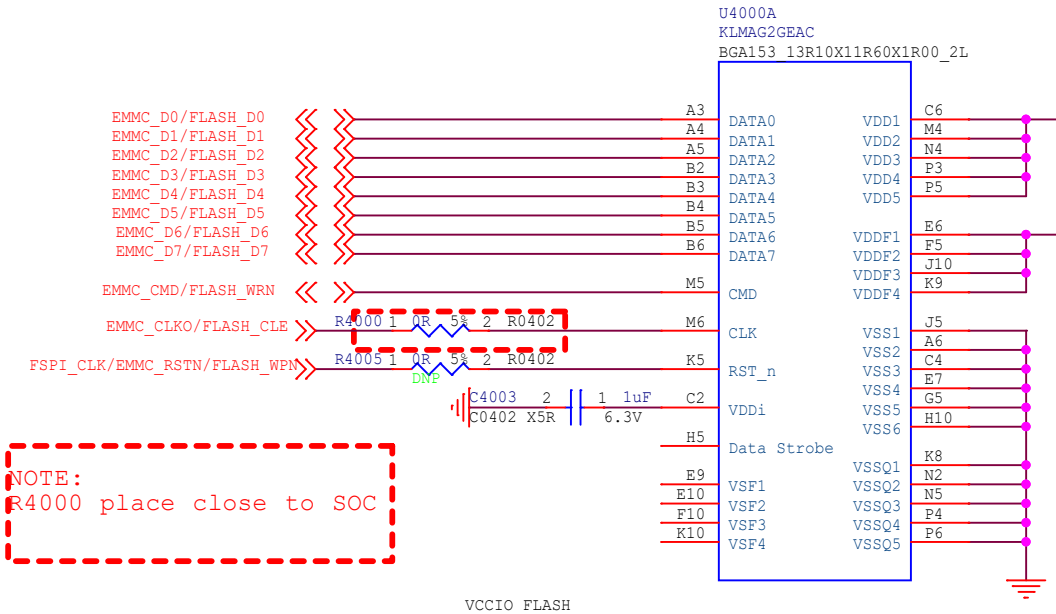




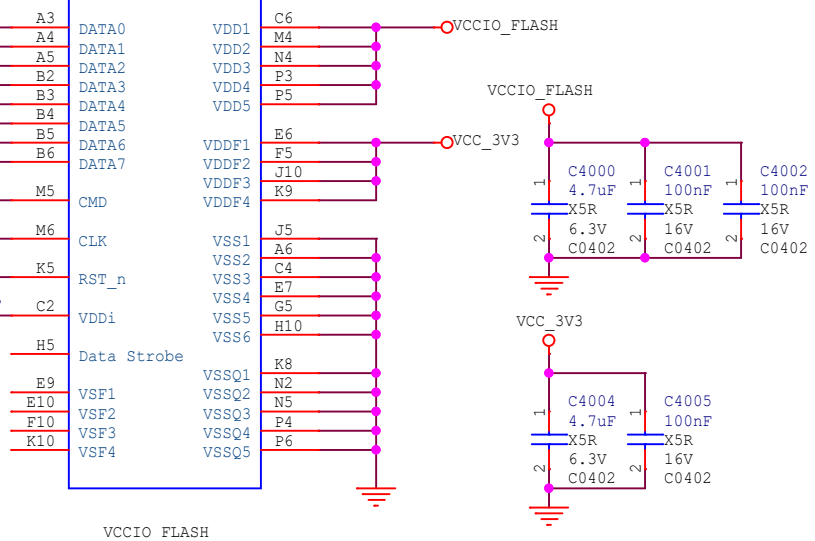
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	33.DRAM_LPDDR4_32 bit				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	31 of 54

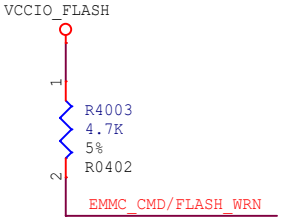
eMMC

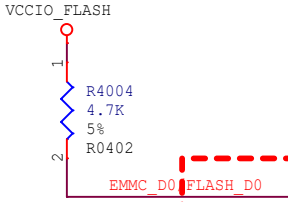
NOTE:
Refer to the latest AVL for parts selection.
NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.

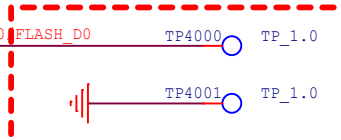


NOTE:
R4000 place close to SOC

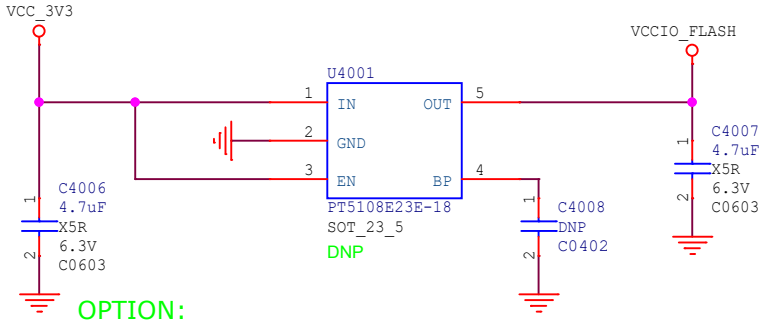




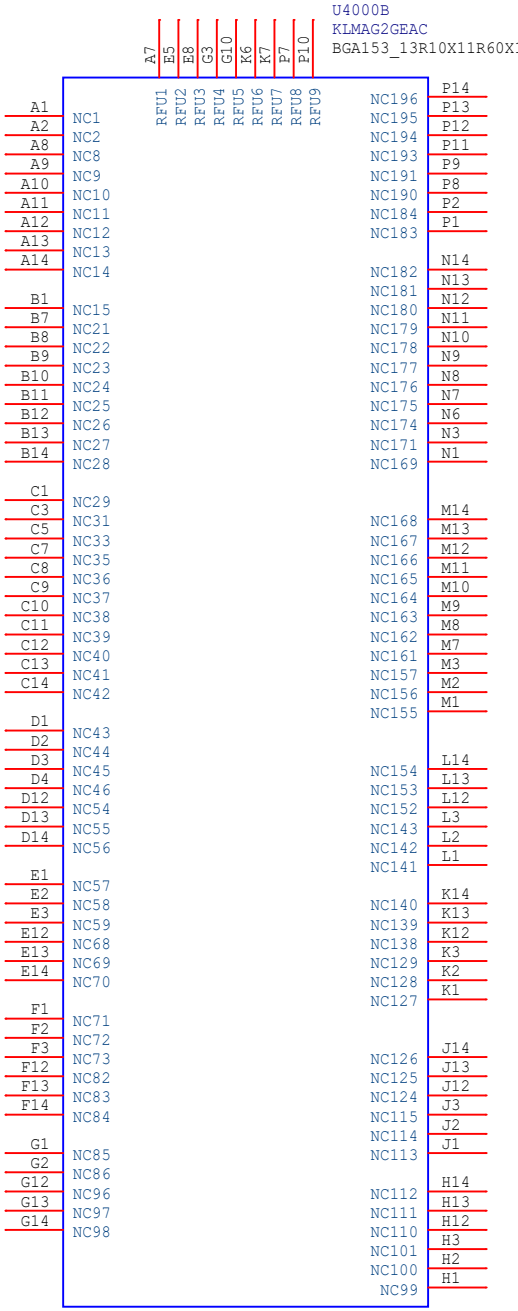




NOTE:
Reserve testpoint for firmware update,
In the power on phase, if FLASH_D0= 0V,
the system will enter the maskROM mode



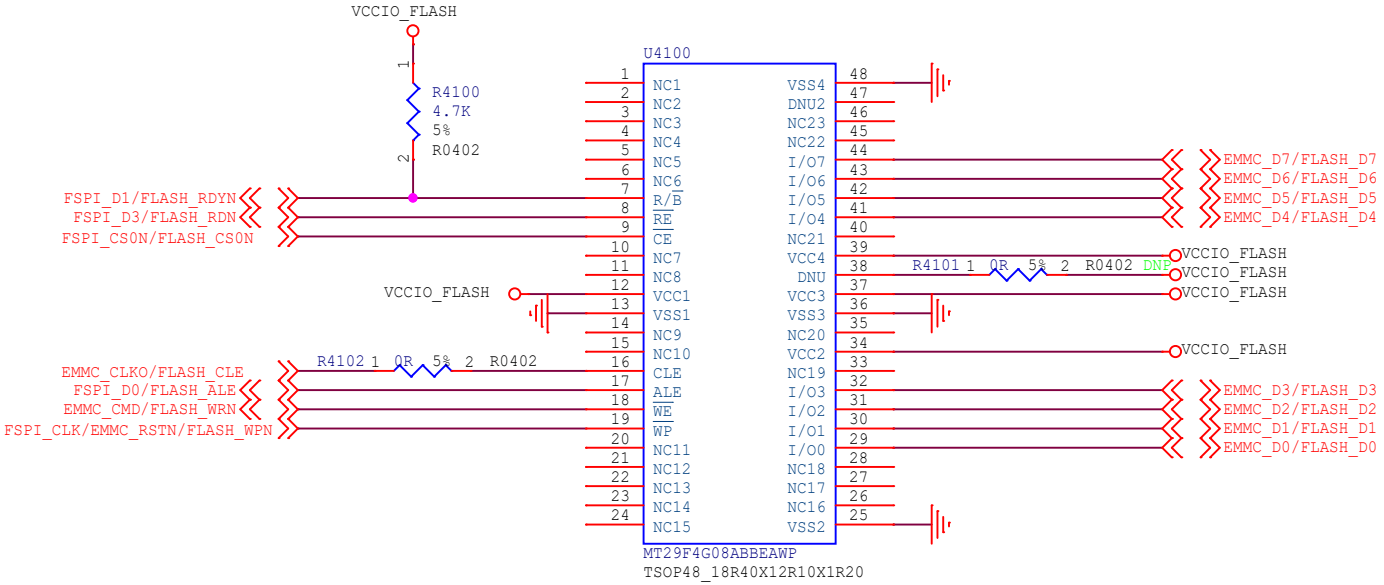
OPTION:
If EMMC peak current > 300mA,
please use LDO supply

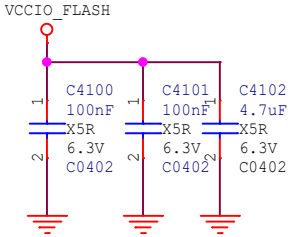


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	40.Flash-eMMC Flash				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	32 of 54

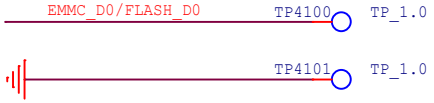
NAND FLASH

NOTE:
Refer to the latest AVL for parts selection.
Only support SLC NAND





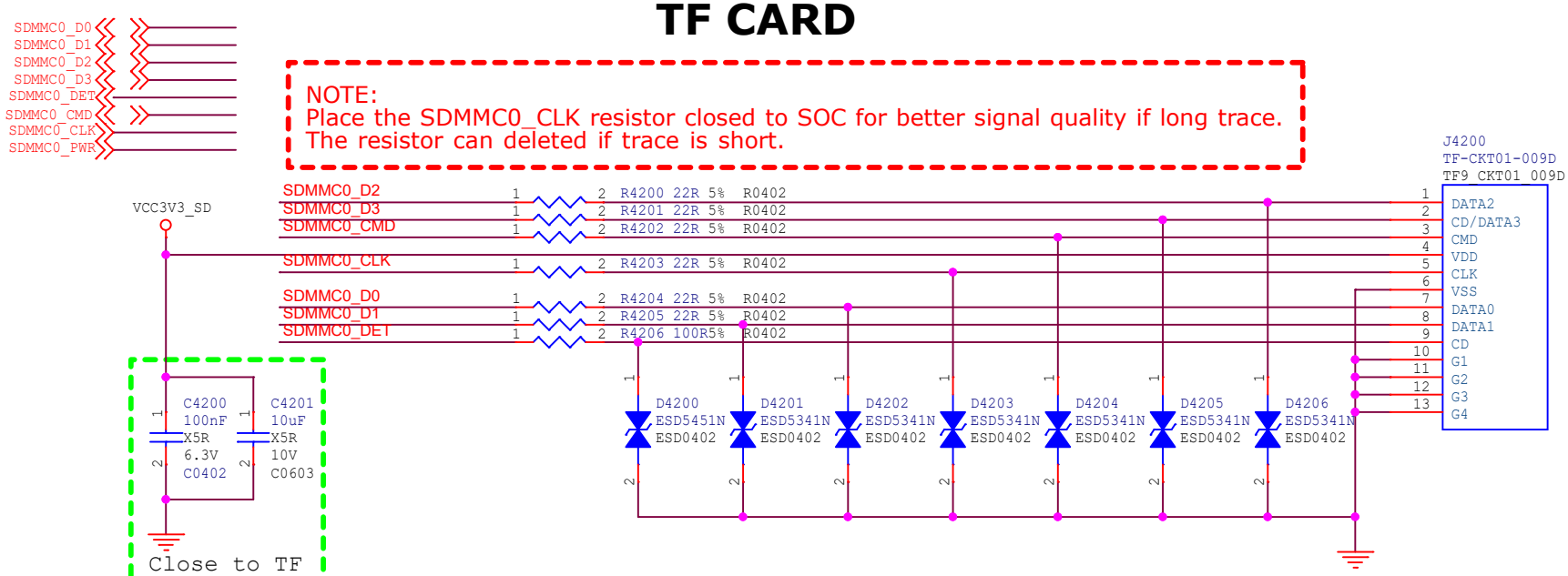
NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.

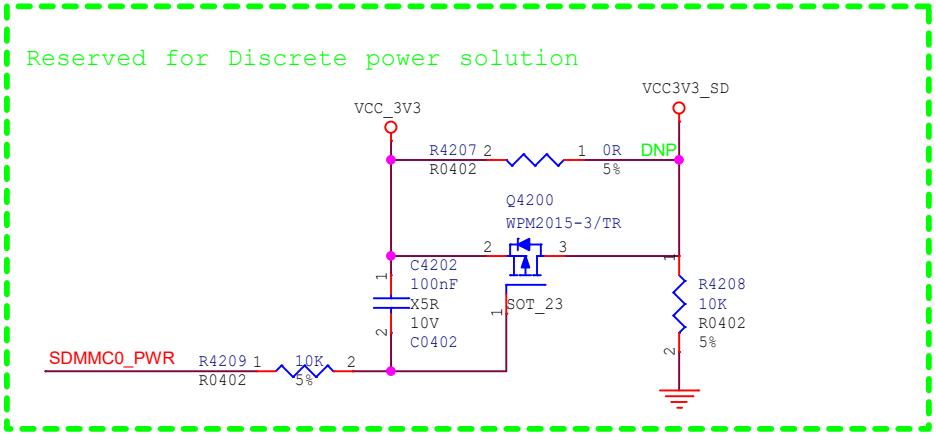


NOTE:
Reserve testpoint for firmware update,
In the power on phase, if FLASH_D0= 0V,
the system will enter the maskROM mode

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	41.Flash-Nand Flash				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	33 of 54

TF CARD

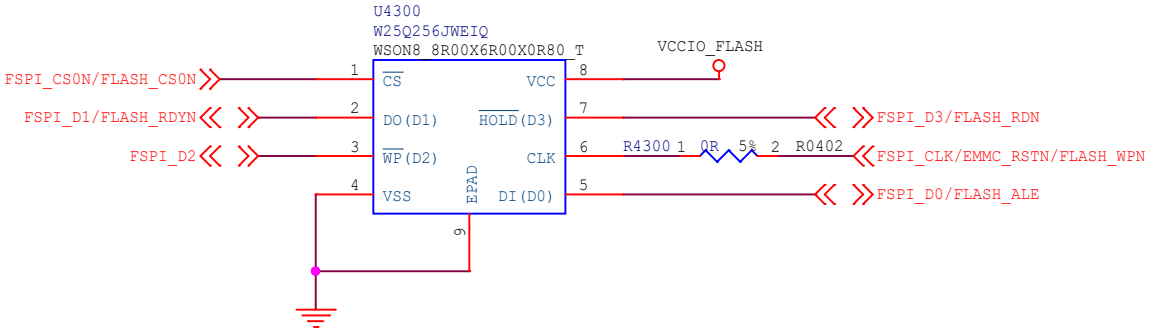


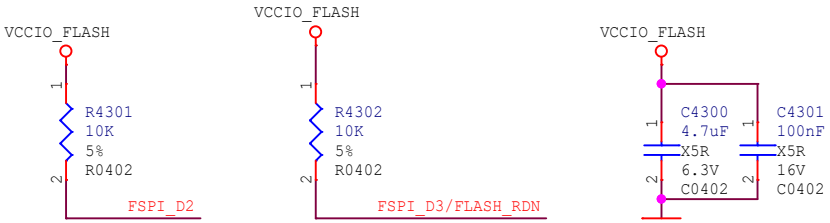


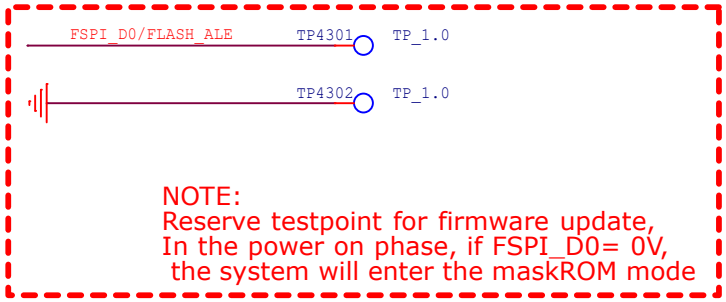
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	42.Flash-Micro-SD Card				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	34 of 54

SPI_Flash

NOTE:
Refer to the latest AVL for parts selection.

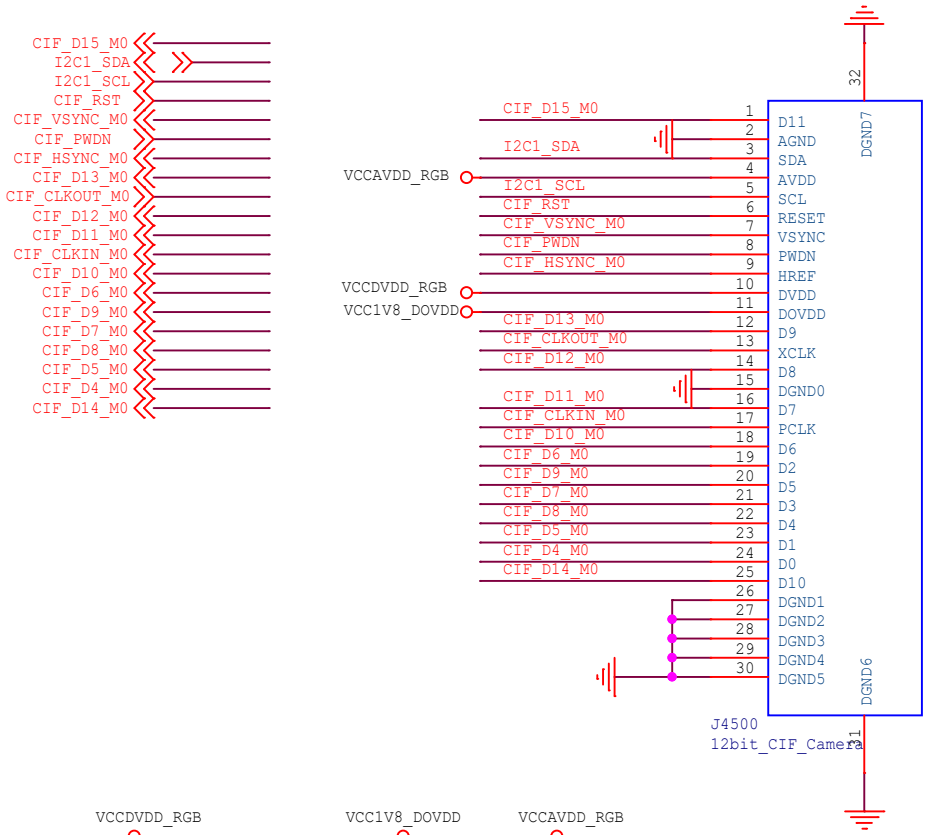






Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	43.Flash-SPI Flash				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	35 of 54

CIF Camera Interface



Correspondence CIF data and BT1120/12bit/10bit/8bit CIF				
16bit CIF data	BT1120	12bit CIF camera	10bit CIF camera	8bit CIF camera
CIF_D0	BT1120_D0			
CIF_D1	BT1120_D1			
CIF_D2	BT1120_D2			
CIF_D3	BT1120_D3			
CIF_D4	BT1120_D4	D0		
CIF_D5	BT1120_D5	D1		
CIF_D6	BT1120_D6	D2	D0	
CIF_D7	BT1120_D7	D3	D1	
CIF_D8	BT1120_D8	D4	D2	D0
CIF_D9	BT1120_D9	D5	D3	D1
CIF_D10	BT1120_D10	D6	D4	D2
CIF_D11	BT1120_D11	D7	D5	D3
CIF_D12	BT1120_D12	D8	D6	D4
CIF_D13	BT1120_D13	D9	D7	D5
CIF_D14	BT1120_D14	D10	D8	D6
CIF_D15	BT1120_D15	D11	D9	D7

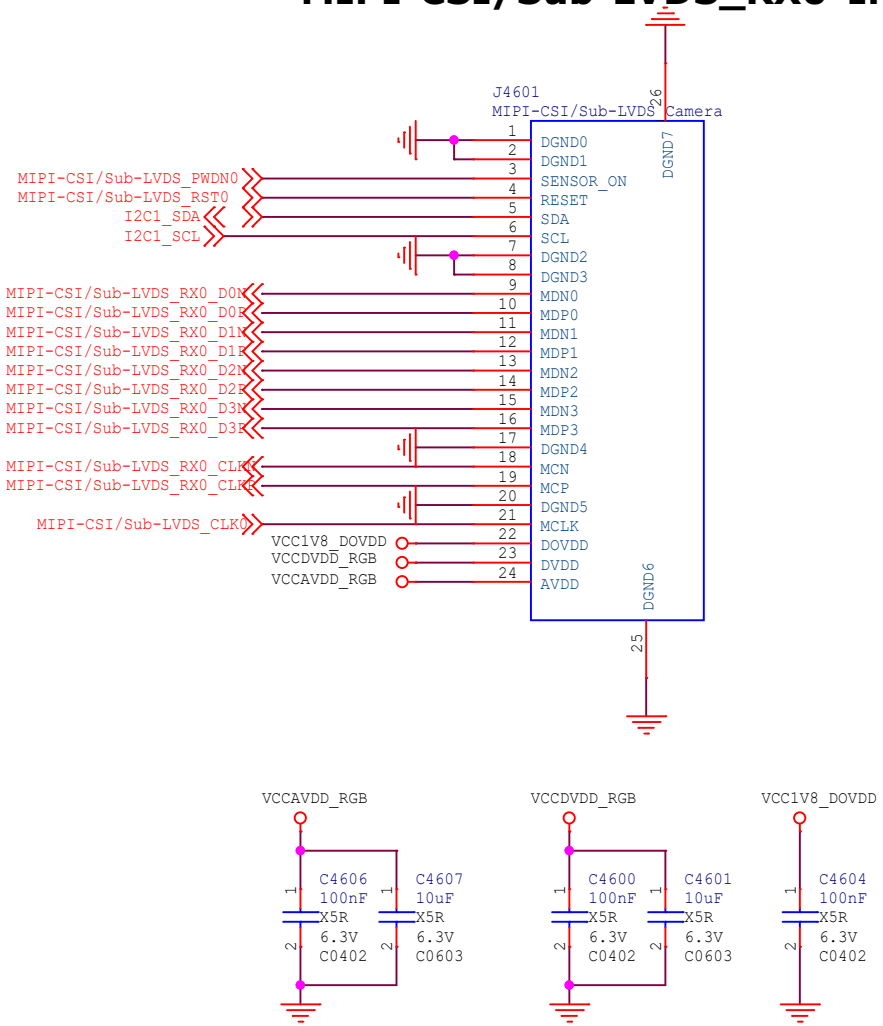
NOTE:
According to the current of the actual camera module, evaluate whether the current output by LDO can meet the requirement of two cameras using at the same time. If not, please add LDO to supply power

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	45.VI-Camera_CIF				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	36 of 54

IPC Splution:
LVDS interface and mipicsi interface share pins,
only one of them can be selected at a time.

NOTE:
1) According to the current of the actual camera module, evaluate whether the current output by LDO can meet the requirement of two cameras using at the same time.
2) If not, please add LDO to supply power.
3) If the I2C addresses of the two cameras are the same, use another set of I2C.
4) Imx307, imx327 sensors must use LVDS interface, and use 4 lanes, HDR frame rate can meet the requirements

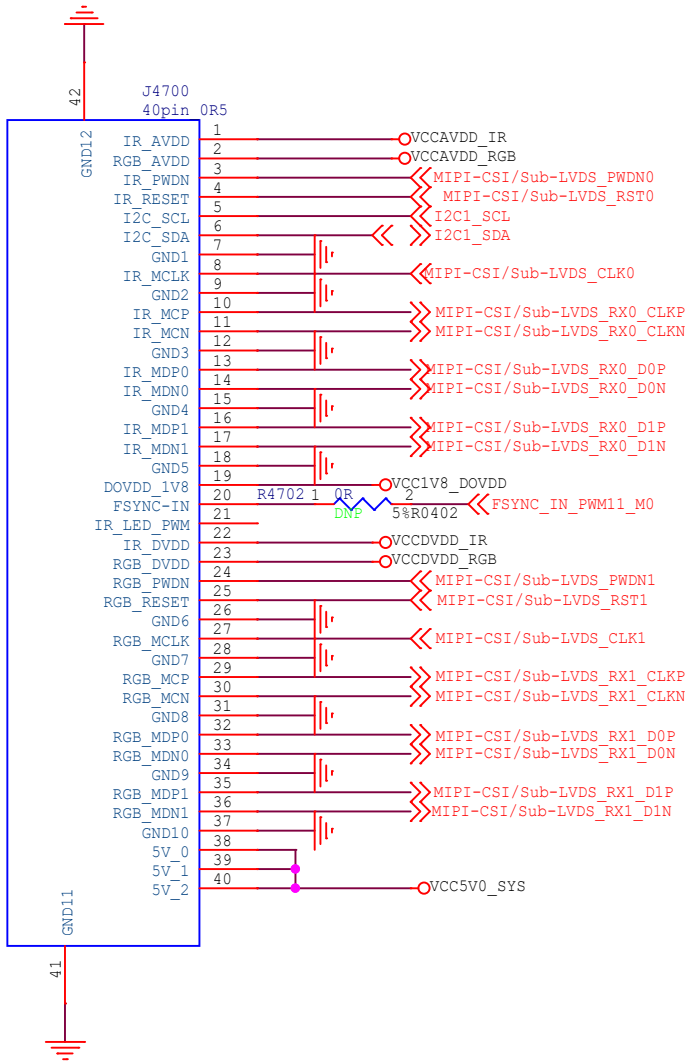
MIPI-CSI/Sub-LVDS_RX0 Interface



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	46.VI-Camera_MIPI-CSI/Sub-LVDS				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	37 of 54

Entrance Gate Solution

2 lane Dual MIPI Camera



NOTE:
1. IMX307/IMAX 327 must use LVDS interface.

2.Pls. pay attention to the I2C address of sensors,
don't use the same I2C address for two sensors.

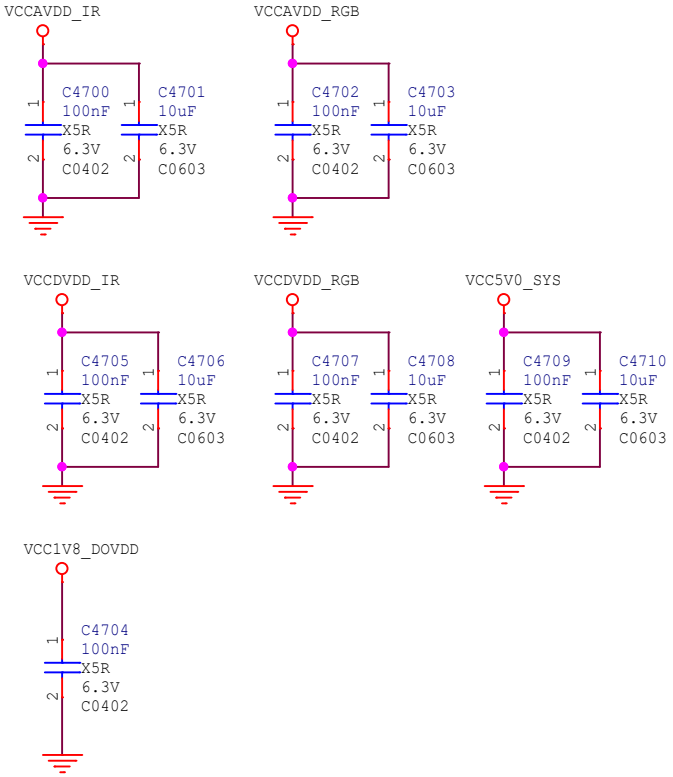
3.About the pin FYNC_IN, pls. connect 0R resistor first,
and then connect to the PWM pin of soc.

4. LVDS0 interfaces and MIPI_CSI_RX0 interfaces are mutiplex.
The two interfaces cannot be used at the same time.
It is the same rule for LVDS1 and MIPI_CSI_RX1.

5. If there are only two lanes need to used, pls.use lane0 and lane1.

6.The DOVDDs are combined for the sensor module recommended by RK,
such as OV2718+GC2053,IMX307+GC2053. But If anothor two sensor modules are used,
the DOVDDs are recommended to separate for the reason of power on sequence.
It is needed to refine the pins of dual camera module.

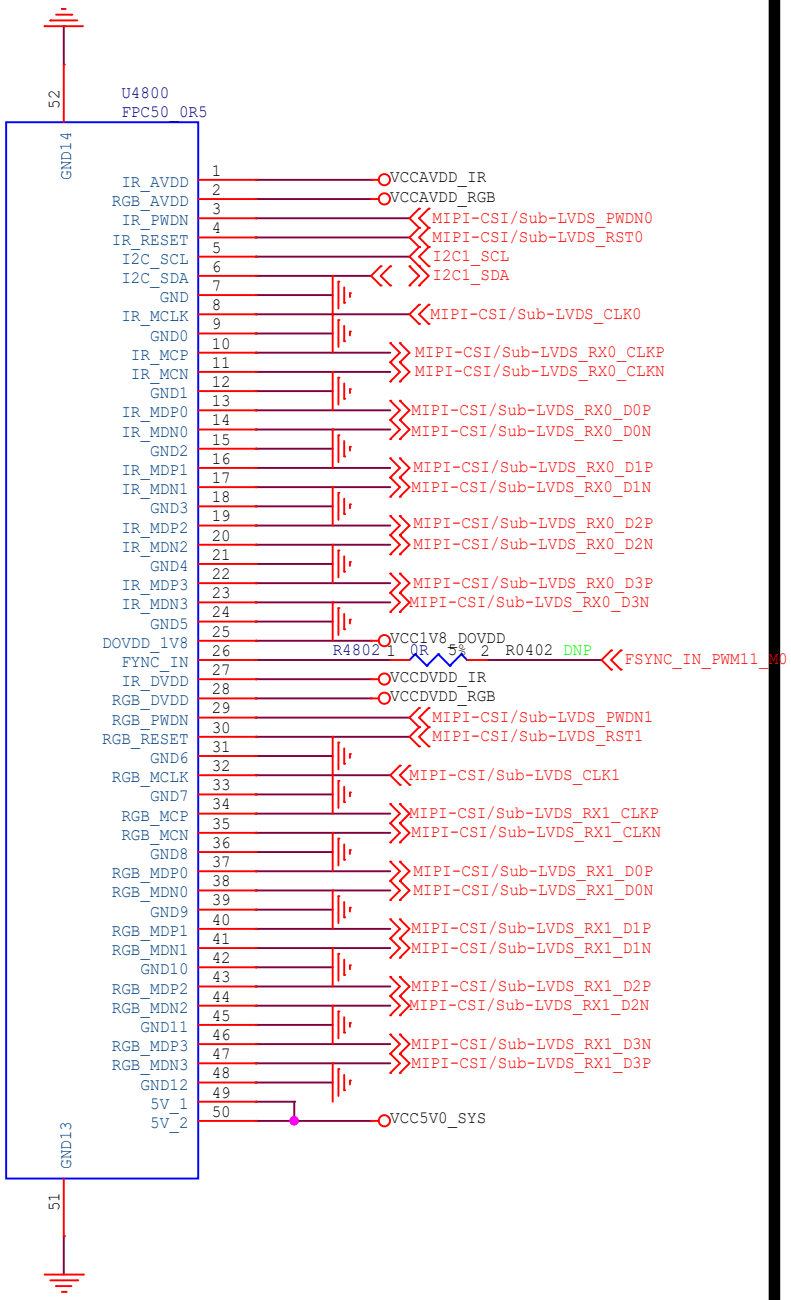
7. The AVDDs of IR camera and RGB camera are needed to supply power separatey.
It's same rule for DVDD.



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	47.Dual MIPI-CS Camera(IR+RGB)				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	38 of 54

Entrance Gate Solution

4 lane dual LVDS/MIPI Camera



NOTE:

1. IMX307/IMAX 327 must use LVDS interface.

2. Pay attention to the I2C address of sensors, don't use the same I2C address for two sensors.

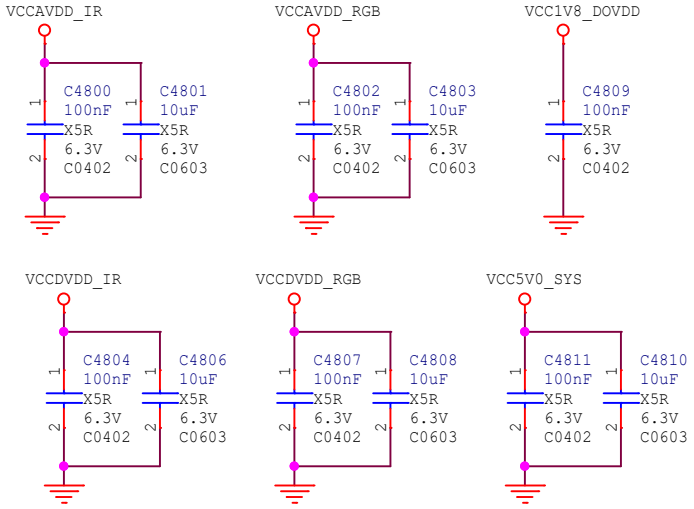
3. About the pin FYNC_IN, pls. connect 0R resistor first, and then connect to the PWM pin of soc.

4. LVDS0 interfaces and MIPI_CSI_RX0 interfaces are mutiplex. The two interfaces cannot be used at the same time. It is the same rule for LVDS1 and MIPI_CSI_RX1.

5. If there are only two lanes need to used, pls.use lane0 and lane1.

6. The DOVDDs are combined for the sensor module recommended by RK, such as OV2718+GC2053, IMX307+GC2053. But If anothor two sensor modules are used, the DOVDDs are recommended to separate for the reason of power on sequence. It is needed to refine the pins of dual camera module.

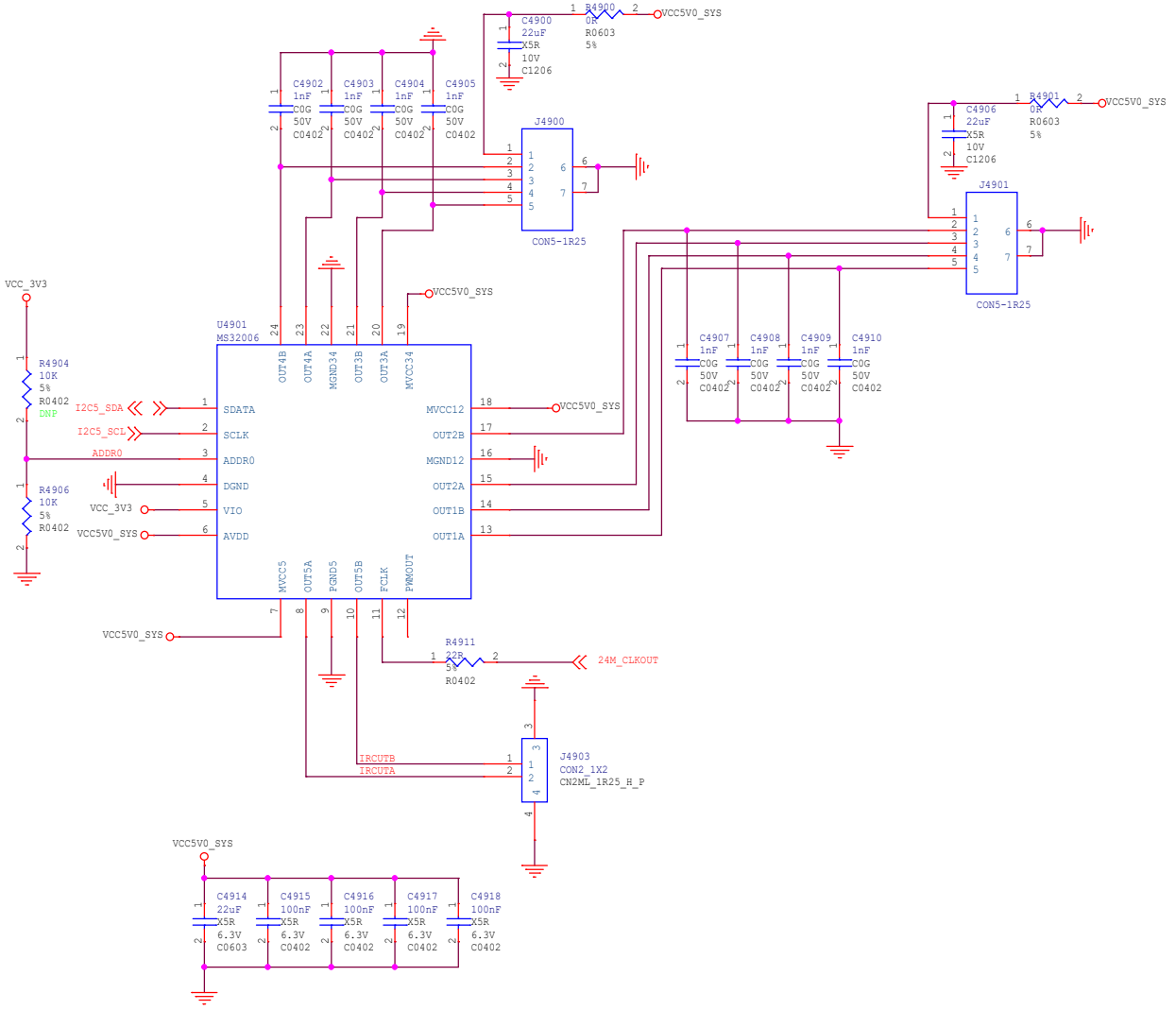
7. The AVDDs of IR camera and RGB camera are needed to supply power separatey. It's same rule for DVDD.



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	48.Dual Sub-LVDS Camera(IR+RGB)				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	39 of 54

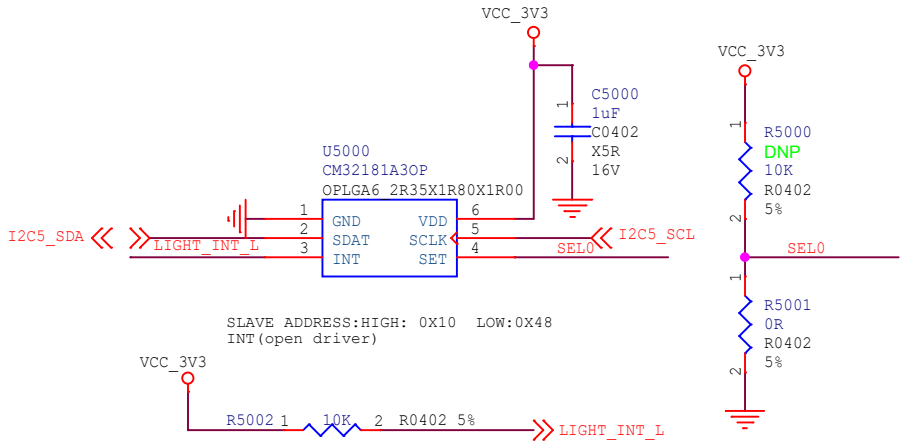
IPC Solution

IR Cut Driver PAN/TILT Driver



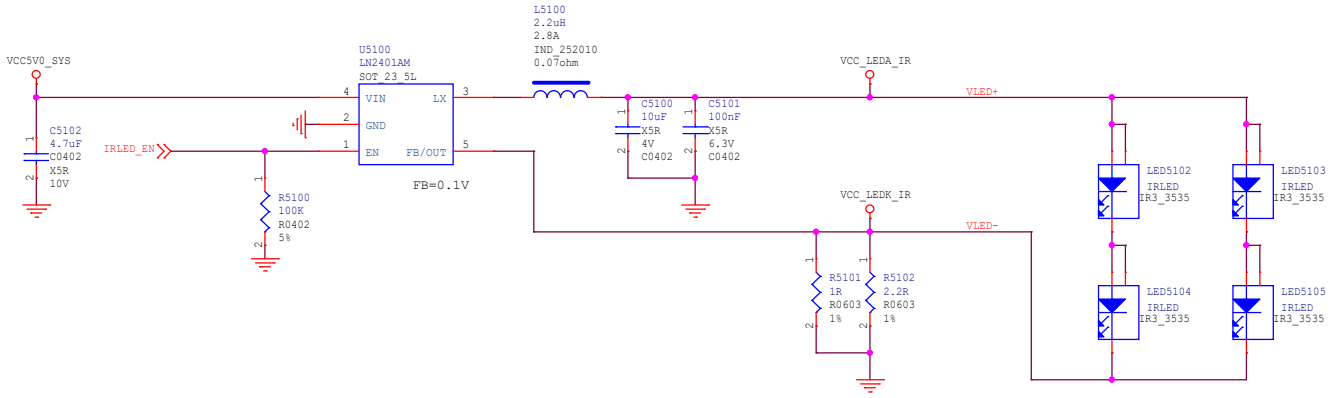
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	49.IRC/Motor Driver(IPC)				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	40 of 54

Light Sensor



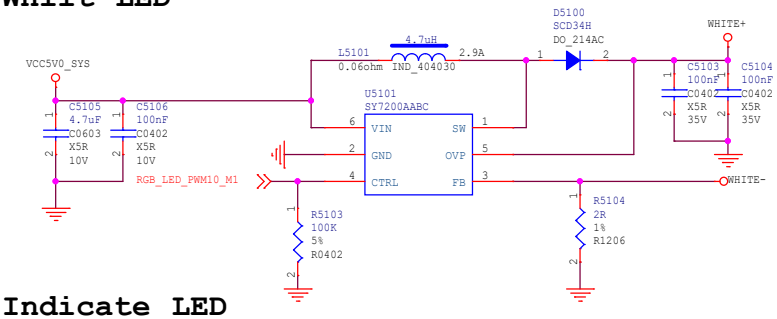
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	50. light sensor				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	41 of 54

IR Driver 850nm Vrf=1.3V



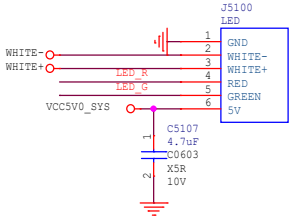
NOTE:
1. IR-LED select 850nm wavelength.
2. Angle of the LED is 90 degree.
3. The total driver current is 120mA for better effect.

Whilt LED



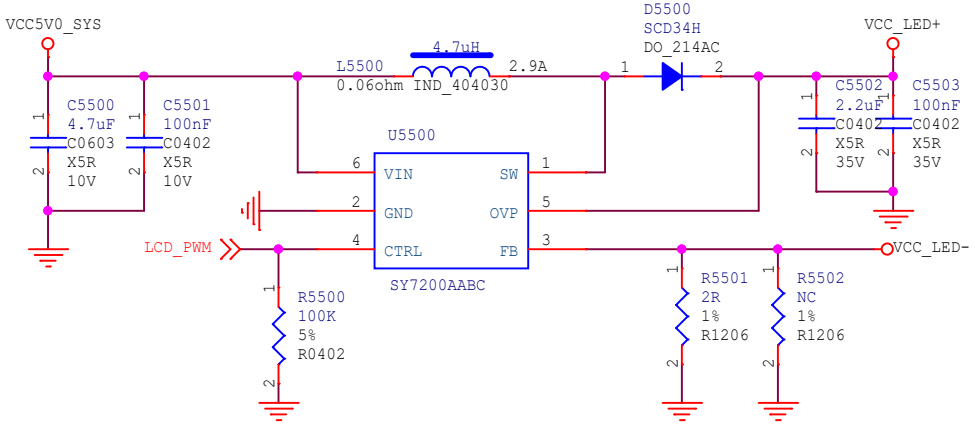
Indicate LED

LED Connector

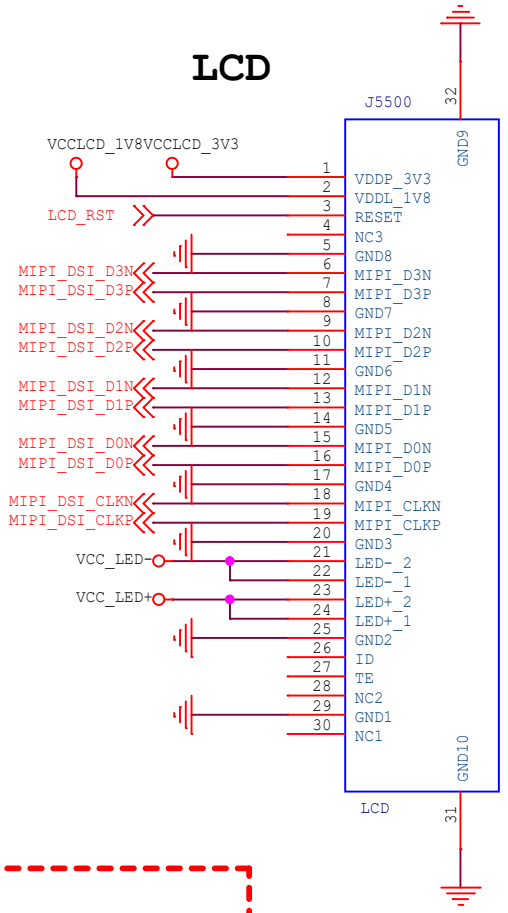


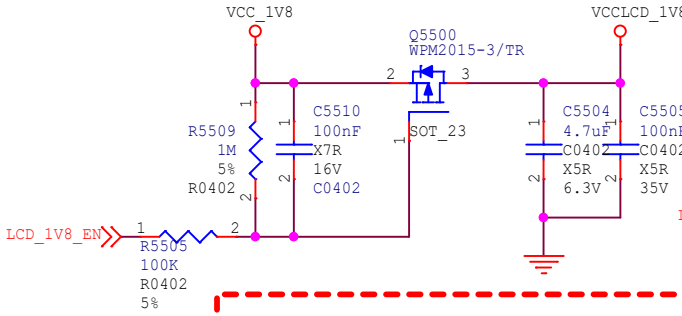
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	51.LED Driver				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	42 of 54

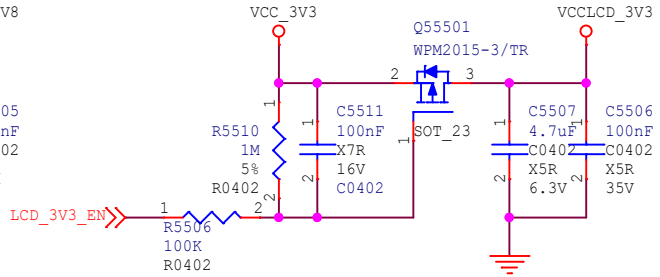
Entrance Gate Solution



LCD

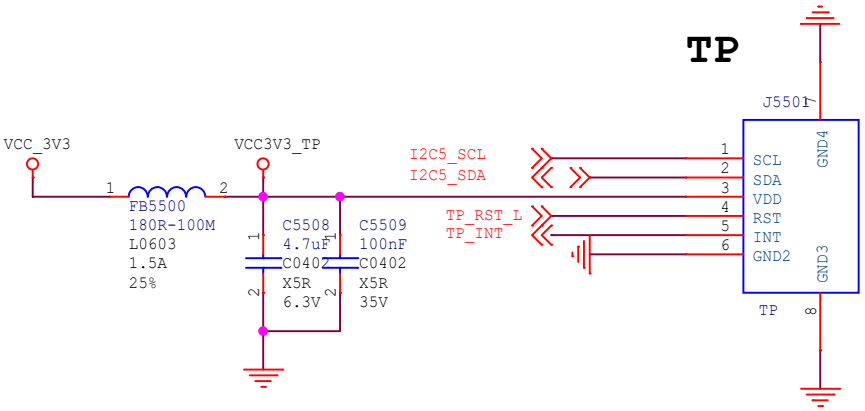






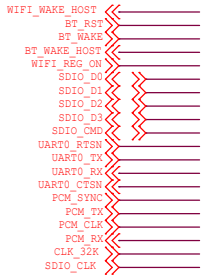
NOTE: The MOS and GPIO are used to control the time-sequence for some LCDs.
If there isn't TF card funtion, then the LDO9 of RK809-2 can supply power for VCCLCD_3V3.
Then the MOS control circuit can be deleted for VCCLCD_3V3.

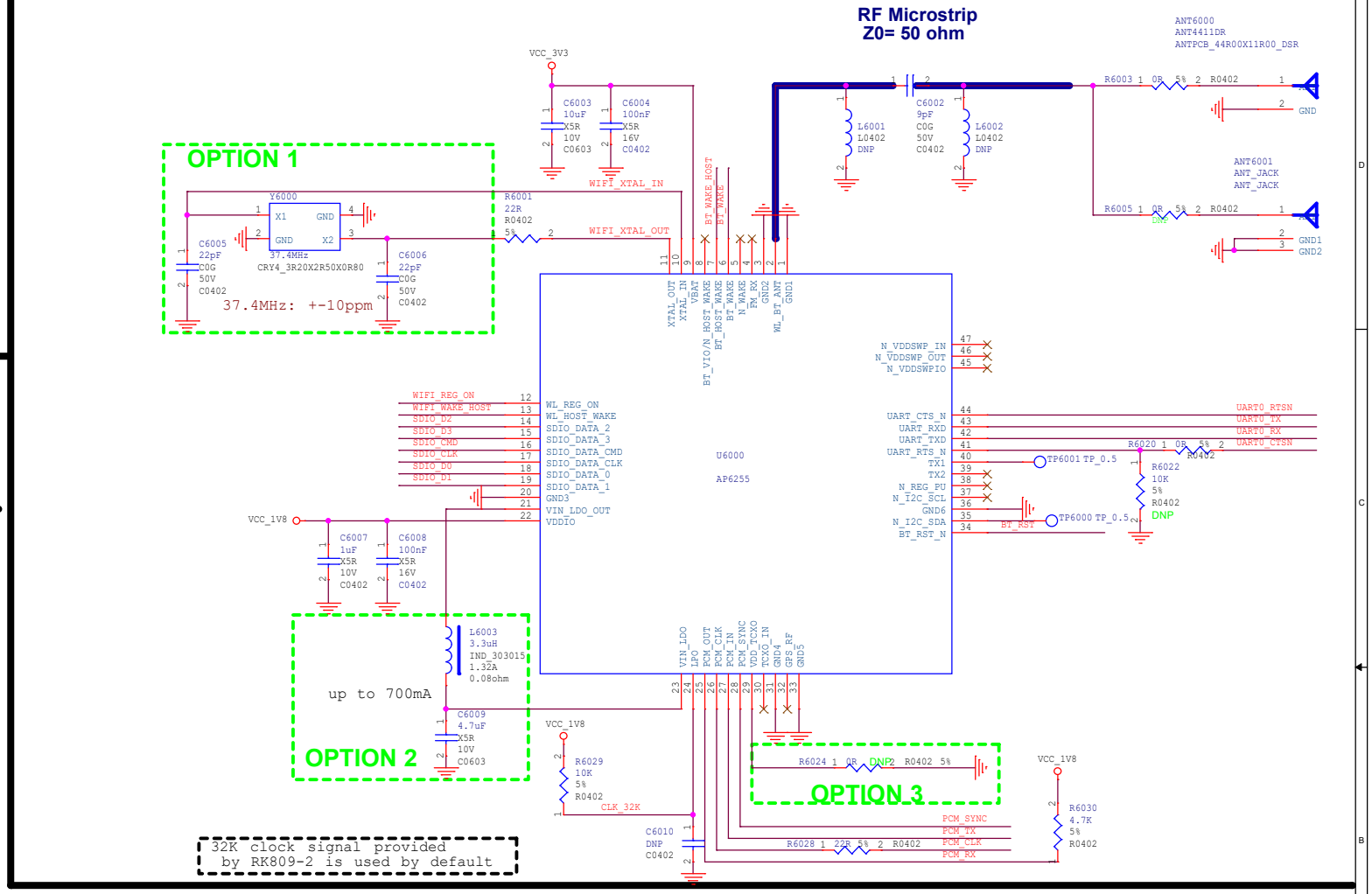
TP



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	55. LCD(GATE)				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	43 of 54

WIFI/BT Module





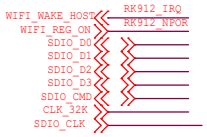
WIFI module		
Pin	AP6255	UWE5622
6	BT_WAKE	CHIP EN
7	BT_HOST_WAKE	AP_INT
12	WL_REG_ON	RST_N
13	WL_HOST_WAKE	SD_INT

Note:
Yes: option circuit be mounted
No: option circuit not be mounted

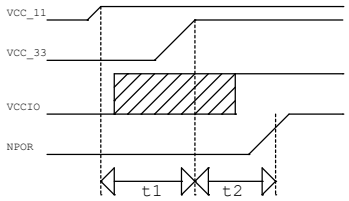
OPTION	WIFI				BT	Crystals	VCCIO_SDIO	OPTION1	OPTION2	OPTION3
	a	b/g/n	ac	5GHz						
AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71-3.63V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.63V	Yes	Yes	No
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.62-3.63V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0
RTL8189FTV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.63V	No	No	No
QCA9377 Module 8223A-SR	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No
UWE5622	Yes	Yes	Yes	Yes	5.0	Module Integrated	1.62-1.98V	No	No	No

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RV1126_RV1109_IPC_ENTRANCEGATE		
File:	60.WIFI/BT-SDIO_1T1R+UART		
Date:	Wednesday, January 20, 2021	Rev:	V1.3
Designed by: Yanhong.Li	Reviewed by: <Checker>	Sheet:	44 of 54

WIFI RK912



Power Sequence



t1>=1ms, t2>=1ms

Power Consumption

State	VCCIO	VCC_33	VCC_11
Sleep	0.1mA	0.1mA	0.1mA
PowerSave(DTIM=1)	0.1mA	2.6mA	1.3mA
TX(11b 11M)	0.8mA	192mA	15.6mA
TX(11g 54M)	0.8mA	169.5mA	16.3mA
TX(11n 65M)	0.8mA	168.6mA	16.4mA
RX(11n 65M)	0.8mA	42.9mA	21.3mA

Note: All data test under continue mode
VCCIO test under 3.3V

RF Routing

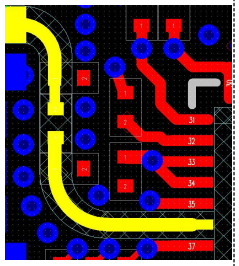
Short and smooth routing with 50 ohm

No layer change, top layer best

Place GND via along RF trace

Integral reference GND for RF trace

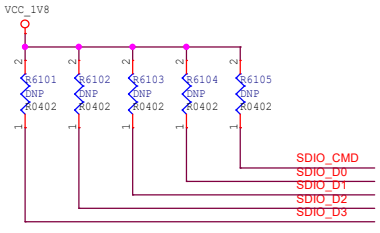
Excavate L2 on RFIO pin and antenna pad



Other Routing Requirement

SDIO CLK trace must be surounded by GND
Do not split L2 GND layer
Epad connet to GND by via alone, minimum 16 via
Pin 4/7/14/18 connet GND by seperate via best

Optional



Note: Reserve pull-high resistors for SDIO data pins base on platform

Crystal Requirement

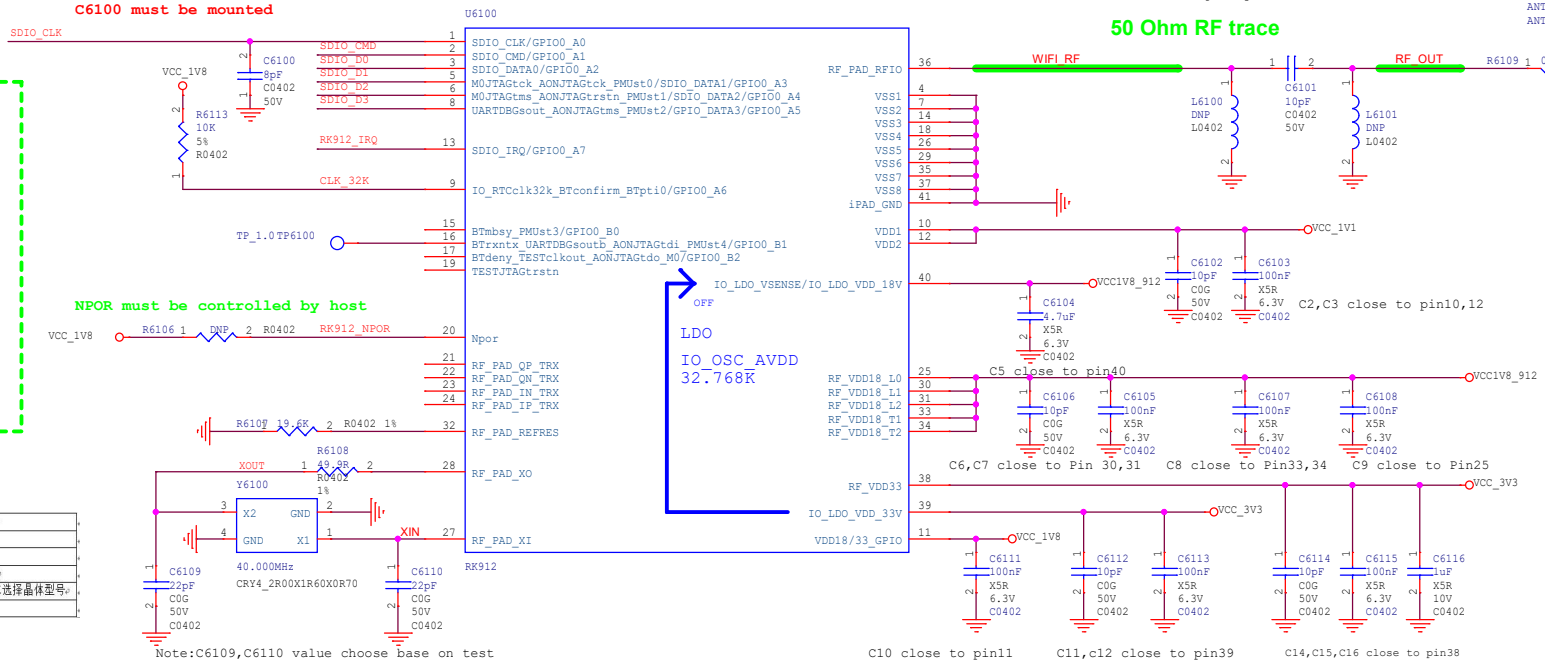
参数	规范			描述
	最小	最大	单位	
频率	40.000000		MHz	
频率偏差	+/-10		ppm	Frequency tolerance
工作温度	-20	80	℃	根据实际产品温度需求选择晶体型号
ESR	/	60	Ohm	

Crystal Routing

Close to RK912
Trace surround by GND
Other signal trace prohibited under crystal

C6100 must be mounted

NPOR must be controlled by host



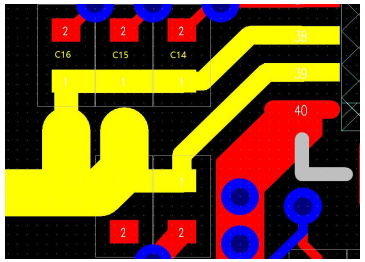
Reserve matching component location for antenna

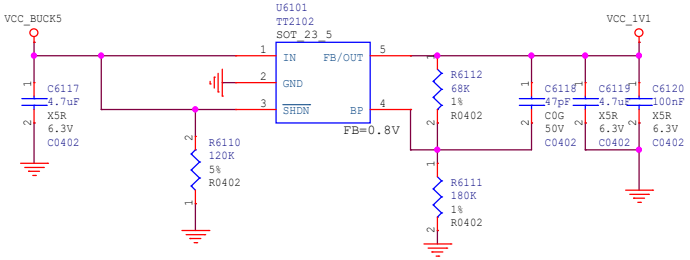
ANT6100
ANT4411DR
ANTPCB_44R00X11R00_DSR

50 Ohm RF trace

Power Routing

Power trace follow star routing
Samll value capacitor closer to pin
10pF closest to pin, then 100nF,
then 1uF





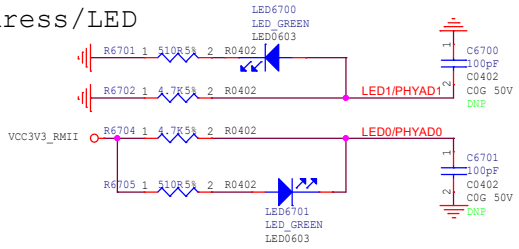
C14,C15,C16 close to pin38

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	61.RK912(option)				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	45 of 54

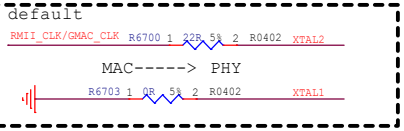
PHY

RMII_TXD0/GMAC_TXD0
RMII_TXD1/GMAC_TXD1
RMII_TXEN/GMAC_TXEN
RMII_RXDV/GMAC_RXDV
RMII_RXER
RMII_RXD0/GMAC_RXD0
RMII_RXD1/GMAC_RXD1
RMII_MDIO/GMAC_MDIO
RMII_MDC/GMAC_MDC
RMII_CLK/GMAC_CLK
EPHY_RSTn
POE12
POE36
POE45
POE78

PHY Address/LED



default



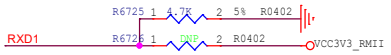
1. No crystal:
R6700,R6703,R6712, R6724 are sodered.
R6708,Y6700,C6702,C6703,R6717 are DNP.

2. With crystal
R6700,R6703,R6712, R6724 are DNP.
R6708,Y6700,C6702,C6703,R6717 are soldered.

MII/RMII Selection

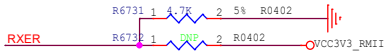
Pull High for RMII mode(default)

WOL/LED0 Selection



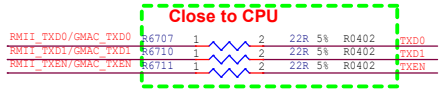
Pull Low for LED0 Mode(default)
Pull High for WOL Mode
WOL:Wake-on-LAN

UTP / Fiber Selection

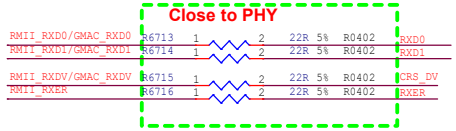


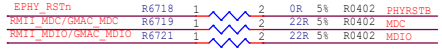
Pull Low for UTP Mode(default)
Pull High for Fiber Mode

Close to CPU

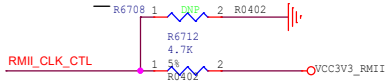


Close to PHY



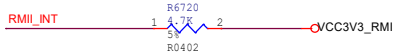


RMII REF_CLK direction

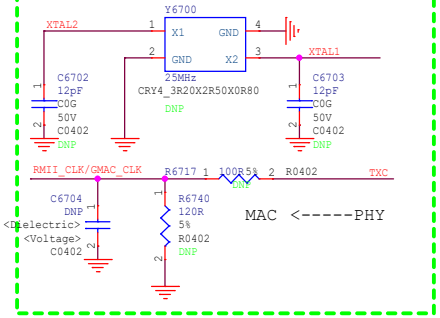


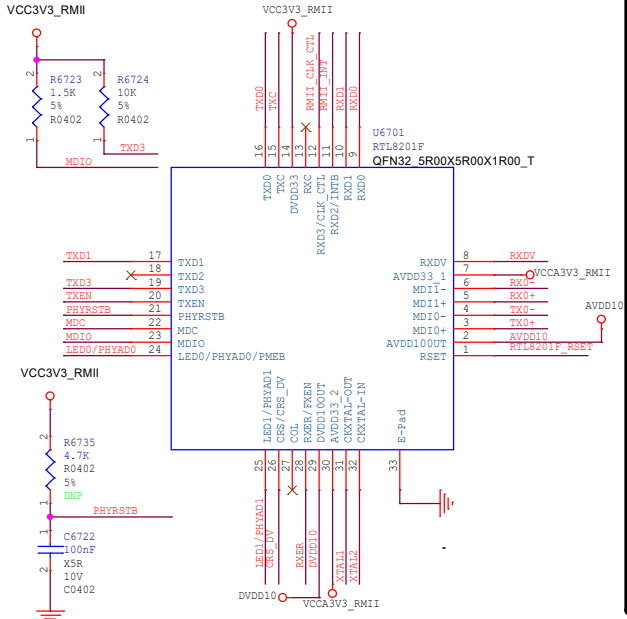
Pull Low for RMII REF_CLK Output mode
Pull High for RMII REF_CLK Input mode

This pin is pulled high by an external 4.7Kohm.
This pin is used for the interrupt function only when in the RMII mode.



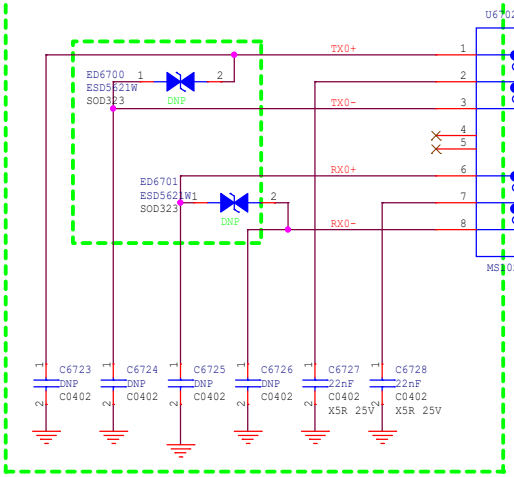
OPTION1



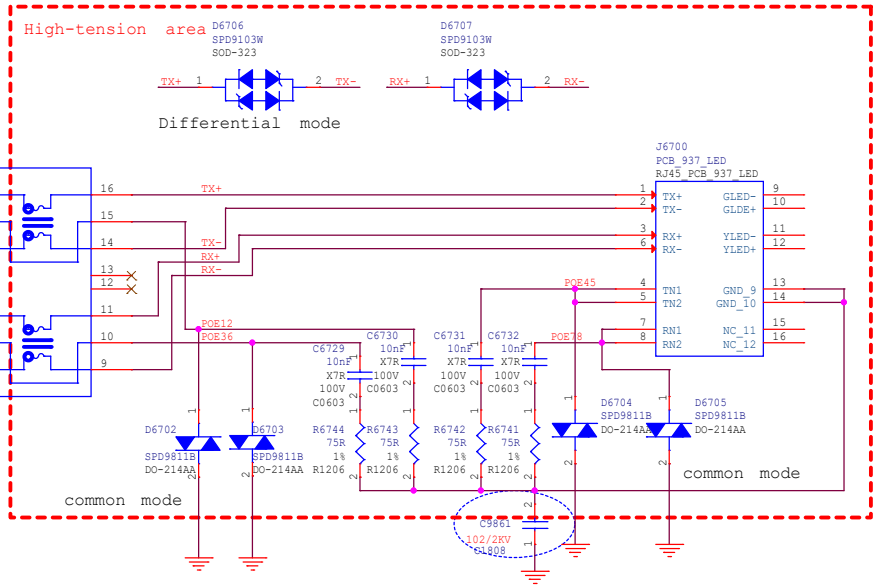


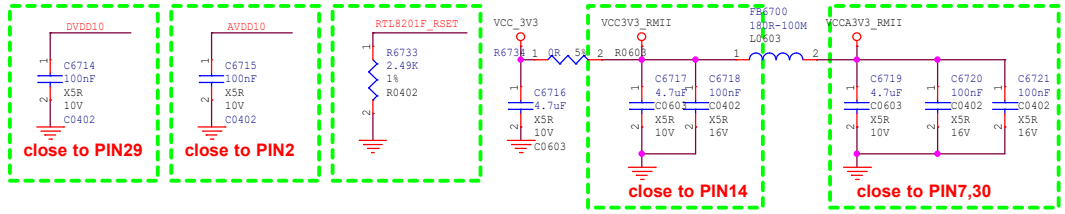
Low-tension area

Differential mode lightning protection



High-tension area





Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	67.Ethernet-EPHY_RMII				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	46 of 54

OPTION:GPHY

10/100/1000M RMII ETHERNET

Close to CPU

Close to PHY

OPTION1

Default

IO pad=1.8V

IO pad=3.3V OPTION1

LINK&ACT

J6800

HR911130C

RJ45_HR911130C

MAC <----- PHY

3.3Vpp

RGMII=3.3V IO,R6824=22R,R6827=DNP
RGMII=1.8V IO,R6824=100R,R6827=120R
If 125M come from RV1126/RV1109,
this part is not used.

CFG_EXT=1:Use the external power source for the IO pad.
CFG_LDO1=1, CFG_LDO0=0: IO pad 1.8V
CFG_LDO1=0,CFG_LDO0=0: IO pad 3.3V

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1'b1	2'b00
External 1.8V (default)	1'b1	2'b10
Internal 1.8V	1'b0	2'b10

VCCIO_PHY Voltage Config

PHY Address Config

PHY Address	PHYAD[2:0]
1 (default)	3'b001

Pull-up for additional 2ns delay to RXC for data latching

Pull-up for additional 2ns delay to TXC for data latching

Pull-up to disable PLL @ ALDPS mode

U6800
RTL8211F-CG
QFN40_5R00X5R00X0R90_T
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial

close to PIN11,40

close to PIN28

close to PIN30

close to PIN3,8,21,38

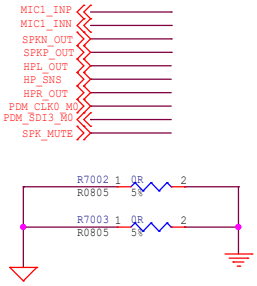
close to PIN29

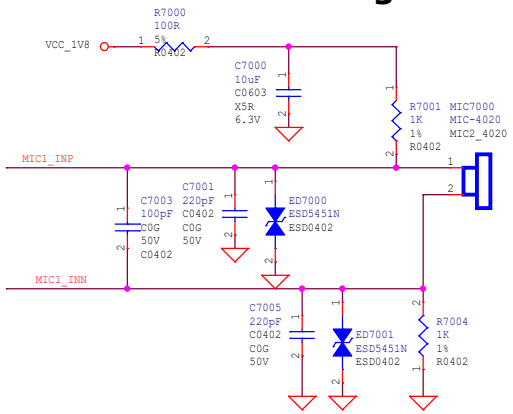
PHYRSTB is 3.3V IO

Rockchip Electronics Co., Ltd	
Project:	RV1126_RV1109_IPC_ENTRANCEGATE
File:	68.Ethernet-GEPHY_RGMII(option)
Date:	Wednesday, January 20, 2021
Rev:	V1.3
Designed by:	Yanhong.Li
Reviewed by:	<Checker>
Sheet:	47 of 54

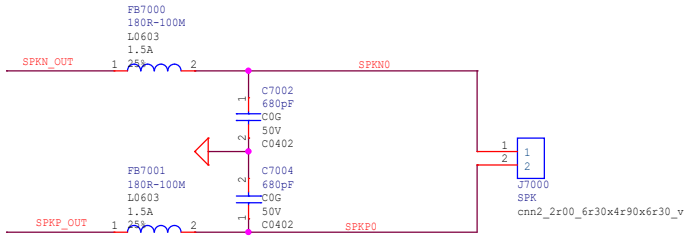
Audio1(MIC/SPK/ NO LOOPBACK) for PMIC RK809-2 power solution

differential Analog MIC

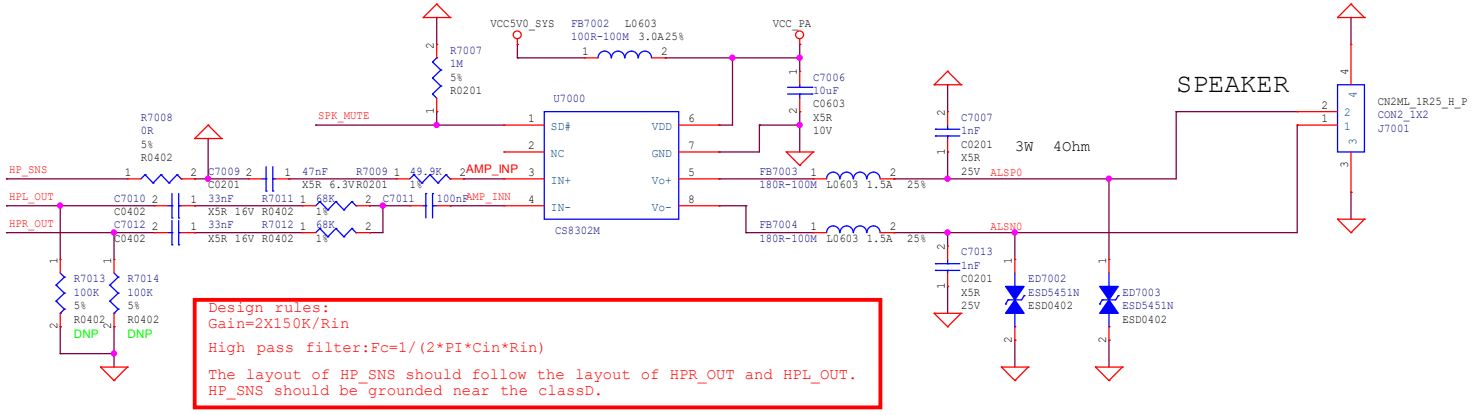


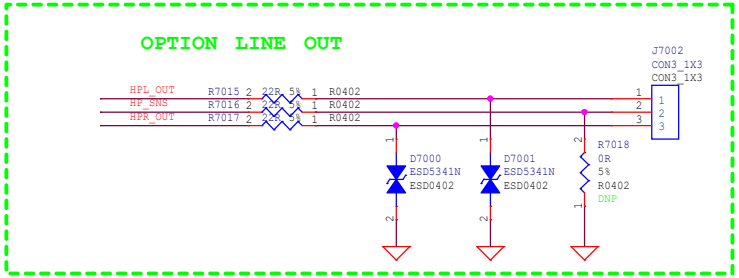


SPK : RL 8Ohm,
1.5W output of class D of RK809-2



Option: RL 4 Ohm,
3W output of class D of CS8302

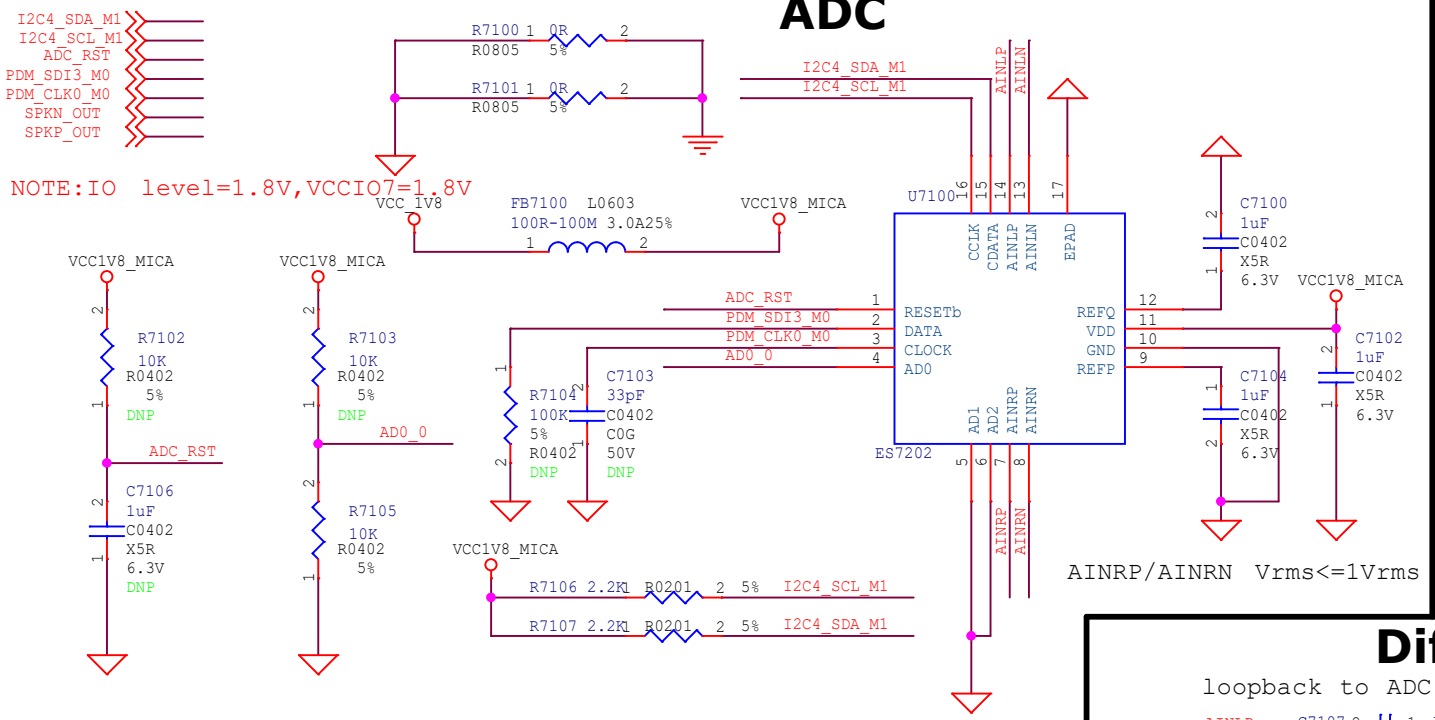




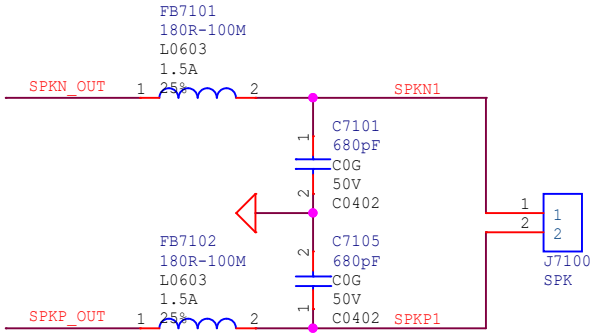
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	70.Audio1(MIC/SPK/NO LOOPBACK)				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	48 of 54

RK809-2+ADC(ES7202) for better loopback effect
One MIC+ SPK+LOOPBACK
for PMIC RK809-2 power solution

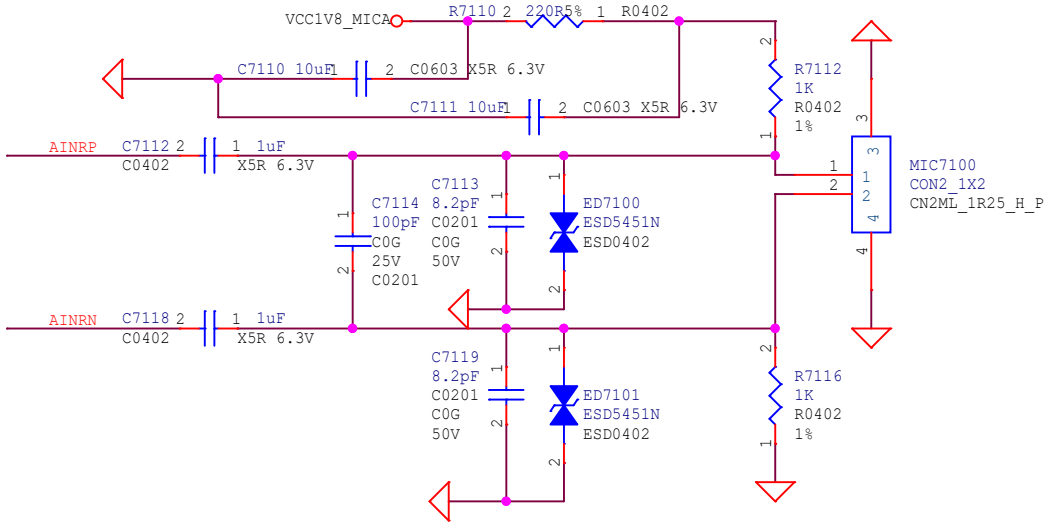
ADC



SPK : RL 8Ohm, 1.5W output of class D of RK809-2

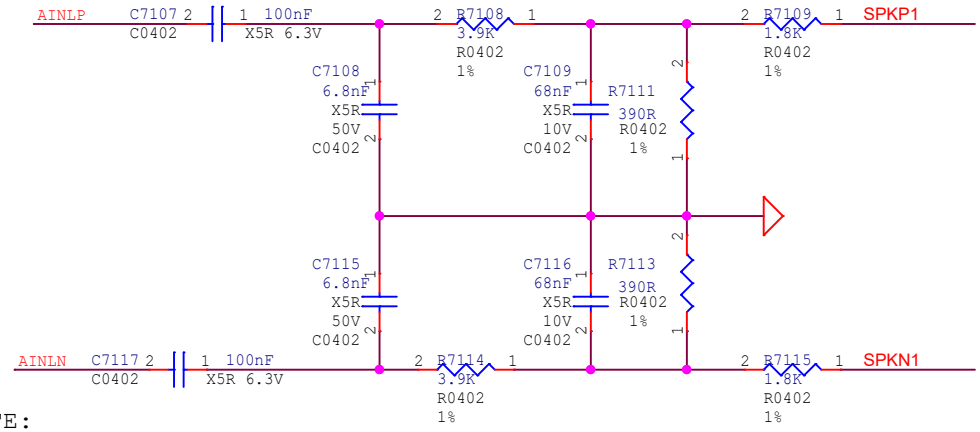


Differential MIC



Differential LOOP BACK

loopback to ADC ES7202



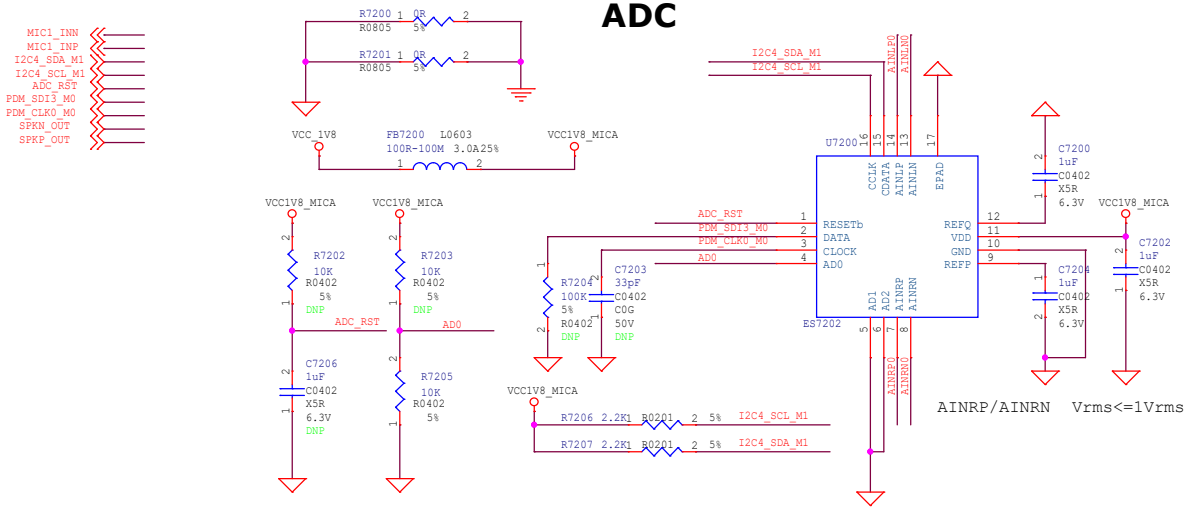
NOTE:
Sample Rate:8KHz, C7108,C7115=6.8nF, C7111,C7113=68nF
Sample Rate:16KHz, C7108,C7115=4.7nF, C7111,C7113=47nF

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	71.Audio(one MIC+RK809-2+ADC)				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	49 of 54

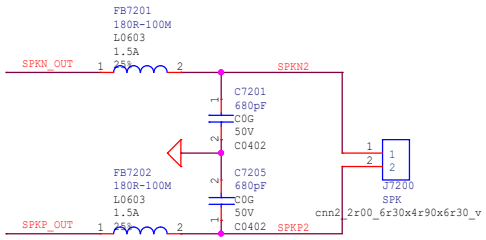
RK809-2+ADC(ES7202) for better loopback effect
Dual MIC+ SPK+LOOPBACK
for PMIC RK809-2 power solution

NOTE: IO level=1.8V,VCCIO7=1.8V
The algorithm options for dual microphones are as follows:
1 algorithm for selecting the third party
2 choose rk dual mic algorithm, but need to apply for the right to use the algorithm

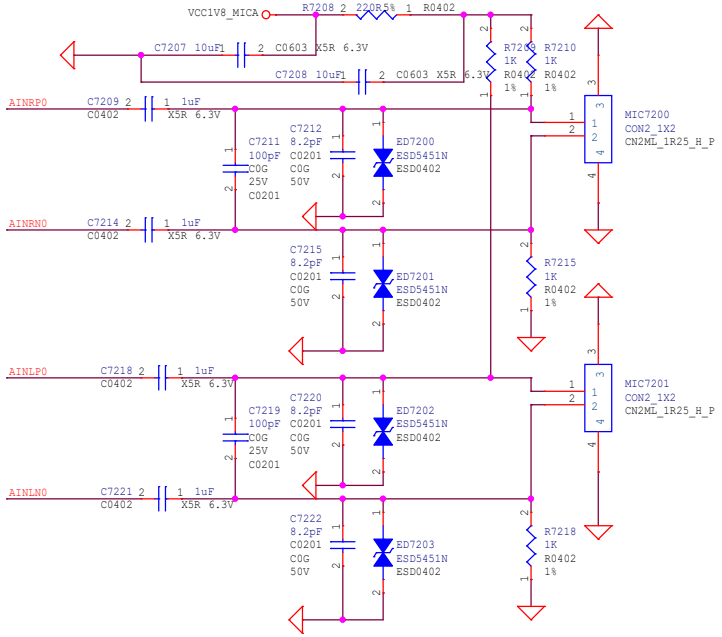
ADC



SPK : RL 8Ohm,
1.5W output of class D of RK809-2

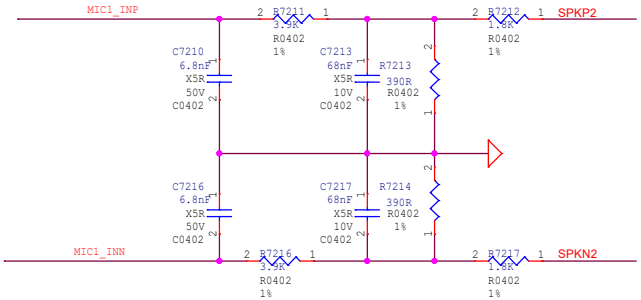


Dual MIC



Differential LOOP BACK

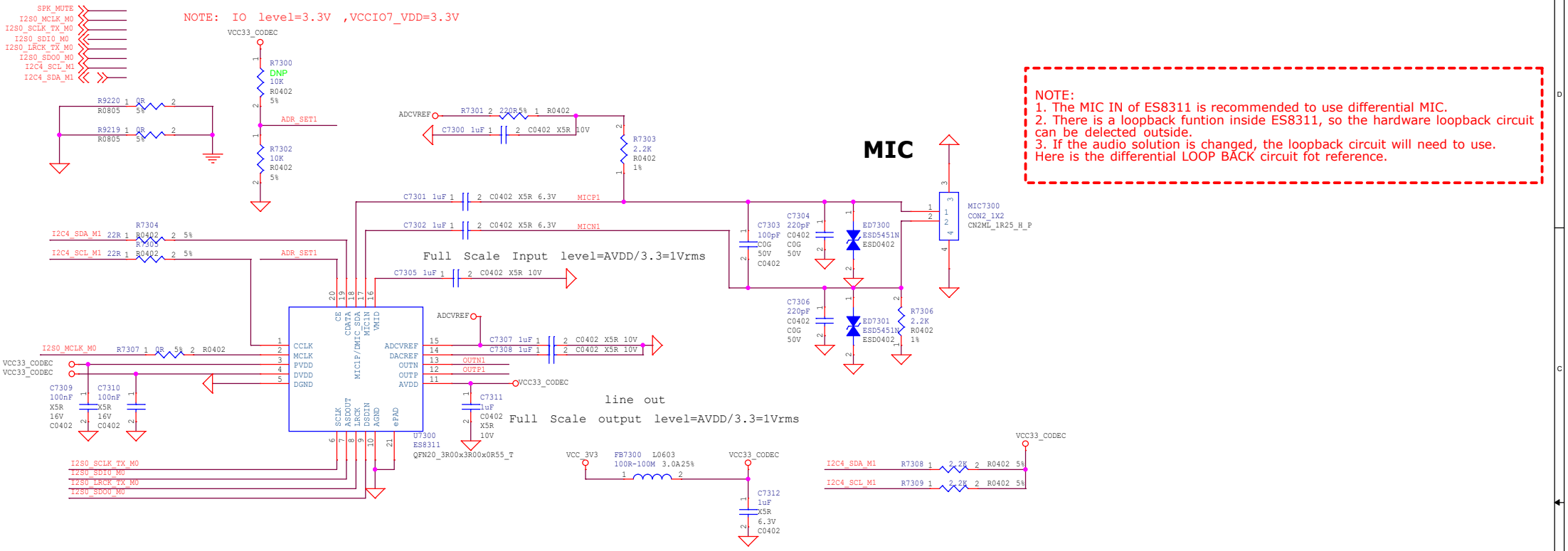
loopback to the mic of RK809-2

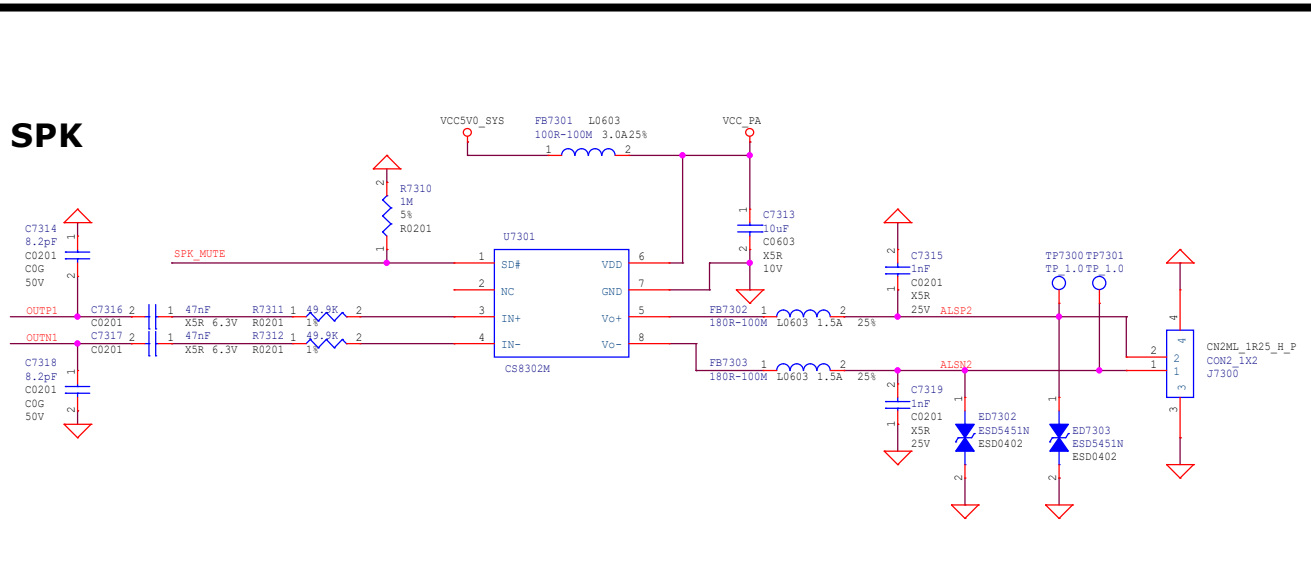


NOTE:
Sample Rate:8KHz, C7210,C7216=6.8nF, C7213,C7217=68nF
Sample Rate:16KHz, C7210,C7216=4.7nF, C7213,C7217=47nF

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd			
Project:	RV1126_RV1109_IPC_ENTRANCEGATE			
File:	72_Audio(dual MIC+RK809-2+ADC)			
Date:	Wednesday, January 20, 2021		Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by: <Checker>	Sheet:	50 of 54

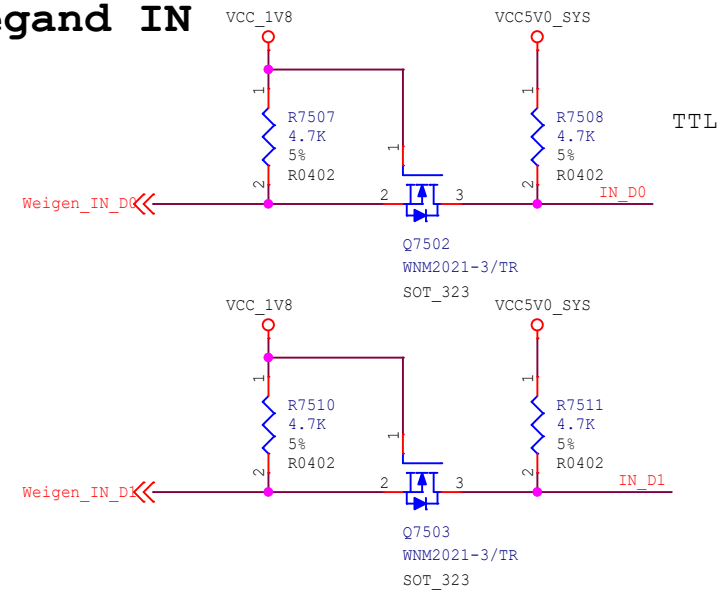
Audio3 for Discrete Power solution



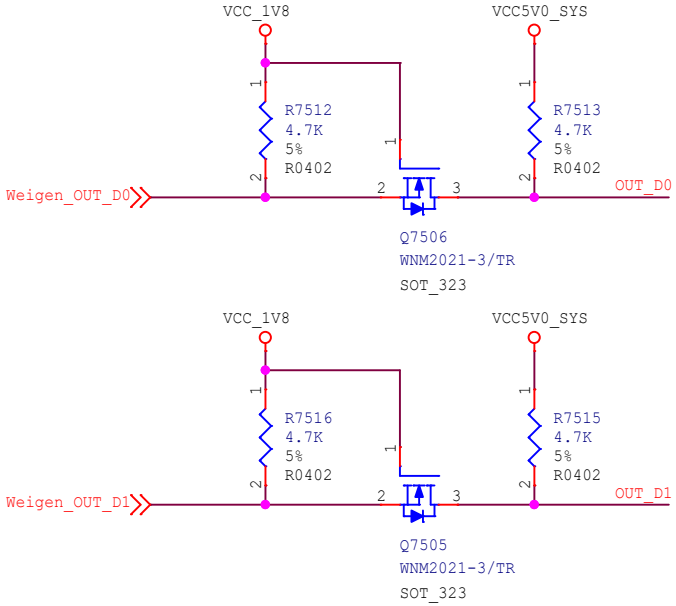


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	73.Audio3(Discrete solution)				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	51 of 54

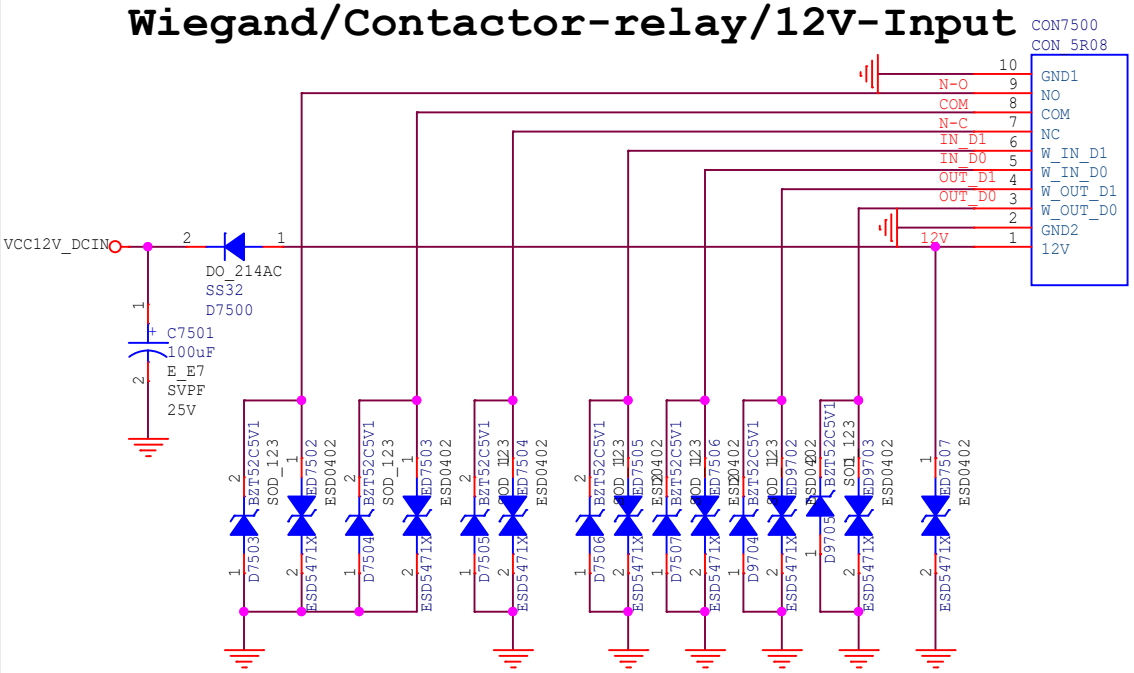
Wiegand IN



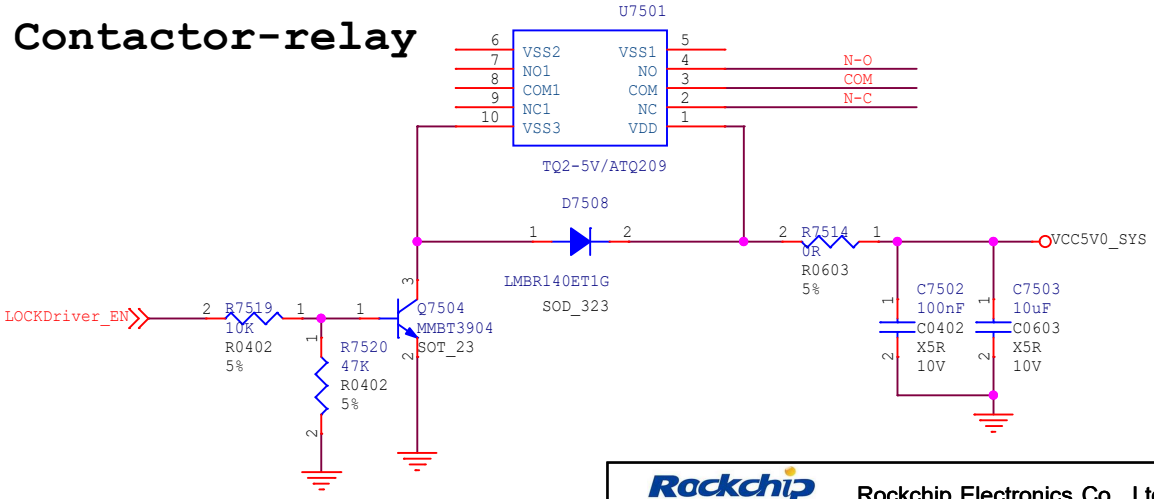
Wiegand OUT



Wiegand/Contactor-relay/12V-Input

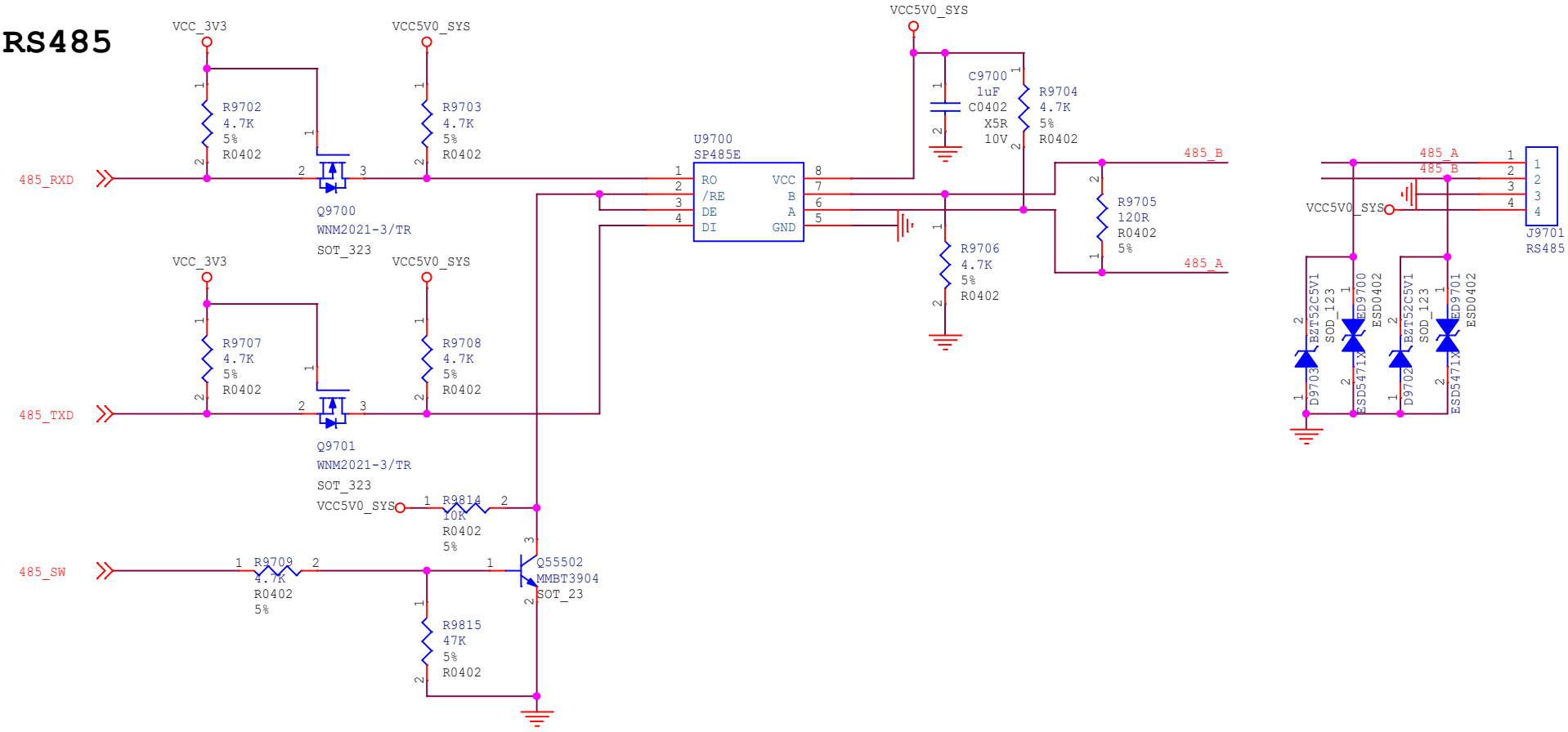


Contactor-relay

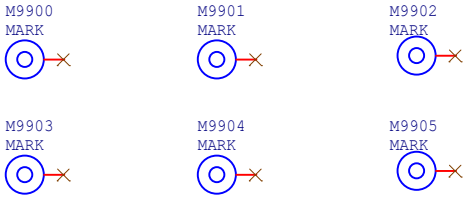


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	75.Wiegand/12V-Input(GATE)				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	52 of 54

RS485



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	97.RS485(GATE)				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	53 of 54



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109_IPC_ENTRANCEGATE				
File:	99.MARK				
Date:	Wednesday, January 20, 2021			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	54 of 54