Global Mixed-mode Technology

G2273A

3A, 1.5MHz, COT Synchronous Step-Down Converter

Features

- **Efficiency Up to 95%**
- **90mΩ and 70mΩ Internal Power MOSFET**
- **V_{IN} Range 2.6V to 5.5V**
- **Adjustable Output Voltage from 0.6V to V_{IN}**
- **Power Save Mode for Light Load Efficiency**
- **Constant-On-Time Control Scheme Design for Fast Transient Response, Stability with MLCC Output Capacitor**
- **100% Duty Cycle for Lowest Dropout**
- **17µA Operating Quiescent Current**
- **Fixed Soft-Start 0.9ms**
- **Output Discharge**
- **Power Good Output**
- **Cycle-by-Cycle Over Current Protection**
- **Input Under Voltage Lockout**
- **Output Under Voltage Protection (Hiccup)**
- **Thermal Shutdown Protection**

Applications

- **Portable and Mobile Devices**
- **Wireless and Networking Devices**
- **LCD TV Power Supply**
- **Solid State Drive**

General Description

The G2273A is a monolithic, step-down, switch mode converter with built-in internal power MOSFETs. It achieves 3A continuous output current from a 2.6V to 5.5V input voltage with excellent load and line regulation. The Output voltage can be regulated to as low as 0.6V. At medium to heavy loads, the switching frequency is 1.5MHz. At light load, the device automatically enters PSM to maintain high efficiency.

The Constant-On-Time control scheme in G2273A provides fast transient response to be optimized over a wide range of loads and output capacitors. Thermal shutdown and cycle-by-cycle current limiting are used for protection.

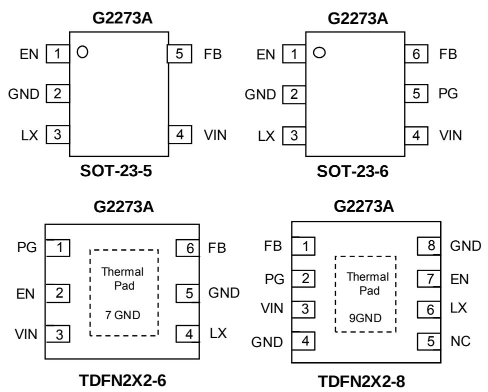
The G2273A are available in SOT-23-5, SOT-23-6, TDFN2X2-6 and TDFN2X2-8 packages.

Ordering Information

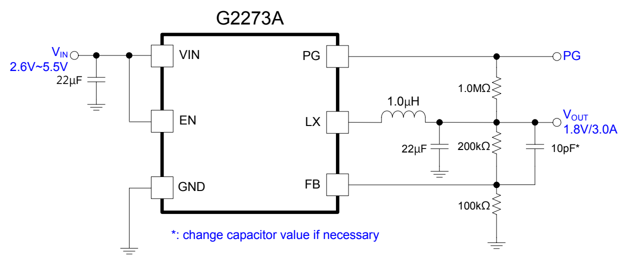
ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2273AT11U	223Ax	-40°C to +85°C	SOT-23-5
G2273ATB1U	223Ax	-40°C to +85°C	SOT-23-6
G2273ARB1U	223A	-40°C to +85°C	TDFN2X2-6
G2273ARC1U	223A	-40°C to +85°C	TDFN2X2-8

Note: T1: SOT-23-5 TB: SOT-23-6 RB: TDFN2X2-6 RC: TDFN2X2-8
1: Bonding Code
U : Tape & Reel
Green: Lead Free / Halogen Free

Pin Configuration



Typical Application Circuit



Absolute Maximum Ratings

VIN, LX, FB . . . . -0.3V to 6V
EN . . . . -0.3V to (V_{IN}+0.3V)
LX (AC, less than 10nS) . . . . -3V to 10V
Thermal Resistance of Junction to Ambient, (θ_{JA})
SOT-23-5 . . . . TBD°C/W
SOT-23-6 . . . . TBD°C/W
TDFN2X2-6. . . . . TBD°C/W
TDFN2X2-8. . . . . TBD°C/W
Continuous Power Dissipation (T_A = +25°C)
SOT-23-5. . . . . .TBDW
SOT-23-6. . . . . .TBDW
TDFN2X2-6. . . . . TBD°C/W
TDFN2X2-8. . . . . TBD°C/W

Thermal Resistance of Junction to Ambient, (θ_{JC})
SOT-23-5 . . . . .TBD°C/W
SOT-23-6 . . . . .TBD°C/W
TDFN2X2-6. . . . . TBD°C/W
TDFN2X2-8. . . . . TBD°C/W
Junction Temperature . . . . -40°C to150°C
Storage Temperature . . . . -65°C to 150°C
Reflow Temperature (soldering, 10sec) . . . . . . 260°C
ESD (HBM) 2KV

Recommended Operating Conditions

Supply Input Voltage. . . . . .2.6V to 5.5V
Ambient Temperature Range. . . . .-40°C to 85°C
Junction Temperature Range. . . . .-40°C to 125°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

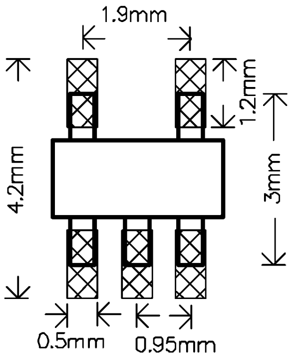
(V_{IN}=5V, T_A=25°C)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

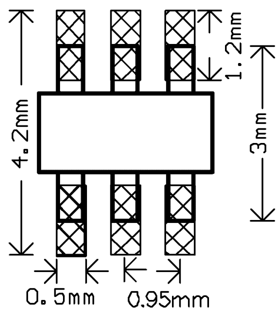
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		2.6	---	5.5	V
VIN Quiescent current	I_Q	No load, device not switching	---	17	25	µA
VIN Shutdown current	I_{SD}	V_{EN}=0V, Shutdown	---	---	1	µA
VIN under voltage lock out threshold	V_{UVLO}	V_{IN} falling	---	2.4	2.5	V
VIN under voltage lock out hysteresis	V_{UVLO_HYS}		---	100	---	mV
Thermal shutdown threshold	T_{JSD}	T_J rising	---	150	---	°C
Thermal shutdown hysteresis	T_{JSD_HYS}		---	30	---	°C
EN Input Logic High Voltage	V_{IH}	2.6V≦V_{IN}≦5.5V	1.2	---	---	V
EN Input Logic Low Voltage	V_{IL}	2.6V≦V_{IN}≦5.5V	---	---	0.4	V
EN Input Leakage Current	I_{EN}	V_{EN}=5V	---	---	0.1	µA
Soft-Start Time	T_{SS}	Time from EN high to 95% of V_{OUT} nominal	---	0.9	---	mS
Power good threshold	V_{PG_R}	V_{OUT} rising, referenced to V_{OUT} nominal	----	95	---	%
	V_{PG_F}	V_{OUT} falling, referenced to V_{OUT} nominal	---	90		%
PG low-level output voltage	$V_{PG(OL)}$	I_{SINK}=1mA	---	---	0.4	V
PG input leakage current	$I_{PG(LK)}$	V_{PG}=5V	---	---	0.1	µA
Power good delay	t_{PG_DLY}	V_{FB} falling	---	40	---	µS
Feedback Reference Voltage	V_{REF}	2.6V≦VIN≦5.5V	0.588	0.6	0.612	V
Feedback Leakage Current	$I_{FB(LK)}$	V_{FB} = 0.6V	---	---	0.1	µA
Output discharge FET on-resistance	R_{DIS}	V_{EN}=0V	---	10	---	Ω
Switching Frequency	f_{SW}	V_{OUT}=1.8V, I_{OUT}=1A	---	1.5	---	MHz
Minimum Off Time	$t_{OFF(MIN)}$	High side PFET	---	80	---	nS
PFET switch on resistance	$R_{DSON(P)}$	VIN=3.6V	---	90	---	mΩ
NFET switch on resistance	$R_{DSON(N)}$	VIN=3.6V	---	70	---	mΩ
PFET switch current limit	$I_{LIM(P)}$		---	6.5	---	A
NFET switch current limit	$I_{LIM(N)}$		---	4.5	---	A

Minimum Footprint PCB Layout Section

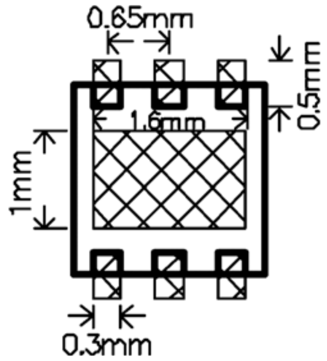
SOT-23-5



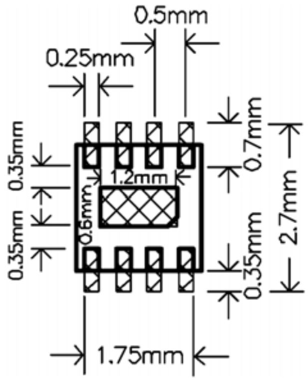
SOT-23-6



TDFN2X2-6

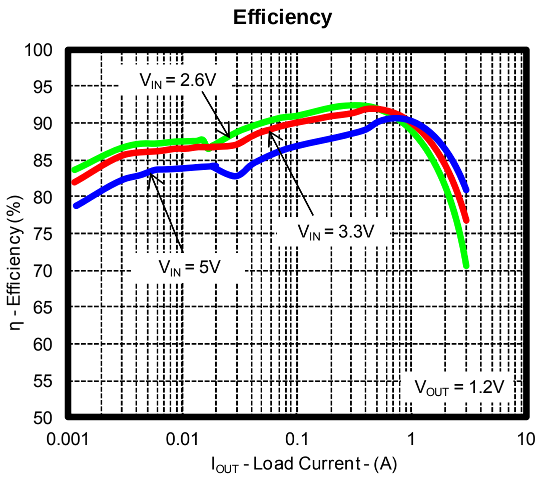


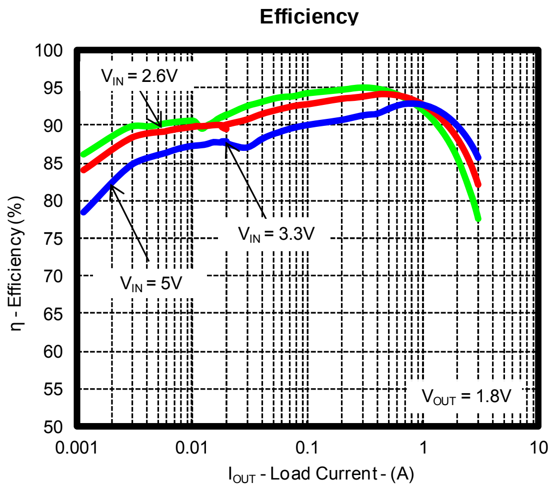
TDFN2X2-8

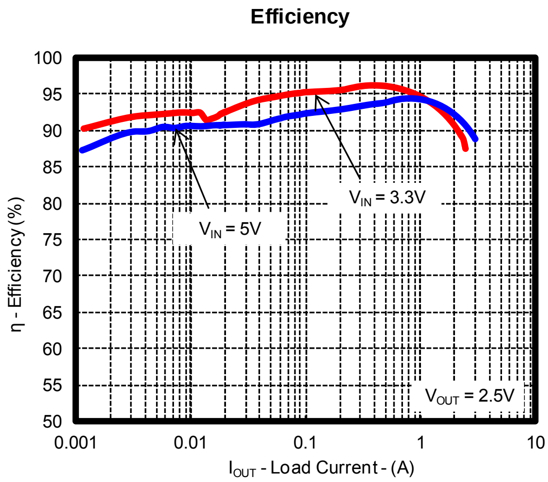


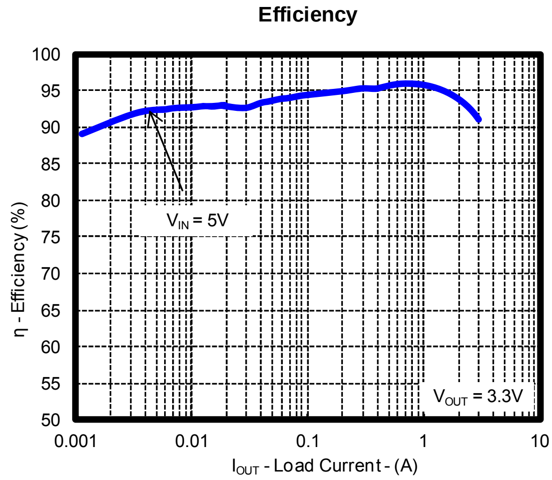
Typical Performance Characteristics

(V_{IN} = 5V, V_{OUT} = 1.8V, T_A = 25°C, unless otherwise noted.)



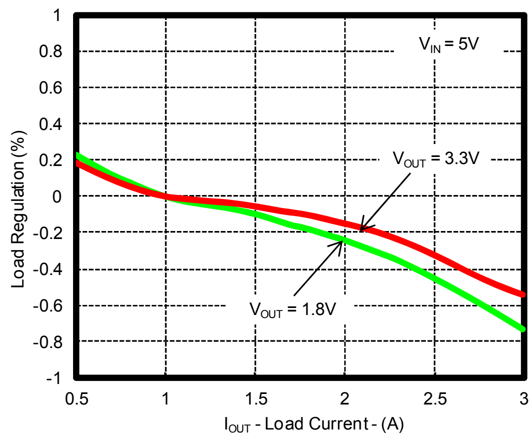




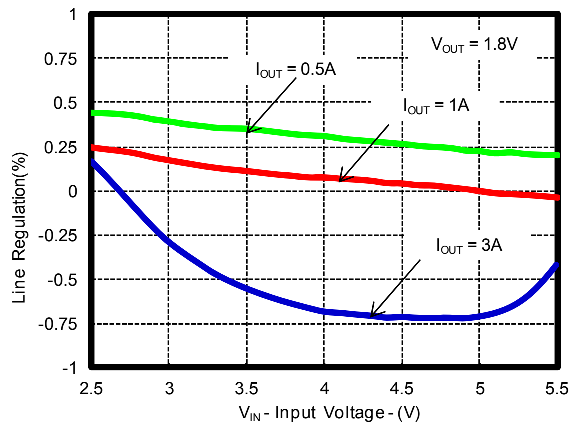


Typical Performance Characteristics (continued)

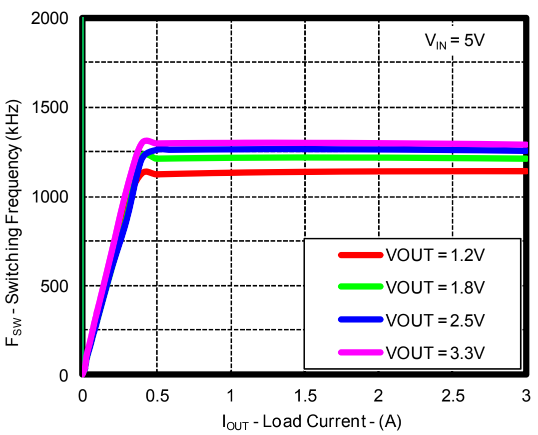
Load Regulation



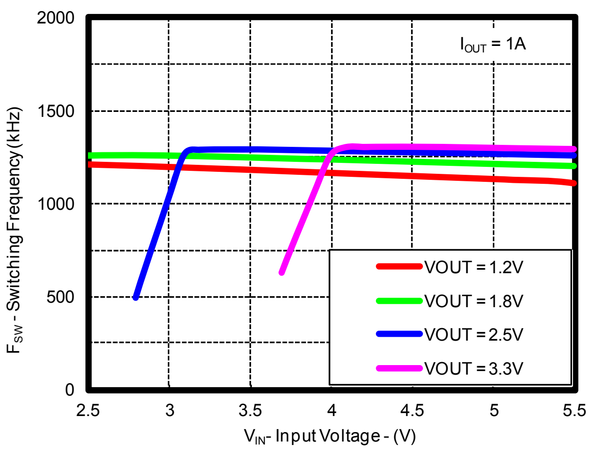
Line Regulation



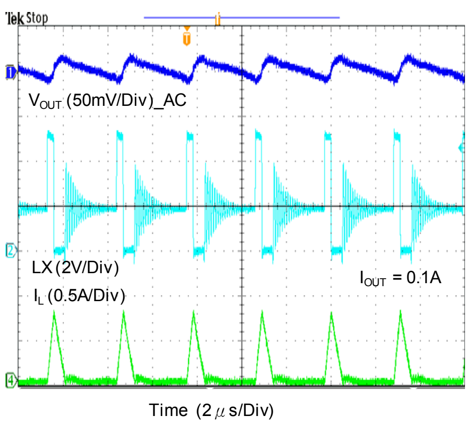
Switching Frequency



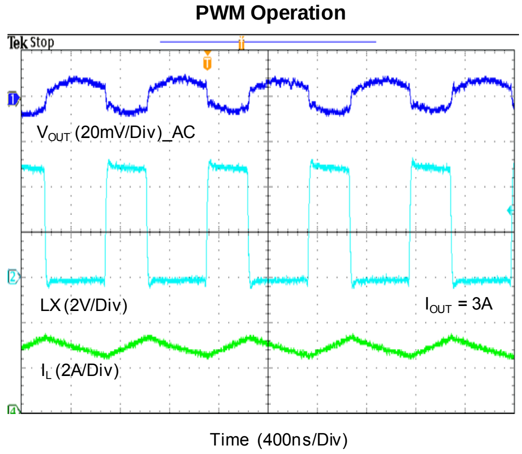
Switching Frequency



PSM Operation

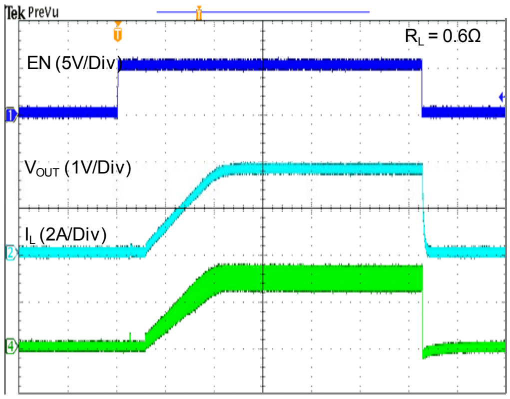


PWM Operation



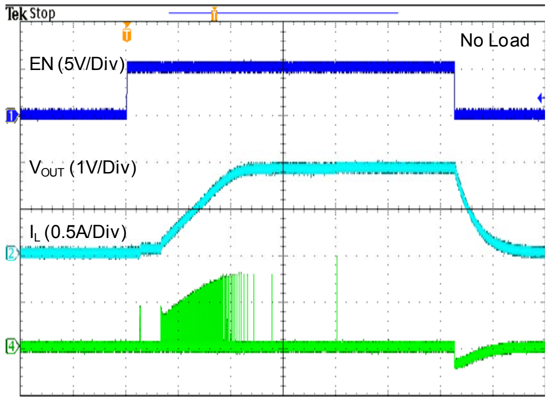
Typical Performance Characteristics (continued)

Start-Up and Shut-Down



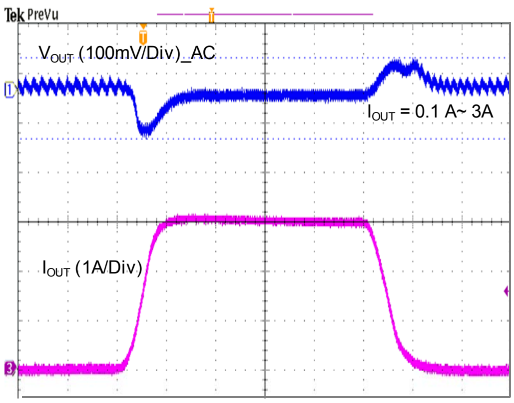
Time (400μs/Div)

Start-Up and Shut-Down



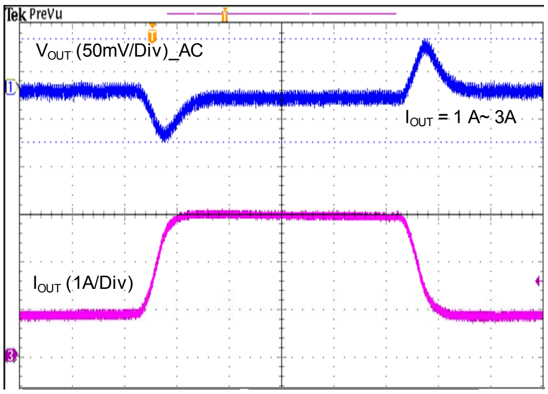
Time (400μs/Div)

Load Transient Response



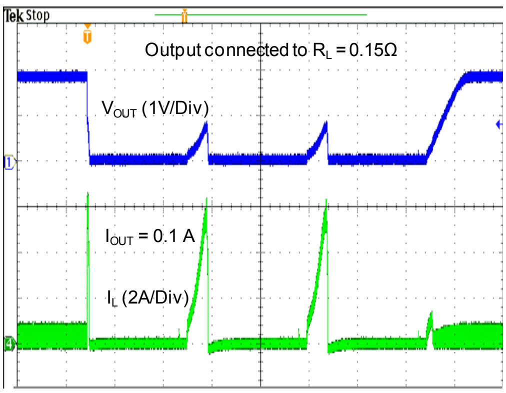
Time (20μs/Div)

Load Transient Response



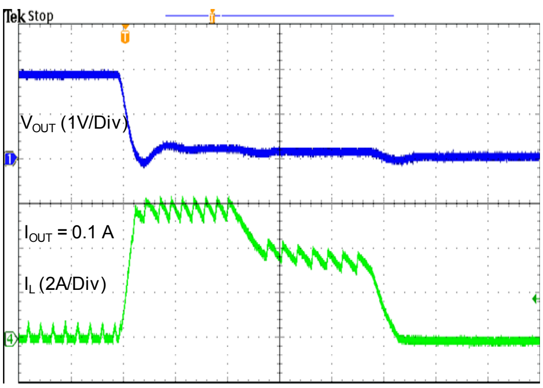
Time (20μs/Div)

Output Short Circuit Protection (Hiccup)



Time (800μs/Div)

Output Short Circuit Protection (Hiccup) - Zoom in

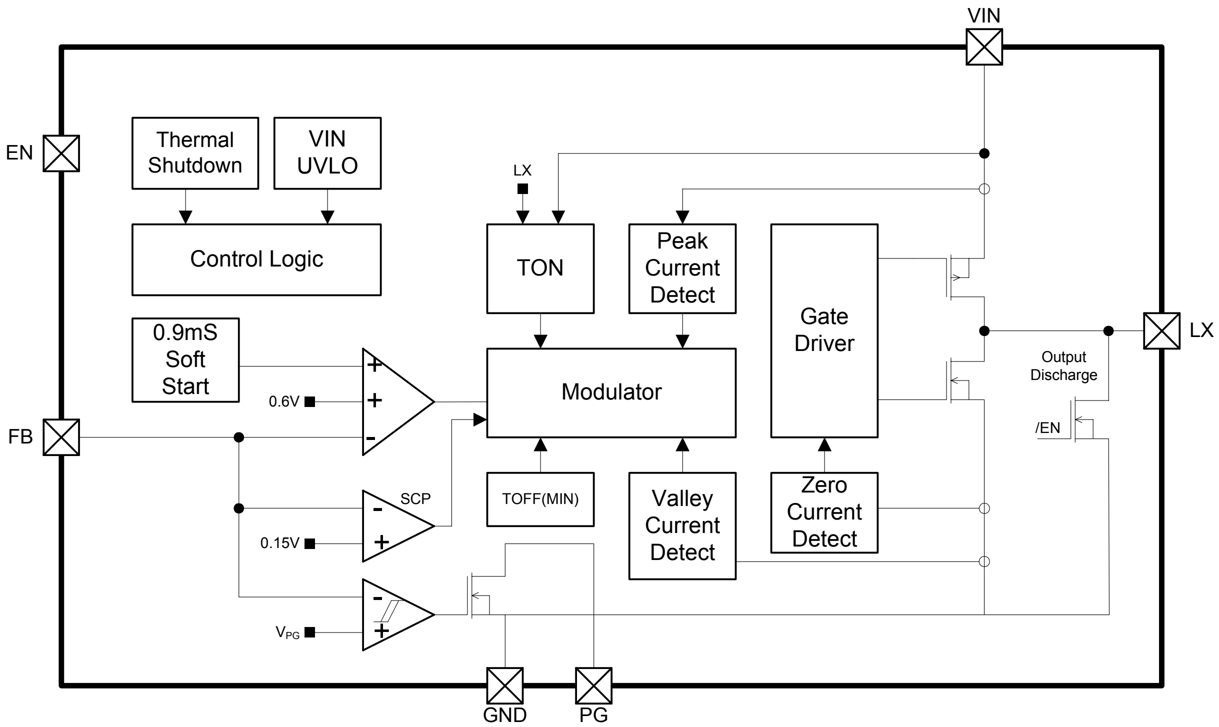


Time (10μs/Div)

Pin Description

PIN No.				NAME	FUNCTION
SOT23-5	SOT23-6	TDFN2X2-6	TDFN2X2-8		
1	1	2	7	EN	Enable Control Input. Do not leave this pin floating.
2	2	5,7	4,8,9	GND	Ground.
3	3	4	6	LX	Switch Node.
4	4	3	3	VIN	Supply Voltage Input.
---	5	1	2	PG	Power good open drain output pin. The pull-up resistor cannot be connected to any voltage higher than 5.5V. If unused, leave it floating.
5	6	6	1	FB	An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage.

Block Diagram



Operation

The G2273A is a high efficiency synchronous step-down DC/DC converter. G2273A provides an adjustable regulated output voltage from 0.6V to V_{IN} while delivering up to 3A of output current with input voltage from 2.6V to 5.5V.

The G2273A uses the constant on-time control scheme. In normal operation, the high side P-MOSFET is turned on when the switch controller is set by the comparator and is turned off when the Ton comparator resets the switch controller.

Low side MOSFET current is measured. The error amplifier adjusts COMP voltage by comparing the feedback signal (VFB) from the output voltage with the internal 0.6V reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference, then the COMP voltage rises to allow higher inductor current to match the load current.

Enable

When the input voltage is greater than the under voltage lockout threshold, a logic-high (>1.2V) enables the converter; a logic-low (<0.4V) forces the IC into shutdown mode. Do not leave this pin floating.
When the device is disabled, there is a resistive discharge path from LX pin.

Soft-Start (SS)

There is an internal built-in soft-start to ramp the output voltage at a fixed slew rate to avoid in-rush current. The typical soft-start time is 0.9ms.

Application Information

The G2273A is a single-phase step-down converter. It provides single feedback loop, constant on-time control with fast transient response. An internal 0.6V reference allows the output voltage to be precisely regulated for low output voltage applications and internal compensation are integrated to minimize external component count. Protection features include over current protection, under voltage protection and over temperature protection.

Output Voltage Setting

Connect a resistive voltage divider at the FB between V_{OUT} and GND to adjust the output voltage. The output voltage is set according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} is the feedback reference voltage 0.6V (typ.).

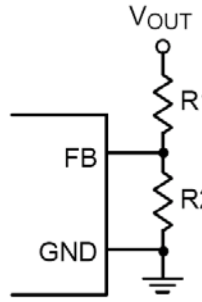


Figure 1. Setting V_{OUT} with a Voltage Divider

Chip Enable and Disable

The EN pin allows for power sequencing between the controller bias voltage and another voltage rail. The G2273A remains in shutdown if the EN pin is lower than 400mV. When the EN pin rises above the VEN trip point, the G2273A begins a new initialization and soft-start cycle.

Internal Soft-Start

The G2273A provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft-start, the internal soft-start capacitor becomes charged and generates a linear ramping up voltage across the capacitor. This voltage clamps the
voltage at the FB pin, causing PWM pulse width to increase slowly and in turn reduce the input surge current. The internal 0.6V reference takes over the loop control once the internal ramping-up voltage becomes higher than 0.6V.

UVLO Protection

The G2273A has input Under Voltage Lockout protection (UVLO). If the input voltage exceeds the UVLO rising threshold voltage (2.5V typ.), the converter resets and prepares the PWM for operation. If the input voltage falls below the UVLO falling threshold voltage during normal operation, the device will stop switching. The UVLO rising and falling threshold voltage has a hysteresis to prevent noise-caused reset.

Inductor Selection The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as shown below :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times LIR \times I_{LOAD(MAX)} \times V_{IN}}$$

where LIR is the ratio of the peak-to-peak ripple current to the average inductor current. Find a low loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2} \times I_{LOAD(MAX)}\right)$$

The calculation above serves as a general reference. To further improve transient response, the output inductor can be further reduced. This relation should be considered along with the selection of the output capacitor. Inductor saturation current should be chosen over IC's current limit.

Input Capacitor Selection

High quality ceramic input decoupling capacitor, such as X5R or X7R, with values greater than 10uF are recommended for the input capacitor. The X5R and X7R ceramic capacitors are usually selected for power regulator capacitors because the dielectric material has less capacitance variation and more temperature stability. For most applications, a 10uF capacitor is sufficient. Higher output voltages may require a 22uF capacitor to increase system stability.

Voltage rating and current rating are the key parameters when selecting an input capacitor. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design.

The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation:

$$I_{IN\_RMS} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} X \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is selecting a proper capacitor for RMS current rating. One good design uses more than one capacitor with low equivalent series resistance (ESR) in parallel to form a capacitor bank.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be approximately calculated using the following equation :

$$\Delta V_{IN} = \frac{I_{OUT(MAX)}}{C_{IN} \times f_{SW}} X \frac{V_{OUT}}{V_{IN}} X \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor Selection

The output capacitor and the inductor form a low pass filter in the Buck topology. In steady state condition, the ripple current flowing into/out of the capacitor results in ripple voltage. The output voltage ripple (VP-P) can be calculated by the following equation:

$$V_{P\_P} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}}\right)$$

When load transient occurs, the output capacitor supplies the load current before the controller can respond. Therefore, the ESR will dominate the output voltage sag during load transient. The output voltage undershoot (VSAG) can be calculated by the following equation:

$$V_{SAG} = \Delta I_{LOAD} \times ESR$$

For a given output voltage sag specification, the ESR value can be determined.

Another parameter that has influence on the output voltage sag is the equivalent series inductance (ESL). The rapid change in load current results in di/dt during transient. Therefore, the ESL contributes to part of the voltage sag. Using a capacitor with low ESL can obtain better transient performance. Generally, using several capacitors connected in parallel can have better transient performance than using a single capacitor for the same total ESR. An output capacitor higher than 22uF is required to increase system stability for lower output voltage applications.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

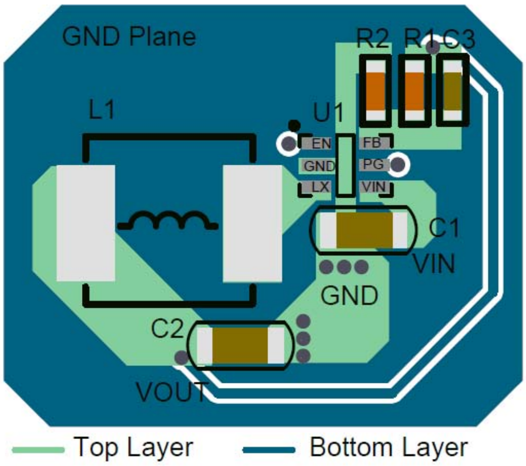
$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}.

Layout Consideration

1. Component Placement:
   - Place input capacitors as close as possible to VIN.
   - Place the feedback resistors and compensation components as close as possible to the IC.
2. Layout Recommendation
   - To prevent electromagnetic interference (EMI) problems and reduce voltage ripple of the device, any high current copper trace which see high frequency switching should be optimized.
   - Therefore, use short and wide traces for power current paths and for power ground tracks, power plane and ground plane are recommended if possible.
   - It is important to minimize the area of the switching nodes and use the ground plane under them to minimize crosstalk to sensitive signals and ICs.
   - It's suggested to keep as complete of a ground plane under G2273A if possible.
   - It is always good practice to keep the sensitive tracks such as feedback connection (FB) away from switching signal connections (LX).

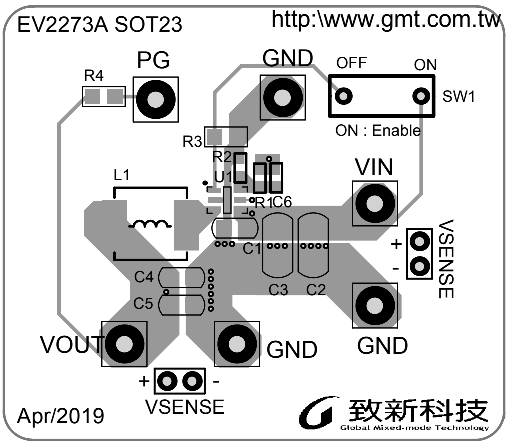


Bill of Materials

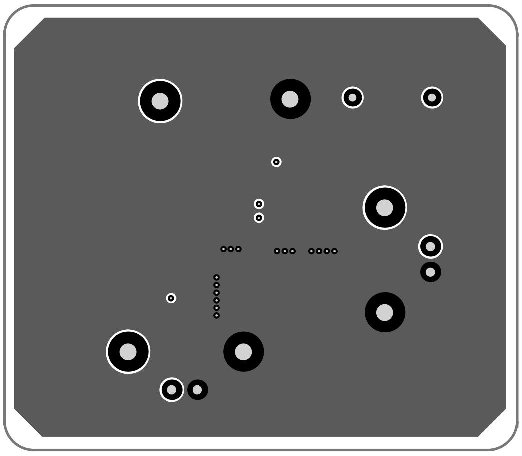
Location	Quantity	Description	Value	Manufacturer
U1	1	SOT23	G2273A	Global Mixed-mode Technology
L1	1	SPM6530T-1R0M	1µH	TDK
R1	1	1%, 0603	Depending on the output voltage	TA-I
R2	1	1%, 0603	100kΩ	TA-I
C1, C4	2	16V, X5R, 0805	22µF	TAIYO YUDEN
C6	1	50V, X5R, 0603	10pF	TAIYO YUDEN

EV Board Layout

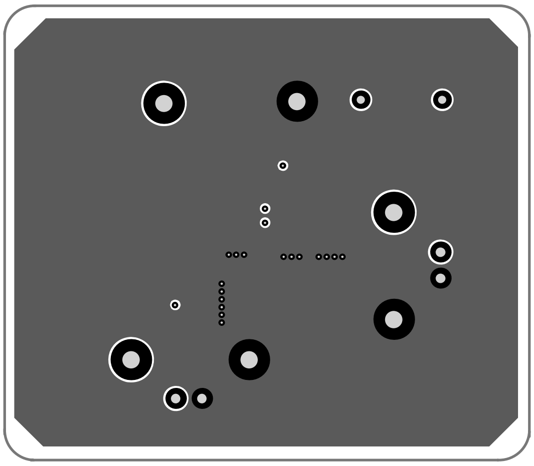
Top Layer



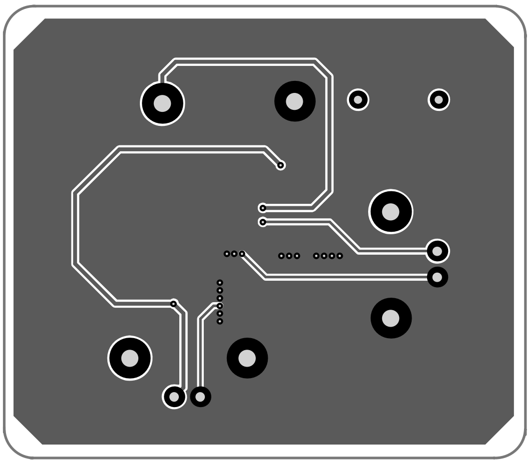
Mid Layer 1



Mid Layer 2

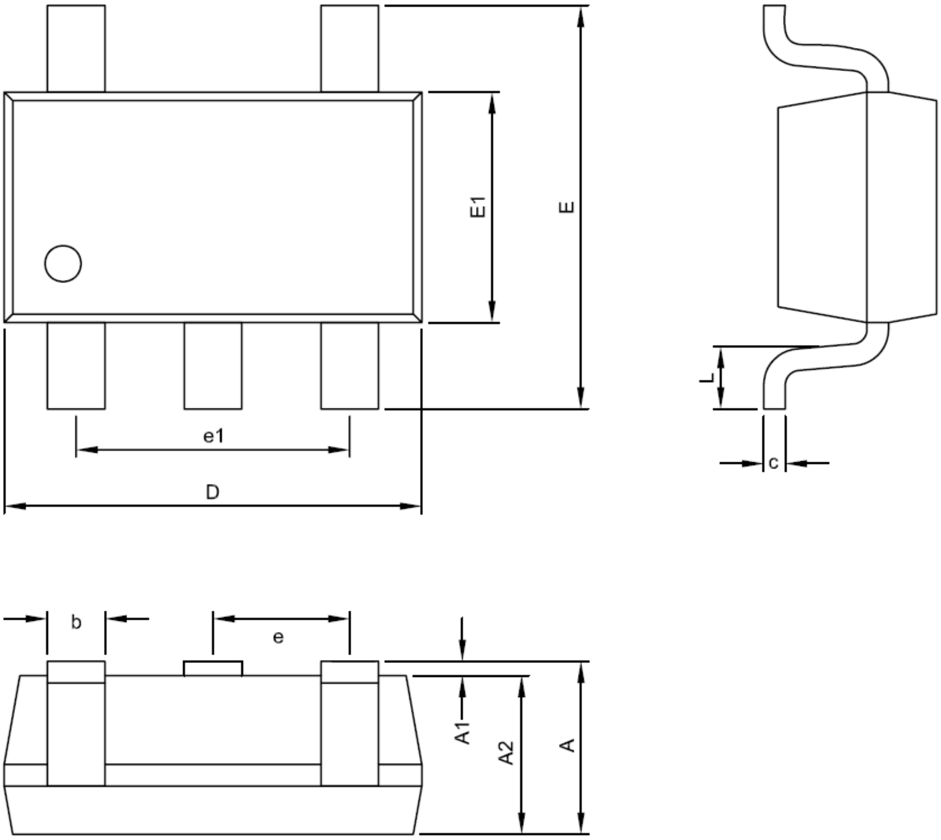


Bottom Layer



EV2273A PCB	Information
Board Material	FR4
Size	51 mm x 44 mm
Board Thickness	1.6mm
Layers	4
Copper Thickness	2oz.

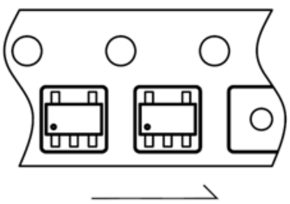
Package Information



SOT-23-5 Package

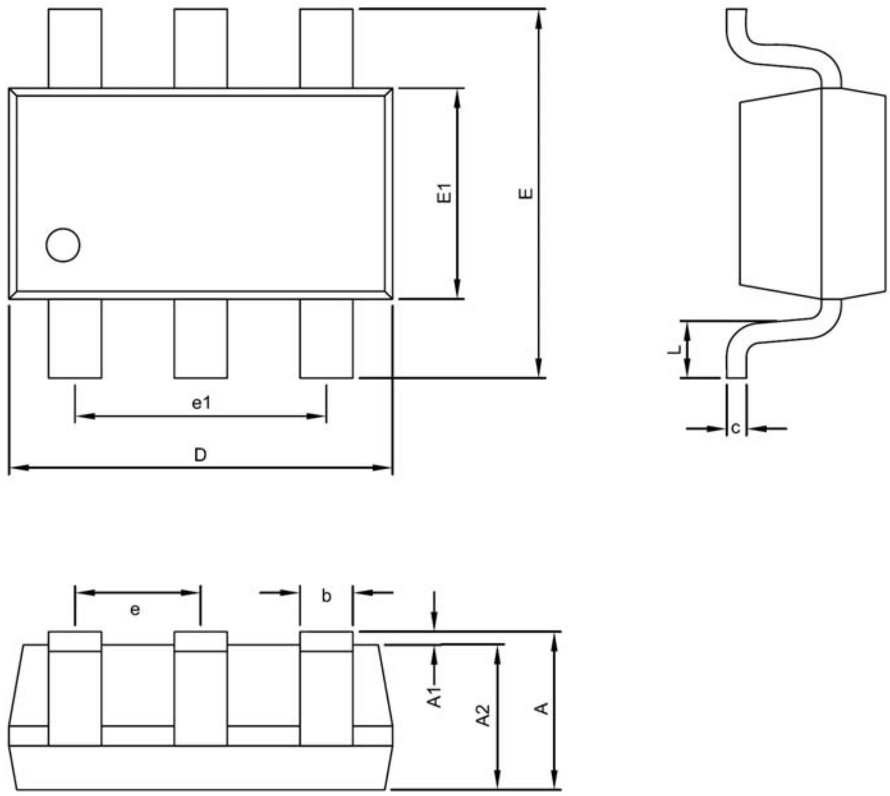
Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.95	1.10	1.45	0.037	0.043	0.057
A1	0.00	---	0.15	0.000	---	0.006
A2	0.90	1.10	1.30	0.035	0.043	0.051
D	2.70	2.90	3.10	0.106	0.114	0.122
E	2.60	2.80	3.00	0.102	0.110	0.118
E1	1.50	1.60	1.70	0.059	0.063	0.067
c	0.08	0.15	0.25	0.003	0.006	0.010
b	0.30	0.40	0.50	0.012	0.016	0.020
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024

Taping Specification



Feed Direction

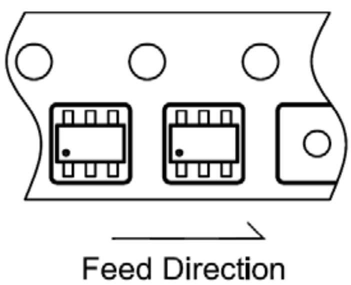
PACKAGE	Q'TY/BY REEL
SOT-23-5	3,000 ea



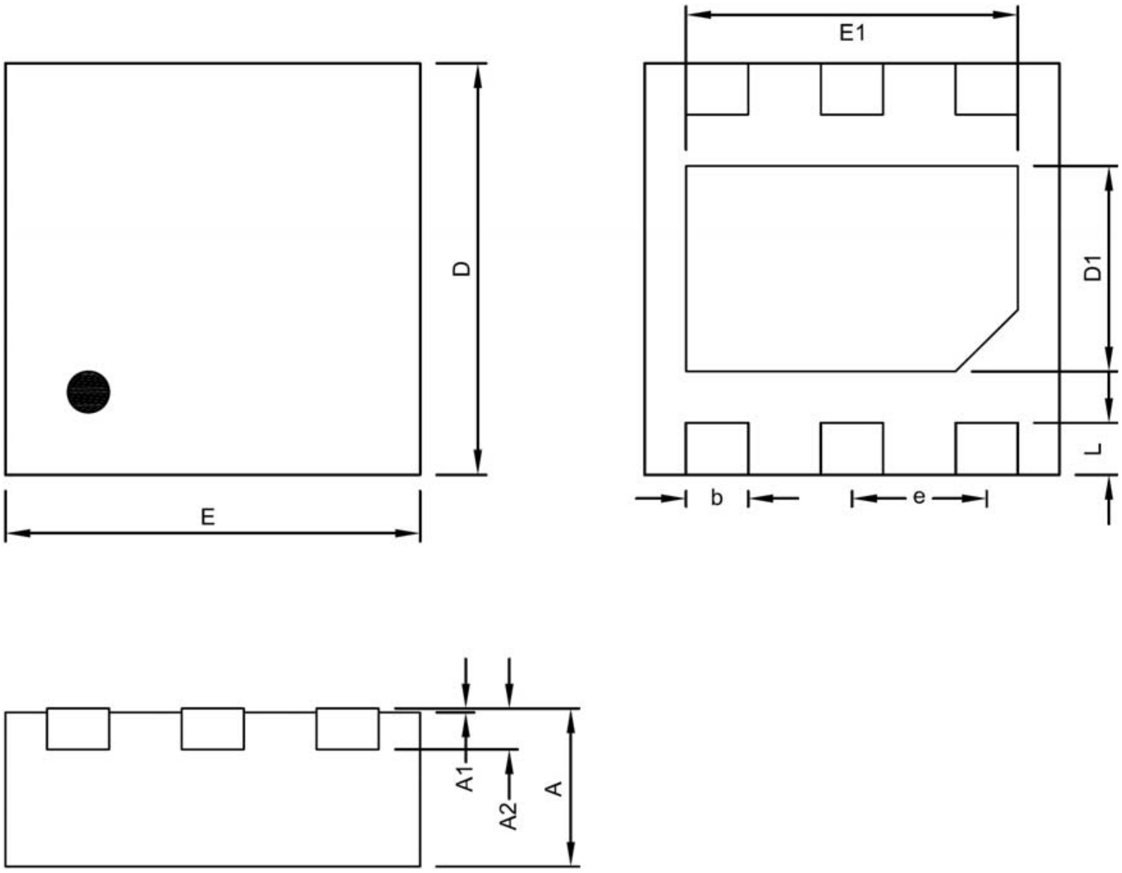
SOT-23-6 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.95	1.10	1.45	0.037	0.043	0.057
A1	0.00	- - -	0.15	0.000	- - -	0.006
A2	0.90	1.10	1.30	0.035	0.043	0.051
D	2.70	2.90	3.10	0.106	0.114	0.122
E	2.60	2.80	3.00	0.102	0.110	0.118
E1	1.50	1.60	1.70	0.059	0.063	0.067
c	0.08	0.15	0.25	0.003	0.006	0.010
b	0.30	0.40	0.50	0.012	0.016	0.020
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024

Taping Specification



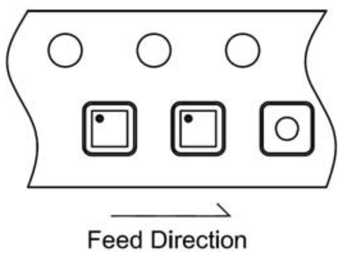
PACKAGE	Q'TY/REEL
SOT-23-6	3,000 ea



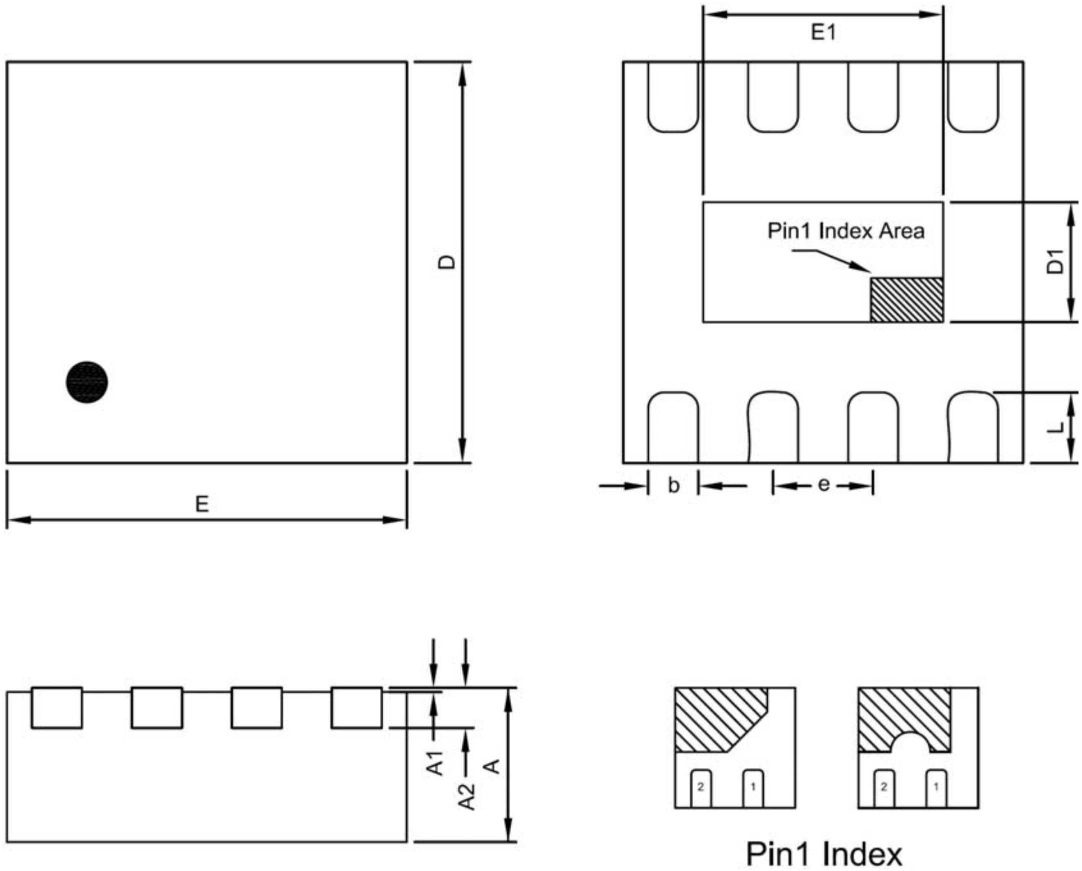
TDFN2X2-6 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	1.95	2.00	2.05	0.0768	0.0787	0.0807
E	1.95	2.00	2.05	0.0768	0.0787	0.0807
D1	0.90	1.00	1.10	0.0354	0.0394	0.0433
E1	1.50	1.60	1.65	0.0591	0.0630	0.0650
b	0.25	0.30	0.35	0.0098	0.0118	0.0138
e	0.65 BSC			0.0256 BSC		
L	0.20	0.25	0.30	0.0079	0.0098	0.0118

Taping Specification



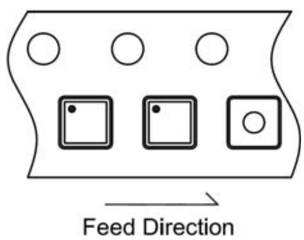
PACKAGE	Q'TY/REEL
TDFN2X2-6	3,000 ea



TDFN2X2-8 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	1.95	2.00	2.05	0.0768	0.0787	0.0807
E	1.95	2.00	2.05	0.0768	0.0787	0.0807
D1	0.55	0.65	0.75	0.0217	0.0256	0.0295
E1	1.15	1.25	1.35	0.0453	0.0492	0.0531
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.30	0.35	0.40	0.0118	0.0138	0.0157

Taping Specification



PACKAGE	Q'TY/REEL
TDFN2X2-8	3,000 ea