RK809
Power Management System
Application Manual

PRELIMINARY CONFIDENTIAL

V1.1

2020-03-10

Fuzhou Rockchip Electronics Co.Ltd

Revision History

Data	Revision	Description
2020-03-10	V1.1	Initial release

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1 SUMMARY

The RK809 is a high-performance power-management integrated circuit (PMIC) integrated Audio Codec for multi-core processor applications that require multiple outputs in single-cell Li-ion battery (including Li-ion and Li-polymer). The RK809 can provide a complete power management and audio management solutions with few external components.

The RK809 provides five high current synchronous step-down converters, 9 LDO regulators, coulombmeter, a real-time clock (RTC), adjustable power-up/power-down sequences and other functions. The RK809 also integrates a set of complete audio sysrem with audio encoder/decoder, MIC input, Head-phone output, ClassD output, I2S interface, etc.

A “battery fuel gauge” is also integrated in the RK809. Using the proprietary algorithms and the sensed battery current and voltage, the fuel gauge can accurately calculate the battery capacity based on the charging/discharging characteristic curve of the battery preloaded in the system. And then send the battery capacity information to the SoC through the I2C interface. There are other functions including tiny-current charging for over-discharged batteries, battery temperature detection, timer for safe charging and chip thermal protection, and so on.

The output voltages of most channels can be configured through the I2C interface. The inputs of all channels have soft start function, which can greatly reduce the inrush current at the startup. Compensating circuits are integrated inside the chip and do not require additional components such as external resistors and capacitors. The 2MHz switching frequency allows small size inductors to be used for buck converters. Also, as all the power switches are integrated on chip, no external power switches and Schottky diodes are needed, which makes the PCB board simple and reduces the system cost significantly.

A real-time clock (RTC) with high stability is also integrated to provide timing function for the processor.

A complete and high-performance audio system is integrated into the RK809, greatly reducing the peripheral circuit. The audio system supports flexible sampling rate configuration, 24bits high-performance DAC decoder, high-performance Head-Phone and Class D PA that provides high-quality audio output; as well as 24bits high-performance ADC encoder and MIC/PGA integration that provide high-quality audio recording function.

The RK809 is available in a QFN68 7.0 mm x 7.0 mm package, with a 0.35-mm pin pitch.

2 FEATURES

- Input range: 2.7V - 5.5V
- Accurate battery fuel gauge
- Real time clock（RTC）
- Ultra low standby current less than 40uA (at 32.768KHz clock frequency)
- Excellent transient response provided by ripple-controlled architecture
- OTP Programmable voltage and power up/down sequences by I2C interface
- Circuit architecture with high conversion efficiency of autonomous IP
- Real ground HeadPhone driver
- 1.3W ClassD PA Driver
- High performance Audio encoder/decoder CODEC
  - One internal PLL
  - Support microphone input
  - Support I2S as the digital signal interface
  - Support programmable digital and analog gains
  - Sampling rate can be up to 192KHz
  - Provide master and slave work mode
  - Support PDM mode (external input PCLK)
  - Support 24bits and 16bits resolutions
- Power channels:
  - CH1: Synchronous BUCK converter,2.5A max
  - CH2: Synchronous BUCK converter,2.5A max
  - CH3: Synchronous BUCK converter,1.5A max
  - CH4: Synchronous BUCK converter,1.5A max
  - CH5: Synchronous BUCK converter,2.5A max
  - CH6-CH7, CH9-CH14: LDOs, 400mA max
  - CH8: Low noise, high PSRR LDO,100mA max
- Fixed and OTP programmable power up sequences
- Package:7mmx7mm QFN68

3 TYPICAL APPLICATION

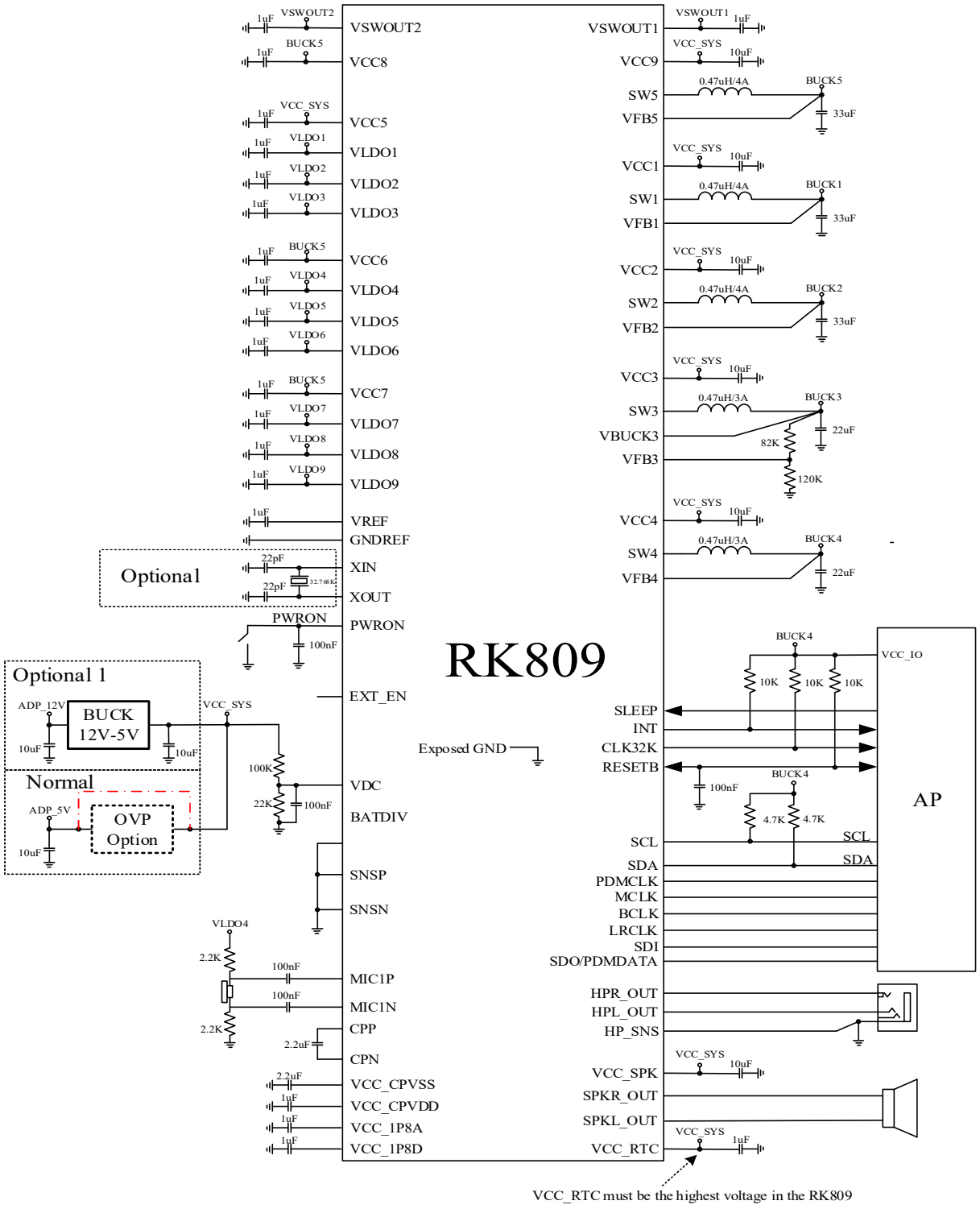

Fig.3-1 RK809 Typical Application Diagram with no battery

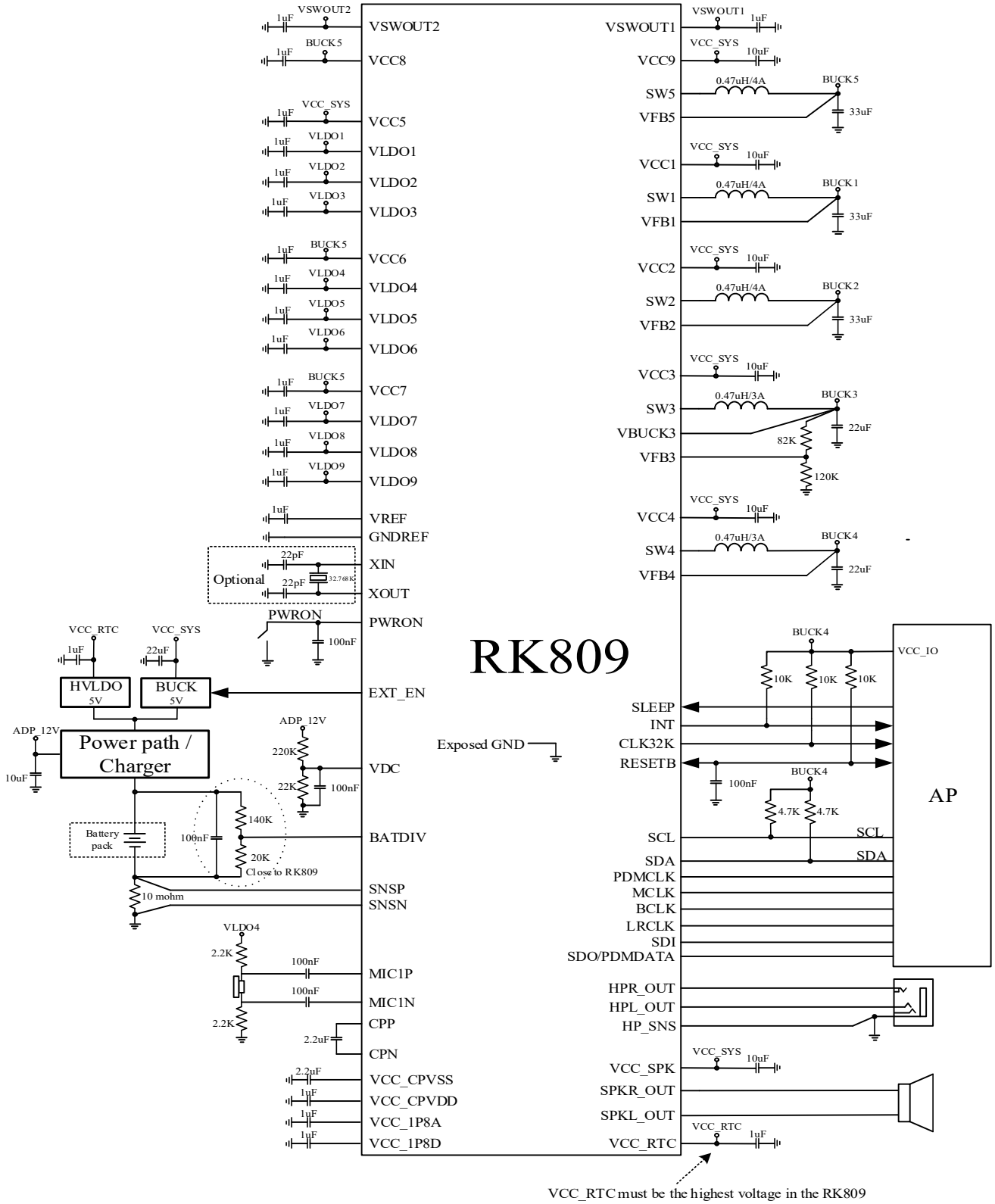

Fig.3-2 RK809 Typical Application Diagram with two batteries

4 PIN DESCRIPTION

QFN68 7mm x 7mm, pitch0.35mm

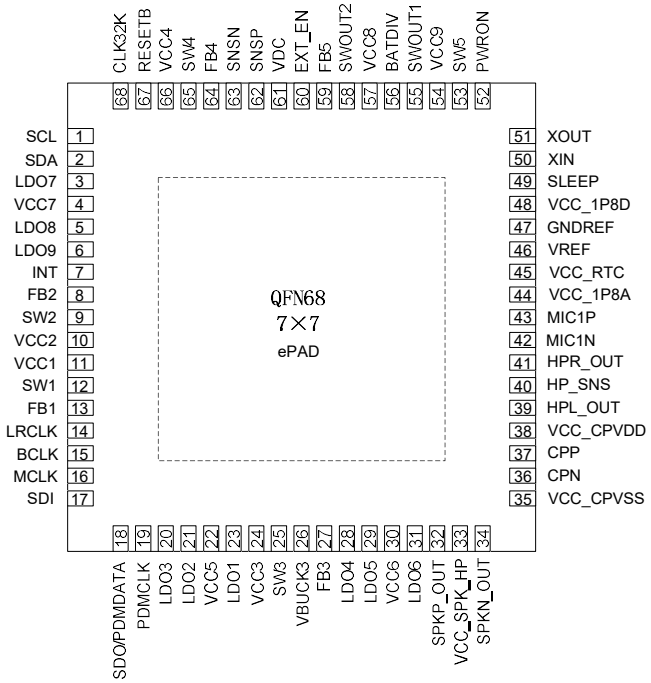

Fig.4-1 Pin Assignment

5 PINOUT DEFINITION

Table.1 Pinout Definition

PIN NO	PIN NAME	PIN DESCRIPTION
1	SCL	I2C clock input
2	SDA	I2C data input and output
3	LDO7	LDO7 output
4	VCC7	Power supply of LDO7/8/9
5	LDO8	LDO8 output
6	LDO9	LDO9 output
7	INT	Interrupt request pin, open drain
8	FB2	Output feedback voltage of buck2
9	SW2	Switching node of buck2
10	VCC2	Power supply of buck2
11	VCC1	Power supply of buck1
12	SW1	Switching node of buck1

PIN NO	PIN NAME	PIN DESCRIPTION
13	FB1	Output feedback voltage of buck1
14	LRCLK	The I2S framing clock
15	BCLK	The I2S bit clock
16	MCLK	The I2S main clock input pin
17	SDI	The I2S DAC input data
18	SDO/PDMDATA	The I2S ADC output data/PDM Data for the DSADC
19	PDMCLK	PDM CLK for the DSADC OUTPUT
20	LDO3	LDO3 output
21	LDO2	LDO2 output
22	VCC5	Power supply of LDO1/2/3
23	LDO1	LDO1 output
24	VCC3	Power supply of buck3
25	SW3	Switching node of buck3
26	VBUCK3	Output voltage of buck3
27	FB3	Output feedback voltage of buck3
28	LDO4	LDO4 output
29	LDO5	LDO5 output
30	VCC6	Power supply of LDO4/5/6
31	LDO6	LDO6 output
32	SPKP_OUT	Positive speaker driver output
33	VCC_SPK_HP	Power supply for speaker and charger pump
34	SPKN_OUT	Negative speaker driver output.
35	VCC_CPVSS	Negative power supply for the headphone
36	CPN	Negative switching node of the charger pump
37	CPP	Positive switching node of the charger pump.
38	VCC_CPVDD	Positive power supply for the headphone
39	HPL_OUT	Left channel output of the headphone
40	HP_SNS	Reference ground for the headphone
41	HPR_OUT	Right channel output of the headphone
42	MICIN	Negative input of the Microphone
43	MICIP	Positive input of the Microphone
44	VCC_1P8A	Power supply for internal 1.8V analog circuit
45	VCC_RTC	Power supply filter
46	VREF	Internal reference voltage
47	GNDREF	Reference ground
48	VCC_1P8D	Power supply for internal 1.8V digital circuit
49	SLEEP	Sleep mode control input

PIN NO	PIN NAME	PIN DESCRIPTION
50	XIN	32.768KHz crystal oscillator input
51	XOUT	32.768KHz crystal oscillator output
52	PWRON	Power on key input, active low, internal 17k resistor pull high to VCC_RTC
53	SW5	Switching node of BUCK5
54	VCC9	Power supply of buck5 and SWOUT1
55	SWOUT1	Power switch out 1
56	BATDIV	Divided voltage of positive battery
57	VCC8	Power supply of SWOUT2
58	SWOUT2	Power switch out 2
59	FB5	Output feedback voltage of buck5
60	EXT_EN	Enable Signal for external high voltage BUCK
61	VDC	If it exceeds 0.55V for the first time, it will start the PMIC(rising edge triggering start).And it is connected to the divider of external power supply generally.
62	SNSP	Bat charging and discharging sense current positive pin
63	SNSN	Bat charging and discharging sense current negative pin
64	FB4	Output feedback voltage of buck4
65	SW4	Switching node of buck4
66	VCC4	Power supply of buck4
67	RESETB	Reset pin after power on, active low
68	CLK32K	32.768KHz clock output, open drain
Exposed pad	Exposed ground	Ground

6 APPLICATIONS INFORMATION

6.1 BUCK1/2

Due to the high integration, the peripheral connection of BUCK1/2 will be very simple. Just need to connect input capacitors, output capacitors and inductors.

Input capacitors recommendation: the full-load current of BUCK1/2 is 2.5A, for better filter of the input ripple current, it is recommended that the input capacitance should not be less than 10uF and the withstand voltage should not be less than 6.3V.

Output capacitors recommendation: Considering the output ripple in steady-state, loop stability amd the speed of transient response, it is recommended that the output capacitance should not be less than 22uF and the withstand voltage should not be less than 6.3V.

Inductor recommendation: Since the full-load current is 2.5A and the switching frequency is 2MHz, assuming the inductor current ripple is about 40 percent of the full-load current ripple, it is recommended to select the inductor with 0.47uH. The maximun peak current can be set at 4A, so the saturation current of inductor should be greater than 4.5A. For better conversion efficiency, select the inductor with Direct Current Resistance (DCR) less than 20mΩ.

PCB design recommendation: During PCB design, the input capacitors must be placed as close to the chip as possible and the circuit between the input capacitor and VCC1/2, GND should be kept as small as possible. Make sure the trace of SW1/2 should be as short as possible in case it disturbs other modules, and the trace of VFB1/2 should be kept away from the SW1/2 as possible as you can. For vias, the VCC1/2 require at least 3 vias of 05/03 perforations, and the VBUCK1/2 require at least 5 vias of 05/03 perforations. Need to pay attention to that for the best filtering effect, the quantity of vias between the negative and the positive of the input/output capacitors should be the same.

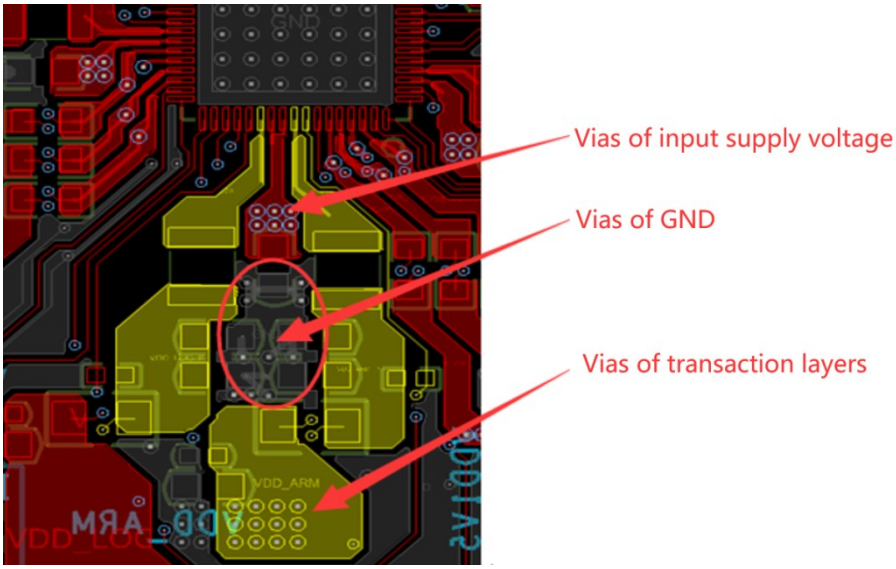

Fig.6-1 Reference of Vias

The BUCK of RK809 uses the ripple-controlled architecture which has better transient response than peak current mode, and smaller output capacitors to save costs.

6.2 BUCK3

Due to the high integration, the peripheral connection of BUCK3 will be very simple. Just need to connect input capacitors, output capacitors and inductors and feedback divider resistors. VOUT=0.8*(1+RH/RL), which RH and RL are divider resistors in different directions. (BUCK3 also can be configured to regulate voltage by inner resistors through the register, while the pins of VBUCK3 and FB3 are connected together.)

Input capacitors recommendation: the full-load current of BUCK3 is 1.5A, for better filter of the input ripple current, it is recommended that the input capacitance should not be less than 10uF and the withstand voltage should not be less than 6.3V.

Output capacitors recommendation: Considering the output ripple in steady-state, loop stability amd the speed of transient response, it is recommended that the output capacitance should not be less than 22uF and the withstand voltage should not be less than 6.3V.

Inductor recommendation: Since the full-load current is 1.5A and the switching frequency is 2MHz, assuming the current ripple of inductor is about 40 percent of the full- load current ripple, it is recommended to select the inductor with 0.47uH or 1uH. The maximun peak current can be set at 3A, so the saturation current of inductor should be greater than 3.5A. For better conversion efficiency, select the inductor with the Direct Current Resistance (DCR) less than 20mΩ.

Divider resistors recommendation: The reference voltage is 0.8V, so the divider resistors should be calculated by the formula:RH=(VBUCK3-0.8)*RL/0.8, which RH and RL are divider resistors in different directions.The recommended resistance range is between 10KΩ and 1MΩ. For example, if the VBUCK3 is 1.25V，when the RL is 100KΩ, the RH is 56.2KΩ according the formula.

PCB design recommendation: During PCB design, the input capacitors must be placed as close to the chip as possible and the circuit between the input capacitor and VCC3, GND should be kept as small as possible. Make sure the trace of SW3 should be as short as possible in case it disturbs other modules, and the trace of VFB3 should be kept away from the SW3 as possible as you can. For vias, the VCC3 require at least 2 vias of 05/03 perforations, and the VBUCK3 require at least 3 vias of 05/03 perforations.

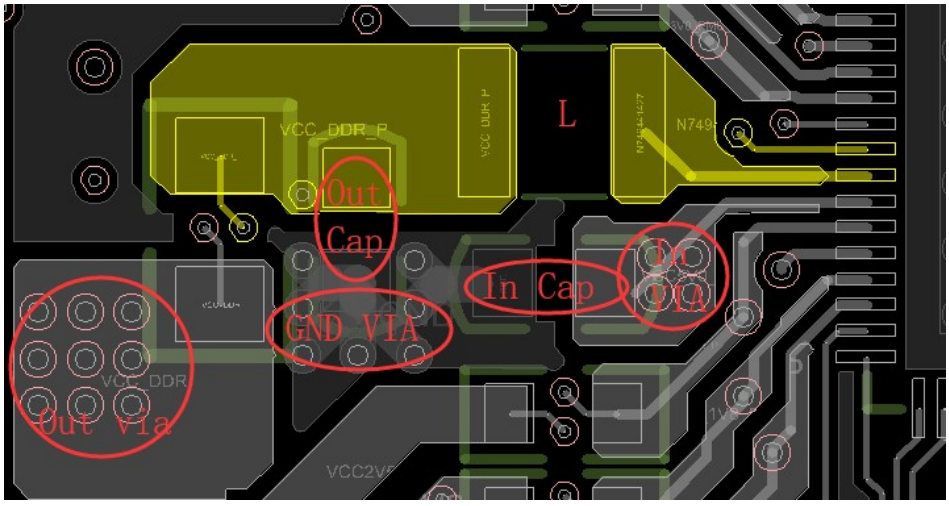

Fig.6-2 Reference of Vias

6.3 BUCK4

Due to the high integration, the peripheral connection of BUCK4 will be very simple. Just need to connect input capacitors, output capacitors and inductors.

Input capacitors recommendation: the full-load current of BUCK4 is 1.5A, for better filter of the input ripple current, it is recommended that the input capacitance should not be less than 10uF and the withstand voltage should not be less than 6.3V.

Output capacitors recommendation: Considering the output ripple in steady-state, loop stability amd the speed of transient response, it is recommended that the output capacitance should not be less than 22uF and the withstand voltage should not be less than 6.3V.

Inductor recommendation: Since the full-load current is 1.5A and the switching frequency is 2MHz, assuming the current ripple of inductor is about 40 percent of the full- load current ripple, it is recommended to select the inductor with 0.47uH or 1uH. The maximun peak current can be set at 3.5A, so the saturation current of inductor should be greater than 4A. For better conversion efficiency, select the inductor with the Direct Current Resistance (DCR) less than 20mΩ.

PCB design recommendation: During PCB design, the input capacitors must be placed as close to the chip as possible and the circuit between the input capacitor and VCC4, GND should be kept as small as possible. Make sure the trace of SW4 should be as short as possible in case it disturbs other modules, and the trace of VFB4 should be kept away from the SW4 as possible as you can. For vias, the VCC4 requires at least 2 vias of 05/03 perforations, and the VBUCK4 requires at least 3 vias of 05/03 perforations.

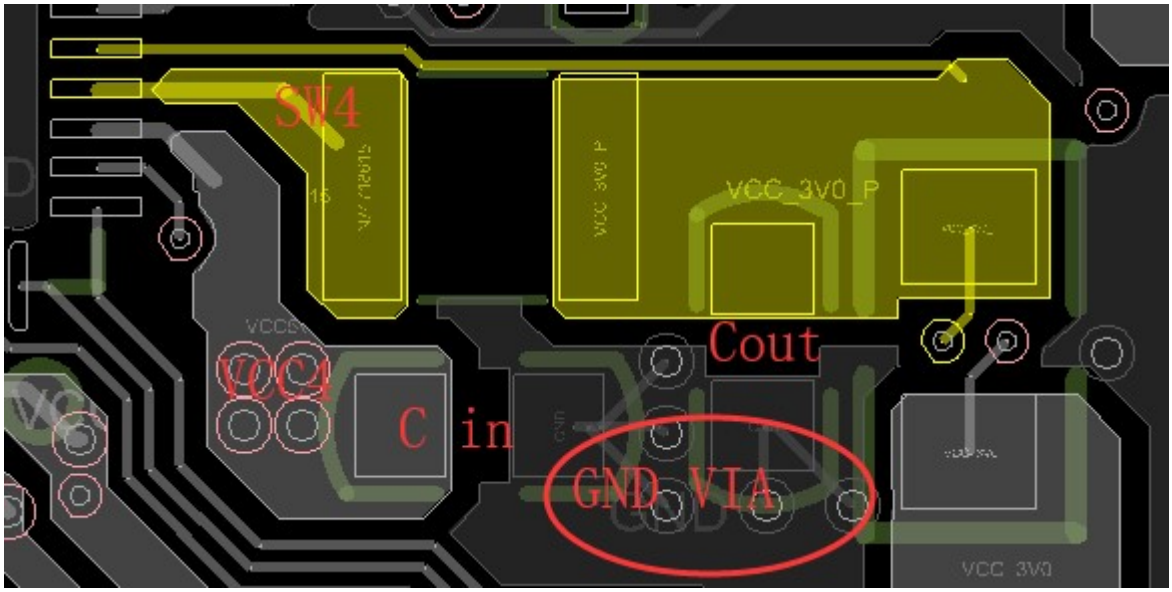

Fig.6-3 Reference of Vias

6.4 BUCK5

Due to the high integration, the peripheral connection of BUCK5 will be very simple. Just need

to connect input capacitors, output capacitors and inductors.

Input capacitors recommendation: the full-load current of BUCK5 is 2.5A, for better filter of the input ripple current, it is recommended that the input capacitance should not be less than 10uF and the withstand voltage should not be less than 6.3V.

Output capacitors recommendation: Considering the output ripple in steady-state, loop stability amd the speed of transient response, it is recommended that the output capacitance should not be less than 33uF and the withstand voltage should not be less than 6.3V.

Inductor recommendation: Since the full-load current is 2.5A and the switching frequency is 2MHz, assuming the current ripple of inductor is about 40 percent of the full- load current ripple, it is recommended to select the inductor with 0.47uH or 1uH. The maximun peak current can be set at 4A, so the saturation current of inductor should be greater than 4A. For better conversion efficiency, select the inductor with the Direct Current Resistance (DCR) less than 20mΩ.

PCB design recommendation: During PCB design, the input capacitors must be placed as close to the chip as possible and the circuit between the input capacitor and VCC9, GND should be kept as small as possible. Make sure the trace of SW5 should be as short as possible in case it disturbs other modules, and the trace of VFB5 should be kept away from the SW5 as possible as you can. For vias, the VCC9 requires at least 2 vias of 05/03 perforations, and the VBUCK5 requires at least 3 vias of 05/03 perforations.

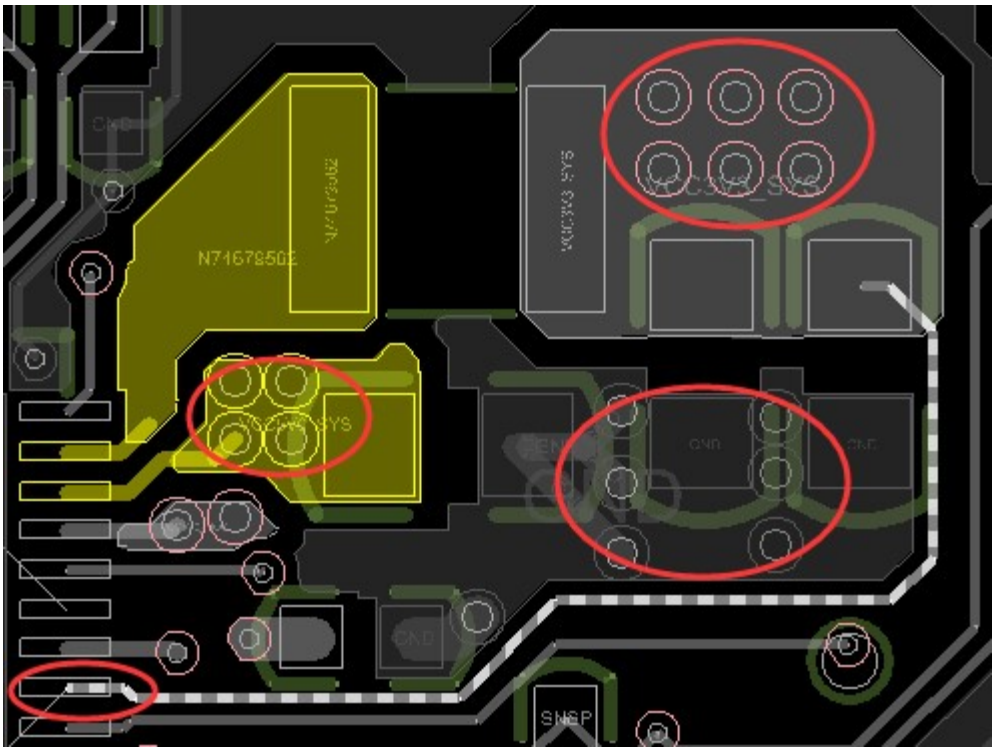

Fig.6-4 Reference of Vias

6.5 LDO

The RK809 also integrates nine LDOs, with LDO1, LDO2, LDO4-LDO8 and LDO9 capable of providing up to 400mA with load. Recommend to select the output capacitors with 1uF and the

withstand voltage 6.3V. The LDO3 is a low noise LDO which provides maximum 100mA with full-load. Recommend to select the output capacitors with 1uF and the withstand voltage 6.3V.

LDO1, LDO2 and LDO3 share an input power supply VCC5 and it is recommended to add a 1.0uF input capacitor with the withstand voltage 6.3V. LDO4, LDO5 and LDO6 share an input power supply VCC6 and it is recommended add a 1.0uF input capacitor with the withstand voltage 6.3V. LDO7, LDO8 and LDO9 share an input power supply VCC7 and it is recommended to add a 1.0uF input capacitor with the withstand voltage 6.3V.

The LDOs of RK809 optimize the loop compensation, requiring only 1.0uF output capacitors to achieve the stable output and cost saving at the same time.

6.6 Battery Fuel Gauge

The battery fuel gauge of RK809 combines the coulombmeter integral algorithm and the open-circuit voltage (OCV) algorithm, taking advantage of the accuracy of the coulombmeter integral algorithm in the case of large current and also considering the precise characteristics of the open-circuit voltage algorithm in the case of small current.

The core algorithm of fuel gauge: The RK809 collects the battety current in real-time, calculates the capacity by the method of integration, and finally gets the state of charge (SOC).

If the shutdown time is long enough (the battery exits the status of polarization), when powered on, the register of OCV will update SOC by looking up the table. When the system current is small, such as in sleep mode, the RK809 will update the voltage and current of RELAX when the collected current is small enough. When the software detects that the flag bit of RELAX becomes high, the voltage will be regarded as the OCV of the battery and then the SOC will be updated by looking up the table.

When the charger charges the battery from less than 20 percent to 100 percent, and there are two RELAX voltage values, the total battery level FCC will be updated.

Notices for using the fuel gauge:

1. The pins of 56, 62 and 63 should be connected to GNG and can not be suspended when the fuel gauge is not used.
2. The divider resistors and filter capacitors that are connected to the pins of 56, 62 and 63 should be placed as close to the chip as possible.

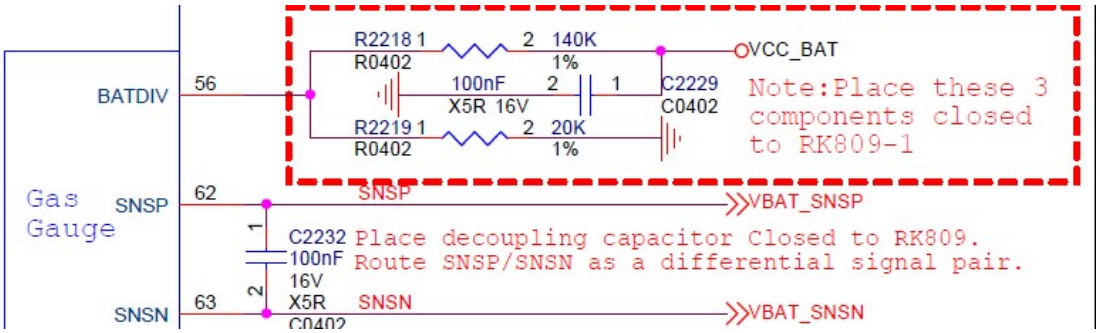

Fig.6-5 Reference Design of Fuel Gauge

3. The current sampling resistor (10mR) should be placed next to the battery holder (not close to the RK809) to minimize the return path of the negative of the battery.

4. The nets of SNSN and SNSP should be connected to the two ends of 10mR resistor, in order to prevent the net of SNSN from being short connected to GND in the operation of copper pour. Please place a 0R resistor close to the 10mR resistor and set the area of KEEPOUT between GND and the resistor.

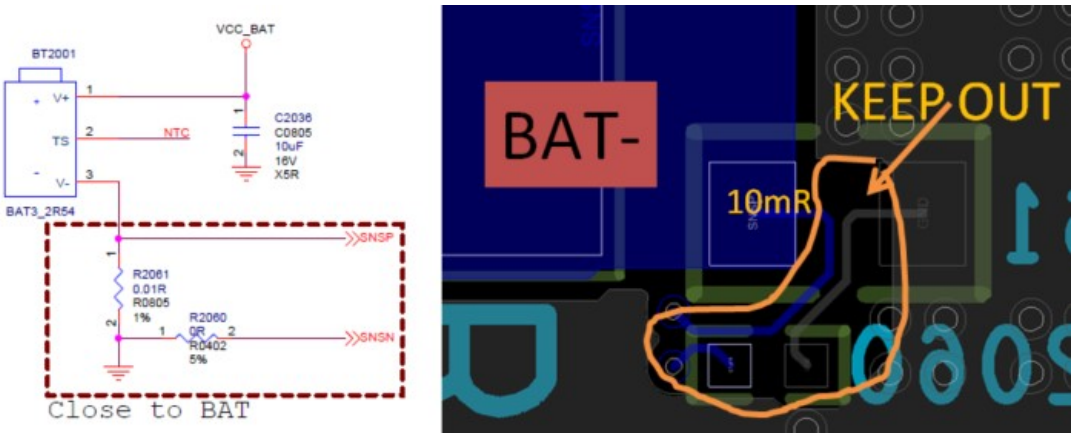

Fig.6-6 Reference Design of Sample Resistance

6.7 Crystal Oscillator

The crystal circuit must be away from SW1, SW2, SW3, SW4 and SW5 since it is sensitive. **In order to prevent interference, it is necessary to use GND to separate the XIN and XOUT.**

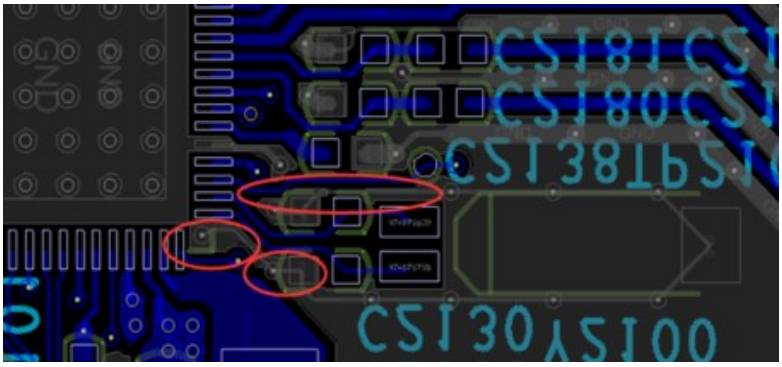

Fig.6-7 Reference Design of Oscillator

6.8 Power on/Power down conditions

Power up process by triggering VDC:

1、 The pin of VCC_RTC is in high level and is generally higher than 3.0V
2、 The pin of VDC is higher than 0.55V
3、 The output of EXT_EN will be high
4、 The voltage of VCC9 exceeds 3.0V in 1.5ms when the output of EXT_EN is high (otherwise it does not power on)
5、 The power up process is started， and each LDO and DCDC start up with a preset power

up sequence

6、 The VDC can be pulled down or kept high after power-on, not affecting the power-on state any more.

Power up process by pressing the PWRKEY:

1、 The pin of VCC_RTC is in high level and is generally higher than 3.0V
2、 The pin of PWRON is pulled down for more than 500ms
3、 The output of EXT_EN will be high
4、 The voltage of VCC9 exceeds 3.0V in 1.5ms when the output of EXT_EN is high (otherwise it does not power on)
5、 The power up process is started， and each LDO and DCDC start up with a preset power up sequence

Power up process of ALARM:

1、 The pin of VCC_RTC is in high level and is generally higher than 3.0V
2、 When time is up, the timing boot up function is enabled
3、 The output of EXT_EN will be high
4、 The voltage of VCC9 exceeds 3.0V in 1.5ms when the output of EXT_EN is high (otherwise it does not power on)
5、 The power up process is started, and each LDO and DCDC start up with a preset power up sequence

Power down process：

1、 The voltage VCC9 is lower than the undervoltage design value
2、 Shutdown by I2C commands
3、 Power down due to overtemperature protection（145℃）
4、 Long press the PWRKEY over 6 seconds to forcedly shutdown

6.9 Power Supply of Chip

VCC_RTC: The VCC_RTC (Pin45) is a pin that associated with digital logic, partial analog control, and the power supply of RTC clock inside the RK809 chip. It is required that the supply voltage must be the highest (or greater than Vmax-0.3V) in all supply pins of the RK809. The pin of VCC_RTC must be the first one to be powered up, or be powered up simultaneously with other power supplies. Other power supplies are not allowed to be powered up before the pin of VCC_RTC.

GPIO: The pins of SDA, SCL, INT, CLK32K and RESETB are open-drain outputs and the maximum input voltage available is the voltage of the VCC_RTC. As input, the VL/VH of SCL, SDA, SLEEP, PWRON and RESETB is fixed at 0.4V/1.26V.

I2S: The VCCIO of LRCK, BCLK, MCLK, SDI and PDMCLK are connected to LDO4, so generally LDO4 is also allocated to supply power for the I2S power domain.

LDOs power supply: The pins of VCC5, VCC6 and VCC7 are powering the LDOs with a minimum voltage of 2V, but the output current will drop to half of the rated output with 2V input.

VCC9: It is not only the power pin of VSWOUT1 and BUCK5, but also a detection pin that enables undervoltage and overvoltage protection. If the voltage of VCC9 is less than 3.0V, the sysytem will automatically shut down after power up.

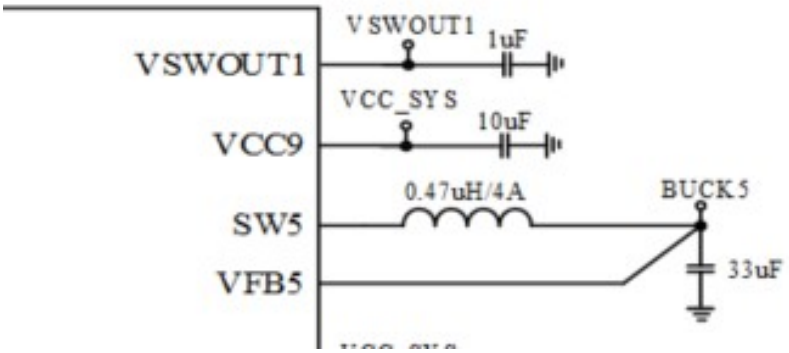

Fig.6-8 Reference Design of VCC9

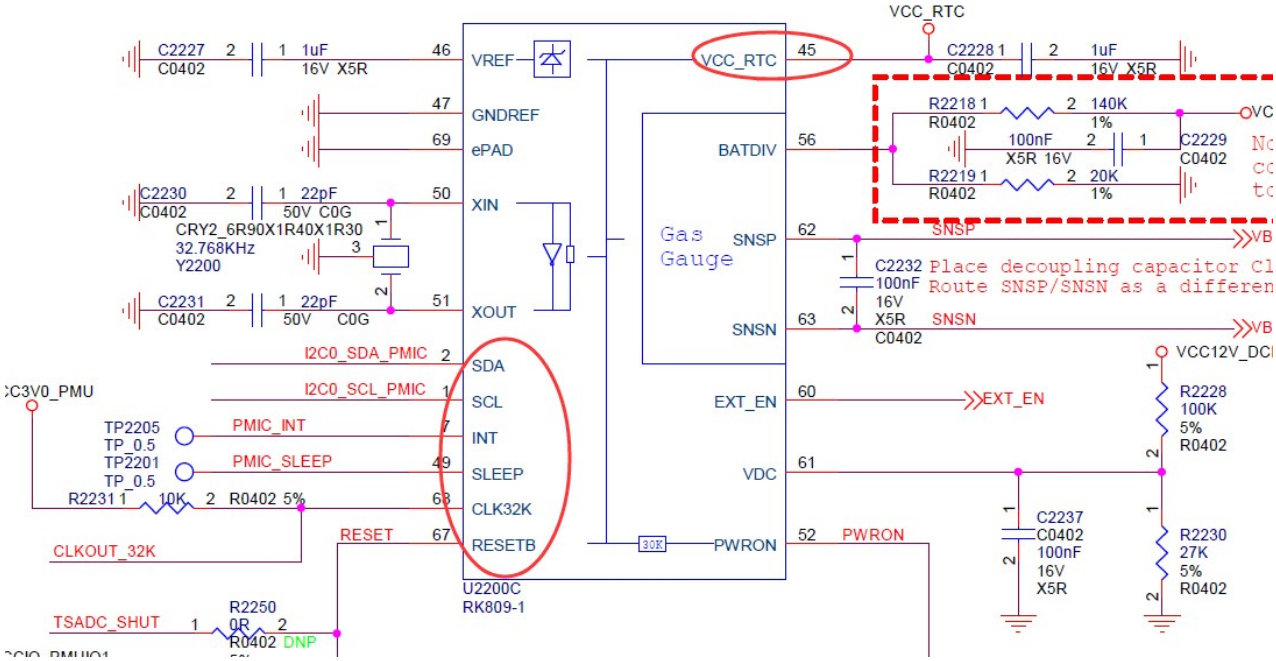

Fig.6-9 Reference Design of Power Supply

6.10 Audio System

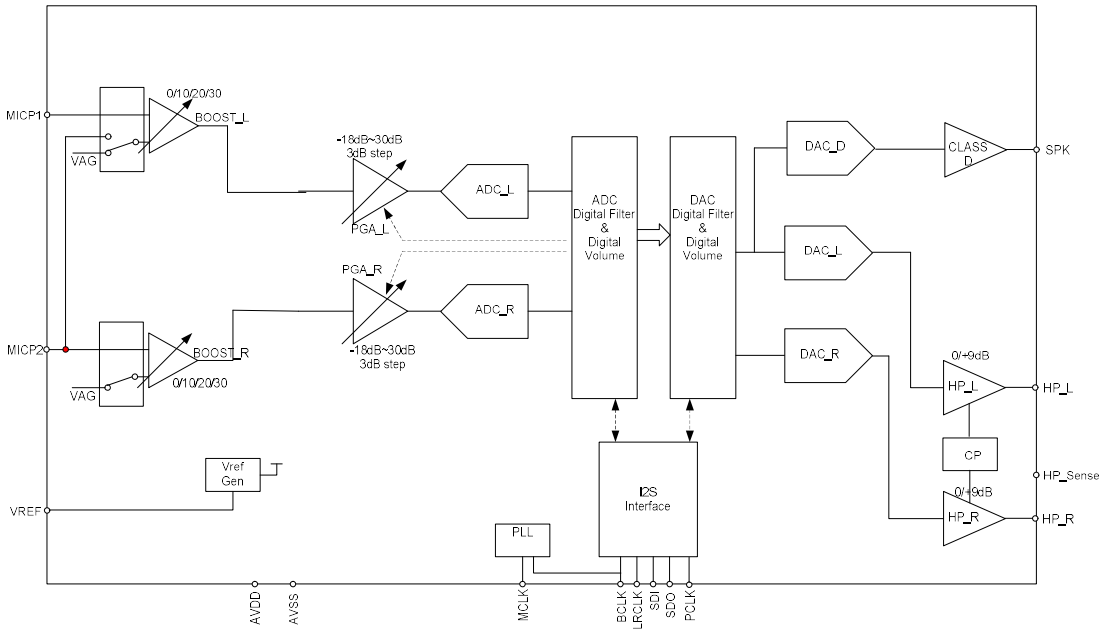

Fig.6-10 Internal Structure of Audio System

The RK809 supports I2S for the digital audio data interface. The I2S/PCM audio digital interface is used to input data to a stereo DAC or output data from a stereo ADC. The I2S/PCM audio interface can be configured as Master mode or Slave mode. In Master Mode, BCLK and LRCLK are provided by RK809, but MCLK is provided by external components. In Slave Mode, BCLK and LRCLK are provided by external components.

The RK809 integrates high-performance stereo ADC and DAC. The audio recording path is composed of MIC, PGA and audio ADC. The audio placback path is composed of DAC, HP or CLASS D.

The RK809 integrates HP-Driven sampling architecture with positive and negative power supplies for better THD performance. The Class-D type amplifier can provide 1.3W output.

Layout：

HP_L/HP_R should be surrounded by GND separately and can not be leaned together, in case of reducing the isolation of left and right channels.

HP_SNS should be pulled to the back of the headphone jack and then connected to the ground. HP_SNS is used to compensate the input signal and also improve isolation of the left and right channels.

MICCP1/MICP2 can be connected to two single-ended input or a differential input. As the differential input, please follow the rules of differential pairs, while they should be surrounded by GND separately as single-ended input.

ClassD: The chip integrates EMI and EMI components can be reserved as backup if not enough.

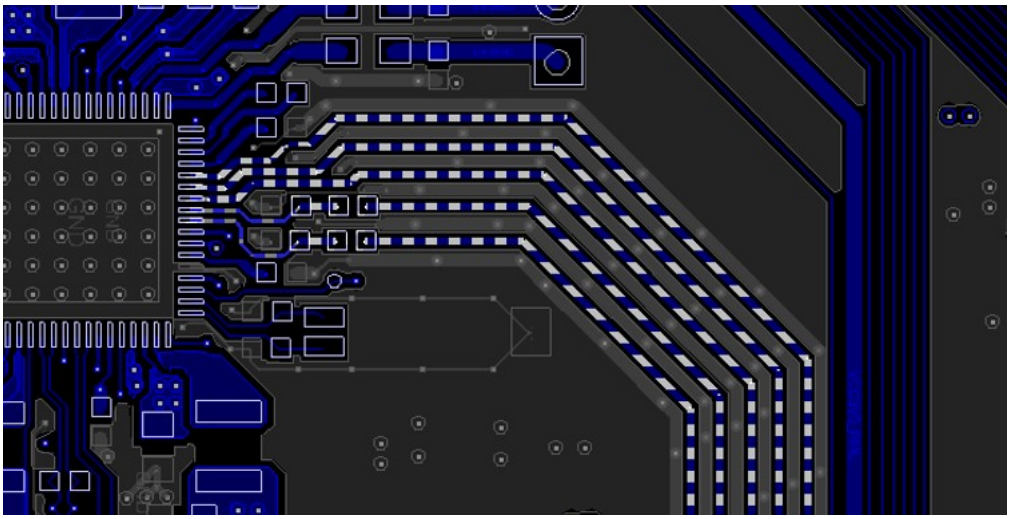

Fig.6-11 Reference Design of Audio System