GC4C33 COB

1/2.7” 4Mega CMOS Image Sensor

Datasheet

V1.1

2019-03-20

Ordering Information

◆ **GC4C33-WA1X6**

(4cell, 150um, back grinding, reconstructed wafer)

GENERATION REVISION HISTORY

REV.	*EFFECTIVE DATE*	*DESCRIPTION OF CHANGES*	*AUTHOR*
V0.0	*2018-08-08*	*Preliminary Version*	*Melinda Zhang*
V0.1	*2018-08-16*	*Update Peripheral circuit diagram*	*Jambo*
V0.2	*2018-08-22*	*Update Two-wire Serial Bus Communication*	*Jambo*
V1.0	*2019-01-07*	*Update feature* *Update Specification* *Update Operation Current* *Update DC Characteristics* *Update Pin Description* *Update QE*	*Tony*
V1.1	*2019-03-20*	*Update DC Characteristics* *Update Die Size*	*Tony*

Galaxycore Incorporation

Content

1. Sensor Overview

1.1 General Description

GC4C33 is a high quality 4Mega CMOS image sensor, for security camera products, digital camera products and mobile phone camera applications. GC4C33 incorporates a 2560H x 1440V pixel array, on-chip 12/10-bit ADC, and image signal processor.

The full-scale integration of high-performance makes the GC4C33 fit the design and reduces the implementation process.

It provides RAW12 and RAW10 data formats with MIPI interface. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

1.2 Features

- Standard optical format of 1/2.7 inch
- 2.24μm×2.24μm BSI pixel
- Output formats: Raw Bayer 12bit/10bit
- 12bit ADC
- MIPI(4_lane)interface support
- PLL support
- Support for frame sync
- 2-exposure staggered HDR support
- Horizontal/Vertical mirror
- OTP support (30bytes for customers): Module information/WB
- Hardware de-mosaic inside

1.3 Application

- Security cameras
- Automotive
- Cellular Phone Cameras
- Digital still cameras and camcorders
- Video telephony and conferencing equipment

1.4 Technical Specifications

Parameter	Typical value
Optical Format	1/2.7 inch
Pixel Size	2.24μm x 2.24μm(BSI)
Active pixel array	2560 x 1440
Shutter type	Electronic rolling shutter
ADC resolution	12/10-bit ADC
Max Frame rate	60fps@full size 30fps@HDR 240fps@720p
Power Supply	AVDD28: 2.8 V DVDD: 1.2V IOVDD: 1.8V
Power Consumption	214mW@30fps 4lane
SNR	40dB
Dark Current	TBD
Sensitivity	3.99V/lus-sec@530nm
Dynamic range	66dB linear
Operating temperature:	-20 ~ 70℃
Stable Image temperature	0~60℃
Storage temperature	-40~125℃
Max Optimal lens chief ray angle(CRA)	35.40 °(non-linear)
Package type	COB

2. DC Characteristics

2.1 Standby Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	TBD	TBD	uA
Digital	I_{DVDD}	—	TBD	TBD	uA
I/O	I_{IOVDD}	—	TBD	TBD	uA

RST: L, PWND: L, MCLK: L/H
Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, T_j=25℃

2.2 Power off Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	0	0	uA
Digital	I_{DVDD}	—	0	0	uA
I/O	I_{IOVDD}	—	0	0	uA

Power off, T_j=25℃

2.3 Operation Current

- **Full size (MIPI 4 lane)**

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	18.5	19	mA
Digital	I_{DVDD}	—	133	137	mA
I/O	I_{IOVDD}	—	1.1	1.3	mA

INCLK: 24MHz, Frame rate: 30fps, Raw 10

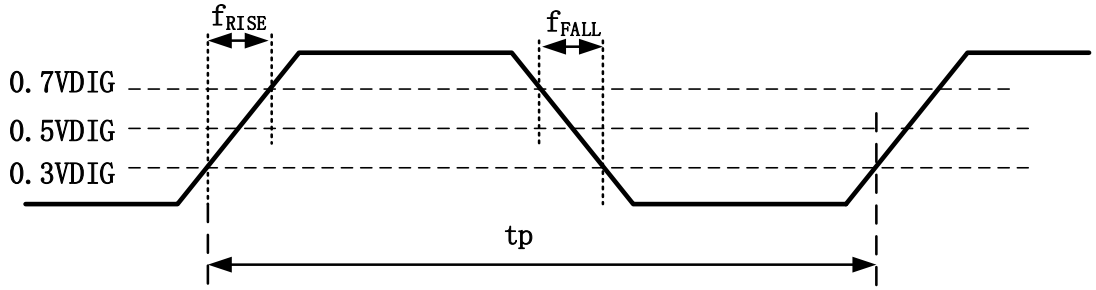
Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, T_j=25℃

2.4 DC Characteristics

Item	Symbol	Min	Typ	Max	Unit
Power supply	V_{AVDD}	2.7	2.8	2.9	V
	V_{DVDD}	1.15	1.2	1.25	V
	V_{IOVDD}	1.7	1.8	2.8	V
Digital Input(Conditions: AVDD = 2.8V, DVDD = 1.2V, IOVDD = 1.8V)					
Input voltage HIGH	**V_{IH}**	0.7*VIF			V
Input voltage LOW	**V_{IL}**			0.3*VIF	V
Digital Output(Conditions: AVDD = 2.8V, IOVDD = 1.8V, standard Loading 25PF)					
Output voltage HIGH	**V_{OH}**	0.8*VIF			V
Output voltage LOW	**V_{OL}**			0.2*VIF	V

3. AC Characteristics

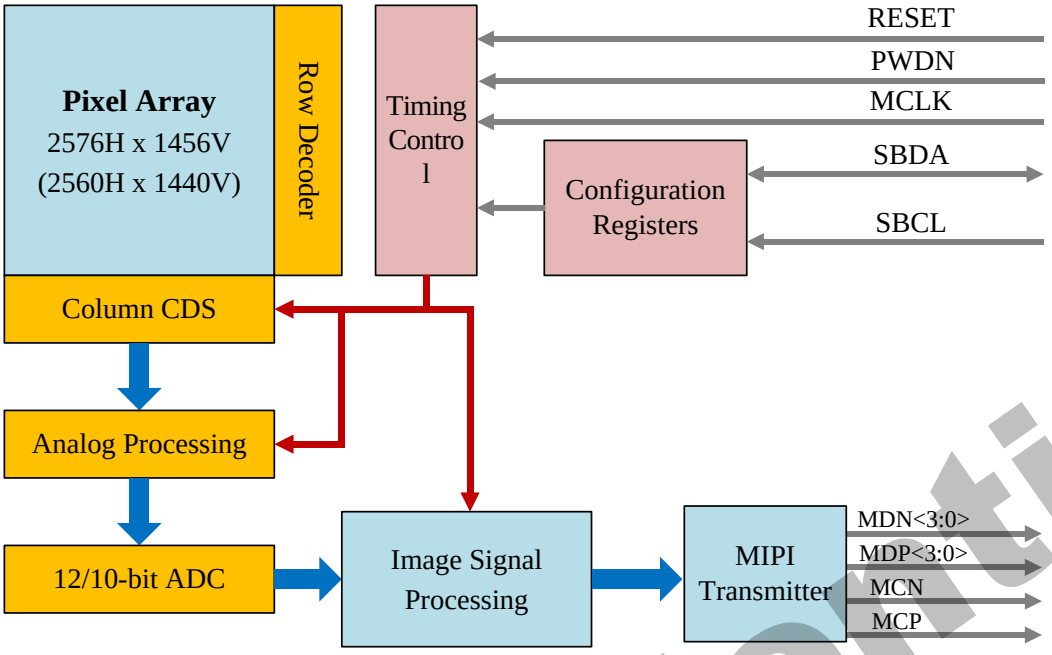
master clock wave diagram



Input clock square waveform specifications：

Item	Symbol	Min.	Typ.	max	unit
Frequency	f_{SCK}	6	24	27	MHz
jitter (period, peak-to-peak)	T_{jitter}			600	ps
Rise Time	f_{RISE}	1		15	ns
Fall Time	f_{FALL}	1		15	ns
Duty Cycle	f_{DUTY}	40		60	%
Input Leakage	f_{ILEAK}	-10		10	μA

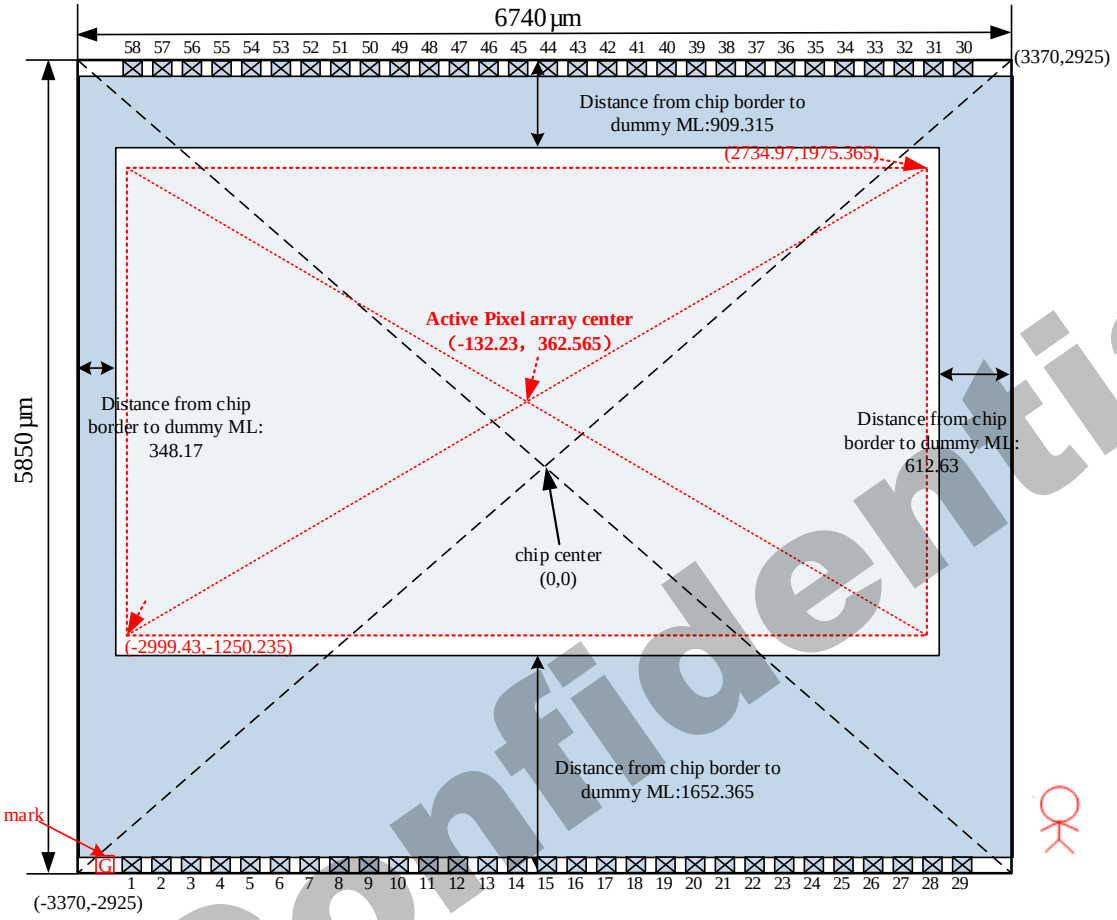
4. Block Diagram



GC4C33 has an active image array of 2560x1440 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The analog signal is transferred to digital signal by 12 bit A/D converter. The digital signals are processed in the ISP Block. Users can easily control these functions via two-wire serial interface bus.

5. Chip Information

5.1 Chip Center and Pin Assignment



Top View

***Die size: 6740 × 5850μm (without scribe line),6820 × 5930μm (with scribe line)**
(6790 ±25μm) × (5900 ±25μm) (RW Package)

***Thickness of die (wafer):150±10μm**

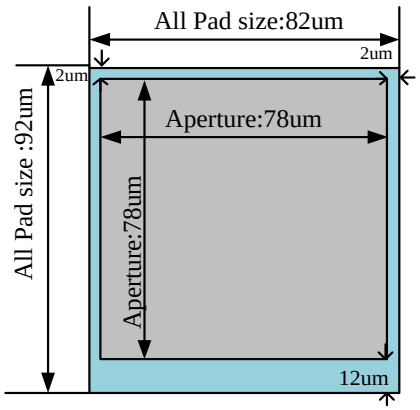
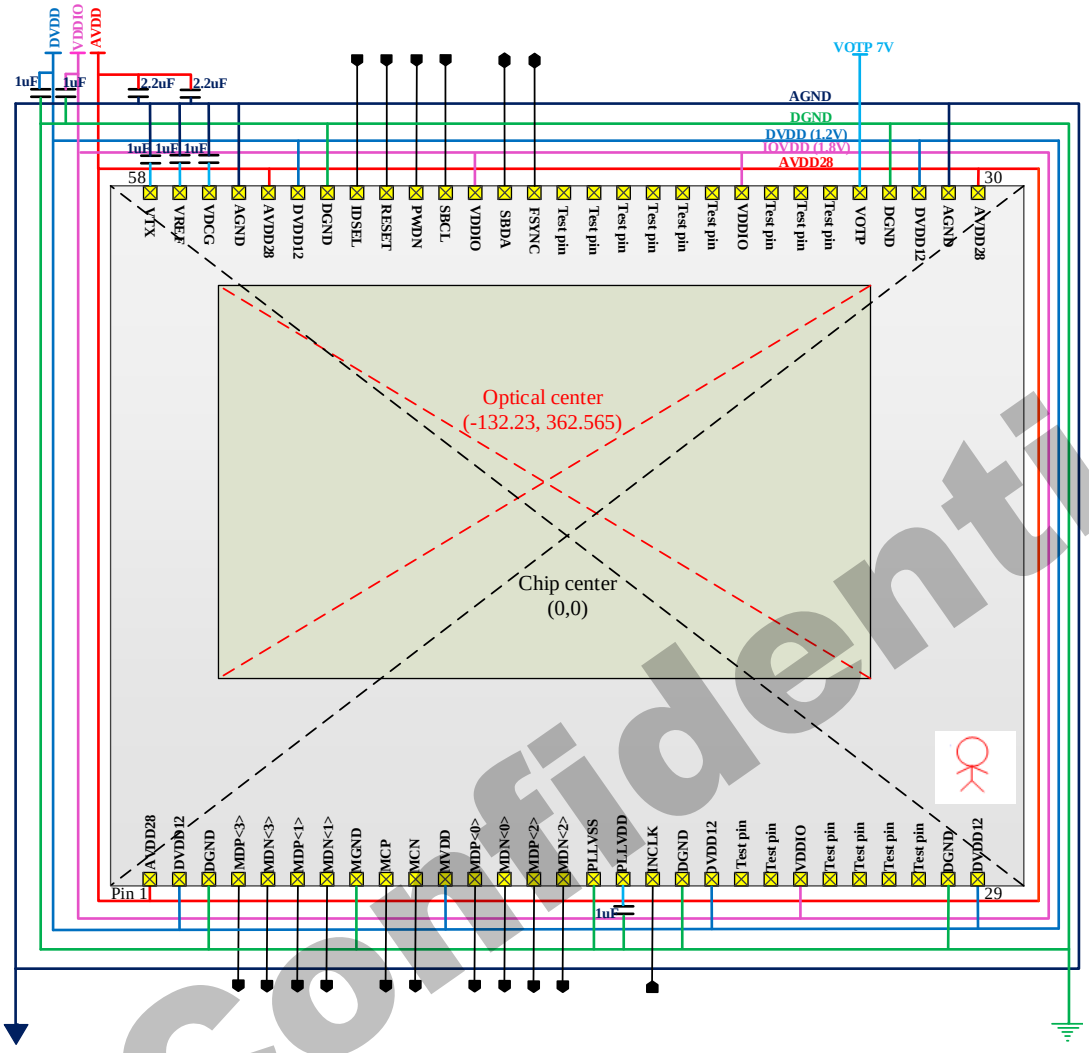


图 3-2 Pad size and aperture

5.2 Peripheral circuit diagram



5.3 Pin Coordinates and Description

Pin	POS X(um)	POS Y(um)	Name	Pin Type	Description
1	-3080	-2871	AVDD28	POWER	Main power supply pin: 2.7~3.0V.
2	-2860	-2871	DVDD12	POWER	Digital power supply pin: 1.15~1.3V.
3	-2640	-2871	DGND	Ground	Ground for digital
4	-2420	-2871	MDP3	Output	MIPI data <3> (+)
5	-2200	-2871	MDN3	Output	MIPI data <3> (-)
6	-1980	-2871	MDP1	Output	MIPI data <1> (+)
7	-1760	-2871	MDN1	Output	MIPI data <1> (-)

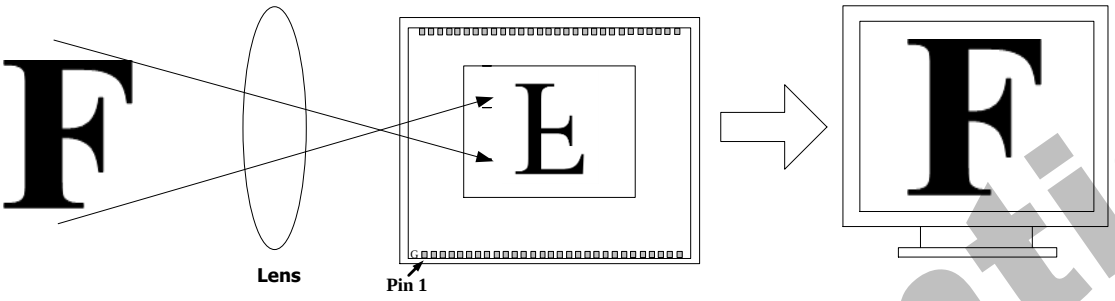
8	-1540	-2871	MGND	Ground	Ground for MIPI
9	-1320	-2871	MCP	Output	MIPI clock (+)
10	-1100	-2871	MCN	Output	MIPI clock (-)
11	-880	-2871	MVDD	Power	MIPI power supply pin: 1.15~1.3V.
12	-660	-2871	MDP0	Output	MIPI data <0> (+)
13	-440	-2871	MDN0	Output	MIPI data <0> (-)
14	-220	-2871	MDP2	Output	MIPI data <2> (+)
15	0	-2871	MDN2	Output	MIPI data <2> (-)
16	220	-2871	PLLVSS	Ground	Ground for PLL
17	440	-2871	PLLVDD	Power	Internal reference voltage
18	660	-2871	INCLK	Input	Sensor input clock
19	880	-2871	DGND	Ground	Ground for digital
20	1100	-2871	DVDD12	POWER	Digital power supply pin: 1.15~1.3V.
21	1320	-2871	Test pin		NC
22	1540	-2871	Test pin		NC
23	1760	-2871	VDDIO	POWER	Power supply for I/O circuits: 1.7~3.0V.
24	1980	-2871	Test pin		NC
25	2200	-2871	Test pin		NC
26	2420	-2871	Test pin		NC
27	2640	-2871	Test pin		NC
28	2860	-2871	DGND	Ground	Ground for digital
29	3080	-2871	DVDD12	POWER	Digital power supply pin: 1.15~1.3V.
30	3080	2871	AVDD28	POWER	Main power supply pin: 2.7~3.0V.
31	2860	2871	AGND	Ground	Ground for analog
32	2640	2871	DVDD12	POWER	Digital power supply pin: 1.15~1.3V.
33	2420	2871	DGND	Ground	Ground for digital
34	2200	2871	VOTP	POWER	For OTP power supply
35	1980	2871	Test pin		NC
36	1760	2871	Test pin		NC
37	1540	2871	Test pin		NC

38	1320	2871	VDDIO	POWER	Power supply for I/O circuits: 1.7~3.0V.
39	1100	2871	Test pin		NC
40	880	2871	Test pin		NC
41	660	2871	Test pin		NC
42	440	2871	Test pin		NC
43	220	2871	Test pin		NC
44	0	2871	Test pin		NC
45	-220	2871	FSYNC	I/O	Frame sync control
46	-440	2871	SBDA	I/O	Two-wire serial bus, data
47	-660	2871	VDDIO	POWER	Power supply for I/O circuits: 1.7~3.0V.
48	-880	2871	SBCL	Input	Two-wire serial bus, clock
49	-1100	2871	PWDN	Input	Sensor power down control: (floating forbidden) 0: standby 1: normal work
50	-1320	2871	RESET	Input	Chip reset control: (floating forbidden) 0: chip reset 1: normal work
51	-1540	2871	IDSEL	Input	IDSEL (floating forbidden) ***0: 0x52/0x53 (default)*** 1: 0x20/0x21
52	-1760	2871	DGND	Ground	Ground for digital
53	-1980	2871	DVDD12	POWER	Digital power supply pin: 1.15~1.3V.
54	-2200	2871	AVDD28	POWER	Main power supply pin: 2.7~3.0V.
55	-2420	2871	AGND	Ground	Ground for analog
56	-2640	2871	VDCG	POWER	Internal power supply, please connect 1μF capacitor to analog ground.
57	-2860	2871	VREF	POWER	Internal power supply, please connect 1μF capacitor to analog ground.
58	-3080	2871	VTX	POWER	Internal power supply, please connect 1μF capacitor to analog ground.

6. Optical Specifications

6.1 Readout Position

The GC4C33 default status is readout from the lower left corner with pin 1 located in the low left corner. The image is inverted vertically and horizontally by the lens, so proper image output results when Pin 1 is located in the low left corner.

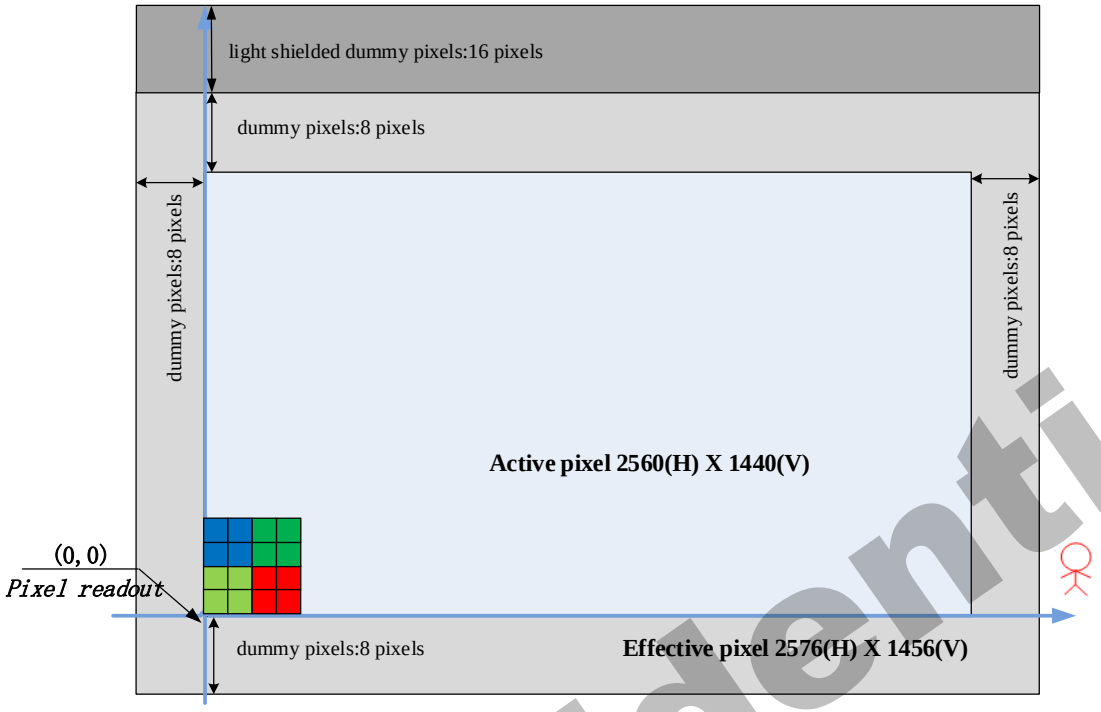


Readout direction can be set by the registers.

Function	Register Address	Register Value	First Pixel
Normal	0x0101[1:0]	00	Gr
Horizontal mirror	0x0101[1:0]	01	R
Vertical Flip	0x0101[1:0]	10	B
Horizontal Mirror and Vertical Flip	0x0101[1:0]	11	Gb

Horizontal Mirror Horizontal Mirror and Vertical Flip Vertical Flip

6.2 Pixel Array



Pixel array is covered by Bayer pattern color filters. The primary color GR/BG array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 2559. If flip in column, column is read out from 2559 to 0.

If no flip in row, row is read out from 0 to 1439. If flip in row, row is read out from 1439 to 0.

6.3 Lens Chief Ray Angle (CRA)

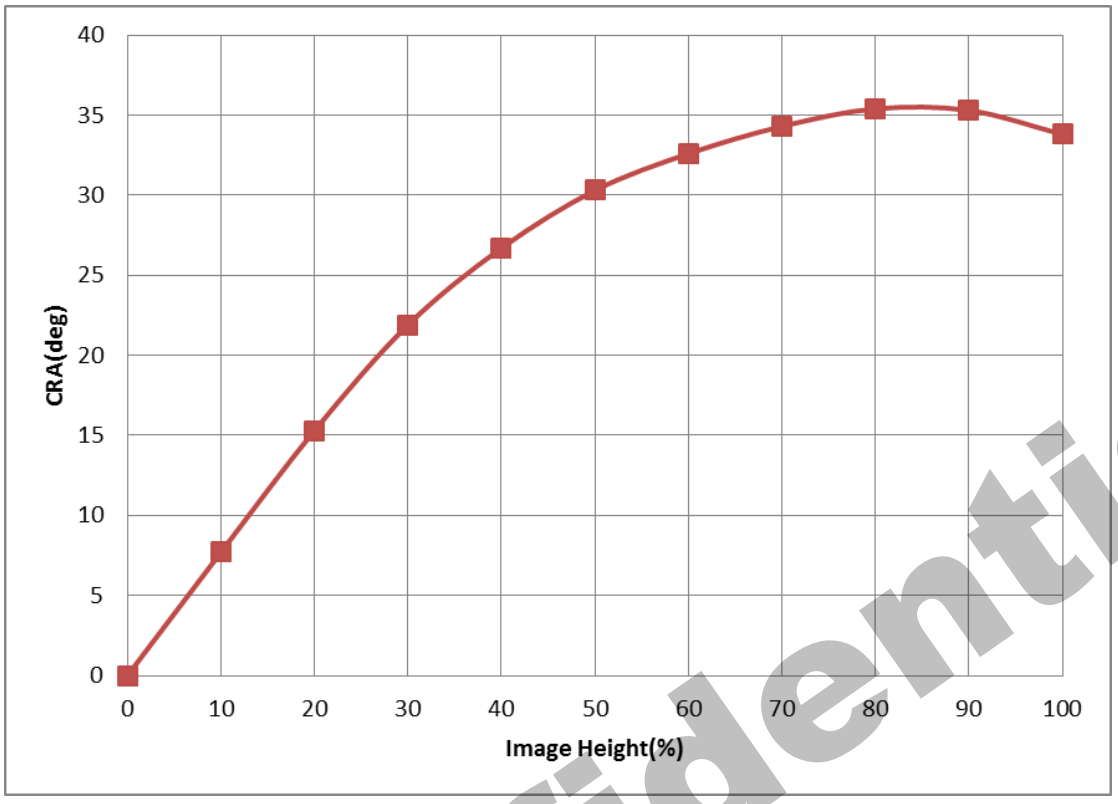
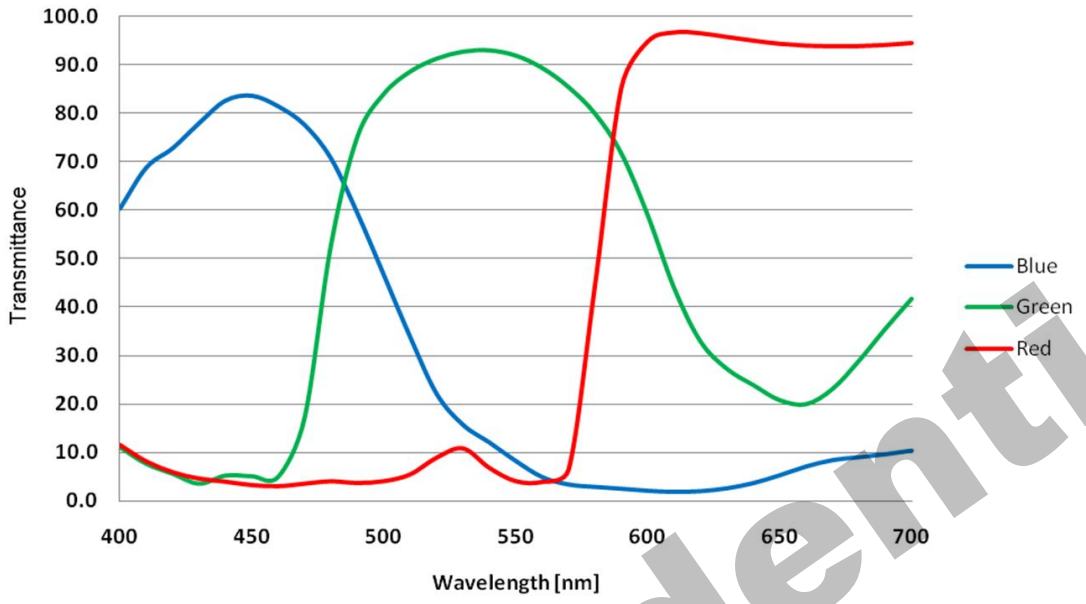


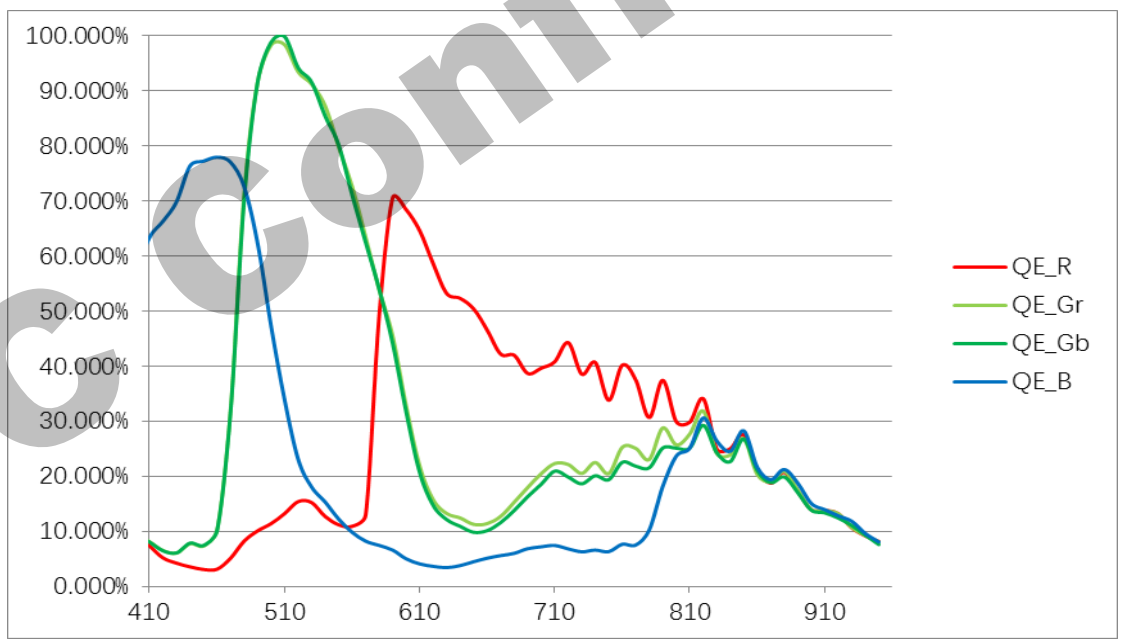
Image Height (%)	Image Height (mm)	CRA (degree)
00	0.000	0.00
10	0.329	7.70
20	0.658	15.30
30	0.987	21.90
40	1.316	26.70
50	1.645	30.30
60	1.974	32.60
70	2.303	34.30
80	2.632	35.40
90	2.961	35.30
100	3.290	33.80

6.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below:



6.5 QE Spectral Characteristic



7. Two-wire Serial Bus Communication

GC4C33 Device Address:

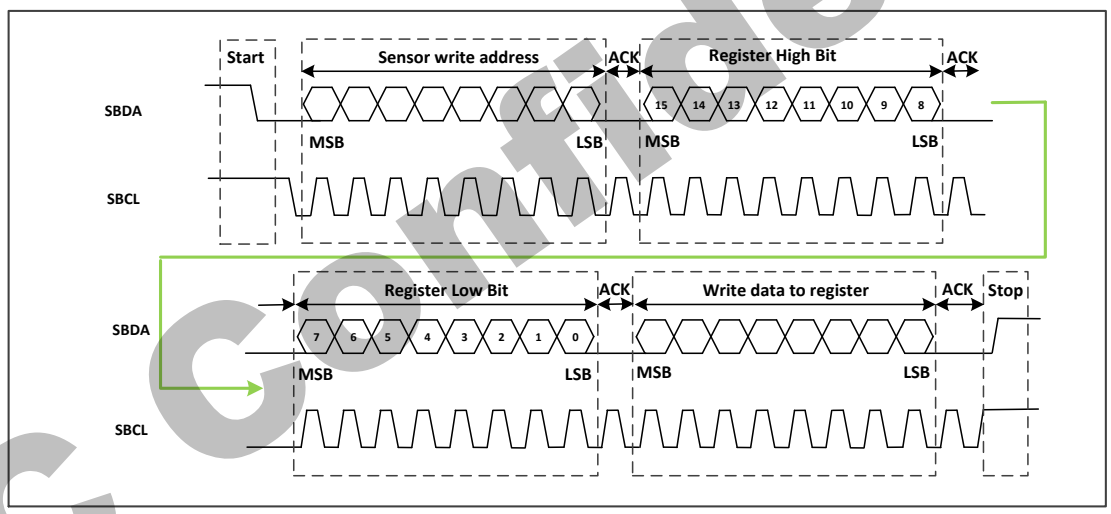
ID_SEL	Slave address write mode	Slave address read mode	Comment
0(default)	**0x52**	**0x53**	**Address 1**
1	**0x20**	**0x21**	**Address 2**

7.1 Protocol

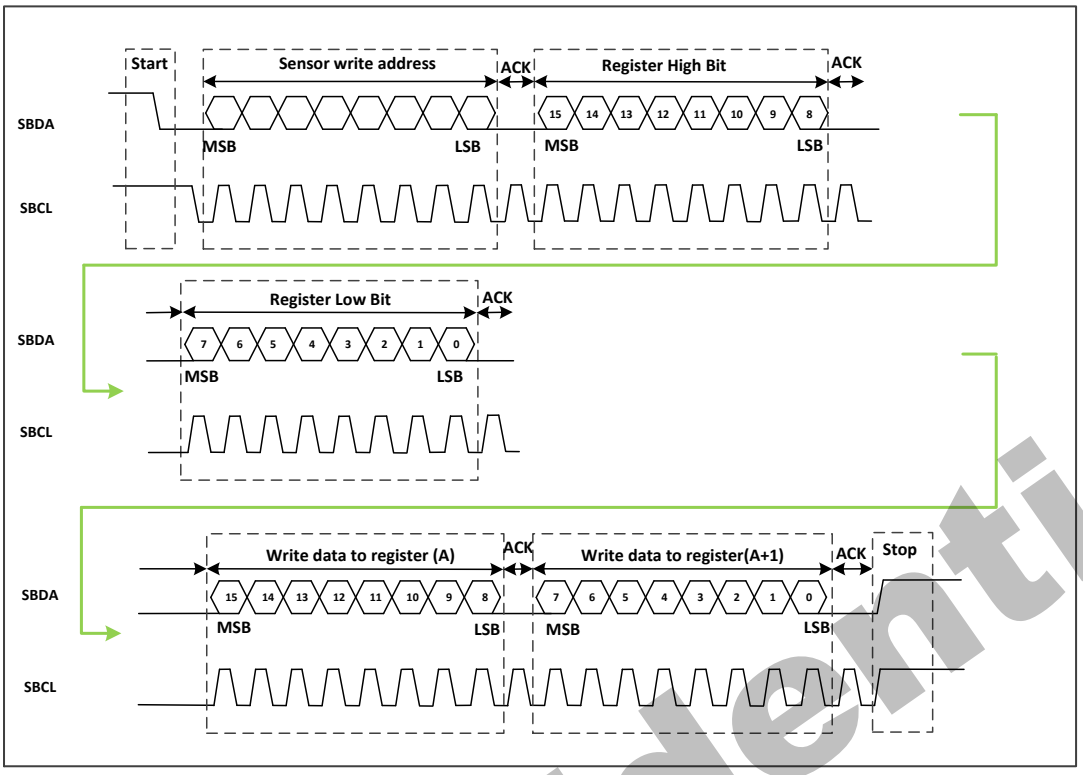
The host must perform the role of a communications master and GC4C33 acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL.**

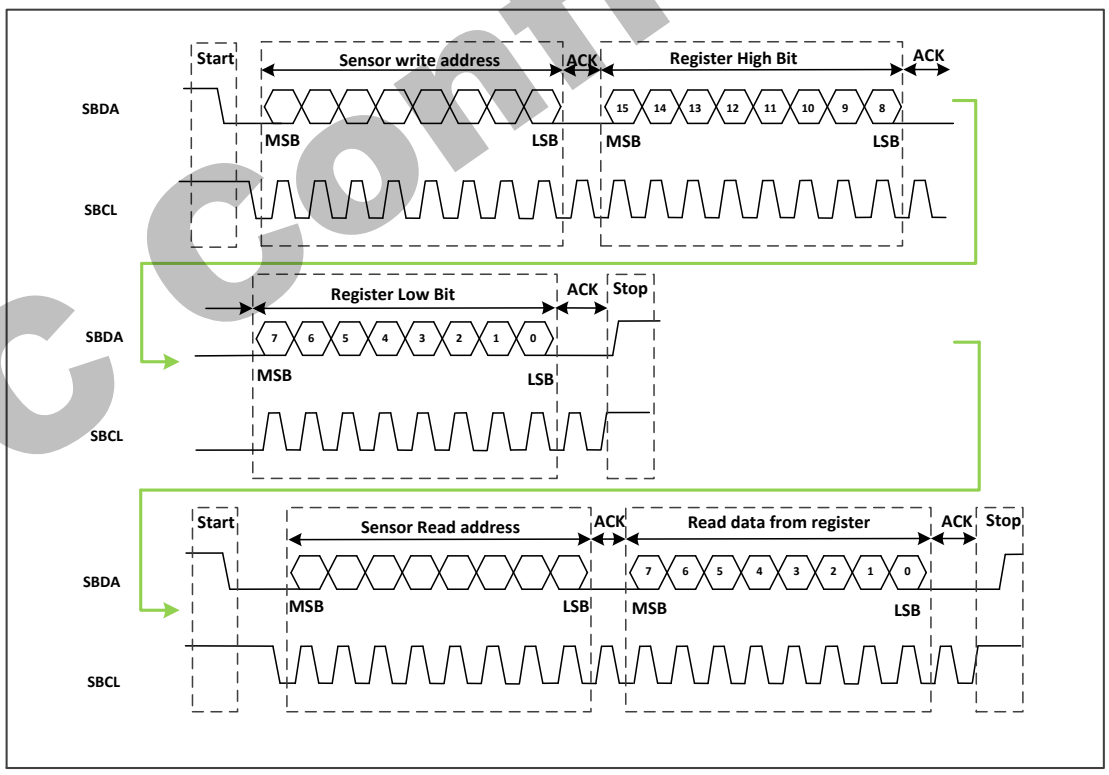
Write operate(2 bytes address –1byte data format):



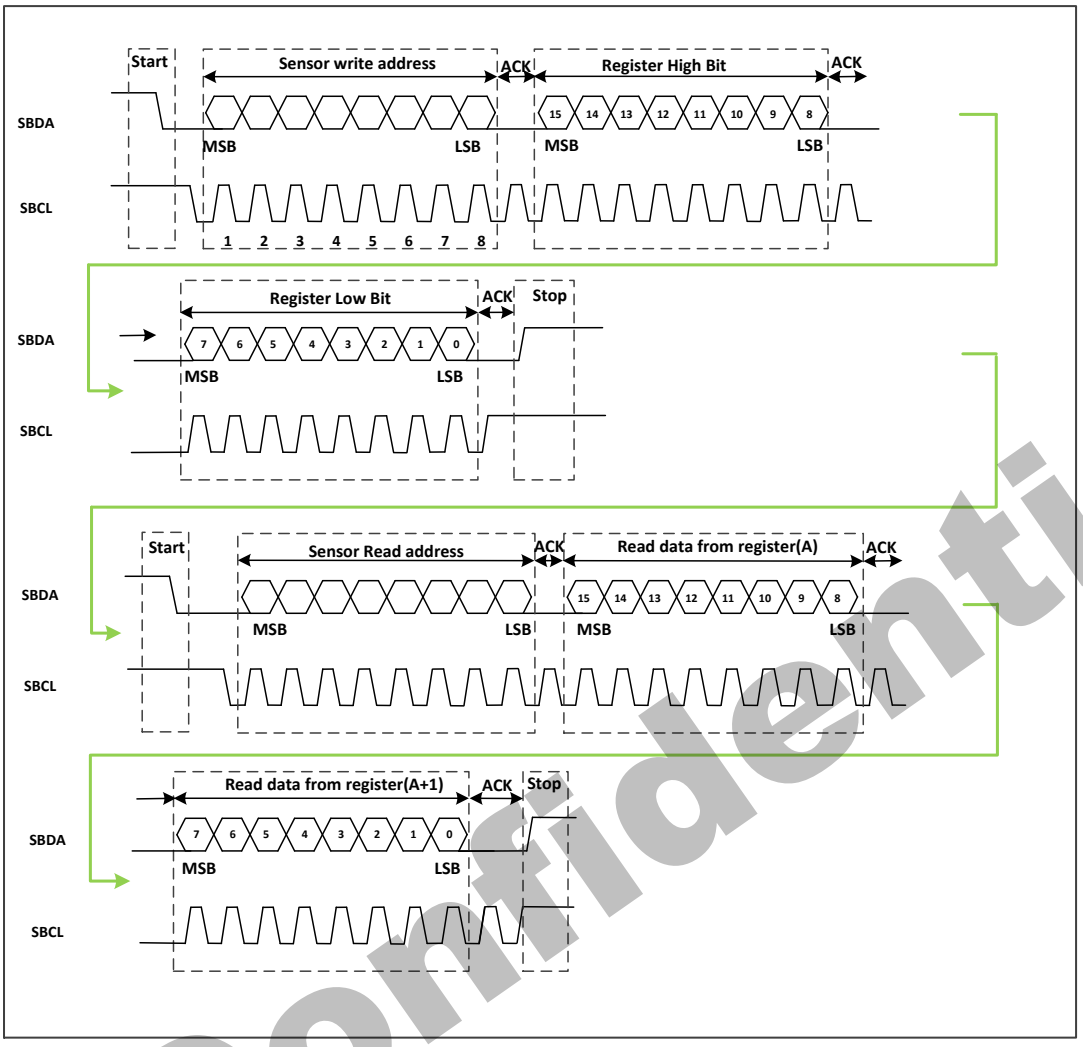
Write operate(2 bytes address –2byte data format)



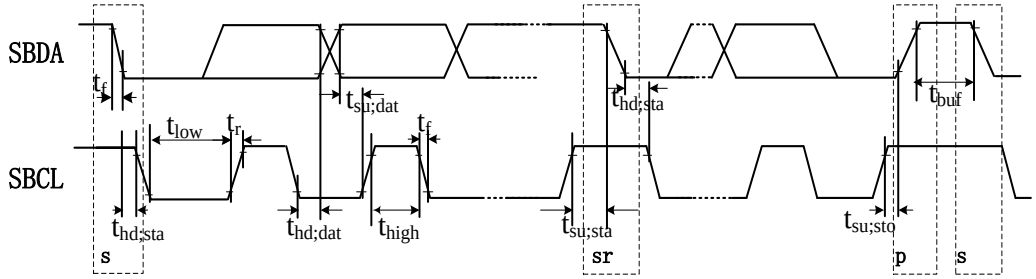
Read Operate(2 bytes address –1byte data format)：



Read Operate(2 bytes address –2byte data format)



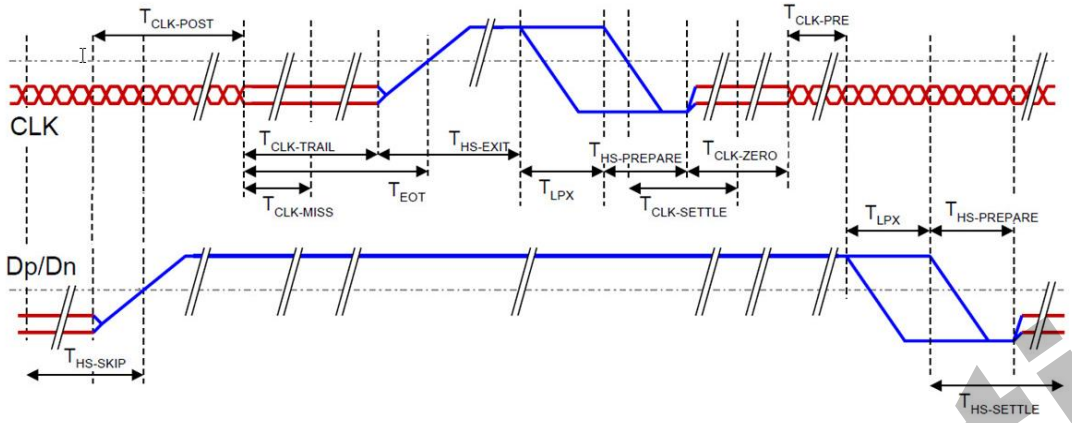
7.2 Serial Bus Timing



Parameter	Symbol	Min.	Typ.	Max.	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between a stop and a start	t_{buf}	1.3	--	--	µs
Hold time for a repeated start	$t_{hd;sta}$	0.6	--	--	µs
LOW period of SBCL	t_{low}	1.3	--	--	µs
HIGH period of SBCL	t_{high}	0.6	--	--	µs
Set-up time for a repeated start	$t_{su;sta}$	600	--	--	ns
Data hold time	$t_{hd;dat}$	0	--	900	ns
Data Set-up time	$t_{su;dat}$	100	--	--	ns
Rise time of SBCL, SBDA	t_r	--	--	300	ns
Fall time of SBCL, SBDA	t_f	--	--	300	ns
Set-up time for a stop	$t_{su;sto}$	0.6	--	--	µs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	--	pf

8. Applications

8.1 Clock lane low-power



Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).

$T_{CLK\_HS\_PREPARE}$: setting by Register 0x0122

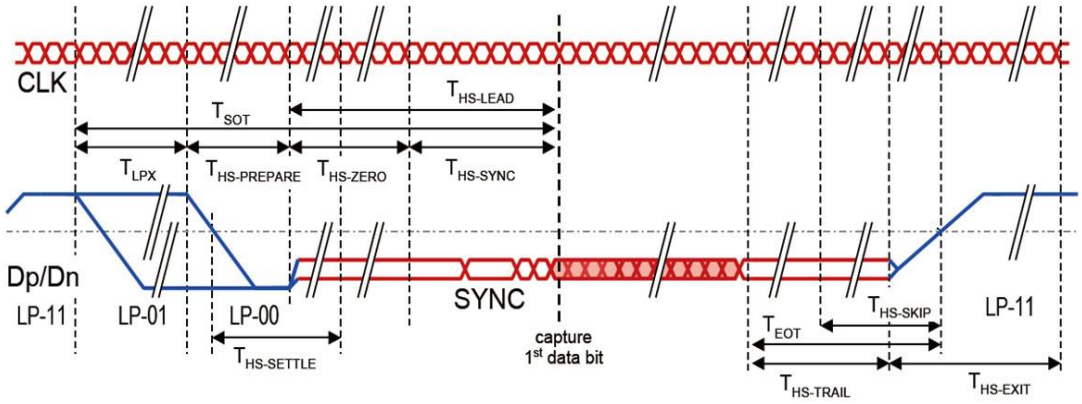
T_{CLK_ZERO}: setting by Register 0x0123

T_{CLK_PRE}: setting by Register 0x0124

T_{CLK_POST}: setting by Register 0x0125

T_{CLK_TRAIL}: setting by Register 0x0126

8.2 Data Burst



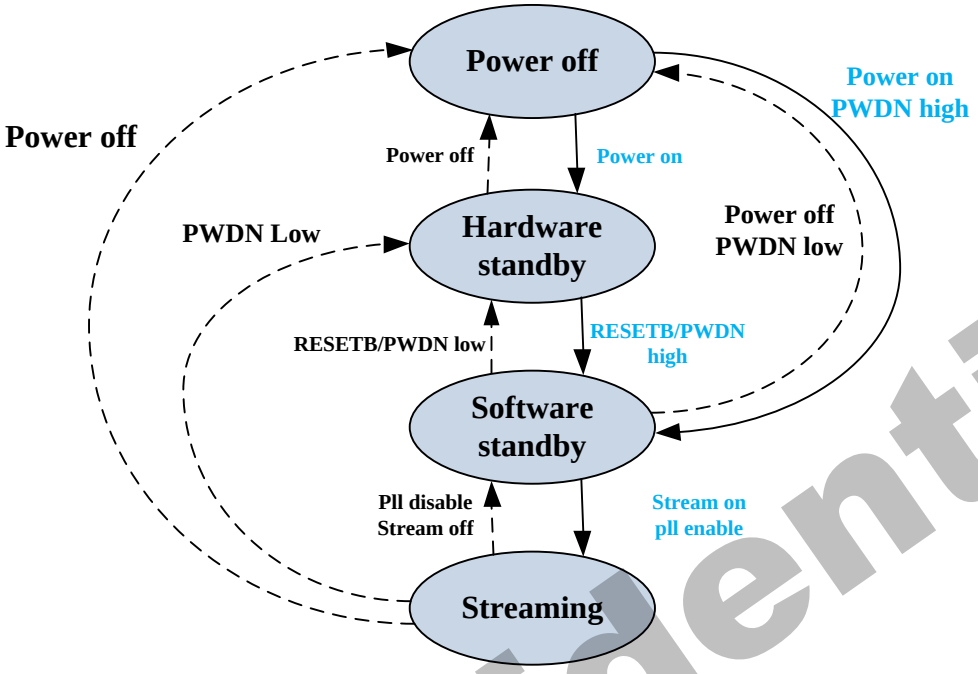
Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.

T_{LPX}:	setting by Register	0x0121
$T_{HS\_PREPARE}$:	setting by Register	0x0129
T_{HS_ZERO}:	setting by Register	0x012a
T_{HS_TRAIL}:	setting by Register	0x012b
T_{HS_EXIT}:	setting by Register	0x0127

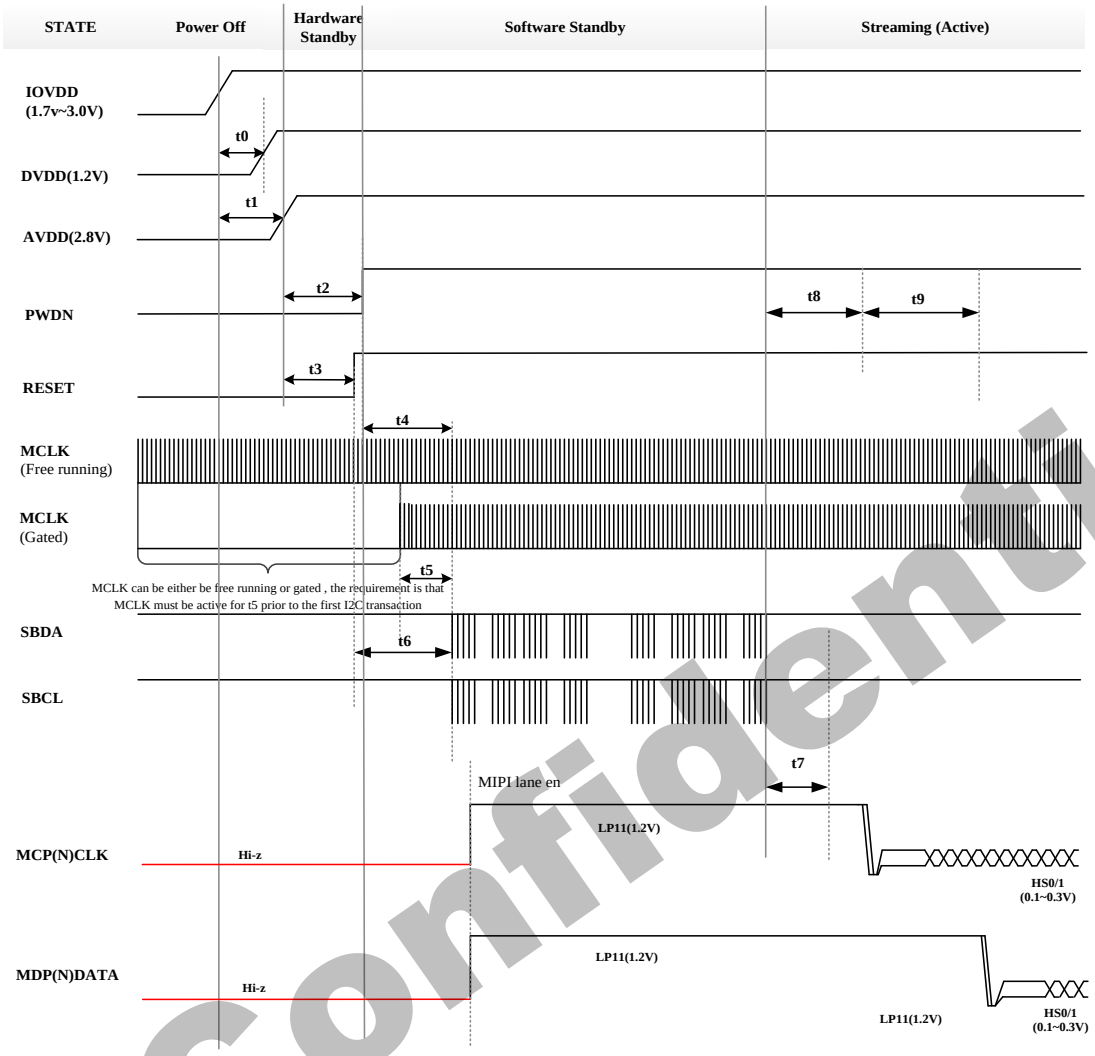
9. Function description

9.1 Operation mode



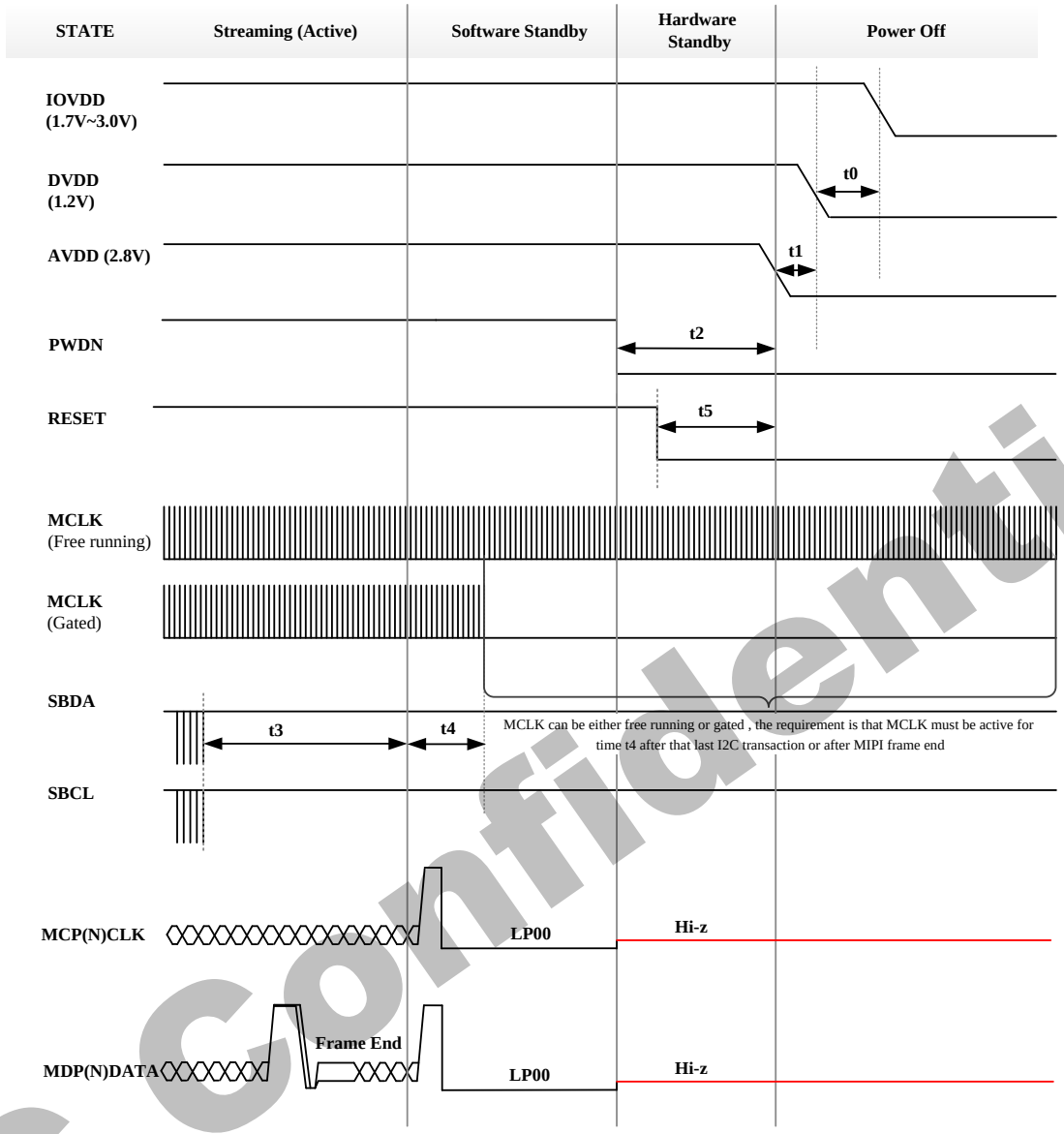
Power state	Description	Activate
Power off	Power supplies are turned off	None
Hardware standby	No communication with sensor, low level on PWDN and RESET, and stop MCLK	PWDN low
Software standby	Two- wire serial communication with sensor, pll is ready for fast return to streaming mode	Stream mode off PLL disable RESET high PWDN high
Streaming	Sensor is fully powered and is streaming image data on the MIPI CSI-2 bus	All

9.2 Power on Sequence



Parameter	Description	Min.	Max.	Unit
t0	From IOVDD to DVDD12	50	-	µs
t1	From IOVDD to AVDD28	50	-	µs
t2	From AVDD28 to PWDN pull high	0	-	µs
t3	From AVDD28 to RESET pull high	0	-	µs
t4	From PWDN to first I2C transaction	50	-	µs
t5	Minimum No. of MCLK cycles prior to the first I2C transaction	1200	-	MCLK
t6	From RESET to first I2C transaction	50	-	µs
t7	PLL start up/lock time	-	1	ms
t8	Entering streaming mode – First frame start sequence (fixed part)		10	ms
t9	Entering streaming mode – First frame start sequence (variable part)	-		lines

9.3 Power off Sequence



Parameter	Description	Min.	Max.	Unit
t0	From DVDD12 pull down to IOVDD pull down	0	-	µs
t1	From AVDD28 pull down to DVDD12 pull down	0	-	µs
t2	From PWDN pull low to AVDD pull down	0		µs
t3	Enter Software Standby CCI command – Device in Software Standby mode	0	-	µs
t4	Minimum number of MCLK cycles after the last CCI transaction or MIPI frame end code.	2000		MCLK
t5	From RESET pull low to AVDD pull down	0	-	µs

- Recommended power on/off sequence is above.
- If the sensor’s power cannot be cut off, please keep power supply, then set PWDN pin low. It will make sensor standby
- Register should be reloaded before works.
- If the standby sequence needs to be modified, please contact FAE of *Galaxycore Inc.*

9.4 Black level calibration

Black level is caused by pixel characteristics and analog channel offset, which makes poor image quality in dark condition and color balance, to reduce these, sensor automatically calibrates the black level every frame with light shield pixel array.

9.5 Integration time

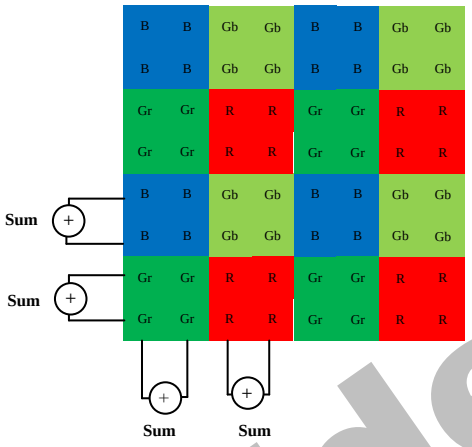
The integration time is controlled by the integration time registers

Addr.	Register name	Description
0x0202	Shutter time	[5:0] shutter time[13:8]
0x0203		[7:0] shutter time[7:0]
0x0340	Frame length	[5:0] frame length[13:8]
0x0341		[7:0] frame length[7:0]

9.6 Binning mode

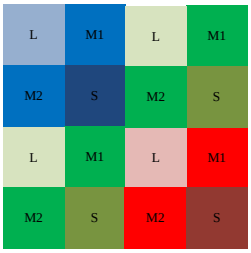
Binning read out mode can be used to obtain an image of lower resolution for full field of view, with lower output rate, and higher SNR.

The following diagram describe on 2x2 pixel binning operations, pixels of two adjacent rows and columns are read out as one pixel.



9.7 HDR mode

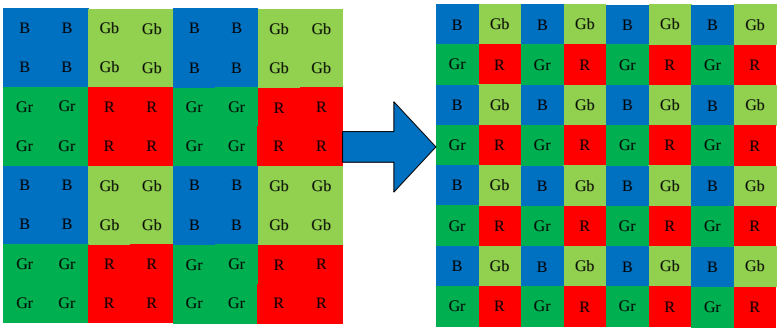
GC4C33 can support different exposure time in different pixel, sensor only can output full size picture and use HDR mode, but without HDR process.



Addr.	Register name	Description
0x0234	HDR mode	[2]HDR mode en
0x0200	Exposure M1	[5:0] Exposure M1 [13:8]
0x0201		[7:0] Exposure M1 [7:0]
0x0202	Exposure L	[5:0] Exposure L [13:8]
0x0203		[7:0] Exposure L [7:0]
0x026a	Exposure S	[5:0] Exposure S [13:8]
0x026b		[7:0] Exposure S [7:0]
0x026c	Exposure M2	[5:0] Exposure M2 [13:8]
0x026d		[7:0] Exposure M2 [7:0]

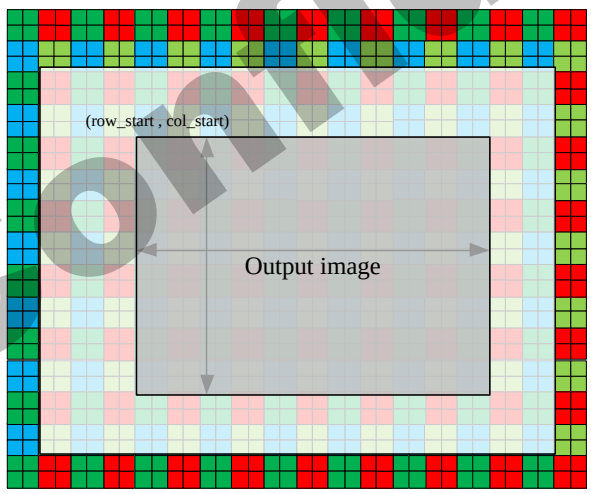
9.8 Hardware De-mosaic mode

GC4C33 can support de-mosaic mode which can change 4cell color pattern to bayer pattern.



9.9 Windowing

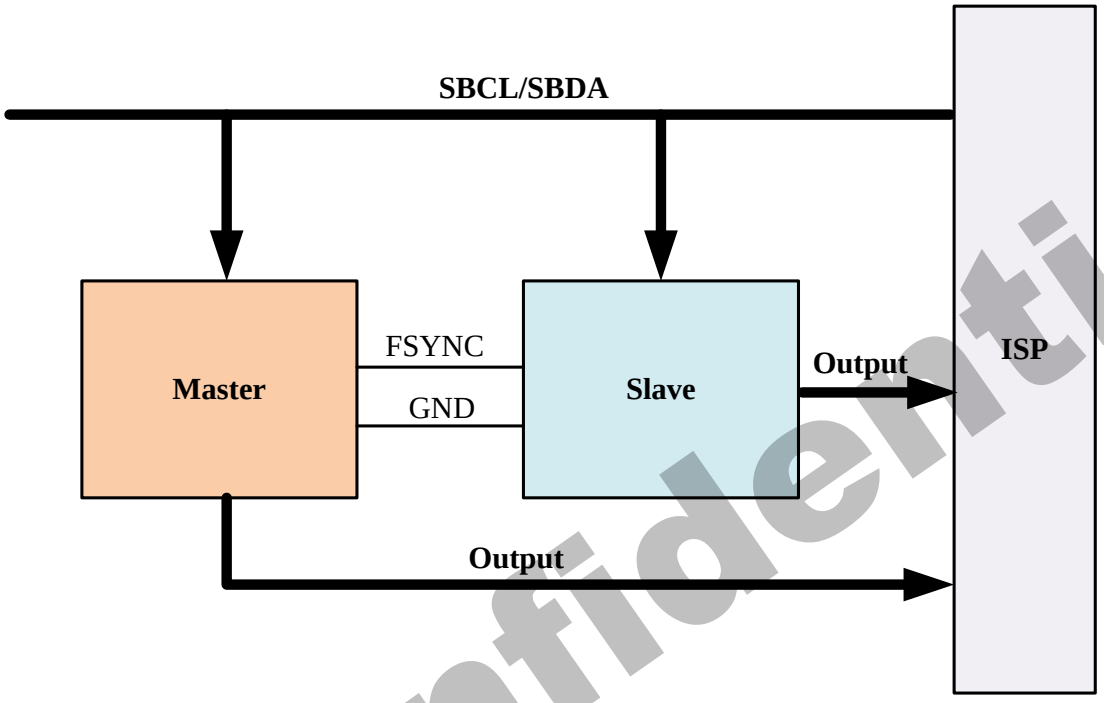
GC4C33 has a rectangular pixel array 2560 x 1440, it can be windowed by output size control, the output image windowing can be used to adjust output size, and it will affect field angle.



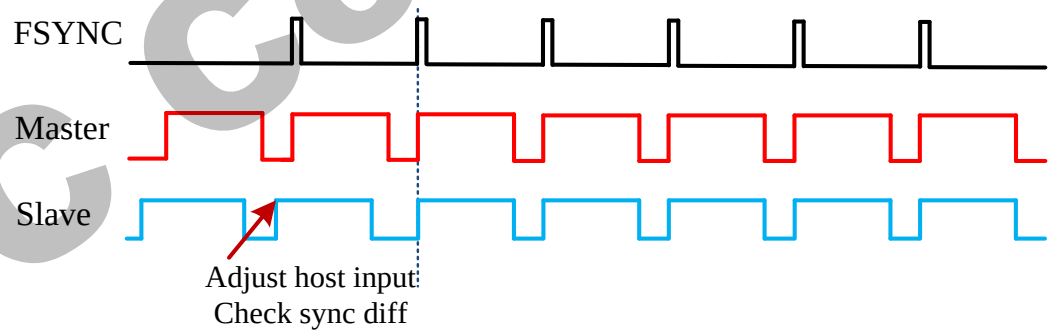
Addr.	Register name	Description
0x034a	win_height	[3:0]win_height[11:8]
0x034b		[7:0]win_height[7:0]
0x0348	win_width	[3:0]win_width[11:8]
0x0349		[7:0]win_width[7:0]
0x0346	Row start	[2:0]row_start[10:8]
0x0347		[7:0]row_start [7:0]
0x0344	Col start	[3:0]col_start[11:8]
0x0345		[7:0]col_start[7:0]

9.10 Frame sync mode

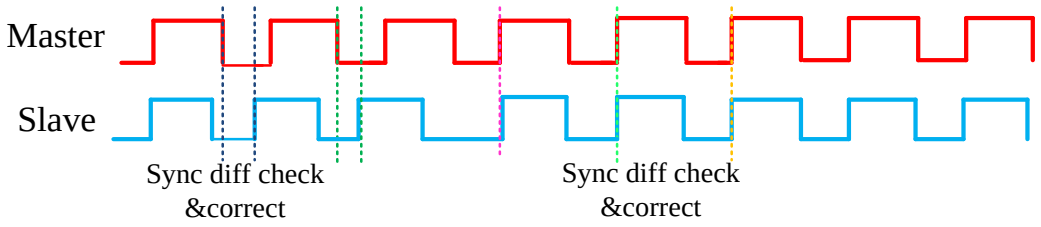
GC4C33 can support hardware frame sync for dual camera application. It can be set both master and slave sensor. When use this mode, the two sensor’s FSYNC pin must connect to each other.



Adjust mismatch sync



Dynamic mismatch sync control



Addr.	Register name	Description
0x027f	fsync_mode	[4]fsync_clear_counter [3]clock en [1]1 master or 0 slave [0]fsync_en
0x0282	fsync_mode_new2	[3] row count mode
0x0283	fsync_mode_new3	[7] gpio_value (gpio_mode on) or Fsync_diff_always_mode (gpio_mode off) [6:0] fsync out position
0x0284	Fsync row time	[7] position_FS_D [3] position_FS_A [2] position_FE_D [1] fsync_out_polarity [0] fsync_in_polarity
0x0285	fsync_mode_new4	[6] first vb clear [5] fsync_row_diff_mode
0x0286	fsync_row_diff_th	[5:0] fsync_row_diff_th
0x0287	Debug_mode4	[5:4] fsync_vb_gap
0x0288	fsync_row_diff_big[13:8]	[5:0] fsync_row_diff_big[13:8]
0x0289	fsync_row_diff_big [7:0]	[7:0] fsync_row_diff_big [7:0]
0x028a	fsync_row_diff_big2[13:8]	[5:0] fsync_row_diff_big2[13:8]
0x028b	fsync_row_diff_big2 [7:0]	[7:0] fsync_row_diff_big2[7:0]

9.11 OTP memory

GC4C33 sensor has 4K bits embedded OTP(One Time Programmable) memory, 30 bytes are for customers , which is for storing camera module calibration date.

9.12 Frame structure

Frame structure is controlled by HB, frame length, window start, window height, window width and VB.

Frame length control

Frame lengths are controlled by window height, minimum VB and shutter time.

- Minimum frame length = window height + 32 + minimum VB
- If shutter time < minimum frame length:

  Actual frame length = minimum frame length

- If shutter time > minimum frame length:

  Actual frame length = shutter time + 16 (recommended).

Addr.	Register name	Description
0x0340	Frame length	[7:0] frame length[15:8]
0x0341		[7:0] frame length[7:0]
0x029d	minimum VB	minimum VB

Line length control

Line length = 1020 (not recommended to be modified)

Addr.	Register name	Description	
0x0342	Line length	[3:0] Line length[11:8]	x2
0x0343		[7:0] Line length[7:0]	x2

Row_time calculate

Row_time = Line length/ PCLK

Line length –> Setting by register 0x0342 and 0x0343.

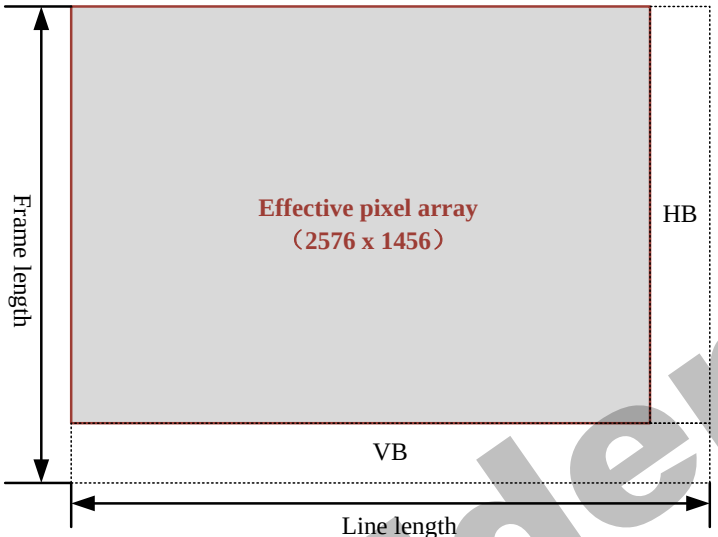
PCLK ->1/4 WPCLK.

Output window array control

Addr.	Register name	Description
0x0351	Out_window_y1	[2:0] Out_window_y1[10:8]
0x0352		[7:0] Out_window_y1[7:0]
0x0353	Out_window_x1	[3:0] Out_window_x1[11:8]
0x0354		[7:0] Out_window_x1[7:0]
0x034e	Out window height	[3:0] Out window height[11:8]
0x034f		[7:0] Out window height[7:0]
0x034c	Out window width	[3:0] Out window width[11:8]
0x034d		[7:0] Out window width[7:0]

Blank time control

1. line blank time is controlled by HB
2. frame blank time
   - frame blank time = frame length lines – window height – 32



10. Register List

System Register

Address	Name	Default Value	R/W	Description
0x03f0	**Sensor_ID_high**	**0x46**	**RO**	**Sensor_ID**
0x03f1	**Sensor_ID_low**	**0xC3**	**RO**	**Sensor_ID**
0x0312	Electirc_mode	0x00	RW	[7] watch_dog_mipi_en [6] watch_dog_cisctl_en [5] I2C_open_ena [4] pwd_dnb [3:0] I2C_esd_rst_mode
0x0314	Mclk_page_mode Rclk_sel_mode	0x70	RW	[6] mclk_page_mode [5:4] rclk_sel 00:mclk 01:serial clk 10:wpllclk 11:rpllclk [3:0] rclk_div
0x0315	Cp_clk_mode	0x00	RW	[5:4] cp clk sel 00:mclk 01:wpll 10:mppll 11:rpll [3:0] cp clk div
0x0316	Mpclk_sel_mode	0x10	RW	[5:4] mpclk_sel 00:mclk 01:reversed 10:wpllclk 11:rpllclk [3:0] mpclk_div
0x0317	Pll_mode1	0x25	RW	[5] bgap_en [4] bypass_clk_auto_switch [3] otpclk_en [2] freq div2 switch delay mode [1] reduce power mode [0] analog pwc
0x031a	clk_div_mode	0x00	RW	[7] freq_div2_enable [6] close_2_frame_freq [1] div2 [0] div1
0x031b	I2c_device_id	0x29	RW	[7:1] I2C device id: 29

0x031c	cm_mode	0x40	RW	[7] regf clk enable [6] mclk_enable [5] div2_mode [4] soc_2pclk_enable [3] div_clk_enable [2] serial clk enable [1] re_lock_pll [0] not_use_pll
0x031d	regf_buf_mode	0x00	RW	
0x031f	Soft reset	0x00	RW	[7] I2C_soft_rst_n [6] I2C_cm_rst_n [5] I2C_MIPI_rst_n [4] CISCTL_rst_n
0x0320	PLL_LDO_set	0x76	RW	[7:5] plldg_ldo_set [4] plldg_ldo_en [3:1] pllmp_ldo_set [0] pllmp_ldo_en
0x0321	PLL_PP_set	0x48	RW	[6:5] ppllclk_div [4:0] ppllclk_prediv
0x0324	PLL_DG_set1	0x10	RW	[7] div2en_sys [6] plldg_en [5] divdg_enb [4:0] rpllclk_div
0x0325	PLL_DG_set2	0x04	RW	[3:2] plldg_prediv [1:0] wpllclk_div
0x0326	PLL_DG_set3	0x50	RW	[7:0] plldg_div
0x0327	PLL_DG_set4	0x05	RW	[6] plldg_ref [5] refdg_enb [4] refdgdiv2d5_en [3] refdgdov1d5_en [2:0] refdg_div
0x0334	PLL_MP_set1	0x00	RW	[6] pllmp_en [5] divmp_enb [4:0] pllclkmp_prediv
0x0335	PLL_MP_set3	0x01	RW	[3:2] scaler_mode_tmp [1:0] pllmp_prediv
0x0336	PLL_MP_set2	0x4b	RW	[7:0] pllmp_div
0x0337	PLL_MP_set4	0x05	RW	[6] pllmp_ref [5] refmp_enb [4] refmpdiv2d5_en [3] refmpdiv1d5_en [2:0] refmp_div

Analog & CISCTL

Address	Name	Default Value	R/W	Description
0x0200	Exposure M1[13:8]	0x00	RW	Exposure M1[13:]
0x0201	Exposure M1[7:0]	0x04	RW	
0x0202	Exposure L[13:8]	0x00	RW	Exposure L[13:0]
0x0203	Exposure L[7:0]	0x10	RW	
0x0207	CISCTL_vb [13:8]	0x00	RW	CISCTL_vb[13:8] Vertical blanking
0x0208	CISCTL_vb [7:0]	0x40	RW	
0x020e	Auto_pregain[9:6]	--	RO	Auto_pregain[9:0]
0x020f	Auto_pregain[5:0]	--	RO	
0x033e	Line_length[7:0]	0x94	RW	Line_length
0x033f	Line_length[15:8]	0x05	RW	
0x0340	Buf_frame_length_h Framelength[13:8]	0x07	RW	[5:0] Buf_frame_length_h Framelength[13:8] RO
0x0341	Buf_frame_length_l Framelength[7:0]	0x0d	RW	[7:0] Buf_frame_length_l Framelength[7:0] RO
0x0342	CISCTL_hb[11:8]	0x02	RW	HB Linelength base on wqpclk
0x0343	CISCTL_hb[7:0]	0xca	RW	
0x0344	Buf_CISCTL_capt_col_start[11:8]	0x00	RW	CISCTL_col_start
0x0345	Buf_CISCTL_capt_col_start[7:0]	0x00	RW	
0x0346	row_start[10:8]	0x00	RW	CISCTL_row_start
0x0347	row_start[7:0]	0x02	RW	
0x0348	win_width[11:8]	0x0a	RW	CISCTL_win_width
0x0349	win_width[7:0]	0x10	RW	
0x034a	win_height[11:8]	0x05	RW	CISCTL_win_height
0x034b	win_height[7:0]	0xc0	RW	
0x034c	out_win_width[11:8]	0x0a	RW	out_win_width
0x034d	out_win_width[7:0]	0x00	RW	
0x034e	out_win_height[11:8]	0x05	RW	out_win_height
0x034f	out_win_height[7:0]	0xa0	RW	
0x0350	Win_mode	0x01	RW	
0x0351	out_win_y1[10:8]	0x00	RW	out_win_y1
0x0352	out_win_y1[7:0]	0x00	RW	
0x0353	out_win_x1[11:8]	0x00	RW	out_win_x1
0x0354	out_win_x1[7:0]	0x00	RW	

CSI/PHY1.5

Address	Name	Default Value	R/W	Description
0x0100		0x00	RW	[3] Lane_ena [2] ULP_ena [1] line_sync_mode [0] mipi_ena
0x0101	Image_Orientation	0x00	RW	[1] updown [0] mirror
0x0103	fifo_prog_full_level1[9:8] fifo_prog_full_level2[9:8]	0x00	RW	[3:2] fifo_prog_full_level1[9:8] [1:0] fifo_prog_full_level2[9:8]
0x0104	fifo_prog_full_level1[7:0]	0x10	RW	[7:0] fifo_prog_full_level1
0x0105	fifo_prog_full_level2[7:0]	0x10	RW	[7:0] fifo_prog_full_level2
0x0106	FIFO_mode	0x38	RW	[7] sram_test_mode [6] fifo_rst_mode [5] fifo1_cs_en [4] fifo2_cs_en [3] SPI_gate_SRAM [2] fifo1_clk_gate_mode [1] fifo2_wr_gate_mode [0] fifo2_rd_gate_mode
0x0107	CSI2_mode2	0x09	RW	[7] virtual channel en [6] mipi input test data en [5] mipi write gate en [4] mipi hb ctl en [3:2] vc3_id [1:0] vc2_id
0x0108	CSI2_mode3	0x04	RW	[3] CSO2_mode_updata_mode [2] mipi_set_auto_en [1:0] switch mode
0x010d	LWC_set[7:0]	0x80	RW	
0x010e	LWC_set[15:8]	0x0c	RW	Raw10：2560x5/4 must be 2x
0x010f	SYNC_set	0xb8	RW	SYNC_set
0x0110	LDI_set_dummy	0x32	RW	Used for first dummy line 0x31 –raw8 0x32 –raw10 0x33 –raw12

0x0111	LP_set	0x2b	RW	RAW10
0x0112	Mipi_raw_mode[15:8]	0x0a	RW	0x0808 RAW8 0x0a0a RAW10 0x0a08 COMP10_8
0x0113	Mipi_raw_mode[7:0]	0x0a	RW	
0x0114	Mipi_lane_num	0x03	RW	00:1lane 01:2lane 10:3lane 11:4lane
0x0115	DPHY_mode	0x10	RW	[7] mipi para invar when div2 [6] DATA lane gate [5] all_lane_open_mode [4:2] switch_msb_mode [1:0] clklane_mode
0x0116	LP_set	0x29	RW	[7:6] hi-z [5:4] use define [3:2] 1 [1:0] 0
0x011b	fifo2_prog_full_level	0x0c	RW	[5:0] fifo2_prog_full_level
0x011c	fifo2_push_prog_full_level	0x10	RW	[5:0] fifo2_push_prog_full_level
0x011d	Sram_test_mode	0x02	RW	[6] raw14 compress [5] compress_predict_out_mode [4] compress_mode [3] cen [2] RF1 gata [1] RF1 gate [0]sram test
0x011f		--	RO	[3] fifo 1_error_valid [2] fifo 1_full_valid [1] fifo_pop_error_valid [0] fifo_push_error_valid
0x0120	T_init_set	0x80	RW	more than 100 us
0x0121	T_LPX_set	0x10	RW	more than 50ns
0x0122	T_CLK_HS_PREPARE_set	0x05	RW	38ns ~95ns LP00
0x0123	T_CLK_zero_set	0x20	RW	more than 300ns
0x0124	T_CLK_PRE_set	0x02	RW	more than 8UI
0x0125	T_CLK_POST_set	0x20	RW	60ns +52UI
0x0126	T_CLK_TRAIL_set	0x08	RW	60ns
0x0127	T_HS_exit_set	0x10	RW	more than 100ns
0x0128	T_wakeup_set	0xa0	RW	1 ms

0x0129	T_HS_PREPARE_set	0x06	RW	45+4UI ~85+5UI
0x012a	T_HS_Zero_set	0x0a	RW	140ns
0x012b	T_HS_TRAIL_set	0x08	RW	60ns
0x012d	mp_reserve	0x00	RW	60ns
0x0130	MIPI_Test	0x00	RW	[2] line_sync_mode_patch [1] mipi_test_clk_mode [0] mipi_test
0x0136	Initial period	0x00	RW	[1] initial_en [0] period_en
0x0137	Initial_time[7:0]	0xff	RW	initial_time
0x0138	Initial_time[15:8]	0x0f	RW	
0x0139	Period_time	0x7f	RW	
0x013a	Period_start_time	0xfe	RW	can not be 8'hff
0x013b	prbs_mode	0x20	RW	[6] prbs11 [5] prbs_9 [4] clane prbs en [3] dlane3 prbs en [2] dlane2 prbs en [1] dlane1 prbs en [0] dlane0 prbs en
0x013c	prbs_seed[7:0]	0x9a	RW	prbs_seed[7:0]
0x013d	prbs_seed[15:8]	0x78	RW	prbs_seed[15:8]
0x013e	prbs_LDI	0x3d	RW	
0x0140	para_buf_mode[7:0]	0x60	RW	[11] auto set para output buf width
0x0141	para_buf_mode[11:8]	0x08	RW	[10] start mode2 [9] start_mode [8] output buf enable [7:4] buf win end [3] pclk buf gate [2] hsync polarity [1:0] delay half mode
0x0142	para_buf_win_width[7:0]	0x80	RW	para_buf_win_width[7:0]
0x0143	para_buf_win_width[11:8] para_buf_win_height[11:8]	0x74	RW	[7:4] para_buf_win_width[11:8] [3:0] para_buf_win_height[11:8]
0x0144	para_buf_win_height[7:0]	0x38	RW	para_buf_win_height[7:0]
0x0145	para_buf_total_width[7:0]	0x98	RW	para_buf_total_width
0x0146	para_buf_total_width[	0x84	RW	[7:4] para_buf_total_width[11:8]

	11:8] para_buf_total_height[11:8]			[3:0] para_buf_total_height[11:8]
0x0147	para_buf_total_height[7:0]	0x65	RW	para_buf_total_height[7:0]
0x014c	MIPI_TSEL	0x01	RW	
0x0180	DPHY_analog_mode1	0x06	RW	[6] mipi_en [5:4] disable_set [3:0] mipi_diff
0x0181	DPHY_analog_mode2	0x00	RW	[7] dphy_data3_en [6] dphy_data2_en [5] dphy_data1_en [4] dphy_data0_en [3] data3delay1s [2] data2delay1s [1] data1delay1s [0] data0delay1s
0x0182	DPHY_analog_mode3	0x00	RW	[7:6] data3lp_drv_10 [5:4] data2lp_drv_10 [3:2] data1lp_drv_10 [1:0] data0lp_drv_10
0x0183	DPHY_analog_mode4	0x55	RW	[7:6] data3ctr [5:4] data2ctr [3:2] data1ctr [1:0] data0ctr
0x0184	DPHY_analog_mode5	0xaa	RW	[7:6] dat3hs_ph [5:4] dat2hs_ph [3:2] dat1hs_ph [1:0] dat0hs_ph
0x0185	DPHY_analog_mode6	0x00	RW	[7] data3lp_drv_2 [6] data2lp_drv_2 [5] data1lp_drv_2 [4] data0lp_drv_2 [3] clkip_drv_2 [2:1] NA [0] dphy_clk_en
0x0186	DPHY_analog_mode7	0x63	RW	[7:6] clkctr [5:4] clkhs_ph [3:2] clklp_drv_10 [1] clklane_p2s_sel NA clkp2s_en [0] clkdelay1s

BLK

Address	Name	Default Value	R/W	Description
0x0040	BLK_mode1	0x23	RW	[1] dark_current_en [0] offset_en
0x0049	BLK_select_row_bits_L	0x3c	RW	[7:0] BLK_select_row_bits[7:0]
0x004a	BLK_select_row_bits_H	0x3c	RW	[7:0] BLK_select_row_bits[15:8]
0x004c	BLK_blooming_row_select_L	0x03	RW	[7:0] BLK_blooming_row_select[7:0]
0x004d	BLK_blooming_row_select_H	0x00	RW	[7:0] BLK_blooming_row_select[15:8]
0x0400	Sdark_offset_G1_L	0x00	RW	[7:0] Sdark_offset_G1[7:0]
0x0401	Sdark_offset_R_L	0x00	RW	[7:0] Sdark_offset_R[7:0]
0x0402	Sdark_offset_B_L	0x00	RW	[7:0] Sdark_offset_B[7:0]
0x0403	Sdark_offset_G2_L	0x00	RW	[7:0] Sdark_offset_G2[7:0]
0x0404	Sdark_offset_G1_M	0x00	RW	[7:0] Sdark_offset_G1[15:8]
0x0405	Sdark_offset_R_M	0x00	RW	[7:0] Sdark_offset_R[15:8]
0x0406	Sdark_offset_B_M	0x00	RW	[7:0] Sdark_offset_B[15:8]
0x0407	Sdark_offset_G2_M	0x00	RW	[7:0] Sdark_offset_G2[15:8]
0x0408	Sdark_offset_G1_H	0x00	RW	[7:0] Sdark_offset_G1[19:16]
0x0409	Sdark_offset_R_H	0x00	RW	[3:0] Sdark_offset_R[19:16]
0x040a	Sdark_offset_B_H	0x00	RW	[3:0] Sdark_offset_B[19:16]
0x040b	Sdark_offset_G2_H	0x00	RW	[3:0] Sdark_offset_G2[19:16]
0x040c	Ndark_offset_G1_L	0x00	RW	[7:0] Ndark_offset_G1[7:0]
0x040d	Ndark_offset_R_L	0x00	RW	[7:0] Ndark_offset_R[7:0]
0x040e	Ndark_offset_B_L	0x00	RW	[7:0] Ndark_offset_B[7:0]
0x040f	Ndark_offset_G2_L	0x00	RW	[7:0] Ndark_offset_G2[7:0]
0x0410	Ndark_offset_G1_M	0x00	RW	[7:0] Ndark_offset_G1[15:8]
0x0411	Ndark_offset_R_M	0x00	RW	[7:0] Ndark_offset_R[15:8]
0x0412	Ndark_offset_B_M	0x00	RW	[7:0] Ndark_offset_B[15:8]
0x0413	Ndark_offset_G2_M	0x00	RW	[7:0] Ndark_offset_G2[15:8]
0x0414	Ndark_offset_G1_H	0x00	RW	[7:0] Ndark_offset_G1[19:16]
0x0415	Ndark_offset_R_H	0x00	RW	[3:0] Ndark_offset_R[19:16]
0x0416	Ndark_offset_B_H	0x00	RW	[3:0] Ndark_offset_B[19:16]
0x0417	Ndark_offset_G2_H	0x00	RW	[3:0] Ndark_offset_G2[19:16]
0x0418	Sdark_offset_T2_G1_L	0x00	RW	[7:0] Sdark_offset_T2_G1[7:0]
0x0419	Sdark_offset_T2_R_L	0x00	RW	[7:0] Sdark_offset_T2_R[7:0]
0x041a	Sdark_offset_T2_B_L	0x00	RW	[7:0] Sdark_offset_T2_B[7:0]

0x041b	Sdark_offset_T2_G2_L	0x00	RW	[7:0] Sdark_offset_T2_G2[7:0]
0x041c	Sdark_offset_T2_G1_M	0x00	RW	[7:0] Sdark_offset_T2_G1[15:8]
0x041d	Sdark_offset_T2_R_M	0x00	RW	[7:0] Sdark_offset_T2_R[15:8]
0x041e	Sdark_offset_T2_B_M	0x00	RW	[7:0] Sdark_offset_T2_B[15:8]
0x041f	Sdark_offset_T2_G2_M	0x00	RW	[7:0] Sdark_offset_T2_G2[15:8]
0x0420	Sdark_offset_T2_G1_H	0x00	RW	[7:0] Sdark_offset_T2_G1[19:16]
0x0421	Sdark_offset_T2_R_H	0x00	RW	[3:0] Sdark_offset_T2_R[19:16]
0x0422	Sdark_offset_T2_B_H	0x00	RW	[3:0] Sdark_offset_T2_B[19:16]
0x0423	Sdark_offset_T2_G2_H	0x00	RW	[3:0] Sdark_offset_T2_G2[19:16]
0x0424	Ndark_offset_T2_G1_L	0x00	RW	[7:0] Ndark_offset_T2_G1[7:0]
0x0425	Ndark_offset_T2_R_L	0x00	RW	[7:0] Ndark_offset_T2_R[7:0]
0x0426	Ndark_offset_T2_B_L	0x00	RW	[7:0] Ndark_offset_T2_B[7:0]
0x0427	Ndark_offset_T2_G2_L	0x00	RW	[7:0] Ndark_offset_T2_G2[7:0]
0x0428	Ndark_offset_T2_G1_M	0x00	RW	[7:0] Ndark_offset_T2_G1[15:8]
0x0429	Ndark_offset_T2_R_M	0x00	RW	[7:0] Ndark_offset_T2_R[15:8]
0x042a	Ndark_offset_T2_B_M	0x00	RW	[7:0] Ndark_offset_T2_B[15:8]
0x042b	Ndark_offset_T2_G2_M	0x00	RW	[7:0] Ndark_offset_T2_G2[15:8]
0x042c	Ndark_offset_T2_G1_H	0x00	RW	[7:0] Ndark_offset_T2_G1[19:16]
0x042d	Ndark_offset_T2_R_H	0x00	RW	[3:0] Ndark_offset_T2_R[19:16]
0x042e	Ndark_offset_T2_B_H	0x00	RW	[3:0] Ndark_offset_T2_B[19:16]
0x042f	Ndark_offset_T2_G2_H	0x00	RW	[3:0] Ndark_offset_T2_G2[19:16]
0x0448	sdark_ratio_G1	0x00	RW	[7:0] sdark_ratio_G1[7:0]
0x0449	sdark_ratio_R	0x00	RW	[7:0] sdark_ratio_R[7:0]
0x044a	sdark_ratio_B	0x00	RW	[7:0] sdark_ratio_B[7:0]
0x044b	sdark_ratio_G2	0x00	RW	[7:0] sdark_ratio_G2[7:0]
0x044c	ndark_ratio_G1	0x80	RW	[7:0] ndark_ratio_G1[7:0]
0x044d	ndark_ratio_R	0x80	RW	[7:0] ndark_ratio_R[7:0]
0x044e	ndark_ratio_B	0x80	RW	[7:0] ndark_ratio_B[7:0]

0x044f	ndark_ratio_G2	0x80	RW	[7:0] ndark_ratio_G2[7:0]
0x0450	channel_gain_G1_L	0x00	RW	[7:0] channel_gain_G1[7:0]
0x0451	channel_gain_R_L	0x00	RW	[7:0] channel_gain_R[7:0]
0x0452	channel_gain_B_L	0x00	RW	[7:0] channel_gain_B[7:0]
0x0453	channel_gain_G2_L	0x00	RW	[7:0] channel_gain_G2[7:0]
0x0454	channel_gain_G1_H	0x00	RW	[2:0] channel_gain_G1[10:8]
0x0455	channel_gain_R_H	0x00	RW	[2:0] channel_gain_R[10:8]
0x0456	channel_gain_B_H	0x00	RW	[2:0] channel_gain_B[10:8]
0x0457	channel_gain_G2_H	0x00	RW	[2:0] channel_gain_G2[10:8]
0x0060	WB_offset	0x40	RW	[7:0] Wb_offset[7:0]

FSYNC

Address	Name	Default Value	R/W	Description
0x027f	fsync_clear_counter fsync_mode	0x08	RW	[7] master clear counter [6] master updata flop [5] master clear counter stop [4] fsync_clear_counter [3] clock en [2] slave ready for receive [1] 1 master or 0 slave [0] en
0x0280	fsync_mode_global	0x80	RW	[7] fsync_vb_gap_lasts [6] strobe_output [5] fsync_out_polarity [4] fsync_in_polarity [3] gpio_mode [2] gpio_value [1] vsync_out_mode [0] fsync_every_frame_slave
0x0281	fsync_mode_new	0x13	RW	[7:2] fsync_time x4+3 [1:0] fsync_mode_new 2'b11:old mode 2'b10:clear_start 2'b01:clear_stop 2'b00:update_flop
0x0282	fsync_mode_new2	0x00	RW	[7] exp_change_retime [6:0] fsync_mode_new2 [5] co-work with old [4] 0: disable aec delay mode using fsync

				[3] row count mode [2] delay to row gap [1] every frame slave en [0] every frame master en
0x0283	fsync_mode_new3	0x04	RW	[7] fsync_row_force [6:0] fsync out position
0x0284	fsync_rowtime	0x00	RW	[7] position_FS_D [6] fsync_row_pos [5] sel_endrow_cnts [4] adj_1X [3] position_FS_A [2] position_FE_D
0x0285	fsync_mode_new4	0x01	RW	[7] fsync_vb_gap_mode_tmp [6] fsync_vb_first_mode_tmp [5] fsync_row_diff_mode [4] fsync_vb_mode [3:2] fsync_vb_gap [1:0] fsync_vb_old
0x0286	fsync_row_diff_th	0x02	RW	[7] fsync_vb_diff_rnd [6] fsync_exp_change_mode [5:0] fsync_row_diff_th
0x0287	debug_mode4	0x58	RW	[7] CISCTL_exp_updata_mode [6] AEC_delay_mode [5] mode_switch close one more frame [4] txlow_r change close one more frame [3:0] fsync_vb_lowbits_disable
0x0288	fsync_row_diff_big_H	0x00	RW	[5:0] fsync_row_diff_big[13:8]
0x0289	fsync_row_diff_big_L	0x04	RW	[7:0] fsync_row_diff_big[7:0]
0x028a	fsync_row_diff_big2_H	0x00	RW	[5:0] fsync_row_diff_big2[13:8]
0x028b	fsync_row_diff_big2_L	0x10	RW	[7:0] fsync_row_diff_big2[7:0]
0x028c	ramp_t1_ref	0x12	RW	whclk
0x028d	debug_mode2	0x92	RW	[6] exp2_base_on_exp1 [5] exp2_eq_exp1_8 [4] exp_change_close_frame [3] exp2_eq_exp1_16 [1] vb_depend_FL