RV1126_RV1109 Reference Design

RV1126_RV1109_IPC_REF_V1.0

RV1126_RV1109 Main difference		
	RV1126	RV1109
CPU	Quad A7 1.5GHz	Dual A7 1.5GHz
NPU	2.0Tops	1.2Tops
ISP	14M Pixel	5M Pixel

Reference Design Main Functions Introduction	
Power	RK809-2 + 2DCDC
RAM	EMMC/SLC NAND FLASH/SPI FLASH
ROM	DDR3L/DDR3/LPDDR3/LPDDR4
Interface	SDMMC/SDIO/MAC/LCD/CIF/MIPI_DSI/MIPI_CSI0/ MIPI_CSI1/LVDS0/LVDS1/I2S/PDM/USB/ADC

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	00.Cover Page				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	1 of 41

Table of Content

Index and Notes

Note

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Graphic Description

Note

Option

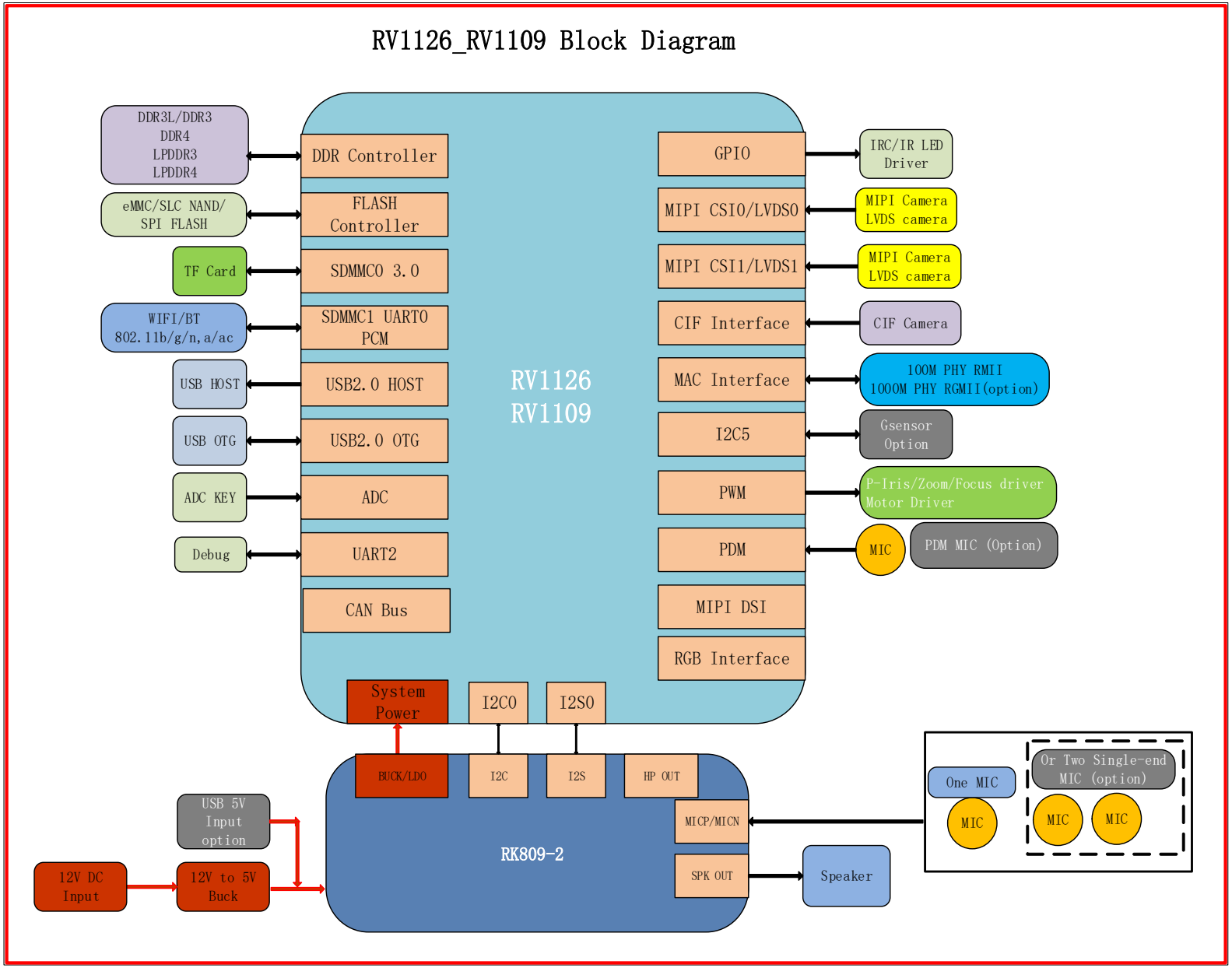
Description

Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics					
Project:	RV1126_RV1109 IPC REF				
File:	01.Index and Notes				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	2 of 41

Revision History

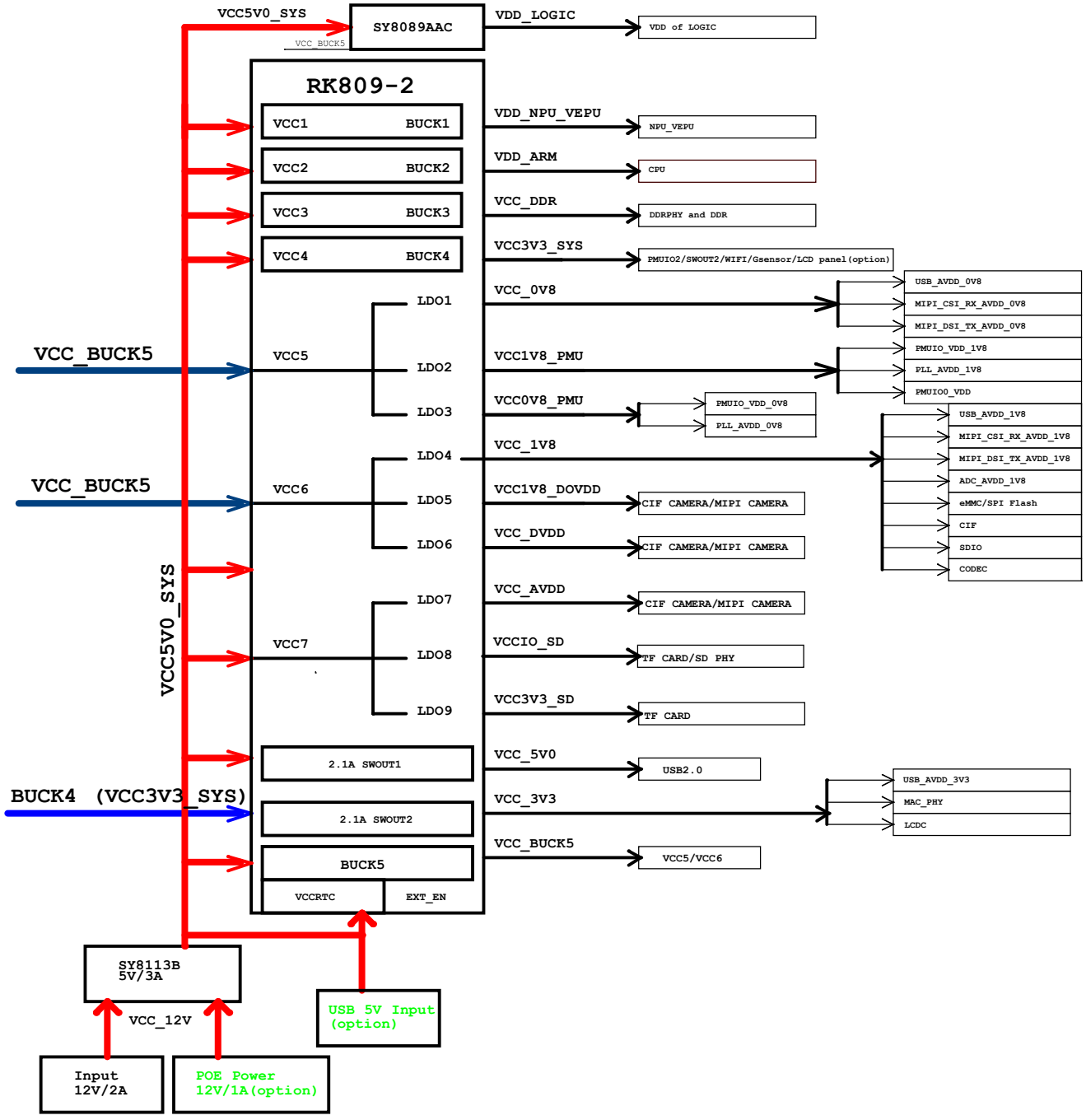
Version	Date	Author	Change Note	Approved
V1.0	2020.04.09	Liyh	IPC REF Design V1.0 for RV1126_RV1109	

RV1126_RV1109 Block Diagram



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	03.Block Diagram				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	4 of 41

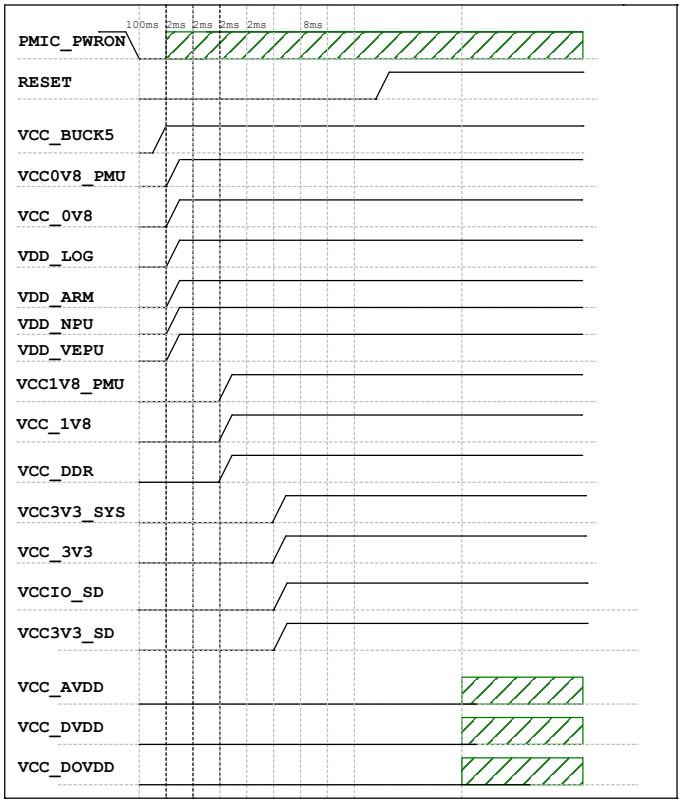
Power Diagram



RV1126_RV1109 Power-on Sequence

Power Name	PMIC Channel	Time Slot (step 2ms)	Default voltage	Supply Limit	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC_BUCK5	RK809-2 BUCK5	Slot: 1	2.2V	2.5A	ON	ON		
VCC0V8_PMU	RK809-2 LDO3	Slot: 2	0.8V	0.1A	ON	ON		
VCC_0V8	RK809-2 LDO1	Slot: 2	0.8V	0.4A	ON	OFF		
VDD_LOGIC	Ext(SY8089AAC)	Slot: 2	0.8V	2.5A	ON	OFF		
VDD_ARM	RK809-2 BUCK2	Slot: 2	0.8V	2.5A	ON	OFF		
VCC1V8_PMU	RK809-2 LDO2	Slot: 3	1.8V	0.4A	ON	ON		
VCC_1V8	RK809-2 LDO4	Slot: 3	1.8V	0.4A	ON	OFF		
VDD_NPU	RK809-2 BUCK1	Slot: 2	0.8V	2.0A	ON	OFF		
VDD_VEPU	RK809-2 BUCK1	Slot: 2	0.8V	2.0A	ON	OFF		
VCC_DDR	RK809-2 BUCK3	Slot: 3	1.5V	1.5A	ON	ON		
VCC3V3_SYS	RK809-2 BUCK4	Slot: 4	3.3V	1.5A	ON	ON		
VCC_3V3	RK809-2 SWOUT2	Slot: 4	3.3V	1.5A	ON	OFF		
VCCIO_SD	RK809-2 LDO8	Slot: 4	3.3V	0.4A	ON	OFF		
VCC3V3_SD	RK809-2 LDO9	Slot: 4	3.3V	0.4A	ON	OFF		
VCC1V8_DOVDD	RK809-2 LDO5		1.8V	0.4A	OFF	OFF		
VCC_DVDD	RK809-2 LDO6		1.2V	0.4A	OFF	OFF		
VCC_AVDD	RK809-2 LDO7		2.8V	0.4A	OFF	OFF		
VCC5V0_HOST	RK809-2 SWOUT1		5V	2.1A	OFF	OFF		
RESET	RK809-2 sent out Reset signal for CPU(timing:10)							

NOTE:VCC_DVDD and VCC_AVDD according to camera sensor voltage



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	04.Power Diagram and Sequence				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	5 of 41

I2C MAP

Port	Pin Name	Domain	Bus Name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Slave Bus Capability	Note
I2C0	I2C0_SCL/GPIO0_B4_u I2C0_SDA/GPIO0_B5_u	PMUIO1	I2C0_SCL_PMIC I2C0_SDA_PMIC	VCC3V3_SYS	RK809-2	0x20		PMIC
I2C1	I2C1_SCL/UART4_CTSN_M2/GPIO1_D3_u I2C1_SDA/UART4_RTSN_M2/GPIO1_D2_u	VCCIO4	I2C1_SCL I2C1_SDA	VCC1V8_DOVDD	IMX323	0X1a		CIF camera
					IMX327	0x34		MIPI camera
I2C5	LCDC_D1/RGMII_CRS_M1/CIF_D1_M1/UART4_CTSN_M1/I2C5_SCL_M0/GPIO2_A5_d LCDC_D7/I2S2_MCLK_M1/CIF_D3_M1/UART5_CTSN_M1/SPI0_CS1n_M2/PWM0_M1/I2C5_SDA_M0/GPIO2_B3_d	VCCIO5	I2C5_SCL_M0 I2C5_SDA_M0	VCC3V3_sensor	MAX6655XA	0x15		Gsensor
					MMC3630KJ	0x30		Magnetic

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Project:	RV1126_RV1109 IPC REF				
File:	05.I2C MAP				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
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IO Power Domain Map

IO Domain	IO Group	Support of IO Voltage		Default Actual assigned IO Domain Voltage			Notes
		1.8V	3.3V	Net Name of Power Supply	Power Source	Voltage	
PMUIO0	***GPIO0A***	✓	✓	*VCC1V8_PMU*	*RK809-2_LDO2*	*1.8V*	
PMUIO1	***GPIO0BC***	✓	✓	*VCC3V3_SYS*	*RK809-2_BUCK4*	*3.3V*	
VCCIO1	***GPIO0CD/GPIO1A***	✓	✓	*VCCIO_FLASH*	*RK809-2_LDO4*	*1.8V*	*GPIO0_B3/FLASH_VOL_SEL pin defined as a set pin for VCCIO1 voltage domain after power-on reset.It is pull-up for 1.8V*
VCCIO2	***GPIO1AB***	✓	✓	*VCCIO_SD*	*RK809-2_LDO8*	*3.3V*	
VCCIO3	***GPIO1BCD***	✓	✓	*VCCIO3_VDD*	*RK809-2_LDO4*	*1.8V*	
VCCIO4	***GPIO1D/GPIO2A***	✓	✓	*VCCIO4_VDD*	*RK809-2_LDO4*	*1.8V*	
VCCIO5	***GPIO2ABCD/GPIO3A***	✓	✓	*VCCIO5_VDD*	*RK809-2_SWOUT2*	*3.3V*	
VCCIO6	***GPIO3ABC***	✓	✓	*VCCIO6_VDD*	*RK809-2_LDO4*	*1.8V*	
VCCIO7	***GPIO3D/GPIO4A***	✓	✓	*VCCIO7_VDD*	*RK809-2_LDO4*	*1.8V*	

Power

U1000N
SOC_RV1126/RV1109
BGA409 14R00X14R00X0R90

NPU/LOGIC/VEPU/ARM Power

NPU_VDD_1	H11
NPU_VDD_2	H12
NPU_VDD_3	J10
NPU_VDD_4	J11
NPU_VDD_5	K10
NPU_VDD_6	K11
LOGIC_VDD_1	H9
LOGIC_VDD_2	J9
LOGIC_VDD_3	L10
LOGIC_VDD_4	M11
LOGIC_VDD_5	H13
LOGIC_VDD_6	J13
VEPU_VDD_1	L9
VEPU_VDD_2	M9
VEPU_VDD_3	N8
VEPU_VDD_4	N9
ARM_VDD_1	N12
ARM_VDD_2	P12
ARM_VDD_3	P13

VDD_NPU_VEPU
VDD_LOGIC
VDD_NPU_VEPU
VDD_ARM

Supply for VCCIO1~7 Power

VCCIO_VDD_1V8 H14

VCC_1V8

C1000 100nF X5R 6.3V C0402

VDD_NPU_VEPU

C1006 10uF X5R 4V C0402
C1005 1uF X5R 6.3V C0402
C1004 1uF X5R 6.3V C0402
C1003 100nF X5R 6.3V C0201
C1002 100nF X5R 6.3V C0201
C1001 100nF X5R 6.3V C0201

For NPU Power

VDD_NPU_VEPU

C1019 10uF X5R 4V C0402
C1018 1uF X5R 6.3V C0402
C1017 100nF X5R 6.3V C0201
C1016 100nF X5R 6.3V C0201

For VEPU Power

VDD_ARM

C1015 10uF X5R 4V C0402
C1014 1uF X5R 6.3V C0402
C1013 100nF X5R 6.3V C0201
C1012 100nF X5R 6.3V C0201

VDD_LOGIC

C1011 10uF X5R 4V C0402
C1009 1uF X5R 6.3V C0402
C1010 1uF X5R 6.3V C0402
C1007 100nF X5R 6.3V C0201
C1008 100nF X5R 6.3V C0201

GND

U1000O
SOC_RV1126/RV1109
BGA409 14R00X14R00X0R90

VSS/AVSS

A1	VSS_1	VSS_53	K9
A21	AVSS_2	VSS_54	K12
B12	VSS_3	VSS_55	K13
C3	VSS_4	VSS_56	K14
C5	VSS_5	VSS_57	L2
C7	VSS_6	VSS_58	L5
C10	VSS_7	VSS_59	L6
C12	VSS_8	VSS_60	L11
D9	VSS_9	VSS_61	L12
D12	VSS_10	VSS_62	L13
D18	AVSS_11	VSS_63	L14
E4	VSS_12	VSS_64	L16
E6	VSS_13	VSS_65	M3
E8	VSS_14	VSS_66	M5
E9	VSS_15	VSS_67	M7
E10	VSS_16	VSS_68	M8
E11	VSS_17	VSS_69	M10
E12	VSS_18	VSS_70	M12
F3	VSS_19	VSS_71	M13
F5	VSS_20	VSS_72	M14
F7	VSS_21	VSS_73	M16
F8	VSS_22	VSS_74	N5
F9	VSS_23	VSS_75	N6
F10	VSS_24	VSS_76	N7
F11	VSS_25	VSS_77	N10
F12	VSS_26	VSS_78	N11
F13	VSS_27	VSS_79	N13
F14	AVSS_28	VSS_80	N14
F15	AVSS_29	VSS_81	N16
G2	VSS_30	VSS_82	P5
G5	VSS_31	VSS_83	P7
G6	VSS_32	VSS_84	P8
G10	VSS_33	VSS_85	P9
G11	VSS_34	VSS_86	P14
G12	VSS_35	VSS_87	P16
G13	VSS_36	VSS_88	R1
G16	AVSS_37	VSS_89	R5
G17	AVSS_38	VSS_90	R12
H4	VSS_39	VSS_91	R13
H5	VSS_40	VSS_92	R14
H6	VSS_41	VSS_93	T6
H7	VSS_42	VSS_94	T9
H10	VSS_43	VSS_95	T10
H15	VSS_44	VSS_96	T14
J5	VSS_45	VSS_97	T17
J6	VSS_46	VSS_98	V17
J12	VSS_47	VSS_99	W9
J14	VSS_48	VSS_100	W14
J16	VSS_49	VSS_101	AA1
K5	VSS_50	VSS_102	AA10
K6	VSS_51	VSS_103	AA21
K8	VSS_52		

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	10.RV1126/1109_Power/GND				
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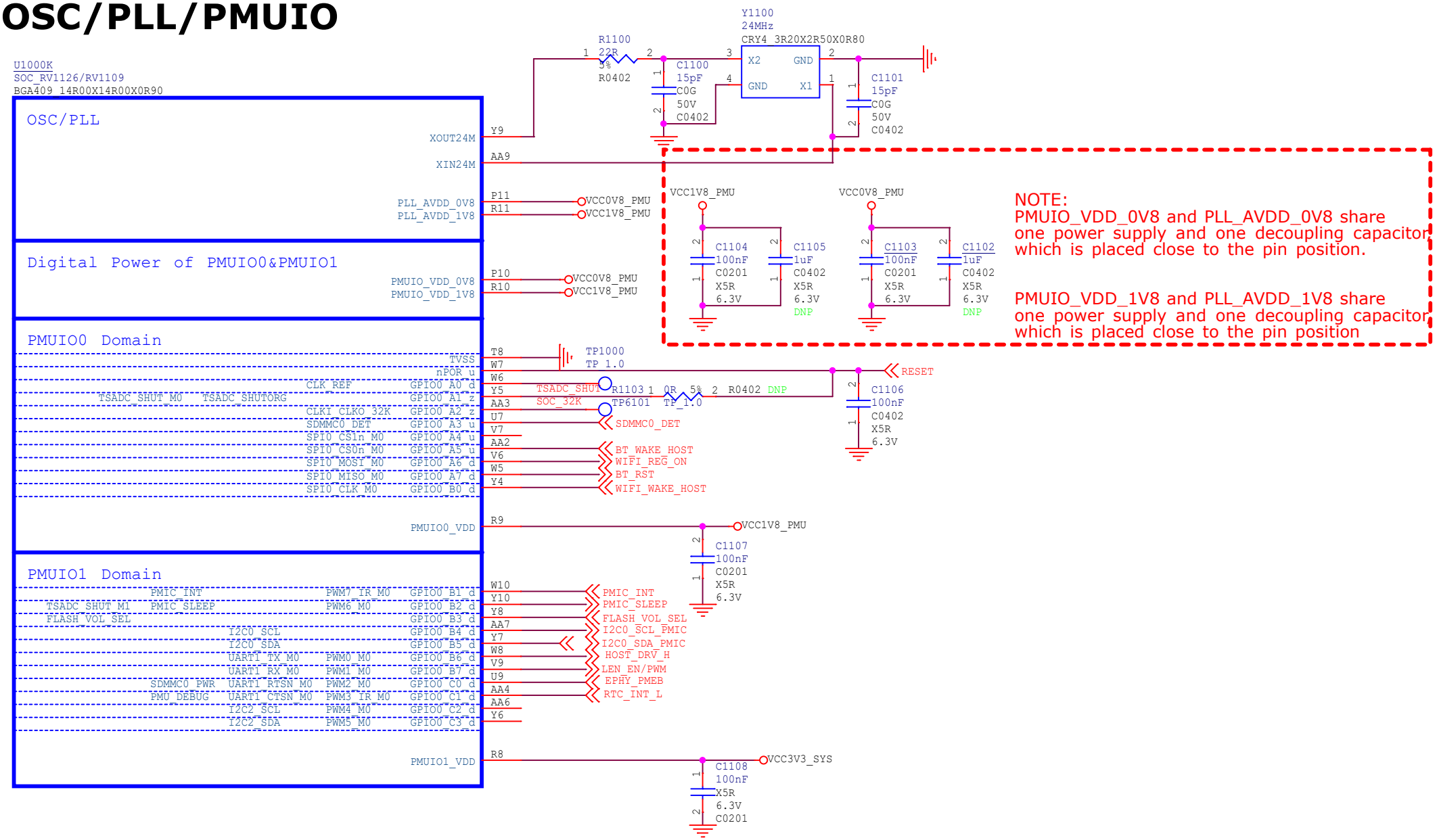
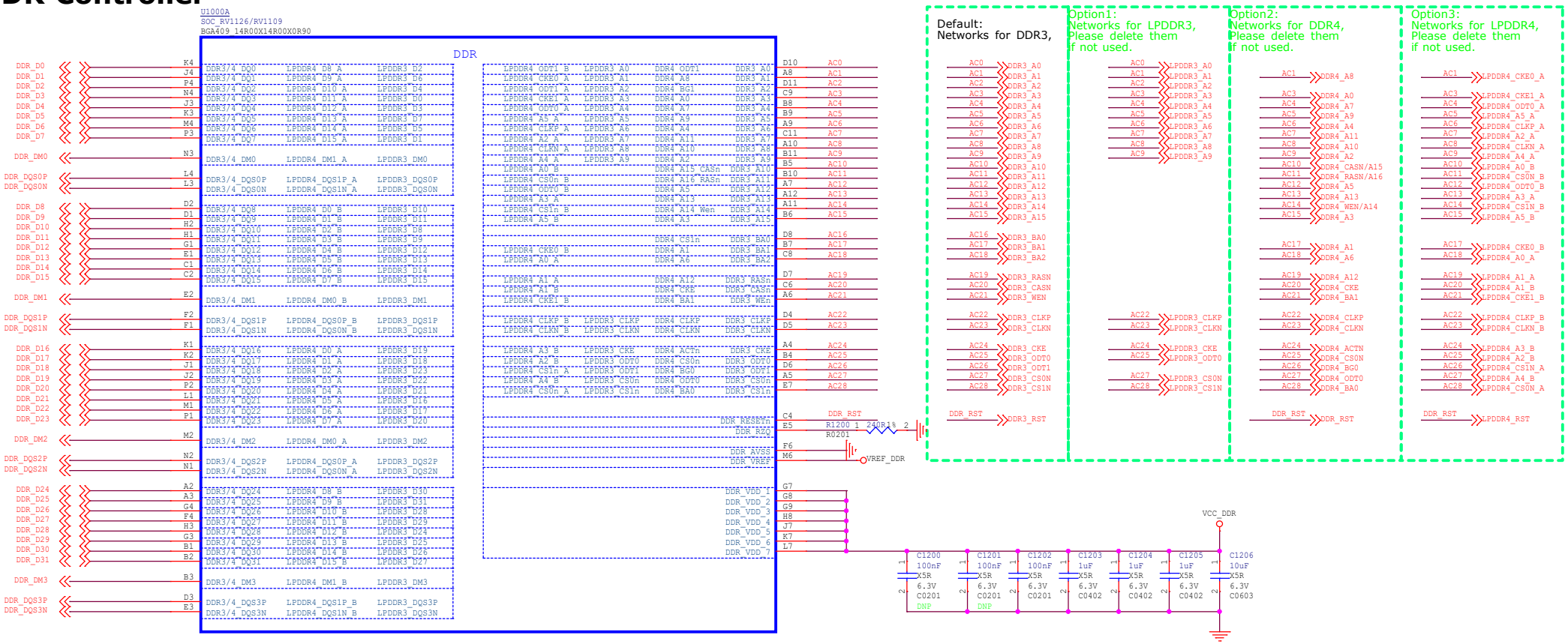
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	8 of 41

OSC/PLL/PMUIO



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	11.RV1126/1109_OSC/PLL/PMUIO				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	9 of 41

DDR Controller



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RV1126_RV1109 IPC REF		
File:	12.RV1126/1109_DRAM Controller		
Date:	Tuesday, April 14, 2020	Rev:	V1.0
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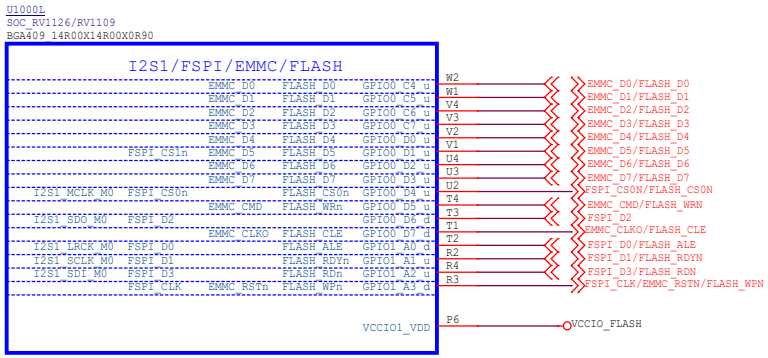
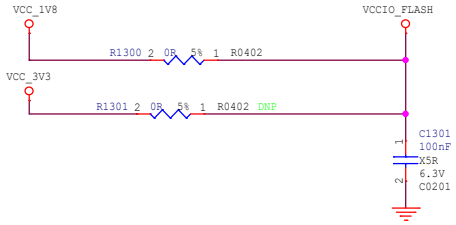
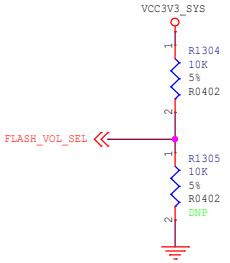
EMMC/FLASH



NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.





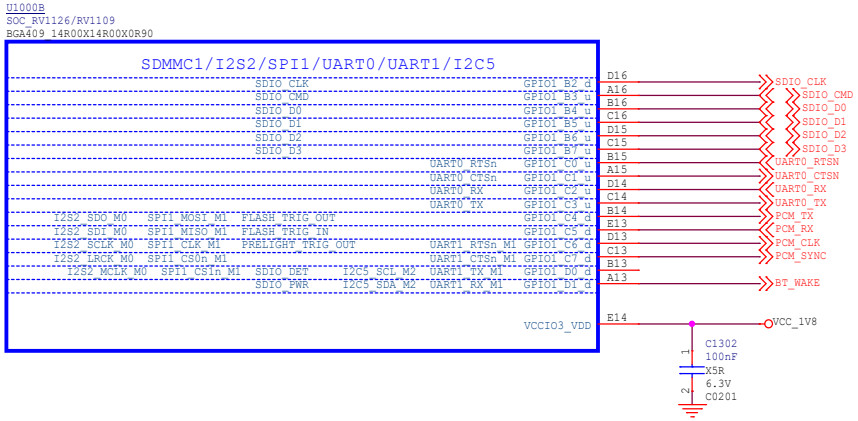
NOTE:
FLASH(VCCIO1) power domain IO supply configuration pin:

Condition	VCCIO1 (VCCIO_FLASH)
FLASH_VOL_SEL=0	3.3V
FLASH_VOL_SEL=1	1.8V Default

SDMMC0/JTAG

NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.

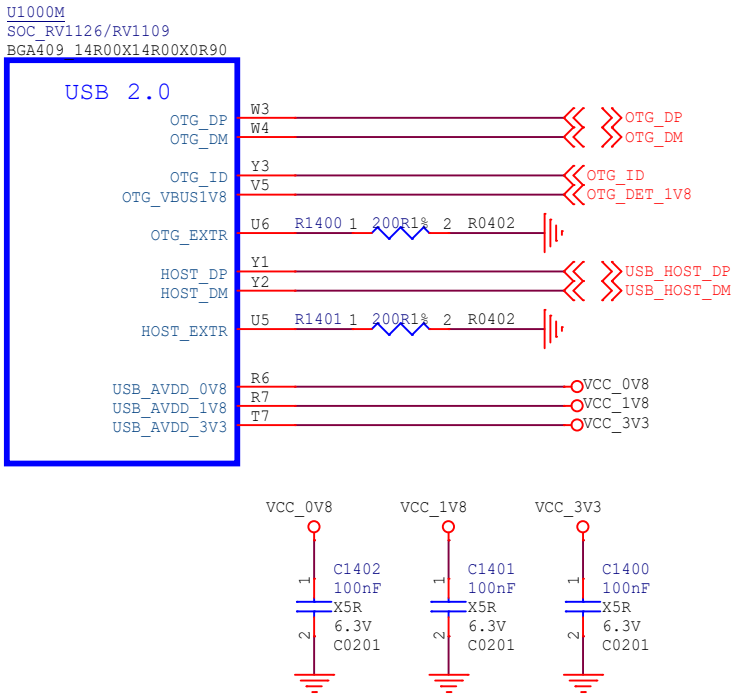
SDMMC1/UART/I2S2



NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RV1126_RV1109 IPC REF		
File:	13.RV1126/1109_Flash/SD		
Date:	Tuesday, April 14, 2020	Rev:	V1.0
Designed by: Yanhong.Li	Reviewed by: <Checker>	Sheet:	11 of 41

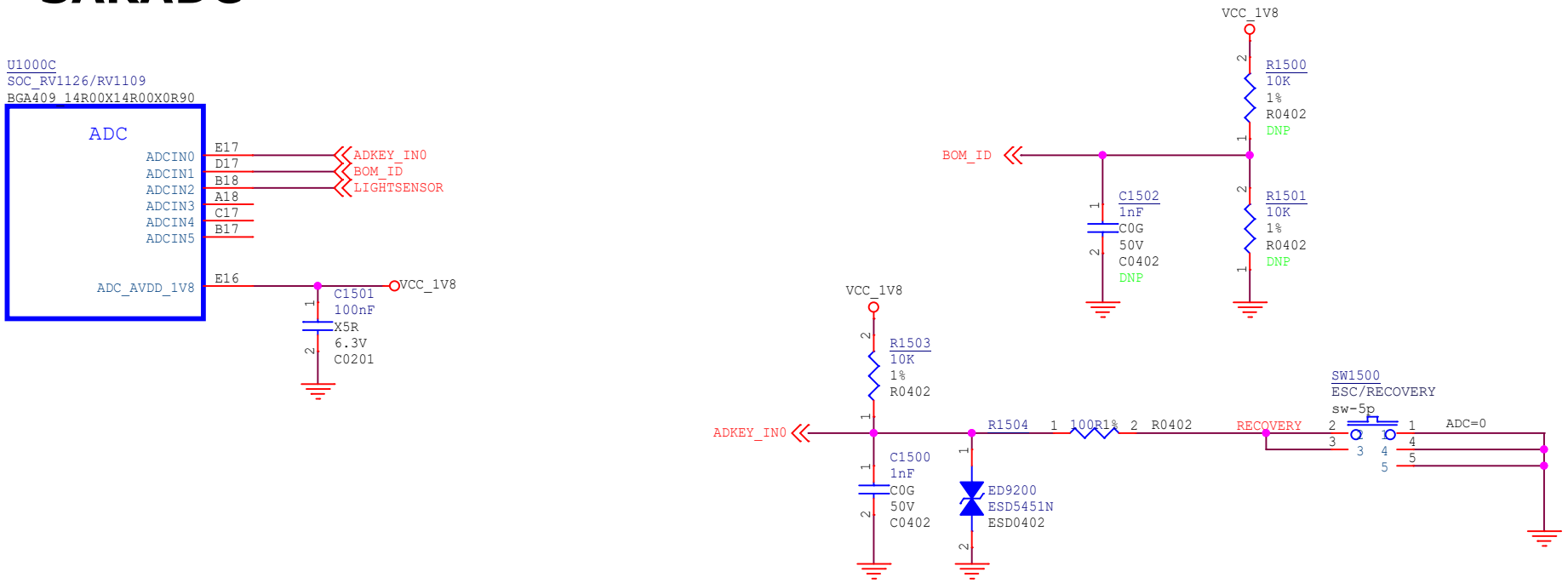
USB Controller



USB2.0 design rules:
1. Max intra-pair skew <4ps
2. Max trace length<6inchs
3. Max allowed via <6
4. Trace impedance 90ohm+/-10%
5. The distance between other signals follows the 3W rule.

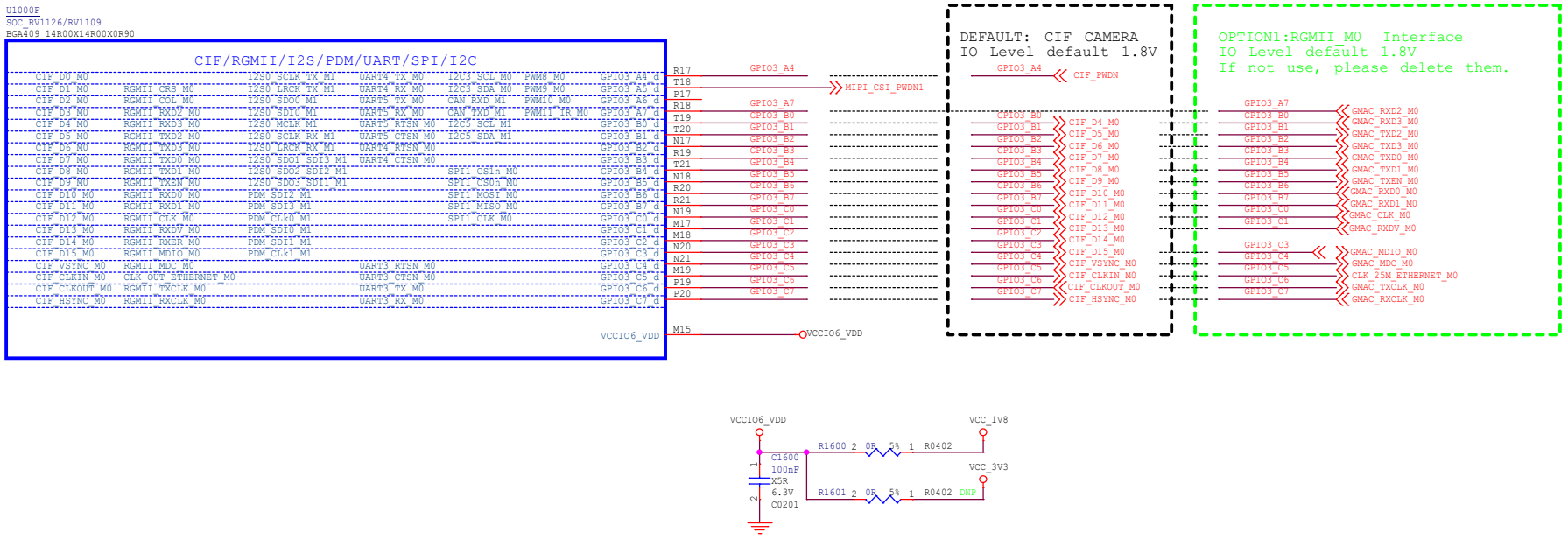
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	14.RV1126/1109_USB Controller				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	12 of 41

SARADC



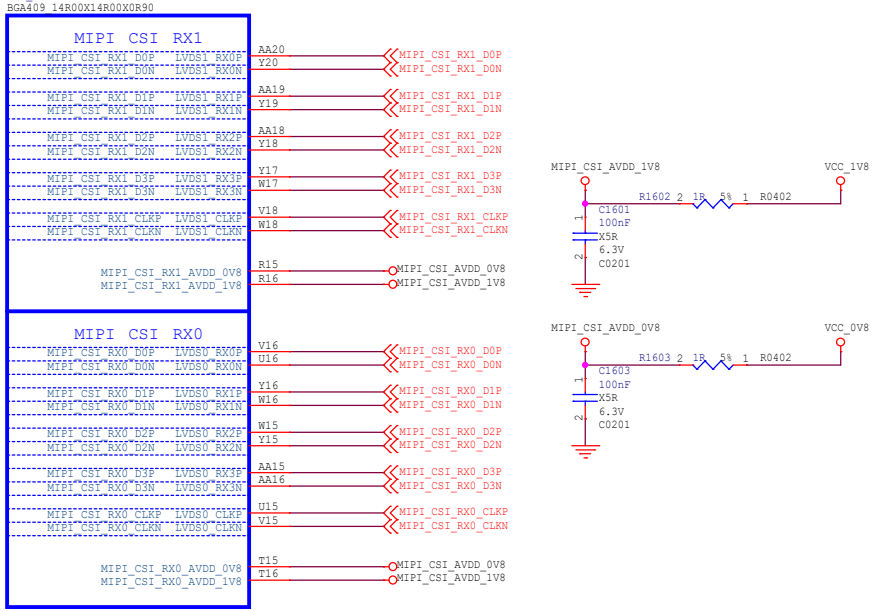
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	15.RV1126/1109_SARADC				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	13 of 41

CIF Interface

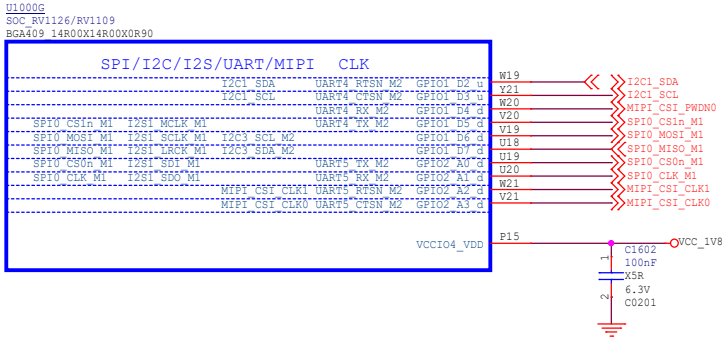


MIPI-CSI Interface

MIPI_CSI_RX0 and MIPI_CSI_RX1 power pins are adjacent, so they share a decoupling capacitor
All the power filter capacitors should be placed close to the power pins of SOC.



I2C/SPI/MIPI-CLK



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RV1126_RV1109 IPC REF		
File:	16.RV1126/1109_VideoInput		
Date:	Tuesday, April 14, 2020	Rev:	V1.0
Designed by: Yanhong.Li	Reviewed by: <Checker>	Sheet:	14 of 41

LCDC/RGMII/PWM

U1000E
SOC_RV1126/RV1109
BGA409_14R00X14R00X0R90

LCDC/RGMII/CIF/UART/JTAG/I2S/SPI/I2C

		UART4_RTSN_M1		RGMII_TXD3_M1		CIF_D0_M1	LCDC_D0	GPIO2_A4_d	J18
I2C5_SCL_M0		UART4_CTSN_M1		RGMII_CRS_M1		CIF_D1_M1	LCDC_D1	GPIO2_A5_d	L17
		UART4_TX_M1	PWM5_M1	RGMII_COL_M1		CIF_D2_M1	LCDC_D2	GPIO2_A6_d	M21
	I2S2_SDO_M1	UART4_RX_M1	PWM4_M1	SPI0_CSn0_M2			LCDC_D3	GPIO2_A7_d	M20
	I2S2_SDI_M1	UART5_TX_M1	PWM3_IR_M1	SPI0_MOSI_M2			LCDC_D4	GPIO2_B0_d	L19
	I2S2_SCLK_M1	UART5_RX_M1	PWM2_M1	SPI0_MISO_M2			LCDC_D5	GPIO2_B1_d	L20
	I2S2_LRCK_M1	UART5_RTSN_M1	PWM1_M1	SPI0_CLK_M2			LCDC_D6	GPIO2_B2_d	K16
I2C5_SDA_M0	I2S2_MCLK_M1	UART5_CTSN_M1	PWM0_M1	SPI0_CS1n_M2		CIF_D3_M1	LCDC_D7	GPIO2_B3_d	K17
				RGMII_RXDV_M1		CIF_D4_M1	LCDC_D8	GPIO2_B4_d	K18
				RGMII_RXD0_M1		CIF_D5_M1	LCDC_D9	GPIO2_B5_d	K19
				RGMII_RXD1_M1		CIF_D6_M1	LCDC_D10	GPIO2_B6_d	K20
				RGMII_CLK_M1		CIF_D7_M1	LCDC_D11	GPIO2_B7_d	K21
				RGMII_RXER_M1		CIF_D8_M1	LCDC_D12	GPIO2_C0_d	J19
				RGMII_MDIO_M1		CIF_D9_M1	LCDC_D13	GPIO2_C1_d	J21
				RGMII_MDC_M1		CIF_D10_M1	LCDC_D14	GPIO2_C2_d	J20
				RGMII_TXD0_M1		CIF_D11_M1	LCDC_D15	GPIO2_C3_d	H20
				RGMII_TXD1_M1		CIF_D12_M1	LCDC_D16	GPIO2_C4_d	H19
				CLK_OUT_ETHERNET_M1		CIF_D13_M1	LCDC_D17	GPIO2_C5_d	G21
				RGMII_TXEN_M1		CIF_D14_M1	LCDC_D18	GPIO2_C6_d	G20
	I2S1_MCLK_M2			RGMII_RXD2_M1		CIF_D15_M1	LCDC_D19	GPIO2_C7_d	G19
	I2S1_SDO_M2			RGMII_RXD3_M1		CIF_VSYNC_M1	LCDC_D20	GPIO2_D0_d	H18
	I2S1_SCLK_M2			RGMII_TXD2_M1		CIF_CLKOUT_M1	LCDC_D21	GPIO2_D1_d	F21
	I2S1_LRCK_M2			RGMII_TXCLK_M1		CIF_CLKIN_M1	LCDC_D22	GPIO2_D2_d	F20
	I2S1_SDI_M2			RGMII_RXCLK_M1		CIF_HSYNC_M1	LCDC_D23	GPIO2_D3_d	F19
I2C3_SCL_M1			PWM6_M1	SPI1_CSn0_M2			LCDC_DEN	GPIO2_D4_d	J17
I2C3_SDA_M1			PWM10_M1	SPI1_CLK_M2			LCDC_HSYNC	GPIO2_D5_d	H17
		UART3_RTSN_M2	PWM9_M1	SPI1_MOSI_M2			LCDC_VSYNC	GPIO2_D6_d	C21
		UART3_CTSN_M2	PWM8_M1	SPI1_MISO_M2			LCDC_CLK	GPIO2_D7_d	D21
I2C4_SCL_M0	CAN_RXD_M0	UART3_TX_M2	PWM7_IR_M1	SPI1_CS1n_M2				GPIO3_A0_u	E20
I2C4_SDA_M0	CAN_TXD_M0	UART3_RX_M2	PWM11_IR_M1					GPIO3_A1_u	E19
A7_JTAG_TCK_M1		UART2_TX_M1						GPIO3_A2_u	G18
A7_JTAG_TMS_M1		UART2_RX_M1						GPIO3_A3_u	H16

J18 ICR_AIN
L17 EPHY_RSTn
M21 P_IN1_PWM5_M1
M20 P_IN2_PWM4_M1
L19 P_IN3_PWM3_M1
L20 P_IN4_PWM2_M1
K16 P_IRIS/ZOOM/FOCUS_AIN1
K17 P_IRIS/ZOOM/FOCUS_AIN2
K18 RMII_RXDV
K19 RMII_RXD0
K20 RMII_RXD1
K21 RMII_CLK
J19 RMII_RXER
J21 RMII_MDIO
J20 RMII_MDC
H20 RMII_TXD0
H19 RMII_TXD1
G21
G20 RMII_TXEN
G19
H18 ICR_BIN
F21 ZOOM_EN_H
F20 FOCUS_EN_H
F19 P_IRIS_EN_H
J17 T_IN1_PWM6_M1
H17 T_IN2_PWM10_M1
C21 T_IN3_PWM9_M1
D21 T_IN4_PWM8_M1
E20 P_IRIS/ZOOM/FOCUS_BIN1
E19 P_IRIS/ZOOM/FOCUS_BIN2
G18 UART2_TX
H16 UART2_RX

VCCIO5_VDD1 J15
VCCIO5_VDD2 K15
VCC_3V3

C1700
100nF
X5R
6.3V
C0201

UART DEBUG

UART2_TX R1700 1 100R 2 5% R0402 DEBUG_TX TP1700
UART2_RX R1702 1 100R 2 5% R0402 DEBUG_RX TP1701
D1701 ESD5471X ESD0402
D1700 ESD5471X ESD0402
TP1702

MIPI-DSI Interface

U1000D
SOC_RV1126/RV1109
BGA409_14R00X14R00X0R90

MIPI_DSI_TX0

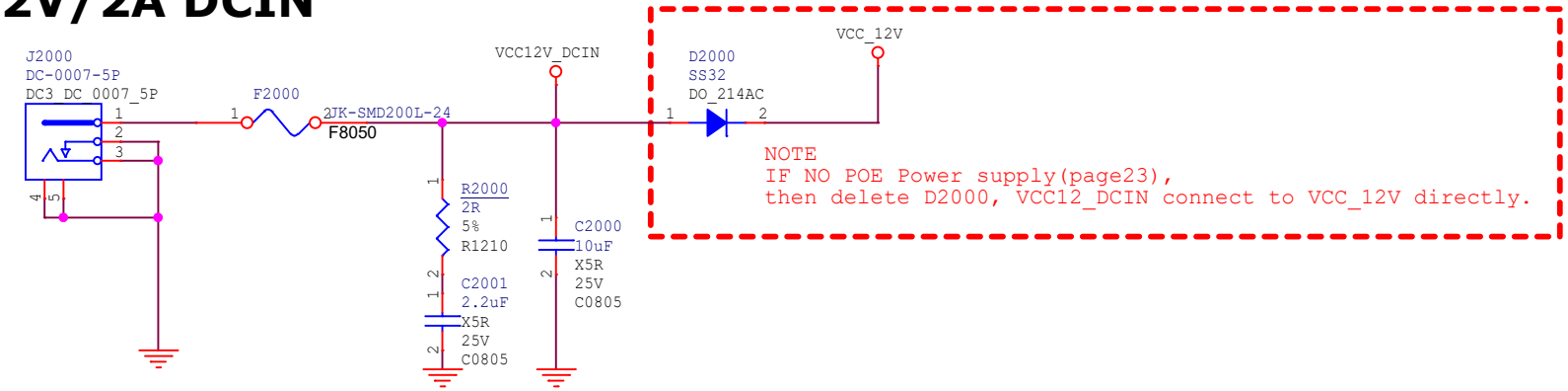
MIPI_DSI_TX0_D0P	A19
MIPI_DSI_TX0_D0N	B19
MIPI_DSI_TX0_D1P	A20
MIPI_DSI_TX0_D1N	B20
MIPI_DSI_TX0_D2P	B21
MIPI_DSI_TX0_D2N	C20
MIPI_DSI_TX0_D3P	D20
MIPI_DSI_TX0_D3N	D19
MIPI_DSI_TX0_CLKP	C19
MIPI_DSI_TX0_CLKN	C18
MIPI_DSI_TX0_AVDD_0V8	E18
MIPI_DSI_TX0_AVDD_1V8	G15

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics			
Project:	RV1126_RV1109 IPC REF			
File:	17.RV1126/1109_VideoOutput Interface			
Date:	Tuesday, April 14, 2020		Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by: <Checker>	Sheet:	15 of 41

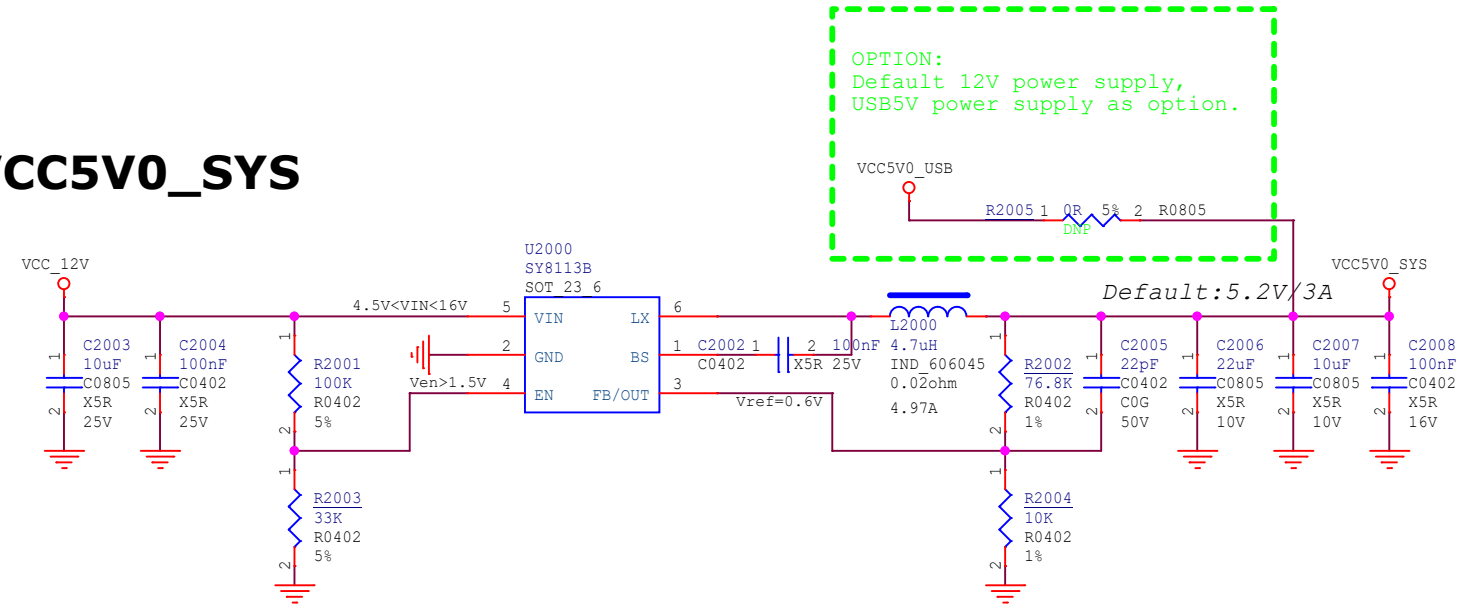
Audio Interface

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	18.RV1126/1109_Audio				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	16 of 41

12V/2A DCIN

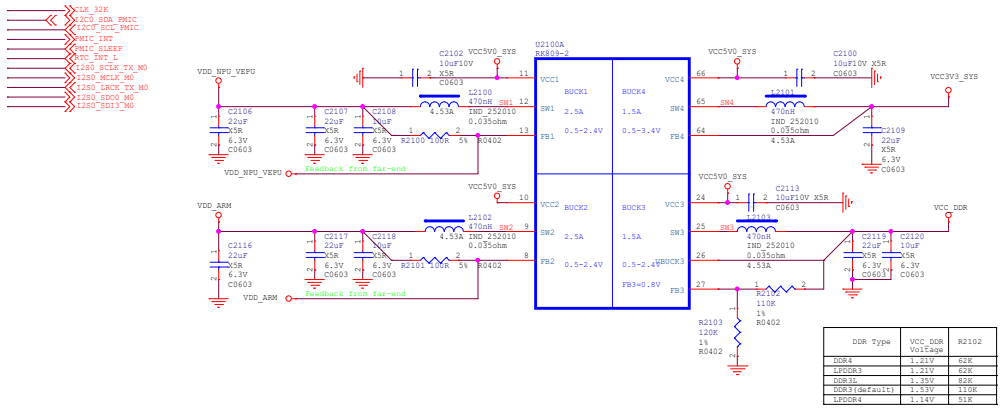


VCC5V0_SYS



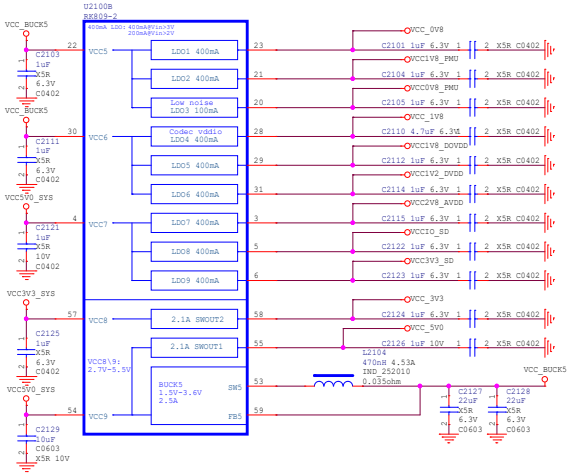
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	20.Power_DC IN				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	17 of 41

PMIC RK809-2 DCDC

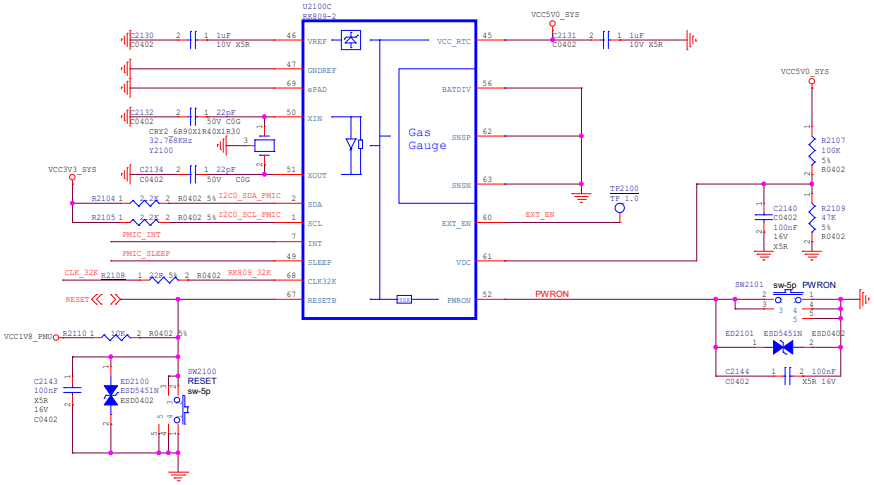


DDR Type	VCC_DDR Voltage	R2102
DDR4	1.21V	62K
LPDDR3	1.21V	62K
DDR3L	1.35V	82K
DDR3(default)	1.53V	110K
LPDDR4	1.14V	51K

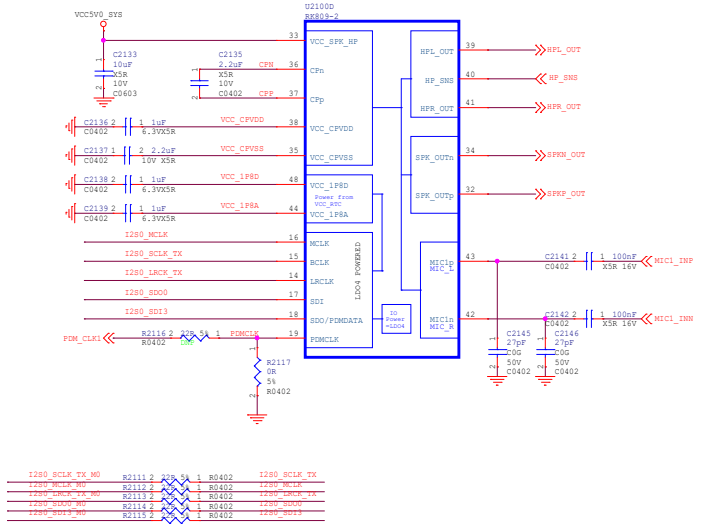
PMIC RK809-2 LDO



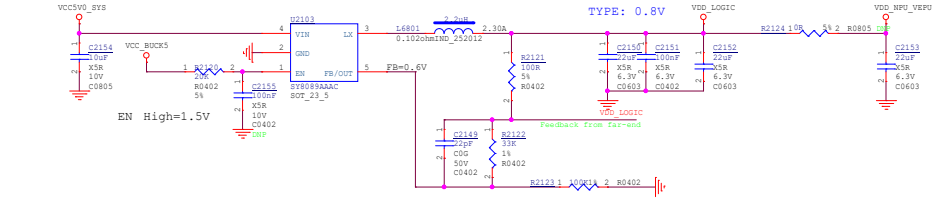
PMIC RK809-2 Managerment

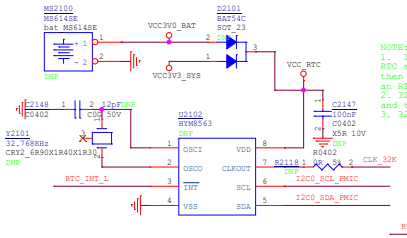


PMIC RK809-2 CODEC



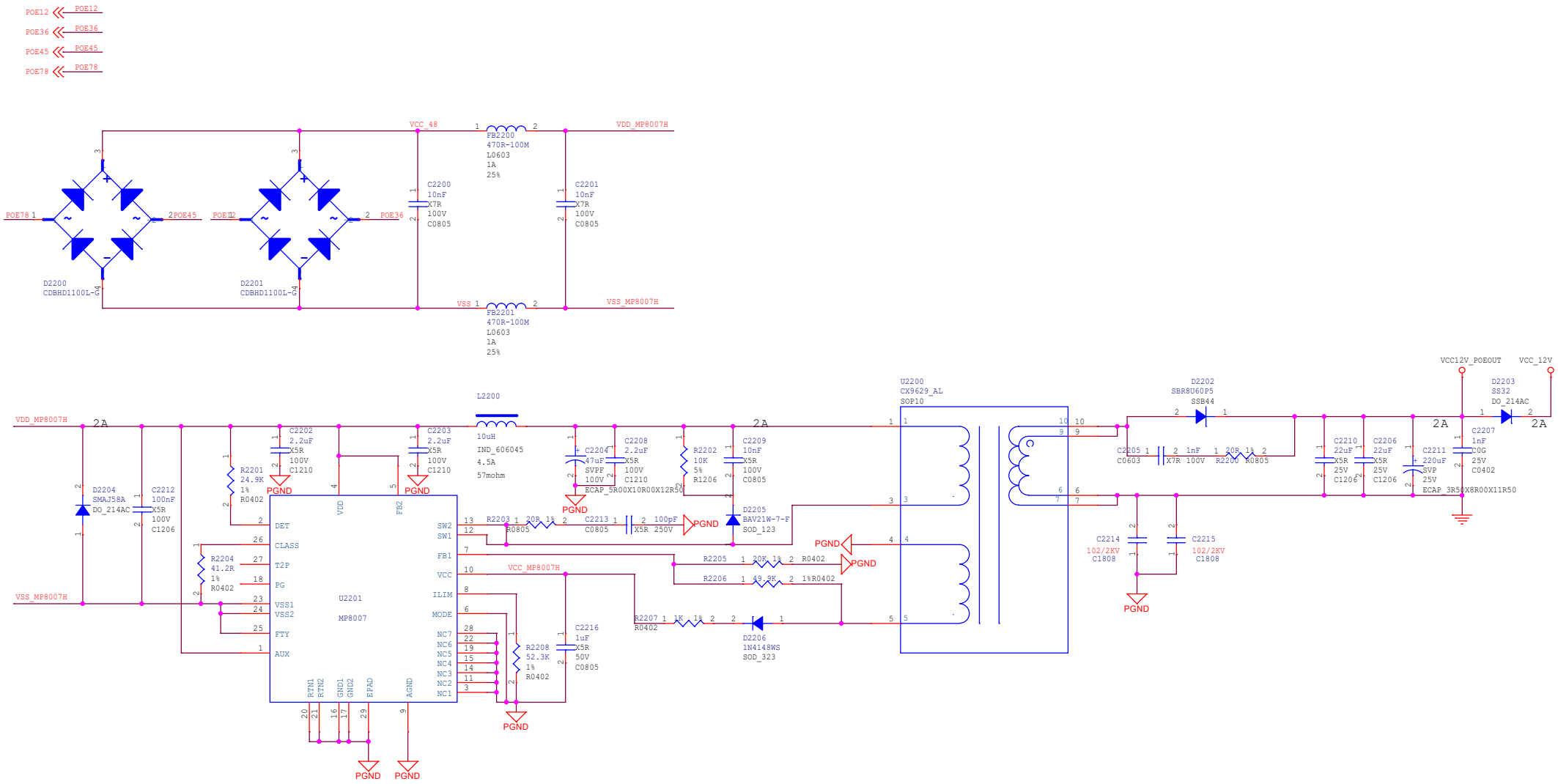
VDD_LOGIC





NOTE:
1. IPC: after the system is powered off, RTC still need to work, then it is necessary to add an RTC IC ,and use battery to power the RTC.
2. 32K crystal is connected to RTC, and the 32K crystal of rk809-2 can be DNP.
3. 32kclk signal can only be output from RTC.

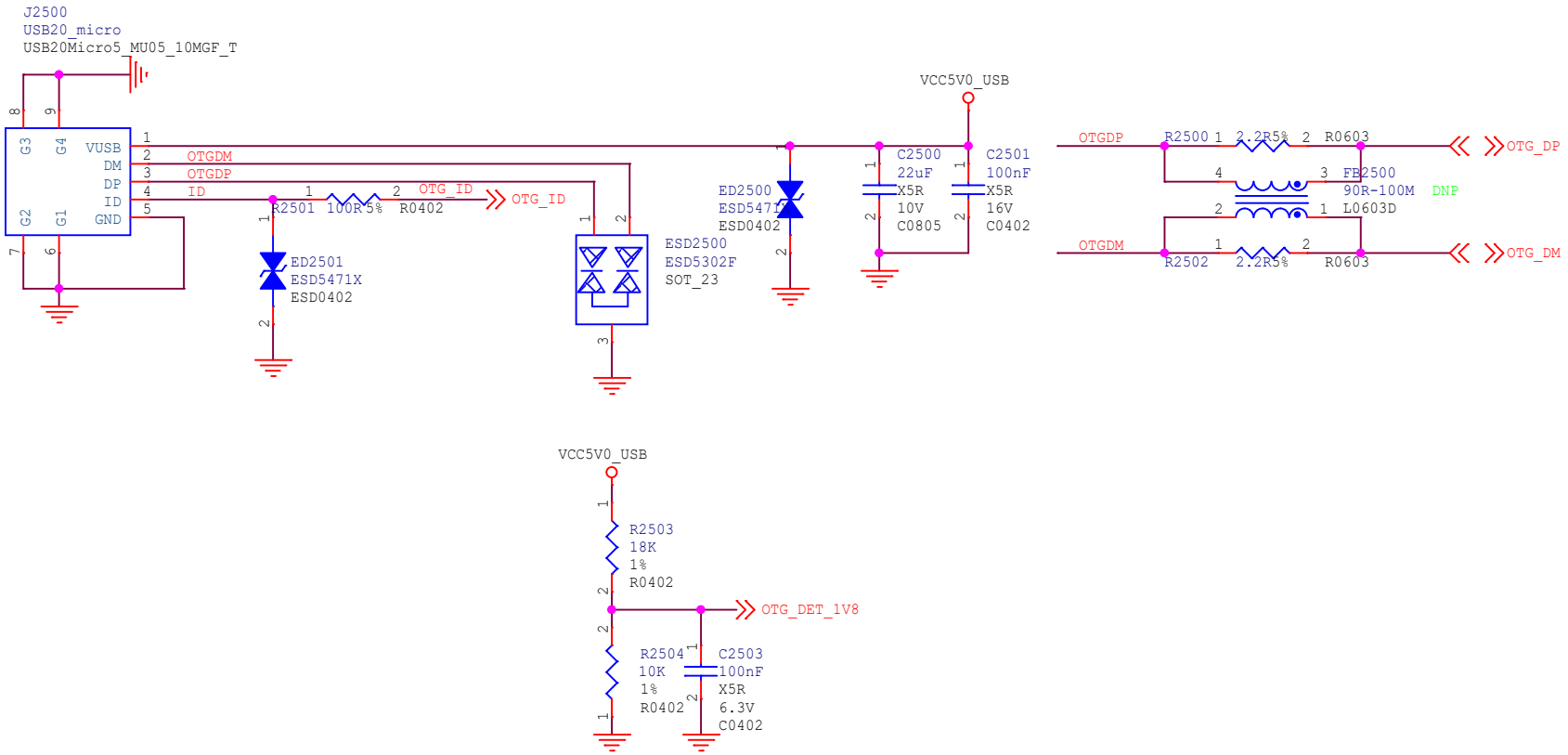
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RV1126_RV1109 IPC REF		
File:	21.Power_PMIC		
Date:	Tuesday, April 14, 2020	Rev:	V1.0
Designed by: Yanhong.Li	Reviewed by: <Checker>	Sheet:	18 of 41



Class	Max Input Power to PD(W)	Classification Current(mA)	R2204(Rclass)
0	12.95	2	578R
1	3.84	10.55	110R
2	6.49	18.7	62R
3	12.95	28.15	41.2R
4	25.5	40.4	28.7R

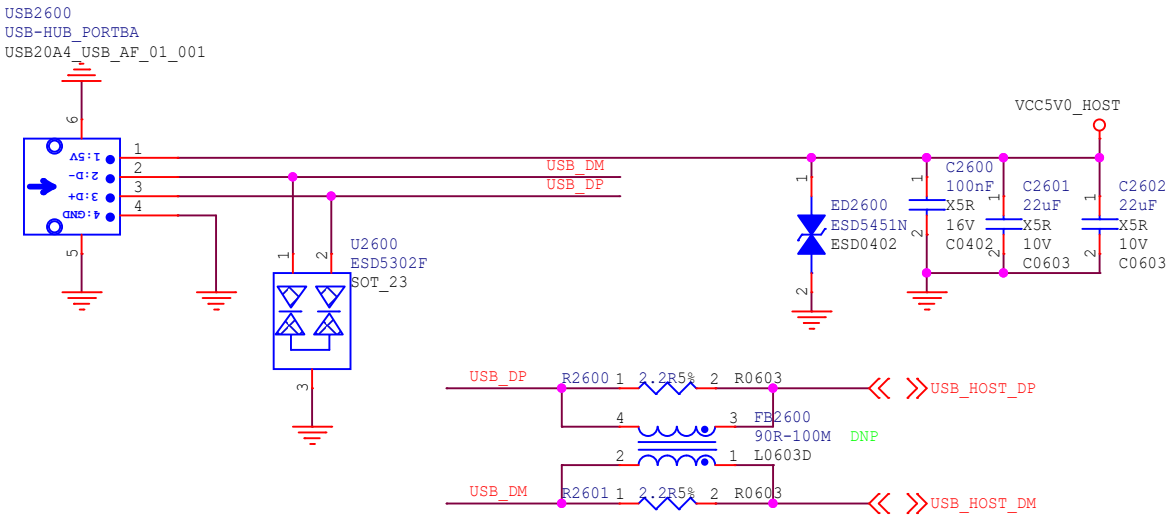
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	23.POE Power(option)				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	19 of 41

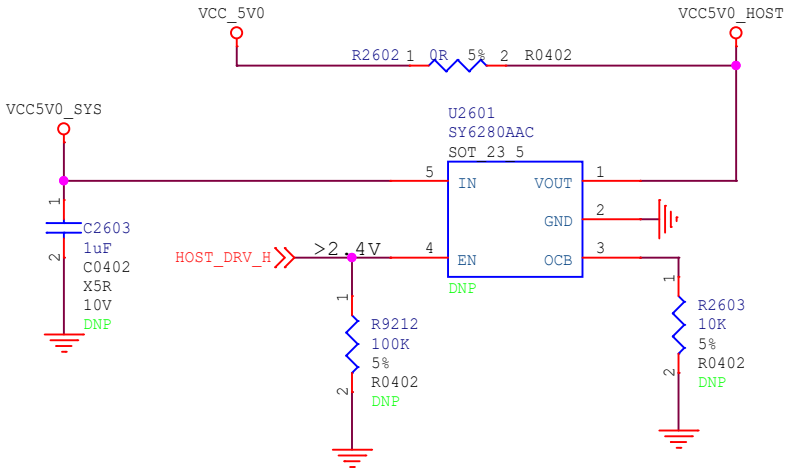
USB2.0 OTG



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	25.USB OTG				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	20 of 41

USB HOST

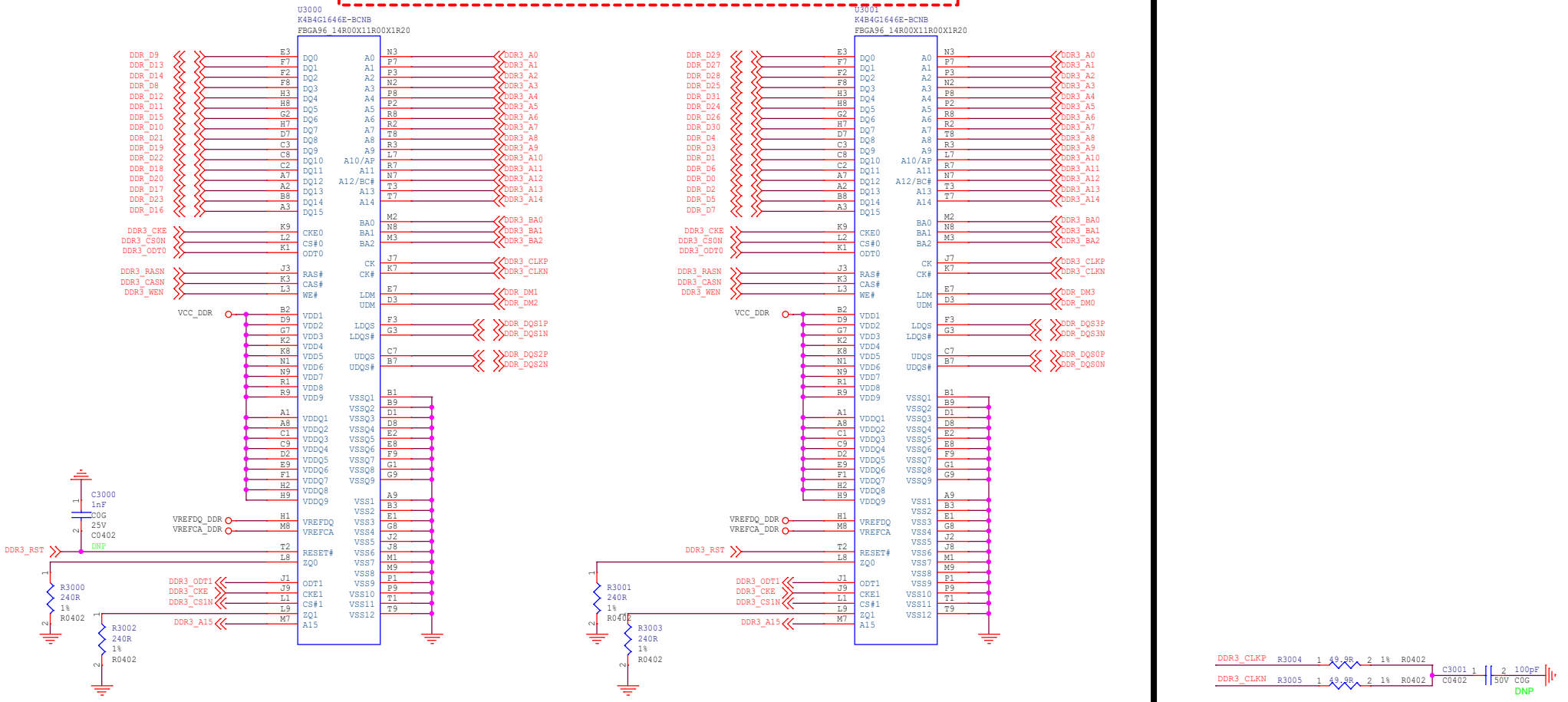




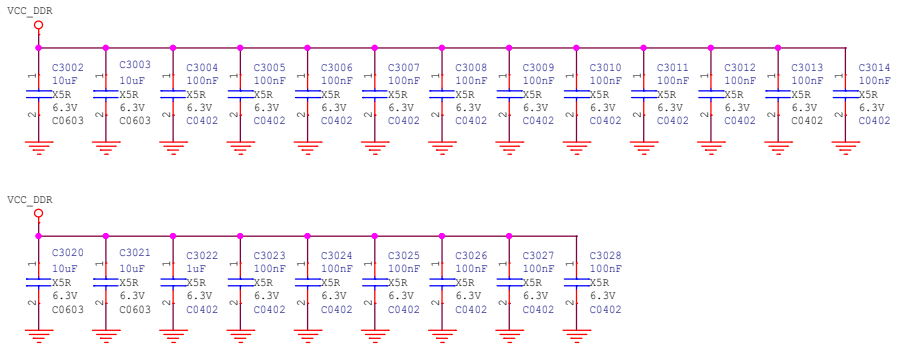
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	26.USB Host				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	21 of 41

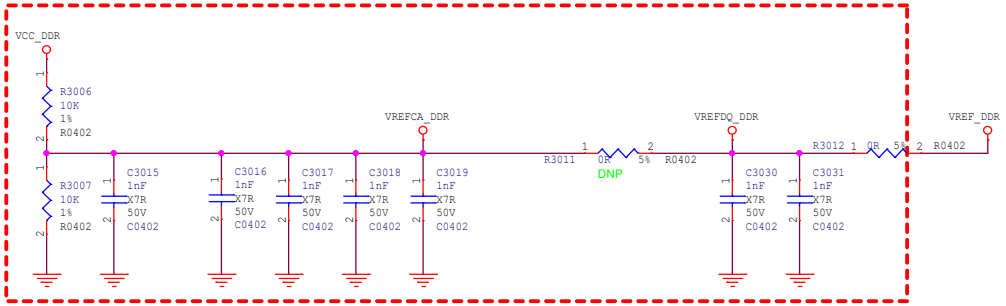
DDR3/DDR3L 2x16bit

NOTE:
This is a two DDR3 template. If only one DDR3 is used, please use DDR_DQ0 ~ DQ15
Refer to the latest AVL for parts selection.



Note:All the Power filter capacitors should be placed close to the power pins of DDR3



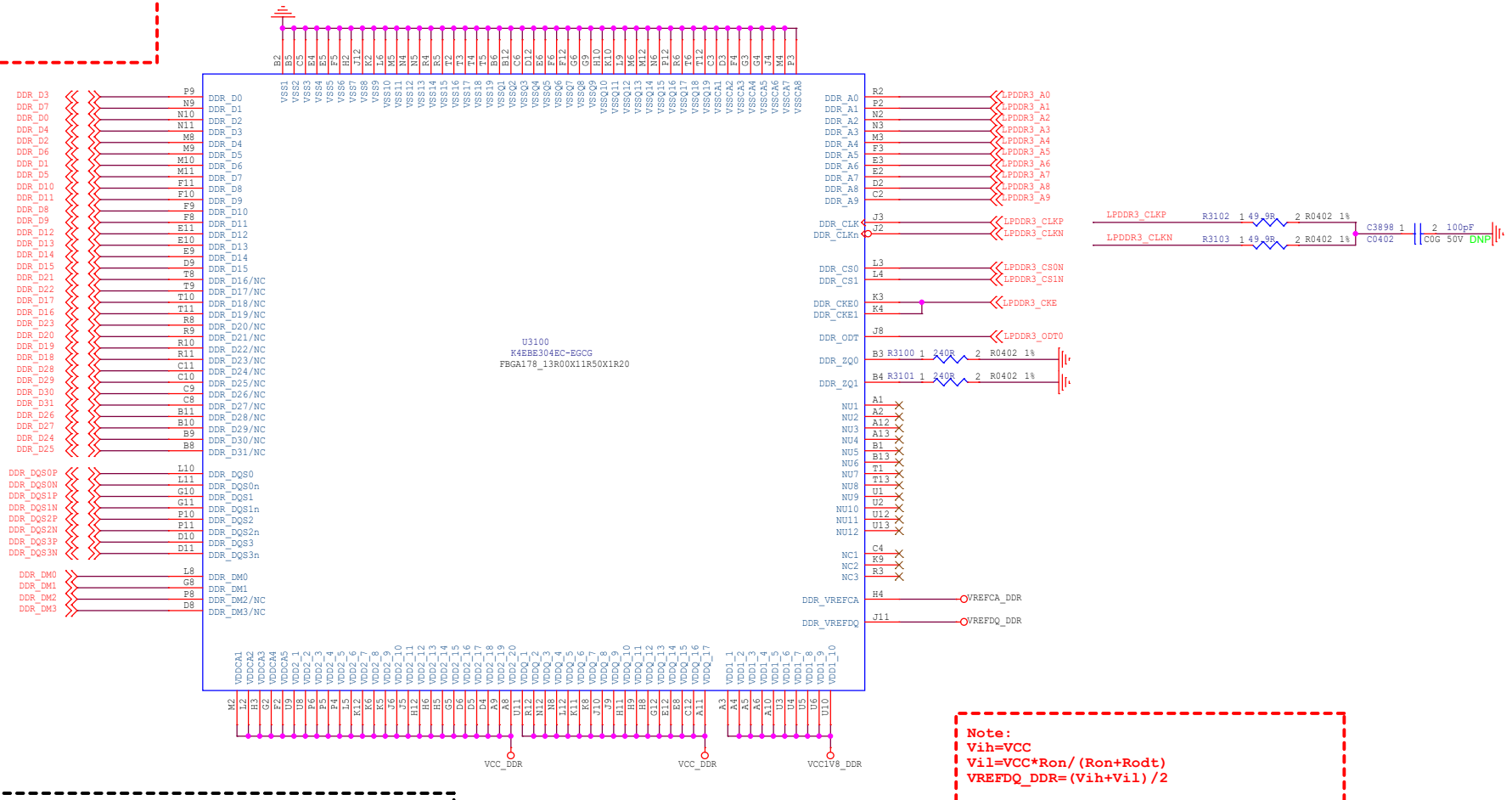


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	30.DRAM_DDR3_96P_2X16bit				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	22 of 41

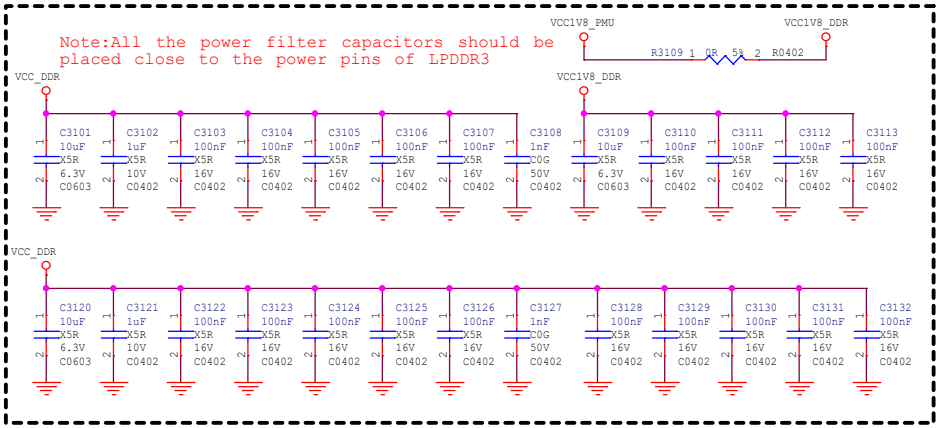
LPDDR3 1x32bit

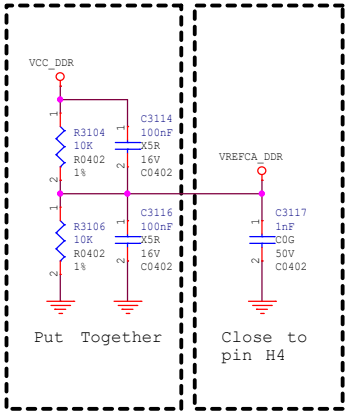
NOTE:
The sequence of DQ shall be done according to the template and shall not be adjusted or changed

Refer to the latest AVL for parts selection.



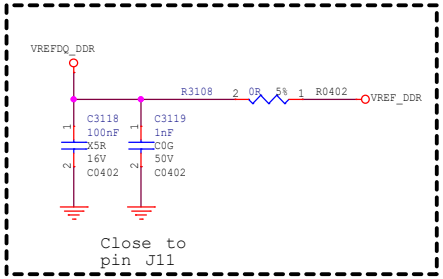
Note:All the power filter capacitors should be placed close to the power pins of LPDDR3





Note:
Vih=VCC
Vil=VCC*Ron/(Ron+Rodt)
VREFDQ_DDR=(Vih+Vil)/2

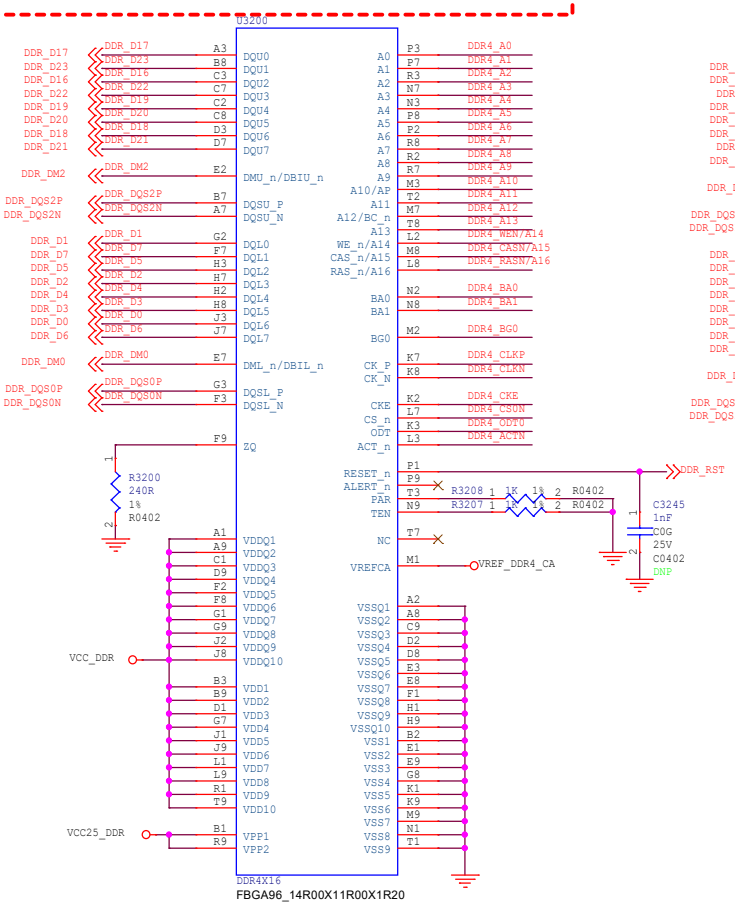
eg:VCC=1.2V,Ron=34ohm,Rodt=240ohm
so,Vih=1.2V,Vil=0.149V,VREFDQ_DDR=0.674V

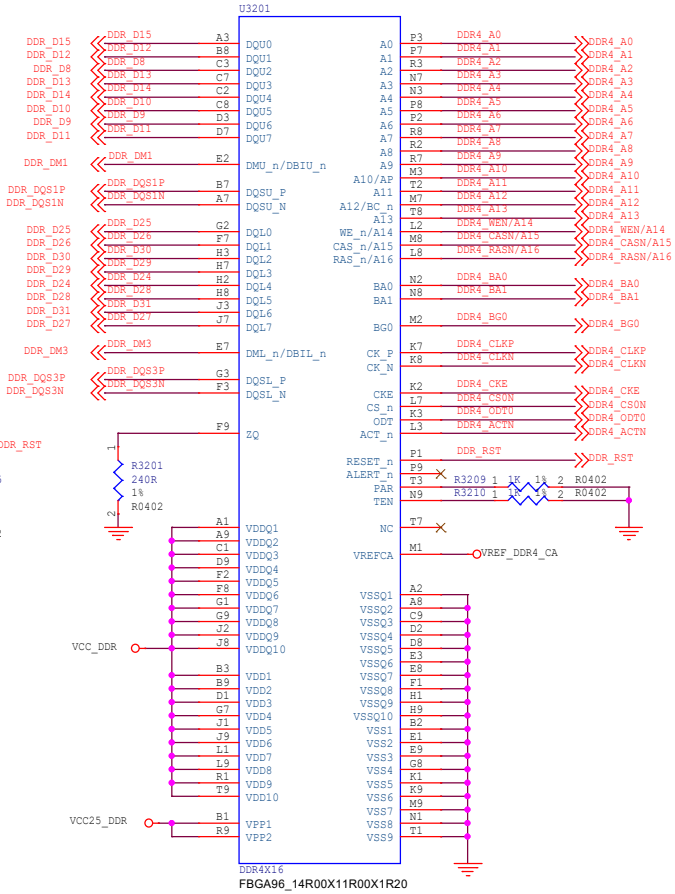


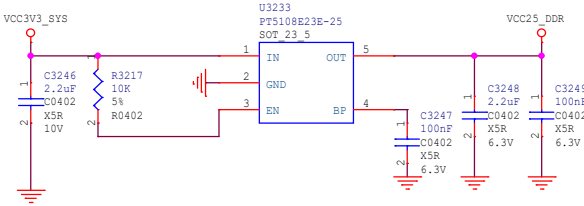
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	31. DRAM_LPDDR3_32 bit				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	23 of 41

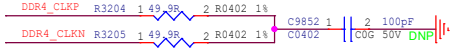
DDR4 2x16bit

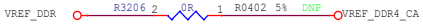
NOTE:
The sequence of DQ shall be done according to the template and shall not be adjusted or changed
Refer to the latest AVL for parts selection.

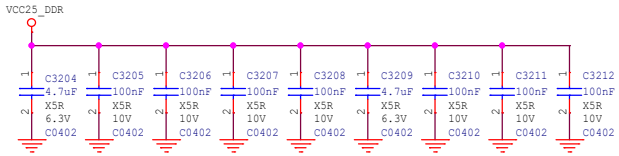


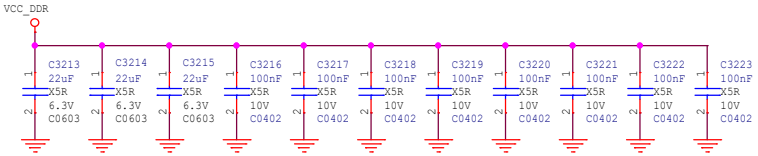


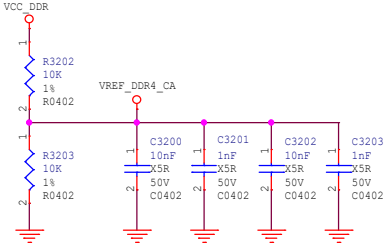


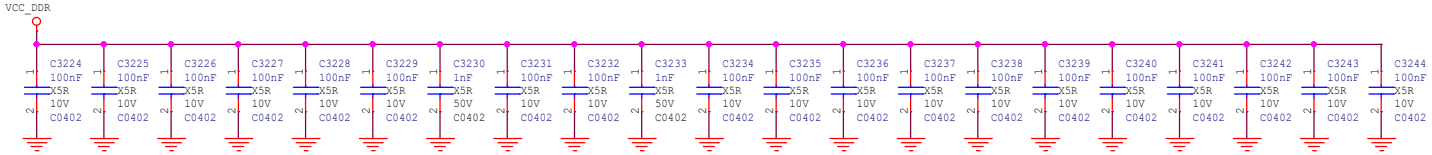








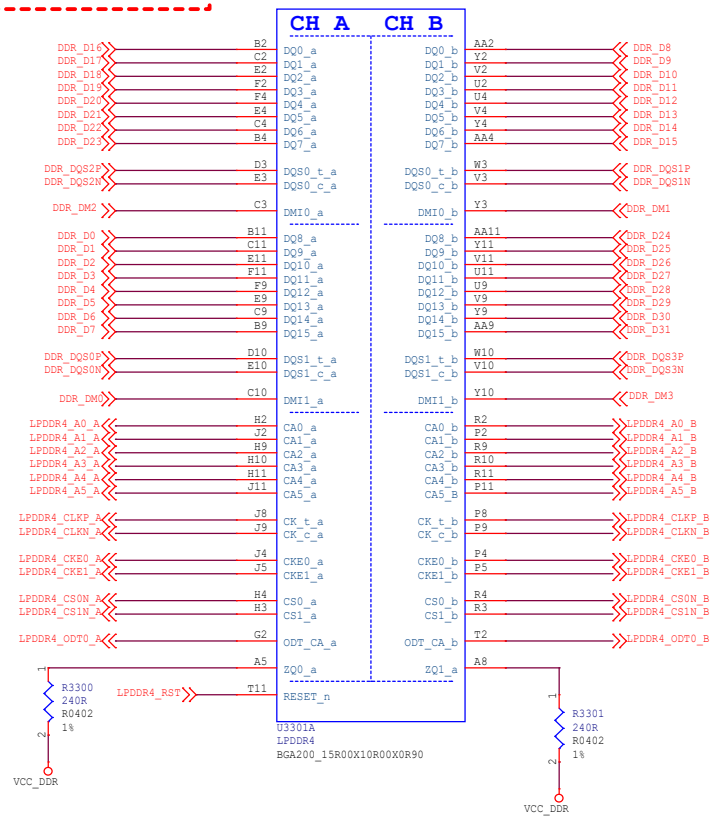


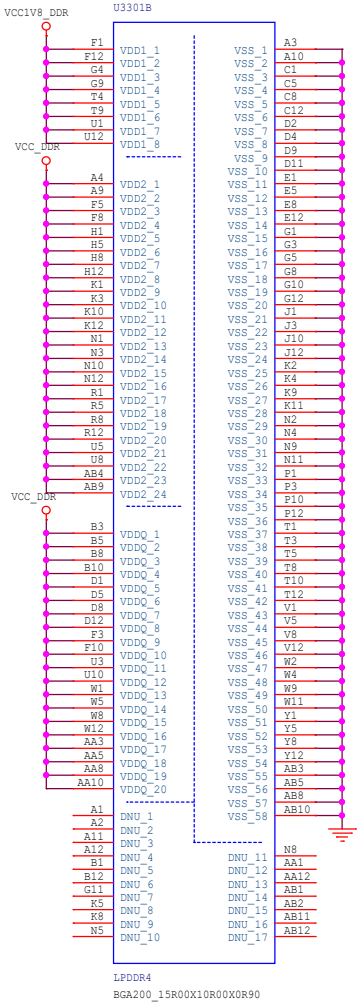


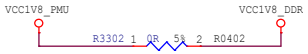
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	31. DRAM_LPDDR3_32 bit				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	24 of 41

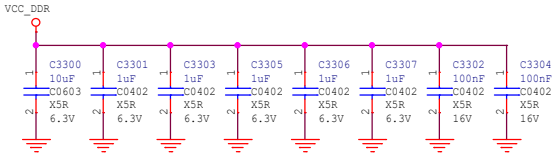
LPDDR4 1x32bit

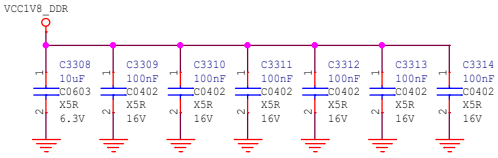
NOTE:
The sequence of DQ shall be done according to the template and shall not be adjusted or changed
Refer to the latest AVL for parts selection.

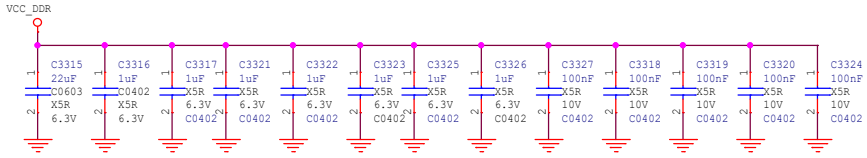








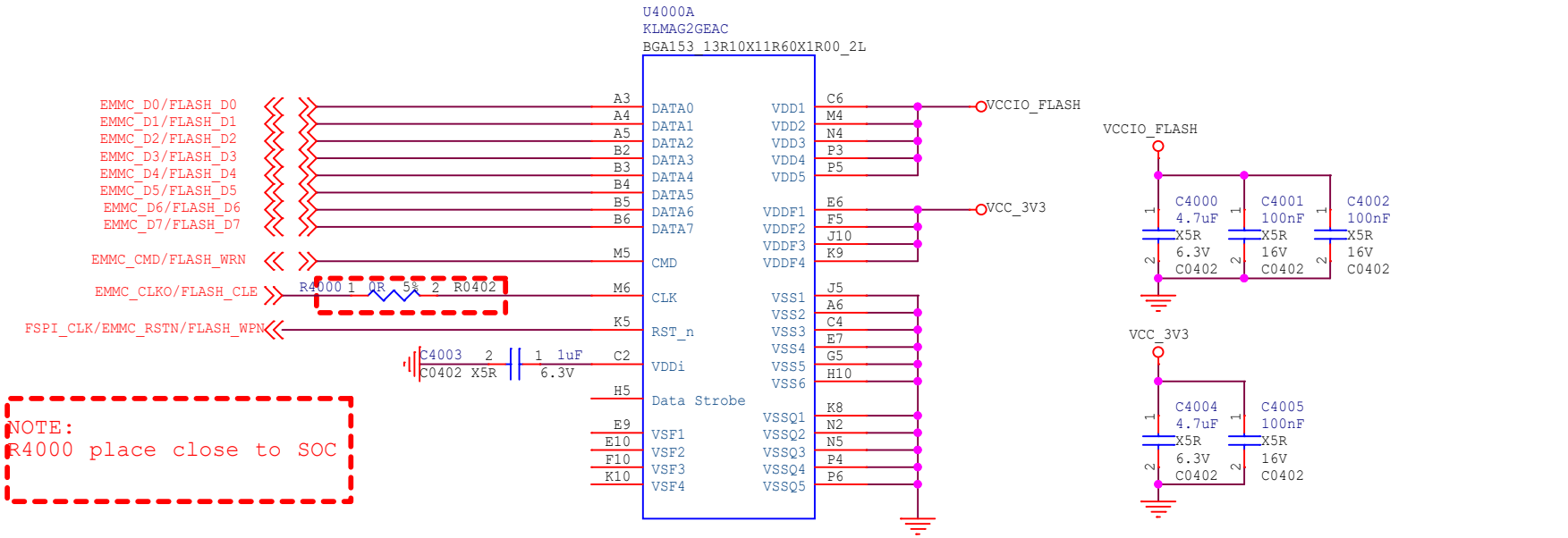




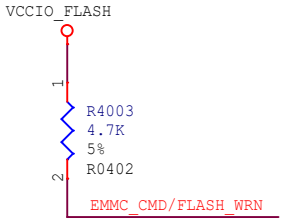
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	33.DRAM_LPDDR4_32 bit				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	25 of 41

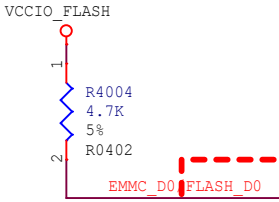
eMMC

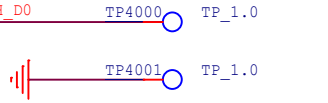
NOTE:
Refer to the latest AVL for parts selection.
NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.



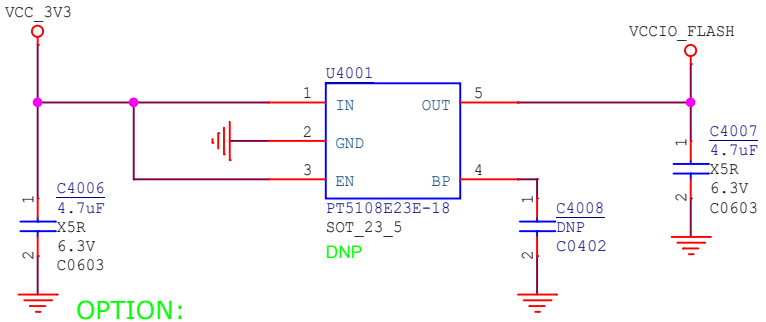
NOTE:
R4000 place close to SOC







NOTE:
Reserve testpoint for firmware update,
In the power on phase, if FLASH_D0= 0V,
the system will enter the maskROM mode

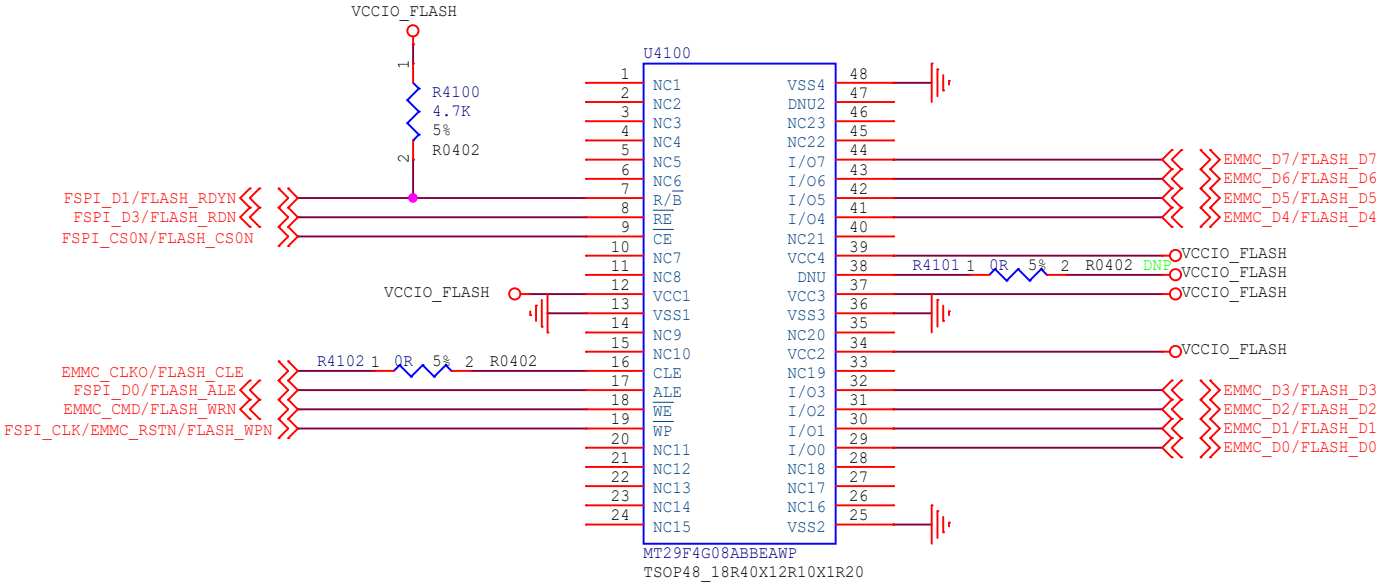


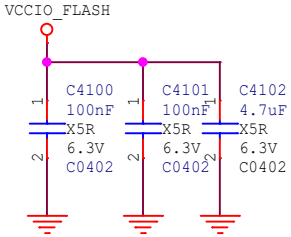
OPTION:
If EMMC peak current > 300mA,
please use LDO supply

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	40.Flash-eMMC Flash				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	26 of 41

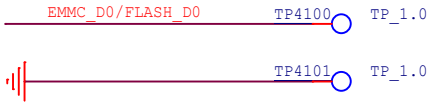
NAND FLASH

NOTE:
Refer to the latest AVL for parts selection.
Only support SLC NAND





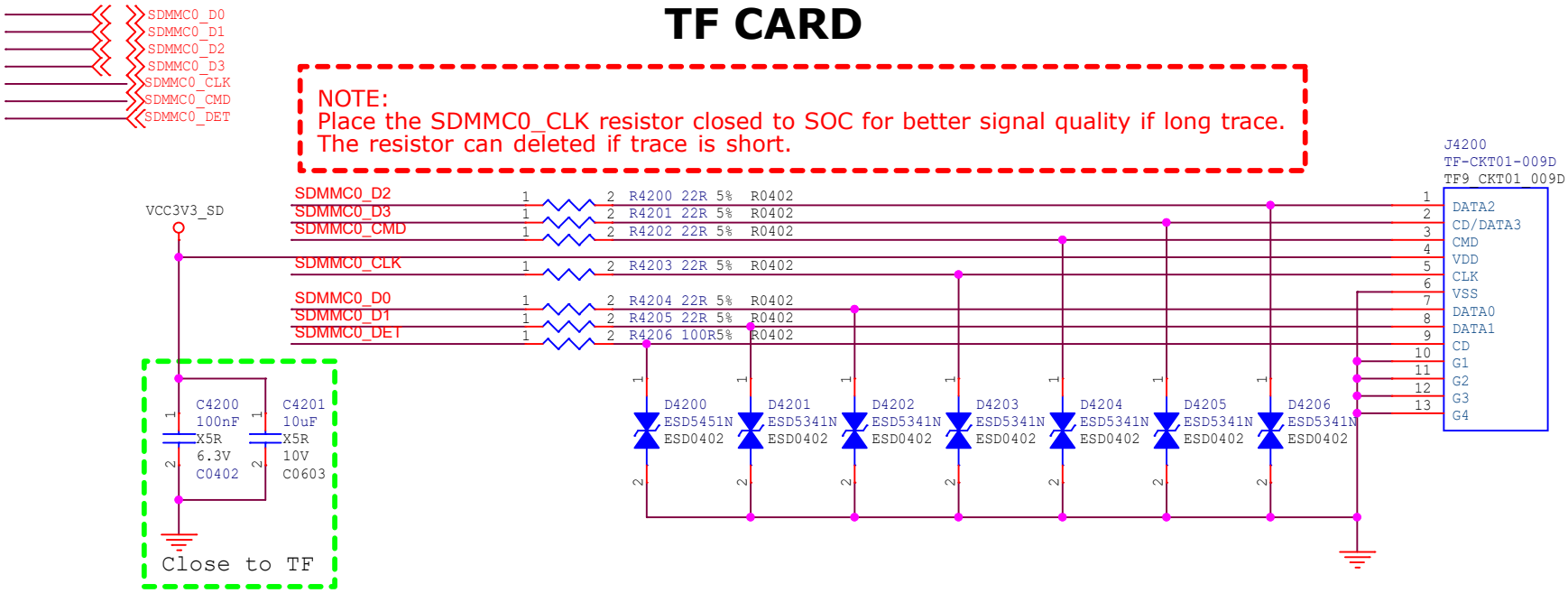
NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.



NOTE:
Reserve testpoint for firmware update,
In the power on phase, if FLASH_D0= 0V,
the system will enter the maskROM mode

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	41.Flash-Nand Flash				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	27 of 41

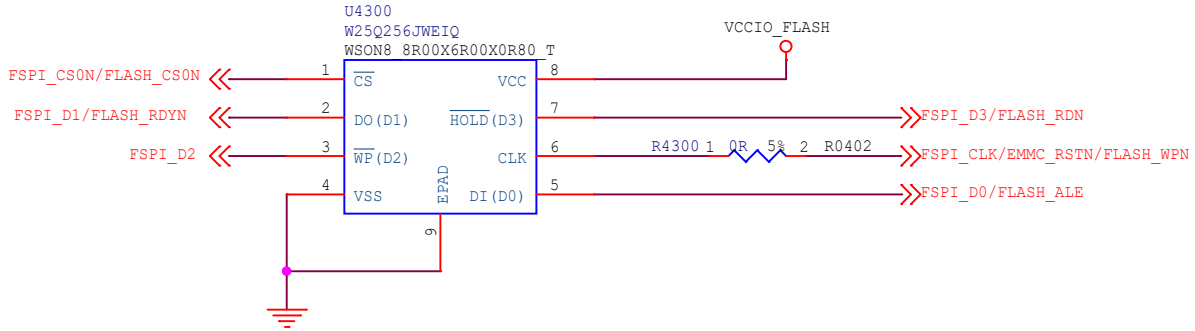
TF CARD

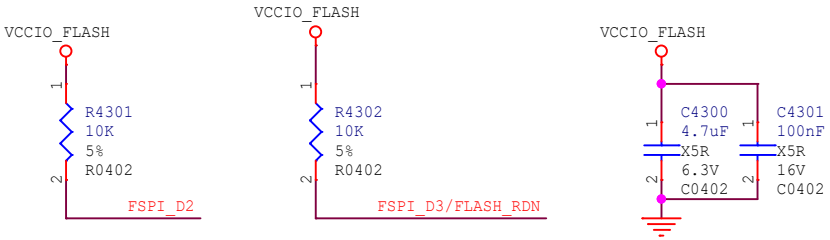


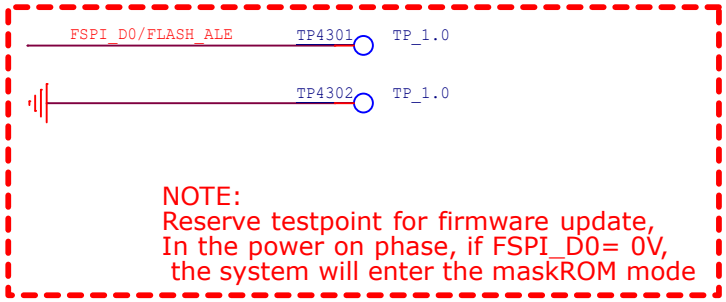
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	42.Flash-Micro-SD Card				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	28 of 41

SPI_Flash

NOTE:
Refer to the latest AVL for parts selection.



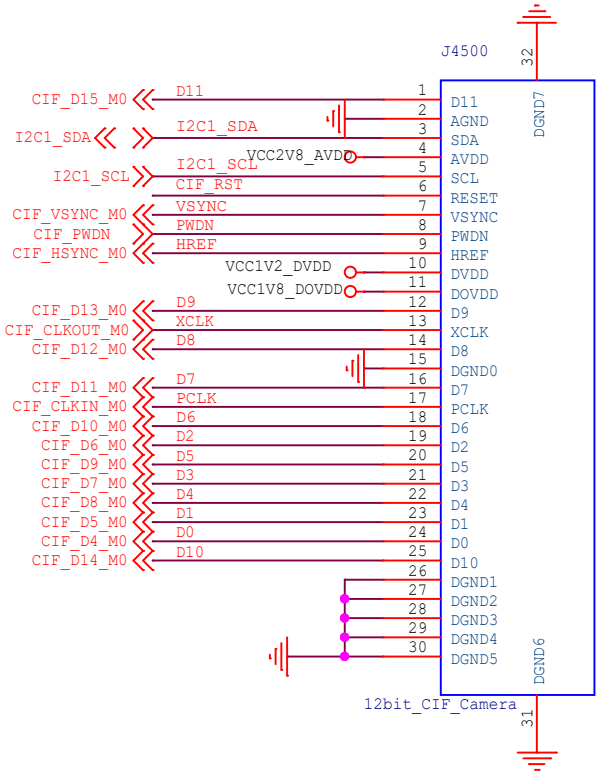




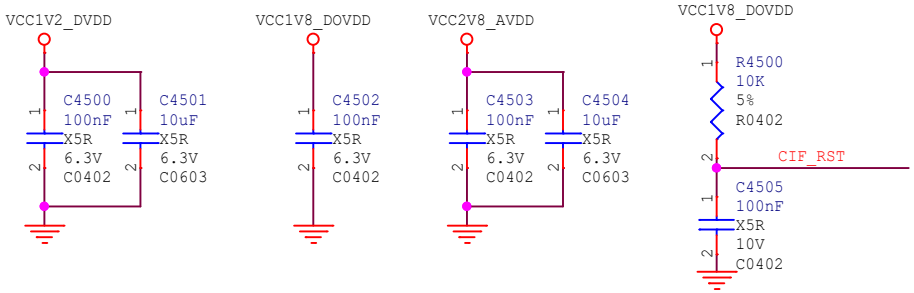
NOTE:
Reserve testpoint for firmware update,
In the power on phase, if FSPI_D0= 0V,
the system will enter the maskROM mode

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	43.Flash-SPI Flash				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	29 of 41

CIF Camera Interface

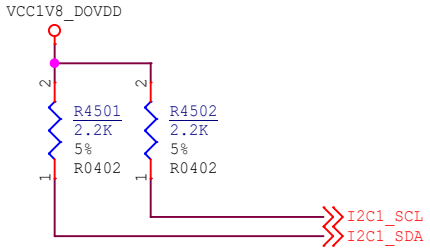


Correspondence CIF data and BT1120/12bit/10bit/8bit CIF				
16bit CIF data	BT1120	12bit CIF camera	10bit CIF camera	8bit CIF camera
CIF_D0	BT1120_D0			
CIF_D1	BT1120_D1			
CIF_D2	BT1120_D2			
CIF_D3	BT1120_D3			
CIF_D4	BT1120_D4	D0		
CIF_D5	BT1120_D5	D1		
CIF_D6	BT1120_D6	D2	D0	
CIF_D7	BT1120_D7	D3	D1	
CIF_D8	BT1120_D8	D4	D2	D0
CIF_D9	BT1120_D9	D5	D3	D1
CIF_D10	BT1120_D10	D6	D4	D2
CIF_D11	BT1120_D11	D7	D5	D3
CIF_D12	BT1120_D12	D8	D6	D4
CIF_D13	BT1120_D13	D9	D7	D5
CIF_D14	BT1120_D14	D10	D8	D6
CIF_D15	BT1120_D15	D11	D9	D7



NOTE:
According to the current of the actual camera module, evaluate whether the current output by LDO can meet the requirement of two cameras using at the same time. If not, please add LDO to supply power

NOTE:
There is also a group of pull-up for I2C1 on page 47. Select one group.

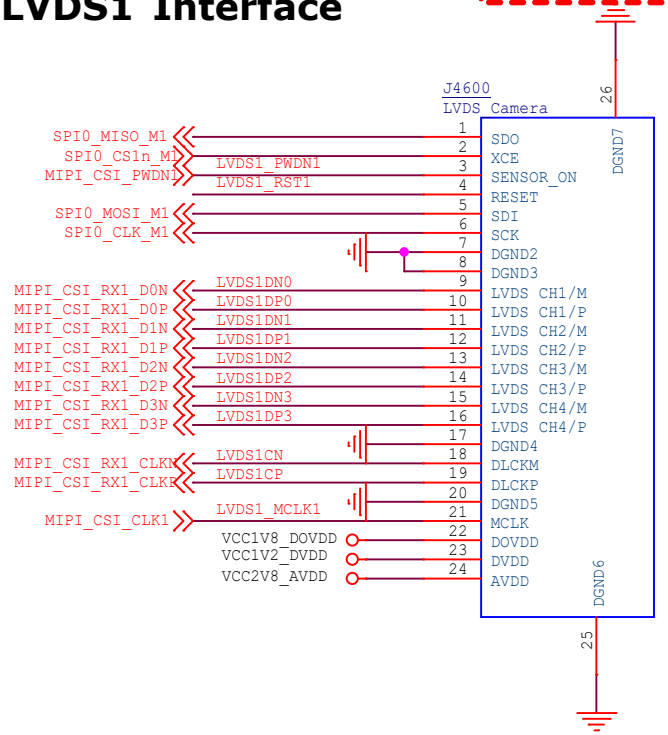


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics			
Project:	RV1126_RV1109 IPC REF			
File:	45.VI-Camera_CIF			
Date:	Tuesday, April 14, 2020		Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by: <Checker>	Sheet:	30 of 41

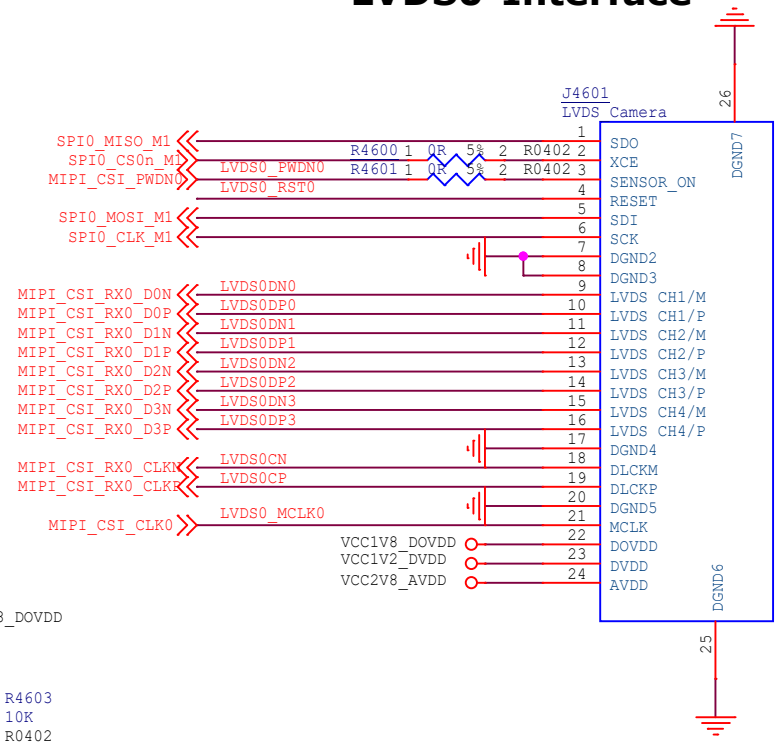
OPTION: LVDS Interface
LVDS interface and mipicsi interface share pins,
only one of them can be selected at a time

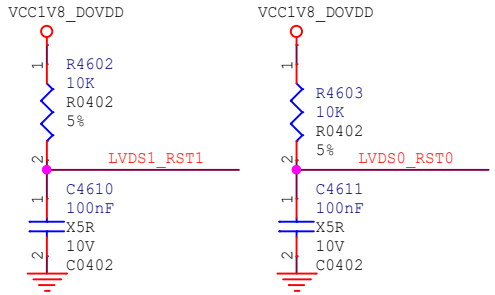
NOTE:
According to the current of the actual camera module,
evaluate whether the current output by LDO can meet
the requirement of two cameras using at the same time.
If not, please add LDO to supply power

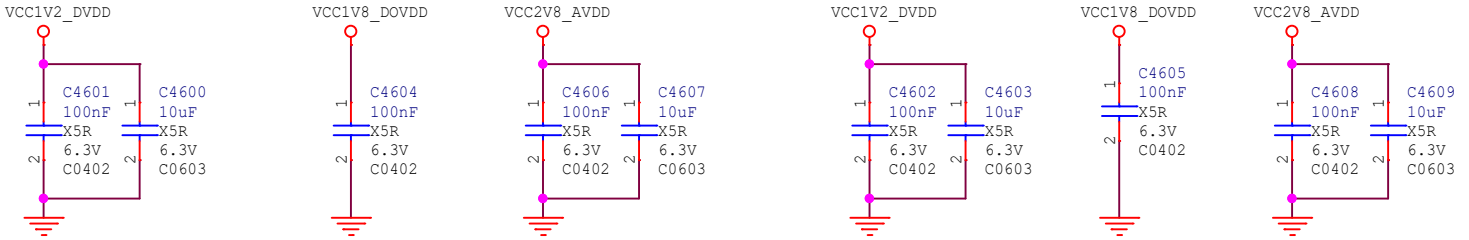
LVDS1 Interface



LVDS0 Interface







Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	46.LVDS/Sub-LVDS Camera(option)				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	31 of 41

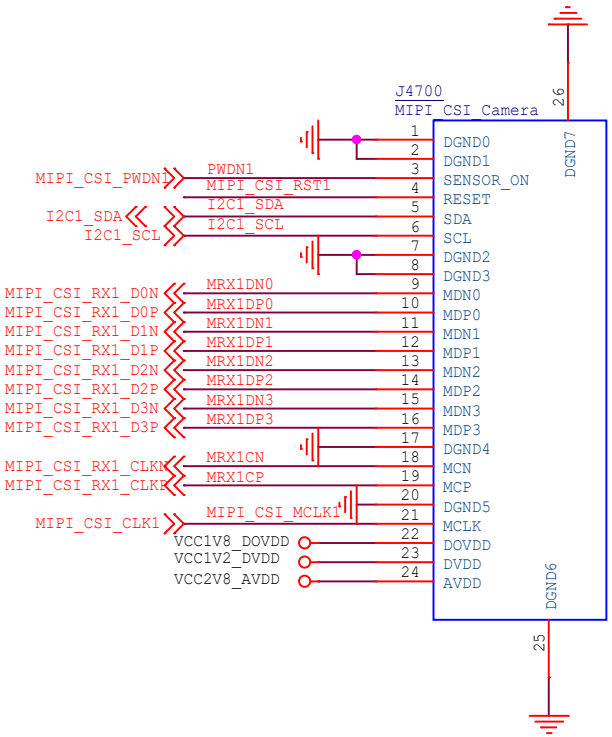
DEFAULT: MIPI_CSI Interface
LVDS interface and mipicsi interface share pins,
only one of them can be selected at a time.

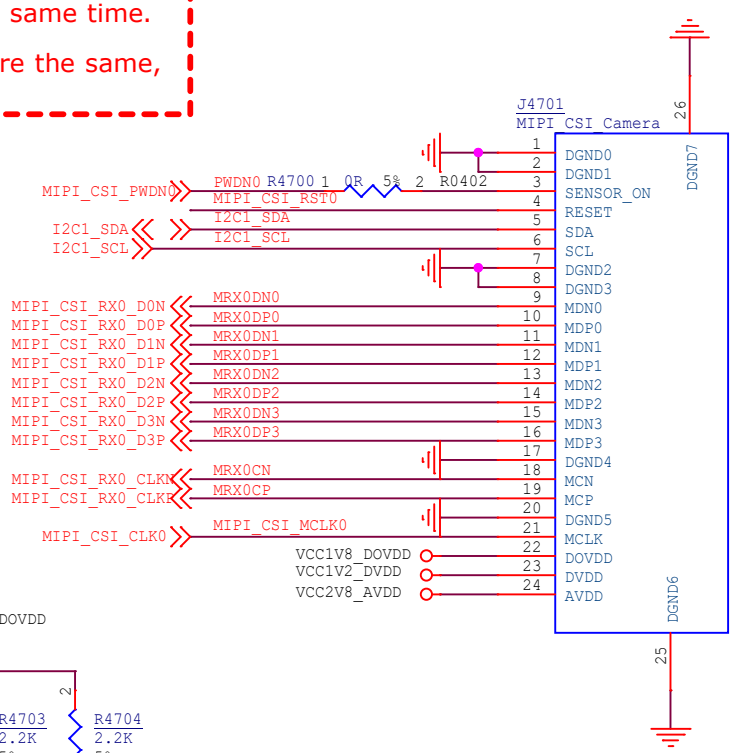
MIPI-CSI_RX1 Interface

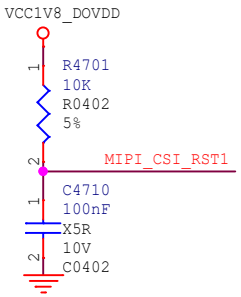
Recommend camera module: OS04A10

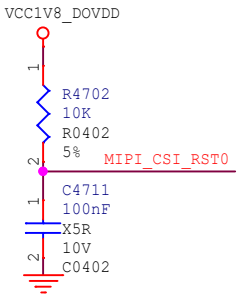
NOTE:
1. According to the current of the actual camera module, evaluate whether the current output by LDO can meet the requirement of two cameras using at the same time.
2.If not, please add LDO to supply power.
3. If the I2C addresses of the two cameras are the same, use another set of I2C.

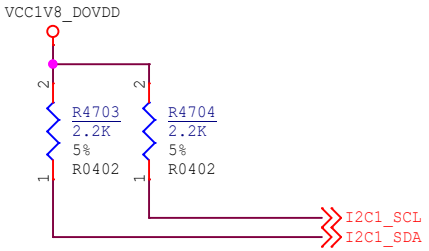
MIPI-CSI_RX0 Interface



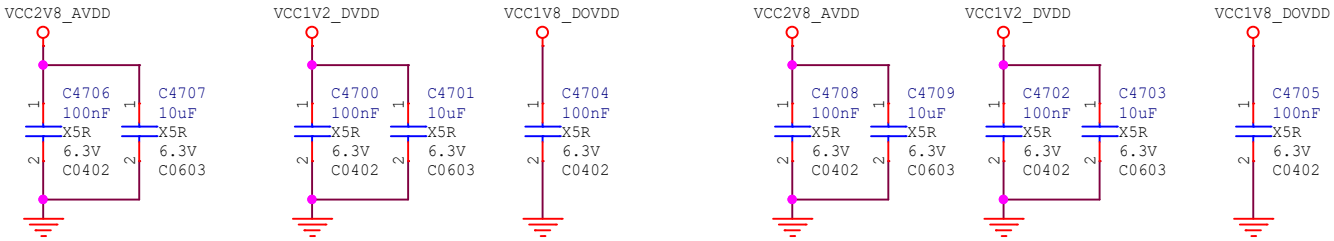








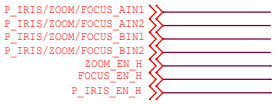
NOTE:
There is also a group of pull-up for I2C1 on page 45.
Select one group.



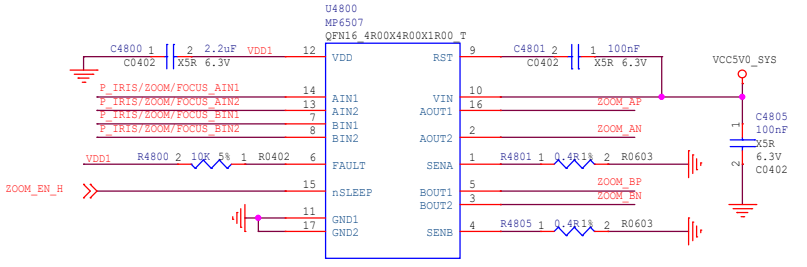
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	47.VI-Camera_MIPI-CSI				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	32 of 41

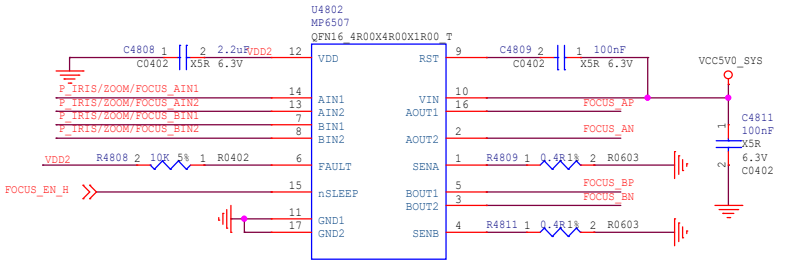
Iris Zoom Focus driver

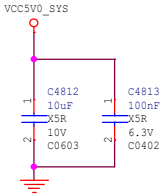
NOTE:
For reference only
Please select the appropriate driver IC
according to the actual lens specifications.

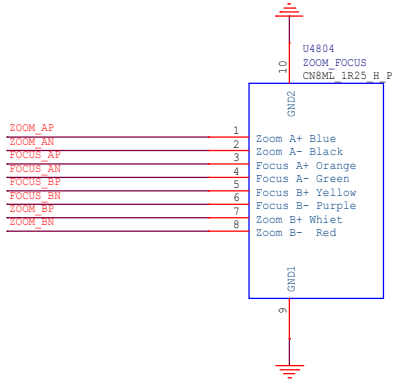


Zoom Focus driver

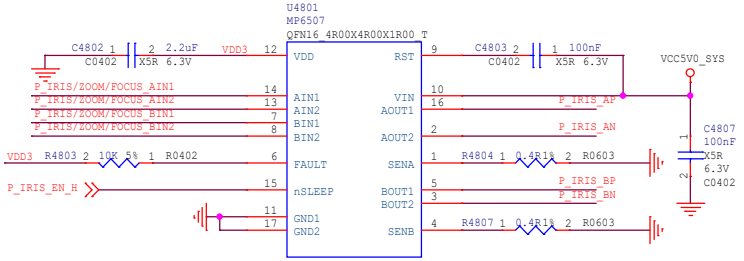


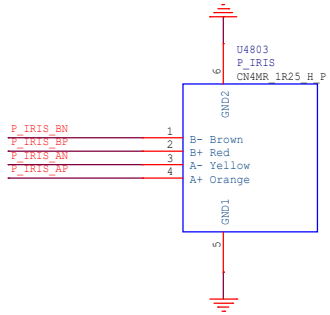






P-Iris driver

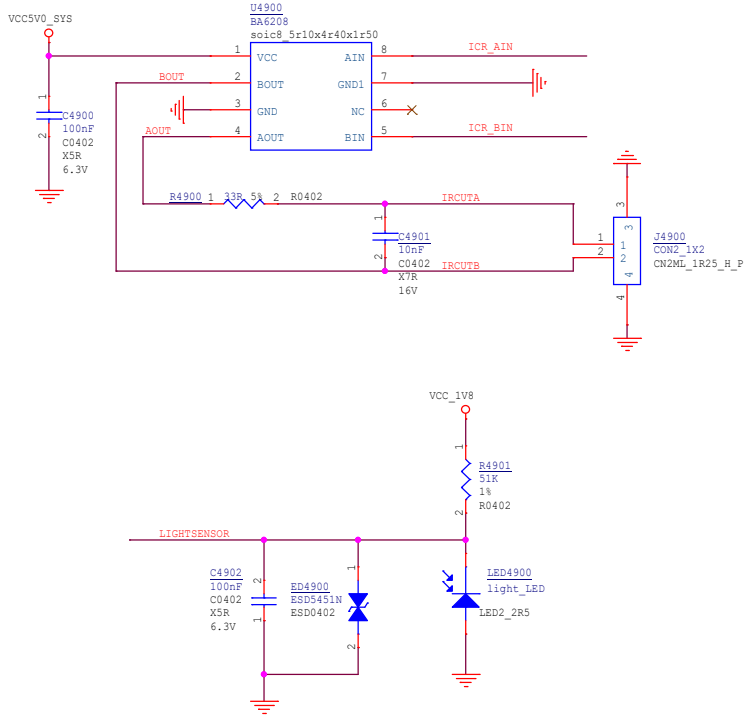




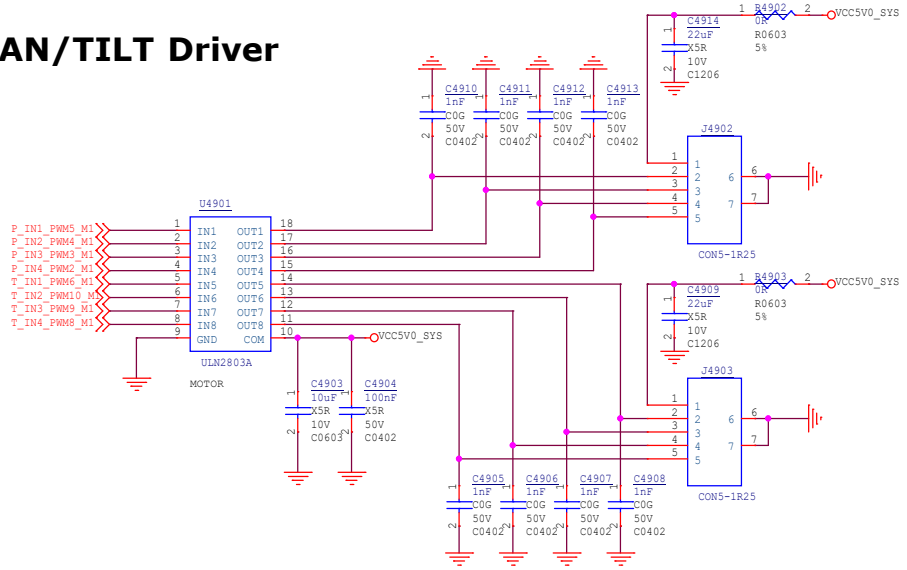
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	48.P-Iris Zoom Focus driver				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	33 of 41

P_IN1_PWM5_M1
P_IN2_PWM4_M1
P_IN3_PWM3_M1
P_IN4_PWM2_M1
T_IN1_PWM6_M1
T_IN2_PWM10_M1
T_IN3_PWM9_M1
T_IN4_PWM8_M1
ICR_AIN
ICR_BIN
LIGHTSENSOR

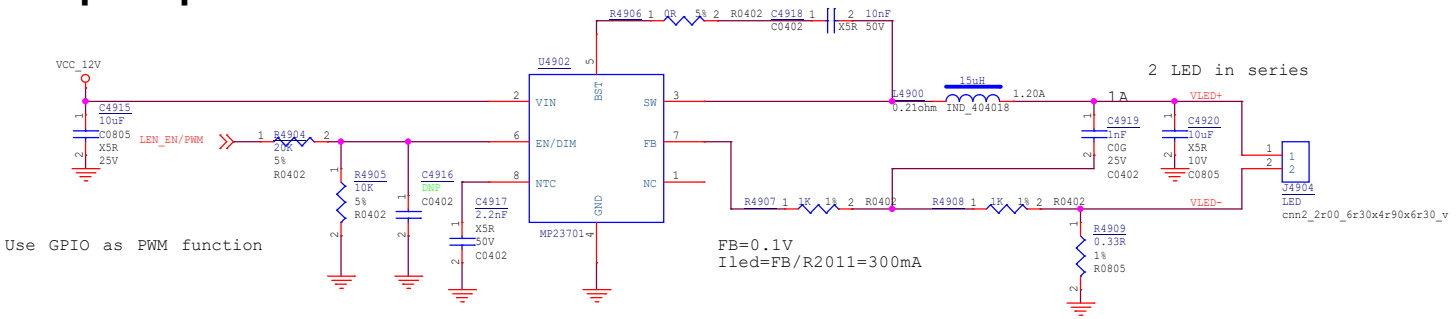
IR Cut Driver



PAN/TILT Driver

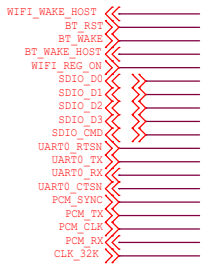


Warm up lamp drive



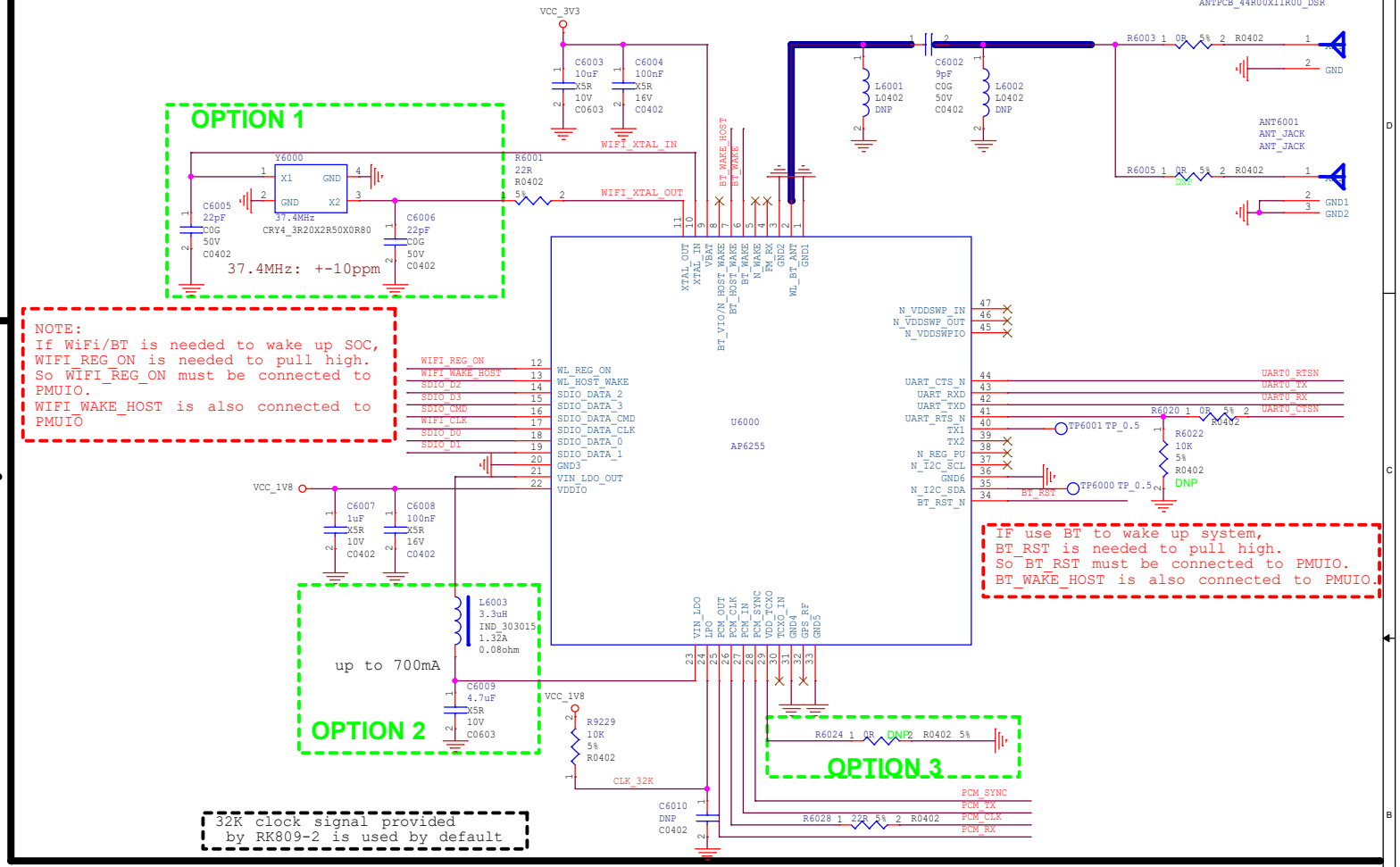
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	49.IRC/Motor Driver				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	34 of 41

WIFI/BT Module



WIFI module		
Pin	AP6255	UWE5622
6	BT_WAKE	CHIP EN
7	BT_HOST_WAKE	AP_INT
12	WL_REG_ON	RST_N
13	WL_HOST_WAKE	SD_INT

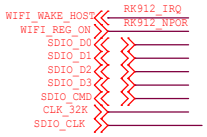
Note:
Yes: option circuit be mounted
No: option circuit not be mounted



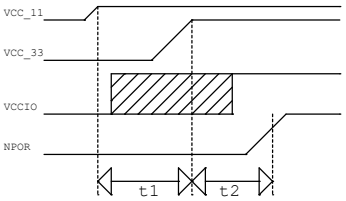
OPTION	WIFI				BT	Crystals	VCCIO_SDIO	OPTION1	OPTION2	OPTION3
	a	b/g/n	ac	5GHz						
AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71-3.63V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.63V	Yes	Yes	No
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.62-3.63V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0
RTL8189FTV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.63V	No	No	No
QCA9377 Module 8223A-SR	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No
UWE5622	Yes	Yes	Yes	Yes	5.0	Module Integrated	1.62-1.98V	No	No	No

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	60.WIFI/BT-SDIO_1T1R+UART				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	35 of 41

WIFI RK912



Power Sequence



t1>=1ms, t2>=1ms

Power Consumption

State	VCCIO	VCC_33	VCC_11
Sleep	0.1mA	0.1mA	0.1mA
PowerSave(DTIM=1)	0.1mA	2.6mA	1.3mA
TX(11b 11M)	0.8mA	192mA	15.6mA
TX(11g 54M)	0.8mA	169.5mA	16.3mA
TX(11n 65M)	0.8mA	168.6mA	16.4mA
RX(11n 65M)	0.8mA	42.9mA	21.3mA

Note: All data test under continue mode
VCCIO test under 3.3V

RF Routing

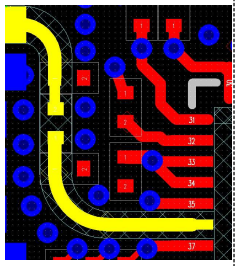
Short and smooth routing with 50 ohm

No layer change, top layer best

Place GND via along RF trace

Integral reference GND for RF trace

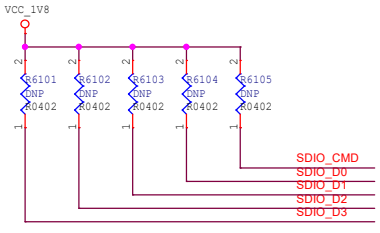
Excavate L2 on RFIO pin and antenna pad



Other Routing Requirement

SDIO CLK trace must be surounded by GND
Do not split L2 GND layer
Epad connet to GND by via alone, minimum 16 via
Pin 4/7/14/18 connet GND by seperate via best

Optional



Note: Reserve pull-high resistors for SDIO data pins base on platform

Crystal Requirement

参数	规范		单位	描述
	最小	最大		
频率	40.000000		MHz	
频率偏差	+/-10		ppm	Frequency tolerance
工作温度	-20	80	℃	根据实际产品温度需求选择晶体型号
ESR	/	60	Ohm	

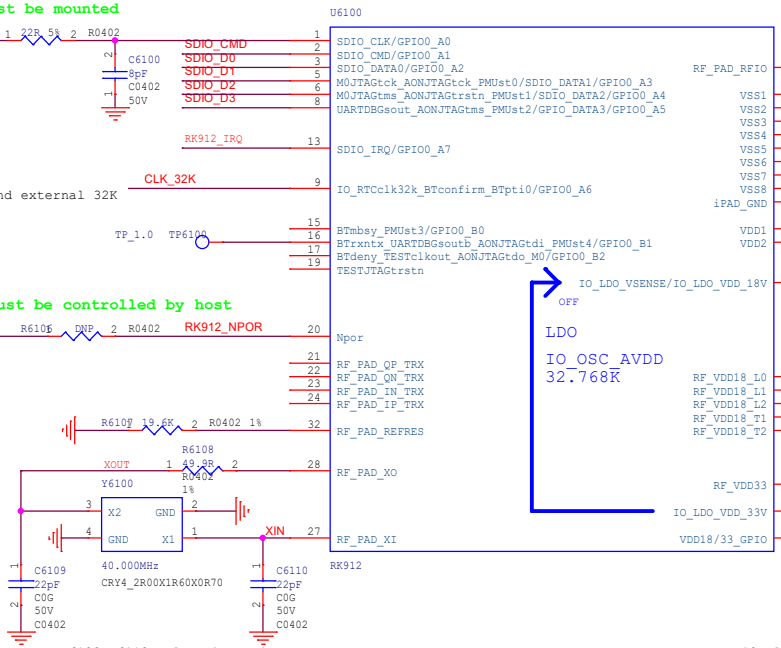
Crystal Routing

Close to RK912
Trace surround by GND
Other signal trace prohibited under crystal

C17 must be mounted

NPOR must be controlled by host

Recommend external 32K

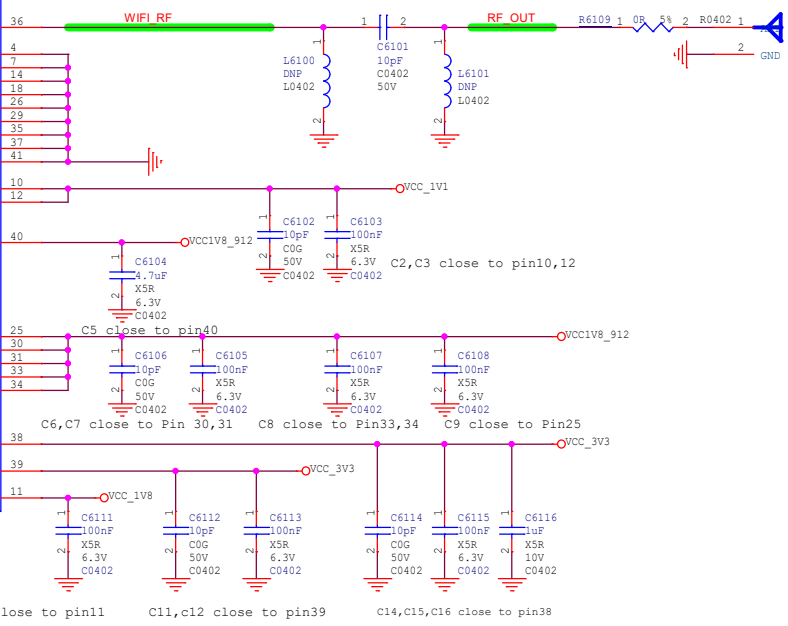


Note:C6109,C6110 value choose base on test

Reserve matching component location for antenna

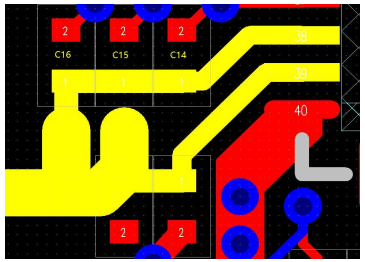
ANT6100
ANT4411DR
ANTPCB_44R00X11R00_DSR

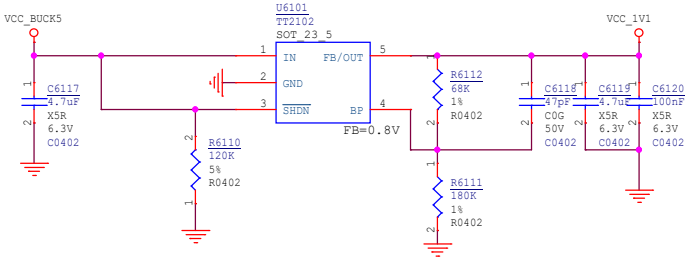
50 Ohm RF trace



Power Routing

Power trace follow star routing
Samll value capacitor closer to pin
10pF closest to pin, then 100nF,
then 1uF





C14,C15,C16 close to pin38

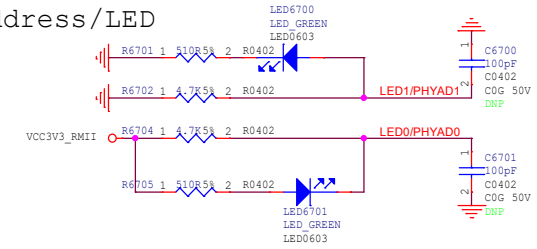
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	60.WIFI/BT-SDIO_1T1R+UART				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	36 of 41

PHY

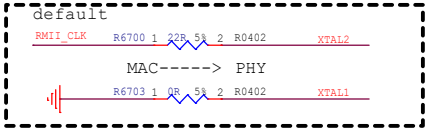
RMII_TXD0
RMII_TXD1
RMII_TXEN
RMII_RXDV
RMII_RXER
RMII_RXD0
RMII_RXD1
RMII_MDIO
RMII_MDC
RMII_CLK
EPHY_RSTn
EPHY_PMEB

POE12
POE36
POE45
POE78

PHY Address/LED



default



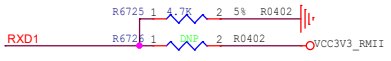
1. No crystal:
R6700,R6703,R6712, R6724 are sodered.
R6708,Y6700,C6702,C6703,R6717 are DNP.

2. With crystal
R6700,R6703,R6712, R6724 are DNP.
R6708,Y6700,C6702,C6703,R6717 are soldered.

MII/RMII Selection

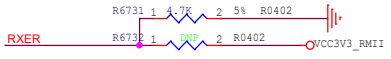
Pull High for RMII mode(default)

WOL/LED0 Selection



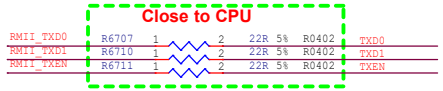
Pull Low for LED0 Mode(default)
Pull High for WOL Mode
WOL:Wake-on-LAN

UTP / Fiber Selection

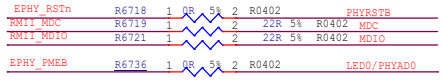


Pull Low for UTP Mode(default)
Pull High for Fiber Mode

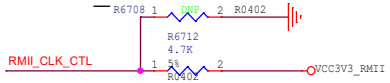
Close to CPU



Close to PHY



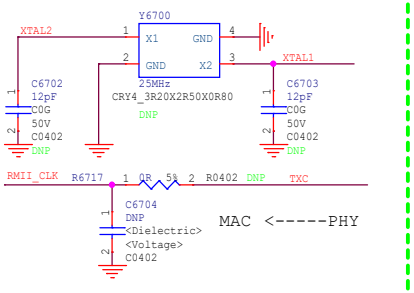
RMII REF_CLK direction



Pull Low for RMII REF_CLK Output mode
Pull High for RMII REF_CLK Input mode

This pin is pulled high by an external 4.7Kohm.
This pin is used for the interrupt function only when in the RMII mode.

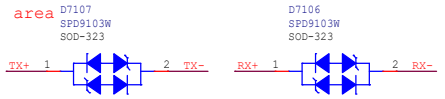
OPTION1



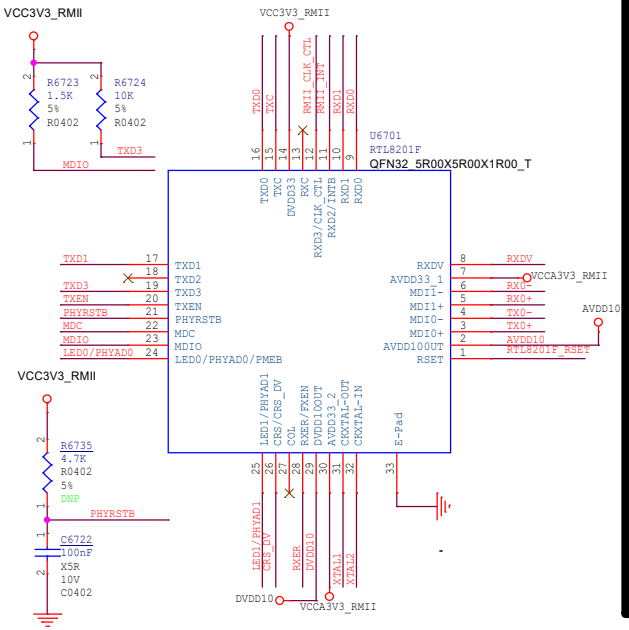
Low-tension area

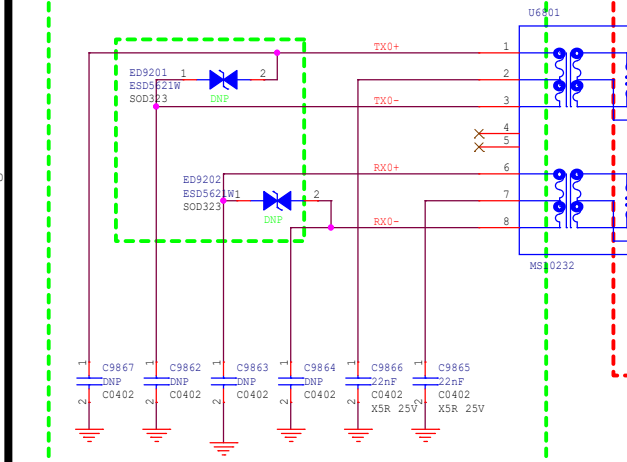
Differential mode lightning protection

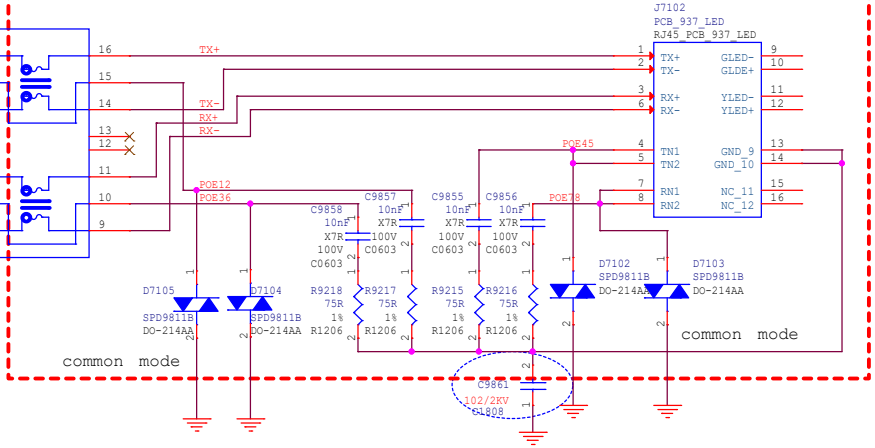
High-tension area

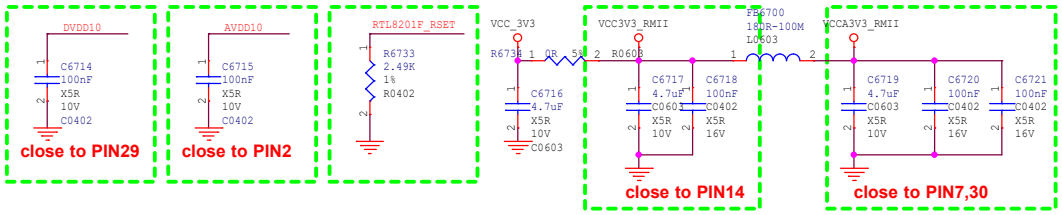


Differential mode









Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RV1126_RV1109 IPC REF		
File:	67.Ethernet-EPHY_RMII		
Date:	Tuesday, April 14, 2020	Rev:	V1.0
Designed by:		Sheet:	37 of 41

OPTION:GPHY

10/100/1000M RMII ETHERNET

Close to CPU

Close to PHY

OPTION1

Default

IO pad=1.8V

IO pad=3.3V OPTION1

LINK&ACT

J6800

HR911130C

RJ45_HR911130C

RGMII=3.3V IO,R6824=22R,R6827=DNP
RGMII=1.8V IO,R6824=100R,R6827=120R
If 125M come from RV1126/RV1109,
this part is not used.

CFG_EXT=1:Use the external power source for the IO pad.
CFG_LDO1=1, CFG_LDO0=0: IO pad 1.8V
CFG_LDO1=0,CFG_LDO0=0: IO pad 3.3V

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1'b1	2'b00
External 1.8V (default)	1'b1	2'b10
Internal 1.8V	1'b0	2'b10

VCCIO_PHY Voltage Config

PHY Address Config

PHY Address	PHYAD[2:0]
1 (default)	3'b001

Pull-up for additional 2ns delay to RXC for data latching

Pull-up for additional 2ns delay to TXC for data latching

Pull-up to disable PLL @ ALDPS mode

U6800
RTL8211F-CG
QFN40_5R00X5R00X0R90_T
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial

close to PIN11,40

close to PIN28

close to PIN30

close to PIN3,8,21,38

close to PIN29

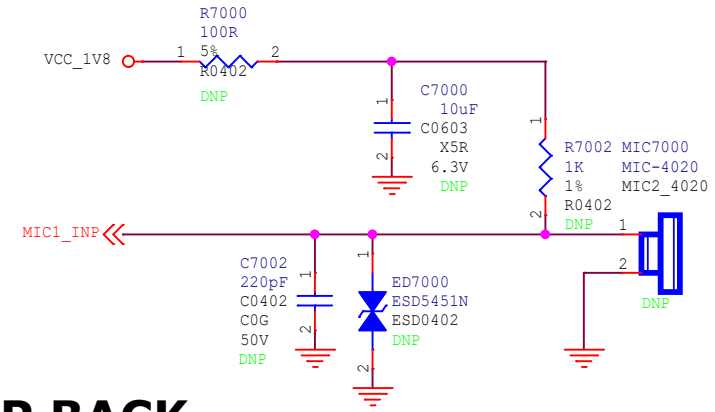
PHYRSTB is 3.3V IO

Project:	RV1126_RV1109 IPC REF
File:	68.Ethernet-GEPHY_RGMII(option)
Date:	Tuesday, April 14, 2020
Rev:	V1.0
Designed by:	Yanhong.Li
Reviewed by:	<Checker>
Sheet:	38 of 41

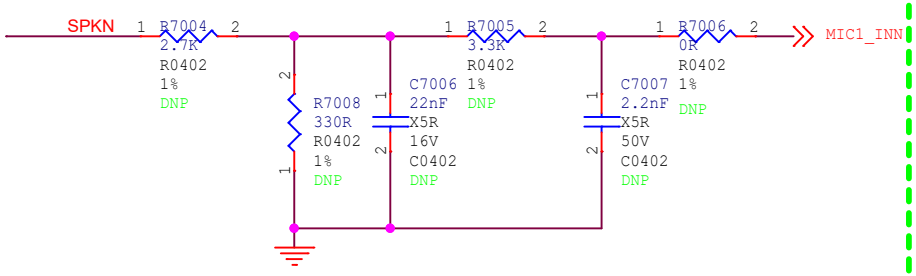
Fuzhou Rockchip Electronics

OPTION1: single end MIC, single loopback

MIC

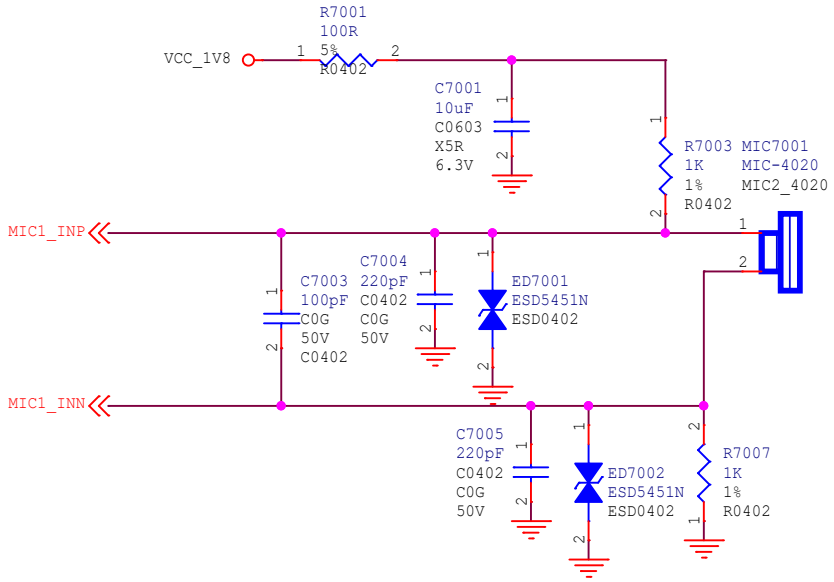


LOOP BACK

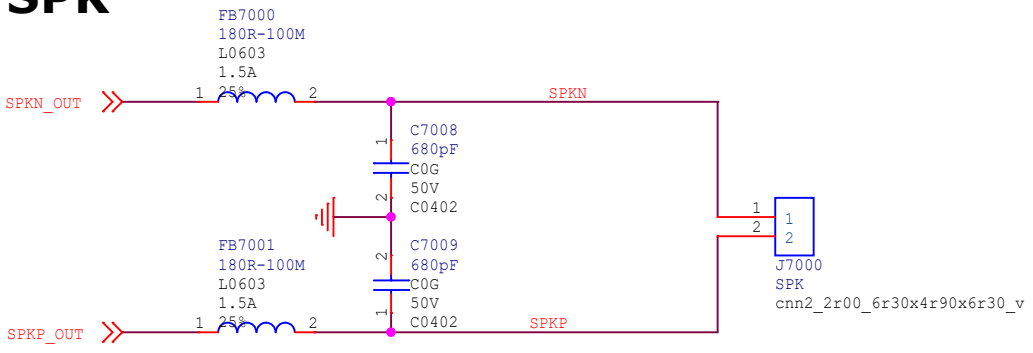


DEFAULT: no loopback, use differential MIC

differential MIC



SPK

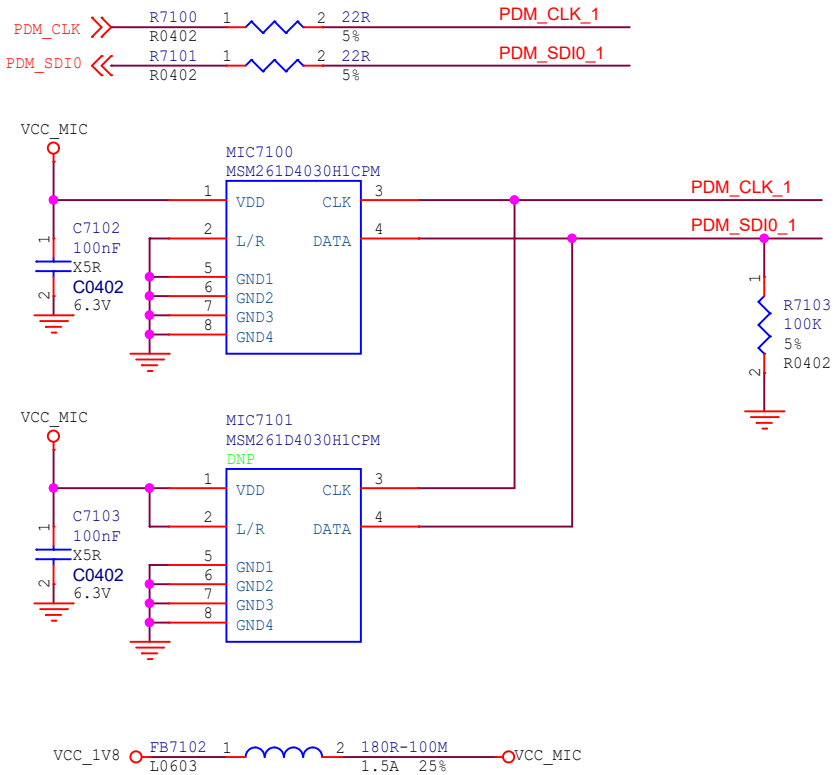


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	70.Audio Port1				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	39 of 41

OPTION: Audio Output2
If use audio output1,
please delete this page.

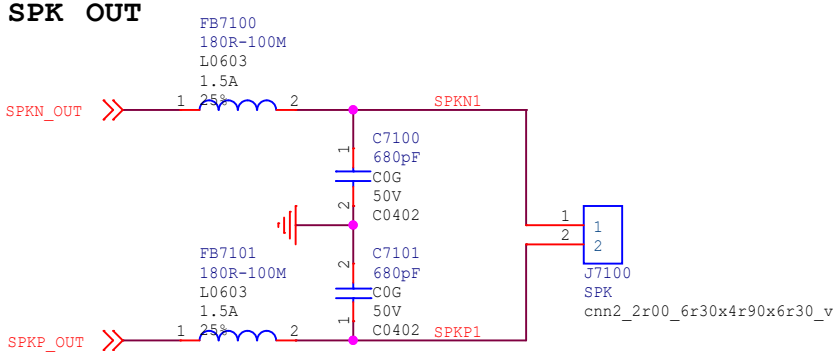
PDM MIC

2 Digital MEMS MIC or 1

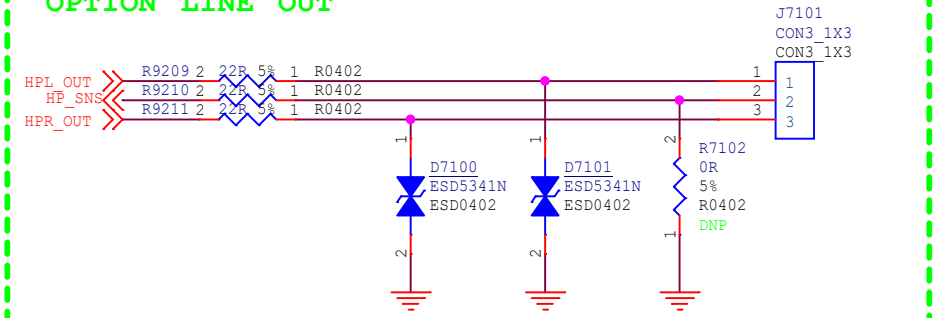


NOTE:
The SDI line should have a 100kohm PD resistor
to discharge the line during the time that all microphones
on the bus have tristated their outputs.

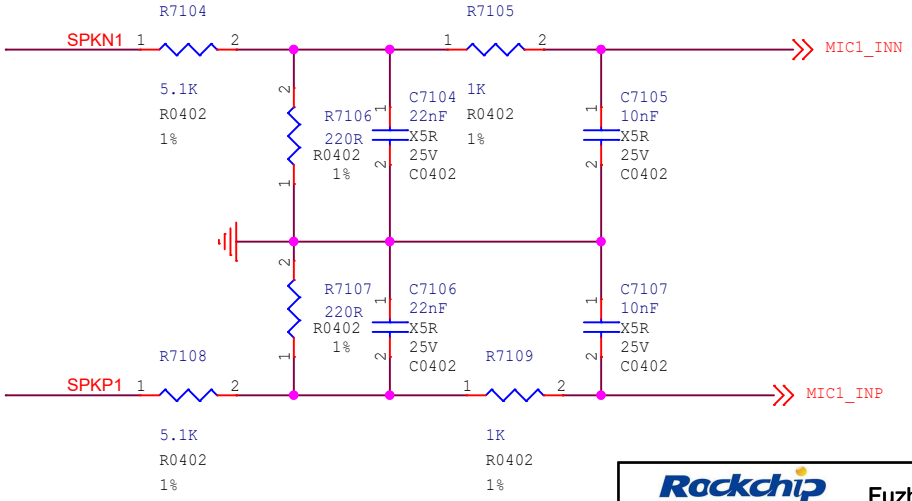
SPK OUT



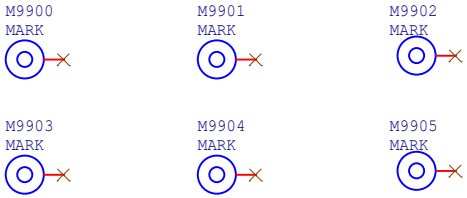
OPTION LINE OUT



Differential LOOP BACK



Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics					
Project:	RV1126_RV1109 IPC REF				
File:	71.Audio Port2(option)				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	40 of 41



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics				
Project:	RV1126_RV1109 IPC REF				
File:	99.MARK/HOLE				
Date:	Tuesday, April 14, 2020			Rev:	V1.0
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	41 of 41