RV1126_RV1109 Reference Design

RV1126_RV1109 Main difference		
	RV1126	RV1109
CPU	Quad A7	Dual A7
NPU	2.0Tops	1.2Tops
ISP	14M Pixel	5M Pixel

Reference Design Main Functions Introduction	
Power	RK809-2 + 1DCDC
RAM	EMMC/SLC NAND FLASH/SPI FLASH
ROM	DDR3L/DDR3/LPDDR3/LPDDR4
Interface	SDMMC/SDIO/MAC/LCD/CIF/MIPI_DSI/MIPI_CSI0/ MIPI_CSI1/LVDS0/LVDS1/I2S/PDM/USB/ADC

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	00.Cover Page				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	1 of 37

Table of Content

Index and Notes

Note

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Graphic Description

Note

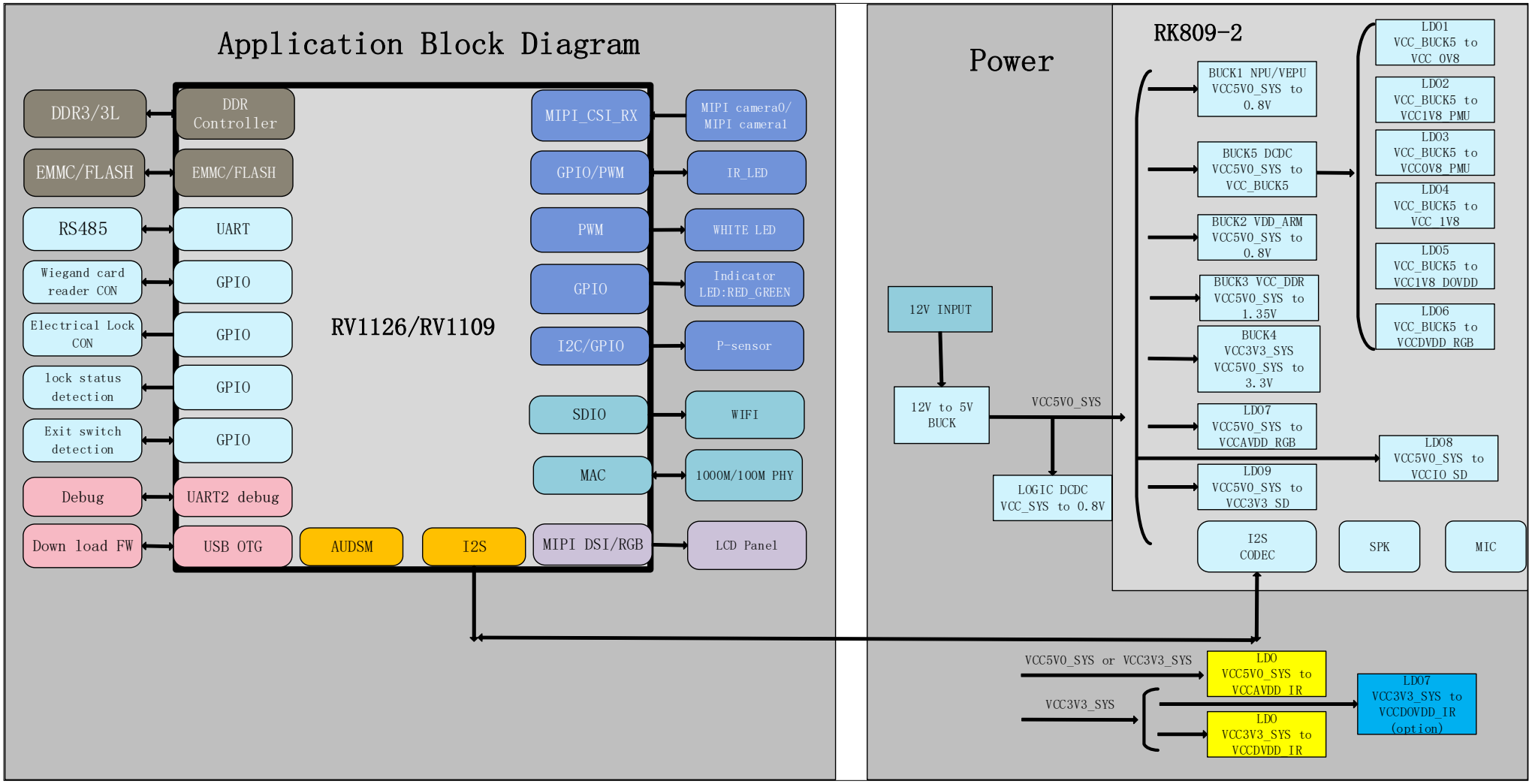
Option

Description

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	01.Index and Notes				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	2 of 37

Revision History

Version	Date	Author	Change Note	Approved
V1.0	2020.06.08	Liyh	Entrancegate REF Design V1.0 for RV1126_RV1109	
V1.1	2020.07.02	Liyh	Entrancegate REF Design V1.1 for RV1126_RV1109 Update: 1.P25 Add usb circuit for improving compability 2.P49 IR_LED Driver current is changed. 3.DDR3 template is changed.	
V1.2	2020.07.21	Liyh	Entrancegate REF Design V1.2 for RV1126_RV1109 Update: 1.Add 4ch dual LVDS camera module interface.	
V1.3	2020.08.20	Liyh	Entrancegate REF Design V1.3 for RV1126_RV1109 Update: 1.It's added a 2R resistor for VCCIO_VDD_1V8 Pin. 2.It's added TF card function. 3.It's added RTC IC funtion. 4.The LDO5,LDO6,LDO7 are used to supply for RGB caemra module. 5.It's added discrete power for IR camera module. 6. It's added the description for dual MIPI/LVDS camera module. It's very important. 7.It's added the description for the IR LED. It's very important. 8.It's added the GPIO control for the VCC3V3-LCDandVCC1V8_LCD. 9.It's added Wiegand OUT function. 10. It's delected dectector funtion.	



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Project:	RV1126_RV1109 GATE REF				
File:	03.Block Diagram				
Date:	Thursday, August 20, 2020			Rev:	V1.3
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RV1126_RV1109 Power-on Sequence

Power Name	PMIC Channel	Time (step=2ms)	Default voltage	Supply Limit	Default ON/OFF	Sleep ON/OFF	Peak Current
VCC_BUCK5	RK809-2 BUCK5	Slot: 1	2.2V	2.5A	ON	ON	
VCC0V8_PMU	RK809-2 LDO3	Slot: 2	0.8V	0.1A	ON	ON	
VCC_0V8	RK809-2 LDO1	Slot: 2	0.8V	0.4A	ON	OFF	
VDD_ARM	RK809-2 BUCK2	Slot: 2	0.8V	2.5A	ON	OFF	0.73A@1.8GHz
VDD_NPU	RK809-2 BUCK1	Slot: 2	0.8V	2.0A	ON	OFF	1.34A@934MHz
VDD_VEPU	RK809-2 BUCK1	Slot: 2	0.8V	2.0A	ON	OFF	0.77A@700MHz
VDD_LOGIC	Ext(SY8089AAC)	Slot 1+3ms	0.8V	2.5A	ON	ON	1.75A
VCC_DDR	RK809-2 BUCK3	Slot: 3	1.5V	1.5A	ON	ON	
VCC1V8_PMU	RK809-2 LDO2	Slot: 3	1.8V	0.4A	ON	ON	
VCC_1V8	RK809-2 LDO4	Slot: 3	1.8V	0.4A	ON	OFF	
VCC3V3_SYS	RK809-2 BUCK4	Slot: 4	3.3V	1.5A	ON	ON	
VCC_3V3	RK809-2 SWOUT2	Slot: 4	3.3V	1.5A	ON	OFF	
VCCIO_SD	RK809-2 LDO8	Slot: 4	3.3V	0.4A	ON	OFF	
VCC3V3_SD	RK809-2 LDO9	Slot: 4	3.3V	0.4A	ON	OFF	
VCC1V8_DOVDD	RK809-2 LDO5		1.8V	0.4A	OFF	OFF	
VCC_DVDD	RK809-2 LDO6		1.2V	0.4A	OFF	OFF	
VCC_AVDD	RK809-2 LDO7		2.8V	0.4A	OFF	OFF	
VCC5V0_HOST	RK809-2 SWOUT1		5V	2.1A	ON	OFF	
RESET	RK809-2 sent out Reset signal for soc(SLOT:5(10ms))						

NOTE:VCC_DVDD and VCC_AVDD according to camera sensor voltage

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Project:	RV1126_RV1109 GATE REF				
File:	04.Power Sequence				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	5 of 37

I2C MAP

Port	Pin Name	Domain	Bus Name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Slave Bus Capability	Note
I2C0	I2C0_SCL/GPIO0_B4_u I2C0_SDA/GPIO0_B5_u	PMUIO1	I2C0_SCL_PMIC I2C0_SDA_PMIC	VCC3V3_SYS	RK809-2	0x20		PMIC
I2C1	I2C1_SCL/UART4_CTSN_M2/GPIO1_D3_u I2C1_SDA/UART4_RTSN_M2/GPIO1_D2_u	VCCIO1	I2C1_SCL I2C1_SDA	VCC1V8_DOVDD	GC2053			MIPI camera
					IMX307			MIPI camera
I2C2	I2C2_SCL/PWM4_M0/GPIO0_C2_d I2C2_SDA/PWM5_M0/GPIO0_C3_d	PMUIO1	I2C2_SCL I2C2_SDA	VCC3V3_SYS				RTC IC
I2C5	LCDC_D1/RGMII_CRS_M1/CIF_D1_M1/UART4_CTSN_M1/I2C5_SCL_M0/GPIO2_A5_d LCDC_D7/I2S2_MCLK_M1/CIF_D3_M1/UART5_CTSN_M1/SPI0_CS1n_M2/PWM0_M1/I2C5_SDA_M0/GPIO2_B3_d	VCCIO5	I2C5_SCL_M0 I2C5_SDA_M0	VCC_3V3				P-Sensor TP

IO Power Domain Map

IO Domain	IO Group	Support of IO Voltage		Default Actual assigned IO Domain Voltage			Notes
		1.8V	3.3V	Net Name of Power Supply	Power Source	Voltage	
PMUIO0	***GPIO0A***	✓	✓	*VCC1V8_PMU*	*RK809-2_LDO2*	*1.8V*	
PMUIO1	***GPIO0BC***	✓	✓	*VCC3V3_SYS*	*RK809-2_BUCK4*	*3.3V*	
VCCIO1	***GPIO0CD/GPIO1A***	✓	✓	*VCCIO_FLASH*	*RK809-2_LDO4*	*1.8V*	*GPIO0_B3/FLASH_VOL_SEL pin defined as a set pin for VCCIO1 voltage domain after power-on reset.It is pull-up for 1.8V*
VCCIO2	***GPIO1AB***	✓	✓	*VCCIO_SD*	*RK809-2_LDO8*	*3.3V*	
VCCIO3	***GPIO1BCD***	✓	✓	*VCCIO3_VDD*	*RK809-2_LDO4*	*1.8V*	
VCCIO4	***GPIO1D/GPIO2A***	✓	✓	*VCCIO4_VDD*	*RK809-2_LDO4*	*1.8V*	
VCCIO5	***GPIO2ABCD/GPIO3A***	✓	✓	*VCCIO5_VDD*	*RK809-2_SWOUT2*	*3.3V*	
VCCIO6	***GPIO3ABC***	✓	✓	*VCCIO6_VDD*	*RK809-2_LDO4*	*1.8V*	
VCCIO7	***GPIO3D/GPIO4A***	✓	✓	*VCCIO7_VDD*	*RK809-2_LDO4*	*1.8V*	

Power

U1000N
RV1126/RV1109
BGA409 14R00X14R00X0R90

NPU/LOGIC/VEPU/ARM Power

NPU_VDD_1	H11	VDD_NPU_VEPU
NPU_VDD_2	H12	
NPU_VDD_3	J10	
NPU_VDD_4	J11	
NPU_VDD_5	K10	
NPU_VDD_6	K11	
LOGIC_VDD_1	H9	VDD_LOGIC
LOGIC_VDD_2	J9	
LOGIC_VDD_3	L10	
LOGIC_VDD_4	M11	
LOGIC_VDD_5	H13	
LOGIC_VDD_6	J13	
VEPU_VDD_1	L9	VDD_NPU_VEPU
VEPU_VDD_2	M9	
VEPU_VDD_3	N8	
VEPU_VDD_4	N9	
ARM_VDD_1	N12	VDD_ARM
ARM_VDD_2	P12	
ARM_VDD_3	P13	

Supply for VCCIO1~7 Power

VCCIO_VDD_1V8 — H14

VCCIO_VDD_1V8 — R1000 3.3R R0402 1% — VCC_1V8

C1000 1nF X5R 25V C0201

NOTE:
If any power domain of vccio 1 ~ vccio 7 is used,
then VCCIO_ VDD_ 1V8 must be connected to 1.8V power supply

VDD_NPU_VEPU

C1006 10uF X5R 4V C0402
C1005 1uF X5R 6.3V C0402
C1004 1uF X5R 6.3V C0402
C1003 100nF X5R 6.3V C0201
C1002 100nF X5R 6.3V C0201
C1001 100nF X5R 6.3V C0201

For NPU Power

VDD_NPU_VEPU

C1019 10uF X5R 4V C0402
C1018 1uF X5R 6.3V C0402
C1017 100nF X5R 6.3V C0201
C1016 100nF X5R 6.3V C0201

For VEPU Power

VDD_ARM

C1015 10uF X5R 4V C0402
C1014 1uF X5R 6.3V C0402
C1013 100nF X5R 6.3V C0201
C1012 100nF X5R 6.3V C0201

VDD_LOGIC

C1011 10uF X5R 4V C0402
C1009 1uF X5R 6.3V C0402
C1010 1uF X5R 6.3V C0402
C1007 100nF X5R 6.3V C0201
C1008 100nF X5R 6.3V C0201

GND

U1000O
RV1126/RV1109
BGA409 14R00X14R00X0R90

VSS/AVSS

A1	VSS_1	VSS_53	K9		
A21	AVSS_2	VSS_54	K12		
B12	VSS_3	VSS_55	K13		
C3	VSS_4	VSS_56	K14		
C5	VSS_5	VSS_57	L2		
C7	VSS_6	VSS_58	L5		
C10	VSS_7	VSS_59	L6		
C12	VSS_8	VSS_60	L11		
D9	VSS_9	VSS_61	L12		
D12	VSS_10	VSS_62	L13		
D18	AVSS_11	VSS_63	L14		
E4	VSS_12	VSS_64	L16		
E6	VSS_13	VSS_65	M3		
E8	VSS_14	VSS_66	M5		
E9	VSS_15	VSS_67	M7		
E10	VSS_16	VSS_68	M8		
E11	VSS_17	VSS_69	M10		
E12	VSS_18	VSS_70	M12		
F3	VSS_19	VSS_71	M13		
F5	VSS_20	VSS_72	M14		
F7	VSS_21	VSS_73	M16		
F8	VSS_22	VSS_74	N5		
F9	VSS_23	VSS_75	N6		
F10	VSS_24	VSS_76	N7		
F11	VSS_25	VSS_77	N10		
F12	VSS_26	VSS_78	N11		
F13	VSS_27	VSS_79	N13		
F14	AVSS_28	VSS_80	N14		
F15	AVSS_29	VSS_81	N16		
G2	VSS_30	VSS_82	P5		
G5	VSS_31	VSS_83	P7		
G6	VSS_32	VSS_84	P8		
G10	VSS_33	VSS_85	P9		
G11	VSS_34	VSS_86	P14		
G12	VSS_35	VSS_87	P16		
G13	VSS_36	VSS_88	R1		
G16	AVSS_37	VSS_89	R5		
G17	AVSS_38	VSS_90	R12		
H4	VSS_39	VSS_91	R13		
H5	VSS_40	VSS_92	R14		
H6	VSS_41	VSS_93	T6		
H7	VSS_42	VSS_94	T9		
H10	VSS_43	VSS_95	T10		
H15	VSS_44	VSS_96	T14		
J5	VSS_45	VSS_97	T17		
J6	VSS_46	VSS_98	V17		
J12	VSS_47	VSS_99	W9		
J14	VSS_48	VSS_100	W14		
J16	VSS_49	VSS_101	AA1		
K5	VSS_50	VSS_102	AA10		
K6	VSS_51	VSS_103	AA21		
K8	VSS_52				

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	10.RV1126/1109_Power/GND				
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Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	8 of 37

OSC/PLL/PMUIO

U1000K
RV1126/RV1109
BGA409_14R00X14R00X0R90

OSC/PLL

XOUT24M Y9
XIN24M AA9
PLL_AVDD_0V8 P11
PLL_AVDD_1V8 R11

Digital Power of PMUIO0&PMUIO1

PMUIO_VDD_0V8 P10
PMUIO_VDD_1V8 R10

PMUIO0 Domain

			TVSS	T8
			nPOR_u	W7
		CLK_REF	GPIO0_A0_d	W6
TSADC_SHUT_M0	TSADC_SHUTORG		GPIO0_A1_z	Y5
		CLKI_CLKO_32K	GPIO0_A2_z	AA3
		SDMMC0_DET	GPIO0_A3_u	U7
		SPI0_CS1n_M0	GPIO0_A4_u	V7
		SPI0_CS0n_M0	GPIO0_A5_u	AA2
		SPI0_MOSI_M0	GPIO0_A6_d	V6
		SPI0_MISO_M0	GPIO0_A7_d	W5
		SPI0_CLK_M0	GPIO0_B0_d	Y4

PMUIO0_VDD R9

PMUIO1 Domain

	PMIC_INT	PWM7_IR_M0	GPIO0_B1_d	W10
TSADC_SHUT_M1	PMIC_SLEEP	PWM6_M0	GPIO0_B2_d	Y10
FLASH_VOL_SEL			GPIO0_B3_d	Y8
	I2C0_SCL		GPIO0_B4_d	AA7
	I2C0_SDA		GPIO0_B5_d	Y7
	UART1_TX_M0	PWM0_M0	GPIO0_B6_d	W8
	UART1_RX_M0	PWM1_M0	GPIO0_B7_d	V9
SDMMC0_PWR	UART1_RTSN_M0	PWM2_M0	GPIO0_C0_d	U9
USB_CTRL PMU_DEBUG	UART1_CTSN_M0	PWM3_IR_M0	GPIO0_C1_d	AA4
	I2C2_SCL	PWM4_M0	GPIO0_C2_d	AA6
	I2C2_SDA	PWM5_M0	GPIO0_C3_d	Y6

PMUIO1_VDD R8

Y1100
24MHz
CRY4_3R20X2R50X0R80

R1100 22R 5% R0402
C1100 15pF C0G 50V C0402
C1101 15pF C0G 50V C0402
C1109 1nF X5R 25V C0201
R1104 3.3R 1% R0402
C1106 100nF X5R 6.3V C0402
R1103 0R 5% R0402
C1107 100nF X5R 6.3V C0201
C1108 100nF X5R 6.3V C0201

VCC0V8_PMU
VCC1V8_PMU
VCC3V3_SYS
PMUIO_VDD_1V8
RESET
RTC_INT_L
TSADC_SHUT
SDMMC0_DET
BT_WAKE_HOST
WIFI_REG_ON
BT_RST
WIFI_WAKE_HOST
PMIC_INT
PMIC_SLEEP
FLASH_VOL_SEL
I2C0_SCL_PMIC
I2C0_SDA_PMIC
LCD_PWM
TP_INT
TP_RST_L
USB_CTRL
I2C2_SCL
I2C2_SDA

NOTE:
USB_CTRL must used GPIO0_C1

NOTE:
PMUIO_VDD_0V8 and PLL_AVDD_0V8 share one power supply and one decoupling capacitor, which is placed close to the pin position.

PMUIO_VDD_1V8 and PLL_AVDD_1V8 share one power supply and one decoupling capacitor, which is placed close to the pin position

VCC1V8_PMU
C1104 100nF X5R 6.3V C0201
C1105 1uF X5R 6.3V C0402 DNP

VCC0V8_PMU
C1103 100nF X5R 6.3V C0201
C1102 1uF X5R 6.3V C0402 DNP

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RV1126_RV1109 GATE REF		
File:	11.RV1126/1109_OSC/PLL/PMUIO		
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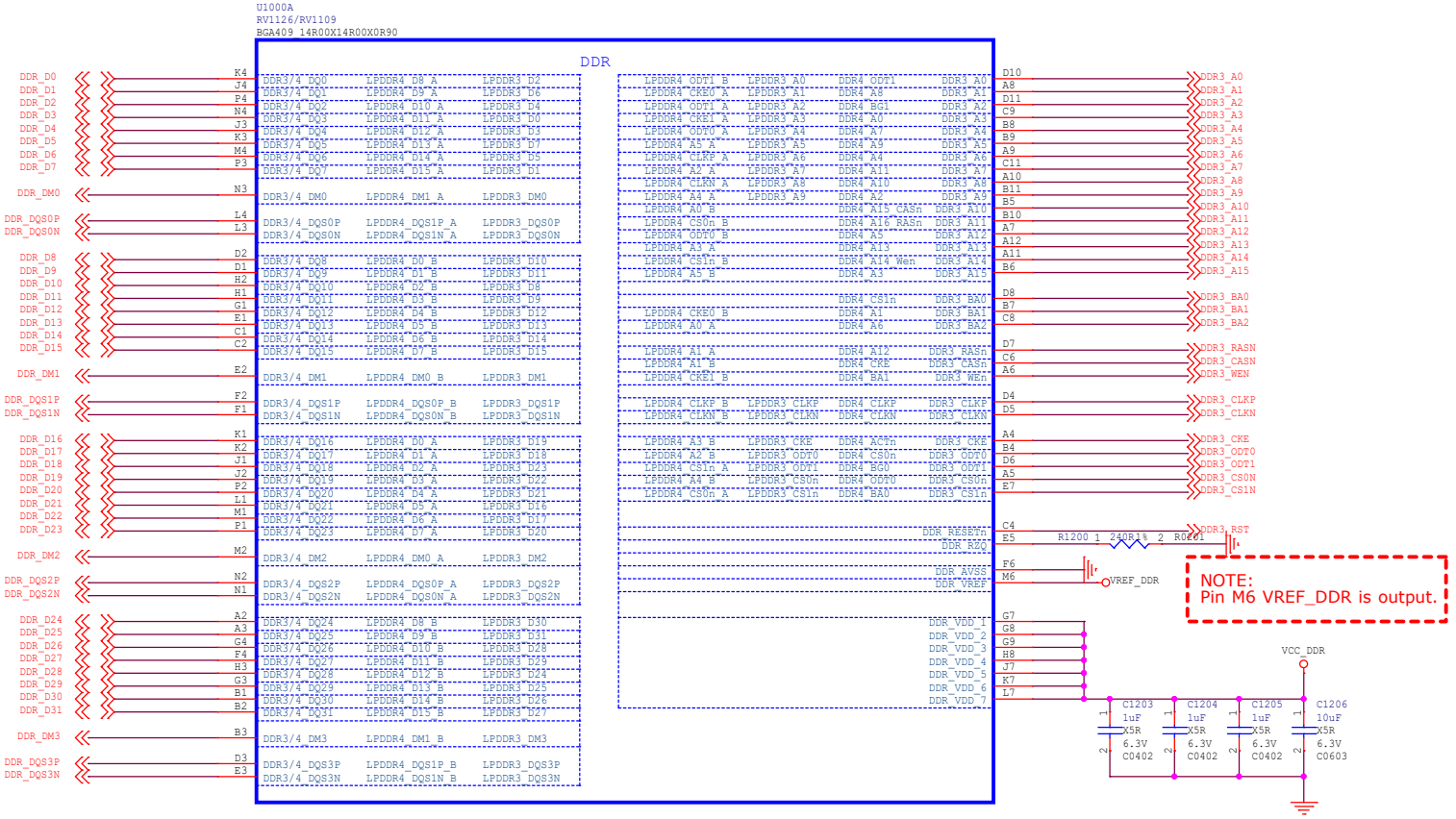
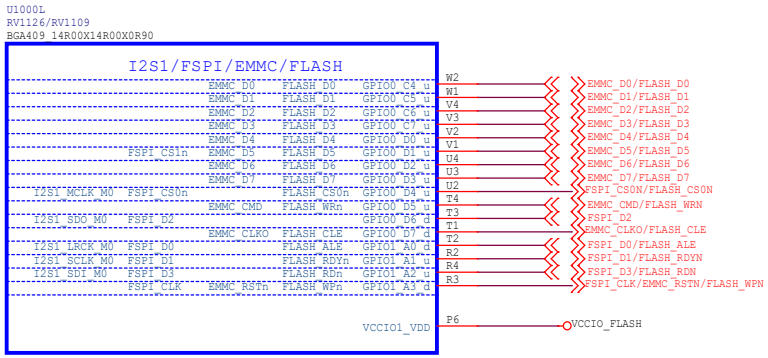
DDR Controller

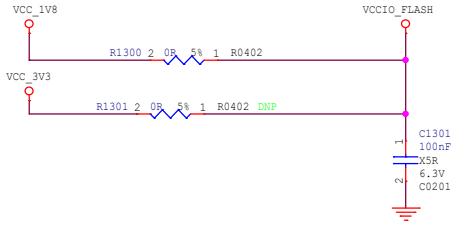


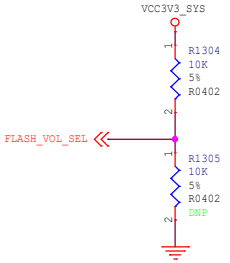
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RV1126_RV1109 GATE REF		
File:	12.RV1126/1109_DRAM Controller		
Date:	Thursday, August 20, 2020	Rev:	V1.3
Designed by: Yanhong.Li	Reviewed by: <Checker>	Sheet:	10 of 37

EMMC/FLASH



NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.

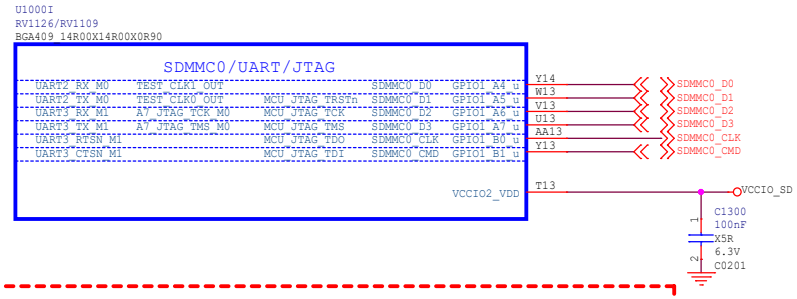




NOTE:
FLASH(VCCIO1) power domain IO supply configuration pin:

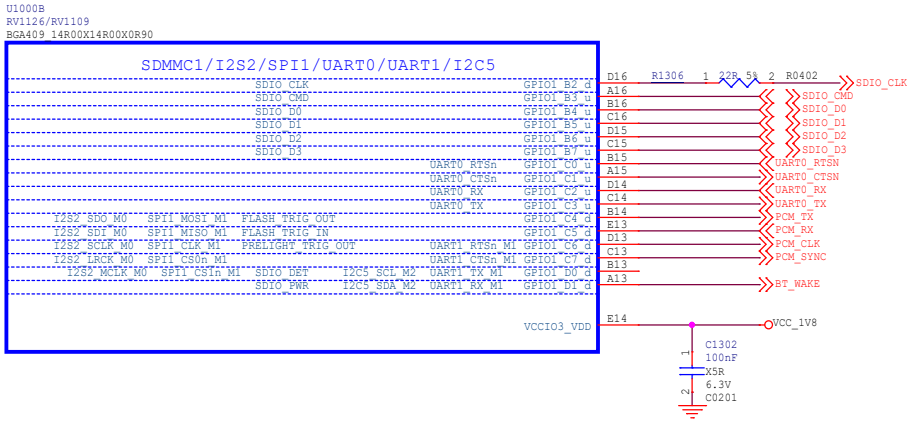
Condition	VCCIO1 (VCCIO_FLASH)
FLASH_VOL_SEL=0	3.3V
FLASH_VOL_SEL=1	1.8V Default

SDMMC0/JTAG



NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.
If SD card is not used,please reserve MCU JTAG interface

SDMMC1/UART/I2S2



NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	13.RV1126/1109_Flash/SD				
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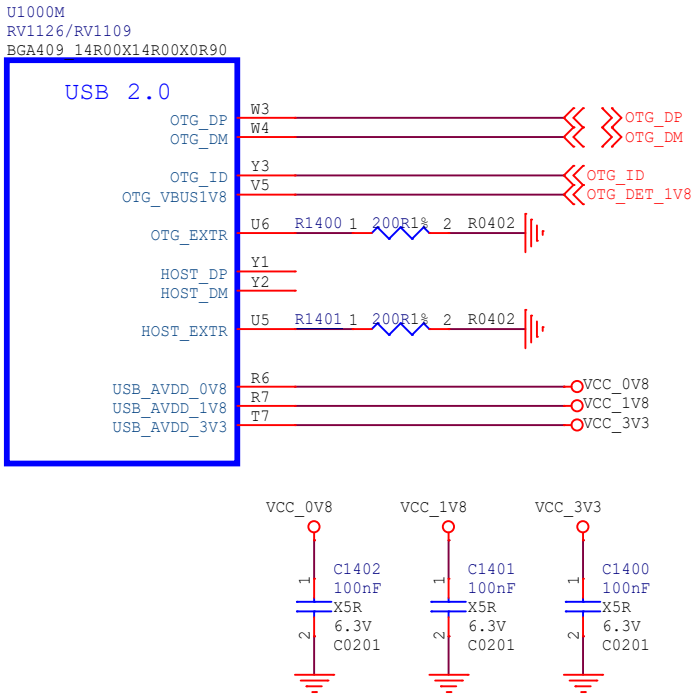
USB Controller



USB2.0 design rules:
1. Max intra-pair skew <4ps
2. Max trace length<6inchs
3. Max allowed via <6
4. Trace impedance 90ohm+/-10%
5. The distance between other signals follows the 3W rule.

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	14.RV1126/1109_USB Controller				
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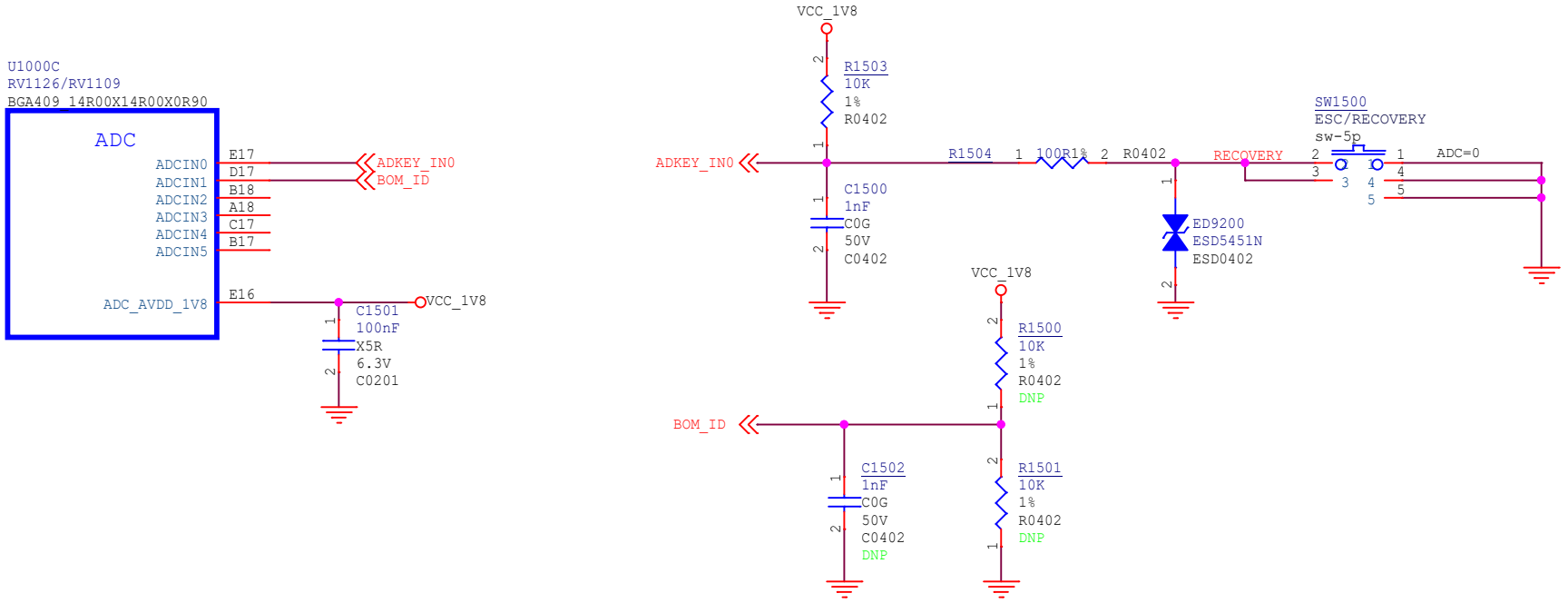
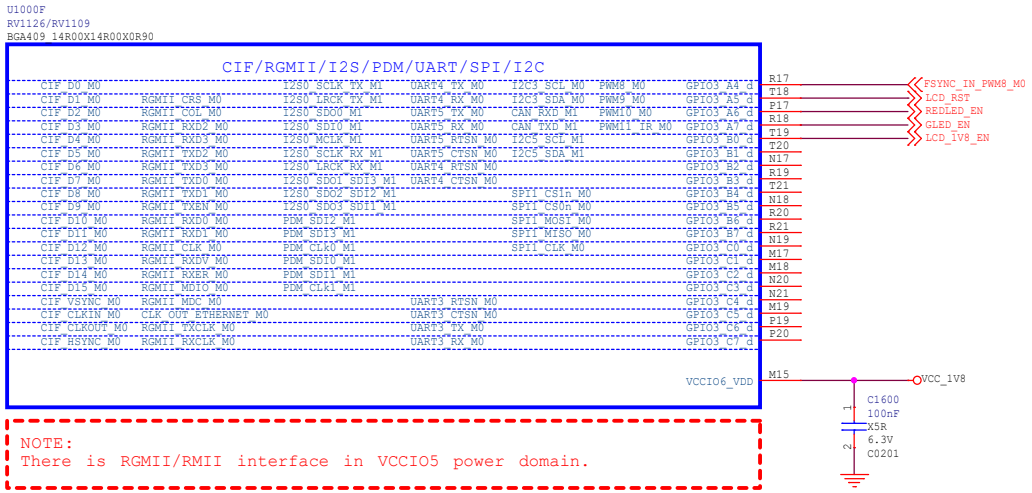
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	12 of 37

SARADC



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	15.RV1126/1109_SARADC				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	13 of 37

CIF Interface

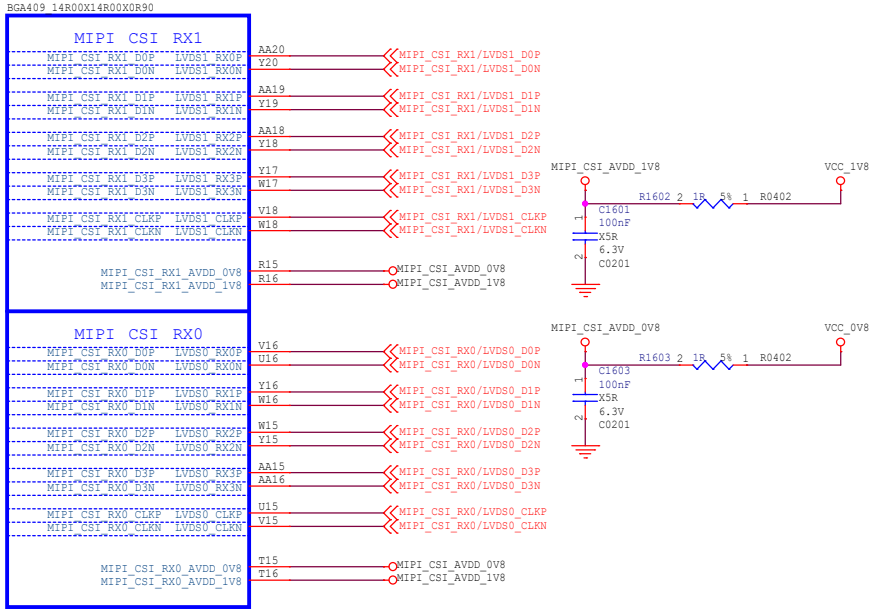


NOTE:
There is RGMII/RMII interface in VCCIO5 power domain.

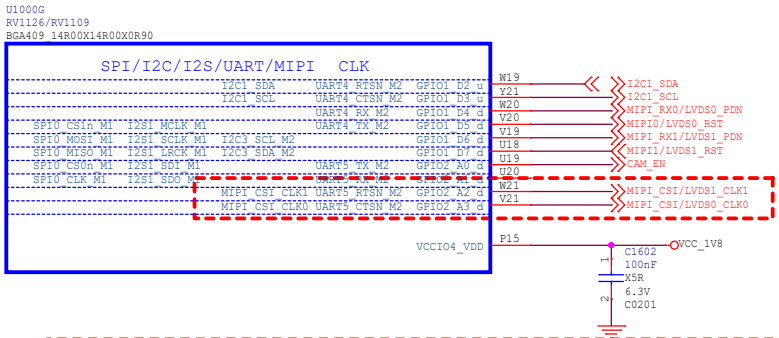
BT1120 RX	DATA:CIF_DATA[15:0] Y[0:7]:CIF_DATA[8:15] Cb[0:7]:CIF_DATA[0:7] CLOCK:CIF_CLKIN
12bit CIF camera	CameraCIF[12:0]:CIF_DATA[15:4] XCLK:CIF_CLKOUT PCLK:CIF_CLKIN HSYNC:CIF_HSYNC VSYNC:CIF_VSYNC
10bit CIF camera	CameraCIF[10:0]:CIF_DATA[15:6] XCLK:CIF_CLKOUT PCLK:CIF_CLKIN HSYNC:CIF_HSYNC VSYNC:CIF_VSYNC
8bit CIF camera	CameraCIF[8:0]:CIF_DATA[15:8] XCLK:CIF_CLKOUT PCLK:CIF_CLKIN HSYNC:CIF_HSYNC VSYNC:CIF_VSYNC

MIPI-CSI Interface

MIPI_CSI_RX0 and MIPI_CSI_RX1 power pins are adjacent, so they share a decoupling capacitor
All the power filter capacitors should be placed close to the power pins of SOC.



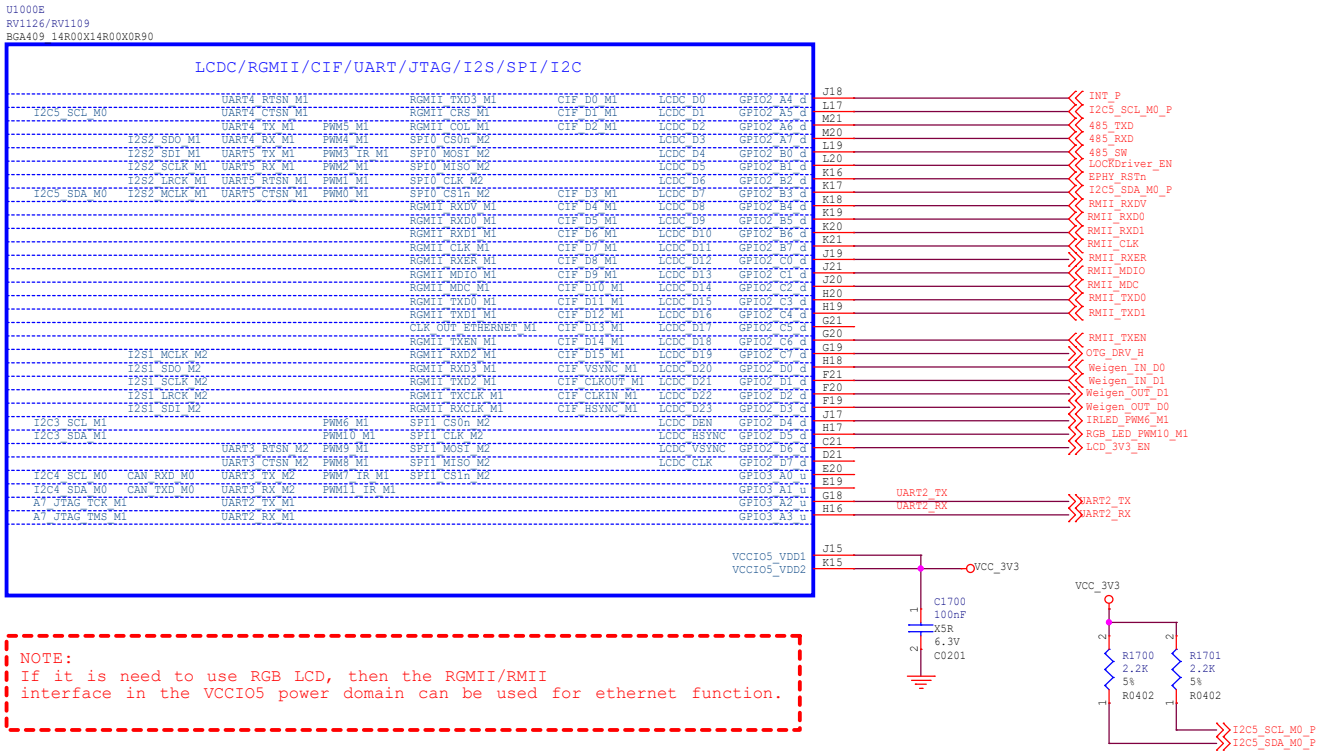
I2C/SPI/MIPI-CLK



NOTE:
The frequence of MIPI_CSI_CLK0 and MIPI_CSI_CLK1 is from the same frequency source, so the output the same frequence.
It's really important for dual camera module.

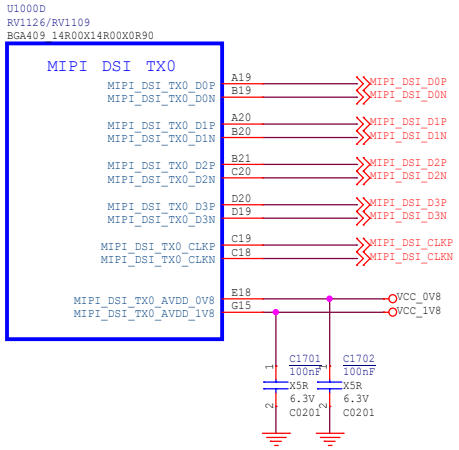
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	16.RV1126/1109_VideoInput				
Date:	Monday, August 24, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	14 of 37

LCDC/RGMII/PWM



BT1120 TX	DATA:LCDC_DATA[15:0] Y[0:7]:LCDC_DATA[8:15] Cb[0:7]:LCDC_DATA[0:7] CLOCK:LCDC_CLK
6bit Serial RGB	DATA:LCDC_DATA[5:0] CLOCK:LCDC_CLK HSYNC:LCDC_HSYNC VSYNC:LCDC_VSYNC DE:LCDC_DEN
8bit Serial RGB	DATA:LCDC_DATA[7:0] CLOCK:LCDC_CLK HSYNC:LCDC_HSYNC VSYNC:LCDC_VSYNC DE:LCDC_DEN
16bit Parallel RGB(RGB656)	R[4:0]:LCDC_DATA[15:11] G[5:0]:LCDC_DATA[10:5] B[4:0]:LCDC_DATA[4:0] CLOCK:LCDC_CLK HSYNC:LCDC_HSYNC VSYNC:LCDC_VSYNC DE:LCDC_DEN
18bit Parallel RGB(RGB666)	R[5:0]:LCDC_DATA[17:12] G[5:0]:LCDC_DATA[11:6] B[5:0]:LCDC_DATA[5:0] CLOCK:LCDC_CLK HSYNC:LCDC_HSYNC VSYNC:LCDC_VSYNC DE:LCDC_DEN
24bit Parallel RGB(RGB888)	R[7:0]:LCDC_DATA[23:16] G[7:0]:LCDC_DATA[15:8] B[7:0]:LCDC_DATA[7:0] CLOCK:LCDC_CLK HSYNC:LCDC_HSYNC VSYNC:LCDC_VSYNC DE:LCDC_DEN

MIPI-DSI Interface



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RV1126_RV1109 GATE REF		
File:	17.RV1126/1109_VideoOutput Interface		
Date:	Thursday, August 20, 2020	Rev:	V1.3
Designed by: Yanhong.Li	Reviewed by: <Checker>	Sheet:	15 of 37

Audio Interface

U1000J
RV1126/RV1109
BGA409_14R00X14R00X0R90

I2S/PDM/ACODEC/I2C

I2S0_SCLK_TX_M0		ACODEC_DAC_CLK			GPIO3_D0_d	W12
I2S0_SCLK_RX_M0	PDM_CLK1_M0	ACODEC_ADC_CLK			GPIO3_D1_d	V12
I2S0_MCLK_M0					GPIO3_D2_d	U12
I2S0_LRCK_TX_M0		ACODEC_DAC_SYNC	AUDPWM_L_M1	AUDDSM_LN	GPIO3_D3_d	W11
I2S0_LRCK_RX_M0	PDM_CLK0_M0	ACODEC_ADC_SYNC			GPIO3_D4_d	Y12
I2S0_SDO0_M0		ACODEC_DAC_DATAR	AUDPWM_R_M1	AUDDSM_LP	GPIO3_D5_d	Y11
I2S0_SDI0_M0	PDM_SDI0_M0	ACODEC_DAC_DATAL			GPIO3_D6_d	AA12
I2S0_SDO1_SDI3_M0	PDM_SDI3_M0	ACODEC_ADC_DATA			GPIO3_D7_d	T11
I2S0_SDO2_SDI2_M0	PDM_SDI2_M0	I2C4_SCL_M1	AUDPWM_L_M0	AUDDSM_RN	GPIO4_A0_d	U11
I2S0_SDO3_SDI1_M0	PDM_SDI1_M0	I2C4_SDA_M1	AUDPWM_R_M0	AUDDSM_RP	GPIO4_A1_d	V11
					VCCIO7_VDD	T12

GPIO3_D0 — I2S0_SCLK_TX_M0
GPIO3_D1 — PDM_CLK1
GPIO3_D2 — I2S0_MCLK_M0
GPIO3_D3 — I2S0_LRCK_TX_M0
GPIO3_D4 — PDM_CLK
GPIO3_D5 — I2S0_SDO0_M0
GPIO3_D6 — PDM_SDI0
GPIO3_D7 — I2S0_SDI3_M0

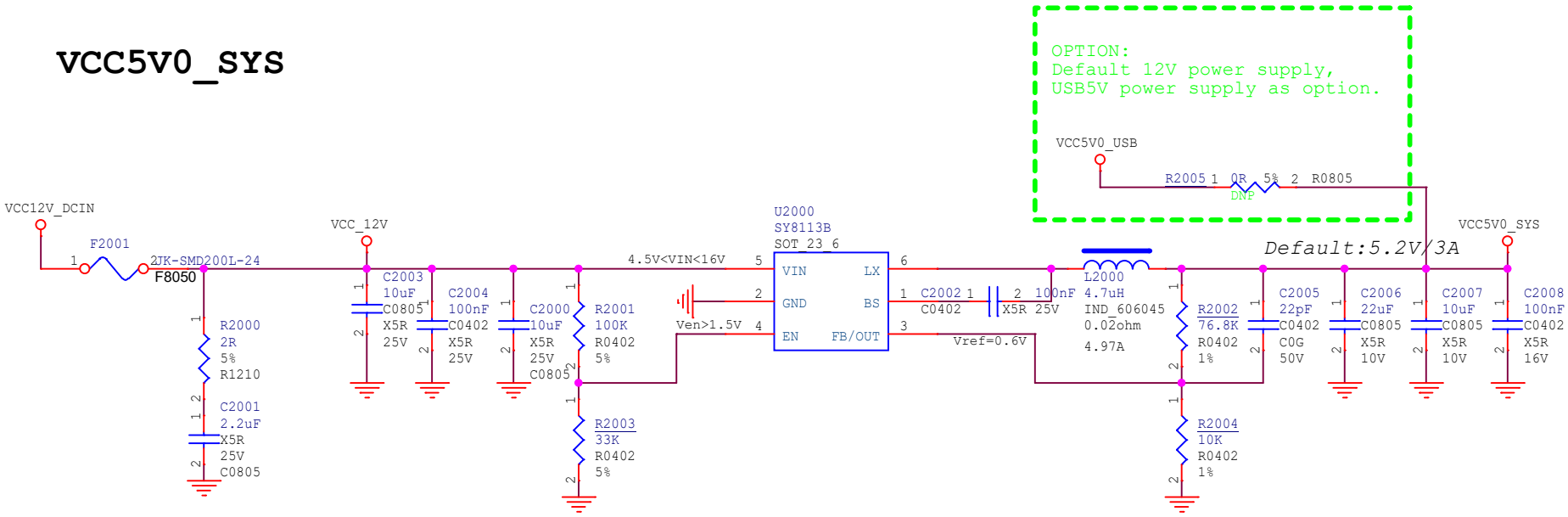
DEFAULT:
I2S0 connect to RK809-2
IO level is 1.8V

T12 — VCC_1V8

C1800
100nF
X5R
6.3V
C0201

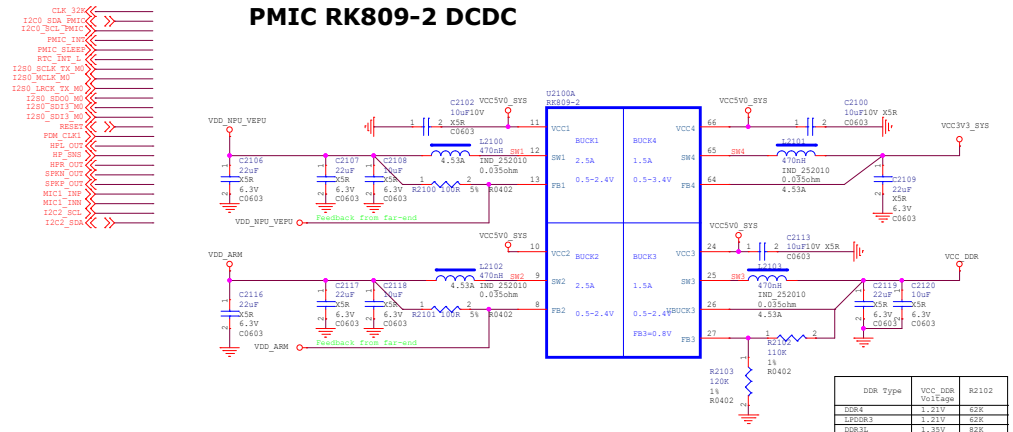
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	18.RV1126/1109_Audio				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	16 of 37

VCC5V0_SYS



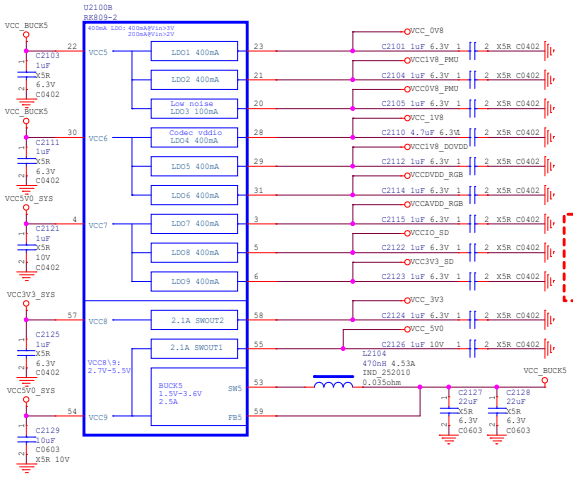
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	20.Power_DC IN				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	17 of 37

PMIC RK809-2 DCDC



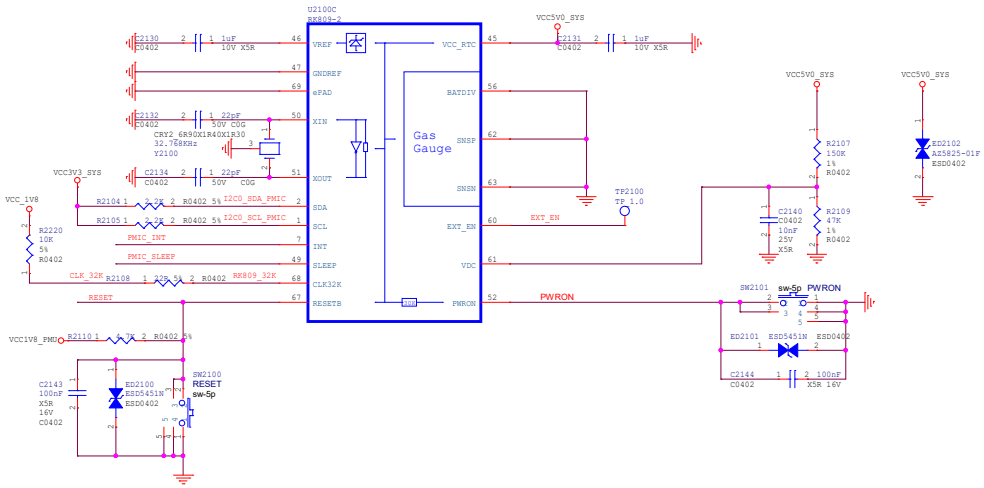
DDR Type	VCC_DDR Voltage	R2102
DDR4	1.21V	62K
LPDDR3	1.21V	62K
DDR3L	1.35V	82K
DDR3(default)	1.53V	110K
LPDDR4	1.14V	51K

PMIC RK809-2 LDO

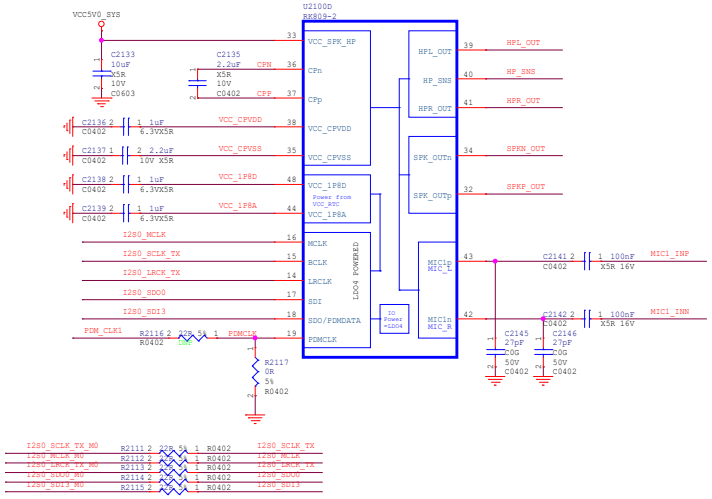


NOTE:
LDO8 and LDO9 output 3.3V default.
If there isn't SD card function,
LDO8 and LDO9 can be used for other function .

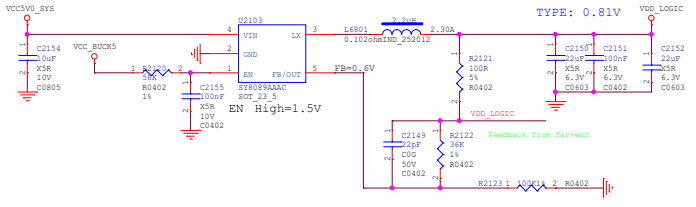
PMIC RK809-2 Managerment



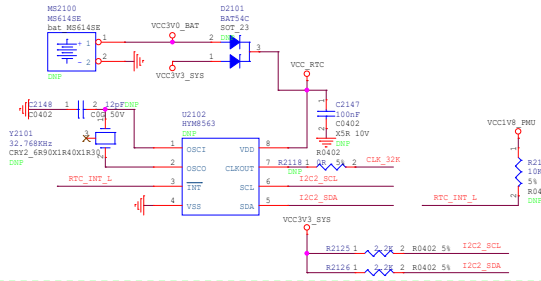
PMIC RK809-2 CODEC



VDD_LOGIC



NOTE:
1. If it still needs the RTC function when the systerm is poweroff, the RTC IC is recommended to use.
2. when the RTC IC is used, then the 32.768KHz crystal for the RK809-2 isn't needed.
3. The 32.768KHz crystal should connect to RTC IC.

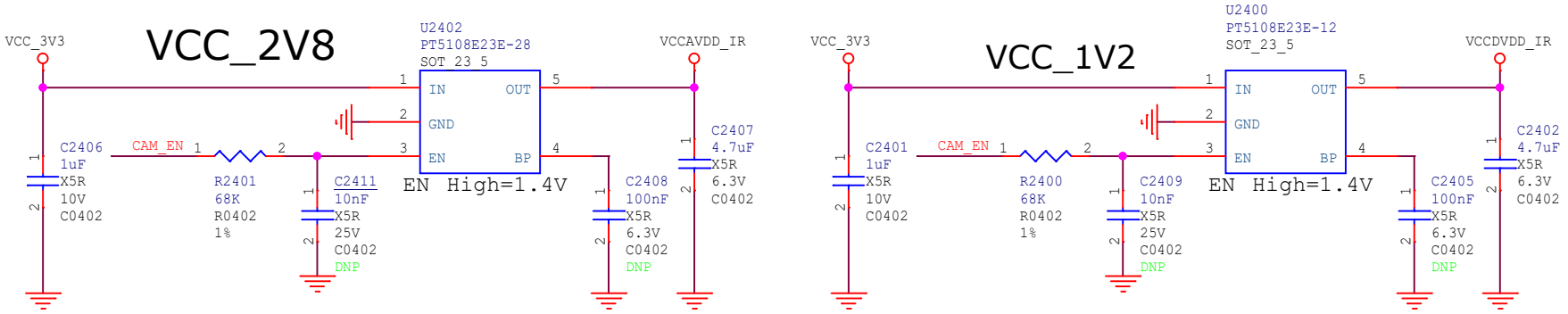


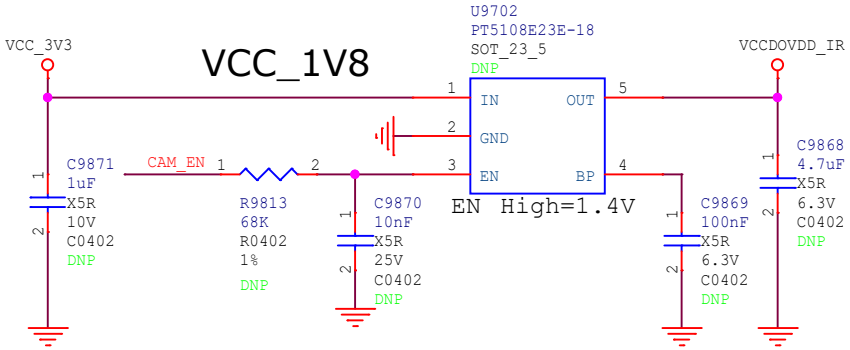
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RV1126_RV1109 GATE REF
File:	21.Power_PMIC
Date:	Thursday, August 20, 2020
Rev:	V1.3
Designed by:	Yanhong.Li
Reviewed by:	<Checker>
Sheet:	18 of 37

Discrete Power for Camera

CAM_EN

NOTE:
The power on sequence is adjusted according to the camera.

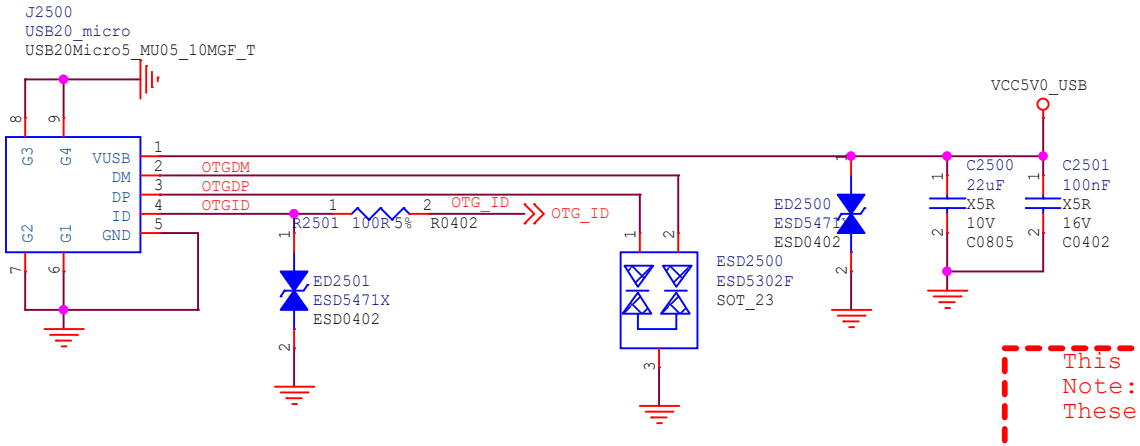


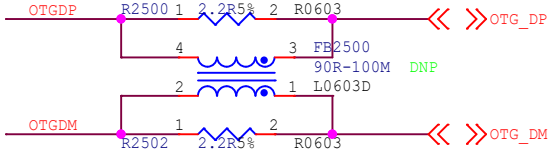


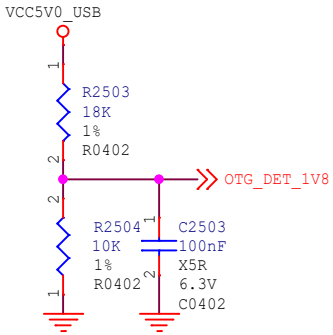
OPTION:
It is used for the camera mudules that the DOVDDs are separated.

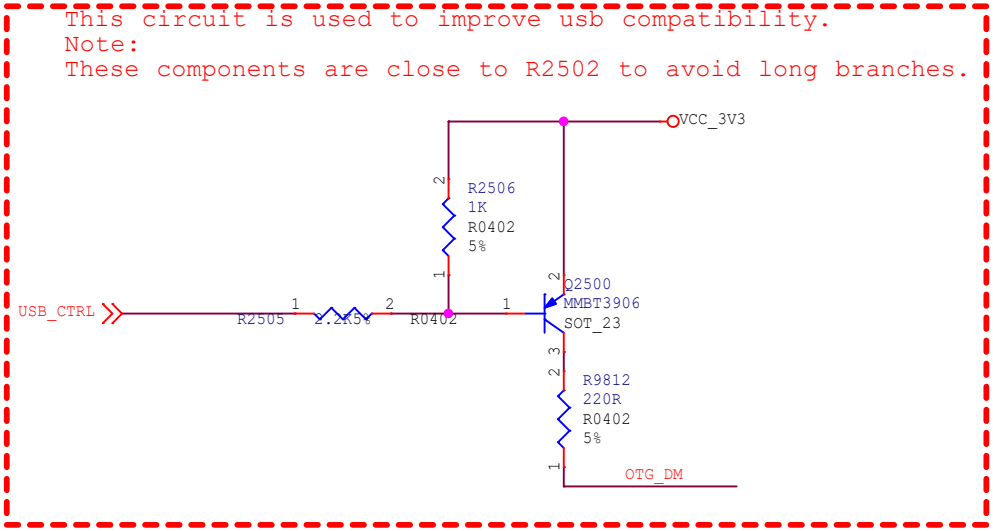
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	24.Discrete Power for Camera				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	19 of 37

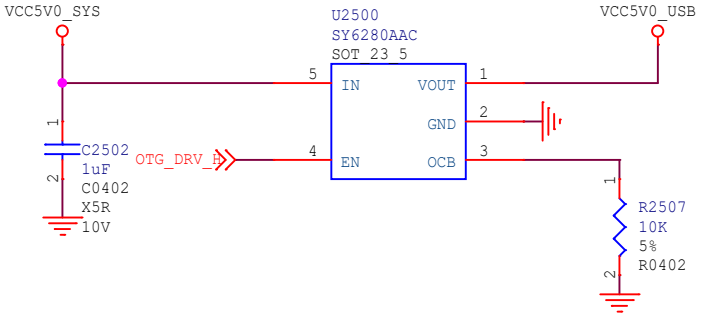
USB2.0 OTG







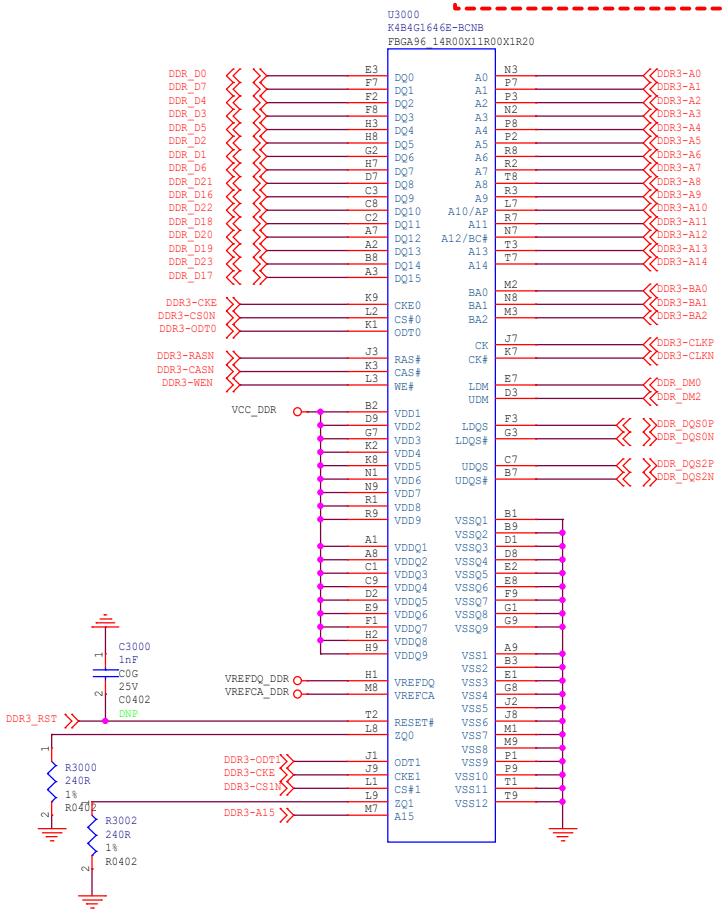


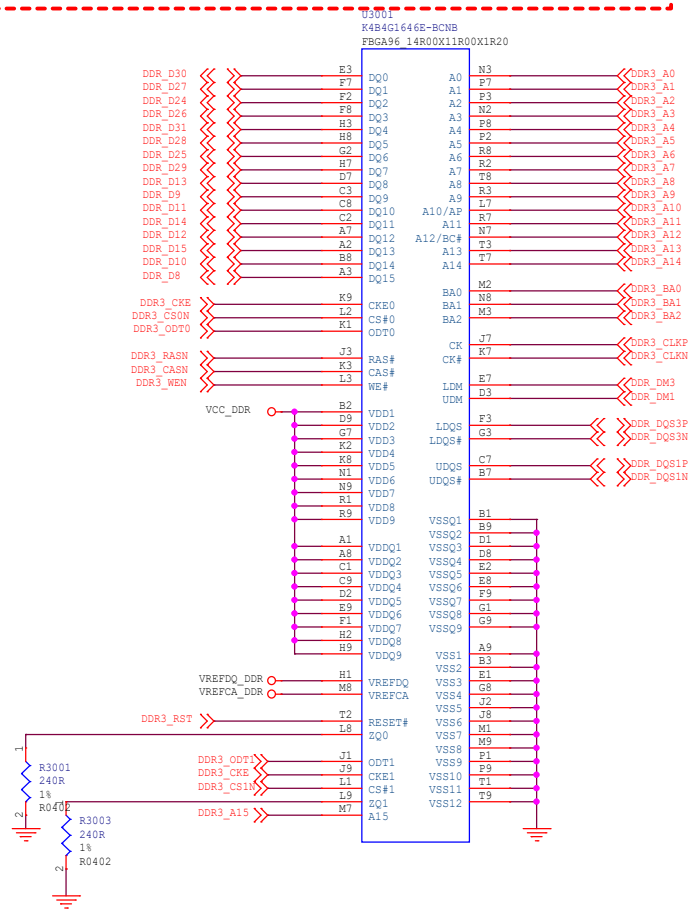


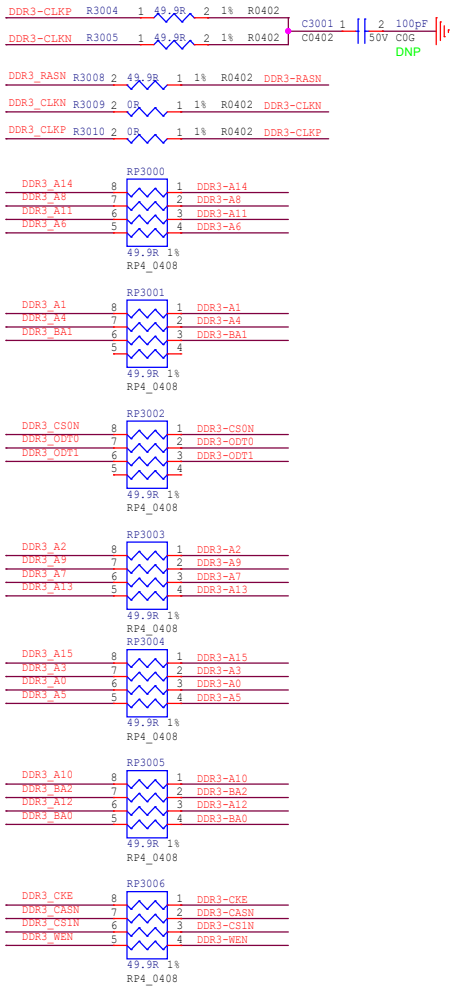
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	25.USB OTG				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	20 of 37

DDR3/DDR3L 2x16bit

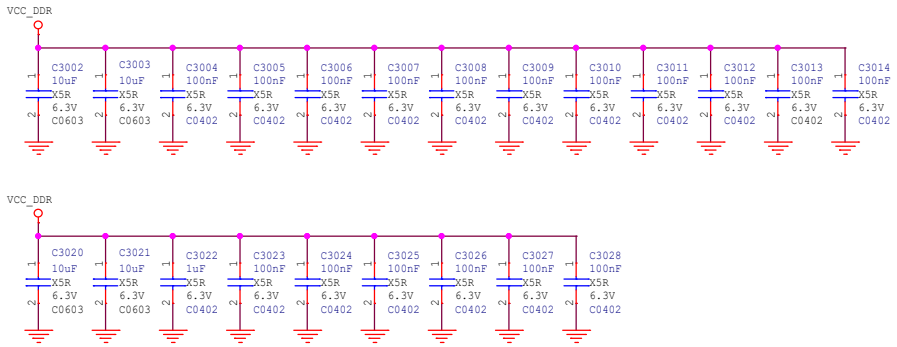
Note:
This is DDR template<RV1126_RV1109_Template_DDR3P216SD4_V10_20200619>. 4 layers PCB.
If only need one pcs DDR, please must use U3000(lane0,lane2).
If need other template, please apply to RK.

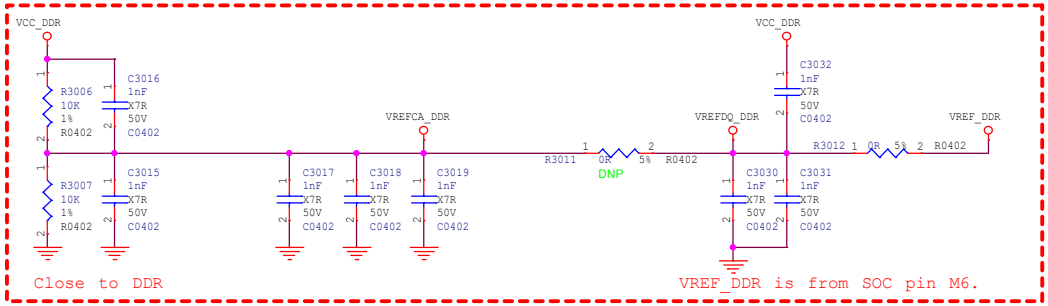






Note:All the Power filter capacitors should be placed close to the power pins of DDR3

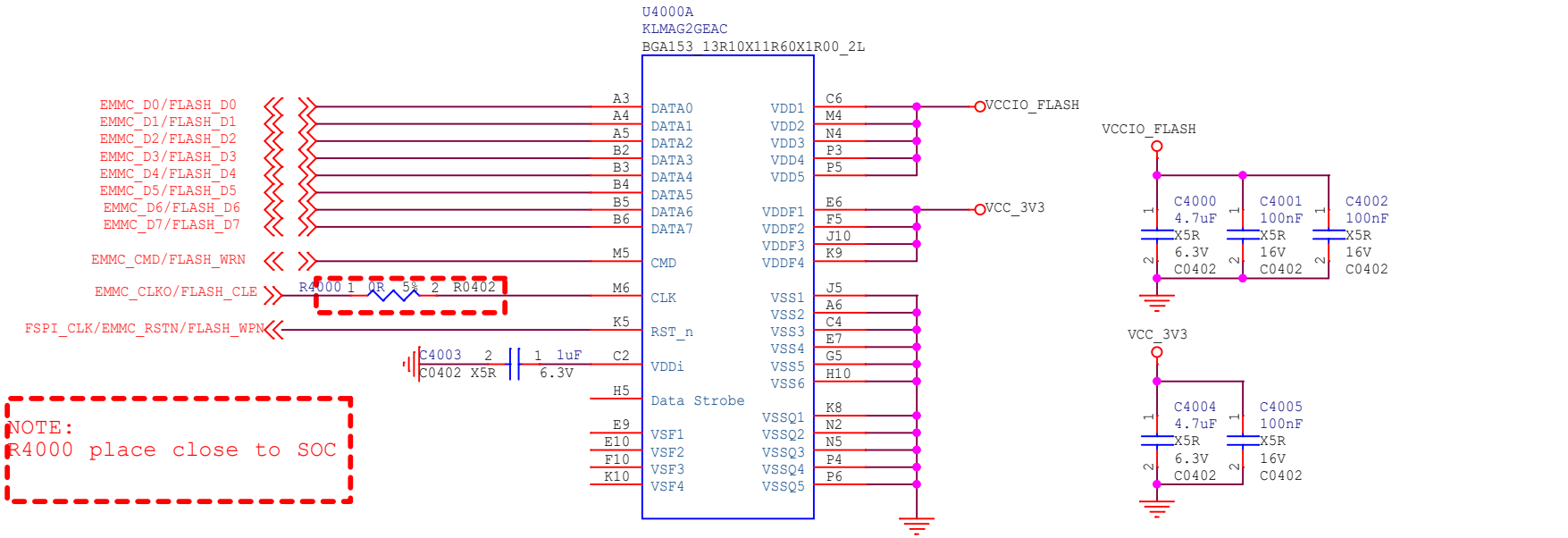




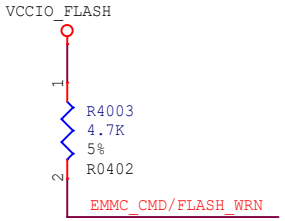
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	30.DRAM_DDR3_96P_2X16bit				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	21 of 37

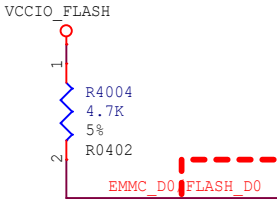
eMMC

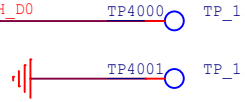
NOTE:
Refer to the latest AVL for parts selection.
NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.



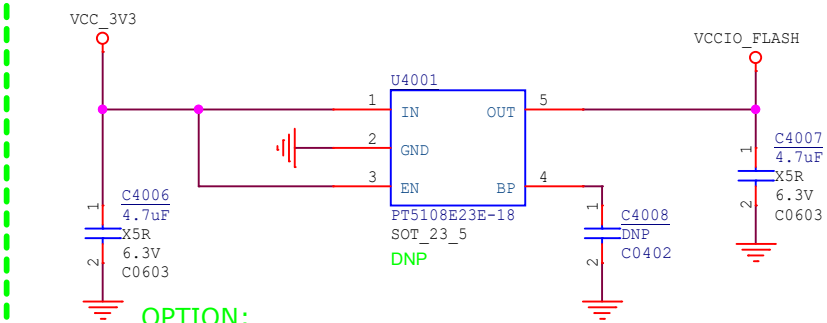
NOTE:
R4000 place close to SOC







NOTE:
Reserve testpoint for firmware update,
In the power on phase, if FLASH_D0= 0V,
the system will enter the maskROM mode

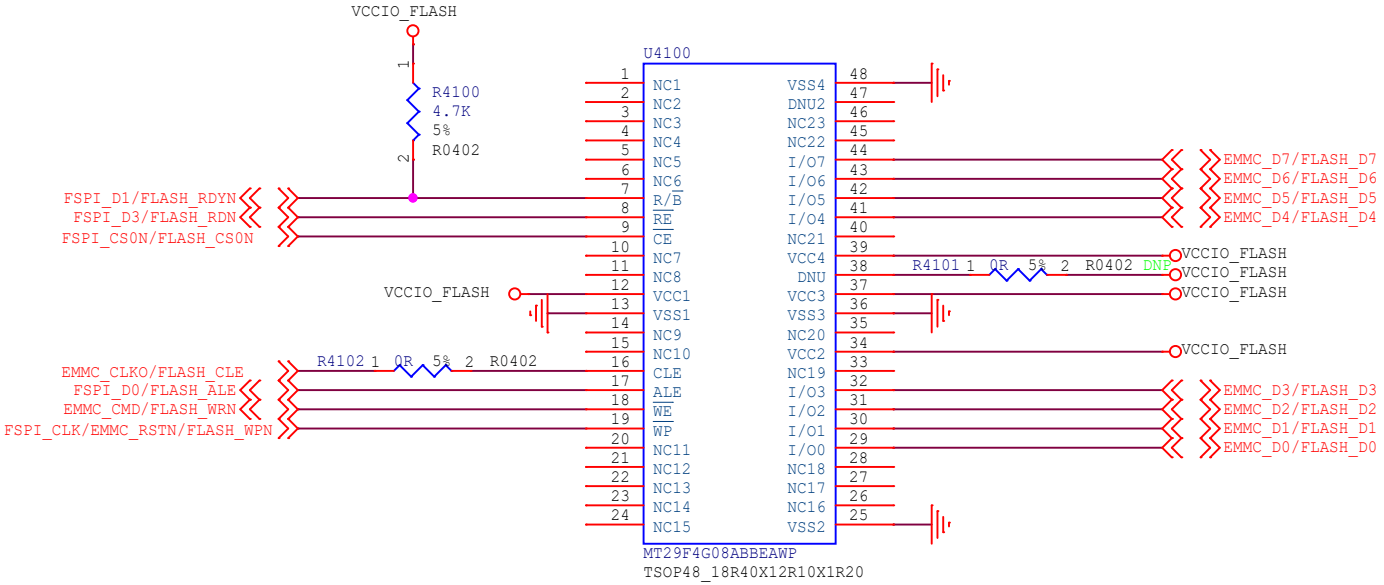


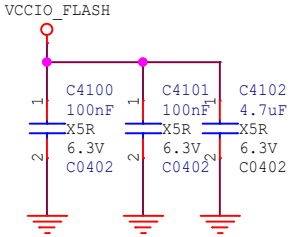
OPTION:
If EMMC peak current > 300mA,
please use LDO supply

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	40.Flash-eMMC Flash				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	22 of 37

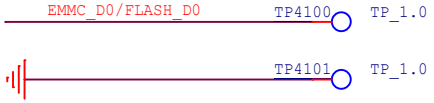
NAND FLASH

NOTE:
Refer to the latest AVL for parts selection.
Only support SLC NAND





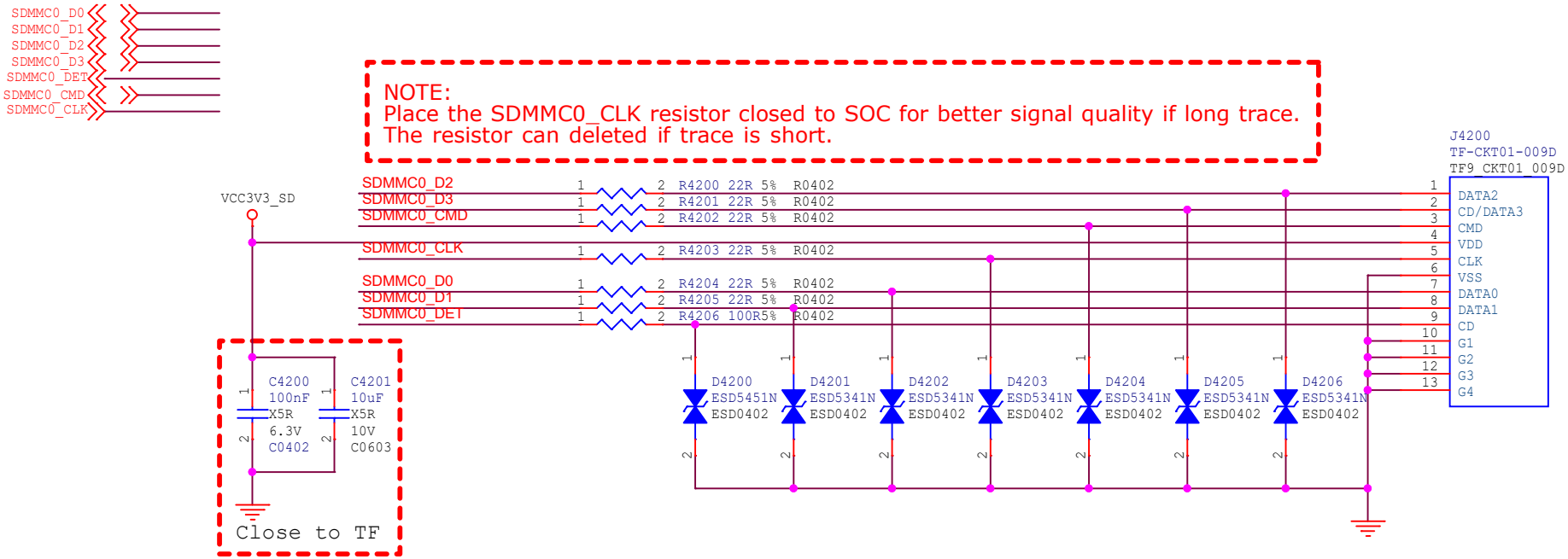
NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.



NOTE:
Reserve testpoint for firmware update,
In the power on phase, if FLASH_D0= 0V,
the system will enter the maskROM mode

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	41.Flash-Nand Flash				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	23 of 37

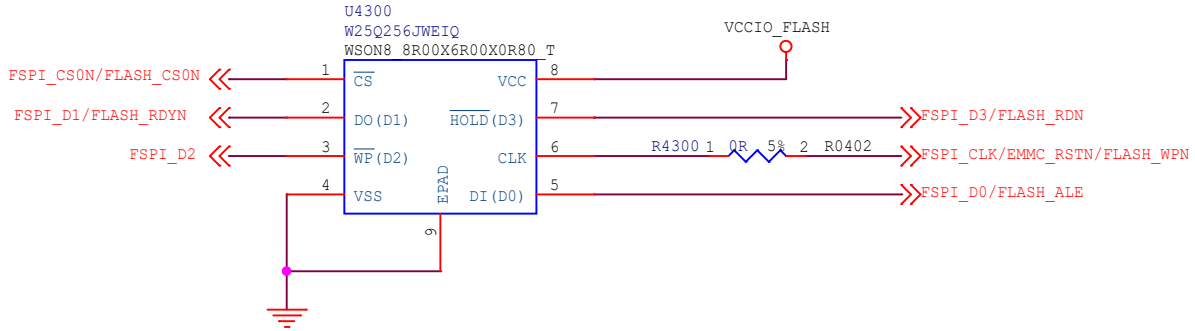
TF CARD

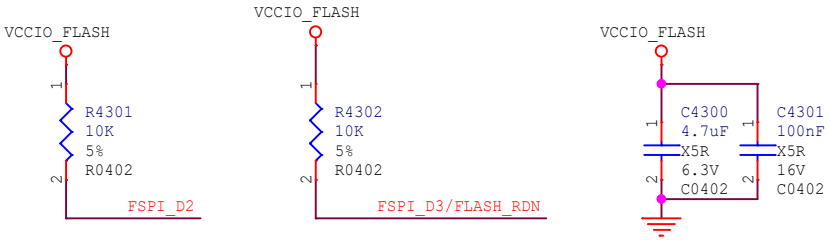


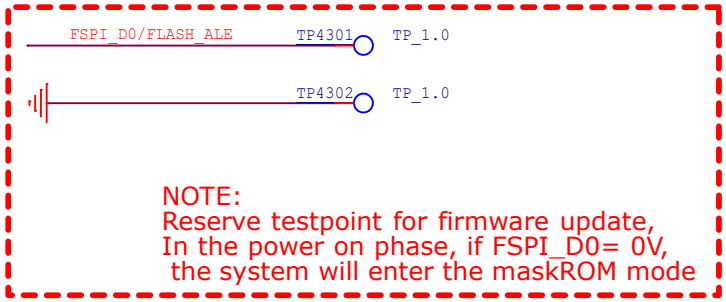
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	42.Flash-Micro-SD Card				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	24 of 37

SPI Flash

NOTE:
Refer to the latest AVL for parts selection.



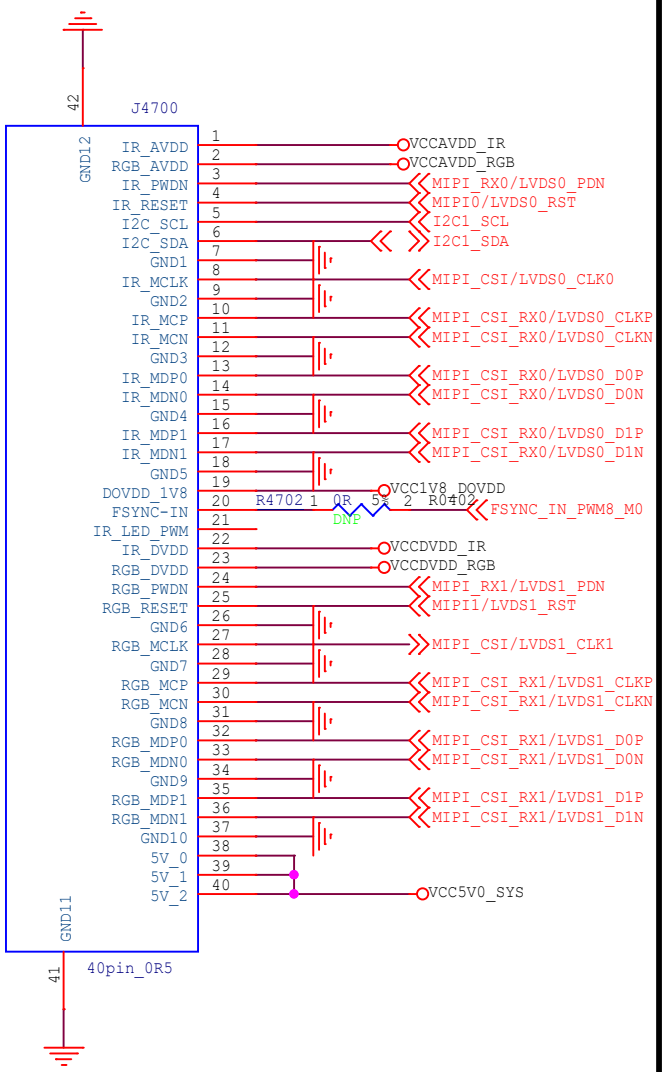




NOTE:
Reserve testpoint for firmware update,
In the power on phase, if FSPI_D0= 0V,
the system will enter the maskROM mode

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	43.Flash-SPI Flash				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	25 of 37

2 lane Dual MIPI Camera



NOTE:
1. IMX307/IMAX 327 must use LVDS interface.

2.Pls. pay attention to the I2C address of sensors,
don't use the same I2C address for two sensors.

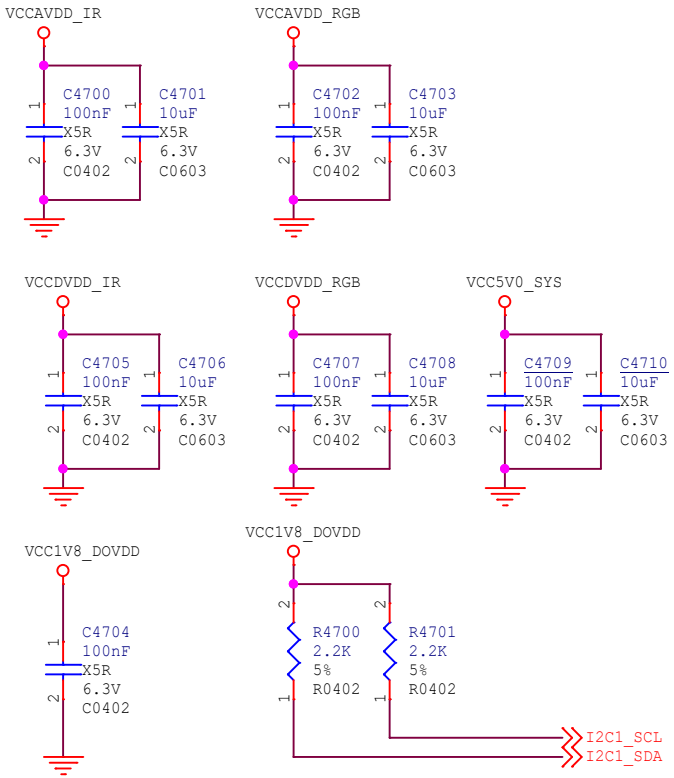
3.About the pin FYNC_IN, pls. connect 0R resistor first,
and then connect to the PWM pin of soc.

4. LVDS0 interfaces and MIPI_CSI_RX0 interfaces are mutiplex.
The two interfaces cannot be used at the same time.
It is the same rule for LVDS1 and MIPI_CSI_RX1.

5. If there are only two lanes need to used, pls.use lane0 and lane1.

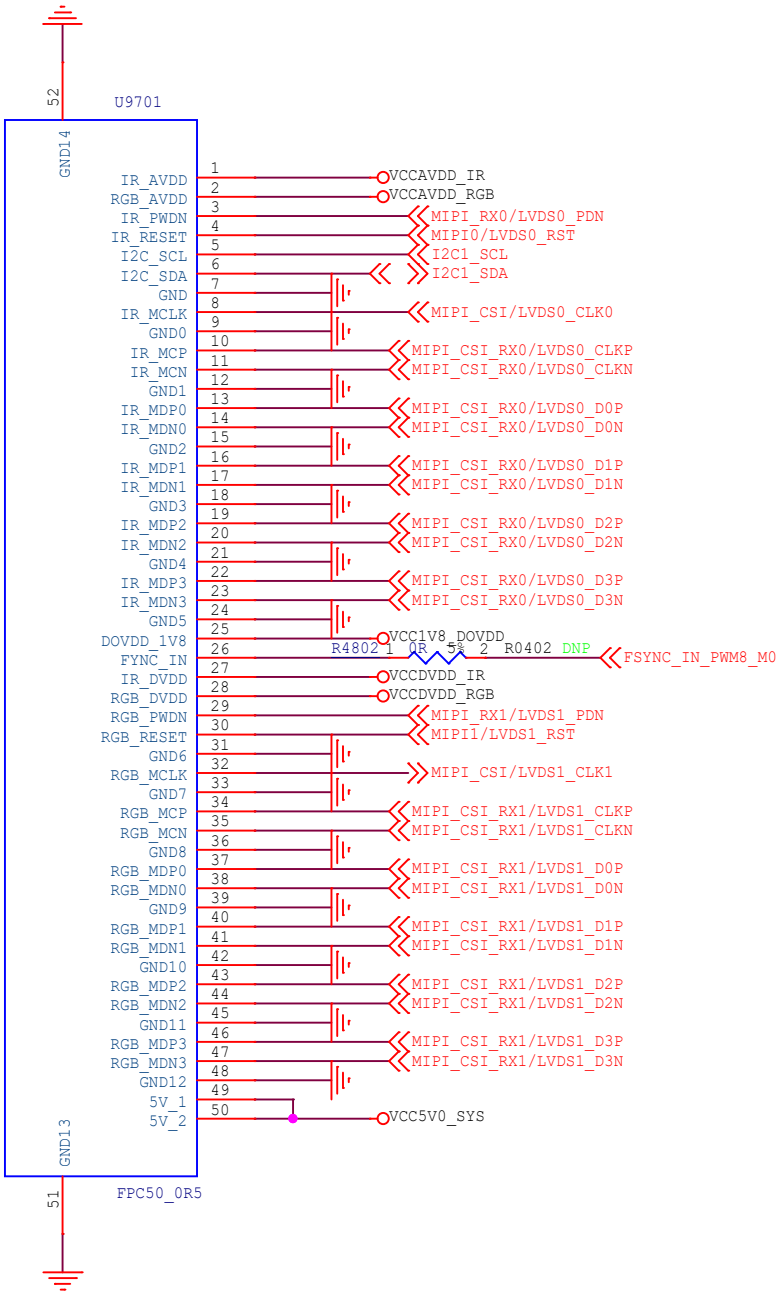
6.The DOVDDs are combined for the sensor module recommended by RK,
such as OV2718+GC2053,IMX307+GC2053. But If anothor two sensor modules are used,
the DOVDDs are recommended to separate for the reason of power on sequence.
It is needed to refine the pins of dual camera module.

7. The AVDDs of IR camera and RGB camera are needed to supply power separatey.
It's same rule for DVDD.



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	47.VI-Camera_MIPI-CSI				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	26 of 37

4 lane dual LVDS Camera



NOTE:

1. IMX307/IMAX 327 must use LVDS interface.

2.Pay attention to the I2C address of sensors, don't use the same I2C address for two sensors.

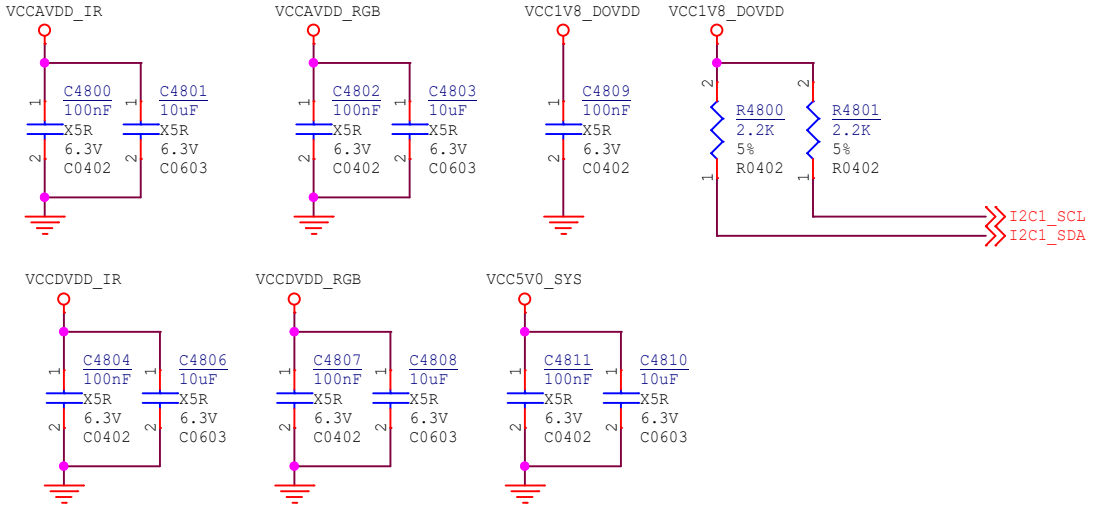
3.About the pin FYNC_IN, pls. connect 0R resistor first, and then connect to the PWM pin of soc.

4. LVDS0 interfaces and MIPI_CSI_RX0 interfaces are mutiplex. The two interfaces cannot be used at the same time. It is the same rule for LVDS1 and MIPI_CSI_RX1.

5. If there are only two lanes need to used, pls.use lane0 and lane1.

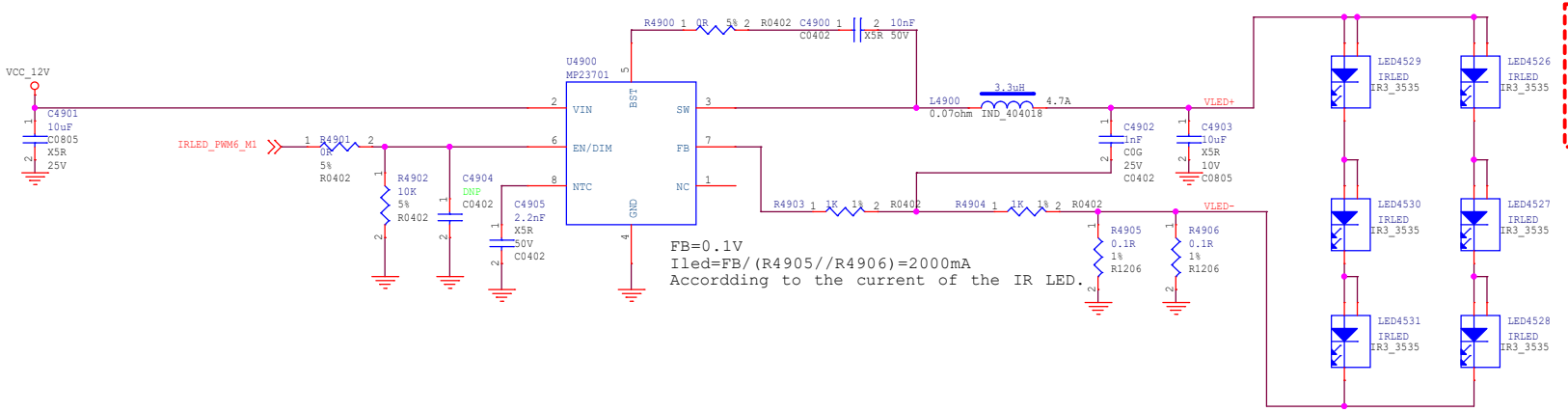
6.The DOVDDs are combined for the sensor module recommended by RK, such as OV2718+GC2053,IMX307+GC2053. But If anothor two sensor modules are used, the DOVDDs are recommended to separate for the reason of power on sequence. It is needed to refine the pins of dual camera module.

7. The AVDDs of IR camera and RGB camera are needed to supply power separatey. It's same rule for DVDD.



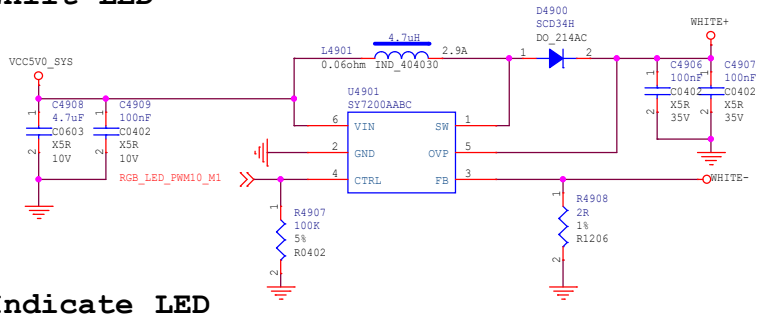
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	48.VI-Camera_LVDS				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	27 of 37

IR_LED

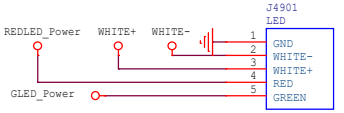


NOTE:
1. IR-LED select 850nm wavelength.
2. Angle of the LED is 90 degree.
3. The total driver current is 120mA for better effect.

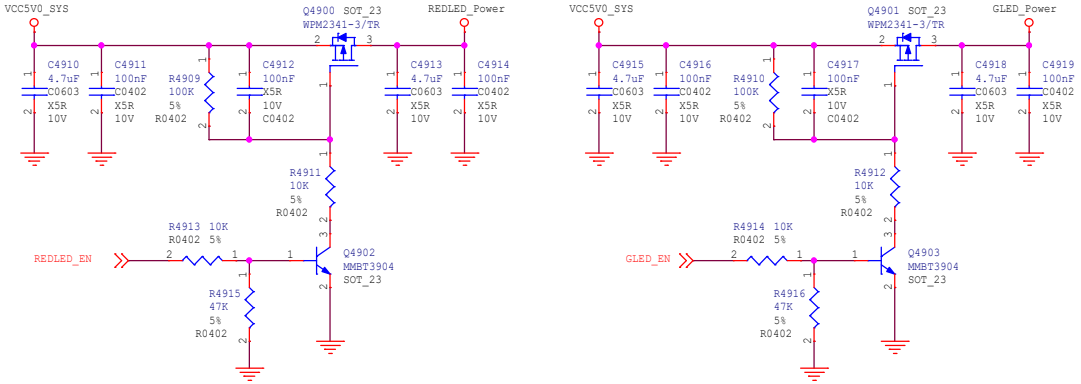
Whilt LED



LED Connector

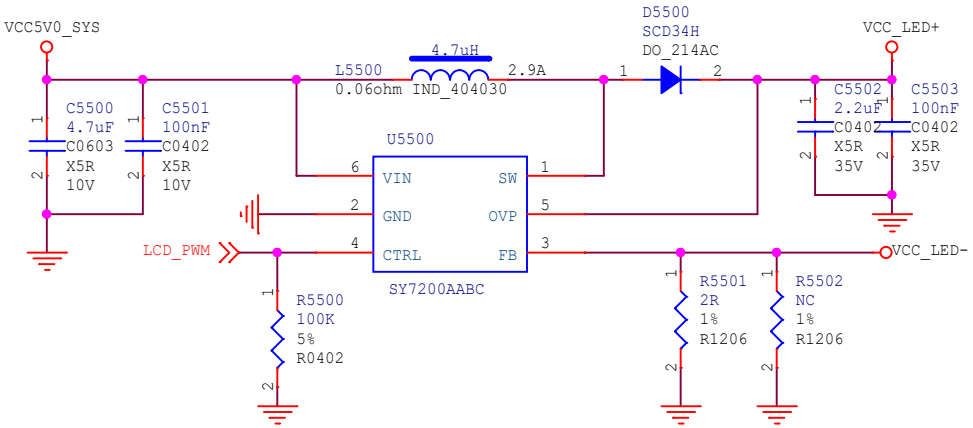


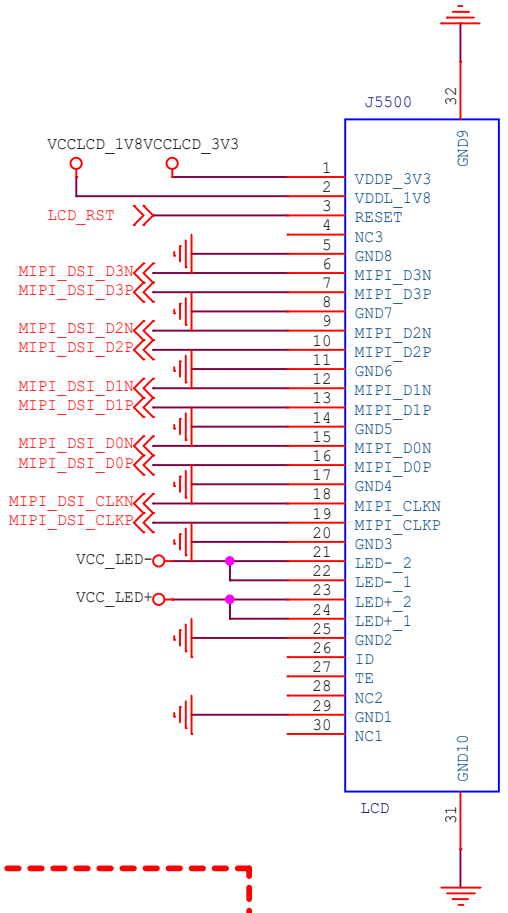
Indicate LED

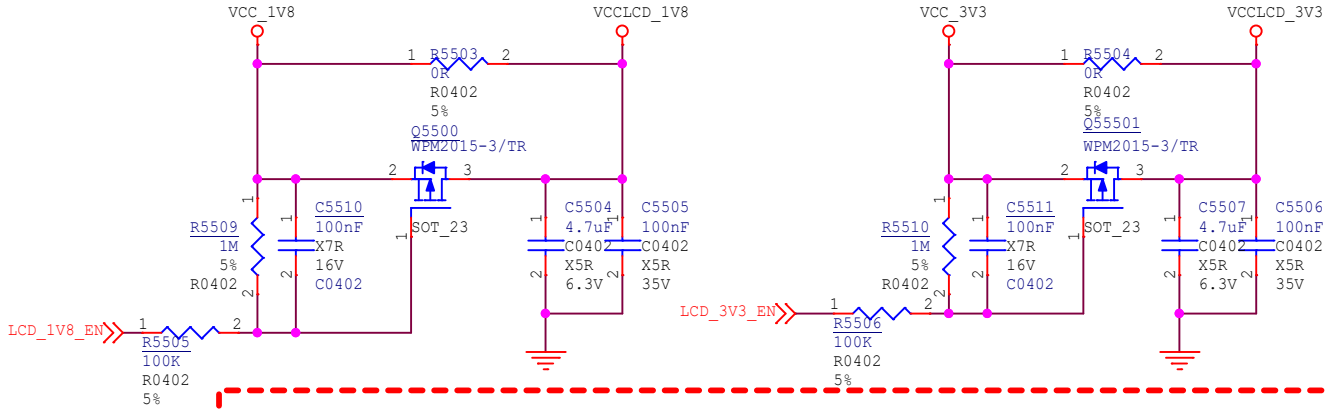


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	49.LED Driver				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	28 of 37

LCD

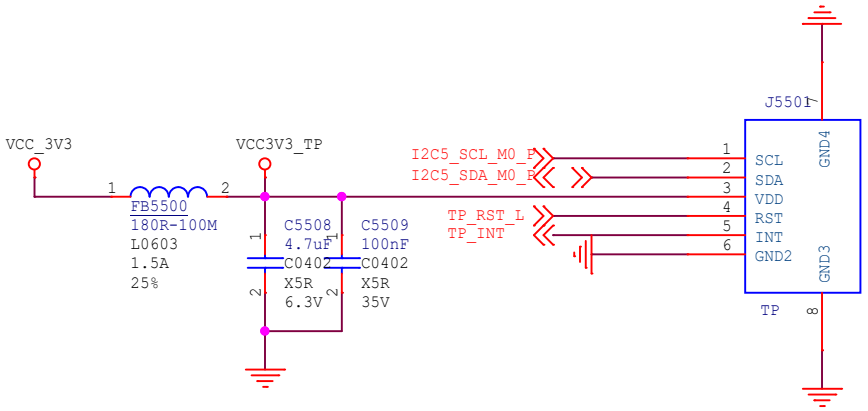






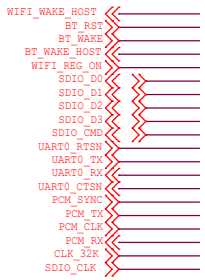
NOTE: The MOS and GPIO are used to control the time-sequence for some LCDs.
If there isn't TF card funtion, then the LDO9 of RK809-2 can supply power for VCCLCD_3V3.
Then the MOS control circuit can be deleted for VCCLCD_3V3.

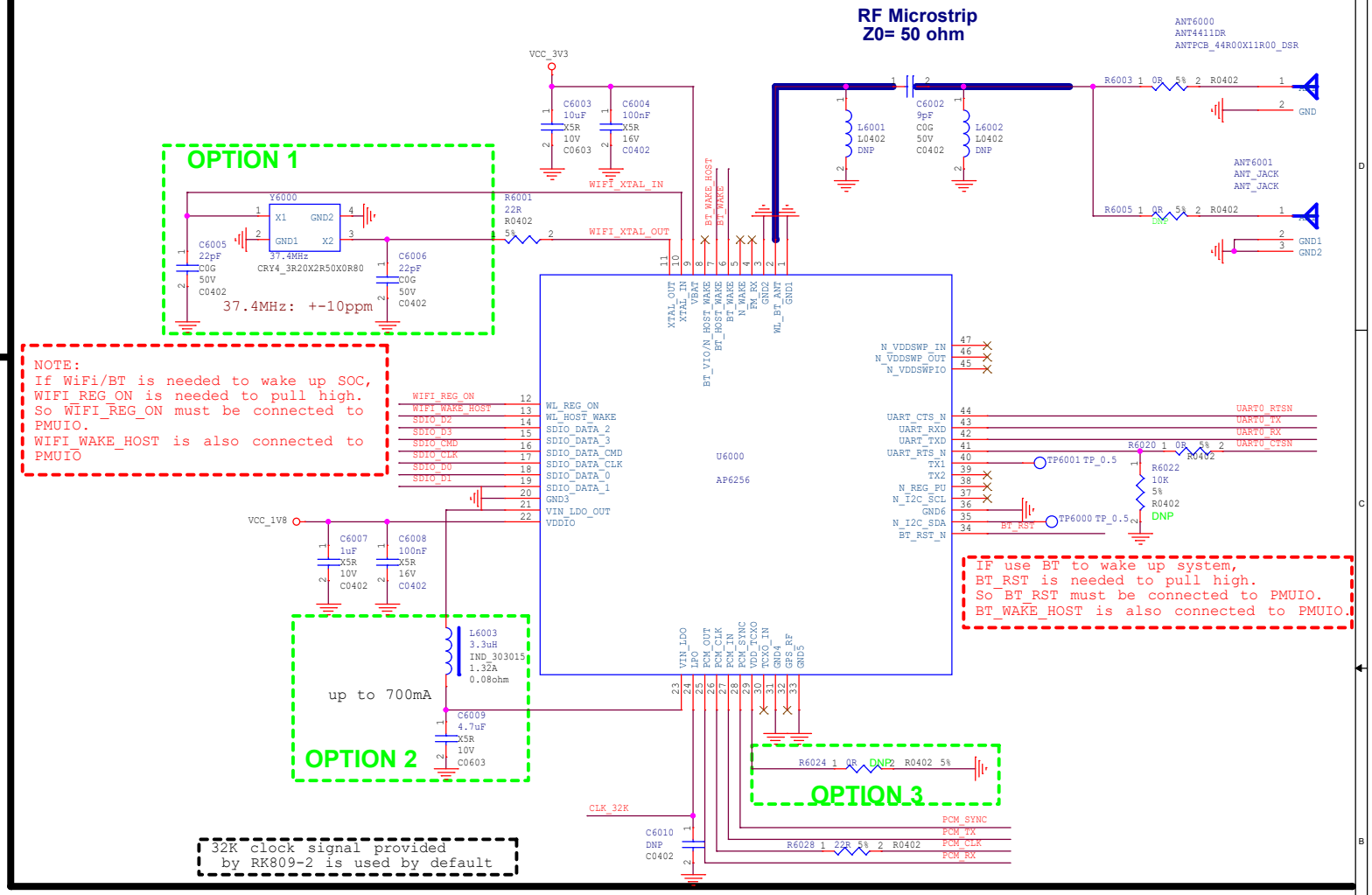
TP



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	49.IRC/Motor Driver				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	29 of 37

WIFI/BT Module





WIFI module		
Pin	AP6255	UWE5622
6	BT_WAKE	CHIP EN
7	BT_HOST_WAKE	AP_INT
12	WL_REG_ON	RST_N
13	WL_HOST_WAKE	SD_INT

Note:
Yes: option circuit be mounted
No: option circuit not be mounted

OPTION	WIFI				BT	Crystals	VCCIO_SDIO	OPTION1	OPTION2	OPTION3
	a	b/g/n	ac	5GHz						
AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71-3.63V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.63V	Yes	Yes	No
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.62-3.63V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0
RTL8189FTV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.63V	No	No	No
QCA9377 Module 8223A-SR	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No
UWE5622	Yes	Yes	Yes	Yes	5.0	Module Integrated	1.62-1.98V	No	No	No

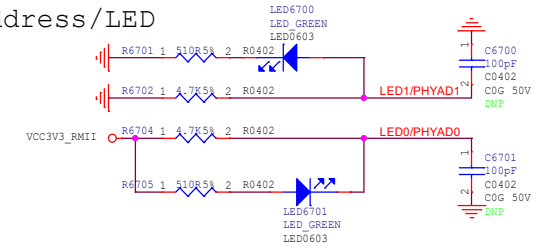
Rockchip 瑞芯微电子 Rockchip Electronics Co., Ltd

Project:	RV1126_RV1109 GATE REF			
File:	60.WIFI/BT-SDIO_1T1R+UART			
Date:	Thursday, August 20, 2020		Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by: <Checker>	Sheet:	30 of 37

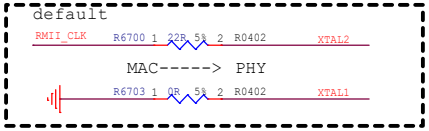
PHY

RMII_TXD0
RMII_TXD1
RMII_TXEN
RMII_RXDV
RMII_RXER
RMII_RXD0
RMII_RXD1
RMII_MDIO
RMII_MDC
RMII_CLK
EPHY_RSTn

PHY Address/LED



default



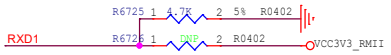
1. No crystal:
R6700,R6703,R6712, R6724 are sodered.
R6708,Y6700,C6702,C6703,R6717 are DNP.

2. With crystal
R6700,R6703,R6712, R6724 are DNP.
R6708,Y6700,C6702,C6703,R6717 are soldered.

MII/RMII Selection

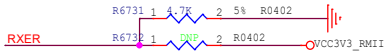
Pull High for RMII mode(default)

WOL/LED0 Selection



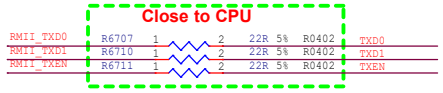
Pull Low for LED0 Mode(default)
Pull High for WOL Mode
WOL:Wake-on-LAN

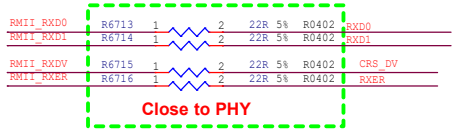
UTP / Fiber Selection



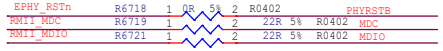
Pull Low for UTP Mode(default)
Pull High for Fiber Mode

Close to CPU

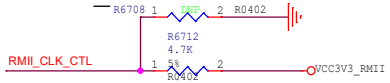




Close to PHY



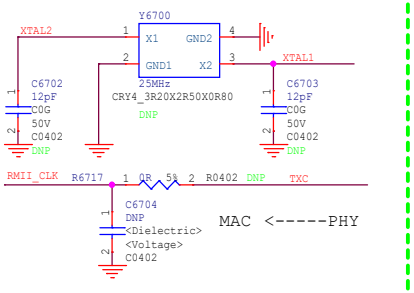
RMII REF_CLK direction

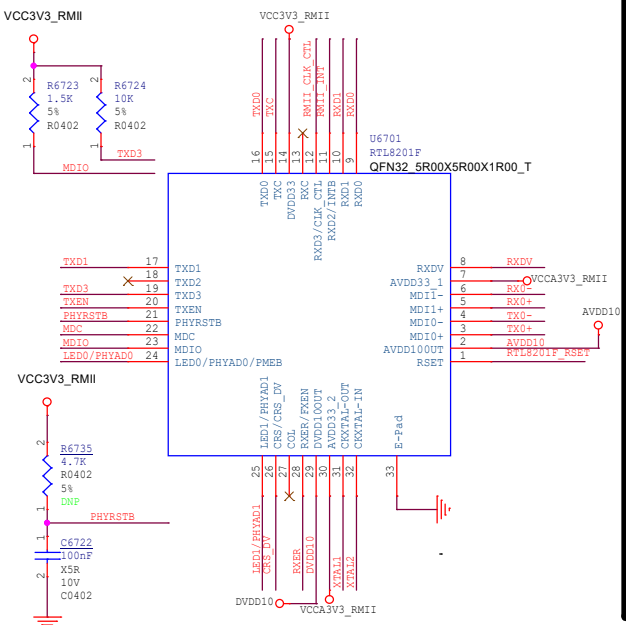


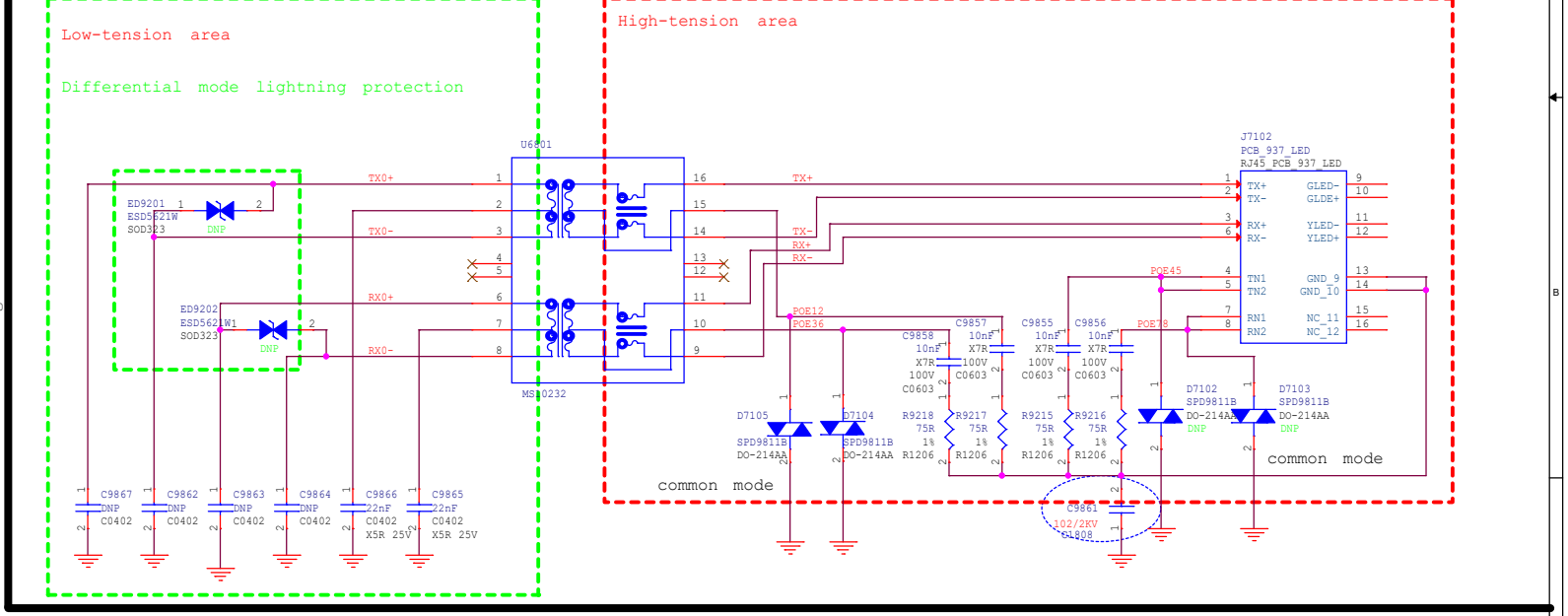
Pull Low for RMII REF_CLK Output mode
Pull High for RMII REF_CLK Input mode

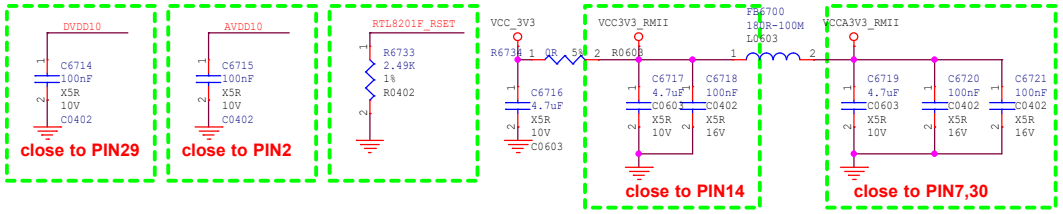
This pin is pulled high by an external 4.7Kohm.
This pin is used for the interrupt function only when in the RMII mode.

OPTION1





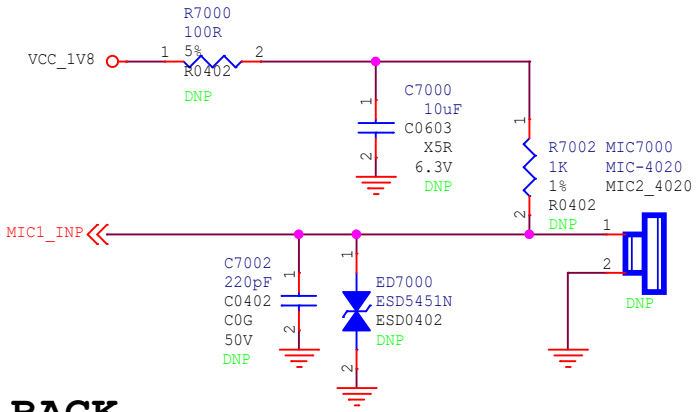




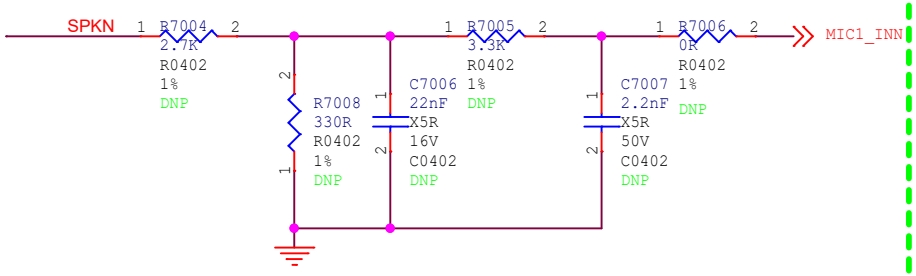
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RV1126_RV1109 GATE REF		
File:	67.Ethernet-EPHY_RMII		
Date:	Thursday, August 20, 2020	Rev:	V1.3
Designed by:		Sheet:	31 of 37

OPTION1: single end MIC, single loopback

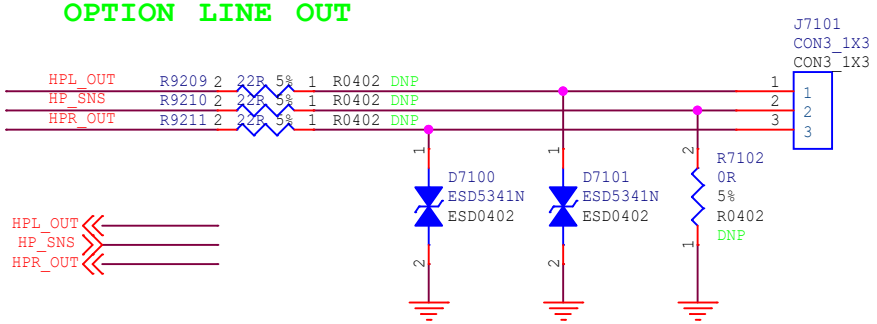
MIC



LOOP BACK

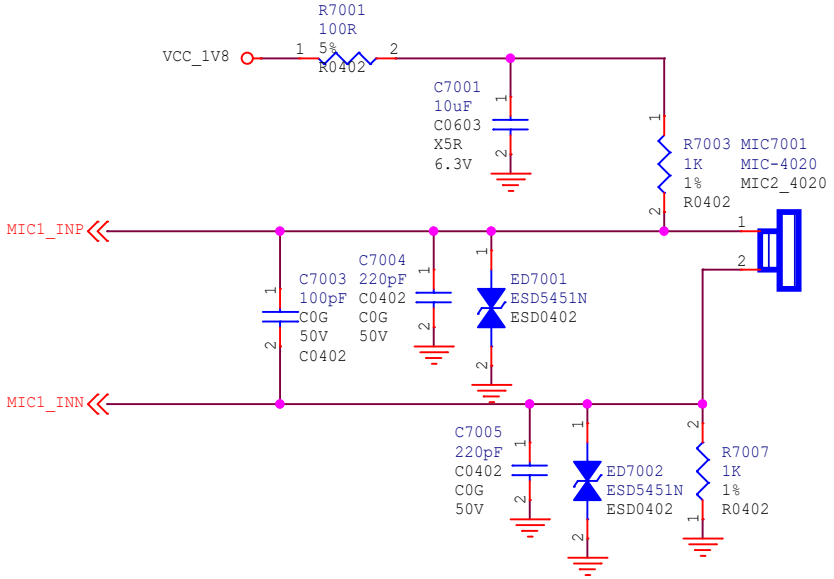


OPTION LINE OUT

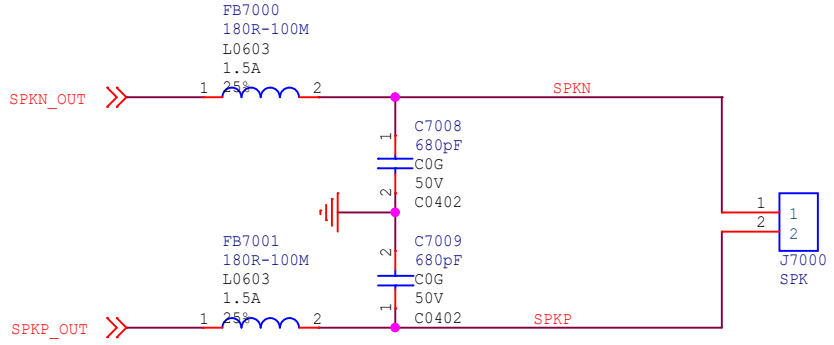


DEFAULT: no loopback, use differential MIC

Differential MIC



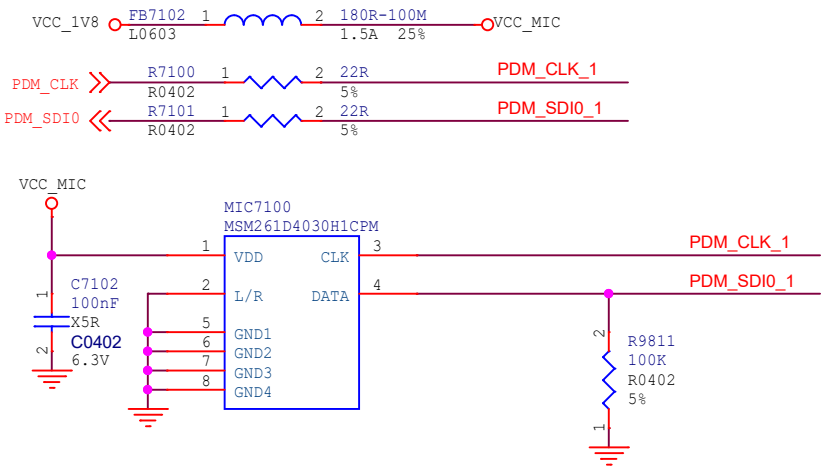
RK809-2 SPK OUT



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	70.Audio Port1				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	32 of 37

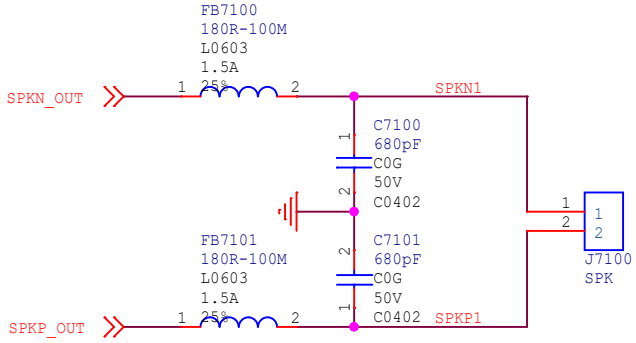
OPTION:
PDM MIC + RK809-2 SPK OUT+Differential LOOP BACK

PDM MIC

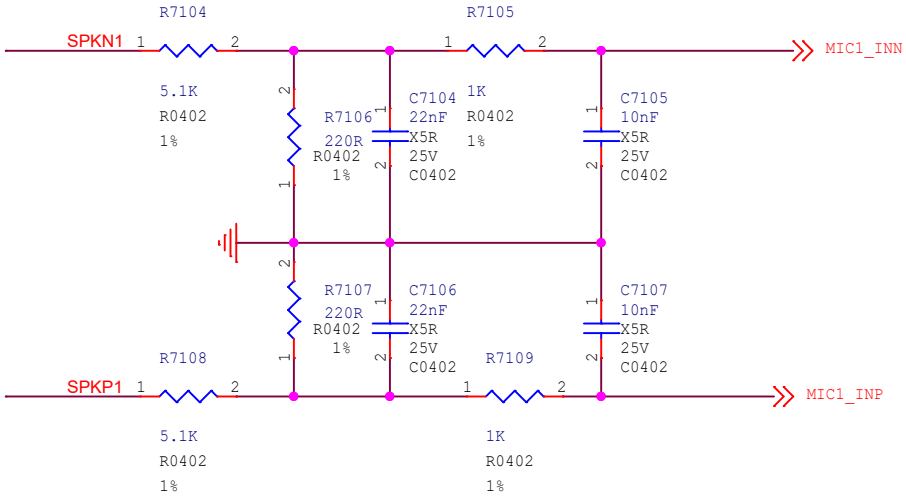


NOTE:
The SDI line should have a 100kohm PD resistor to discharge the line during the time that all microphones on the bus have tristated their outputs.

RK809-2 SPK OUT

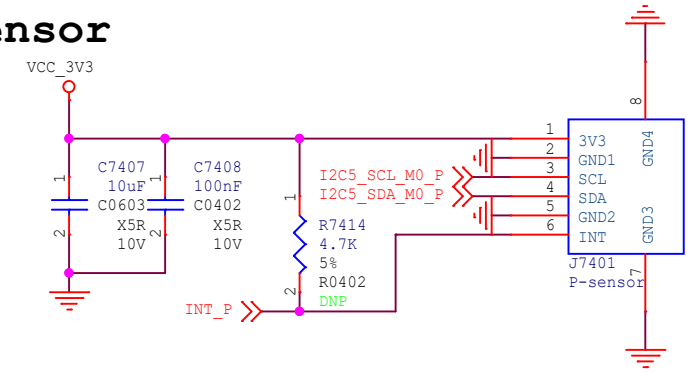


Differential LOOP BACK



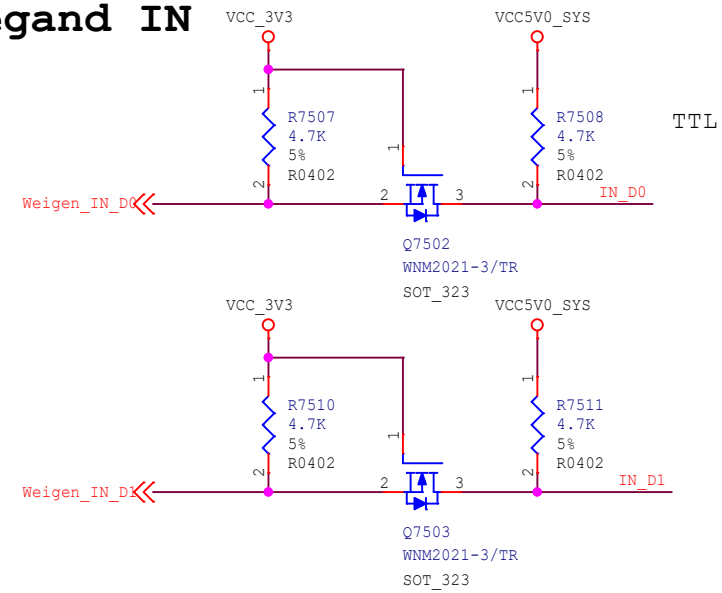
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	71.Audio Port2(MIC option)				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	33 of 37

P-sensor

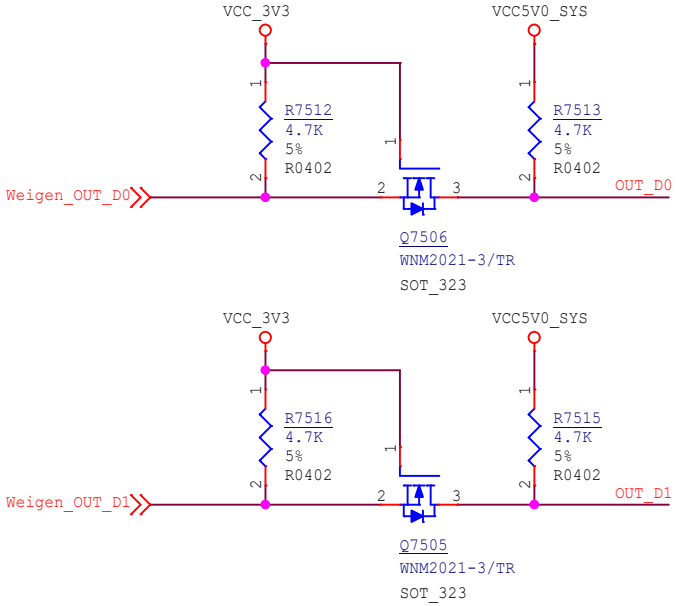


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	74.P-sensor Connector				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	34 of 37

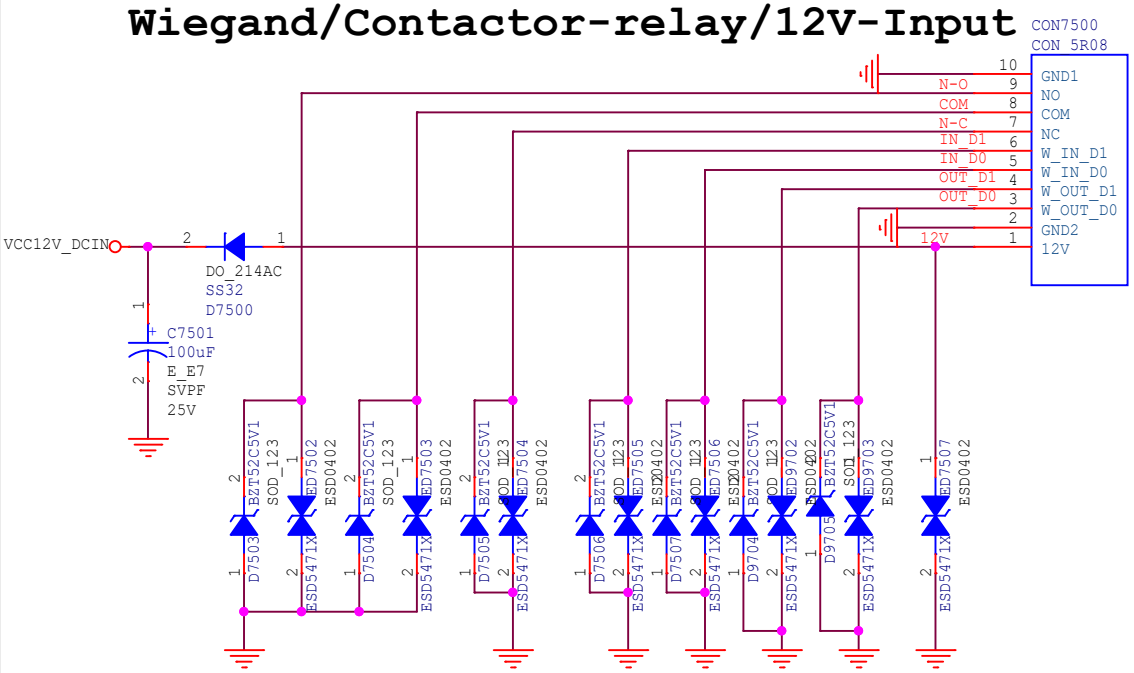
Wiegand IN



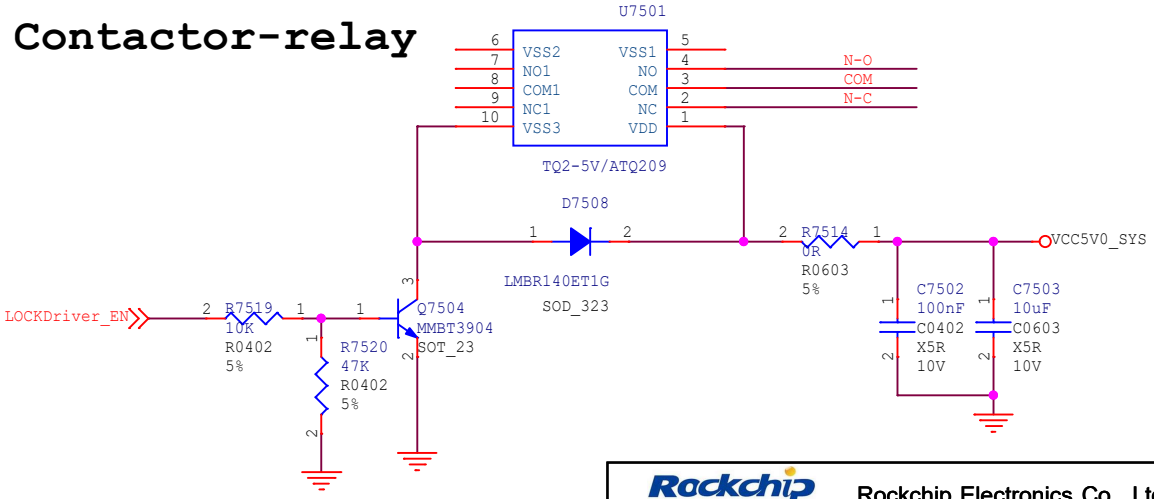
Wiegand OUT



Wiegand/Contactor-relay/12V-Input

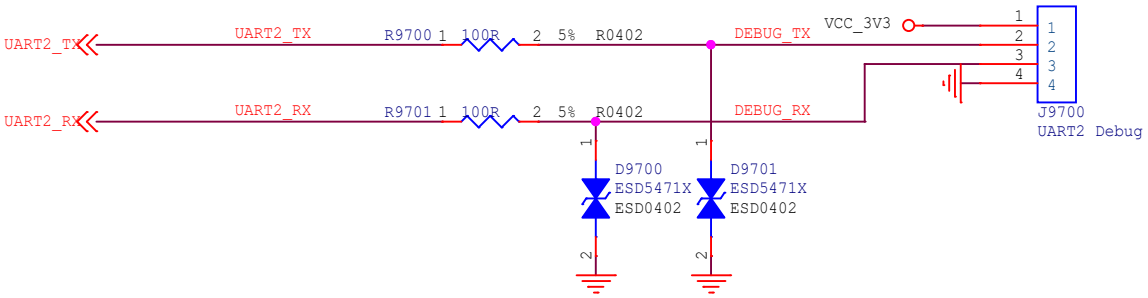


Contactor-relay

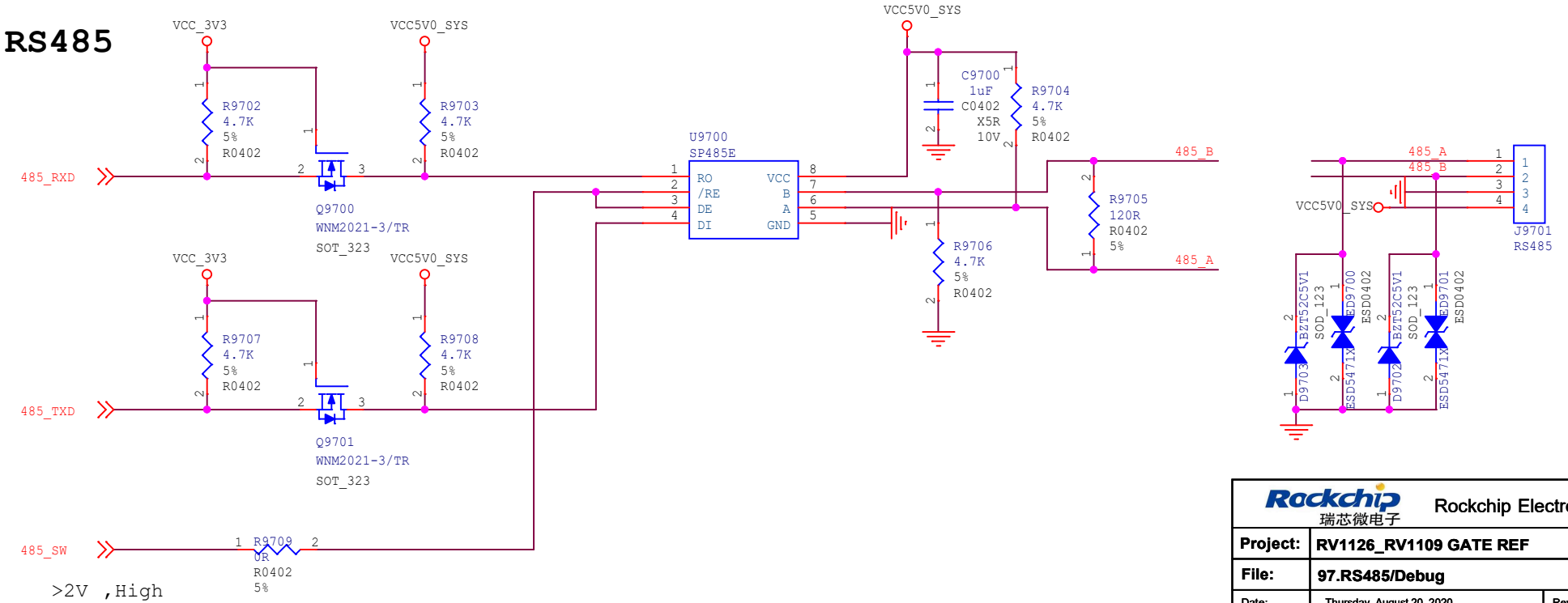


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	75.Wiegand/12V-Input				
Date:	Thursday, August 20, 2020			Rev:	V1.3
Designed by:	Yanhong.Li	Reviewed by:	<Checker>	Sheet:	35 of 37

UART DEBUG



RS485



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	97.RS485/Debug				
Date:	Thursday, August 20, 2020			Rev:	V1.3
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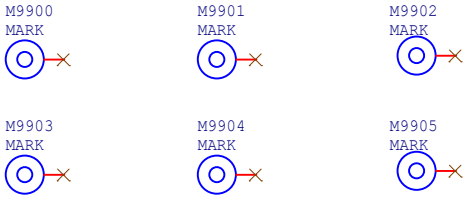

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 GATE REF				
File:	99.MARK/HOLE				
Date:	Thursday, August 20, 2020			Rev:	V1.3
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