RV1126_RV1109_USB_AI_Camera_DEMO_DDR3P216DD6_V15

Main Functions Introduction

01) Power: Discrete power supply
02) DRAM: DDR3 4Gb x 2
03) ROM: eMMC 8GB/SPI nand 512MB
04) Support USB2.0 OTG
05) Support MIPI CSI RX
06) Support Motor Dricer Control
07) Support Option MIC Array
08) Support Debug

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Index and Notes

Table of Content

Note

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Graphic Description

Rockchip Confidential

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Project:	RV1126_RV1109 AI Camera				
File:	01.Index and Notes				
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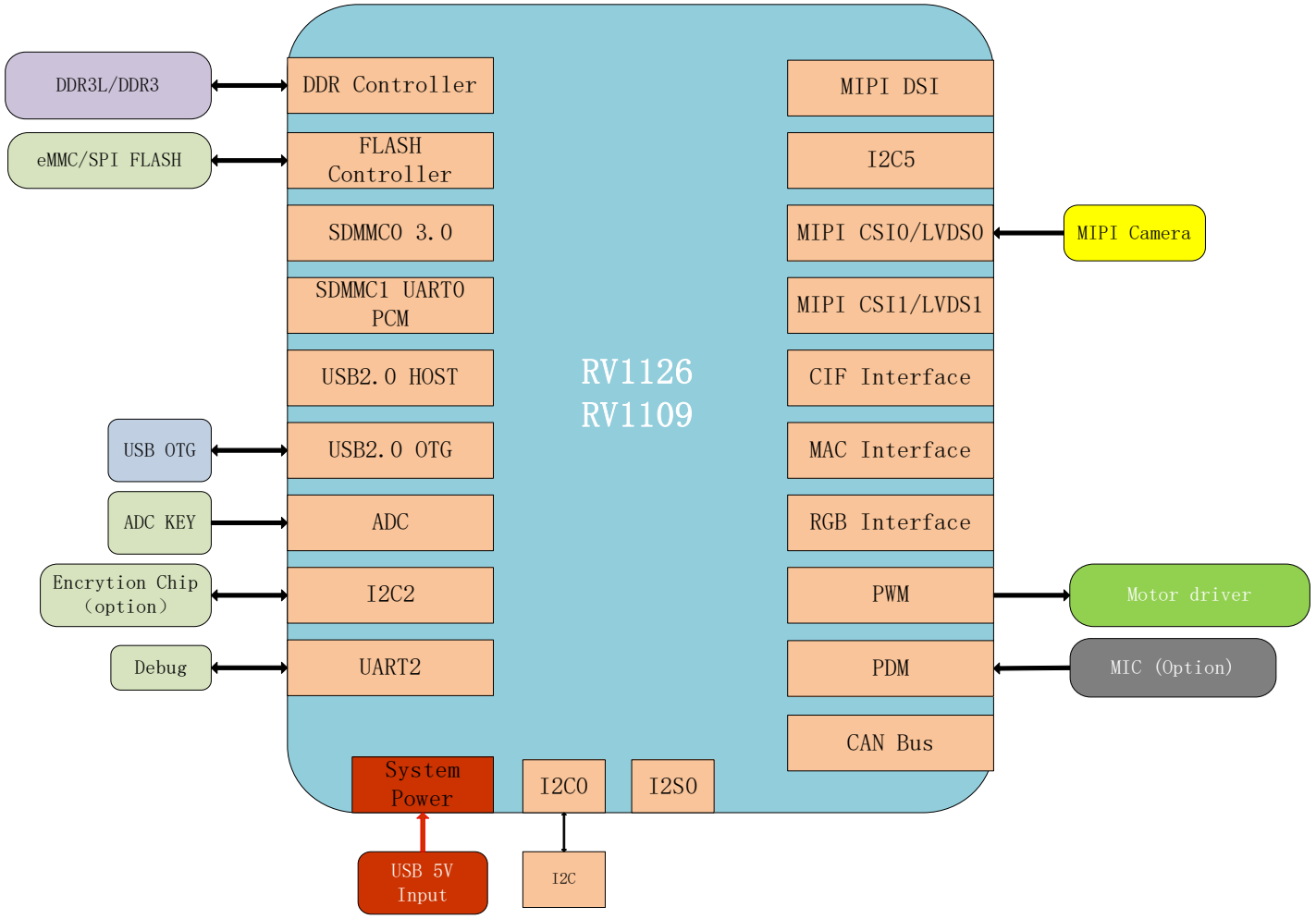
Revision History

Version	Date	Author	Change Note	Approved
V1.0	2020.03.30	whb	First edition AI Camera for RV1126/1109	
V1.1	2020.07.22	whb	Modify the VCC_1V2 and VCC_3V3 power path	
V1.2	2020.08.20	whb	Add power sleep control signal and other	
V1.3	2020.10.30	whb	Optimize 1.8V power supply	
V1.4	2020.12.21	whb	Modify the VDD_LOG power and improve the USB OTG signal	
V1.5	2021.02.07	whb	Modify the reset IC model、power on timing and add power IC model	

RV1126_RV1109 Block Diagram



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Project:	RV1126_RV1109 AI Camera				
File:	03.Block Diagram				
Date:	Sunday, February 07, 2021			Rev:	V1.5
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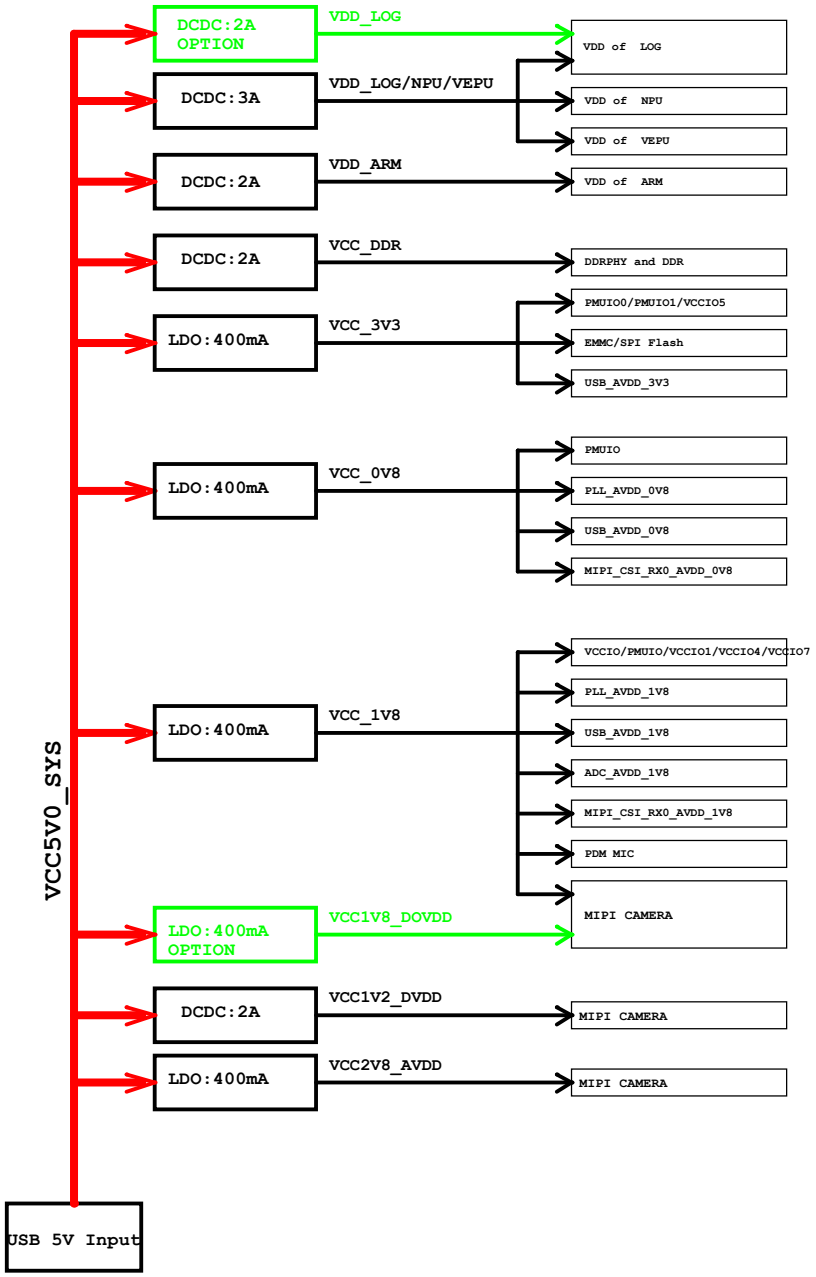
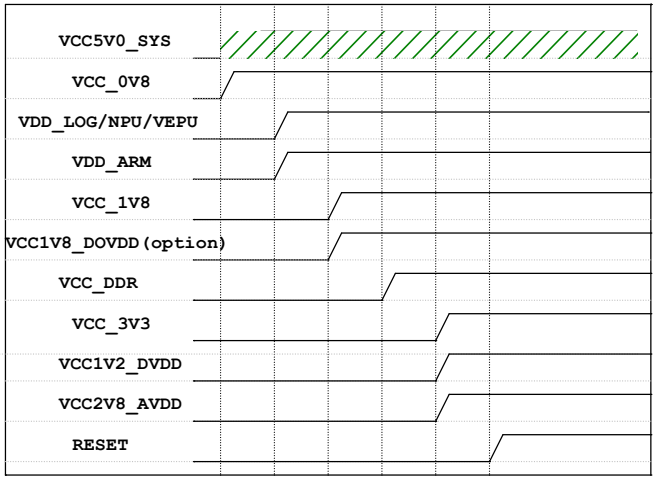
Power Diagram



Power-on Sequence

Power Name	PMIC Channel	Time Slot (step 6ms)	Default voltage	Supply Limit	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC_0V8	LDO	Slot: 1	0.8V	0.4A	ON	ON		
VDD_LOG/NPU/VEPU	BUCK	Slot: 2	0.825V	3.0A	ON	ON		
VDD_ARM	BUCK	Slot: 2	0.824V	2.0A	ON	ON		
VCC_1V8	LDO	Slot: 3	1.8V	0.4A	ON	ON		
VCC1V8_DOVDD(option)	LDO	Slot: 3	1.8V	0.4A	ON	ON		
VCC_DDR	BUCK	Slot: 4	1.35V	1.0A	ON	ON		
VCC_3V3	LDO	Slot: 5	3.3V	0.4A	ON	ON		
VCC1V2_DVDD	BUCK	Slot: 5	1.2V	1.0A	ON	ON		
VCC2V8_AVDD	LDO	Slot: 5	2.8V	0.4A	ON	ON		



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Project:	RV1126_RV1109 AI Camera				
File:	04.Power Diagram and Sequence				
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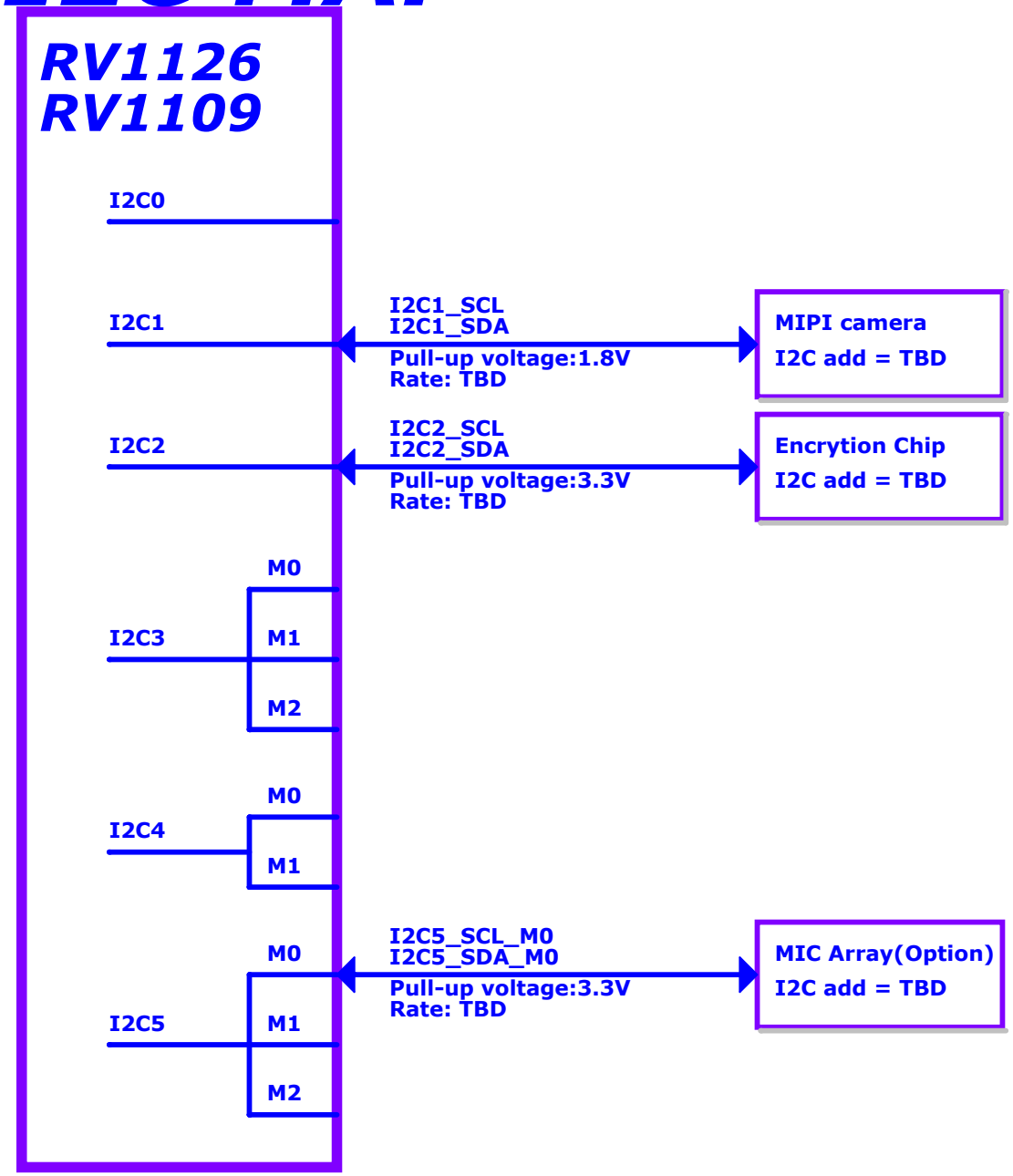
I2C MAP



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Project:	RV1126_RV1109 AI Camera				
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IO Power Domain Map

IO Domain	IO Group	Support of IO Voltage		Default Actual assigned IO Domain Voltage			Notes
		1.8V	3.3V	Net Name of Power Supply	Power Source	Voltage	
PMUIO0	***GPIO0A***	✓	✓	*VCC_3V3*		*3.3V*	
PMUIO1	***GPIO0BC***	✓	✓	*VCC_3V3*		*3.3V*	
VCCIO1	***GPIO0CD/GPIO1A***	✓	✓	*VCCIO_FLASH*		*1.8/3.3V*	*GPIO0_B3/FLASH_VOL_SEL pin defined as a set pin for VCCIO1 voltage domain after power-on reset.It is pull-up for 1.8V*
VCCIO2	***GPIO1AB***	✓	✓	*NC*			
VCCIO3	***GPIO1BCD***	✓	✓	*NC*			
VCCIO4	***GPIO1D/GPIO2A***	✓	✓	*VCC_1V8*		*1.8V*	
VCCIO5	***GPIO2ABCD/GPIO3A***	✓	✓	*VCC_3V3*		*3.3V*	
VCCIO6	***GPIO3ABC***	✓	✓	*NC*			
VCCIO7	***GPIO3D/GPIO4A***	✓	✓	*VCC_1V8*		*1.8V*	

Power

U1000N
RV1126_RV1109
BGA409_14R00X14R00X0R90

NPU/LOGIC/VEPU/ARM Power

NPU_VDD_1	H11	VDD_NPU/VEPU
NPU_VDD_2	H12	
NPU_VDD_3	J10	
NPU_VDD_4	J11	
NPU_VDD_5	K10	
NPU_VDD_6	K11	
LOGIC_VDD_1	H9	VDD_LOG
LOGIC_VDD_2	J9	
LOGIC_VDD_3	L10	
LOGIC_VDD_4	M11	
LOGIC_VDD_5	H13	
LOGIC_VDD_6	J13	
VEPU_VDD_1	L9	VDD_NPU/VEPU
VEPU_VDD_2	M9	
VEPU_VDD_3	N8	
VEPU_VDD_4	N9	
ARM_VDD_1	N12	VDD_ARM
ARM_VDD_2	P12	
ARM_VDD_3	P13	

Supply for VCCIO1~7 Power

VCCIO_VDD_1V8 H14 — R1000 3.3R R0402 5% — VCC_1V8

C1022 1nF X5R 50V C0402
C1000 100nF X5R 6.3V C0402

VDD_LOG
Close to VDD_LOG
C1001 10uF X5R 6.3V C0603
C1002 1uF X5R 6.3V C0402
C1003 1uF X5R 6.3V C0402
C1004 100nF X5R 6.3V C0402
C1005 100nF X5R 6.3V C0402

VDD_NPU/VEPU
Close to VDD_NPU
C1006 10uF X5R 6.3V C0603
C1007 1uF X5R 6.3V C0402
C1008 1uF X5R 6.3V C0402
C1009 100nF X5R 6.3V C0402
C1010 100nF X5R 6.3V C0402
C1011 100nF X5R 6.3V C0402

VDD_NPU/VEPU
Close to SOC
C1020 22uF X5R 6.3V C0603
C1021 22uF X5R 6.3V C0603

VDD_ARM
Close to VDD_ARM
C1012 10uF X5R 6.3V C0603
C1013 1uF X5R 6.3V C0402
C1014 100nF X5R 6.3V C0402
C1015 100nF X5R 6.3V C0402

VDD_NPU/VEPU
Close to VDD_VEPU
C1016 10uF X5R 6.3V C0603
C1017 1uF X5R 6.3V C0402
C1018 100nF X5R 6.3V C0402
C1019 100nF X5R 6.3V C0402

GND

U1000O
RV1126_RV1109
BGA409_14R00X14R00X0R90

VSS/AVSS

A1	VSS_1		VSS_53	K9	
A21	AVSS_2		VSS_54	K12	
B12	VSS_3		VSS_55	K13	
C3	VSS_4		VSS_56	K14	
C5	VSS_5		VSS_57	L2	
C7	VSS_6		VSS_58	L5	
C10	VSS_7		VSS_59	L6	
C12	VSS_8		VSS_60	L11	
D9	VSS_9		VSS_61	L12	
D12	VSS_10		VSS_62	L13	
D18	AVSS_11		VSS_63	L14	
E4	VSS_12		VSS_64	L16	
E6	VSS_13		VSS_65	M3	
E8	VSS_14		VSS_66	M5	
E9	VSS_15		VSS_67	M7	
E10	VSS_16		VSS_68	M8	
E11	VSS_17		VSS_69	M10	
E12	VSS_18		VSS_70	M12	
F3	VSS_19		VSS_71	M13	
F5	VSS_20		VSS_72	M14	
F7	VSS_21		VSS_73	M16	
F8	VSS_22		VSS_74	N5	
F9	VSS_23		VSS_75	N6	
F10	VSS_24		VSS_76	N7	
F11	VSS_25		VSS_77	N10	
F12	VSS_26		VSS_78	N11	
F13	VSS_27		VSS_79	N13	
F14	AVSS_28		VSS_80	N14	
F15	AVSS_29		VSS_81	N16	
G2	VSS_30		VSS_82	P5	
G5	VSS_31		VSS_83	P7	
G6	VSS_32		VSS_84	P8	
G10	VSS_33		VSS_85	P9	
G11	VSS_34		VSS_86	P14	
G12	VSS_35		VSS_87	P16	
G13	VSS_36		VSS_88	R1	
G16	AVSS_37		VSS_89	R5	
G17	AVSS_38		VSS_90	R12	
H4	VSS_39		VSS_91	R13	
H5	VSS_40		VSS_92	R14	
H6	VSS_41		VSS_93	T6	
H7	VSS_42		VSS_94	T9	
H10	VSS_43		VSS_95	T10	
H15	VSS_44		VSS_96	T14	
J5	VSS_45		VSS_97	T17	
J6	VSS_46		VSS_98	V17	
J12	VSS_47		VSS_99	W9	
J14	VSS_48		VSS_100	W14	
J16	VSS_49		VSS_101	AA1	
K5	VSS_50		VSS_102	AA10	
K6	VSS_51		VSS_103	AA21	
K8	VSS_52				

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File:	10.RV1126/1109_Power/GND			
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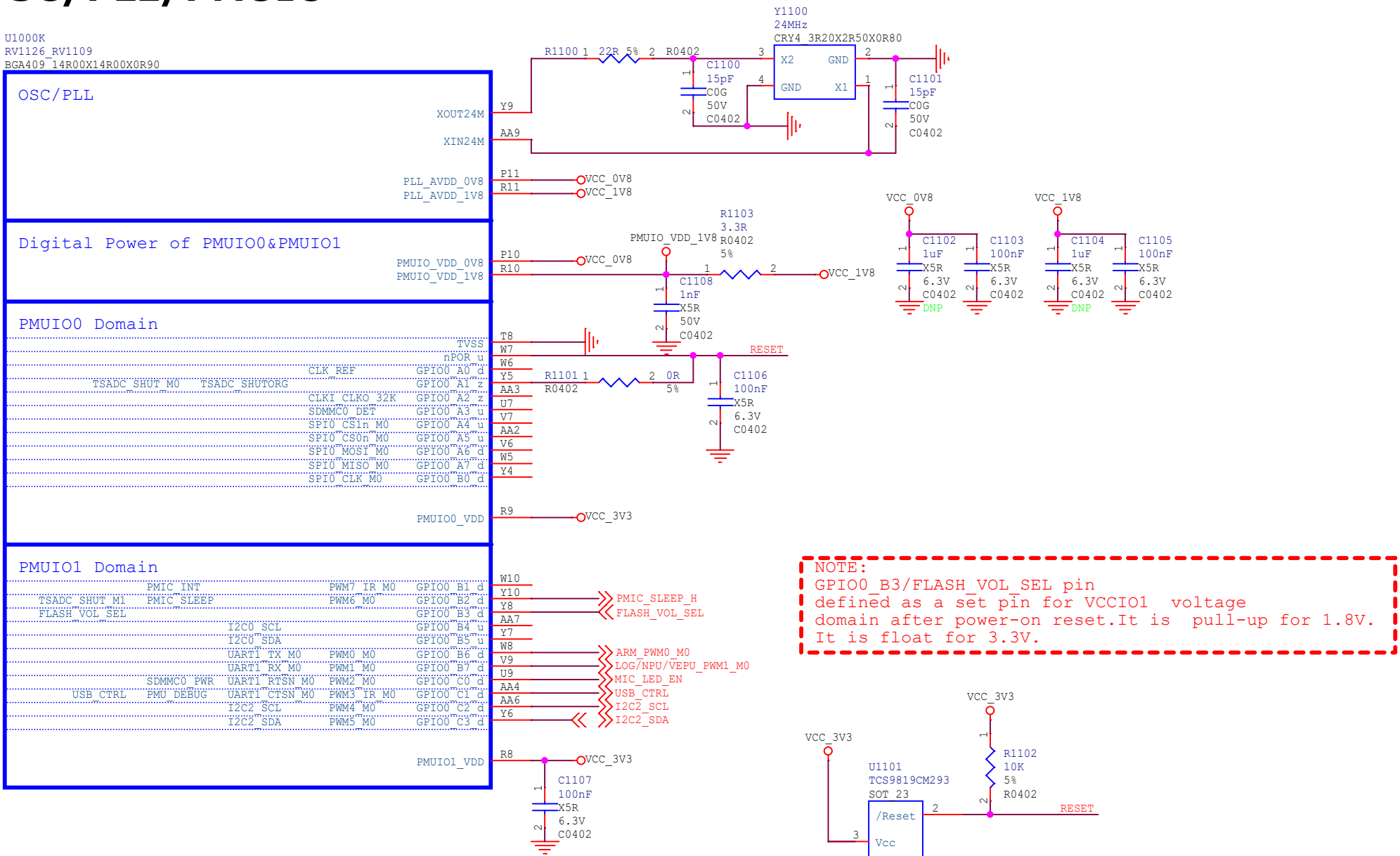
OSC/PLL/PMUIO



NOTE:
GPIO0_B3/FLASH_VOL_SEL pin
defined as a set pin for VCCIO1 voltage
domain after power-on reset.It is pull-up for 1.8V.
It is float for 3.3V.

RESET IC

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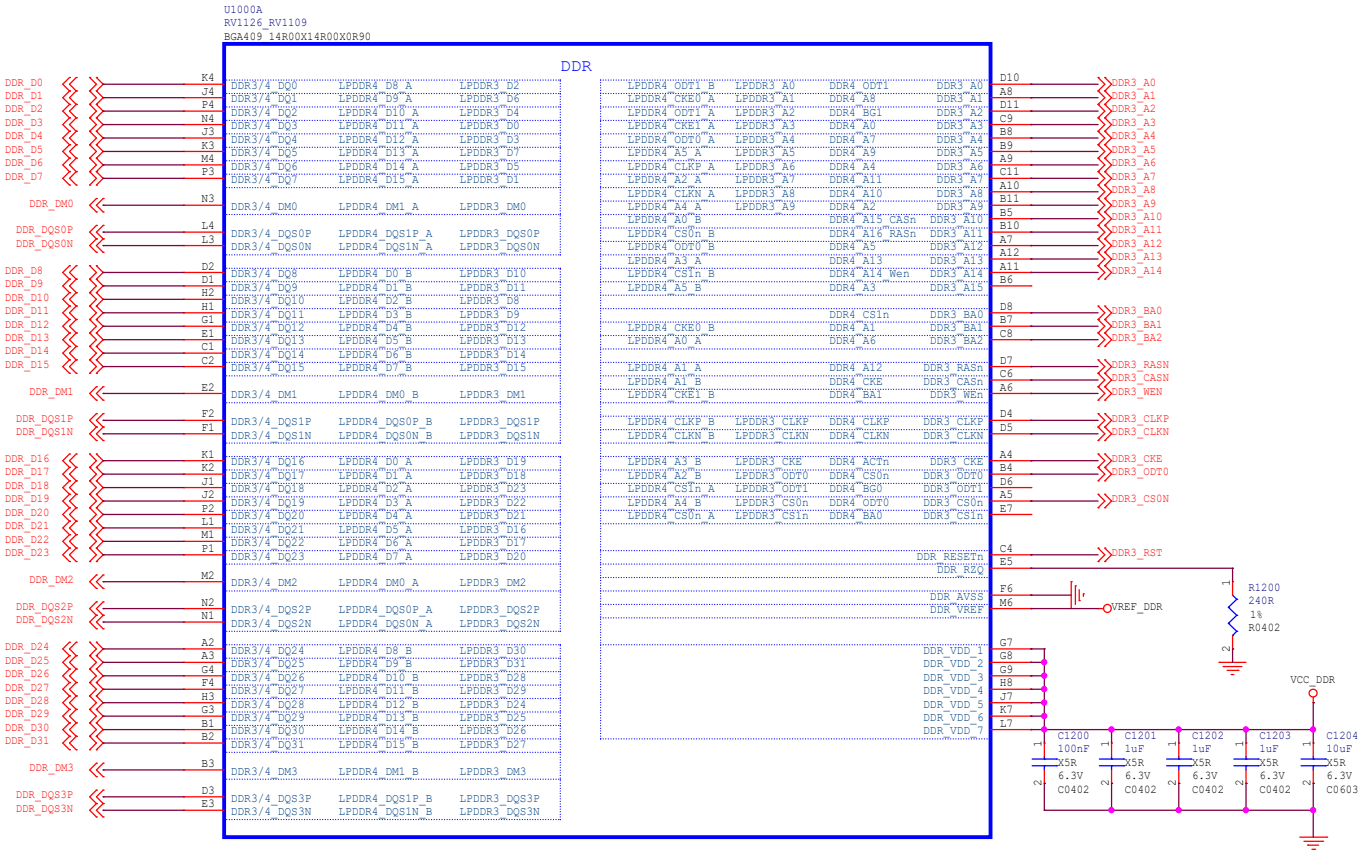
Project:	RV1126_RV1109 AI Camera		
File:	11.RV1126/1109_OSC/PLL/PMUIO		
Date:	Sunday, February 07, 2021	Rev:	V1.5
Designed by: whb	Reviewed by:	Sheet:	9 of 28

DDR Controller



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Project:	RV1126_RV1109 AI Camera				
File:	12.RV1126/1109_DRAM Controller				
Date:	Sunday, February 07, 2021			Rev:	V1.5
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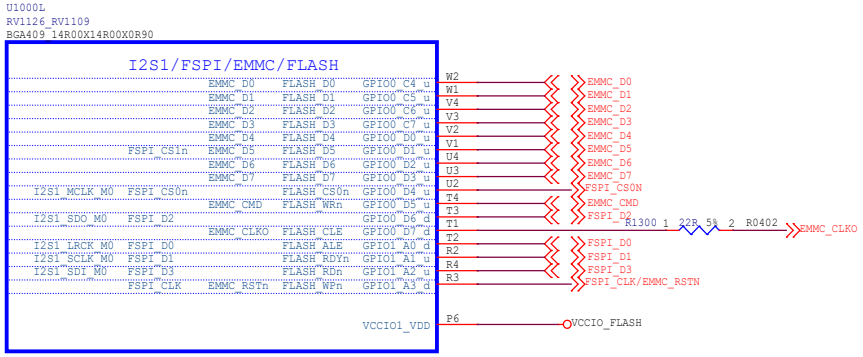
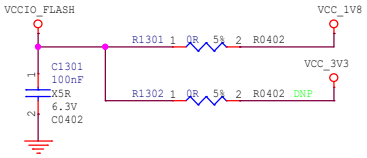
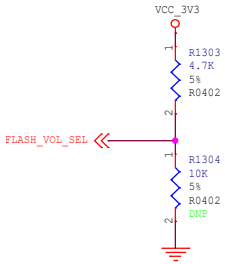
EMMC/FLASH



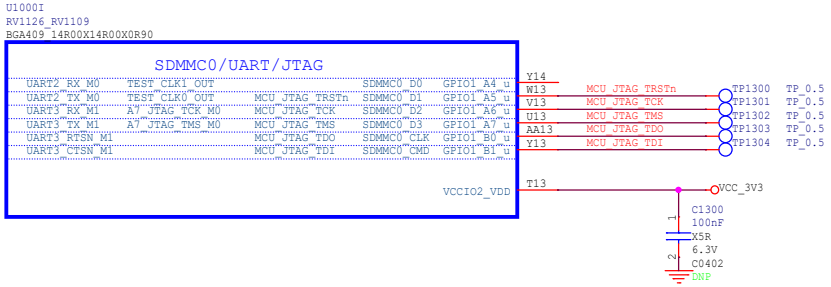




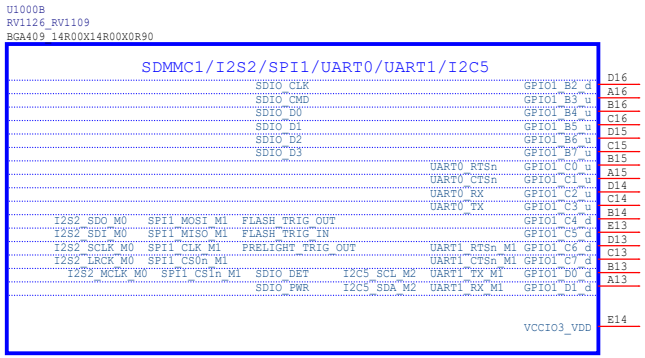
NOTE:
FLASH(VCCIO1) power domain IO supply configuration pin:

Condition	VCCIO1 (VCCIO_FLASH)
FLASH_VOL_SEL=0	3.3V
FLASH_VOL_SEL=1	1.8V Default

SDMMC0/JTAG



SDMMC1/UART/I2S2



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Project:	RV1126_RV1109 AI Camera				
File:	13.RV1126/1109_Flash/SD				
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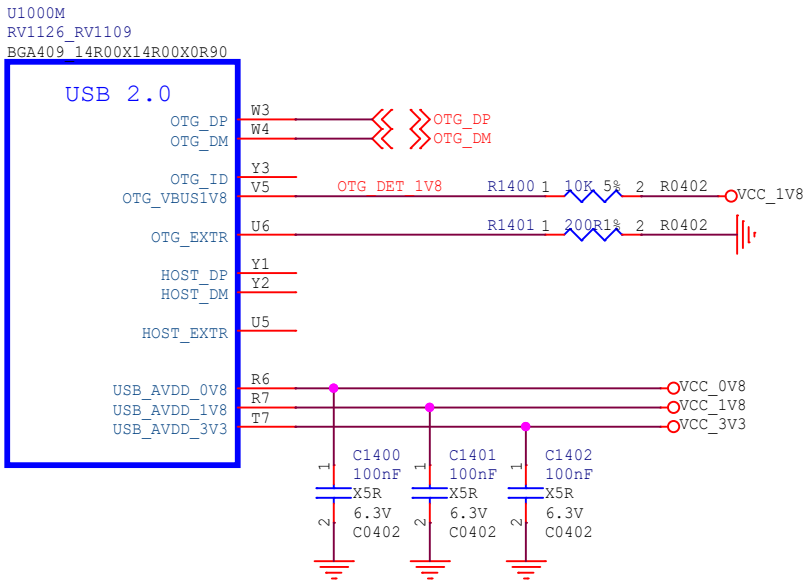
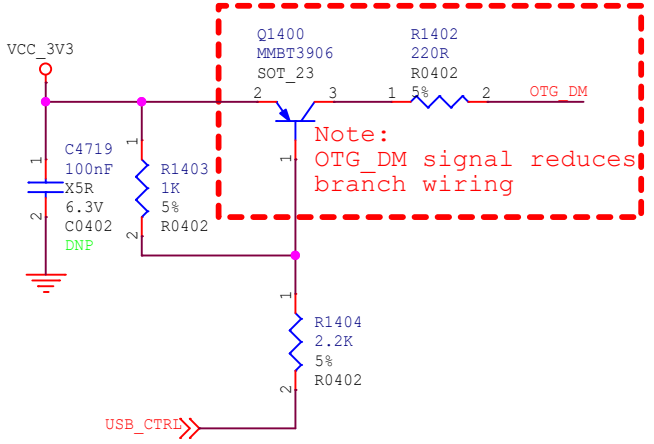
USB Controller





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Project:	RV1126_RV1109 AI Camera				
File:	14.RV1126/1109_USB Controller				
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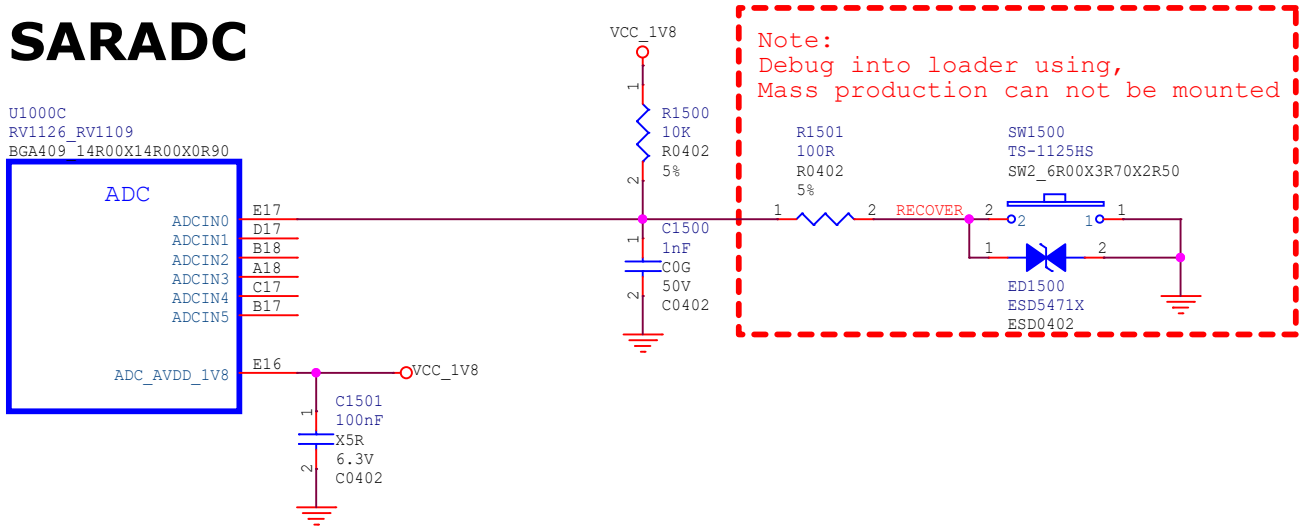
SARADC



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Project:	RV1126_RV1109 AI Camera				
File:	15.RV1126/1109_SARADC				
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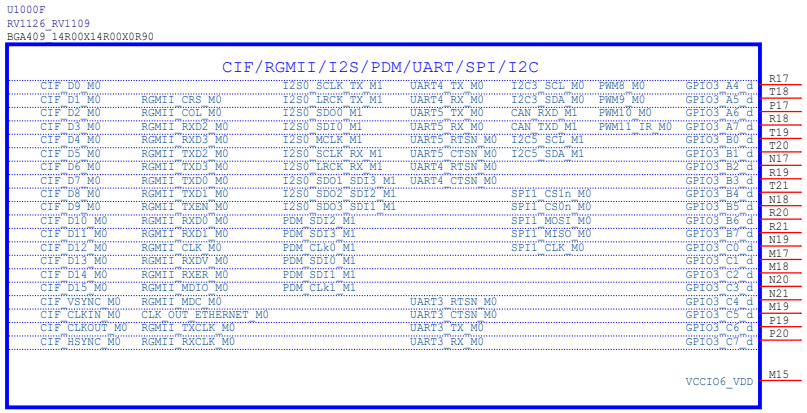
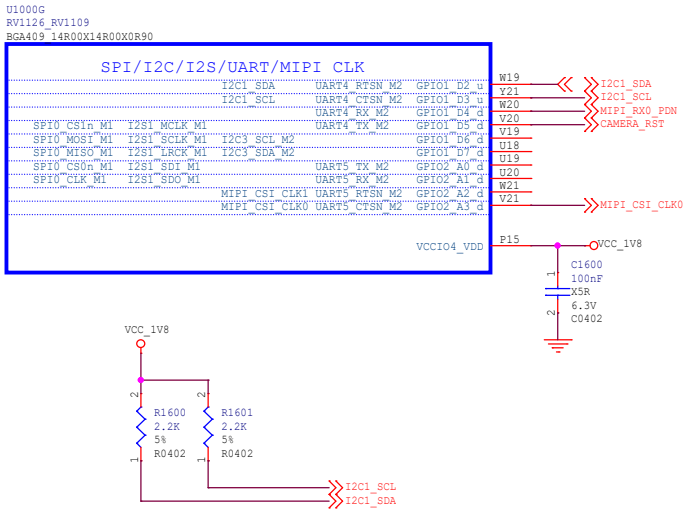
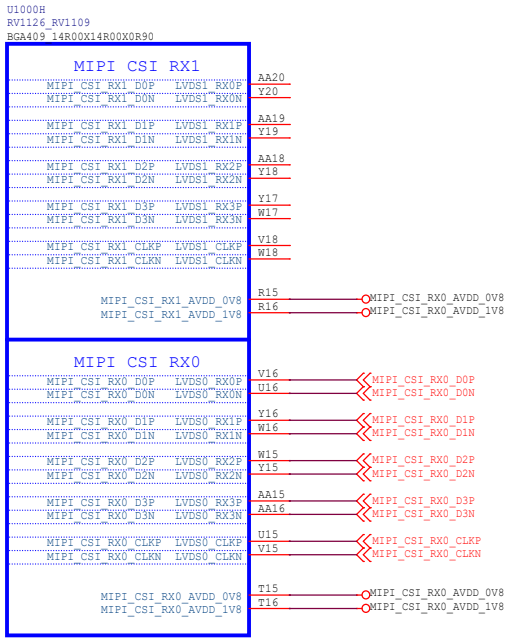
CIF Interface

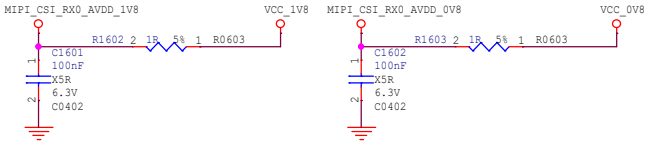


I2C/SPI/MIPI-CLK



MIPI-CSI Interface





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Project:	RV1126_RV1109 AI Camera				
File:	16.RV1126/1109_VideoInput				
Date:	Sunday, February 07, 2021			Rev:	V1.5
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LCDC/RGMII/PWM

U1000E
RV1126_RV1109
BGA409_14R00X14R00X0R90

LCDC/RGMII/CIF/UART/JTAG/I2S/SPI/I2C

		UART4_RTSN_M1		RGMII_TXD3_M1	CIF_D0_M1	LCDC_D0	GPIO2_A4_d	J18
I2C5_SCL_M0		UART4_CTSN_M1		RGMII_CRS_M1	CIF_D1_M1	LCDC_D1	GPIO2_A5_d	L17
		UART4_TX_M1	PWM5_M1	RGMII_COL_M1	CIF_D2_M1	LCDC_D2	GPIO2_A6_d	M21
	I2S2_SDO_M1	UART4_RX_M1	PWM4_M1	SPI0_CS0n_M2		LCDC_D3	GPIO2_A7_d	M20
	I2S2_SDI_M1	UART5_TX_M1	PWM3_IR_M1	SPI0_MOSI_M2		LCDC_D4	GPIO2_B0_d	L19
	I2S2_SCLK_M1	UART5_RX_M1	PWM2_M1	SPI0_MISO_M2		LCDC_D5	GPIO2_B1_d	L20
	I2S2_LRCK_M1	UART5_RTSN_M1	PWM1_M1	SPI0_CLK_M2		LCDC_D6	GPIO2_B2_d	K16
I2C5_SDA_M0	I2S2_MCLK_M1	UART5_CTSN_M1	PWM0_M1	SPI0_CS1n_M2	CIF_D3_M1	LCDC_D7	GPIO2_B3_d	K17
				RGMII_RXDV_M1	CIF_D4_M1	LCDC_D8	GPIO2_B4_d	K18
				RGMII_RXD0_M1	CIF_D5_M1	LCDC_D9	GPIO2_B5_d	K19
				RGMII_RXD1_M1	CIF_D6_M1	LCDC_D10	GPIO2_B6_d	K20
				RGMII_CLK_M1	CIF_D7_M1	LCDC_D11	GPIO2_B7_d	K21
				RGMII_RXER_M1	CIF_D8_M1	LCDC_D12	GPIO2_C0_d	J19
				RGMII_MDIO_M1	CIF_D9_M1	LCDC_D13	GPIO2_C1_d	J21
				RGMII_MDC_M1	CIF_D10_M1	LCDC_D14	GPIO2_C2_d	J20
				RGMII_TXD0_M1	CIF_D11_M1	LCDC_D15	GPIO2_C3_d	H20
				RGMII_TXD1_M1	CIF_D12_M1	LCDC_D16	GPIO2_C4_d	H19
				CLK_OUT_ETHERNET_M1	CIF_D13_M1	LCDC_D17	GPIO2_C5_d	G21
				RGMII_TXEN_M1	CIF_D14_M1	LCDC_D18	GPIO2_C6_d	G20
	I2S1_MCLK_M2			RGMII_RXD2_M1	CIF_D15_M1	LCDC_D19	GPIO2_C7_d	G19
	I2S1_SDO_M2			RGMII_RXD3_M1	CIF_VSYNC_M1	LCDC_D20	GPIO2_D0_d	H18
	I2S1_SCLK_M2			RGMII_TXD2_M1	CIF_CLKOUT_M1	LCDC_D21	GPIO2_D1_d	F21
	I2S1_LRCK_M2			RGMII_TXCLK_M1	CIF_CLKIN_M1	LCDC_D22	GPIO2_D2_d	F20
	I2S1_SDI_M2			RGMII_RXCLK_M1	CIF_HSYNC_M1	LCDC_D23	GPIO2_D3_d	F19
I2C3_SCL_M1			PWM6_M1	SPI1_CS0n_M2		LCDC_DEN	GPIO2_D4_d	J17
I2C3_SDA_M1			PWM10_M1	SPI1_CLK_M2		LCDC_HSYNC	GPIO2_D5_d	H17
		UART3_RTSN_M2	PWM9_M1	SPI1_MOSI_M2		LCDC_VSYNC	GPIO2_D6_d	C21
		UART3_CTSN_M2	PWM8_M1	SPI1_MISO_M2		LCDC_CLK	GPIO2_D7_d	D21
I2C4_SCL_M0	CAN_RXD_M0	UART3_TX_M2	PWM7_IR_M1	SPI1_CS1n_M2			GPIO3_A0_u	E20
I2C4_SDA_M0	CAN_TXD_M0	UART3_RX_M2	PWM11_IR_M1				GPIO3_A1_u	E19
A7_JTAG_TCK_M1		UART2_TX_M1					GPIO3_A2_u	G18
A7_JTAG_TMS_M1		UART2_RX_M1					GPIO3_A3_u	H16

VCCIO5_VDD1 J15
VCCIO5_VDD2 K15

I2C5_SCL_M0
I2C5_SDA_M0
work_led R1700 1 510R5% 2 R0402
LED1700
LED_RED
LED0603
CAM_EN
Mot_EN_H
Mot_AEN/nEN_PWM6_M1
Mot_BEN/STEP_PWM10_M1
Mot_BPH/DIR_PWM9_M1
Mot_APH/M0_PWM8_M1
Mot_state/M1
Mot_nFAULT
UART2_TX
UART2_RX
VCC_3V3
C1700
100nF
X5R
6.3V
C0402
VCC_3V3

MIPI-DSI Interface

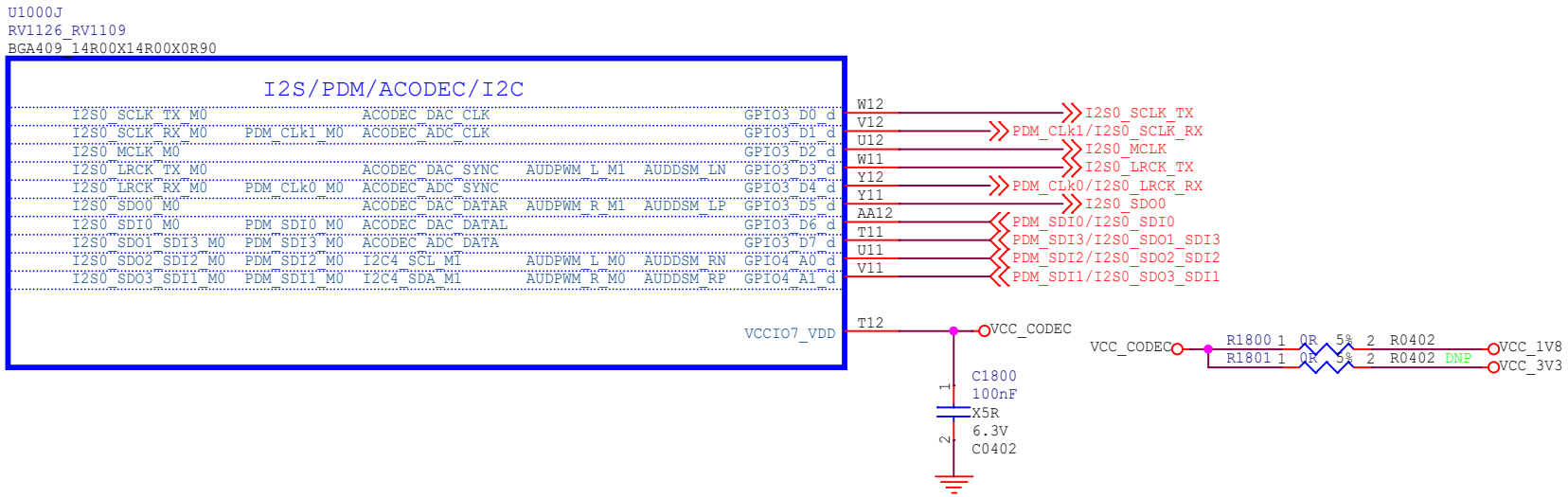
U1000D
RV1126_RV1109
BGA409_14R00X14R00X0R90

MIPI DSI TX0

MIPI_DSI_TX0_D0P	A19
MIPI_DSI_TX0_D0N	B19
MIPI_DSI_TX0_D1P	A20
MIPI_DSI_TX0_D1N	B20
MIPI_DSI_TX0_D2P	B21
MIPI_DSI_TX0_D2N	C20
MIPI_DSI_TX0_D3P	D20
MIPI_DSI_TX0_D3N	D19
MIPI_DSI_TX0_CLKP	C19
MIPI_DSI_TX0_CLKN	C18
MIPI_DSI_TX0_AVDD_0V8	E18
MIPI_DSI_TX0_AVDD_1V8	G15

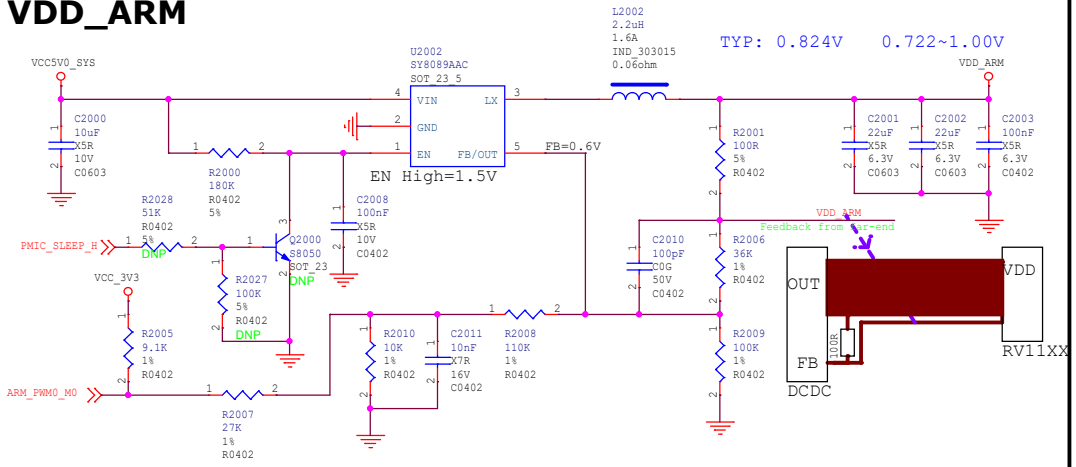
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RV1126_RV1109 AI Camera		
File:	17.RV1126/1109_VideoOutput		
Date:	Sunday, February 07, 2021	Rev:	V1.5
Designed by:	whb	Reviewed by:	Sheet: 15 of 28

Audio Interface

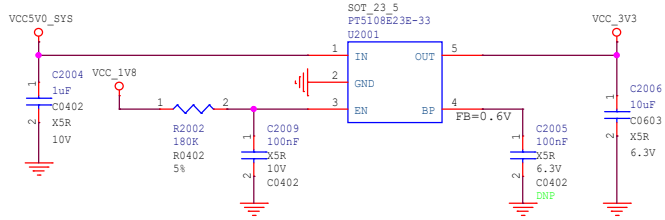


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 AI Camera				
File:	18.RV1126/1109_Audio				
Date:	Sunday, February 07, 2021			Rev:	V1.5
Designed by:	whb	Reviewed by:		Sheet:	16 of 28

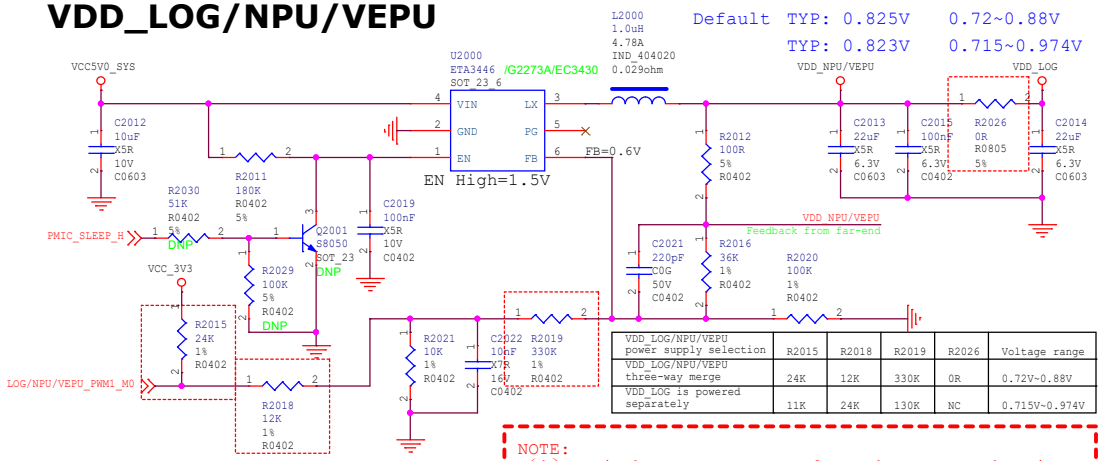
VDD_ARM



VCC_3V3



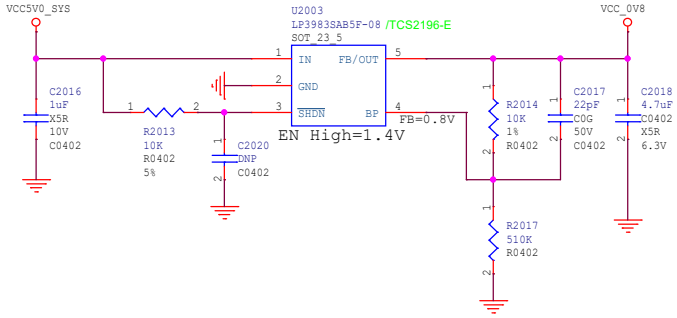
VDD_LOG/NPU/VEPU



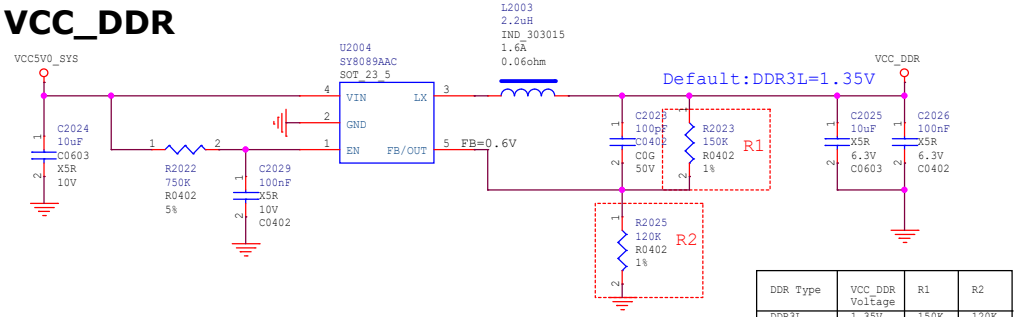
VDD_LOG/NPU/VEPU power supply selection	R2015	R2018	R2019	R2026	Voltage range
VDD_LOG/NPU/VEPU three-way merge	24K	12K	330K	0R	0.72V~0.88V
VDD_LOG is powered separately	11K	24K	130K	NC	0.715V~0.974V

NOTE:
(1) It is better not to replace the DCDC, otherwise good transient and noise within 80mV must be selected.
(2) If RV1126 is used and the NPU frequency is up to 934M, the VDD_LOG requires a separate power supply.

VCC_0V8

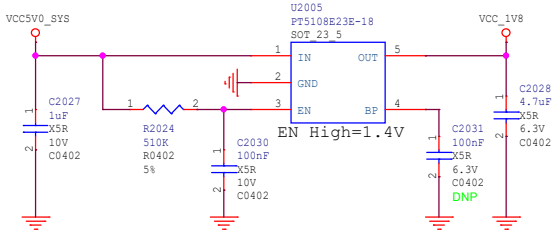


VCC_DDR



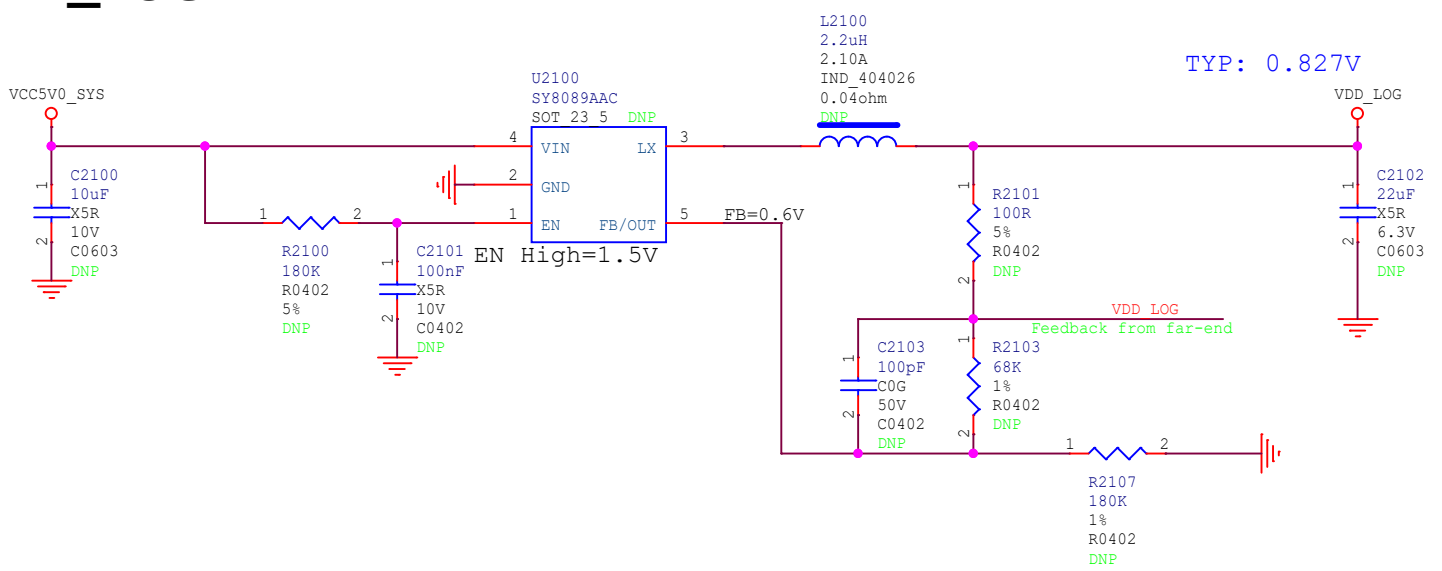
DDR Type	VCC_DDR Voltage	R1	R2
DDR3L	1.35V	150K	120K
DDR3	1.50V	150K	100K

VCC_1V8

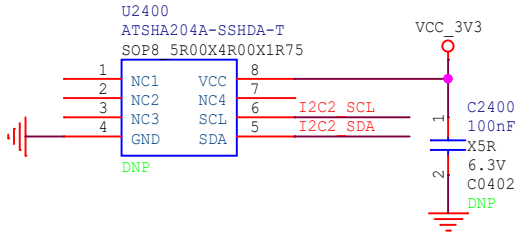


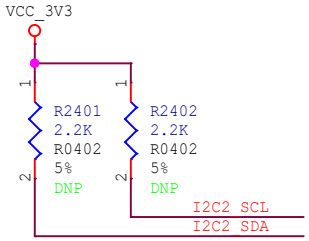
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 AI Camera				
File:	20.Power_SYS				
Date:	Sunday, February 07, 2021			Rev:	V1.5
Designed by:	whb	Reviewed by:		Sheet:	17 of 28

VDD_LOG



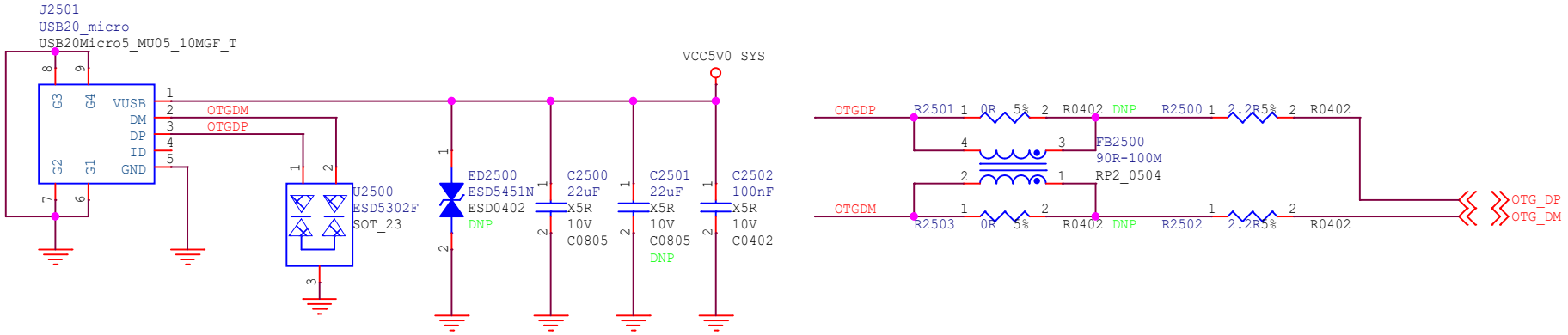
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 AI Camera				
File:	21.Power_SYS				
Date:	Sunday, February 07, 2021			Rev:	V1.5
Designed by:	whb	Reviewed by:		Sheet:	18 of 28





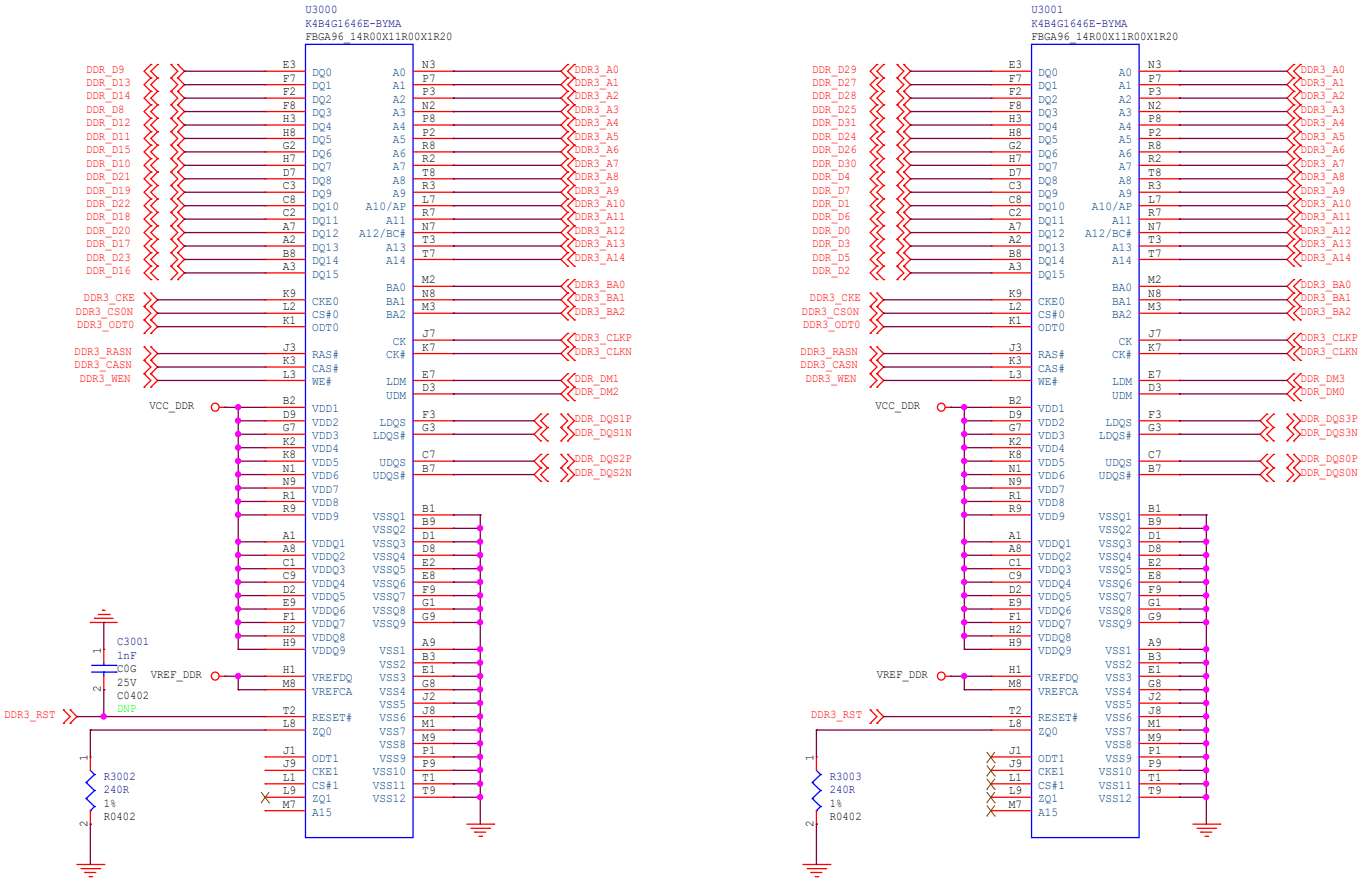
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 AI Camera				
File:	24.Encrytion Chip				
Date:	Sunday, February 07, 2021			Rev:	V1.5
Designed by:	whb	Reviewed by:		Sheet:	19 of 28

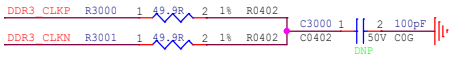
USB2.0 OTG



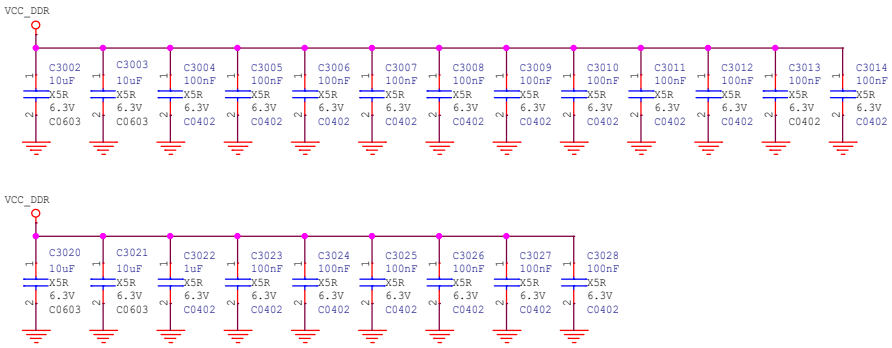
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 AI Camera				
File:	25.USB OTG				
Date:	Sunday, February 07, 2021			Rev:	V1.5
Designed by:	whb	Reviewed by:		Sheet:	20 of 28

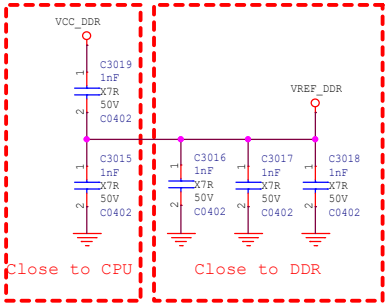
DDR3/DDR3L 2x16bit





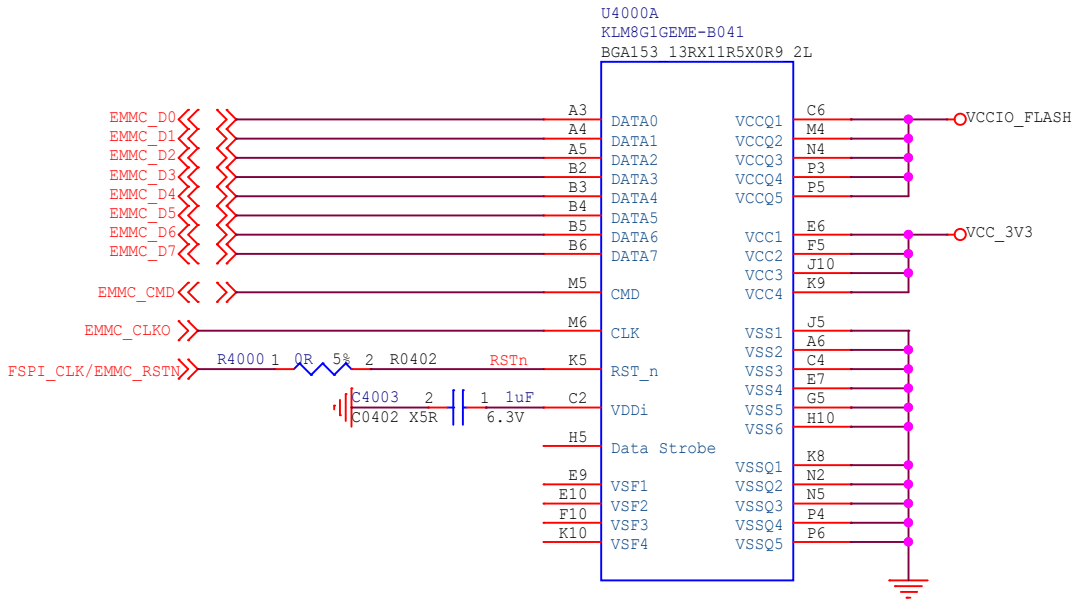
Note:All the Power filter capacitors should be placed close to the power pins of DDR3

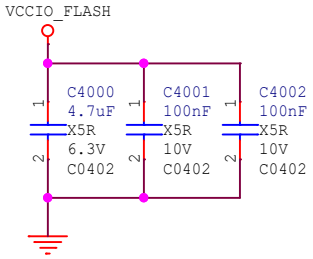


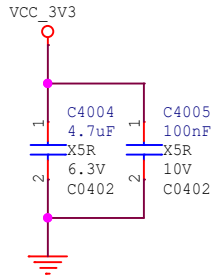


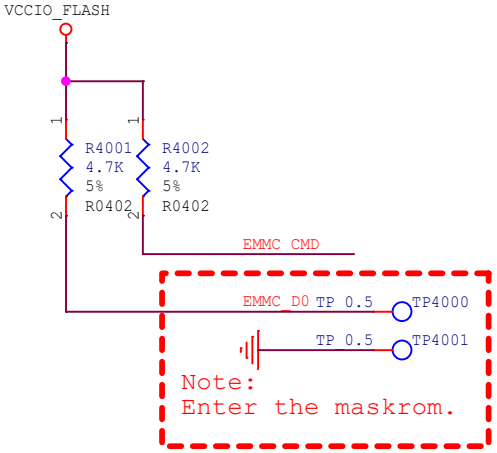
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 AI Camera				
File:	30.DRAM_DDR3_96P_2X16bit				
Date:	Sunday, February 07, 2021			Rev:	V1.5
Designed by:	whb	Reviewed by:		Sheet:	21 of 28

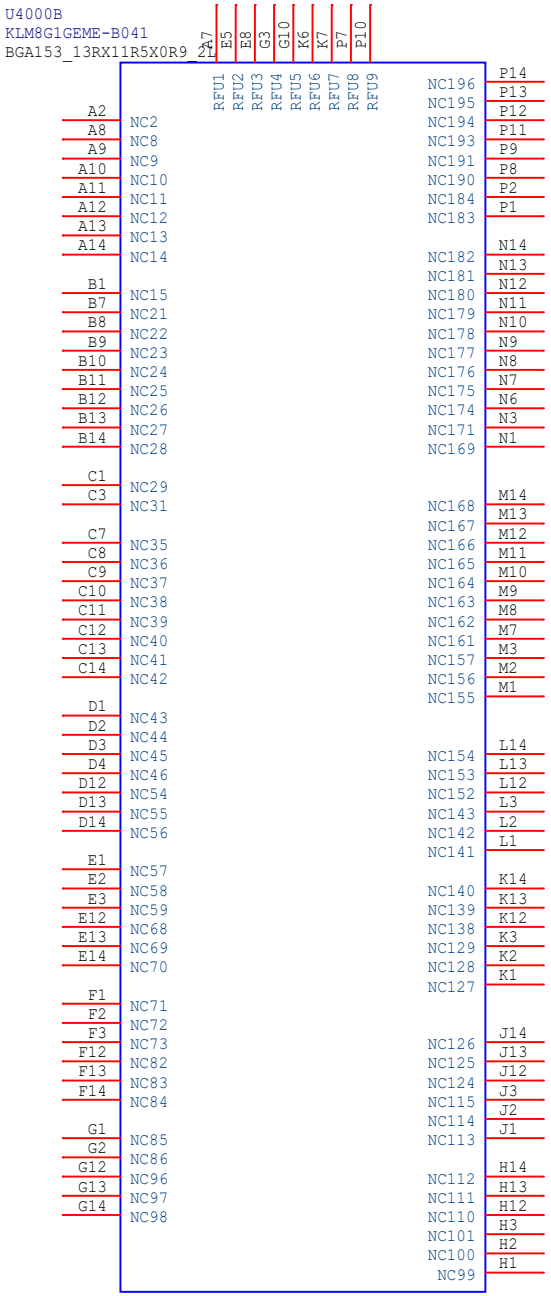
eMMC







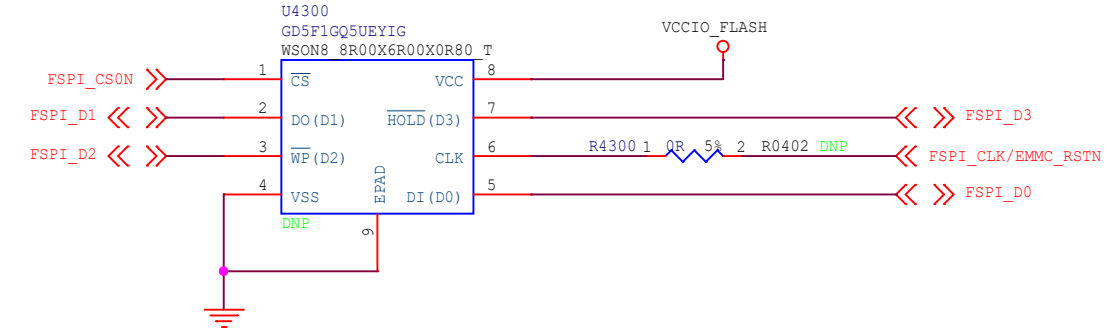


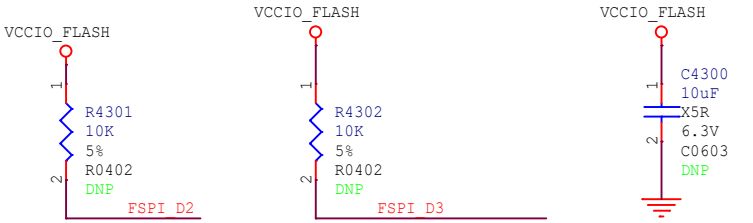


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RV1126_RV1109 AI Camera		
File:	40.Flash-eMMC Flash		
Date:	Sunday, February 07, 2021	Rev:	V1.5
Designed by: whb	Reviewed by:	Sheet:	22 of 28

SPI_Flash

NOTE:
Refer to the latest AVL for parts selection.

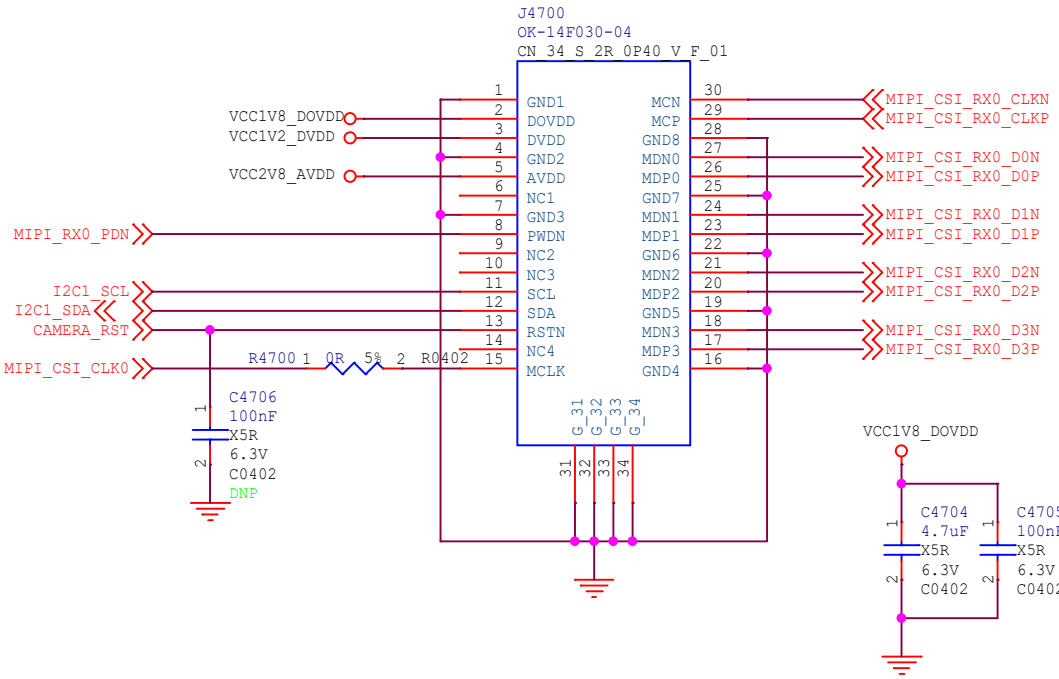


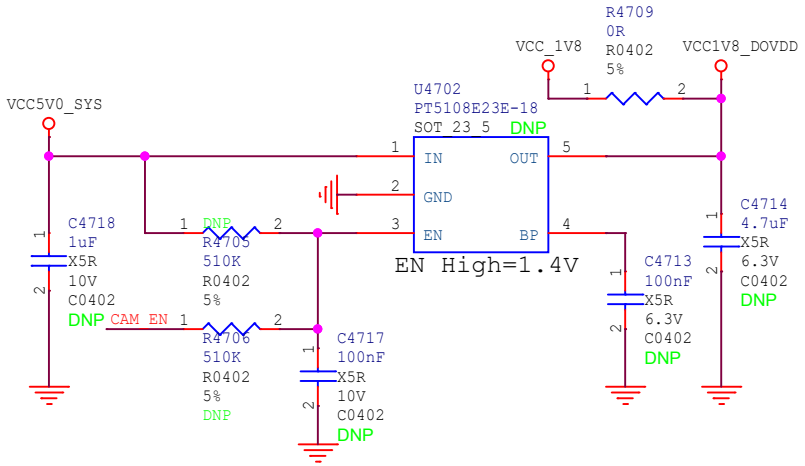


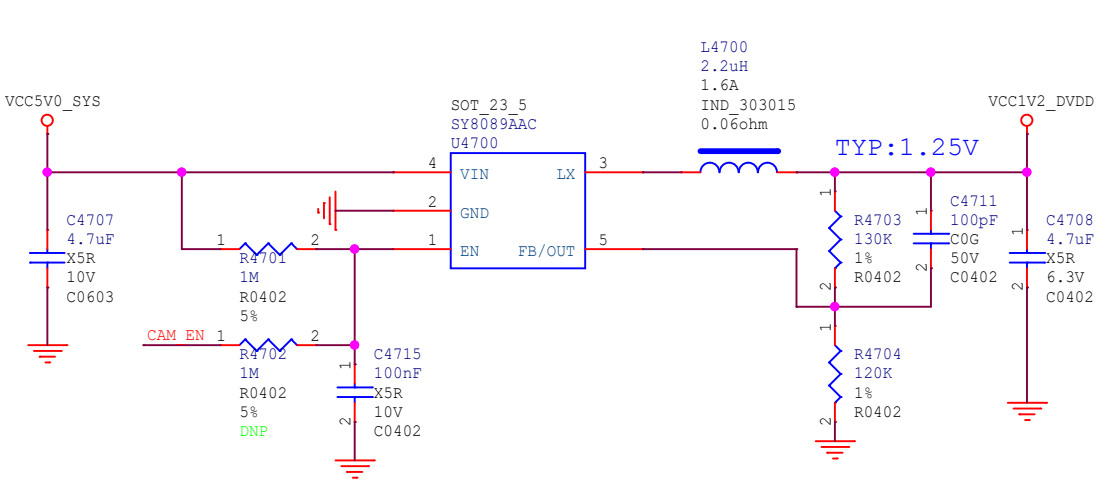
NOTE:
Reserve testpoint for firmware update,
if FLASH_D0=0V at power on reset,
then system will enter into maskrom mode

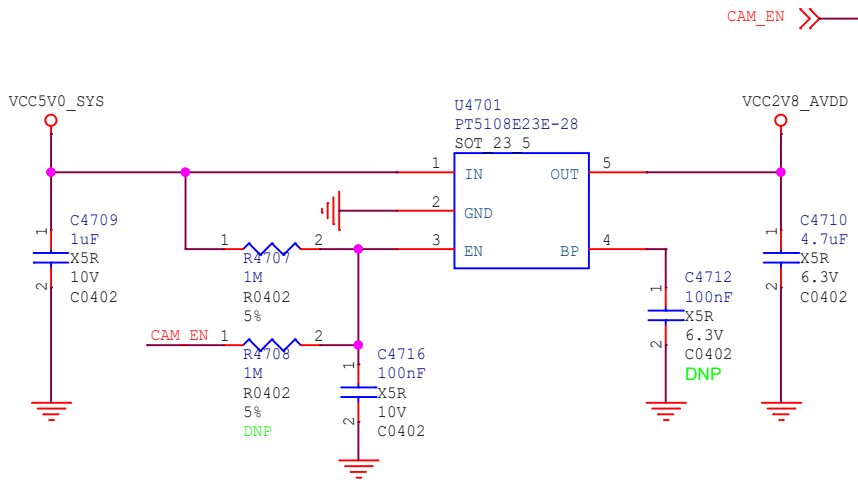
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 AI Camera				
File:	43.Flash-SPI Flash(option)				
Date:	Sunday, February 07, 2021			Rev:	V1.5
Designed by:	whb	Reviewed by:		Sheet:	23 of 28

MIPI-CSI_RX0 Interface





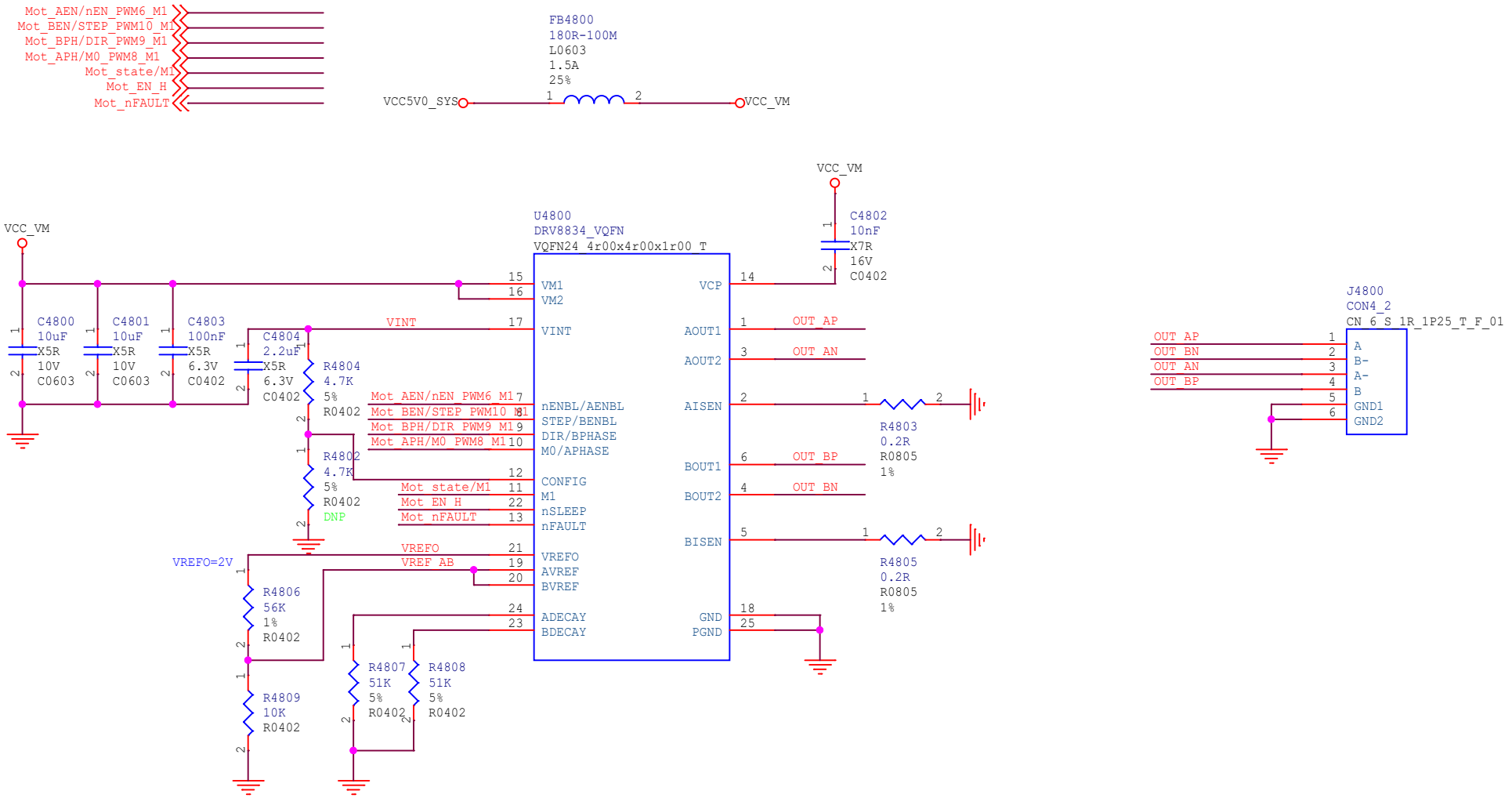




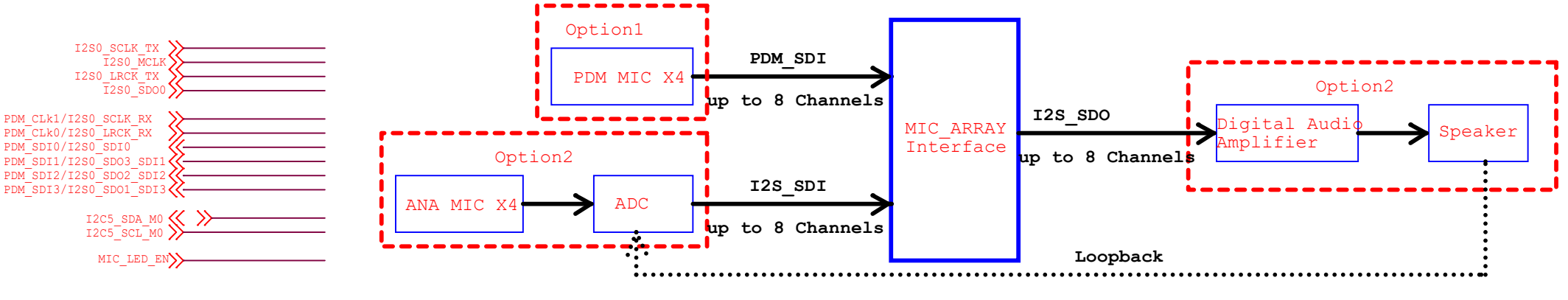
Note:
The power-on timing needs to be adjusted according to the actual camera module used
Default power-on timing:
VCC1V8_DOVDD-->VCC1V2_DVDD/VCC2V8_AVDD

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RV1126_RV1109 AI Camera		
File:	47.VI-Camera_MIPI-CSI		
Date:	Sunday, February 07, 2021	Rev:	V1.5
Designed by: whb	Reviewed by:	Sheet:	24 of 28

Iris Zoom Focus driver

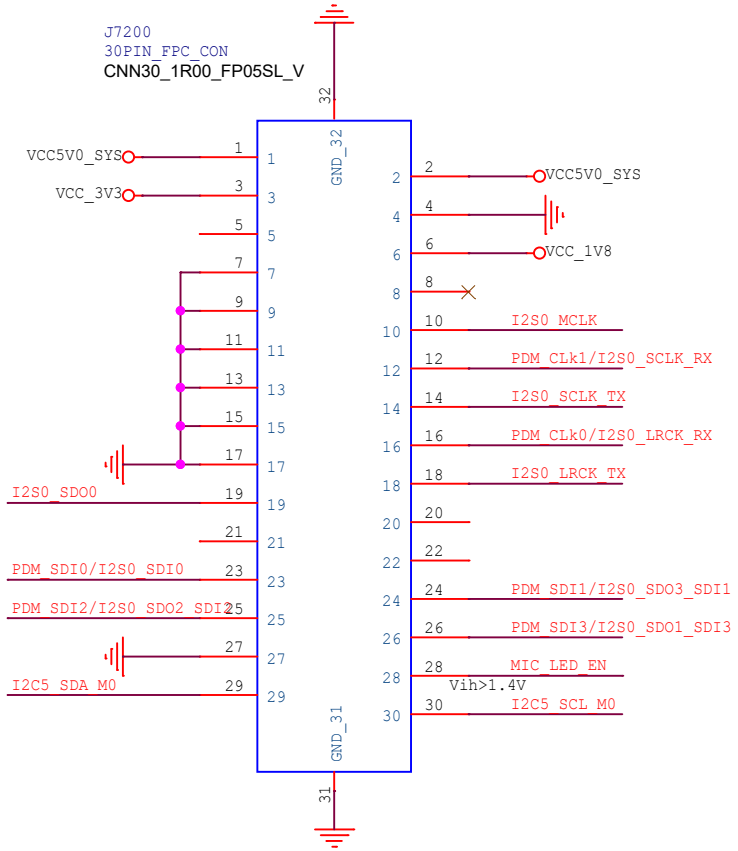


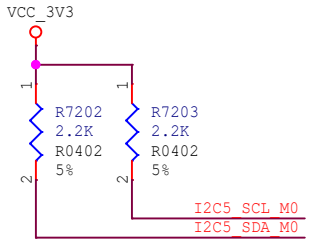
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RV1126_RV1109 AI Camera		
File:	48.Motor driver		
Date:	Sunday, February 07, 2021	Rev:	V1.5
Designed by: whb	Reviewed by:	Sheet:	25 of 28

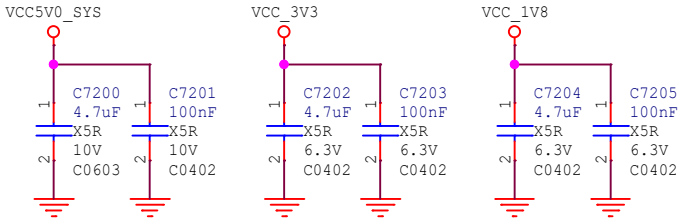


NOTE:
MIC support mode PDM or I2S

MIC_ARRAY Interface

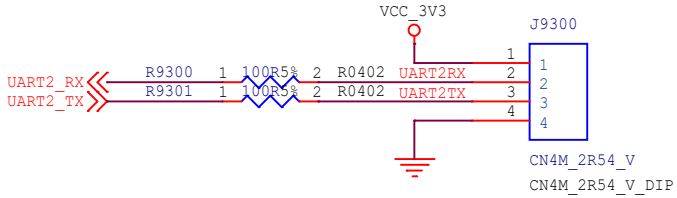






Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RV1126_RV1109 AI Camera		
File:	72.MIC Array Interface(option)		
Date:	Sunday, February 07, 2021	Rev:	V1.5
Designed by: whb	Reviewed by:	Sheet:	26 of 28

Debug UART2



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RV1126_RV1109 AI Camera				
File:	93.Debug				
Date:	Sunday, February 07, 2021			Rev:	V1.5
Designed by:	whb	Reviewed by:		Sheet:	27 of 28

M9900
MARK

M9901
MARK

M9902
MARK

M9903
MARK

M9904
MARK

M9905
MARK

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	**RV1126_RV1109 AI Camera**				
File:	**99.MARK/HOLE**				
Date:	Sunday, February 07, 2021			Rev:	V1.5
Designed by:	whb	Reviewed by:		Sheet:	28 of 28