
STM32
CubeMX

1. Description

1.1. Project

Project Name	SWITCH_TWO_FALLING
Board Name	P-NUCLEO-WB55-NUCLEO
Generated with:	STM32CubeMX 6.5.0
Date	07/12/2022

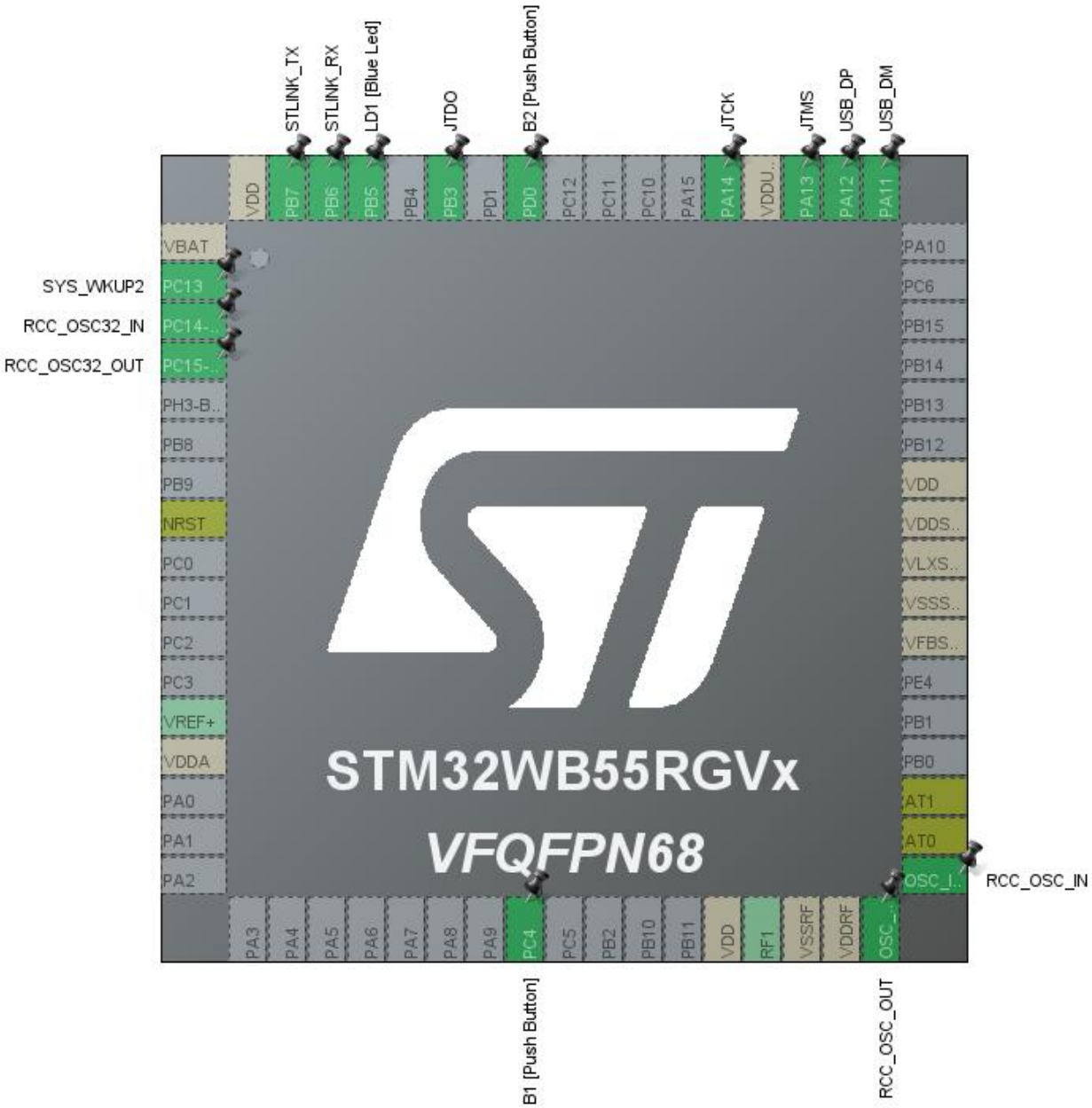
1.2. MCU

MCU Series	STM32WB
MCU Line	STM32WBx5
MCU name	STM32WB55RGVx
MCU Package	VFQFPN68
MCU Pin number	68

1.3. Core(s) information

Core(s)	ARM Cortex-M4

2. Pinout Configuration

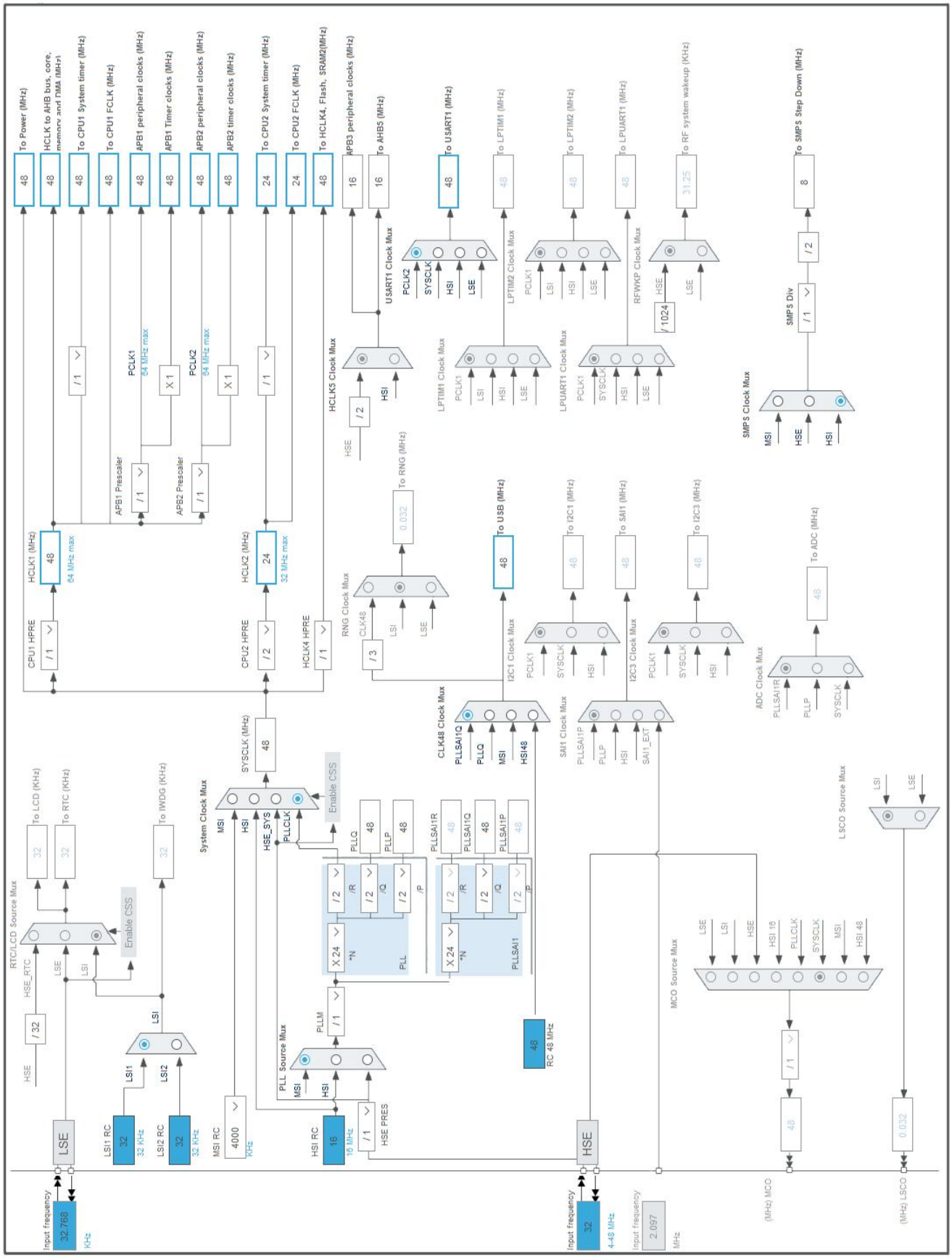


3. Pins Configuration

Pin Number VFQFPN68	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	SYS_WKUP2	
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
8	NRST	Reset		
14	VDDA	Power		
25	PC4 *	I/O	GPIO_Input	B1 [Push Button]
30	VDD	Power		
32	VSSRF	Power		
33	VDDRF	Power		
34	OSC_OUT	MonoIO	RCC_OSC_OUT	
35	OSC_IN	MonoIO	RCC_OSC_IN	
36	AT0	NC		
37	AT1	NC		
41	VFBSMPS	Power		
42	VSSSMPS	Power		
43	VLXSMPS	Power		
44	VDDSMPS	Power		
45	VDD	Power		
52	PA11	I/O	USB_DM	
53	PA12	I/O	USB_DP	
54	PA13	I/O	SYS_JTMS-SWDIO	JTMS
55	VDDUSB	Power		
56	PA14	I/O	SYS_JTCK-SWCLK	JTCK
61	PD0 *	I/O	GPIO_Input	B2 [Push Button]
63	PB3	I/O	SYS_JTDO-SWO	JTDO
65	PB5 *	I/O	GPIO_Output	LD1 [Blue Led]
66	PB6	I/O	USART1_TX	STLINK_RX
67	PB7	I/O	USART1_RX	STLINK_TX
68	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	SWITCH_TWO_FALLING
Project Folder	C:\Users\user\STM32CubeIDE\workspace_1.9.0\SWITCH_TWO_FALLING
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_WB V1.13.3
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_USART1_UART_Init	USART1
4	MX_USB_PCD_Init	USB

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32WB
Line	STM32WBx5
MCU	STM32WB55RGVx
Datasheet	DS11929_Rev3

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

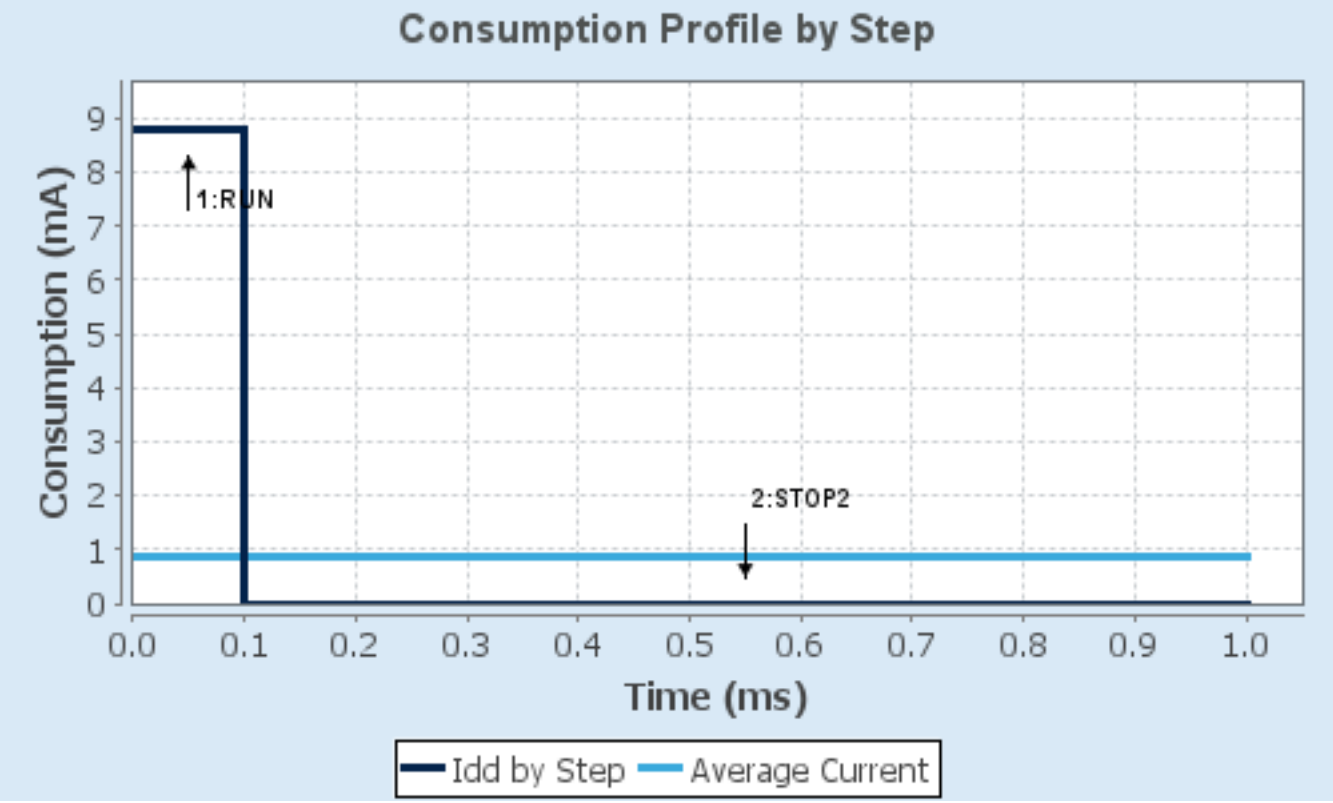
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	SRAM1/Flash-PowerDown	FLASH/ART/CACHE
CPU Frequency	64 MHz	0 Hz
Clock Configuration	HSI PLL Regulator_ON	ALL CLOCKS OFF Regulator_ON
Clock Source Frequency	16 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	8.8 mA	1.85 µA
Duration	0.1 ms	0.9 ms
DMIPS	80.0	0.0
Ta Max	103.76	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	881.66 µA
Battery Life	5 months, 7 days, 21 hours	Average DMIPS	8.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
9
8
7
6
5
4
3
2
1
0
1:RUN
2:STOP2
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.1.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Enabled
MSI State	Enabled
HSI State	Enabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
LSE Drive Capability	LSE oscillator low drive capability

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

Peripherals Clock Configuration:

Generate the peripherals clock configuration	TRUE

7.2. SYS

Debug: Trace Asynchronous Sw

mode: System Wake-Up 2

Timebase Source: SysTick

7.3. USART1

Mode: Asynchronous

7.3.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200

Word Length	**7 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.4. USB

mode: Device (FS)

7.4.1. Parameter Settings:

Basic Parameters:

Speed	Full Speed 12MBit/s
Physical interface	Internal Phy
Sof Enable	Disabled

Power Parameters:

Low Power	Disabled
Link Power Management	Disabled
Battery Charging	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
	OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
SYS	PC13	SYS_WKUP2	n/a	n/a	n/a	
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	JTMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	JTCK
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	JTDO
USART1	PB6	USART1_TX	Alternate Function Push Pull	**Pull-up ***	Low	STLINK_RX
	PB7	USART1_RX	Alternate Function Push Pull	**Pull-up ***	Low	STLINK_TX
USB	PA11	USB_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	USB_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PC4	GPIO_Input	Input mode	**Pull-up ***	n/a	B1 [Push Button]
	PD0	GPIO_Input	Input mode	**Pull-up ***	n/a	B2 [Push Button]
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1 [Blue Led]

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD/PVM0/PVM2 interrupts through EXTI lines 16/31/33	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USB high priority interrupt	unused		
USB low priority interrupt, USB wake-up interrupt through EXTI line 28	unused		
CPU2 SEV interrupt through EXTI line 40 and PWR CPU2 HOLD wake-up interrupt	unused		
USART1 global interrupt	unused		
PWR switching on the fly, end of BLE activity, end of 802.15.4 activity, end of critical radio phase interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

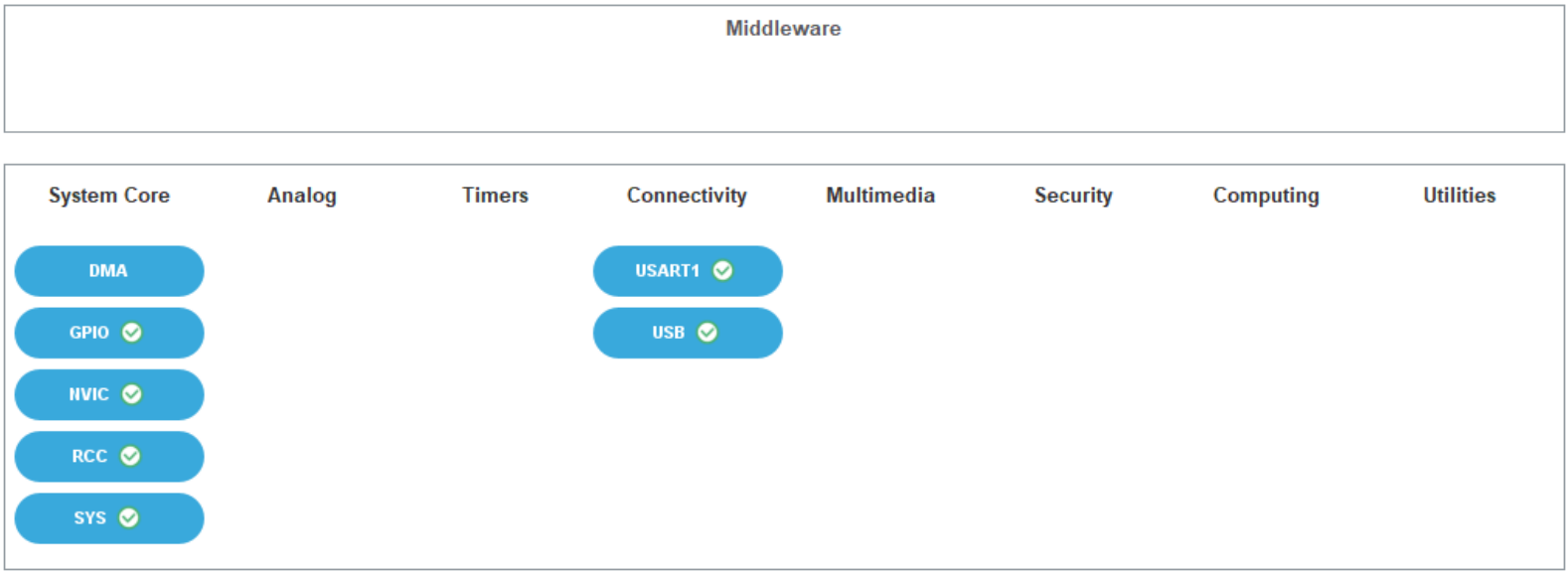
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link