

→ Ripple aren't state machines, but have seq logic

→ Sync all " "

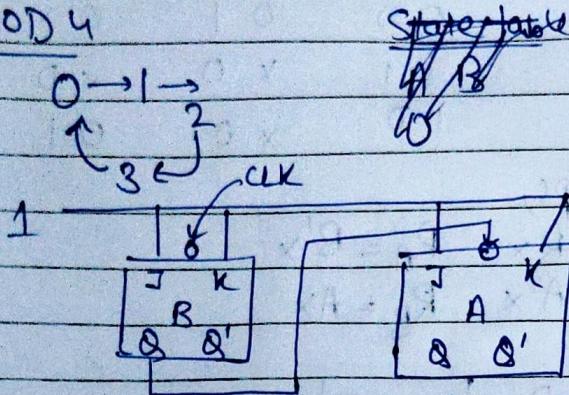
### Ripple Counter

↳ cascaded JK FF with JK lead wired high

↳ Q/p is added to the CLK of next

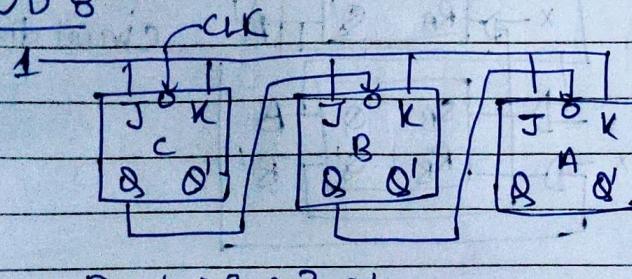
↳ FF generating LSB of count receives input CLK

#### MOD 4



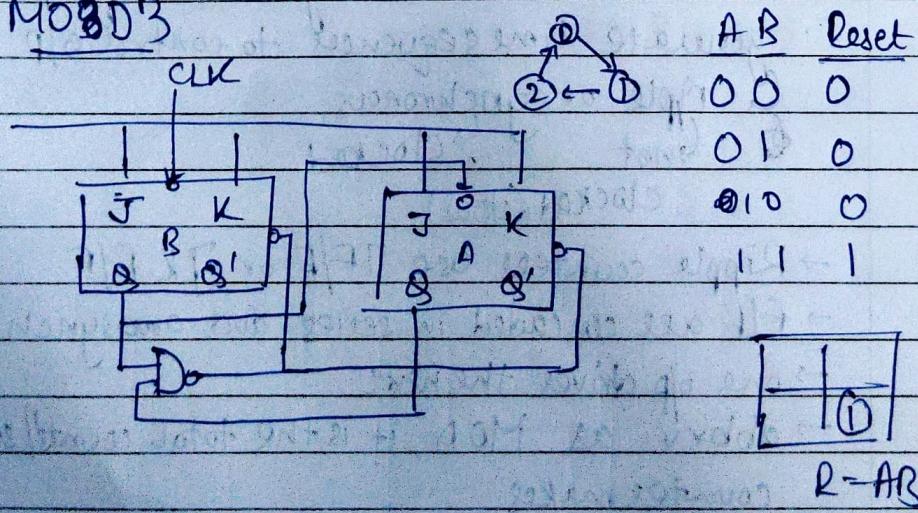
00 → 0  
01 → 1  
10 → 2  
11 → 3

#### MOD 8



000 → 0  
001 → 1  
010 → 2  
011 → 3  
0100 → 4  
101 → 5  
110 → 6  
111 → 7

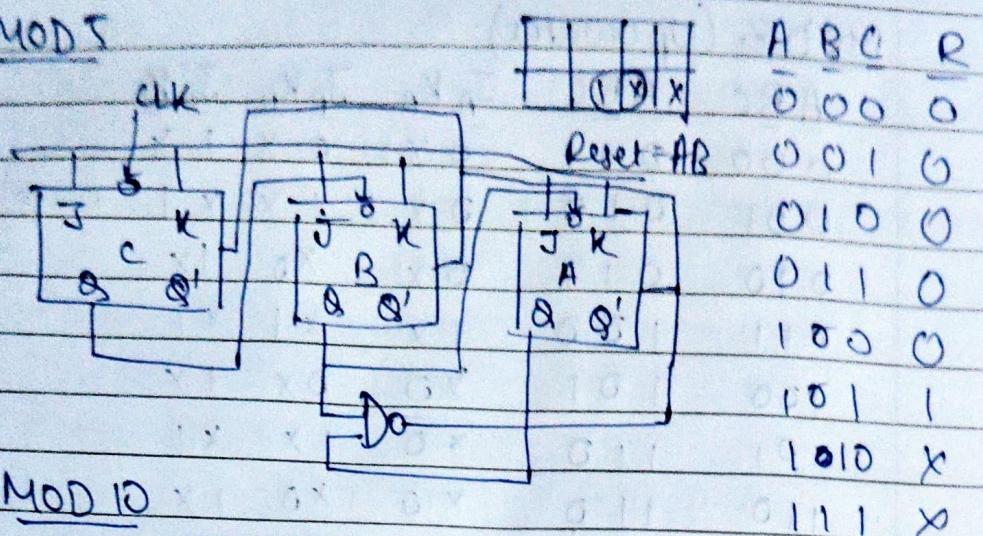
#### MOD 3



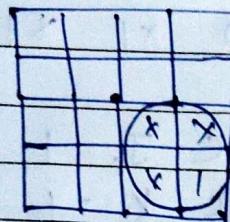
R = AB

11

MOD5



MOD10



$$\bar{Q} = \overline{AC}, \quad Q = AC$$

Same as above just connect AC

MOD14 - Similar

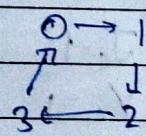
Synchronous Counters (parallel counters)

→ all same as synch.

→ there is a master clock generator.

→ CLK connected to all

MOD4

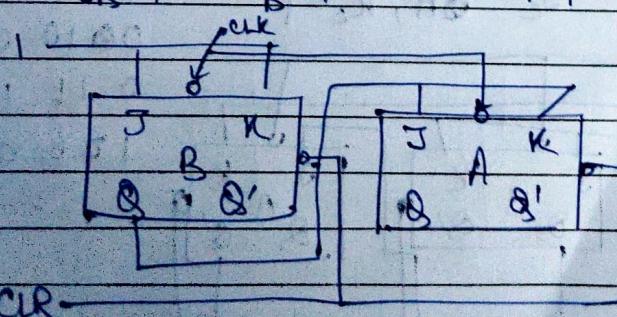


p state	next state	F/F
A B	A B	J <sub>A</sub> K <sub>A</sub> J <sub>B</sub> K <sub>B</sub>
0 0	0 1	0 X 1 X
0 1	1 0	0 X X 1
1 0	1 1	X 0 1 X
1 1	0 0	X 0 X 1

from K-map,

$$J_A = B, \quad K_A = B$$

$$J_B = 1, \quad K_B = 1$$



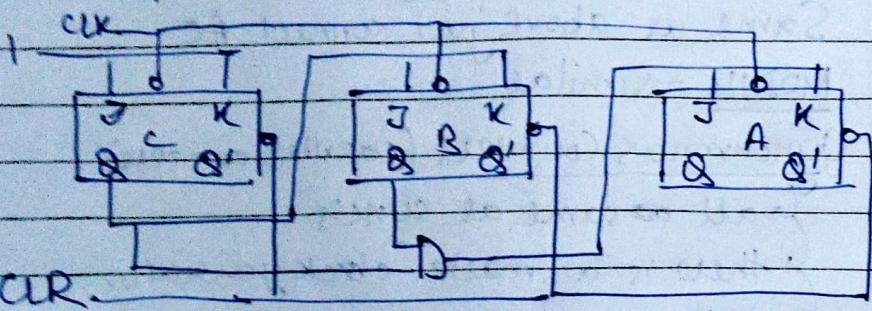
## MOD8 (Upcounter)

A	B	C	J <sub>A</sub>	K <sub>A</sub>	J <sub>B</sub>	K <sub>B</sub>	J <sub>C</sub>	K <sub>C</sub>
0	0	0	1	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	0	0	0	X	1	1
0	1	1	0	1	0	X	0	X
1	0	0	1	0	1	X	1	1
1	0	1	1	0	0	X	1	X
1	1	0	0	0	1	X	0	X
1	1	1	0	0	0	X	1	1

from k maps,

$$J_A = BC \quad J_B = C' \quad J_C = 1$$

$$K_A = BC \quad K_B = C' \quad K_C = 1$$



Down Counter is reverse

$$J_A = B'C' \quad J_B = C' \quad J_C = 1$$

$$K_A = B'C' \quad K_B = C \quad K_C = 1$$

## MOD5

$$J_A = BC, K_A = 1$$

$$J_B = C, K_B = C$$

$$J_C = A', K_C = 1$$

$$\begin{array}{ccccccccc} A & B & C & A & B & C & J_A & K_A & J_B & K_B \\ \hline 0 & 0 & 0 & 0 & 0 & 1 & 0X & 0X & 0X & 0X \end{array}$$

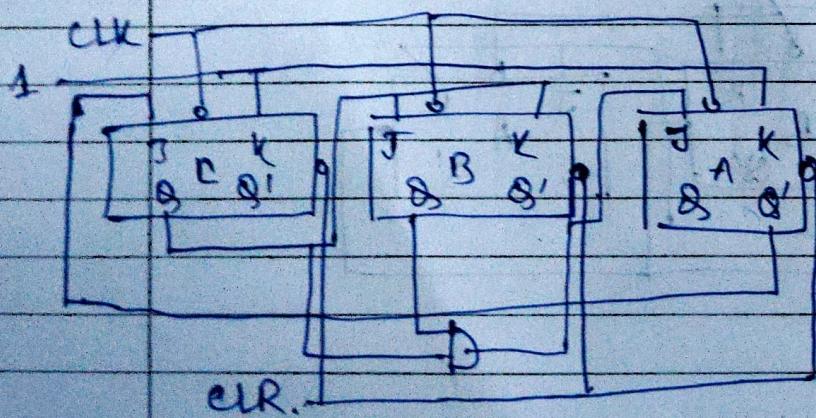
$$0 & 0 & 1 & 0 & 1 & 0 & 0X & 1X & 1X & 0X$$

$$0 & 1 & 1 & 0 & 0 & 1 & 0X & X0 & X0 & 0X$$

$$1 & 0 & 0 & 0 & 0 & 0 & X1 & 0X & 0X & 0X$$

$$1 & 0 & 0 & 0 & 0 & 0 & 0X & 0X & 0X & 0X$$

$$\begin{array}{c} J_C \quad K_C \\ \hline 1 & X \\ X & 1 \\ 1 & X \\ X & 1 \\ 0 & X \end{array}$$



## Register

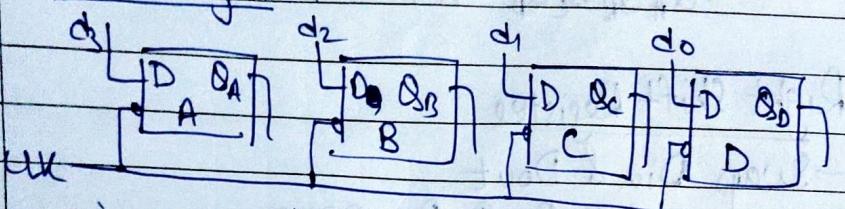
- ↳ a grp of memory elements that store binary info
- ↳ F/F used for 1 bit info
- ↳ F/Fs arranged to form registers, each F/F is called stage.

↳ All F/F have common clock Pulse

↳ n bit  $\Leftrightarrow$  n F/Fs

printers, temp memory

## Buffer Register



→ implemented using D flip flop (negative edge triggered)

→  $d_3, d_2, d_1, d_0$  is applied as input

→ 1<sup>st</sup> neg edge

$$Q_A Q_B Q_C Q_D = d_3 d_2 d_1 d_0$$

→ retain o/p

## Controlled Buffer Register

→ input depends on ctrl input

→ CLR is active  $\Rightarrow Q_A Q_B Q_C Q_D = 0000$

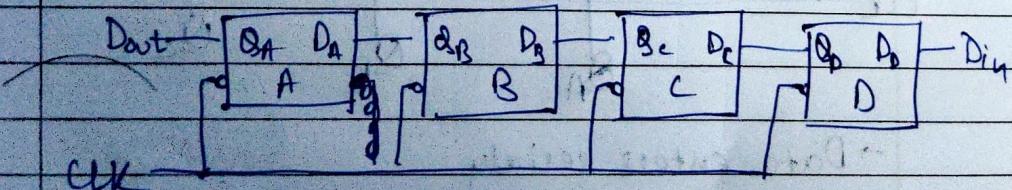
→ ... " inactive  $\Rightarrow$  can receive data.

## Shift Register

↳ useful in storage & transfer of data

↳ shifts data to L or R

## Left Shift Register



→ Initially  $D_{in} = 1$  &  $Q_A Q_B Q_C Q_D = 0000$

→ 1<sup>st</sup> pulse

$$\hookrightarrow Q_A Q_B Q_C Q_D = 0001$$

→ 2<sup>nd</sup> pulse

$$\hookrightarrow Q_A Q_B Q_C Q_D = 0011$$

→ 3<sup>rd</sup> pulse

$$\hookrightarrow Q_A Q_B Q_C Q_D = 0111$$

→ 4<sup>th</sup> pulse

$$\hookrightarrow Q_A Q_B Q_C Q_D = 1111$$

Answer appears at Dout

### Right Shift Register

→ Swap  $D_{in}$  &  $D_{out}$

→  $D_{in} = 1$  &  $Q_A Q_B Q_C Q_D = 0000$

→ 1<sup>st</sup> Pulse

$$\hookrightarrow Q_A Q_B Q_C Q_D = \cancel{0001}$$

→ 3<sup>rd</sup> Pulse

$$\hookrightarrow Q_A Q_B Q_C Q_D = 1110$$

→ 2<sup>nd</sup> Pulse

$$\hookrightarrow Q_A Q_B Q_C Q_D = 1100$$

→ 4<sup>th</sup> Pulse

$$\hookrightarrow Q_A Q_B Q_C Q_D = 1111$$

Bits are transferred in two ways

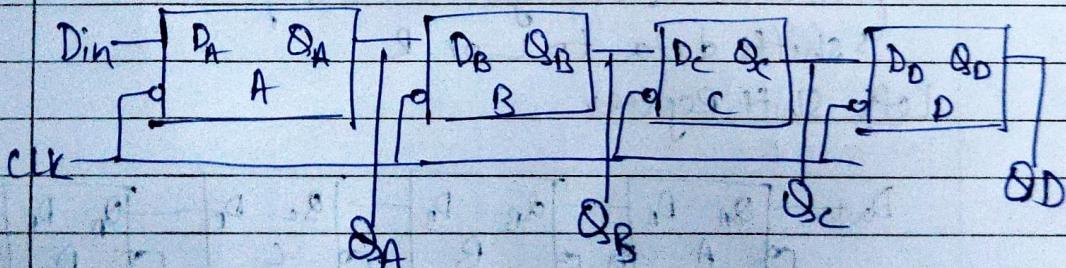
↳ if it is done serially → serial shifting

↳ ... " simultaneously → parallel shifting

In  $\Rightarrow$  See In ParIn

Out  $\Rightarrow$  See  $\overset{\text{out}}{\text{D}}$  ParOut

### Serial In Parallel Out Shift Register (SIPO)



→ Data enters serially

→ Output is simultaneous

Let 1011 is added to the register.

first  $Q_A Q_B Q_C Q_D = 0000$

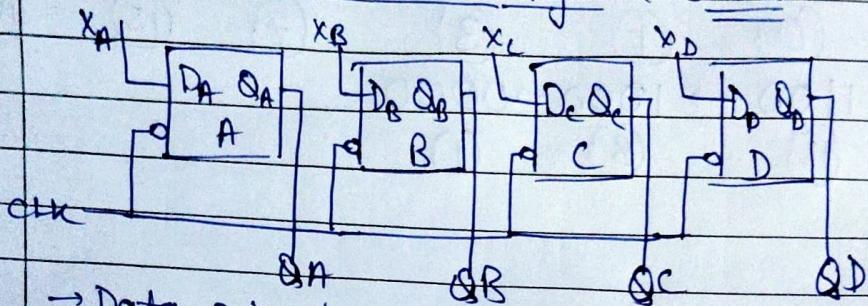
$D_A = 1 \Rightarrow Q_A Q_B Q_C Q_D = 1000$

$D_B = 1 \Rightarrow Q_A Q_B Q_C Q_D = 1100$

$D_C = 0 \Rightarrow \dots = 0110$ ,

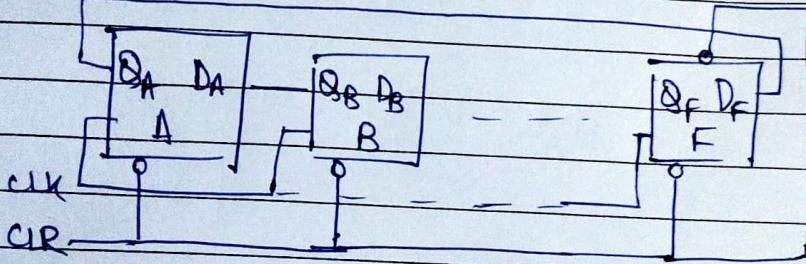
$D_D = 1 \Rightarrow \dots = 1011$

### Parallel In-Parallel Out register (PIPO)



→ Data simultaneous input, output parallel too.

### Ring Counter



→ requires hardware

→ simplest shift register

→ 1 bit  $\Rightarrow n$  states.

→ 1<sup>st</sup> pulse

↳ low-high  $\Rightarrow Q_A - Q_F = 000001$

↳ edge  $\Rightarrow Q_A - Q_F = 000010$

→ 2<sup>nd</sup> pulse

↳  $Q_A - Q_F = 000100$

⋮

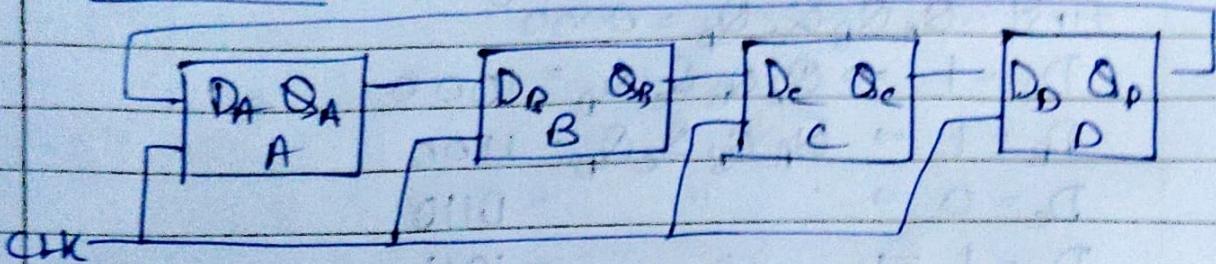
→ 58<sup>th</sup> Pulse

↳  $Q_A - Q_F = 100000$

→ 6<sup>th</sup> Pulse

↳  $Q_A - Q_F = 000001$

## Johnson Counter



$0000 \rightarrow 0001 \rightarrow 0011 \rightarrow 0111 \rightarrow 1111 \rightarrow 1110 \rightarrow$   
① ② ③ ④ ⑤ ⑥

$1100 \rightarrow 1000 \rightarrow 0000$   
⑦ ⑧ ⑨