Jetson Xavier NX Tuning and Compliance Guide

Application Note

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Document History

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Version	Date	Description of Change
1.0	April 9, 2020	Initial Release
1.1	October 30, 2020	Added "Tools" section in the "Jetson Xavier NX Ethernet Compliance Test Guide" chapter
1.2	December 11, 2010	• Updated Table 18 • Updated "DUT" under DP and eDP tuning section

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Jetson Xavier NX USB 2.0 Tuning Guide

This chapter describes the registers and steps needed to tune the USB 2.0 high speed eye diagram for the NVIDIA® Jetson Xavier™ NX module. USB IF provides complete test specification and instructions on their website for high-speed host and device mode testing. NVIDIA typically uses Tektronix oscilloscopes for USB characterizations.

Customers are free to use oscilloscopes from other vendors to do USB characterization.

USB 2.0 Tuning Required Equipment

The following equipment is required:

- Tektronix TDS694C or faster digital sampling oscilloscope
- Tektronix P6247 or P6248 or equivalent differential probe * 1
- High-speed USB Electrical Test Fixture
- Oscilloscope USB test software
- Tool to access register/memory space in NVIDIA® Xavier™ or build a special image to force USB test mode enabled

Registers for Host Mode Testing

Toggle the Jetson Xavier NX module USB registers listed in Table 1 to force Test J, Test K, Test SE0 NAK, and Test Packet on the respective USB port.

Table 1. Host Mode Test Registers

Description	Register Name and Setting
Normal Operations	T_XUSB_XHCI_OP_PORTPMSCHS_x[31:28] = 0000b
Test J	T_XUSB_XHCI_OP_PORTPMSCHS_x[31:28] = 0001b
Test K	T_XUSB_XHCI_OP_PORTPMSCHS_x[31:28] = 0010b
Test SE0 NAK	T_XUSB_XHCI_OP_PORTPMSCHS_x[31:28] = 0011b
Test Packet	T_XUSB_XHCI_OP_PORTPMSCHS_x[31:28] = 0100b

Force Enable	T_XUSB_XHCI_OP_PORTPMSCHS_x[31:28] = 0101b

The xUSB USB 2.0 port register addresses are as follows:

- Port 0: 0x03610464: T_XUSB_XHCI_OP_PORTPMSCHS_4
- Port 1: 0x03610474: T_XUSB_XHCI_OP_PORTPMSCHS_5
- Port 2: 0x03610484: T_XUSB_XHCI_OP_PORTPMSCHS_6

USB 2.0 Test Mode Programming Sequence

The programming sequence for enabling USB 2.0 test mode is as follows:

Note: The output of USB 2.0 test pattern is only supported for point to point connections.

1. Connect any USB device to the port (this will prevent the controller from entering power down mode).

Note: "Any USB device" refers to any real device, such as HS uDISK or LS mouse.

2. Disable the auto suspend for the controllers:
   a). For example: the following command under Linux Kernel:
   echo on > /sys/bus/usb/devices/usb1/power/control

Note: The "usb1" here is the XHCI USB2 controller; it may map to "usb2" if there is another USB controller on the board. The XHCI bus number can be found under /sys/devices/3610000.xhci/.

3. Set PP (Port Power) to Disabled state by T_XUSB_XHCI_OP_PORTSC[9] = 0.
   Port 0: 0x03610460: T_XUSB_XHCI_OP_PORTSC_4
   Port 1: 0x03610470: T_XUSB_XHCI_OP_PORTSC_5
   Port 2: 0x03610480: T_XUSB_XHCI_OP_PORTSC_6
4. Set RS (Run/Stop) bit in the T_XUSB_XHCI_OP_USBCMD_0[0] = 0.
   0x03610020: T_XUSB_XHCI_OP_USBCMD_0

5. Wait for the HCHalted (HCH) bit in the T_XUSB_XHCI_OP_USBSTS_0[0] = 1.
   0x03610024: T_XUSB_XHCI_OP_USBSTS_0
6. Set the xUSB Port Test Control registers in PORTPMSCHS register (see Section "Register for Host Mode Testing").

Note: Per "USB 2.0 Specification," only a single downstream facing port can be in test_mode at a given time.

7. Disable Pad PD (power down) by clearing the
   T_XUSB_PADCTL_USB2_OTG_PADx_CTL_0_0[26] = 0.
   Port 0: 0x03520088: T_XUSB_PADCTL_USB2_OTG_PAD0_CTL_0_0
   Port 1: 0x035200C8: T_XUSB_PADCTL_USB2_OTG_PAD1_CTL_0_0
   Port 2: 0x03520108: T_XUSB_PADCTL_USB2_OTG_PAD2_CTL_0_0
8. Disable Bias Pad PD (power down) by clearing the
   XUSB_PADCTL_USB2_BIAS_PAD_CTL_0_0 bit [11] = 0
   0x03520284: XUSB_PADCTL_USB2_BIAS_PAD_CTL_0_0
9. Plug in the test fixture to start the USB 2.0 eye diagram test.

Note: In Steps 3, 6, and 7, Port 0 is USB0_DP/DN (Pins 111 and 109), Port 1 is USB1_DP/DN (Pins 117 and 115), and Port 2 is UBS2_DP/DN (Pins 123 and 121).

Registers to Adjust USB 2.0 Eye Diagram

Table 2 lists the Jetson Xavier NX module USB registers that are needed to tune the USB 2.0 eye diagram. Refer to the "Tuning Procedure" section on how to use these registers during characterization.

Table 2. Xavier USB Registers

Register Name	Bit Field	Description
XUSB_PADCTL_USB2_OTG_PAD0_CTL_0_0 (Address 0x03520088) for Port 0 XUSB_PADCTL_USB2_OTG_PAD1_CTL_0_0 (Address 0x035200C8) for Port 1 XUSB_PADCTL_USB2_OTG_PAD2_CTL_0_0 (Address 0x03520108) for Port 2		
HS_SLEW[1]	8:6	HSSLEW (high speed slew rate control)
HS_CURR_LEVEL[2]	5:0	Setup (high speed drive strength control)
XUSB_PADCTL_USB2_OTG_PAD0_CTL_1_0 (Address 0x0352008C) for Port 0 XUSB_PADCTL_USB2_OTG_PAD1_CTL_1_0 (Address 0x035200CC) for Port 1 XUSB_PADCTL_USB2_OTG_PAD2_CTL_1_0 (Address 0x0352010C) for Port 2		
RPD_CTRL	30:26	RPD_CTRL (15K host pull down)
TERM_RANGE_ADJ	6:3	ATERM (high speed termination control)

Register Name	Bit Field	Description
XUSB_PADCTL_USB2_BIAS_PAD_CTL_0_0 (Address 0x03520284)		
HS_SQUELCH_LEVEL	2:0	HSSQUELCH (squelch level control for device RX testing)
XUSB_PADCTL_USB2_OTG_PAD0_CTL_3_0 (Address 0x03520094) for Port 0 XUSB_PADCTL_USB2_OTG_PAD1_CTL_3_0 (Address 0x035200D4) for Port 1 XUSB_PADCTL_USB2_OTG_PAD2_CTL_3_0 (Address 0x03520114) for Port 2		
HS_RXEQ[3]	8:6	HS_RXEQ (device RX testing)
HS_TXEQ[3]	3:1	HS_TXEQ (device TX testing)
HS_DIN_DLY_SEL[4]	0	Pre-emphasis duration

Notes:

[1]HS_SLEW where 0'b000 = slowest and 0'b111 = fastest

[2]HS_CURR_LEVEL where 0'b000000 = highest current level and 0'b111111 = lowest current level

[3]If system has inner cable, consult with AE for recommendations and perform certificate/functional test verification

[4]HS_DIN_DLY_SEL where 0b0 = 0.5-bit and 0b1 = 1-bit delayed data of HS_DIN

Table 3. TXEQ and RXEQ Pre-Emphasis

HS_TXEQ[2:0]	AC Gain	HS_RXEQ[2:0]	SQ Level
000	+0 dB (default)	000	-0 dB (default)
001	+1.3 dB	001	-1.2 db
010	+2.5 dB	010	-2.0 dB
011	+3.5 dB	011	-3.5 dB

Table 4. HS_SQUELCH Level

HS_SQUELCH[2:0]	EL17
000	140 mV (default)
001	90 mV
010	102.5 mV
011	115 mV
100	127.5 mV
101	152.5 mV
110	165 mV
111	177.5 mV

USB 2.0 Tuning Procedure

During production, each NVIDIA Jetson Xavier NX module is calibrated based on the silicon process, the corresponding USB drive strength (HS_CURR_LEVEL), HS termination (TERM_RANGE_ADJ), and 15K host pull down (RPD_CTL) fuses are burnt on each chip.

Table 5 lists the registers that are used to find the default drive strength and HS termination value by reading from the FUSE_USB_CALIB fuse and the FUSE_USB_CALIB_EXT fuse.

Table 5. FUSE_USB Registers

Register Name	Bit Field	Description
FUSE_USB_CALIB (Address 0x038201F0)		
USB_CALIB	28:23	Reserved
USB_CALIB	22:17	HS_CURR_LEVEL for USB Port 2
USB_CALIB	16:11	HS_CURR_LEVEL for USB Port 1
USB_CALIB	10:7	TERM_RANGE_ADJ for all USB ports
USB_CALIB	5:0	HS_CURR_LEVEL for USB Port 0
FUSE_USB_CALIB_EXT (Address 0x03820350)		
USB_CALIB_EXT	4:0	RPD_CTRL for all USB ports

During the characterization stage, manually adjusting the HS_CURR_LEVEL value should be enough to fulfill compliance requirements. It is possible to try and increase termination as a last resort.

Note: NVIDIA does not recommend customers adjusting termination values. Note that if the TERM_RANGE_ADJ needs to be adjusted, it may result in an impedance mismatch on the board and further attention might be needed.

If modification to HS_CURR_LEVEL is necessary, it must be done as an offset to the default fused value to account for silicon process differences.

! CAUTION: Do not apply a global overwrite HS_CURR_LEVEL value for all silicon. There is a mechanism provided in software to read fuse USB drive strength and add an offset to it.

Consult NVIDIA SWPM/CE for additional information.

- To change high speed slew rate, write directly to: XUSB_PADCTL_USB2_OTG_PADx_CTL_0_0 bits 8:6
- To change receive squelch level, write directly to: XUSB_PADCTL_USB2_BIAS_PAD_CTL_0_0 bits 2:0
- To compensate for long cable loss, use the XUSB_PADCTL_USB2_OTG_PADx_CTL_3_0 HS_TXEQ/HS_RXEQ bit directly.

HS_CURR_LEVEL Offset Adjustment Procedure

If the default value does not fit customer design, adjust the HS_CURR_LEVEL register in order to pass the USB HS eye diagram.

Follow this procedure:

1. Obtain default value; read register FUSE_USB_CALIB (Address 0x038201F0)
   a). USSB_CALIB[5:0] USB pad HS_CURR_LEVEL[5:0] for Port 0
   b). USSB_CALIB[16:11] USB pad HS_CURR_LEVEL[5:0] for Port 1
   c). USSB_CALIB[22:17] USB pad HS_CURR_LEVEL[5:0] for Port 2
2. Calculate the offset from fused HS_CURR_LEVEL value and desired value to pass eye mask.
   a). For example, if default value is 0x20 and desired value is 0x1C, then offset = -4
   b). For example, if default value is 0x10 and desired value is 0x14, then offset = +4
3. Adjust HS_CURR_LEVEL register as described in the "Tuning Procedure" section (Note: maximum allowable offset: +/-6 steps).
4. Provide the "tuned offset value" to software team

Software Verification

NVIDIA recommends a functional check. Connect the DUT to USB hosts and devices to perform a check on functionality.

To check if software has implemented the tuned offset step properly, load new software with offset included into another DUT and check to ensure:

HS_CURR_LEVEL = USB_CALIB + tuned offset steps

Jetson Xavier NX USB 3.1 Compliance Test Guide

This chapter serves as a high-level guide to compliance testing of the USB 3.1 SuperSpeed (SS up to 5 Gbps) and SuperSpeed+ (SS+ up to 10 Gbps) PHY in host mode on the Jetson Xavier NX module. The NVIDIA Jetson Xavier NX module has been tested for specification compliance and has passed under worst case scenarios. NVIDIA expects that no tuning will be required if customers follow the routing guidelines published in the relevant design guides.

USB 3.1 Compliance Testing

The *Electrical Compliance Test Specification SuperSpeed Universal Serial Bus Rev 1.0a* provides the compliance criteria and test descriptions for SuperSpeed USB devices, hubs, and host controllers.

The *Electrical Compliance Test Specification Enhanced SuperSpeed Universal Serial Bus Rev 1.0a* provides the compliance criteria and test descriptions for SuperSpeed+ USB devices, hubs, and host controllers that conform to the *Universal Serial Bus 3.1 Specification, Rev 1.0.*

Refer to the test specification documents mentioned for a high-level overview of the tests that are performed to check the compliance criteria. Depending on the brand of equipment being used for the test, customers can then refer to the manufacturer's documentation for step-by-step procedure on how to perform the test.

Note: When the Jetson Xavier NX module is in USB RCM mode, it may not be in compliance with the USB 3.1 specification.

Placing the USB 3.1 Controller in Compliance Mode

To run the USB 3.1 TX electrical compliance test, the Jetson Xavier NX module USB 3.1 controller must be placed in compliance mode.

For SuperSpeed TX Electrical Tests refer to sections TD.1.1, TD.1.3, and TD.1.4 in the *Electrical Compliance Test Specification SuperSpeed Universal Serial Bus* at the following link:

https://usb.org/sites/default/files/SuperSpeedPHYComplianceTest_Spec1_0a.pdf

For SuperSpeed+ TX Electrical Tests, refer to sections: TD 1.4, TD 1.5, and TD1.7 in the *Electrical Compliance Test Specification Enhanced SuperSpeed Universal Serial Bus* at the following link:

https://www.usb.org/sites/default/files/EnhancedSuperSpeedPHYComplianceTestSpec.pdf

Follow these steps to place the device under test into compliance mode:

1. Boot up the DUT. Ensure the USB 3.x (3.0 for SS or 3.1 for SS+) Host Test Fixture is not connected to the DUT.
2. Install the latest OS (Linux, for example) image for the Jetson Xavier NX module.
3. Install the devmem2 tool (for the Linux installed in Step 2, for example) by running the following command.

```
$ sudo apt-get install devmem2
```

4. Launch the USB 3.1 Compliance Test Software on the scope.
5. Disable the auto suspend for the controllers:

```
$ echo on > /sys/bus/usb/devices/usb1/power/control
$ echo on > /sys/bus/usb/devices/usb2/power/control
```

6. Enter compliance test mode.

```
$ ./devmem2 0x03610440 w 0x10340
```

7. Plug in the USB 3.x Host test fixture to DUT. The other end of fixture should be connected to a scope such that DUT TX+/- with 50 ohm termination on the scope.

   For connection details refer to the "Transmitter Test Topologies" section in the document, *USB 3.0 Electrical Test Fixture Topologies*, at the following link:

   https://www.usb.org/sites/default/files/documents/superspeedtesttopologies.pdf

   For SuperSpeed+ Compliance testing, refer to the "TX Tests" section in the *USB3p1_fixture_topologies_11-8-2017_0.pdf* file at the following link for connection topology:

   https://www.usb.org/document-library/usb-31-electrical-test-fixture-topology

8. Use ./devmem2 0x3610420 (i.e. for port 0) command to read back the LTSSM state.

> Note: The Jetson Xavier NX module contains one USB 3.1 ports; their PORTSC offset and pin # are:
>
> USBSS_TX/RX (pins 168/166/163/161), offset = 0x440
>
> Writing 0x10340 will change the internal state of XUSB. Therefore, it is not expected to read back the same value. However, Bits[8:5] should be set to 0xA for compliance test mode, otherwise repeat Steps 1 through 7.

9. Connect RX+/- to external Ping.LFPS (20 MHz frequency; 2 periods) signal generator.

   Sending a PING.LFPS to the RX port of the DUT in compliance state will cause the compliance pattern to transition to next one. Contact generator vendor for support to provide required number of Ping.LFPS till controller pumps out the required compliance pattern.
10. Based on compliance pattern (CP) requirement for the current test, repeat Step 9 to pump out required CP pattern.
11. Let the test complete.

Placing the USB 3.1 Controller in Loopback Mode

To run the RX electrical JTOL test, the Jetson Xavier NX module must be trained to loopback mode.

For SuperSpeed RX Electrical Tests, refer to Sections: TD 1.2 and TD.1.5 in the document, *Electrical Compliance Test Specification SuperSpeed Universal Serial Bus Rev 1.0a*, at the following link:

https://usb.org/sites/default/files/SuperSpeedPHYComplianceTest_Spec1_0a.pdf

For SuperSpeed+ RX Electrical Tests, refer to Section TD 1.10 in the *Electrical Compliance Test Specification Enhanced SuperSpeed Universal Serial Bus* at the following link:

https://www.usb.org/sites/default/files/EnhancedSuperSpeedPHYComplianceTestSpec.pdf

Follow these steps to place the device under test into loopback mode:

1. Boot up the DUT. Make sure that the USB 3.x Host Test Fixture is not connected to the DUT.
2. Install the latest Linux image for Jetson Xavier NX module.
3. Run the following script to disable power management for USB Host Controller.

```
#!/bin/sh
for hub in $(ls -d /sys/bus/usb/devices/usb?); do
echo on > $hub/power/control
done
```

4. Configure BERT to pump out the loopback training sequence, refer to Steps 5 through 11 in Section "TD.1.5 Receiver Jitter Tolerance Test" of the following specification:

   https://usb.org/sites/default/files/SuperSpeedPHYComplianceTest_Spec1_0a.pdf

   For SuperSpeed+, upon detecting DUT Power On, refer to Steps 14 through 18 in Section "TD.1.10 Receiver Jitter Tolerance Test at 10 GT/s" of the following specification:

   https://www.usb.org/sites/default/files/EnhancedSuperSpeedPHYComplianceTestSpec.pdf
5. Connect the USB 3.x Host Test Fixture to the DUT.

   For fixture topologies and connections for Superspeed RX testing, refer to the following:

   https://www.usb.org/document-library/usb-31-electrical-test-fixture-topology
6. Start JTOL test after the controller is in loopback or repeat Steps 1 through 5.
7. Let the test complete.

Jetson Xavier NX PCIe Compliance Testing Reference

NVIDIA Jetson Xavier NX includes the Peripheral Component Interconnect Express (PCIe) interface. The implementation in NVIDIA Jetson Xavier NX supports PCIe Gen1, PCIe Gen2, PCIe Gen3 and PCIe Gen4 link speeds.

This chapter includes a list of recommended test equipment, software, and setup required to run the PCI Express (PCIe) electrical compliance tests. The Jetson Xavier NX has been tested under worst case scenarios and the hardware can adapt to the compliant devices and channel automatically. The hardware calibrates the termination impedance for both PCIe transmitter and receiver, adjusts the output amplitude, and the receiver fully adapts any internal parameter that is required. Additionally, it performs periodic equalization for the higher speed signals to compensate for temperature effect. Therefore, no tuning will be required if customer designs follow the routing guidelines published in our design guide.

The lane mappings for the configurations are internal to the PCIe root port controller. For the supported configurations, refer to the OEM product design guide for Jetson Xavier NX.

PCIe Required Equipment

The components required to perform PCIe compliance testing include:

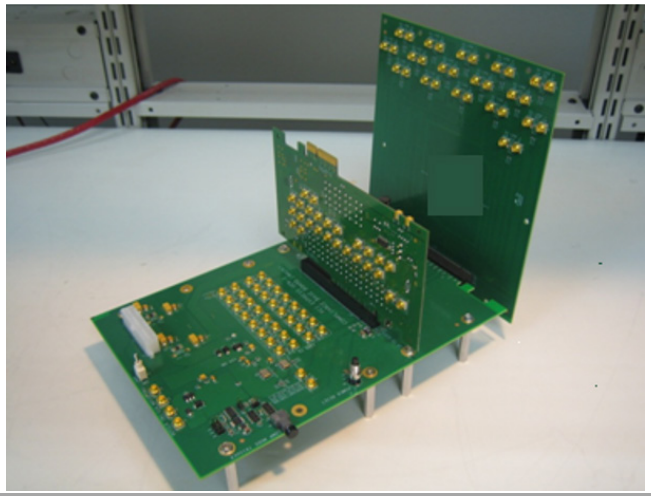
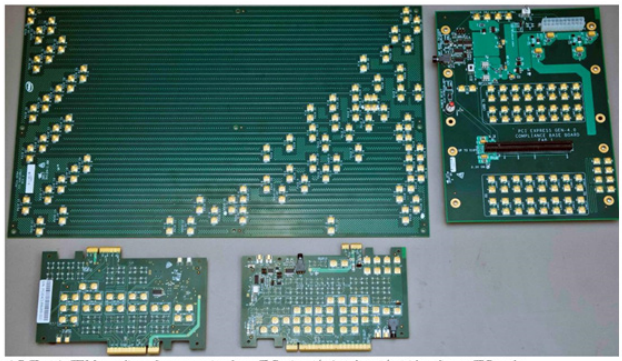
- Test fixtures
- Oscilloscope
- Probe(s)
- Cables
- Software
  - SIGTEST software (SigTest 4.0.46/4.0.51), or similar
  - PCISIG Clock Jitter Tool

There are many tools currently available to help with compliance testing. The following sections list some of the equipment available.

Test Fixtures

Test fixtures are used to connect the probes to the TX pins of the PCIe interface. Fixtures of different interface types are available and are recommended over using adapters to convert the interface Type. Whichever fixture is selected, it must have SMP interconnects to avoid impedance mismatches due to discontinuities.

Table 6. Partial List of PCIe Test Fixtures

Product	Image and Description
PCIe Gen3 CLB/CBB	
PCIe Gen4 CLB/CBB/ISI board	 Figure 3 PCIe 4.0 CEM compliance fixtures consist of two CLBs (a x4/x8 and a x1/x16 board), one CBB and a variable ISI channel board

Note:

CLB is the Compliance Load Board.

- Gen3
- Gen4

There are two different versions of CLB:

- x1/x16 which has x1 and x16 card edges for testing x1 and x16 motherboard slots
- x4/x8 which has x4 and x8 card edges for testing x4 and x8 motherboard slots

ISI board used add extra loss in Gen4.

The Compliance Load Board (CLB) version(s) needed for testing a motherboard depend on the slot widths on the motherboard. All slots on the motherboard must be tested. Ordering information for the CLB can be found on PCISIG website: https://pcisig.com/

Oscilloscope

An oscilloscope is used to measure the signals.

Table 7. Partial List of Oscilloscopes

Company	Product	Image and Description
Keysight	A real time oscilloscope with the bandwidth limited to 25 GHz (maximum bandwidth must be greater than or equal to 25 GHz) and a minimum sample rate of 64 GS/s. 13G for Gen3 at least. 25G for Gen4 at least.	
Keysight	M8000 BERT,16G.	

Probes

Normally, PCIe CEM compliance test uses the high bandwidth cable to connect the oscilloscope to the test fixture. If probes are needed, the following can be used.

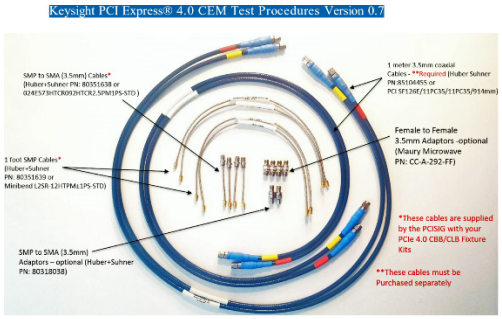
Table 8. Partial List of Probes

Company	Product	Image and Description
Keysight	N2803A,30G. Probe needs the front attachment, based on test environment.	

Cables

Cables are used to measure signal quality.

Table 9. Partial List of Cables

Company	Product	Image and Description
No vendor limited	SMA (male)-SMA (male) cable,25G bandwidth	
	SMA (female)-SMP cable,25G bandwidth	
	SMP-SMP, 25G bandwidth	
	SMA male connector to SMP female connector.25G bandwidth.	
	SMP 50 ohm terminator	

Software

Use of official compliance test software is recommended, but not required. While manually measuring the signal might be just as effective, it must ultimately pass with the compliance software at the compliance house.

Table 10. Recommended Test Software

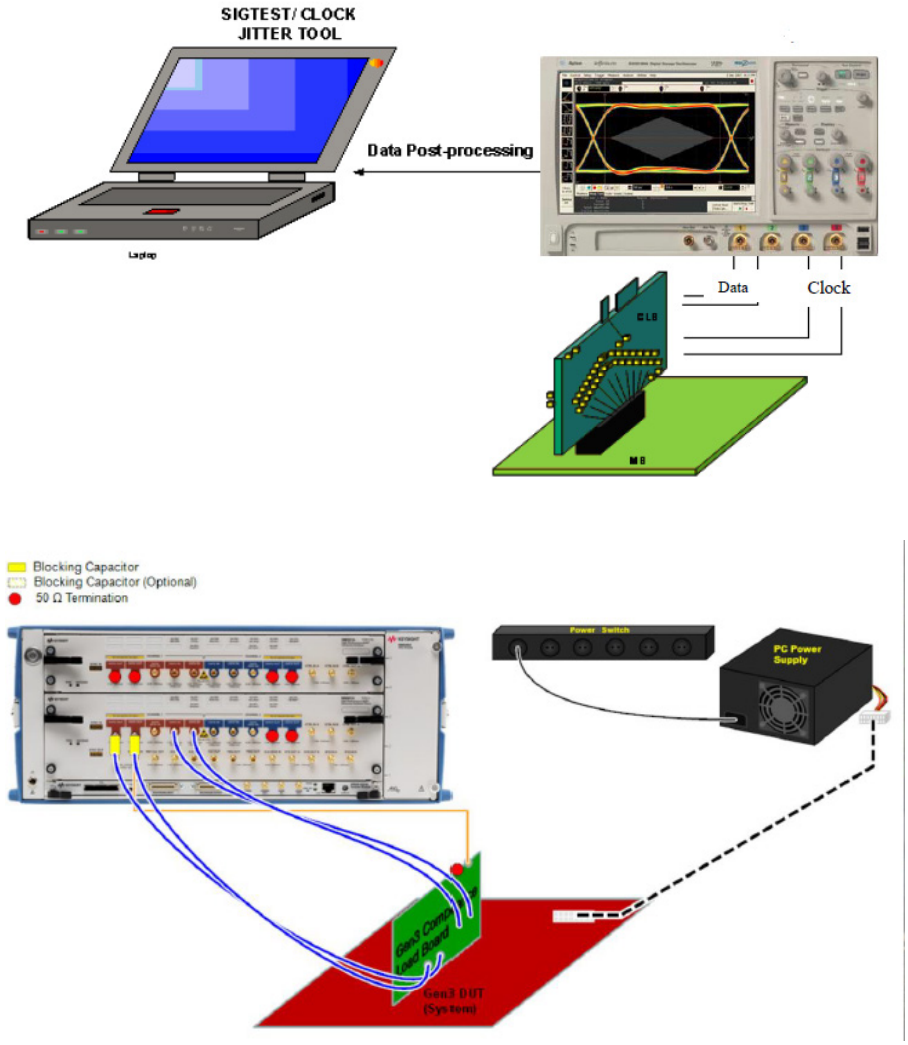
Company	Product	Image and Description
PCISIG	SIGTEST	SIGTEST post processing analysis tool https://www.intel.com/content/www/us/en/design/technology/high-speed-io/tools.html?grouping=rdc%20Content%20Types&sort=title:asc
PCISIG	Clock Jitter Tool	Clock Jitter tool https://www.intel.com/content/www/us/en/design/technology/high-speed-io/tools.html?grouping=rdc%20Content%20Types&sort=title:asc
Keysight	Infiniium SW	https://www.keysight.com/main/software.jspx?ckey=2488819&lc=chi&cc=CN&nid=-32529.1150275&id=2488819
Keysight	IO library SW	https://www.keysight.com/zh-CN/pd-1985909/io-libraries-suite?nid=-33002.977662&cc=CN&lc=chi
Keysight	M8070 BERT	https://www.keysight.com/zh-CN/pd-2449505-pn-M8070A/system-software-for-m8000-series-of-ber-test-solutions?nid=-32914.1100508&cc=CN&lc=chi
Bitifeye	N5990 SW	https://www.bitifeye.com/download/.

PCIe Compliance Testing Setup Example

Figure 1 is a setup example for PCIe compliance testing. The following list applies to Figure 1.

- TX:
  - CPU mode CEM test need Clock and data both.
  - Every PC can install SigTest and clock jitter tool, suggest using a high-performance PC.
  - SW ready, that means SW enable PCIE IP.
  - If test is not lane 0, suggest using 50ohm SMP terminator on un-test lanes.
  - Alternate Method of System TX Signal Quality Test at 16GT/s
- RX:
  - Need RX calibration first in Gen3/4
  - Rx EQ need BERT support Protocol feature.
  - RX test are different between CTS 3.0 and CTS 4.0

Figure 1. PCIe Compliance Testing Setup Example



PCIe Compliance Testing

PCISIG provides the compliance standards and test descriptions for system boards and add-in cards that comply with that latest version of the *PCI Express Card Electromechanical Specification*. Customers should refer to the document for an overview of the tests that are performed to check the compliance criteria. Depending on the brand of equipment being used for the test, customers can then refer to the manufacturer's documentation for step-by-step procedure to perform the test.

PCI Express specification require devices to have a built-in mechanism for testing the electrical characteristics. Therefore, when the transmit lanes of the device are terminated with a 50-ohm load, the transmit lanes will automatically be forced into compliance mode.

In order to keep the PCIe controller enabled, the patch (8660b87.diff) attached to this application note should be applied.

Commands to apply patch:

```
git am 8660b87.diff
```

To access the attached file(s), click the **Attachment** icon on the left-hand toolbar on this PDF (using Adobe Acrobat Reader or Adobe Acrobat). Select the file and use the Tool Bar options (**Open, Save**) to retrieve the file(s).

Testing with PCI Express Devices

For compliance testing, CLB v3.0/4.0 which is the Compliance Load Board is required. If the DUT has an onboard PCIe device and hence does not have a PCIe slot or connectors, then the PCI device should be taken off from the board for CLB v3.0/4.0 to be hooked up.

TX Compliance Pattern Sequence

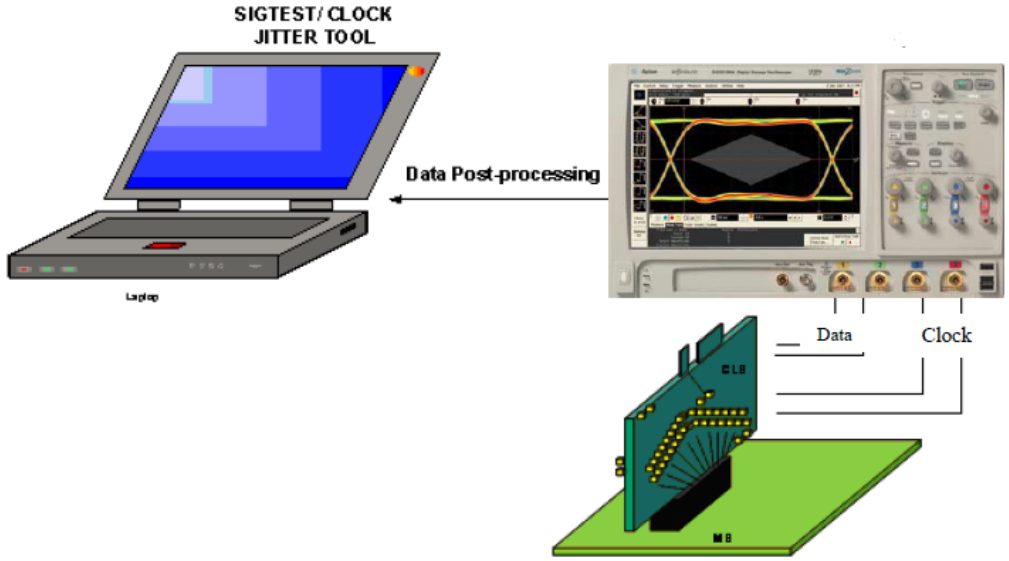
- Default power on: 2.5GT/s (-3.5dB) mode
- First toggle: 5GT/s (-3.5dB) mode
- Second toggle: 5GT/s (-6dB) mode
- Third-Thirteenth toggle: 8GT/s (P0-P10), PCIe 3.0 mode
- Fourteenth to Twenty-fourth toggle: (P0-P10), PCIe 4.0 mode

TX_GEN1/2/3 Test

Use the following steps for TX_GEN1/2/3 testing.

1. Insert CLB 3.0/4.0 on the PCIe slot
2. Connect data and clock cable from CLB to oscilloscope
3. Connect J5/J85 to Rx Lane 0 used for pattern sequence change
4. Power on DUT, enable PCIe software if needed.
5. Use differential mode, data → ch1-ch3, clock → ch2-ch4.
6. Set scale (20 µs)/Bandwidth (13G at least)/memory depth (10M)/Sample rate (40G).
7. Toggle the button and change compliance pattern sequence, capture the data and clock → *.bin, be sure the UI number meet the required:
   a). Gen1, 10E6 X 400.0ps = 400.0 µs
   b). Gen2, 10E6 X 200.0ps = 200.0 µs
   c). Gen3, 10E6 X 200.0ps = 200.0 µs
8. Note if SSC is on or off

Figure 2. TX_GEN1/2/3 Test Connection Example

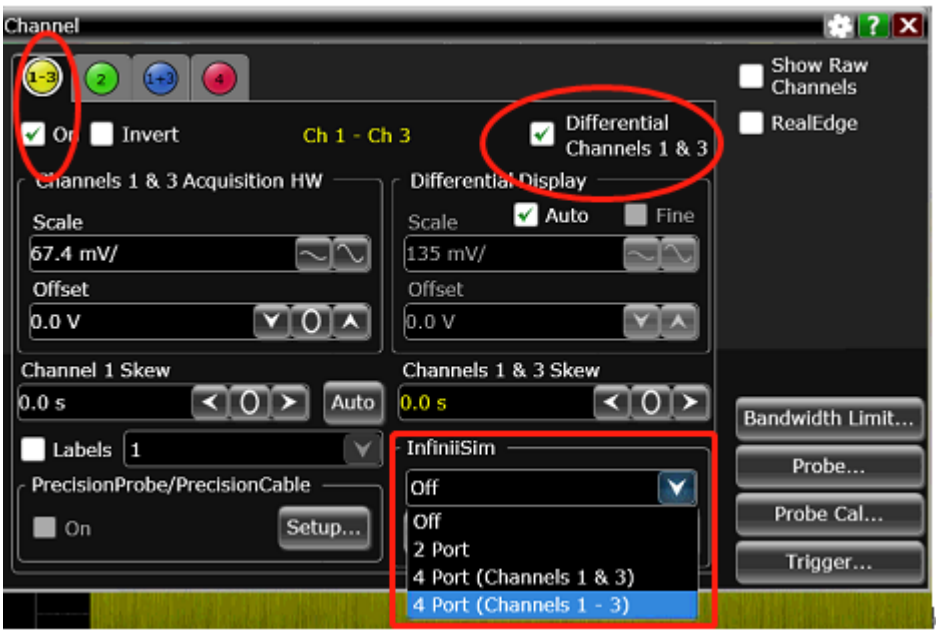


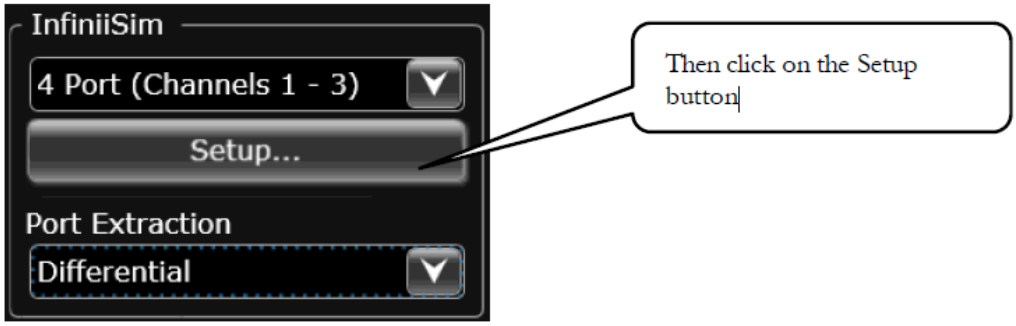
TX_GEN4 Test

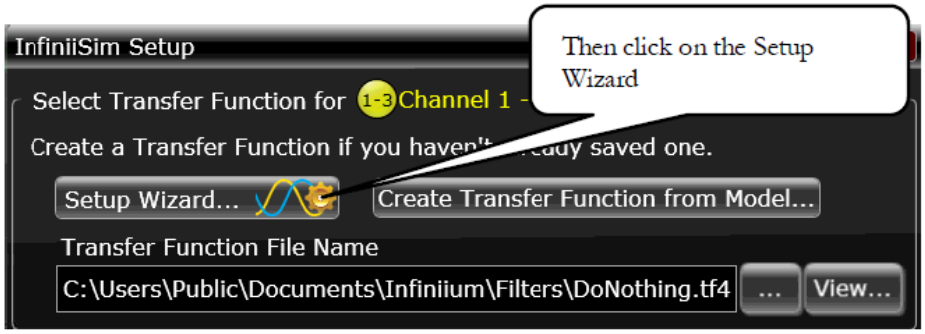
Use the following steps for TX_GEN4 testing.

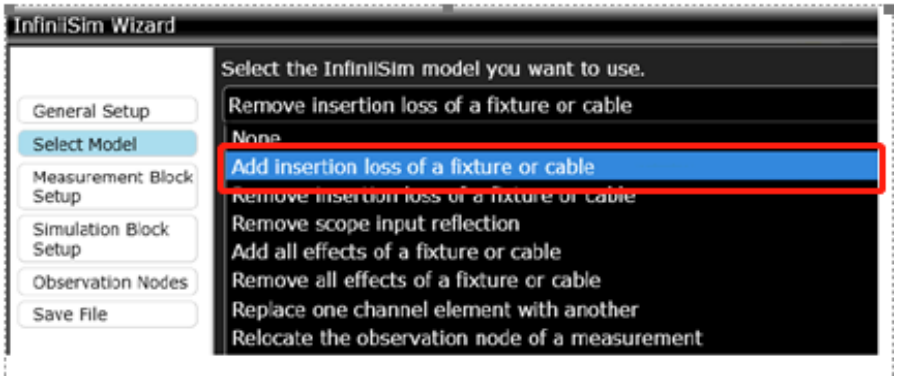
1. Insert CLB 4.0 on the PCIe slot
2. Add ISI board loss to meet PCIe compliance requirement (VNA can take this loss)
3. Connect clock to OSC, Data: CLB →Cable →ISI board →Cable →OSC
4. Connect J5/J85 to Rx Lane 0 used for pattern sequence change
5. Power on DUT, enable PCIe software if needed
6. Use differential mode, data →ch1-ch3, Enable infiniiSim function on Data, *refpkg_endpoint_3db_thru.s4p* in the SigTest folder, clock →ch2-ch4
7. Set scale (12.5 µs)/Bandwidth (25G at least)/memory depth (10M)/Sample rate (80G).
8. Toggle the button and change compliance pattern sequence, capture the data and clock →*.bin, be sure the UI number meet the required

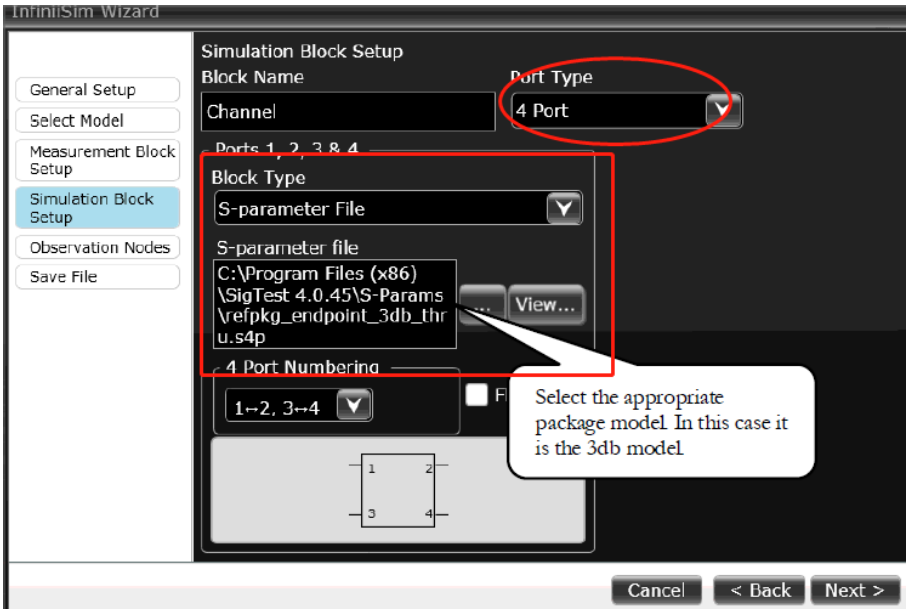
   a). Gen4, 2.0 X 10E6 X 62.5ps = 125.0µs
9. Note if SSC is on or off


Channel
Show Raw Channels
RealEdge
Invert
Ch 1 - Ch 3
Differential Channels 1 & 3
Channels 1 & 3 Acquisition HW
Differential Display
Scale
67.4 mV/
Offset
0.0 V
Auto
Fine
135 mV/
Channel 1 Skew
Channels 1 & 3 Skew
0.0 s
Labels
PrecisionProbe/PrecisionCable
On
Setup...
InfiniiSim
Off
2 Port
4 Port (Channels 1 & 3)
4 Port (Channels 1 - 3)
Bandwidth Limit...
Probe...
Probe Cal...
Trigger...


InfiniiSim
4 Port (Channels 1 - 3)
Setup...
Port Extraction
Differential
Then click on the Setup button

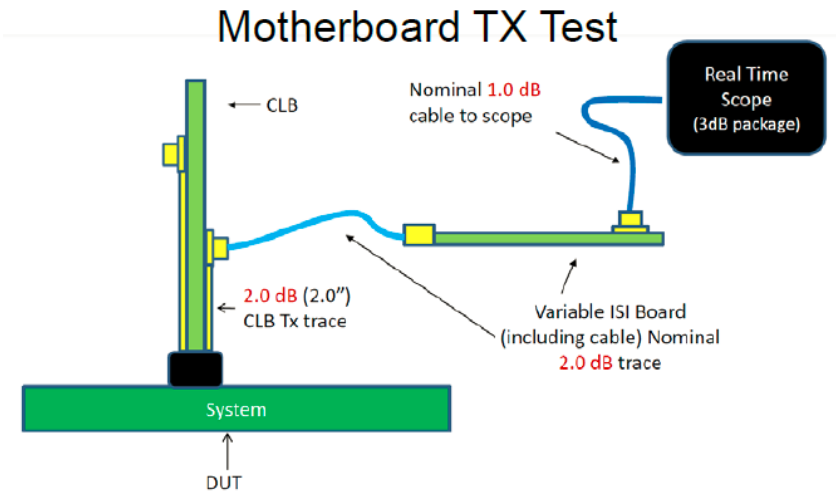

InfiniiSim Setup
Select Transfer Function for
Channel 1 -
Create a Transfer Function if you haven't
saved one.
Setup Wizard...
Create Transfer Function from Model...
Transfer Function File Name
C:\Users\Public\Documents\Infiniium\Filters\DoNothing.tf4
...
View...
Then click on the Setup Wizard


InfiniiSim Wizard
General Setup
Select Model
Measurement Block Setup
Simulation Block Setup
Observation Nodes
Save File
Select the InfiniiSim model you want to use.
Remove insertion loss of a fixture or cable
None
Add insertion loss of a fixture or cable
Remove scope input reflection
Add all effects of a fixture or cable
Remove all effects of a fixture or cable
Replace one channel element with another
Relocate the observation node of a measurement



10. Alternate method of system TX signal quality test at 16 GT/s

Figure 3. TX_GEN4 Test Connection Setup Example



Alternate Method of System TX Signal Quality Test at 16 GT/s

An alternate method of performing 16 GT/s system signal quality test is provided here. The data and 100 MHz reference clock can be captured and post-processed separately. The data will be processed with SigTest using the 16 GT/s add-in card signal quality template file (PCIe_4_16G_CEM.dat). The pass/fail limits for eye width at 1E-12 and eye height at 1E-12 will

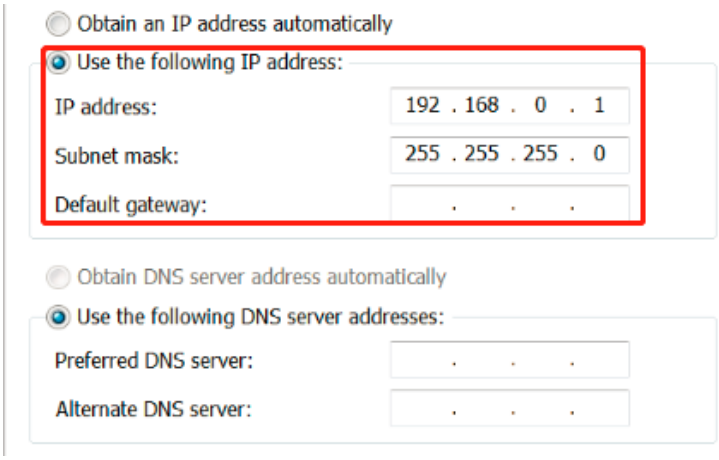
remain unchanged for 16 GT/s system signal quality test. The reference clock will be post-processed with a separate clock tool to ensure the random jitter is less than equal to 0.7 ps RMS as defined in the *PCI Express Base Specification*.

The signal quality test is the required test method for System TX signal quality testing at 16 GT/s. This alternate method is only to be used when the signal quality test fails.

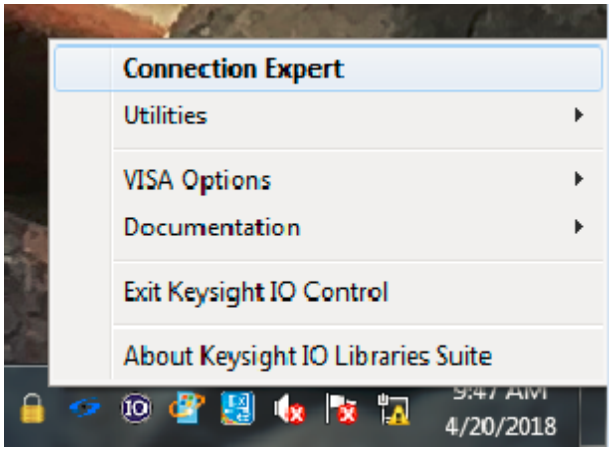
RX_SETUP

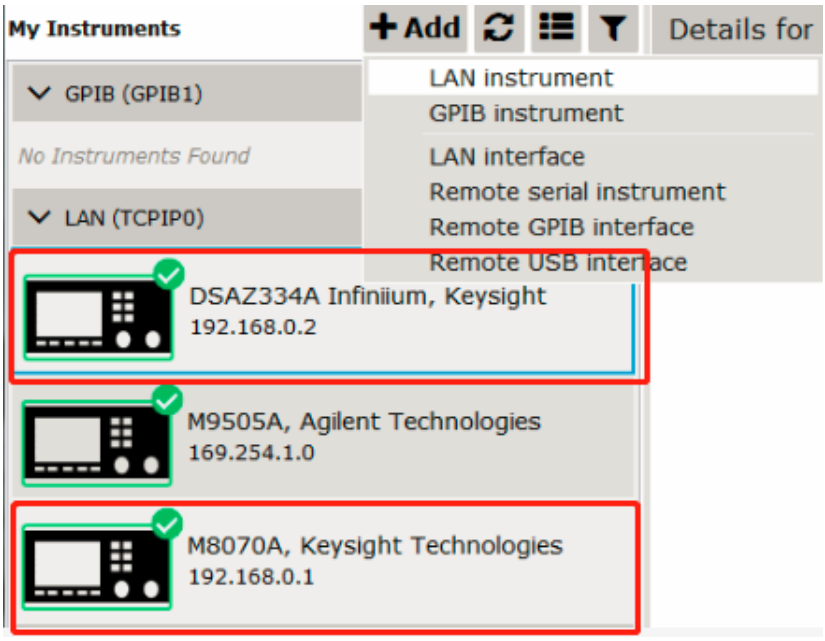
Use the following steps for RX_SETUP.

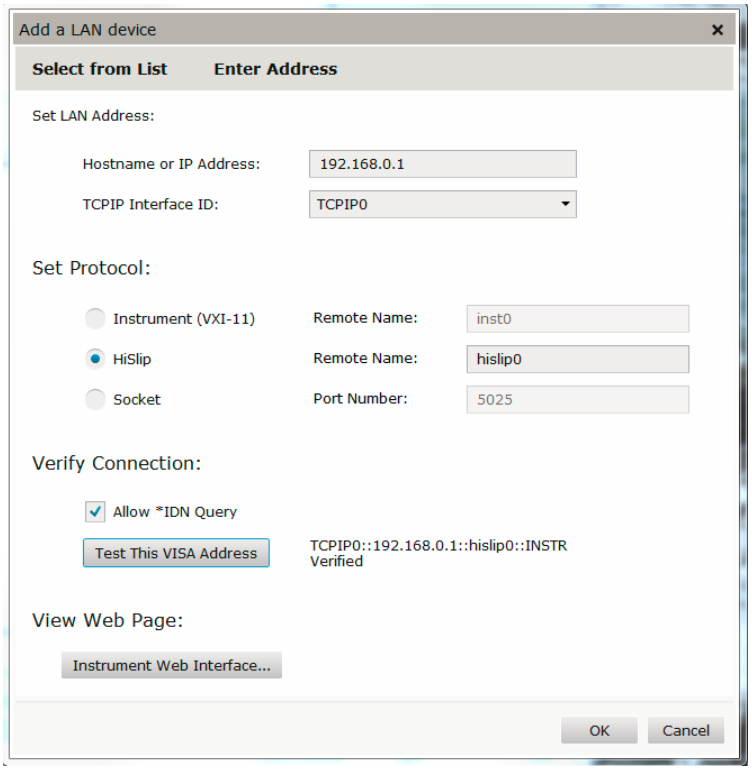
1. Install M8070 SW/Install SigTest/Install N5990.
2. Launch up M8070A SW first. Note: M8070A must start before connection setting.
3. Set Local network:
   a). Install or update software on J-Bert and oscilloscope, close window firewall
   b). Set Local Area network among host and equipment
   c). Bert: 192.168.0.1; OSC: 192.168.0.2



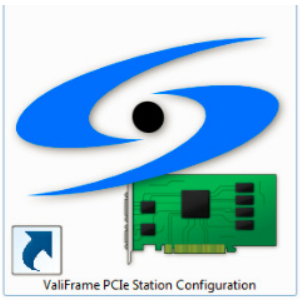
4. Open the BERT IO control software on M8000

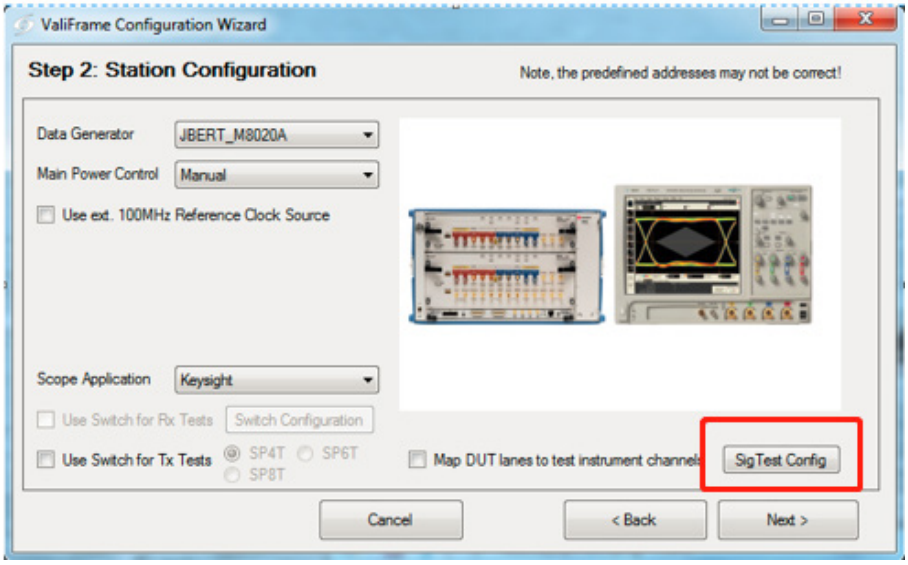




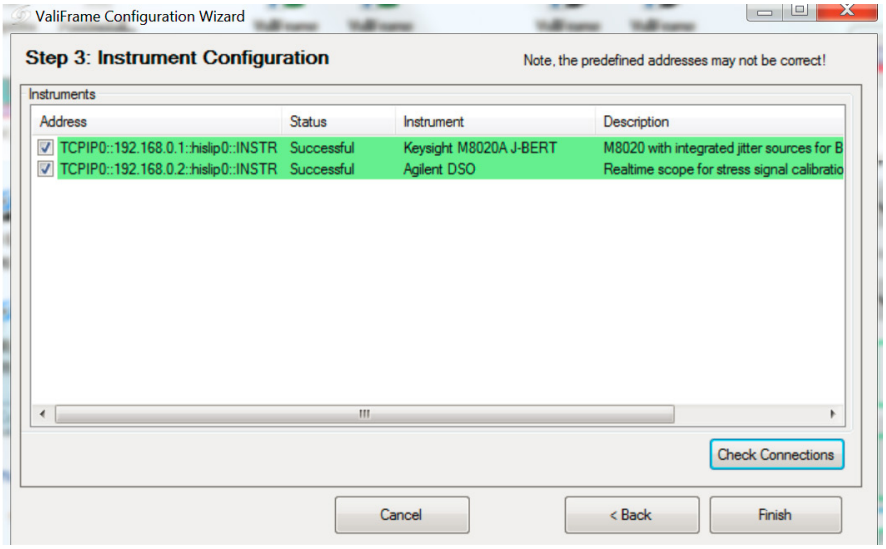


5. PCIe station configuration. Note: the SigTest version and route location





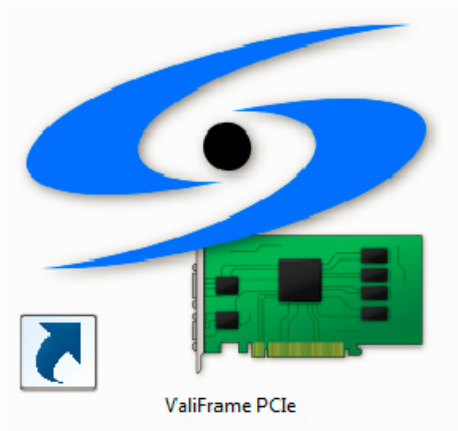
6. Input address detail information

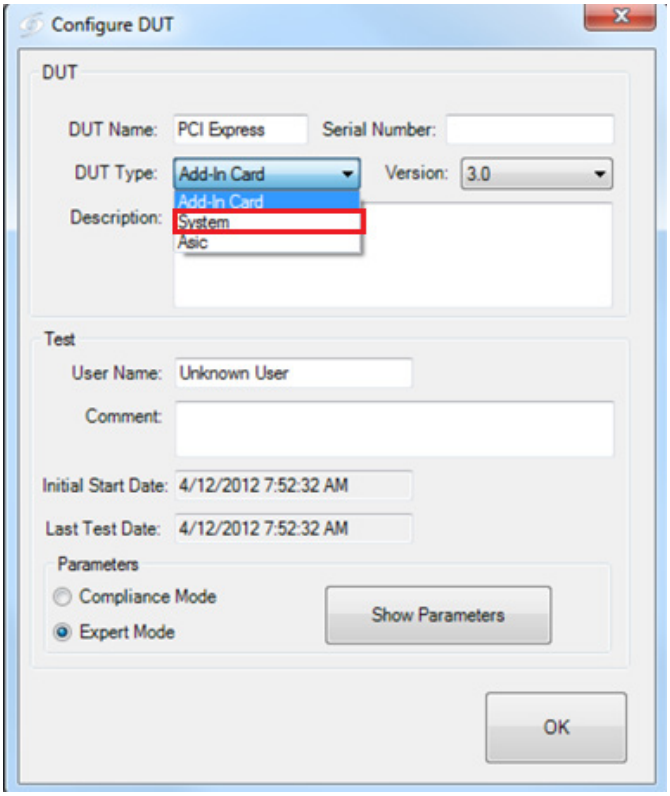


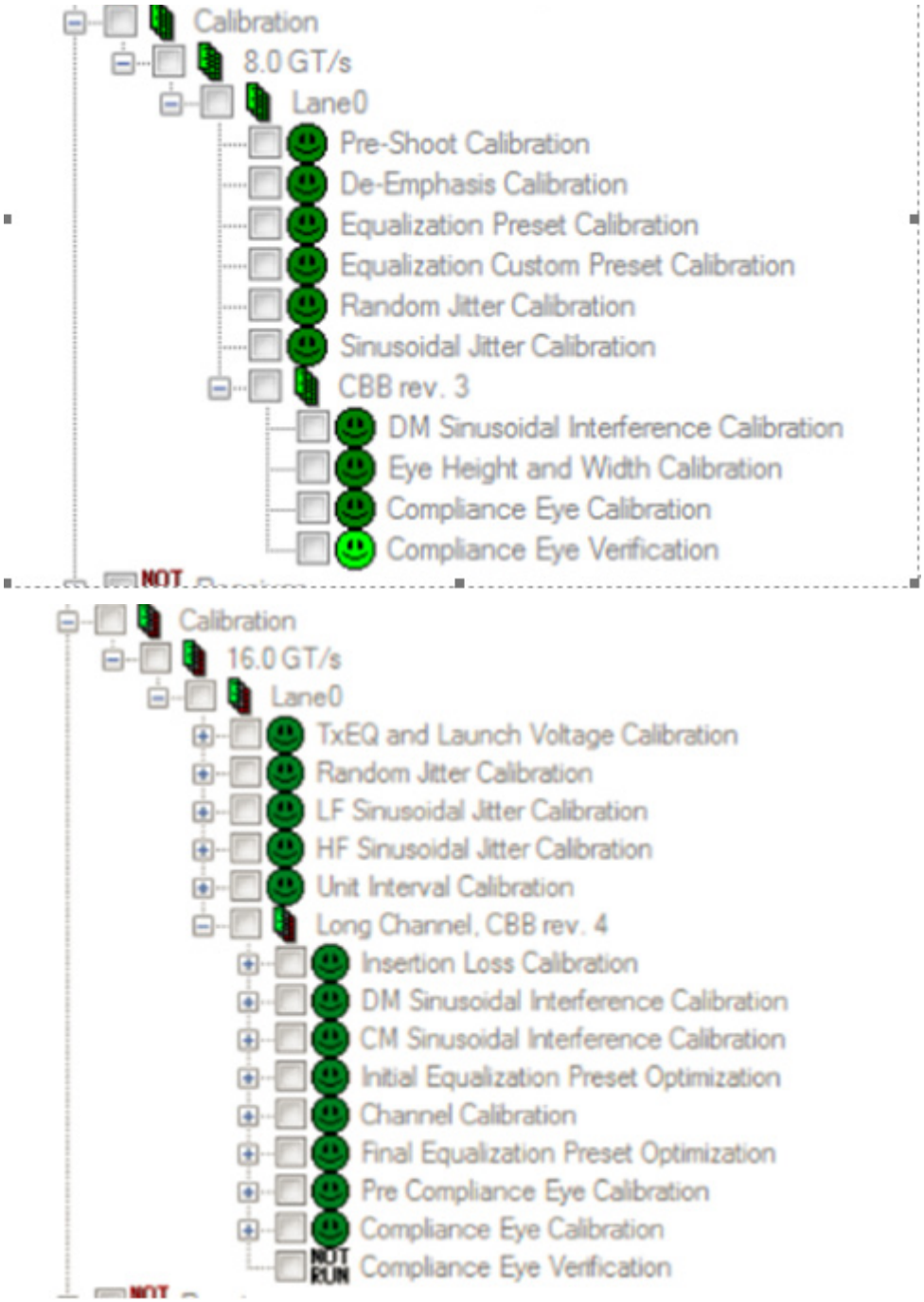
RX_GEN3/4 Calibration

Use the following steps for RX_GEN3/4 calibration.

1. Select the System related items.
2. Execute the All calibration items.
3. Every step connection will show at the start.
4. After calibration pass, then are green smile face.



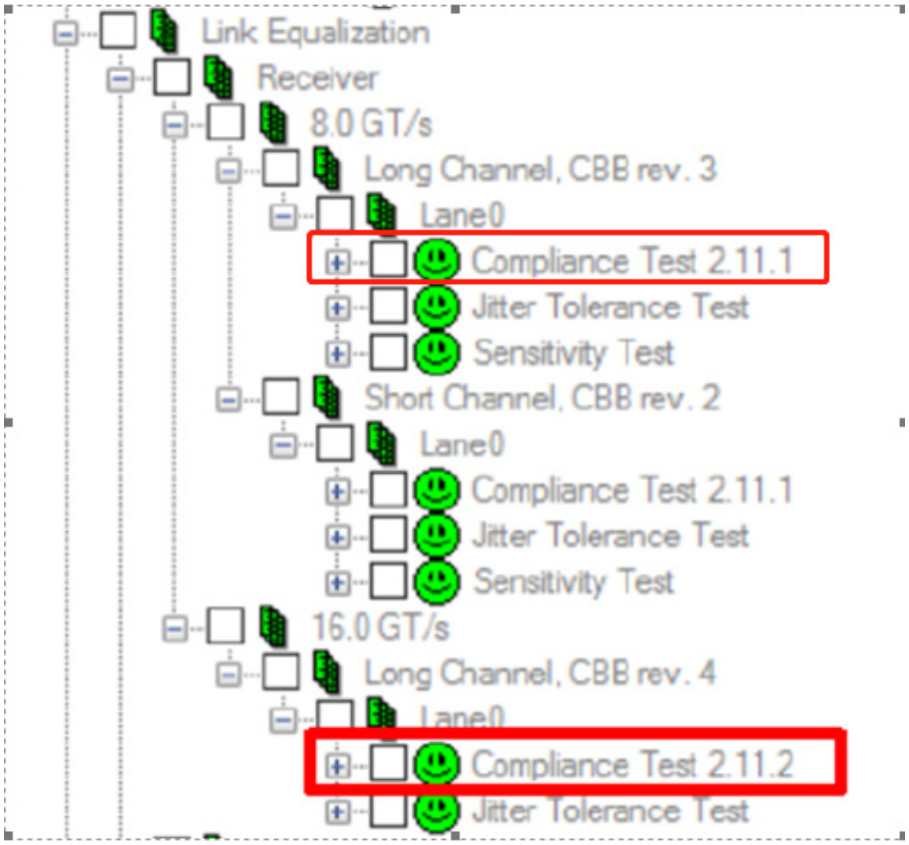



Calibration
8.0 GT/s
Lane0
Pre-Shoot Calibration
De-Emphasis Calibration
Equalization Preset Calibration
Equalization Custom Preset Calibration
Random Jitter Calibration
Sinusoidal Jitter Calibration
CBB rev. 3
DM Sinusoidal Interference Calibration
Eye Height and Width Calibration
Compliance Eye Calibration
Compliance Eye Verification
Calibration
16.0 GT/s
Lane0
TxEQ and Launch Voltage Calibration
Random Jitter Calibration
LF Sinusoidal Jitter Calibration
HF Sinusoidal Jitter Calibration
Unit Interval Calibration
Long Channel, CBB rev. 4
Insertion Loss Calibration
DM Sinusoidal Interference Calibration
CM Sinusoidal Interference Calibration
Initial Equalization Preset Optimization
Channel Calibration
Final Equalization Preset Optimization
Pre Compliance Eye Calibration
Compliance Eye Calibration
NOT RUN
Compliance Eye Verification

RX_LINK EQ Test, Gen3/4

Use the following steps for RX_LINK EQ testing for PCIe Gen3 and Gen4 testing.

1. Select the system related items
2. Run start
3. Connection will show at the start
4. After test, there is a green smile face or a red face



TX Signal Qualification Steps

Use the following steps for TX signal qualification.

1. Flash L4T to the DUT.
2. Connect all cables and fixtures as documented.
3. Power on DUT and board will boot to L4T.
4. In L4T idle, Gen1 signal might be seen on scope. Toggle CLB to switch speed and preset.
5. Capture waveforms and analyze by SigTest.

Notes: The following register writes might be required to Qual Gen4 as software might only support up to Gen3.

For PEX x1:

- Clear bit[7] in address 0x14160004
- Set bit[0] in address 0x360008bc
- Set bit[0:3] to 0x4 in address 0x3600007c
- Set bit[0:3] to 0x4 in address 0x360000a0
- Set bit[7] in address 0x14160004

For PEX x4:

- Clear bit[7] in address 0x141A0004
- Set bit[0] in address 0x3A0008bc
- Set bit[0:3] to 0x4 in address 0x3A00007c
- Set bit[0:3] to 0x4 in address 0x3A0000a0
- Set bit[7] in address 0x141A0004

RX Signal Qualification Steps

Use the following steps for RX signal qualification.

1. Flash L4T to the DUT.
2. Connect all cables and fixtures as documented.
3. Power on DUT and board will boot to L4T.
4. Start test from SW on Bert.

Note: The default test mode for RX test in the test software is “interactive mode.” Change to “static sequence” if DUT is having issue to enter loopback mode.

Debugging

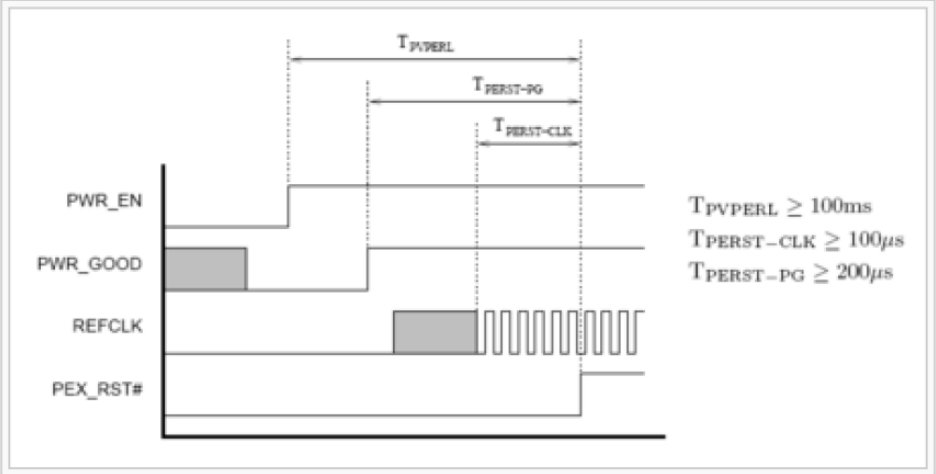
High speed I/O design is difficult to debug and will get harder as speeds increase. The following are a few common PCI Express issues.

If PCI Express does not Work

If PCI Express does not respond or no signals are being sent out, verify the following:

1. Check the applied power for expected value.
2. Check that clocks are on.
3. Check for chip reset de-assertion.
4. Check the power sequencing.

Figure 4. Power Sequence Diagram



Device Fails at ASPM L0/L1 Enabled

Connect device to a PCIe bus analyzer (ie LeCroy Protocol Analyzer) to assist with the debug.

1. Configure analyzer to trigger on root repeatedly sending PM_Request_Ack DLLPs
2. Capture the bus traffic at the time the bus failure occurs

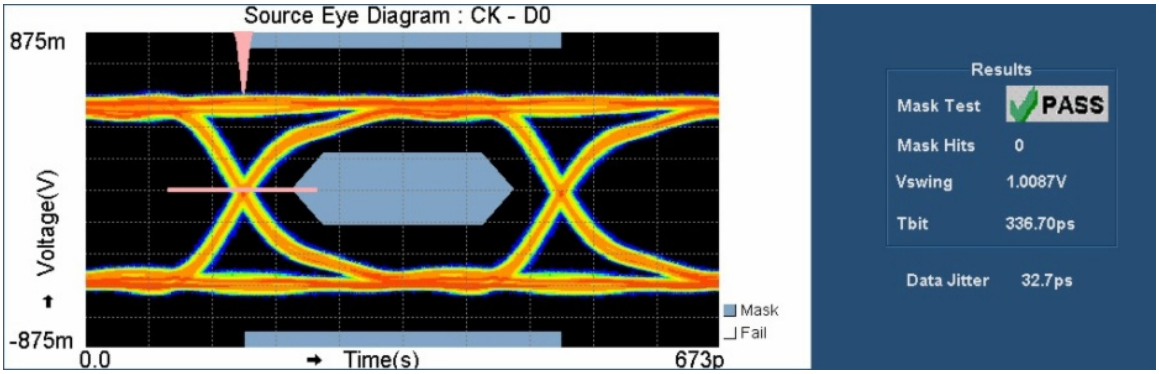
Jetson Xavier NX Series HDMI Tuning Guide

The NVIDIA Jetson Xavier NX includes HDMI™ technology; this chapter describes the registers and steps needed to tune the HDMI signals output from the NVIDIA® Xavier™ system on chip (SoC).

In order to meet HDMI compliance, tuning may be required to adjust the TMDS signal such that the voltage swing is close to 500 mV ± 100 mV single-ended, or 1000 mV ± 200 mV differentially. This is to ensure the signal integrity is clean, meets the HDMI specifications, and the device is optimized for low power consumption.

Note: Prior to any tuning, scope and probes must be calibrated. Refer to the documentation for your scope and probe for instructions on how to calibrate.

Figure 5. Source Eye Diagram: CK-D0



Abbreviations and Definitions

Table 11 lists the abbreviations that may be used throughout this application note and their definitions.

Table 11. Abbreviations and Definitions

Abbreviation	Definition
CTS	Compliance Test Specification
DUT	Device Under Test
EMI	Electromagnetic Interference
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
PVT	Process, Voltage, and Temperature
RF	Radio Frequency
Sink	Any type of receiver, such as a display or panel
SOR	Serial Output Resource – Module naming referring to the HDMI block
Source	Any type of transmitter, such as Xavier
TMDS	Transition-Minimized Differential Signaling

HDMI Tuning Setup

This section describes the HDMI tuning setup.

HDMI Tuning Required Equipment

There are many tools currently available to perform the HDMI tuning. The following components are required:

- Test fixture
- Oscilloscope
- Probes
- DC power supply
- Software
  - HDMI compliance software
  - Tools to access register space in Xavier

The following subsections list some of the acceptable equipment that may be used.

Note: The items highlighted with green in the following sections are the tools that NVIDIA used for validation and tuning. This guide will refer to those tools specifically for the rest of this chapter.

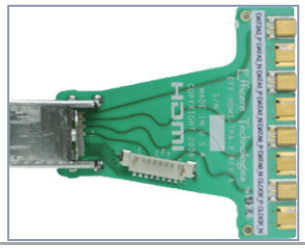
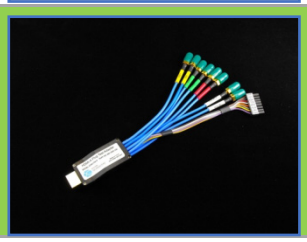
Test Fixture

Test fixtures are used to connect the probes to the output of the HDMI interface. The following example fixtures listed use the Type-A interface for HDMI 1.4b compliance. Fixtures of different interface types are available and are recommended instead of using adapters to convert the interface type.

For HDMI 2.0 compliance, ensure that the test fixture can support the higher bitrate with minimal insertion loss.

The fixture selected must have SMA interconnects to avoid impedance mismatches due to discontinuities.

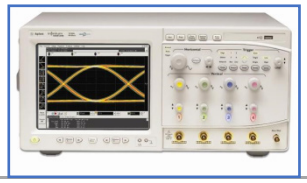
Table 12. Partial List of Acceptable HDMI Test Fixtures Type A

Efficere	**EFF-HDMI-TP-P**	
Agilent	**N1080A**	
Wilder Tech	**HDMI-TPA-P**	

Oscilloscope

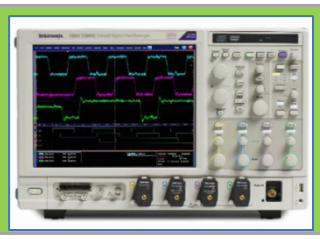
The scope is used to display and measure the signals. The HDMI 1.4 specification requires that the scope has at least 8 GHz of bandwidth and a sampling rate of at least 10 GS/s if the pixel clock is equal to or less than 165 MHz, or sampling rate of at least 20 GS/s if the pixel clock is greater than 165 MHz.

Table 13. Partial List of Acceptable Oscilloscopes for HDMI 1.4 Tuning

Tektronix	**TDS6804B or better**	
Agilent	**DS080000B or better**	

For HDMI 2.0, a scope with at least 16 GHz of bandwidth is recommended.

Table 14. Partial List of Acceptable Oscilloscopes for HDMI 2.0 Tuning

Tektronix	**DPO/MSO 70000 series 16 GHz or better**	
Agilent	**Infinium 90000 series 16 GHz or better**	

Probes

Probes are used to connect the scope to the test fixture. The probes must have at least 8 GHz of bandwidth for HDMI 1.4b testing and at least 12 GHz of bandwidth for HDMI 2.0 testing.

At least two (2) probes are required for tuning, four (4) probes are ideal.

Untested lanes must be terminated appropriately. See the "DC Power Supply" section for details.

Table 15. Partial List of Acceptable Probes

Tektronix	**P7313SMA**	
Agilent	**1169A Requires Agilent N5380A**	
Agilent	**N5380A Used with Agilent 1169A**	

DC Power Supply

Any power supply that can supply a constant voltage of 3.3V is needed to terminate the HDMI signals. Refer to the probe's instruction manual on how to supply this termination voltage to the probes.

Note: All untested lanes must be terminated to 3.3V using 50 Ω terminators. Irrespective of the tools used, it is important to make sure that they are calibrated and meet industry standards in order to obtain accurate measurements.

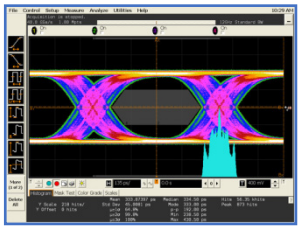
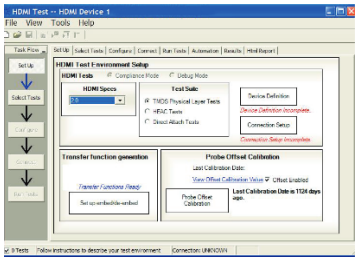
HDMI Tuning Software

This section describes the software used for HDMI tuning.

HDMI Compliance Test Software

NVIDIA recommends that the official compliance test software be used to ensure accurate results. Although manually measuring the signal may be as effective, it must ultimately pass with the compliance software at the compliance house.

Table 16. Partial List of Acceptable Test Software

HDMI 1.4b Testing		HDMI 2.0 Testing	
Tektronix TDSHT3 or later		**TekExpress HDM or later**	
Agilent N5399A or later		**Agilent N5399C or later**	

Xavier Software Tools

Consult your software team or contact your NVIDIA representative for assistance with software tools to access the register space in Xavier.

HDMI Method for Tuning

Tuning is done by running the eye diagram tests on each of the data lanes while shmoo'ing the applicable registers. The objective is to keep the differential voltage swing as close to 1000 mV as possible, while providing the eye diagram enough margin to meet HDMI specifications.

Internal Termination

To effectively shmoo for the correct voltage swing, the drive strength can be estimated by calculating the parallel resistance to AVDD_HDMI/AVcc, assuming exact 50 ohms to 3.3V in the receiver. The equivalent resistance can be calculated based on the internal resistance settings. Then refer to the register description section for the current per drive strength tap to calculate the voltage swing.

With the equivalent termination and current per drive strength, the approximate voltage swing can be calculated. However, for higher speeds and routing differences, increased drive strength and pre-emphasis may be needed to overcome signal loss due to routing or EMI damping components.

On Xavier, the internal termination has an internal calibration mechanism which calibrates the internal termination to 50Ω, depending on the external RSET value, silicon variation and temperature variation.

Procedures

Calibrate the scope and probes before you begin. Refer to your scope and probe user manuals for details on how to calibrate.

DUT

This guide does not cover setup of HDMI at any specific resolution. Work with your software team and NVIDIA representative to prepare the DUT for testing. Following are the general steps to set up the HDMI connection.

1. Disable Hot Plug Detect: The driver or OS may disable HDMI output if it detects the panel being disconnected. Try the following methods to prevent that:
   a). **Method #1:** Disable the HPD interrupt via software by setting the HPD pin to TRISTATE.
   b). **Method #2:** Disconnect the HPD circuit from the HDMI connector, manually rework HPD circuit to a desired voltage level to input to Xavier to make the software consider HDMI is still connected.

   (Refer to the carrier I/O board schematics for how to do that. If this method is chosen, the circuit must be restored before performing the HDMI certification tests.)
2. Configure the DUT to drive HDMI at the supported resolutions: 480p (27 MHz), 720p (74.25 MHz), 1080p (148.5 MHz), 2160p/30 (297 MHz), or 2160p/60 (594 MHz).
3. Attach the test fixture to the DUT.

4. Attach the probe-ends to the test fixture, and properly connect the termination voltage to the probes. Untested lanes must be properly terminated.
5. Attach the probes to the scope.

Note: For using an HDMI converter (to GMSL/FPD link/MIPI, etc) design on board, HDMI CTS is not required. To check the HDMI signal quality from Xavier, probe the HDMI signals closest to the input of the HDMI converter to confirm if the signals meet the HDMI source electrical spec or HDMI converter's input electrical spec.

Oscilloscope

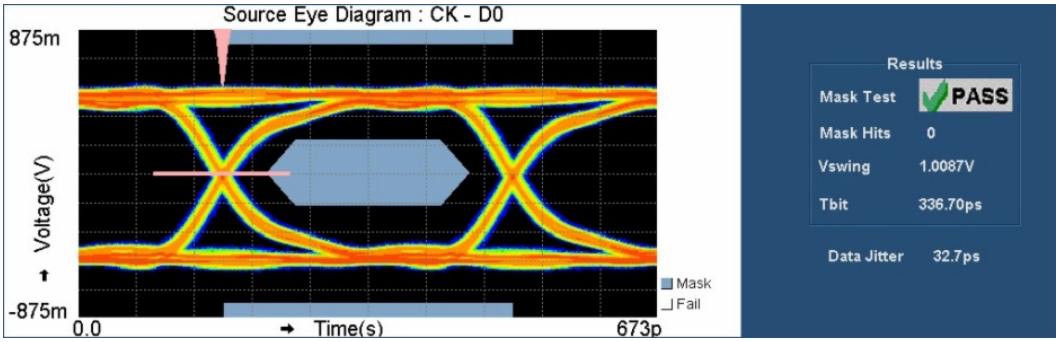
1. Ensure the probes are using the termination voltage of 3.3V.
2. Start the HDMI compliance software.
3. Set up the HDMI compliance software to take the Eye Diagram and configure the probes to the proper clock and data assignments.
4. Run the eye diagram test.
5. Check the voltage swing and margin result (see Figure 6).
6. Refer to Registers section and note the internal termination, drive strengths, and pre-emphasis settings.
7. Repeat for all data lanes, using different register settings, at all supported resolutions.

! Tips:

When shmoo'ing drive strengths or pre-emphasis, keep the same value across each data lane. The HDMI pads for each of the data pairs and the clock are the same and should have very minor variation.

Since HDMI clock has less transitions than data, its settings can be weaker than the data lanes. This can save some power and lower possible noise or EMI.

Figure 6. Voltage Swing and Margin Results



Objectives

While there is no margin specification, a good rule of thumb is to provide:

- At least 40 mV of margin above and below the eye mask
- Voltage swing of around 1000 mV
- Find settings for:
  - 480p
  - 720p
  - 1080p
  - 2160p/30
  - 2160p/60

> **!** Tips:
> - Lower drive strength, IO peak current, and pre-emphasis settings will lower the power consumption.
> - Fast rising/falling edges will contribute to increased EMI.

Voltage Swing Target

This guide targets a differential voltage swing of 1000 mV.

The target can be lowered to help reduce EMI and RF related issues.

> **!** CAUTION: Note that if the user lowers the differential voltage swing target, the user assumes complete responsibility for issues or consequences arising as a result. In addition, the user must test random parts to ensure HDMI compliance with the new differential voltage settings.

Registers

The Serial Output Resource (SOR) module can be configured to output HDMI or VESA® DisplayPort™ (DP). Jetson Xavier NX has 2x instances of the SOR0~1 for DP0~1 pins. SOR0 controls the DP0 pins and SOR1 controls DP1.

The following table lists the detail registers to tune the Xavier Drive Strength, Pre-Emphasis Controls, etc.

Table 17. HDMI_DP0~1 (SOR0~1) Registers

Register Name	Bit Fields	Description	Notes
SOR_NV_PDISP_SOR_PLL1_0 (Address: 0x15b005a8) SOR_NV_PDISP_SOR_PLL1_1 (Address: 0x15b405a8)			
RESERVED	31:16	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
TMDS_COMPOUT	15:15	Internal Termination Calibration Comparator Output	When calibrating the internal termination, this read-only register will output 0 if the termination is lower than 50Ω and 1 if the termination is higher.
RESERVED	14:14	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
TMDS_TERMADJ	12:09	Internal Termination Resistance Control	Requires TMDS_TERM to be enabled.
TMDS_TERM	08:08	Internal Termination Enable	Enables internal termination
RESERVED	07:00	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
SOR_NV_PDISP_SOR_PLL3_0 (Address: 0x15b005b0) SOR_NV_PDISP_SOR_PLL3_1 (Address: 0x15b405b0)			
RESERVED	31:28	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
BG_VREF_LEVEL	27:24	Bandgap Voltage Level	Changes the reference voltage used to generate the current for the pads. Higher settings equate to higher current draw per tap for DRIVE_CURRENT and PREEMPHASIS.
RESERVED	23:00	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
SOR_NV_PDISP_SOR_LANE_DRIVE_CURRENT0_0 (Address: 0x15b00138) SOR_NV_PDISP_SOR_LANE_DRIVE_CURRENT0_1 (Address: 0x15b40138)			
LANE3_DP_LANE3	31:24	Drive Strength Controls for the Clock Lane for HDMI and Lane 3 for DP/eDP	Each tap increases the drive strength by 0.400mA, with a base of 0.000mA. 000.0000 → 0.000mA 000.0001 → 0.400mA ... 011.0000 → 19.200mA (starting to borrow from pre-emphasis drivers) 100.0111 → 28.200mA (max)
LANE2_DP_LANE0	23:16	Drive Strength Controls for Lane 2 for HDMI and Lane 0 for DP/eDP	
LANE1_DP_LANE1	15:08	Drive Strength Controls for Lane 1 for HDMI and Lane 1 for DP/eDP	

Register Name	Bit Fields	Description	Notes
LANE0_DP_LANE2	07:00	Drive Strength Controls for Lane 0 for HDMI and Lane 2 for DP/eDP	100.1000→25.400mA
SOR_NV_PDISP_SOR_LANE_PREEMPHASIS0_0 (Address: 0x15b00148) SOR_NV_PDISP_SOR_LANE_PREEMPHASIS0_1 (Address: 0x15b40148)			
LANE3_DP_LANE3	31:24	Pre-Emphasis Controls for the Clock Lane for HDMI and Lane 3 for DP/eDP	Pre-emphasis controls take lower precedence than drive strength and may not have any noticeable effect at higher drive strengths. Refer to the TRM for more detailed information.
LANE2_DP_LANE0	23:16	Pre-Emphasis Controls for Lane 2 for HDMI and Lane 0 for DP/eDP	
LANE1_DP_LANE1	15:08	Pre-Emphasis Controls for Lane 1 for HDMI and Lane 1 for DP/eDP	
LANE0_DP_LANE2	07:00	Pre-Emphasis Controls for Lane 0 for HDMI and Lane 2 for DP/eDP	
SOR_NV_PDISP_SOR_DP_PADCTL0_0 (Address: 0x15b005b8) SOR_NV_PDISP_SOR_DP_PADCTL0_1 (Address: 0x15b405b8)			
RESERVED	31:24	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
PAD_CAL_PD	23:23	Pad Calibration Power Down	Set to 0 to enable calibration, 1 to disable
TX_PU	22:22	Transmitter pull-up resistors.	Enables the pull-ups for the current sources.
RESERVED	21:16	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
TX_PU_VALUE	15:08	TX pull-up current source drive	Provides additional current for the current drivers. Can help improve the transition edge speeds and overall voltage swings.
RESERVED	07:00	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.

Xavier Register Settings

The following table describes the default settings that passed HDMI compliance on NVIDIA Jetson Xavier NX Devkit across PVT. Refer to the previous tables for register descriptions.

Note: The settings may differ with customized carrier I/O board as the signal path differs (for example, different trace layout or connection through a flex cable).

Table 18. Xavier Register Settings

Pixel Clock Frequency	<54 MHz	54~111 MHz	112~223 MHz	224~300 MHz	301~600 MHz
SOR_NV_PDISP_SOR_PLL1_x					
TMDS_TERMADJ[1]	N/A	N/A	N/A	N/A	N/A
TMDS_TERM	0x1	0x1	0x1	0x1	0x1
SOR_NV_PDISP_SOR_PLL3_x					
BG_VREF_LEVEL	0x8	0x8	0x8	0x8	0x8
SOR_NV_PDISP_SOR_LANE_DRIVE_CURRENT0_x					
LANE3_DP_LANE3	0x33	0x33	0x37	0x33	0x33
LANE2_DP_LANE0	0x3A	0x3A	0x3A	0x3D	0x3D
LANE1_DP_LANE1	0x3A	0x3A	0x3A	0x3D	0x3D
LANE0_DP_LANE2	0x3A	0x3A	0x3A	0x3D	0x3D
SOR_NV_PDISP_SOR_LANE_PREEMPHASIS0_x					
LANE3_DP_LANE3	0x00	0x00	0x00	0x00	0x00
LANE2_DP_LANE0	0x00	0x00	0x00	0x00	0x00
LANE1_DP_LANE1	0x00	0x00	0x00	0x00	0x00
LANE0_DP_LANE2	0x00	0x00	0x00	0x00	0x00
SOR_NV_PDISP_SOR_DP_PADCTL0_x					
TX_PU_VALUE	0x00	0x00	0x00	0x40	0x60
TX_PU	0x1	0x1	0x1	0x1	0x1

Note:

[1]Settings for TMDS_TERMADJ will vary depending on termination calibration results. The settings for the register will get updated automatically.

Note: The "_x" in the register names represents 0~1 of SOR. See "Registers" section for details.

HDMI Tuning Final Check

This section describes the final check for HDMI tuning.

Sanity Check

After tuning is completed, the settings should be sanity-checked to make sure they do not violate any other parts of the HDMI specifications and there is enough margin.

The DUT should go through the full set of electrical tests outlined in the HDMI Compliance Test Specifications (CTS) document to ensure that the DUT can pass HDMI certification.

If there are any failures, the settings must be tuned again until there is a passing result.

Note: Higher power consumption is expected if the new settings are stronger than the default settings. Stronger settings are required due to, but not limited to, longer traces, EMI chokes on the signal paths, or signal integrity issues.

Updating the Software

After the tuned settings have been verified, they need to be updated into the OS or the driver. Contact the appropriate software team, or your NVIDIA representative to update new tuned settings.

- The 480p settings apply to pixel clock resolutions ⩽ 54 MHz
- The 720p settings apply to pixel clock resolutions between > 54 MHz to ⩽ 111 MHz
- The 1080p settings apply to pixel clock resolutions between > 111 MHz to ⩽ 223 MHz
- The 2160p/30 settings apply to pixel clock resolutions between > 223 MHz to ⩽ 300 MHz
- The 2160p/60 settings apply to pixel clock resolutions between > 301 MHz to ⩽ 600 MHz

Note: Ranges can be adjusted according to design and use-cases. More ranges can also be defined as long as proper tuning and software implementation is performed.

Final Steps

After the settings have been updated in the driver, you must verify that the new tuned settings are really applied to each of the target resolutions.

A visual check-out is recommended as well. Connect the DUT to an HDMI panel and visually check that there is no corruption at any of the supported HDMI resolutions.

Jetson Xavier NX Series DisplayPort and Embedded DisplayPort Tuning Guide

This chapter describes the registers and procedure to tune the VESA DisplayPort (DP) and Embedded DisplayPort (eDP) for the NVIDIA Jetson Xavier NX series processor.

DisplayPort is a video interface using AC-coupled signals to transmit serialized data to a single display sink, such as monitors. The eDP interface is used for internal connections to drive smaller sinks such as panels or embedded displays.

In addition to the standard DP data rates (RBR/HBR/HBR2/HBR3) and voltage levels (400 mV, 600 mV, 800 mV, and 1200 mV), eDP also supports four other intermediate bit rates and lower, optional, voltage swings below 400 mV.

Since there is no compliance specification for the additional bit rates and lower voltage levels supported in eDP, this guide only covers the standard rates and voltage levels using the DP 1.4a Compliance Test Specification (CTS). The concepts can still be applied for the other bit rates and voltage levels.

Tuning is needed to make sure the DP interface can meet the specification for each of the different combinations of voltage and frequency outputs, while minimizing power consumption.

Design choices such as, but not limited to, long routing and layer transitions, can heavily affect the signal integrity, and require some adjustments to overcome the loss.

Abbreviations and Definitions

Table 19 lists the abbreviations that may be used throughout this application note and their definitions.

Table 19. Abbreviations and Definitions

Abbreviation	Definition
CTS	Compliance Test Specification
DP	DisplayPort
eDP	Embedded DisplayPort
DUT	Device Under Test
RBR	Reduced Bit Rate (1.62 Gbps)
HBR	High Bit Rate (2.7 Gbps)
HBR2	High Bit Rate 2 (5.4 Gbps)
HBR3	High Bit Rate 3 (8.1 Gbps)
Link Training	Establishing a link between source and sink before normal operation
SSC	Spread Spectrum Clock, will reduce EMI
Sink	Any type of receiver, such as a display or panel
SOR	Serial Output Resource. Module naming referring to the DP/eDP block
Source	Any type of transmitter, such as NVIDIA® Xavier™

DP and eDP Tuning Required Equipment

The following hardware and software are required:

- Hardware
  - DP Plug Test Fixture, corresponding to the plug type
  - Oscilloscope and Probes
- Software
  - DisplayPort Compliance Test Software
  - Debug tools to access registers
  - AUX channel automation (optional)

Test Fixtures

Test fixtures connect the probes to the outputs of the Serial Output Resource (SOR) of the DUT. NVIDIA recommends that a native fixture be selected and that no adapters be used between the DP connector and the DP test fixture, since adapters will heavily affect the signal integrity.

List of test fixture vendors:

- WilderTech
- VPrime
- Keysight

Oscilloscope and Probes

The oscilloscope and probes are used to measure the signal electrically. The equipment must be capable of accurately measuring the maximum bitrate supported by the DUT, up to 8.1 Gbps (HBR3).

The following are examples of testing solutions:

- Tektronix:

  https://www.tek.com/displayport-0

  https://www.tek.com/datasheet/displayport-14-and-type-c-compliance-debug-solution

  https://www.tek.com/oscilloscope/dpo70000-mso70000

  https://www.tek.com/oscilloscope/dpo70000sx

  https://www.tek.com/datasheet/displayport%28tm%29-14-sink-calibration-and-test-software-%28dp-sink-bsx-dp-sink%29

- Keysight:

  https://www.keysight.com/en/pd-2858984-pn-U7232E/displayport-14-compliance-and-validation-test-software

  https://literature.cdn.keysight.com/litweb/pdf/5991-1784EN.pdf?id=2295383

DP and eDP Software

Only compliance test software should be used to guarantee an accurate result for compliance. Debug tools to access Xavier register space are necessary to fine-tune the settings. AUX channel automation can help make testing hands-free.

Contact the test equipment dealer directly for more information.

DP and eDP Method of Tuning

There are several settings in the DP PHY to tune the output to meet the specs in the DP (CTS). The following sections describe the major controls to tune for characterization. Tuning consists of adjusting the settings to meet each voltage swing, pre emphasis, and maximum differential voltage test for each driver configuration.

Drive Strength

Drive strength controls the amount of drive current of each of the four lanes and can be configured individually, affecting the overall voltage swing. This control has higher priority over pre-emphasis, meaning if the settings are maxed out, there will be no current drivers for the other controls.

To save power, this setting can be reduced until it can pass with sufficient margin, roughly 20-30%.

Pre-Emphasis

Pre-emphasis controls affects the voltage swing of the transition bit. There needs to be distinct levels of pre-emphasis to meet specifications. Increasing pre-emphasis also affects non-transition bits, effectively lowering the voltage swing of the non-transition bits.

To save power, this setting can be reduced until it can pass with sufficient margin; roughly 20-30%.

Post Cursor2

Post Cursor2 is deprecated and should always be set to 0.

Headroom Relief (TX_PU_VALUE)

Due to the low input voltage for the interface, an additional source is needed for high voltage swing operation. TX_PU should be enabled for all drive levels. Note that TX_PU_VALUE is generally low for 400 mV and 600 mV swing levels and higher for 800 mV and 1200 mV levels.

DP and eDP Tuning Procedures

Before proceeding with the tuning procedure, the scope and probes must be calibrated. Refer to your scope and probe user manuals on how to calibrate.

DUT

The node "/sys/kernel/debug/tegra_dpX/test_settings" can be used to dynamically change the settings shown in Table 20.

The format of the command is as follow:

echo [arg1]=[val1],[arg2]=[val2],.....,[argN]=[valN] > /d/tegra_dp[X]/test_settings

where, X=DP head number

Example:

echo sw=2,pre=0,lanes=4,patt=d102,br=hbr2,panel=0 > /d/tegra_dp0/test_settings

Table 20. DP Command Options

Settings	Arguments [arg]	Values [val]
Drive Current Level	sw	0, 1, 2, 3
Pre-emphasis Level	pre	0, 1, 2, 3
Number of Lanes	lanes	1, 2, 4

Settings	Arguments [arg]	Values [val]
Test Pattern	patt	none, t1, t2, t3, d102, sblerrrate, prbs7, pltpat, hbr2compliance, cp2520_pat1, cp2520_pat3, t4
Bit Rate	br	rbr, hbr, hbr2, hbr3
TX_PU Disabled (internal PHY setting, should always be set to 0)	Tx_pu_disable	0, 1
Panel Mode	panel	0, 1

Configure the DUT using the command described to output the appropriate output configuration, such as bit rate, swing levels, and test patterns. Then connect the test fixture to the DUT and the test fixture to probes to the scope. Any untested lanes should be terminated with 50 Ω to GND.

Oscilloscope

After calibration, initialize the compliance test software and configure it for all the modes supported by the DUT.

Objectives

Settings for drive strength, pre-emphasis, and TX_PU, must be found for the following output configurations.

DisplayPort

The tuned settings must work across all bit rates supported by the DUT: RBR, HBR, and HBR2 (optional), and HBR3 (optional).

Table 21. DisplayPort Configurations

Drive Level	Pre-Emphasis Level	Post Cursor2
400 mV	0.0 dB	0
400 mV	3.5 dB	0
400 mV	6.0 dB	0
400 mV	9.5 dB	0

Drive Level	Pre-Emphasis Level	Post Cursor2
600 mV	0.0 dB	0
600 mV	3.5 dB	0
600 mV	6.0dB	0

Drive Level	Pre-Emphasis Level	Post Cursor2
800 mV	0.0 dB	0
800 mV	3.5 dB	0

Drive Level	Pre-Emphasis Level	Post Cursor2
1200 mV	0.0 dB	0

Embedded DisplayPort

The settings in Table 22 are required for fast link training. Since there is no spec for the other bit rates or voltage levels, this guide will not cover them.

Table 22. Embedded DisplayPort Configurations

Bit Rate	Drive Level	Pre-Emphasis Level	Post Cursor2 Level
RBR	400 mV	0.0 dB	0
HBR	400 mV	0.0 dB	0
HBR2	400 mV	0.0 dB	0

Registers

The Serial Output Resource (SOR) module can be configured to output HDMI or DisplayPort (DP). Jetson Xavier NX has two instances of the SOR module and two sets of DP pins. SOR0 controls the DP0 pins, and SOR1 controls DP1 pins.

To select which SOR to access, simply replace the trailing number with the SOR number. For example, SOR_NV_PDISP_SOR_DP_PADCTL0_0 for the first SOR and SOR_NV_PDISP_SOR_DP_PADCTL0_1 for the second SOR.

Table 23. Xavier SOR Registers

Register Name	Bit Fields	Description	Notes
SOR0: SOR_NV_PDISP_SOR_LANE_DRIVE_CURRENT0_0 (Address 0x15b00138) SOR1: SOR_NV_PDISP_SOR_LANE_DRIVE_CURRENT0_1 (Address 0x15b40138)			
LANE0_DP_LANE2	07:00	Drive Strength Controls for Lane 0	Only lower 7 bits used. Higher values equal to stronger settings.
LANE1_DP_LANE1	15:08	Drive Strength Controls for Lane 1	
LANE2_DP_LANE0	23:16	Drive Strength Controls for Lane 2	
LANE3_DP_LANE3	31:24	Drive Strength Controls for Lane 3	
SOR0: SOR_NV_PDISP_SOR_LANE_PREEMPHASIS0_0 (Address 0x15b00148) SOR1: SOR_NV_PDISP_SOR_LANE_PREEMPHASIS0_1 (Address 0x15b40148)			
LANE0_DP_LANE2	07:00	Pre-Emphasis Controls for Lane 0	Only lower 6 bits used. Higher values equal to stronger settings.
LANE1_DP_LANE1	15:08	Pre-Emphasis Controls for Lane 1	
LANE2_DP_LANE0	23:16	Pre-Emphasis Controls for Lane 2	
LANE3_DP_LANE3	31:24	Pre-Emphasis Controls for Lane 3	
SOR0: SOR_NV_PDISP_SOR_DP_PADCTL0_0 (Address 0x15b005b8) SOR1: SOR_NV_PDISP_SOR_DP_PADCTL0_1 (Address 0x15b405b8)			
RESERVED	07:00	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
TX_PU_VALUE	15:08	Headroom Relief Value	Only bits 14:12 are used.
RESERVED	21:16	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
TX_PU	22:22	Headroom Relief Enable 0x0 = Disable 0x1 = Enable	Enables TX_PU_VALUE.
RESERVED	31:23	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.

DisplayPort Reference Settings

The following table shows the settings achieved for DisplayPort with an NVIDIA internal reference board. Tuning results on other platforms may differ.

Table 24. DisplayPort Settings on NVIDIA Reference Board

Levels			Register Settings				
Drive	Pre-Emphasis	Post Cursor2	DRIVE_CURRENT	PREEMPHASIS	POSTCURSOR	TX_PU_VALUE	TX_PU
400 mV	0.0 dB	0	0x15	0x00	0x0	0x20	0x1
400 mV	3.5 dB	0	0x1c	0x0b	0x0	0x30	0x1
400 mV	6.0 dB	0	0x23	0x18	0x0	0x40	0x1
400 mV	9.5 dB	0	0x2d	0x2d	0x0	0x60	0x1
600 mV	0.0 dB	0	0x20	0x00	0x0	0x30	0x1
600 mV	3.5 dB	0	0x27	0x0f	0x0	0x40	0x1
600 mV	6.0 dB	0	0x2f	0x20	0x0	0x60	0x1
800 mV	0.0 dB	0	0x2c	0x01	0x0	0x40	0x1
800 mV	3.5 dB	0	0x36	0x18	0x0	0x60	0x1
1200 mV	0.0 dB	0	0x3C	0x00	0x0	0x60	0x1

DP and eDP Tuning Final Steps

This section describes the final check for DisplayPort and Embedded DisplayPort tuning.

Sanity Check

After tuning is completed, the settings should be sanity-checked to make sure they do not violate any other parts of the DisplayPort specifications and that there is a comfortable amount of margin based on the user's analysis.

The DUT should go through the battery of electrical tests outlined in the DP CTS document to ensure that the DUT will pass DP certification.

If there are any failures, the settings must be tuned again until there is a passing result.

Updating the Software

After the tuned settings have been verified, they need to be updated in the OS or the driver.

Final Check

After the settings have been updated in the driver, verify that the tuned settings are applied for each of the requested modes.

A visual check-out is recommended as well. Connect the DUT to a DP or eDP panel and visually verify that there is no corruption at any of the supported bitrates.

Jetson Xavier NX Ethernet Compliance Test Guide

This chapter serves as the high-level guide to compliance testing of the 1000Base-T interface in NVIDIA Jetson Xavier NX. The Jetson Xavier NX has been tested for specification compliance, therefore, no tuning will be required if customer designs follow the routing guidelines published in our design guides.

Ethernet Compliance Testing

The *IEEE Standard for Ethernet* defined by IEEE802.3ab provides the compliance criteria and test descriptions for 1000Base-T. Customers should refer to the document for a high-level overview of the tests that are performed to check the compliance criteria. Depending on the brand of equipment being used for the test, customers can then refer to the manufacturer's documentation for step-by-step procedure to perform the test.

Tools

Mdio-tool is a generic tool which can be used to access the PHY registers from the Linux command line. It can be downloaded and compiled from the following location:

https://github.com/PieVo/mdio-tool

Note: The original makefile is for cross-compilation, therefore it can be built directly on the device through the command "gcc -o mdio-tool mdio-tool.c"

Placing Jetson Xavier NX in Compliance Mode

The Jetson Xavier NX integrates a Realtek RTL8211FDI Gigabit Ethernet PHY. Therefore, to perform compliance testing on the Jetson Xavier NX, customers will need to contact Realtek to obtain documentation on how to access the internal registers.

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