Jetson AGX Xavier Series Product

Design Guide

DG-09840-001_v2.4 | January 2021

Document History

DG-09840-001_v2.4

Version	Date	Description of Change
	August 29, 2018	Initial Release
	November 15, 2018	Pin Description Table • Updated pin types for UPHY[9:8] in full pin descriptions table General • Updated module name to Jetson AGX Xavier Overview • Updated Jetson AGX Xavier Interfaces table PCIe and I2S functions • Updated # of UARTs to 5 Main Connector Details • Added text and figure for standoff requirements • Added 2.5mm height connector option for carrier board Power • Updated Power and System Pin Desc. table (and full table] • Updated Usage columns • Updated pin type column • Corrected title of Table 8 • Added SYS_VIN_HV Input and simplified DC Jack figure • Added note for MCU based power button supervisor designs • Added non-MCU based power-on circuit description • Updated Power Discharge to match latest reference design USB • Updated Simple USB Type A Connection Example figure • Added note under USB type C example that designs related to microcode. • Removed level shifter on USB Micro ID signal and added note PCIe • Updated PCIe figure and table Root Port and added PEX_L5 control. • Updated PCIe RST pull-up value figure/table and checklist.

Version	Date	Description of Change
		• Added PCIe Endpoint Connection figure and table • Updated PCIe Intra-pair skew length • Updated range and value for PCIe AC cap for GEN3. Video Input • Updated Misc. Pin Descriptions table for UART4_TX/CTS Audio • Corrected I2S1/DAP1 signals descriptions UART • Added UART7 option on module SPI2 pins Debug • Added simple debug UART connection section Strapping • Added notes for to pull-up resistors on RAM_CODE straps. Design Checklist • Added pull-up on OVERTEMP_N • Updated terminations for GPIO30 • Added power jack option to Carrier Board Supplies section • Removed AC caps for UFS • Updated pin types for UPHY[9:8]
	February 20, 2019	Power • SYS_VIN_HV Input: Updated note on Type C PD support • Updated Simplified Button Power-on Circuitry figure • Power Button Supervisor: Updated note related firmware USB • Updated note related to Type C firmware • Updated USB Type C figure and notes for test points. • Updated USB Type A Connection figure • Updated USB Micro AB Connection figure PCIe • Updated PEX_WAKE_N usage in Pin Description tables • Corrected connection figures for for NVHS0_SLVS_REFCLK UFS • Updated figure module pin #s/names for UFS CLK/RST. MIPI CSI

Version	Date	Description of Change
		• Updated with relaxed skews based on frequency (0.4*UI) I2C • Updated figure module pin #s for I2C3 Boundary Scan • Updated Boundary Scan figure module pin #s Pin Descriptions • Corrected I2S1 pin #s, description and direction.
2.0	May 12, 2020	Main 699-pin Connector Details • Added Module Installation and Removal Section Video Input • Added SLVS XCE and SCLR signals to Pin Desc. • Added pin tolerance were applicable • Updated control signal direction to match SLVS usage • Update SLVS connection figure: • Corrected XCE and XCLR connections and changed to generic name for SLVS imager/connector in figure • Added SLVS connections tables I2C and Design Checklist (I2C section) • Added note for series resistors on I2C for M.2 sockets
2.1	July 27, 2020	• Update Table 2-1 to C5 only supports EP • Added Chapter 4 on reference design considerations • Added DV/Dt section (Section 5.5.1) including optional disable or tuning • Added optional additional diode to DV/dt circuit to allow more drop before triggering system shutdown (asserting VDDIN_PWR_BAD_N) in Figure 5-12 • Added descriptions per lane for data lane pin descriptions table (Table 7-2) • Added more details to the "Usage/Description" column in Table 7-3 • Updated to reflect RP only and added details for EP usage to the PCIe clock and control pin descriptions table (Table 7-4) • Updated Section 7.2 "PCI Express" for C5 only as EP • Updated Figure 7-4 for C5 only as EP • Removed C0 and C4 as EP in Figure 7-5 • Added UPHY_REFCLK1/2_N/P pins but indicated it is unused as EP not supported on C0 and C4 in Table 7-14 • Added NVHS0_SLVS_REFCLK_N/P pin to Table 7-14 • Removed C0 and C4 from Table 7-15 as these are no longer supported as Eps

Version	Date	Description of Change
		• Added NVHS0_SLVS_REFCLK_N/P and PEX_WAKE_N pins to Table 7-15 • Added load switch on 3.3V to eDP/DP connector in Figure 9-1 • Updated Figure 9-3 to show load switch providing 5V to the connector and added related note • Removed mention of debug and added note in Table 13-10 • Removed mention of debug connector and changed UART2 connection on CB to UART USB bridge in Figure 13-7 • Added Section 15.1 "USB Recovery Mode" • Removed UART2 as debug UART and removed related note in Figure 15-1 • Replaced example showing UART2 with one showing UART3 instead and removed note in Figure 15-2 • Removed mention of UART2 in Section 15.2.2 and the table listed in the section • Added bring-up checklist to the attachments and listed in Chapter 18
2.2	November 18, 2020	• Added notes to Figure 5-3, Figure 5-4, and Figure 7-3 • Added note to clarify PCIe clock output and RFCLK input signaling type to Figure 7-4 • Added insertion loss S-parameter plot figure (Figure 7-6) • Updated Table 10-5 based on new guidelines from IOSI based on improved model
2.3	January 28, 2021	• Updated to include Jetson AGX Xavier Industrial (JAXi) • Updated pin description attachment
2.4	June 8, 2021	• Attachment: Updated pin description Excel file • Module spacing: Updated Section 3.3: Module to Carrier Board Standoff Height Recommendations Updated mating connector spacing tolerance and column titles/spacing numbers in Table 3-1 and Table 3-2 • Updated STANDBY_ACK_N description in Table 5-1: Power, System, and Thermal Pin Descriptions. • PCIE: Table 7-4: PCIe Clock and Control Pin Descriptions; updated CLKREQ, RST and WAKE pin descriptions. • USB: Updated Figure 7-1: Simple USB Type A Connection Example. • I2S: Updated Table 12-1: Jetson AGX Xavier Audio Pin Description to indicate I2S6 (DAP6 on SoC) is not supported for JAXi.

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Chapter 1. Introduction

This design guide contains recommendations and guidelines for engineers to follow to create a product that is optimized to achieve the best performance from the interfaces supported by the NVIDIA® Jetson AGX Xavier™ series System-on-Module (SOM).

This design guide provides detailed information on the capabilities of the hardware module, which may differ from supported configurations by provided software. Refer to software release documentation for information on supported capabilities.

Note: References to Jetson AGX Xavier applies to any of the Jetson AGX Xavier series of modules including Jetson AGX Xavier Industrial (JAXi) except where explicitly noted.

1.1 References

Refer to the following documents or models listed for more information. Always use the latest revision of all documents.

- *Jetson AGX Xavier Series Module Data Sheet*
- *Xavier Series Processors Technical Reference Manual*
- *Jetson AGX Xavier Series Developer Kit Carrier Board Specification*
- *Jetson AGX Xavier Series Module Pinmux*
- *Jetson AGX Xavier Series Thermal Design Guide*
- *Jetson AGX Xavier Series Developer Kit Carrier Board Design Files*
- *Jetson AGX Xavier Series Developer Kit Carrier Board BOM*
- *Jetson AGX Xavier Series Supported Component List*

1.2 Abbreviations and Definitions

Table 1-1 lists abbreviations that may be used throughout this document and their definitions.

Table 1-1. Abbreviations and Definitions

Abbreviation	Definition
CEC	Consumer Electronic Control
CAN	Controller Area Network
DP	VESA® DisplayPort® (output)
eDP	Embedded DisplayPort
eMMC	Embedded MMC
HDMI™	High Definition Multimedia Interface
I2C	Inter IC
I2S	Inter IC Sound Interface
LDO	Low Dropout (voltage regulator)
LPDDR4x	Low Power Double Data Rate DRAM, Fourth-generation
PCIe (PEX)	Peripheral Component Interconnect Express interface
PCM	Pulse Code Modulation
PHY	Physical Layer
PMIC	Power Management IC
RTC	Real Time Clock
SDIO	Secure Digital I/O Interface
SLVS	Scalable Low Voltage Signaling
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver-Transmitter
UFS	Universal Flash Storage
USB	Universal Serial Bus

Chapter 2. Jetson AGX Xavier

Jetson AGX Xavier resides at the center of the embedded system solution and includes:

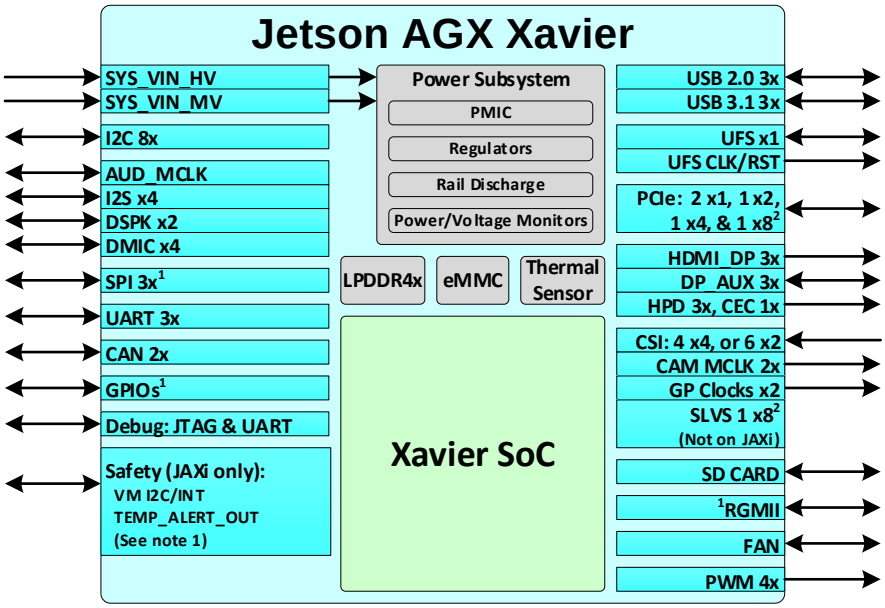
- Power (PMIC/Regulators, etc.)
- DRAM (LPDDR4x)
- eMMC
- Power and Voltage Monitors
- Thermal Sensor

Table 2-1. Jetson AGX Xavier Specifications

Category	Function		Category	Function
USB	USB 2.0 (x4) USB 3.1 (Up to x3)		PCIe	x5 (x1 Root Port or Endpoint and x4 Root Port only
Camera	CSI (6x2 or 4x4) D-PHY and C-PHY		Display	HDMI / DP (up to x3) see note HPD x3, CEC x1, DP_AUX/DDC x3
LAN	Gigabit Ethernet RGMII I/F		SPI	x3
SD Card	SD card or SDIO		Fan	PWM and TACH
Audio	I2S (x4), control and clock Digital Mic and Speaker IFs		Debug	JTAG and UART
CAN	x2		System	Power control, Reset, Alerts
I2C	x8		Power	Main Inputs (HV and MV)
UART	x5			

Note: HDMI and DP share the same pins. See Chapter 9 for display details.

Figure 2-1. System Block Diagram



Notes:

1. SPI2, RGMII, GPIO31, and GPIO33 are available to use with a Safety MCU.
2. PCIe x8 interface and SLVS share the same pins.

Table 2-2. Connector Pinout Matrix Part 1: Columns A-F

	A	B	C	D	E	F
01			SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV
02			SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV
03	PRSNT0	SYS_VIN_HV	GND	SYS_VIN_HV	GND	SYS_VIN_HV
04	SDCARD_D2	GND	RGMII_RD0	GND	I2S2_FS	GND
05	SDCARD_CMD	RGMII_TXC	RGMII_RXC	RGMII_RX_CTL	RGMII_RD3	I2S2_DOUT
06	UFS0_REF_CLK	SDCARD_CLK	UFS0_RST_N	SDCARD_D3	RGMII_SMA_MDC	I2S2_DIN
07	GPIO29	GND	I2S1_SDOUT	GND	RGMII_SMA_MDIO	GND
08	PEX_WAKE_N	GPIO11	PEX_L5_CLKREQ_N	I2S1_FS	SDCARD_D0	SDCARD_D1
09	GND	PEX_L1_RST_N	GND	PEX_L1_CLKREQ_N	GND	GPIO16
10	USB2_P	RSVD	USB1_N	PEX_L0_RST_N	GPIO12	GPIO15
11	USB2_N	GND	USB1_P	GND	PEX_L0_CLKREQ_N	GND
12	GND	UPHY_RX10_P	GND	UPHY_RX11_P	GND	USB0_P
13	GND	UPHY_RX10_N	GND	UPHY_RX11_N	GND	USB0_N
14	UPHY_RX8_N	GND	UPHY_RX9_N	GND	PEX_CLK0_N	GND
15	UPHY_RX8_P	GND	UPHY_RX9_P	GND	PEX_CLK0_P	GND
16	GND	UPHY_RX6_P	GND	UPHY_RX7_P	GND	PEX_CLK1_P
17	GND	UPHY_RX6_N	GND	UPHY_RX7_N	GND	PEX_CLK1_N
18	UPHY_RX4_P	GND	UPHY_RX5_N	GND	RSVD	GND
19	UPHY_RX4_N	GND	UPHY_RX5_P	GND	RSVD	GND
20	GND	UPHY_RX2_N	GND	UPHY_RX3_P	GND	PEX_CLK3_P
21	GND	UPHY_RX2_P	GND	UPHY_RX3_N	GND	PEX_CLK3_N
22	UPHY_RX0_P	GND	UPHY_RX1_N	GND	PEX_CLK4_N	GND
23	UPHY_RX0_N	GND	UPHY_RX1_P	GND	PEX_CLK4_P	GND
24	GND	NVHS0_SLVS_RX1_N	GND	NVHS0_SLVS_RX0_P	GND	PEX_CLK5_P
25	GND	NVHS0_SLVS_RX1_P	GND	NVHS0_SLVS_RX0_N	GND	PEX_CLK5_N
26	NVHS0_SLVS_RX3_P	GND	NVHS0_SLVS_RX2_N	GND	UPHY_REFCLK1_N	GND
27	NVHS0_SLVS_RX3_N	GND	NVHS0_SLVS_RX2_P	GND	UPHY_REFCLK1_P	GND
28	GND	NVHS0_SLVS_RX5_N	GND	NVHS0_SLVS_RX4_P	GND	RSVD
29	GND	NVHS0_SLVS_RX5_P	GND	NVHS0_SLVS_RX4_N	GND	RSVD
30	NVHS0_SLVS_RX7_P	GND	NVHS0_SLVS_RX6_N	GND	NVHS0_SLVS_REFCLK0_P	GND
31	NVHS0_SLVS_RX7_N	GND	NVHS0_SLVS_RX6_P	GND	NVHS0_SLVS_REFCLK0_N	GND
32	GND	RSVD	GND	RSVD	GND	RSVD
33	GND	RSVD	GND	RSVD	GND	RSVD
34	RSVD	GND	RSVD	GND	RSVD	GND
35	RSVD	GND	RSVD	GND	RSVD	GND
36	GND	RSVD	GND	RSVD	GND	RSVD
37	GND	RSVD	GND	RSVD	GND	RSVD
38	RSVD	GND	RSVD	GND	CSI0_D1_N	GND
39	RSVD	GND	RSVD	GND	CSI0_D1_P	GND
40	GND	RSVD	GND	RSVD	GND	RSVD
41	CSI2_D0_P	GND	CSI2_D1_N	GND	CSI0_D0_N	GND
42	CSI2_D0_N	CSI2_CLK_N	CSI2_D1_P	CSI5_D0_P	CSI0_D0_P	CSI0_CLK_N
43	GND	CSI2_CLK_P	GND	CSI5_D0_N	GND	CSI0_CLK_P
44	CSI7_D0_P	GND	CSI5_CLK_P	GND	CSI3_D0_N	GND

	A	B	C	D	E	F
45	CSI7_D0_N	CSI7_CLK_P	CSI5_CLK_N	CSI5_D1_N	CSI3_D0_P	CSI3_CLK_N
46	GND	CSI7_CLK_N	GND	CSI5_D1_P	GND	CSI3_CLK_P
47	HDMI_DP1_TX0_P	GND	CSI7_D1_P	GND	CSI4_D1_P	GND
48	HDMI_DP1_TX0_N	HDMI_DP1_TX1_N	CSI7_D1_N	HDMI_DP1_TX2_N	CSI4_D1_N	CSI4_CLK_P
49	GND	HDMI_DP1_TX1_P	GND	HDMI_DP1_TX2_P	GND	CSI4_CLK_N
50	HDMI_DP2_TX2_N	GND	HDMI_DP2_TX3_N	GND	HDMI_DP1_TX3_P	GND
51	HDMI_DP2_TX2_P	HDMI_DP2_TX1_P	HDMI_DP2_TX3_P	HDMI_DP2_TX0_P	HDMI_DP1_TX3_N	DP0_AUX_CH_N
52	GND	HDMI_DP2_TX1_N	GND	HDMI_DP2_TX0_N	GND	DP0_AUX_CH_P
53	I2C5_CLK	GND	I2C5_DAT	GND	I2C3_DAT	I2C3_CLK
54	GPIO17	WDT_RESET_OUT_N	GPIO33	GPIO03	FAN_TACH	GPIO22
55	GPIO34	GPIO30	GPIO18	SPI1_MOSI	SPI1_CS0_N	SPI3_CLK
56	SPI1_MISO	SPI1_CS1_N	UART2_RX	SPI3_MISO	SPI3_CS1_N	GPIO36
57	UART2_CTS	GND	SPI3_CS0_N	GND	GND	GND
58	GPIO20	GPIO21	UART2_TX	JTAG_TDO	JTAG_TMS	CAN0_DIN
59	GPIO05	GPIO04	I2S3_SCLK	CAN0_DOUT	GPIO06	GPIO07
60	JTAG_TCK	JTAG_TDI	I2S3_FS	SPI2_CS0_N	I2C4_DAT	SPI2_MOSI
61	SYSTEM_OC_N	CAN1_DIN	GPIO09	I2C4_CLK	SPI2_CLK	VCOMP_ALERT_N
62	GPIO10	GPIO08	GND	SPI2_MISO	GND	GND
63	GND	SYS_VIN_HV	SYS_VIN_HV	GND	SYS_VIN_HV	SYS_VIN_HV
64			SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV
65			SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV

Legend					
Ground	Power	Reserved – Must be left unconnected unless otherwise directed.	No pins at that location	JAXi only	Safety MCU usage on JAXi

Table 2-3. Connector Pinout Matrix Part 2: Columns G-L

	G	H	J	K	L
01	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV		
02	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV		
03	GND	SYS_VIN_HV	GND	SYS_VIN_HV	GND
04	I2S2_CLK	GND	GPIO01	GND	UART4_RTS
05	RGMII_TD1	ENET_RST_N	ENET_INT	I2C1_CLK	UART4_TX
06	RGMII_TD3	RGMII_RD2	RGMII_TD0	RGMII_RD1	GPIO02
07	GPIO13	GND	RGMII_TD2	RGMII_TX_CTL	GND
08	PEX_L4_CLKREQ_N	I2S1_SDIN	GND	GND	I2C1_DAT
09	GND	MCLK01	PEX_L4_RST_N	PEX_L3_RST_N	GPIO28
10	USB3_N	PEX_L5_RST_N	PEX_L3_CLKREQ_N	RSVD	FORCE_RECOVERY_N
11	USB3_P	GND	RSVD	GND	STANDBY_REQ_N
12	GND	UPHY_TX11_P	GND	UPHY_TX10_N	GND
13	GND	UPHY_TX11_N	GND	UPHY_TX10_P	GND
14	UPHY_TX9_N	GND	UPHY_TX8_P	GND	I2S1_CLK
15	UPHY_TX9_P	GND	UPHY_TX8_N	GND	GPIO14
16	GND	UPHY_TX7_P	GND	UPHY_TX6_N	GND
17	GND	UPHY_TX7_N	GND	UPHY_TX6_P	GND
18	UPHY_TX5_N	GND	UPHY_TX4_P	GND	RSVD
19	UPHY_TX5_P	GND	UPHY_TX4_N	GND	RSVD
20	GND	UPHY_TX3_P	GND	UPHY_TX2_N	GND
21	GND	UPHY_TX3_N	GND	UPHY_TX2_P	GND

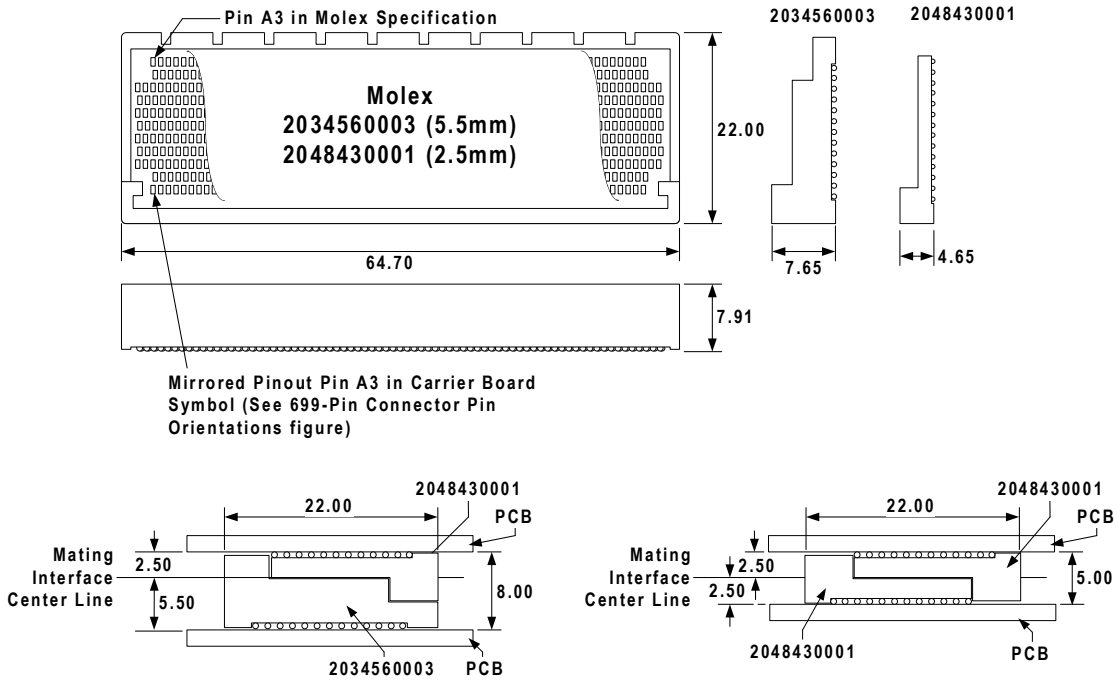
	G	H	J	K	L
22	UPHY_TX1_N	GND	UPHY_TX0_P	GND	SYS_VIN_MV
23	UPHY_TX1_P	GND	UPHY_TX0_N	GND	SYS_VIN_MV
24	GND	NVHS0_TX0_P	GND	NVHS0_TX1_N	GND
25	GND	NVHS0_TX0_N	GND	NVHS0_TX1_P	GND
26	NVHS0_TX2_N	GND	NVHS0_TX3_P	GND	SYS_VIN_MV
27	NVHS0_TX2_P	GND	NVHS0_TX3_N	GND	SYS_VIN_MV
28	GND	NVHS0_TX4_P	GND	NVHS0_TX5_N	GND
29	GND	NVHS0_TX4_N	GND	NVHS0_TX5_P	GND
30	NVHS0_TX6_N	GND	NVHS0_TX7_P	GND	SYS_VIN_MV
31	NVHS0_TX6_P	GND	NVHS0_TX7_N	GND	SYS_VIN_MV
32	GND	RSVD	GND	RSVD	GND
33	GND	RSVD	GND	RSVD	GND
34	RSVD	GND	RSVD	GND	SYS_VIN_MV
35	RSVD	GND	RSVD	GND	SYS_VIN_MV
36	GND	RSVD	GND	RSVD	GND
37	GND	RSVD	GND	RSVD	GND
38	RSVD	GND	RSVD	GND	SYS_VIN_MV
39	RSVD	GND	RSVD	GND	SYS_VIN_MV
40	GND	MID1	GND	MID0	GND
41	CSI1_D0_P	GND	CSI1_D1_P	GND	RSVD
42	CSI1_D0_N	CSI1_CLK_N	CSI1_D1_N	GND	RSVD
43	GND	CSI1_CLK_P	GND	CSI6_D0_N	GND
44	CSI3_D1_P	GND	CSI6_CLK_P	CSI6_D0_P	VM_I2C_SCK
45	CSI3_D1_N	CSI6_D1_N	CSI6_CLK_N	GND	VM_I2C_DAT
46	GND	CSI6_D1_P	GND	HDMI_DP0_TX3_P	GND
47	CSI4_D0_N	GND	HDMI_DP0_TX2_P	HDMI_DP0_TX3_N	VM_INT_N
48	CSI4_D0_P	HDMI_DP0_TX0_N	HDMI_DP0_TX2_N	GND	UART4_RX (RSVD)
49	GND	HDMI_DP0_TX0_P	GND	GPIO25	UART4_CTS
50	HDMI_DP0_TX1_N	GND	HDMI_CEC	DP2_HPD	GPIO35
51	HDMI_DP0_TX1_P	GPIO26	GPIO24	DP1_HPD	UART1_RTS
52	GND	GPIO27	DP1_AUX_CH_P	DP0_HPD	OVERTEMP_N
53	DP2_AUX_CH_P	MCLK03	DP1_AUX_CH_N	UART1_TX	VCC_RTC
54	DP2_AUX_CH_N	UART1_CTS	MCLK02	UART1_RX	MODULE_POWER_ON
55	GPIO23	MCLK04	GPIO32	GND	VDDIN_PWR_BAD_N
56	SPI3_MOSI	GND	GND	GPIO19	TEMP_ALERT_N
57	GND	UART5_CTS	SPI1_CLK	PWM01	MCLK05
58	UART2_RTS	UART5_RX	UART5_TX	UART5_RTS	PERIPHERAL_RESET_N
59	TEMP_ALERT_OUT (JAXi only)	NVJTAG_SEL	I2S3_DIN	I2S3_DOUT	RSVD
60	NVDBG_SEL	GPIO31	STANDBY_ACK_N	UART3_RX_DEBUG	SYS_RESET_N
61	JTAG_TRST_N	CAN1_DOUT	I2C2_CLK	I2C2_DAT	POWER_BTN_N
62	GND	UART3_TX_DEBUG	GND	FAN_PWM	CARRIER_POWER_ON
63	SYS_VIN_HV	GND	SYS_VIN_HV	GND	PRSNT1
64	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV		
65	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV		

Legend					
Ground	Power	Reserved – Must be left unconnected unless otherwise directed.	No pins at that location	JAXi only	Safety MCU usage on JAXi

Chapter 3. Main Connector Details

The main 699-pin connector on the Jetson AGX Xavier module is from the Molex Mirror Mezz family (Part # 2048430001). This mates with the Molex 2034560003 or another 2048430001 (shown in the following figure) on the carrier board. Refer to the Molex Mirror Mezz connector specification for details.

Figure 3-1. 699-pin Connector Dimensions

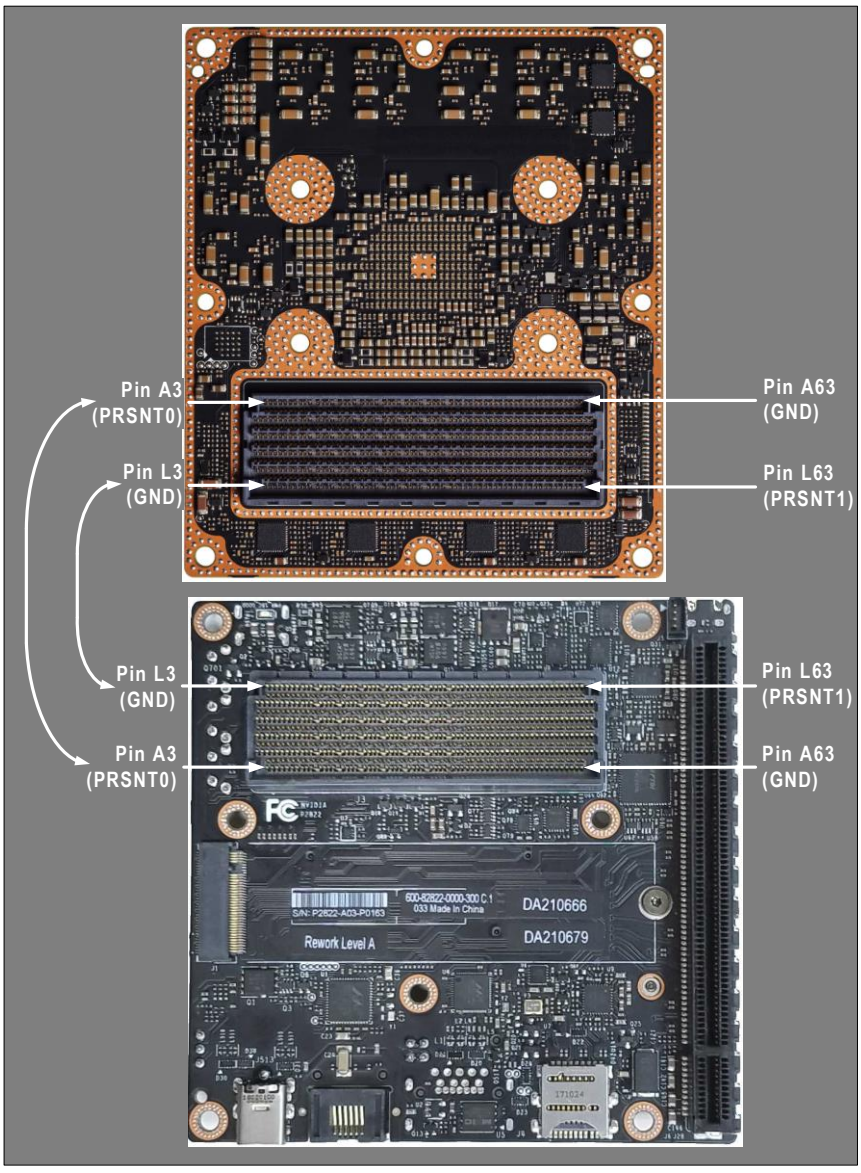


Note: Various documents related to the Molex Mirror Mezz connector can be found at: https://www.molex.com/molex/products/datasheet.jsp?part=active/2034560003_PCB_HEADERS.xmlandchannel=ProductsandLang=en-US. The Molex Application Guide for Mirror Mezz™ which includes details for connector mounting can be found at: https://www.molex.com/pdm_docs/as/2028280001-AS-000.pdf

3.1 Connector Pin Orientations

The symbol pinout for the 699-pin connector on the carrier board is mirrored such that the pin numbers match when the module and carrier board connectors are mated. See the following figure. The orientation shown matches the carrier board in the upright position as well as the layout file.

Figure 3-2. 699-pin Connector Pin Orientations



3.2 Module to Carrier Board Spacing Details

The spacing between the module PCB and the carrier board PCB are shown in the following figures for the following two cases:

- 5.5 mm connector on the carrier board (8mm nominal spacing)
- 2.5 mm connector (5 mm nominal spacing).

The standoffs to support the module are located between the carrier board and the bottom plate.

Figure 3-3. 5.5 mm Height on Carrier Board – Molex Part # 2034560003

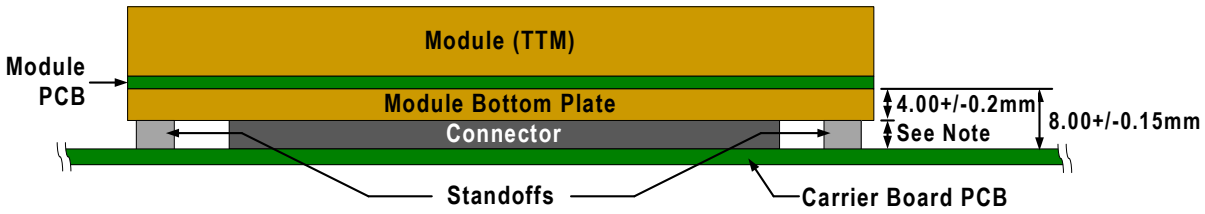
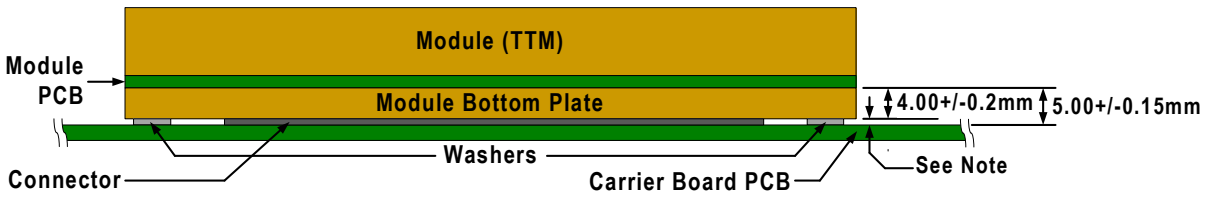


Figure 3-4. 2.5 mm Height on Carrier Board – Molex Part # 2048430001



Notes: See Section 3.3 on recommendations for standoff heights.

If the Molex Part # 2048430001, 2.5 mm height connector is used, there can be no components under the module on the carrier board due to the extremely limited clearance.

3.3 Module to Carrier Board Standoff Height Recommendations

Standoffs/Spacers are required between the module bottom plate and the carrier board. The height should be chosen to accommodate the tolerances in the bottom plate and connector mating heights as well as the standoff itself. If the standoff is too short, the carrier board PCB may warp as the mounting screws are tightened. The two cases (5.5 mm and 2.5 mm connector on carrier board) are described in this section and are followed with tables that show the possible permutations of tolerances across the three items involved. (bottom plate, mated connectors, and spacers). The platform designer can determine if a different height would be more appropriate but should consider both the PCB warpage (standoff height too short) and sweep range to find the best balance.

The following examples are based on Molex parts using spacer heights and spacer tolerances to produce a workable solution.

Molex Part # 2034560003 (5.5 mm height – 8.00+/-0.15 mm board to board spacing) case

For this case, a standoff height of 4.5 mm is recommended. This is based on a standoff with ±0.13 mm height tolerance. The tolerance for the bottom plate is ±0.2 mm and for mated connectors the tolerance is ±0.15 mm.
Table 3-1 shows example calculations using the connector board spacing, module bottom plate height and recommended standoff height with tolerances mentioned.

Table 3-1. Standoff Height Calculations for 5.5 mm Height Connector Case

Board to Board Spacing (mm)	Bottom Plate Height (mm)	Gap (mm)	Standoff Height	Board to Board Spacing (mm)
7.85	3.8	4.05	4.37	0.32
7.85	3.8	4.05	4.63	0.58
7.85	4.2	3.65	4.37	0.72
7.85	4.2	3.65	4.63	0.98
8.15	3.8	4.35	4.37	0.02
8.15	3.8	4.35	4.63	0.28
8.15	4.2	3.95	4.37	0.42
8.15	4.2	3.95	4.63	0.68
			Connector sweep range	1.5
			Min to Max sweep usage	0.98
			Remaining sweep	0.52

Notes:

1. Positive values mean no PCB warpage but less sweep. Negative values can result in PCB warpage.
2. The mating connector height tolerance comes from the Molex connector specification.
3. The connector contact sweep range can be found on the Molex website in the Mirror Mezz area.
4. The module bottom plate height/tolerance can be found in the *Jetson AGX Xavier Data Sheet*.

Molex Part # 2048430001 (2.5 mm height – 5.00+/-0.15 mm board to board spacing) case

For this case, a standoff height of 1.5 mm is recommended. This is based on a standoff (washer) with ±0.13 mm height tolerance. The tolerance for the bottom plate is ±0.2 mm and for mated connectors the tolerance is ±0.15 mm. Note that washers may typically have significantly larger tolerances which should be considered. Table 3-2 shows example calculations using the connector board spacing, module bottom plate height and recommended standoff/washer height with tolerances mentioned.

Table 3-2. Standoff Height Calculations for 2.5 mm Height Connector Case

Board to Board Spacing (mm)	Bottom Plate Height (mm)	Board to Bottom Plate Gap (mm)	Standoff Height (mm)	Space Beyond Ideal Mating Spec. (mm)
4.85	3.8	1.05	1.37	0.32
4.85	3.8	1.05	1.63	0.58
4.85	4.2	0.65	1.37	0.72
4.85	4.2	0.65	1.63	0.98
5.15	3.8	1.35	1.37	0.02
5.15	3.8	1.35	1.63	0.28
5.15	4.2	0.95	1.37	0.42
5.15	4.2	0.95	1.63	0.68
Connector sweep range (From Connector Spec)				1.5
Worst case space beyond the ideal connector mating case (from table above)				0.96
Remaining connector pin contact length				0.54

Notes:

1. Positive values mean no PCB warpage but less sweep. Negative values can result in PCB warpage.
2. See additional notes in the "Notes" section of Table 3-1.

3.4 Module Installation and Removal

To install the Jetson AGX Xavier Series module correctly, follow the following sequence and mounting hardware instructions:

1. Connectors should be parallel with respect to each other during mating.
2. Use a smooth motion during mating (no mechanical shock, knocking, hammering).
3. It will be ideal if push/pressure points are marked on the "B" side of the PCB for operators.
4. The top and bottom PCB are to be bolted to enhance reliability.
5. Secure with M3 screws (4x) from the top of the module. Torque the screws to 2.5 lbf-in.

If a fixture is used to do the mating, then that fixture should hold the mating connectors parallel to within ± 2 degrees. Also, the fixture should allow the connectors to become parallel as the mating process progresses.

To remove the Jetson AGX Xavier Series module correctly, follow the following sequence and mounting hardware instructions:

1. The PCB design needs to have enough finger reachability/space required to hold the board for un-mating.
2. Remove mounting screws (4x) from the top of the module.
3. Rock the top board a few times, no more than ± 3 degrees, to gradually disengage the connectors.

Figure 3-5. Module Removal

Chapter 4. Reference Design Considerations

The Jetson AGX Xavier Developer Kit Carrier Board design files are provided as a reference design. This chapter describes details necessary for designers to know to replicate certain features if desired. In addition, aspects of the design that are specific to the NVIDIA developer kit usage but not useful or supported on a custom carrier board are also identified.

Most of the features implemented on the Jetson AGX Xavier Developer Kit carrier board design can be duplicated by copying the connections from the P2822 carrier board reference design. This following listed features have aspects that would require additional information.

- **Button Power MCU:** The developer kit carrier board implements a button power MCU (EFM8SB10F2G). This device is programmed with firmware that is available on the Jetson Download Center. The posting is titled *Jetson AGX Xavier and Jetson Xavier NX Power Button Supervisor Firmware*. The connections used on the reference design must be followed exactly and the firmware provided must be used to ensure correct functionality.
- **USB Type C PD Controller:** Designs that intend to follow the NVIDIA carrier board design and include the Type C PD Controller (CYPD4226 - U513 on the P2822 carrier board) need to replicate the circuitry on the latest carrier board exactly. The firmware binary is used to program the Cypress CYPD4226 controller. The customer should get the flashing instructions from Cypress. No support or source code is provided for this firmware. If modifications or source code are required, Cypress should be contacted directly for support. This firmware binary is released under the L4T firmware EULA.
- **DV/Dt circuit:** A portion of the P2822 discharge circuit includes a means of detecting when a sudden power loss has occurred. This DV/Dt circuit triggers when the input voltage droops about 0.5V. The intent of the circuit is to provide as much time as possible to discharge critical carrier board supplies before the module loses power in order to meet power-down sequence requirements. This circuit is recommended but may need to be tuned depending on the power supply characteristics and the power requirements of a design. See Section 5.5 "Power Discharge" for details.

The following list is the Jetson AGX Xavier Developer Kit carrier board features that should not be copied as they are not required or useful for a custom carrier board design or will not be supported by NVIDIA.

- **The ID EEPROM (P2822 – U501)** is a feature that is used for NVIDIA internal purposes, but not useful on a custom design. A similar function may be desired for a custom design, but the NVIDIA software will not interact with these devices and the I2C address used by the developer kit carrier board ID EEPROM on the I2C2 interface (7'h57) should be avoided.
- **Debug connector and FTDI circuit:** These features are used at NVIDIA for internal debugging and development purposes. These are not required, and support will not be provided if implemented. Designers have the option to implement something similar on their custom carrier boards but should develop their own circuit to meet their needs.

Chapter 5. Power

This chapter describes the power specifications for the Jetson AGX Xavier Series module.

CAUTION: Jetson AGX Xavier is not hot-pluggable. Before installing or removing the module, the main power supply (to SYS_VIN_HV and SYS_VIN_MV pins) must be disconnected and the power rails allowed to discharge to <0.6V.

Note: Additional power, system, and thermal signals related to safety can be found in Section 15.5 "Safety MCU JAXi Only."

Table 5-1. Power, System, and Thermal Pin Descriptions

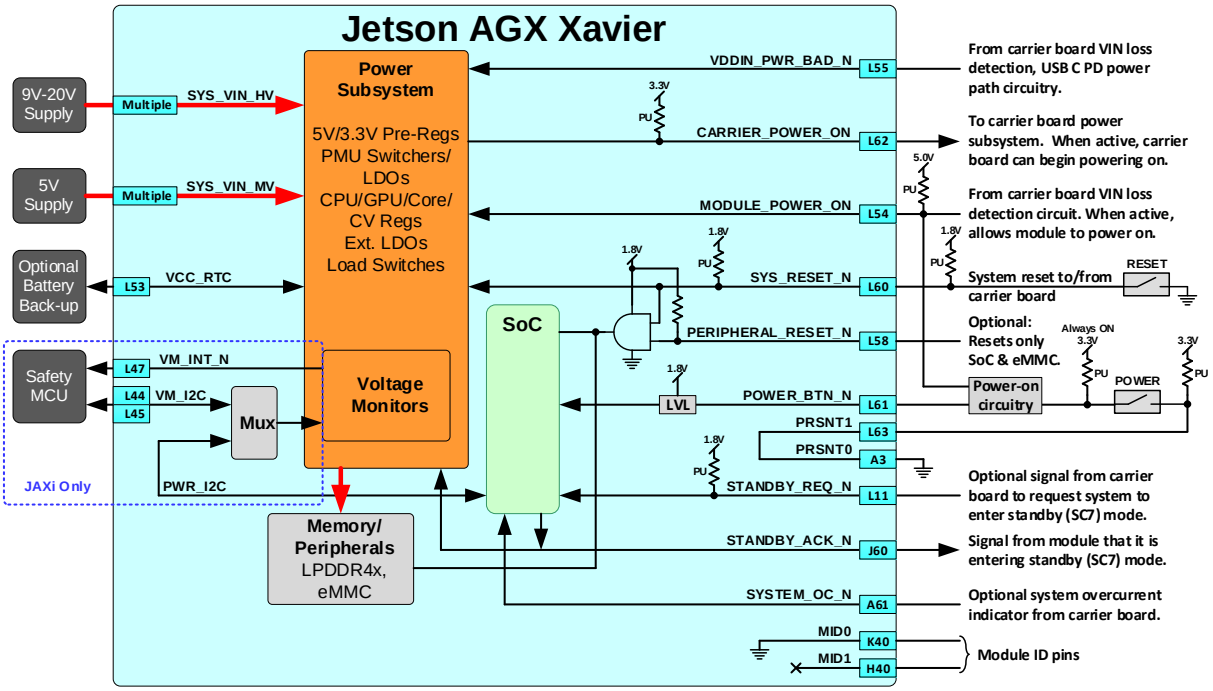
Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
Note 1	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V	–	–
Note 2	SYS_VIN_MV	–	System Voltage Input - Medium	Main Medium Voltage DC Input	Input	Power: 5.0V	–	–
L53	VCC_RTC	–	Real-Time-Clock. Optionally used to provide back-up power for RTC. Connects to Lithium Cell or super capacitor on carrier board. PMIC is supply when charging cap/cell. Super cap or coin cell is source when system is disconnected from power.	Battery back-up using Super-capacitor	Bidir	Power: Input Voltage Range: 1.65V-5.5V Output Voltage Range: See Note 6	–	–
L62	CARRIER_ POWER_ON	–	Carrier Power On. Used as part of the power up sequence. When asserted, it is safe for the carrier board to power up. 100kΩ pull-up to 3.3V on module.	Used to enable 1.8V/3.3V regulators and routed to power button supervisor and discharge circuits.	Output	na	–	–
L10	FORCE_ RECOVERY_N	SOC_GPIO00	Force Recovery strap pin. Held low when SYS_RESET_N goes inactive (power-on or reset button press) to enter force recovery mode.	Routed to Force Recovery button and automation header.	Input	CMOS – 1.8V	ST	pu
L54	MODULE_ POWER_ON	–	Module Power On. Signal to module to start power-on sequence. Driven by power button supervisor if implemented. Open-drain if power button supervisor MCU not implemented. If non-MCU circuit used, signal should have a 100kΩ pull-up to VDD_5V.	Generated by power button supervisor or non-MCU power-on circuit.	Input	5.0V Open-Drain (Non-MCU case). CMOS – 3.3V (Power Button MCU case)	–	–
L58	PERIPHERAL_ RESET_N	–	Peripheral Reset. Driven from carrier board to force reset of SoC and eMMC and QSPI (not PMIC). 100kΩ pull-up to 1.8V on the module.	Unused	Input	CMOS – 1.8V	–	–

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
L61	POWER_BTN_N	POWER_ON	Power Button. Used to initiate a system power-on and to enter/exit SC7. 3.3V to 1.8V level shifter on the module.	Generated by power button supervisor.	Input	Open Drain, 3.3V	ST	pd
J60	STANDBY_ ACK_N	SOC_PWR_REQ	Standby Acknowledge. Indicates module is in standby (SC7 state). Signal should only be observed and not affected by the carrier board. A buffer on the signal is recommended if it will be connected in the platform.	Automation header	Output	CMOS – 1.8V	ST	1
L11	STANDBY_ REQ_N	SOC_GPIO01	Standby Request. Requests module enter standby (SC7 state). 10kΩ pull-up to 1.8V is present on the module.	Not used	Input	CMOS – 1.8V	ST	pu
L60	SYS_RESET_N	SYS_RESET_N	System Reset: Connected to NRST_IO of PMIC. Bidirectional reset driven from PMIC to carrier board for devices requiring full system reset. Can also be driven from carrier board to module to initiate full system reset (including PMIC) (i.e. From RESET button). 1kΩ pull-up to 1.8V is present on the module.	Various system reset functions. Also routed to reset button, JTAG header, and automation header.	Bidir	Open Drain, 1.8V	JT_RST	z
A61	SYSTEM_OC_N	BATT_OC	Battery Over-current (and Thermal) warning	Automation Header	Input	CMOS – 1.8V	ST	pd
F61	VCOMP_ ALERT_N	VCOMP_ALERT	Supports either GPIO operation or SoC Thermal Over-current alert #1.	Unused	Input	CMOS – 1.8V	ST	pd
L55	VDDIN_PWR_ BAD_N	–	VDD_IN Power Bad. Carrier board indication to the module that the VDD_IN power is not valid. Carrier board should de-assert this (drive high) only when SYS_VIN_HV/MV have reached the required voltage levels and are stable. This prevents SoC from powering up until the main input supply voltages are stable. 10kΩ pull-up to 5V on the module.	Driven by VIN loss detection, USB PD power and discharge circuits. Used in power button supervisor circuit.	Input	Open-drain – 5.0V	–	–
B54	WDT_RESET_ OUT_N	SOC_GPIO23	Watchdog Timeout	Unused	Output	CMOS – 1.8V	ST	1
L52	OVERTEMP_N	SOC_GPIO55	Force Power Off Request	Routed to power button supervisor circuit.	Input	CMOS – 1.8V	ST	Pd
L56	TEMP_ALERT_N	–	ALERT*/THERM2 from Temp Sensor on module	Unused	Output	Open Drain, 1.8V	–	–
A3	PRSNT0	–	Present #[1:0]. Tied together on module. Used to detect when module is connected to the carrier board. Can be used to keep carrier board from powering the module until the module is installed in the carrier board.	Tied to GND	na	na	–	–
L63	PRSNT1	–		Tied to one side of power button.				
K40	MID0	–	Module ID #0	Tied to GND	na	Na	–	–
H40	MID1	–	Module ID #1	Unconnected	na	na		

Notes:

1. SYS_VIN_HV pin #s: C65, D65, E65, F65, G65, H65, J65, C64, D64, E64, F64, G64, H64, J64, B63, C63, E63, F63, G63, J63, B3, D3, F3, H3, K3, C2, D2, E2, F2, G2, H2, J2, C1, D1, E1, F1, G1, H1, J1.
2. SYS_VIN_MV pin #s: L39, L38, L35, L34, L31, L30, L27, L26, L23, L22.
3. In the Type/Dir column, Output is from Jetson AGX Xavier. Input is to Jetson AGX Xavier. Bidir is for Bidirectional signals.
4. The MPIO Pad Codes are described in the Xavier Series (SoC) Technical Reference Manual "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
5. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.
6. The output voltage is configurable in the PMIC. It can be disabled if a non-rechargeable source is connected, or set to 2.5V, 3.0V, 3.3V or 3.5V.

Figure 5-1. Power Block Diagram



5.1 Supply Allocation

Table 5-2 describes the power subsystem allocation for Jetson AGX Xavier.

Table 5-2. Internal Power Subsystem Allocation

Power Rails	Usage	(V)	Power Supply	Source
VDD_CPU	SoC CPU rail	Variable	NCP81276 and FDMF5833 (x2)	SYS_VIN_HV
VDD_GPU	SoC GPU rail	Variable	NCP81276 and FDMF5833 (x2)	SYS_VIN_HV
VDD_CORE (SOC)	SoC Core rail	Variable	NCP81276 and FDMF5833 (x2)	SYS_VIN_HV
VDD_CV	SoC CV rail	Variable	NCP81276 and FDMF5833 (x2)	SYS_VIN_HV
VDDIO_SYS_1V0	SoC AVDDIO_HDMI_DP[3:0], PEX_DVDD, NVHS0_DVDD rails	1.0	PMIC Switcher SD0	SYS_VIN_MV
VDDIO_SYS_1V8HS	See Note 1	1.8	PMIC Switcher SD1	SYS_VIN_MV
VDDIO_SYS_1V8LS	See Note 2	1.8	PMIC Switcher SD2	SYS_VIN_MV
AVDD_CSI_1V2	SoC AVDD_CSI and VDDIO_UFS rails (See note 3)	1.2	PMIC LDO7	SYS_VIN_MV
EN_VDD_1V0	Enable for FETs gating discharge of VDDIO_SYS_1V0 rail (See note 3)	na	PMIC LDO8	SYS_VIN_MV
VDDIO_AO_1V8	See note 4	1.8	PMIC Switcher SD3	SYS_VIN_MV
DDR_AP_1V1	SoC VDDIO_DDRx rail	1.1	PMIC Switcher SD4	SYS_VIN_MV
VDD_RTC	SoC RTC rail	Variable	PMIC LDO0	SYS_VIN_MV
DDR_VDD2_ 1V1_EN	See Note 5	Na	PMIC LDO1	SYS_VIN_MV
VDDIO_AO_3V3	SoC VDDIO_AUDIO_HV and VDDIO_AO_HV rails	3.3	PMIC LDO2	SYS_VIN_MV
VDD_EMMC_3V3	eMMC device 3.3V rail	3.3	PMIC LDO3	SYS_VIN_MV
VDD_USB_3V3	SoC AVDD_USB rail	3.3	PMIC LDO5	SYS_VIN_MV

Power Rails	Usage	(V)	Power Supply	Source
VDD_SDIO_3V3	SoC VDDIO_SDMMC1_HV and VDDIO_SDMMC3_HV rails	3.3	PMIC LDO6	SYS_VIN_MV
DDR_VDD2_1.1V	SoC VDDIO_VDD2_DDRx and DRAM VDD2 rails.	1.1	LTC3636	SYS_VIN_HV
VDD_DDRQ	VDDIO_DDRxLV and LPDDR4x VDDQ rails	0.6 LPDDR4x	LTC3636	SYS_VIN_HV

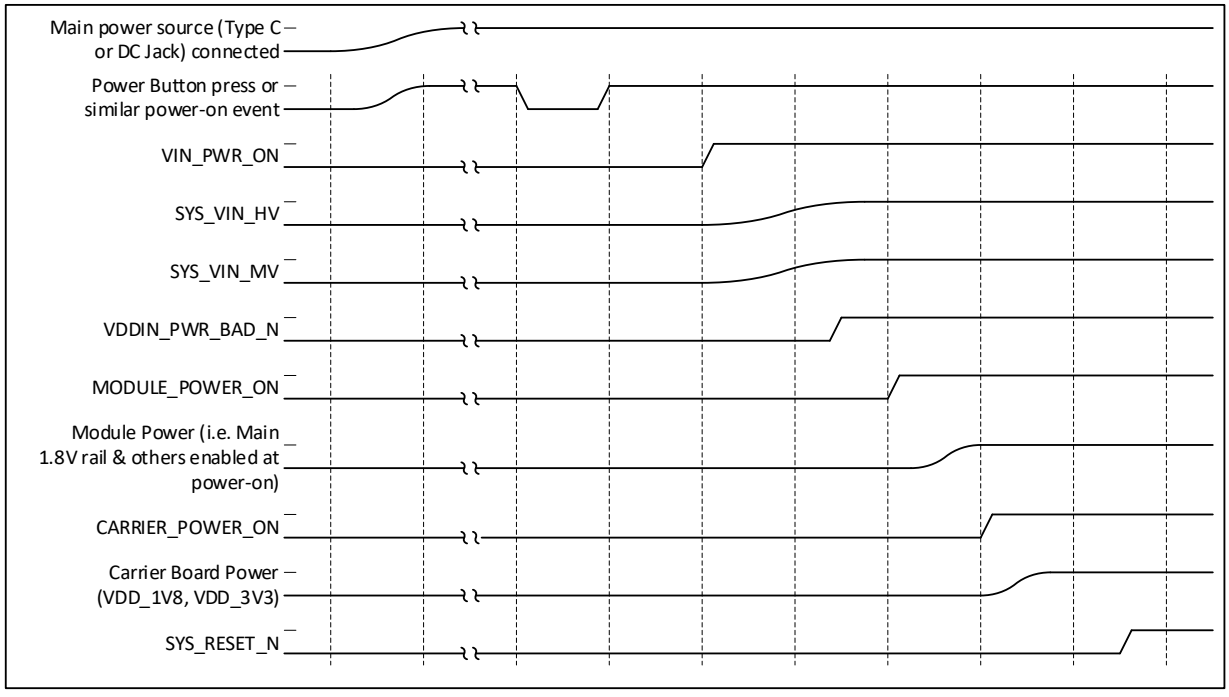
Notes:

1. SoC AVDD_PLL_NVHS_EUTMIP, VDD_HDMI_DP_PLL_0_1/1_3, PEX_HVDD, NVHS0_HVDD and NVHS0_PLL0_HVDD rails
2. SoC VDDIO_UART/AUDIO/SDMMC4/DMMC3_HV_VCLAMP/ VDDIO_SDMMC1_HV_VCLAMP/CONN/EQOS/QSPI/, AVDD_PLL_AA1_CV_ADC/DD2D3D4DPHBCS/CC2C3PADC_BPMP/C4_REFE, eMMC device VCCQ and QSPI device VDD rails.
3. These rails are sourced from the PMIC Switcher SD2 used for VDDIO_SYS_1V8LS which is sourced from SYS_VIN_MV.
4. SoC VDDIO_EDP/PEX_CTL/DEBUG/CAM/AO/VREFR0/ SYS, VPP_FUSE, AVDD_PLL_AON/MSC/GADC_M/MSD/XADC_MSB, VCLAMP_USB, AVDD_OSC, LPDDR4x device VDD1, Temp Sensor VDD
5. Enable (RUN2 pin) for VDD_DDRQ supply and Enable for discharge of DDR_VDD2_1.1V, VDDIO_SYS_1V8HS/SYS_1V8LS/AO_1V8 rails.

5.2 Power Sequencing

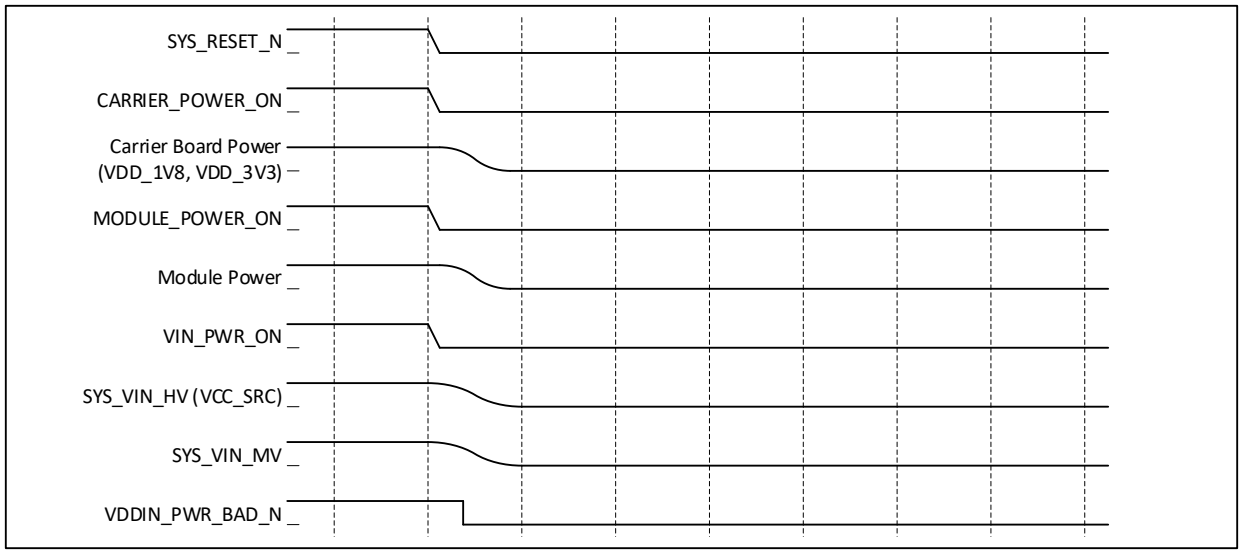
The following figures describe the power sequencing for Jetson AGX Xavier.

Figure 5-2. Power Up Sequence



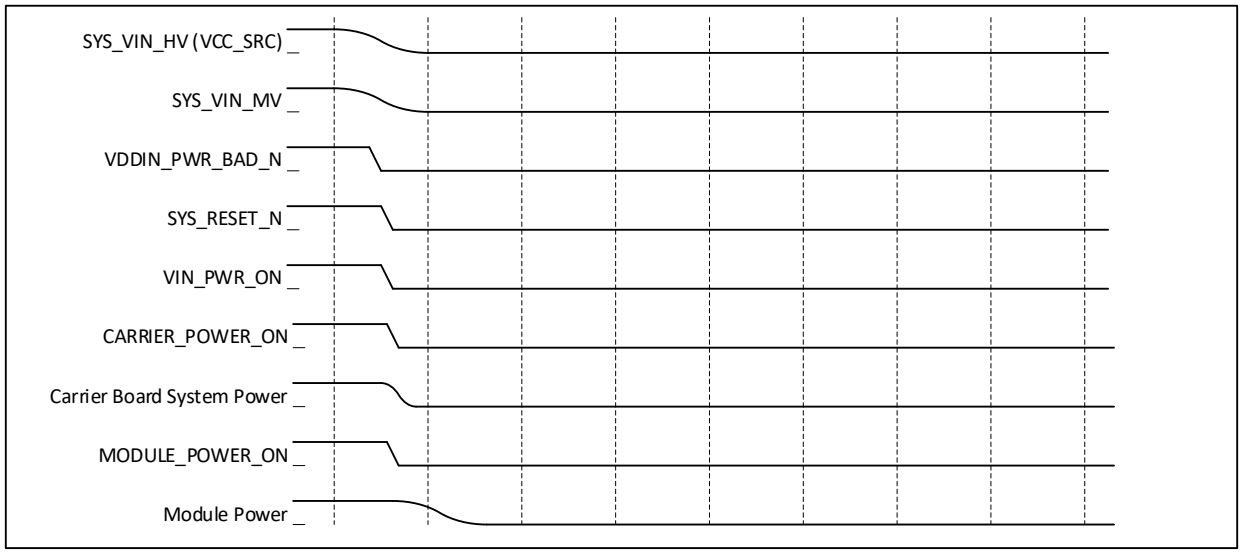
Note: The signal VIN_PWR_ON shown in the power sequences is not a pin on the module. This signal is used on the DevKit design to enable the SYS_VIN_HV and SYS_VIN_MV supplies.

Figure 5-3. Power Down Sequence Controlled Case



Note: SYS_VIN_MV must go below 100 mV before system can be powered on again.

Figure 5-4. Power Down Sequence Uncontrolled Case



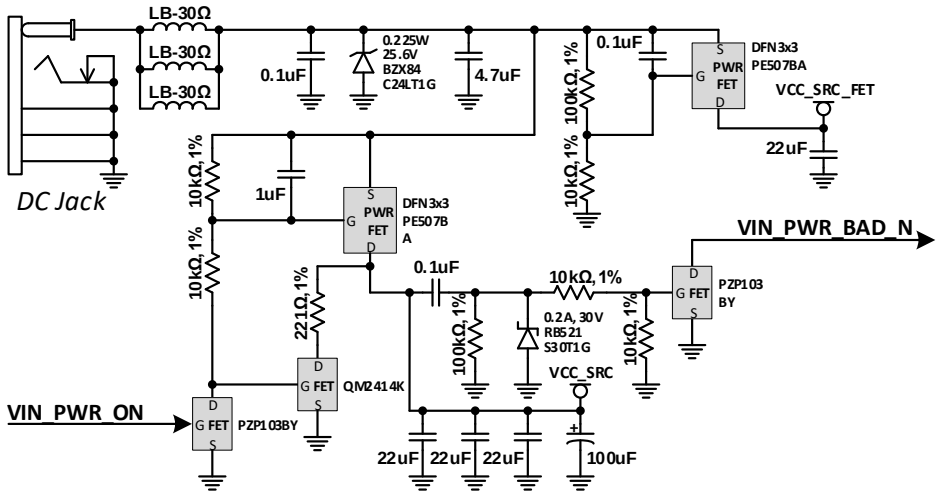
Note: SYS_VIN_MV must go below 100 mV before system can be powered on again.

5.3 SYS_VIN_HV Input

The Jetson AGX Xavier Developer Kit carrier board allows the main system power to be supplied either by one of the USB Type C connectors or a DC power Jack. The details for implementing Type C for power, etc. can be found in the P2822 reference schematics. If a design only requires a simple DC power jack, the circuit in the following figure can be used.

Note: Designs that intend to follow the NVIDIA carrier board design and include the Type C PD Controller (CYPD4226 - U513 on NVIDIA carrier board) need to replicate the circuitry on the latest P2822 carrier board exactly. NVIDIA will provide the binary and the customer should get the flashing instructions from Cypress.

Figure 5-5. Simplified DC Jack Power Connections



Note: Designs which implement an eFUSE or current limiting device on the input power rail of the module should select a part that DOES NOT limit reverse current.

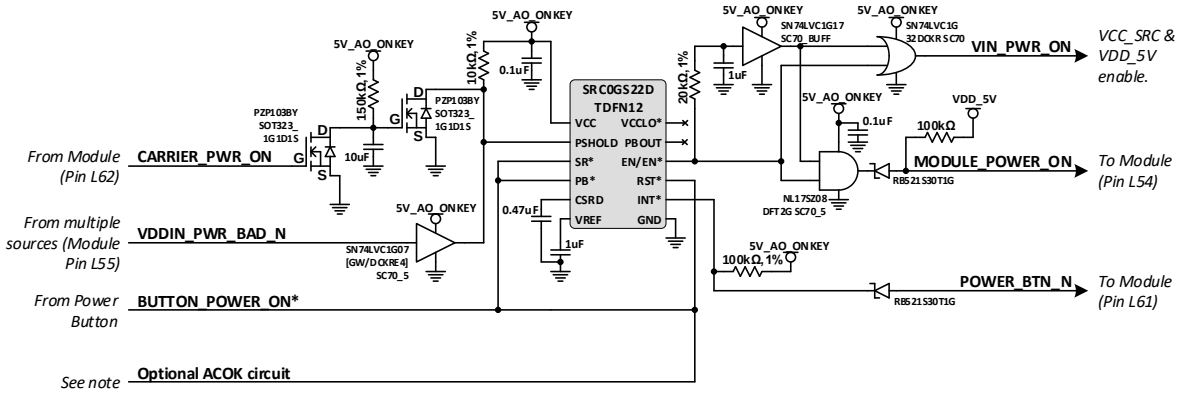
5.4 Power-On

This section details the power-on features for Jetson AGX Xavier.

5.4.1 Power-On No MCU

The Jetson AGX Xavier Developer Kit carrier board implements a button power-on supervisor circuit that utilizes an EFM8SB10F8G-A MCU from Silicon Labs. For designs that do not want to use this approach, a circuit that does not use the MCU is shown in the following figure.

Figure 5-6. Simplified Button Power-On Circuitry



Notes:

1. To support auto-power-on or for a connection to a charger, see Figure 5-7.
2. Designs which implement an eFUSE or current limiting device on the input power rail of the module should select a part that DOES NOT limit reverse current.

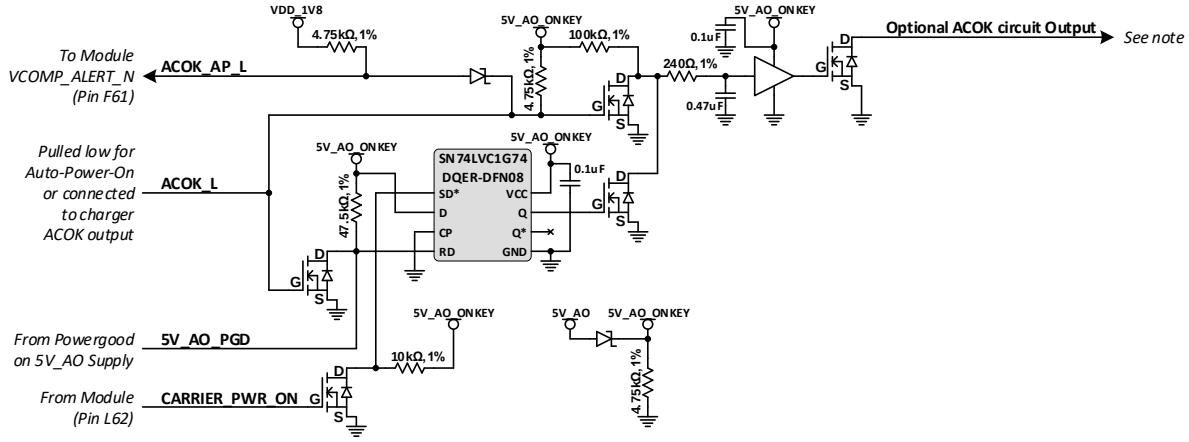
Table 5-3. Simplified Button Power Circuitry Timing

Timing	Parameter	Min	Units
$T_{DEBOUNCE}$	Power button active duration	>50	ms

5.4.1.1 Auto Power-On Option No MCU

For designs that will not have a power button but should power on when the main power supply is connected, the optional ACOK circuit shown in Figure 5-7 should be implemented and the ACOK_L signal pulled to GND.

Figure 5-7. Optional ACOK Circuitry



Note: See Figure 5-6.

5.4.2 Power Button Supervisor MCU Power-On

The NVIDIA Jetson AGX Xavier carrier board implements a power button supervisor. This supervisor is a low power device meant to intercept push-button (momentary) switches to control ON/Enable signals to the module PMIC and main processor. This supervisor is always powered and allows close to complete system power OFF while providing proper timing for ON/OFF signals to the system. The selected MCU to perform this function is the EFM8SB10F8G-A-QFN20 from Silicon Labs.

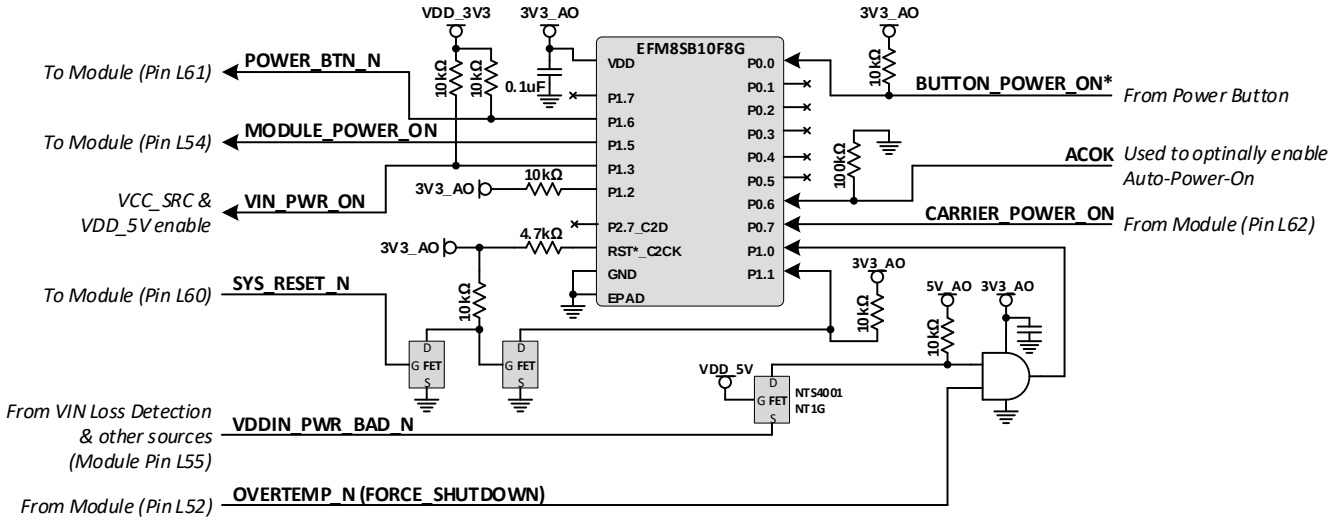
Note: Designs that intend to follow the NVIDIA carrier board design and include the EFM8SB10F8G-A-QFN20 MPU for Button Power Button control need to replicate the circuitry on the latest P2822 carrier board exactly. NVIDIA will provide the binary and the customer should get the flashing instructions from Silicon Labs. Otherwise, another solution such as the one described earlier in the Power-On (No MCU) can be used.

Table 5-4. Power Button Supervisor Control Signals

Signal Name	Associated Module Pin #	I/O Type	Trigger Level	Drive Mode	Description	MCU Pin
BUTTON_POWER_ON*		Input (debounced)	Level	OD (HiZ)	Power Button	P0.0
ACOK		Input (debounced)	Edge	OD (HiZ)	Determine when USB power is supplied	P0.6
CARRIER_POWER_ON	L62	Input	Level	OD (HiZ)	Closed loop on power output	P0.7
RESET_N (SYS_RESET_N)	L60	Input	Edge	OD (HiZ)	Monitor / Power Good mask	P1.1
FORCE_SHUTDOWN_N (OVERTEMP_N)	L52	Input	Level	OD (HiZ)	Triggers shutdown sequence	P1.0
BRD_SEL		Input		OD (HiZ)	Strap pin for board selection	P1.2
VIN_PWR_ON		Output		PP	Enable power to module	P1.3
MODULE_POWER_ON	L54	Output		PP	Enable input to PMIC	P1.5
POWER_BTN_N	L61	Output		OD	Buffered output of power button signal	P1.6

Note: OD – Open-drain. PP = Push-pull.

Figure 5-8. Power-On Button Circuit



5.4.2.1 Defined behaviors

For all actions triggered by BUTTON_POWER_ON*, there will be a de-bounce time before triggering any output signal. All timings below are referenced from AFTER the de-bouncing. Therefore, a "0 ms" value indicates that the signal should start right after de-bounce. De-bounce time is 20 ms.

5.4.2.2 Power OFF -> Power ON (Power Button Case)

Power button press use case: User presses the Power Button briefly, and the MCU sends the power enable signals to the module (VIN_PWR_ON) and to the PMIC on the module (MODULE_POWER_ON). The signal representing the Power Button to Jetson AGX Xavier (POWER_BTN_N), will have the same (brief) duration of the Power Button input to the MCU. Once the power button is pressed, the power OK input (ACOK) is ignored, as the power ON sequence is already initiated by the power button.

Figure 5-9. Power-OFF to On Sequence Power Button Case

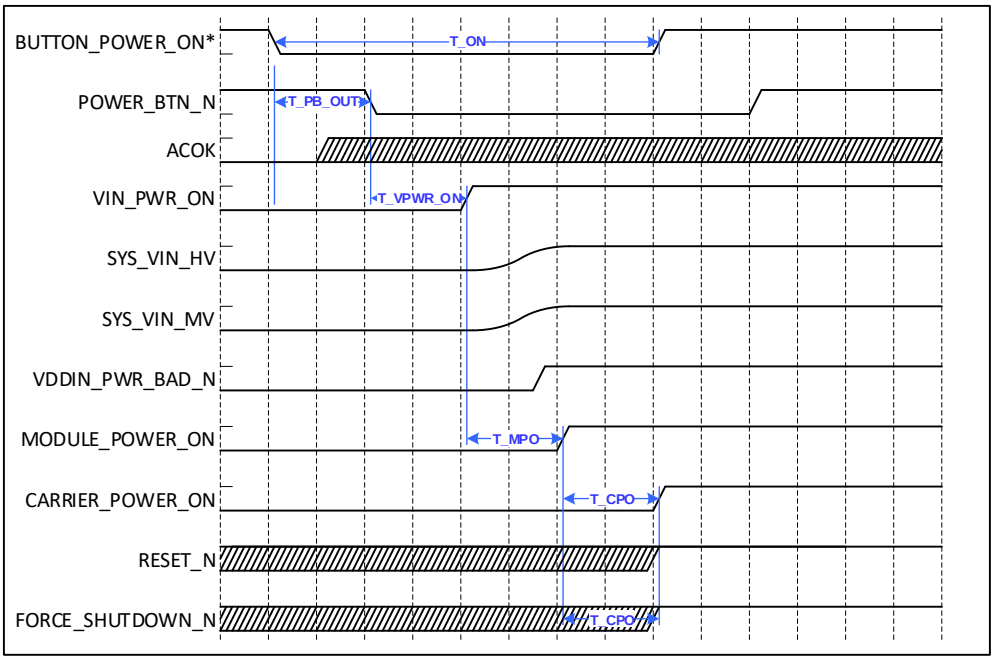


Table 5-5. Power-OFF to On Timing Power Button Case

Timing	Parameter	Typical	Units
T_PB_OUT	Delay to POWER_BTN_N assertion (de-bounce only)	20	ms
T_VPWR_ON	Delay to first rail ON	0	ms
T_MPO	MODULE_POWER_ON (module PMIC enable) delay from power VIN_PWR_ON rising edge	80	ms
T_CPO	Maximum allocated delay to CARRIER_POWER_ON assertion	10	ms

5.4.2.3 Power OFF -> Power ON (Auto-Power-On Case)

When the user connects the main power source, the MCU sends the power enable signals to the module (VIN_PWR_ON) and enables MODULE_POWER_ON. This is accomplished by having the ACOK signal driven high instead of pulled to GND.

The signal representing the Power Button to Jetson AGX Xavier (POWER_BTN_N) will continue following the power button (BUTTON_POWER_ON*) behavior. However, once the power ON sequence is initiated by the connection of the main power source, and ACOK is driven high (by push-pull driver powered from 3V3_AO), the power button signals will not affect the MCU behavior until the PWR_GOOD signal verification is complete.

Figure 5-10. Power-OFF to On Sequence Auto Power-On Case

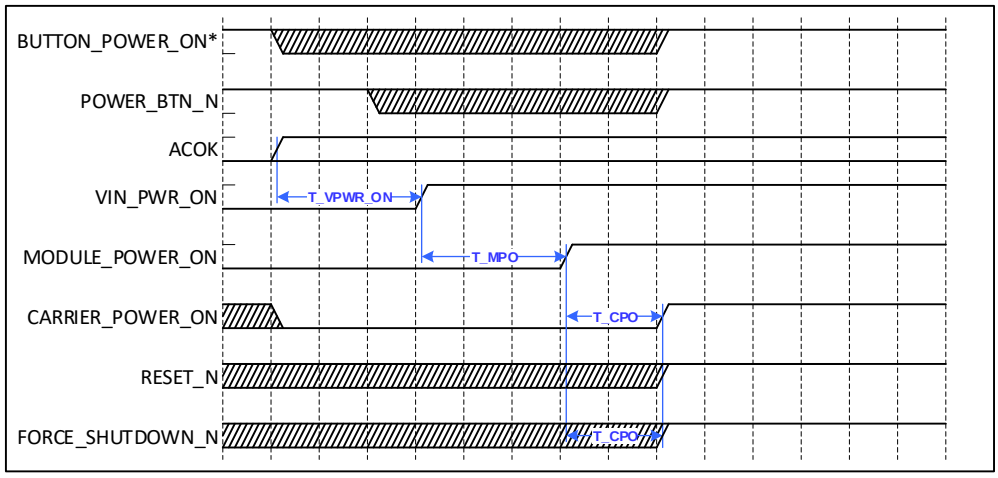


Table 5-6. Power-OFF to On Timing Auto Power-On Case

Timing	Parameter	Typical	Units
T_VPWR_ON_AC	Delay from ACOK detected high with main power source applied to first rail ON (de-bounce only)	20	ms
T_MPO_AC	MODULE_POWER_ON active delay from VIN_PWR_ON rising edge	80	ms
T_CPO_AC	Maximum allocated delay to CARRIER_POWER_ON active	10	ms

5.4.2.4 Power ON -> Power OFF (Power Button Held Low > 10 Seconds)

With the system in power ON state, the user holds the power button for more than 10 seconds. The same button signal is relayed to Jetson AGX Xavier through the buffered signal POWER_BTN_N. The system is forced to shut down at the 10 seconds mark.

Figure 5-11. Power-On to OFF Power Button Held Low > 10 Seconds

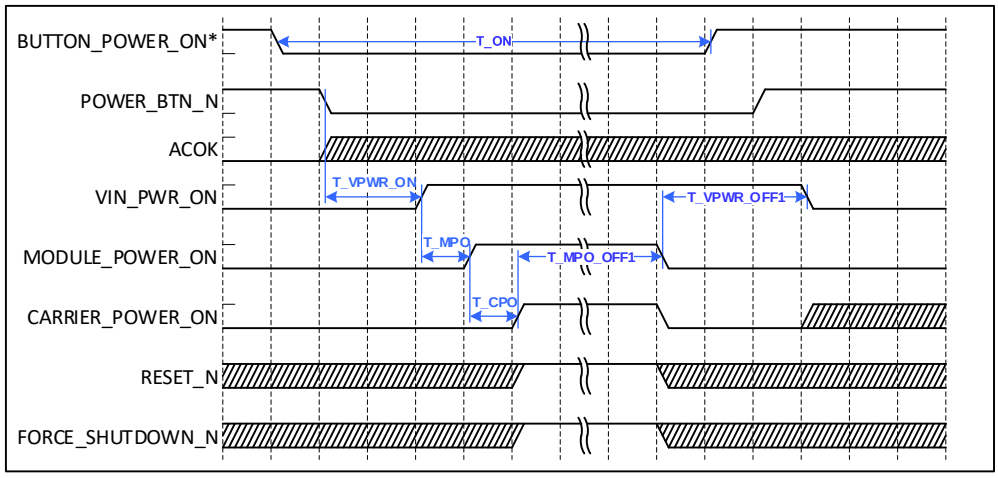


Table 5-7. Power-On to OFF Timing Power Button Held Low > 10 Seconds

Timing	Parameter	Typical	Units
T_ON	Power button active duration for forced OFF (T_PWR_ON + T_MPO_ON + T_CPO + T_MPO_OFF1)	> 10	s
T_VPWR_ON	Delay to first rail ON (de-bounce only)	20	ms
T_MPO_OFF1	Wait time to force MODULE_POWER_ON OFF	10	s
T_MPO_ON	Enable delay from VIN_PWR_ON rising edge	80	ms
T_CPO	Maximum allocated delay to detect CARRIER_POWER_ON	10	ms
T_VPWR_OFF1	Delay to first rail OFF	10	ms

5.5 Power Discharge

To meet the Power Down requirements, discharge circuitry is required. Figure 5-12 shows a simplified version of what is in the P2822 Jetson AGX Xavier carrier board. The DISCHARGE signal is generated, based on a transition of the CARRIER_POWER_ON signal or the removal of the main supply (VDD_SRC). When DISCHARGE is asserted, the various carrier board rails that need to be discharged are pulled to GND. Removal of the VDD_SRC supply also causes VDDIN_PWR_BAD_N to go active which causes Jetson AGX Xavier to initiate a controlled shut down.

5.5.1 DV/Dt Circuit Considerations

The portion of the circuit that asserts VDDIN_PWR_BAD_N when power is removed is designed to start the shutdown as soon as a voltage drop of ~0.5V is detected. This DV/Dt circuit helps to provide more time to discharge the necessary rails before the module loses power. It is recommended that the circuit be kept as shown to provide the most margin for properly sequencing power off during sudden power removal cases. If the supply cannot

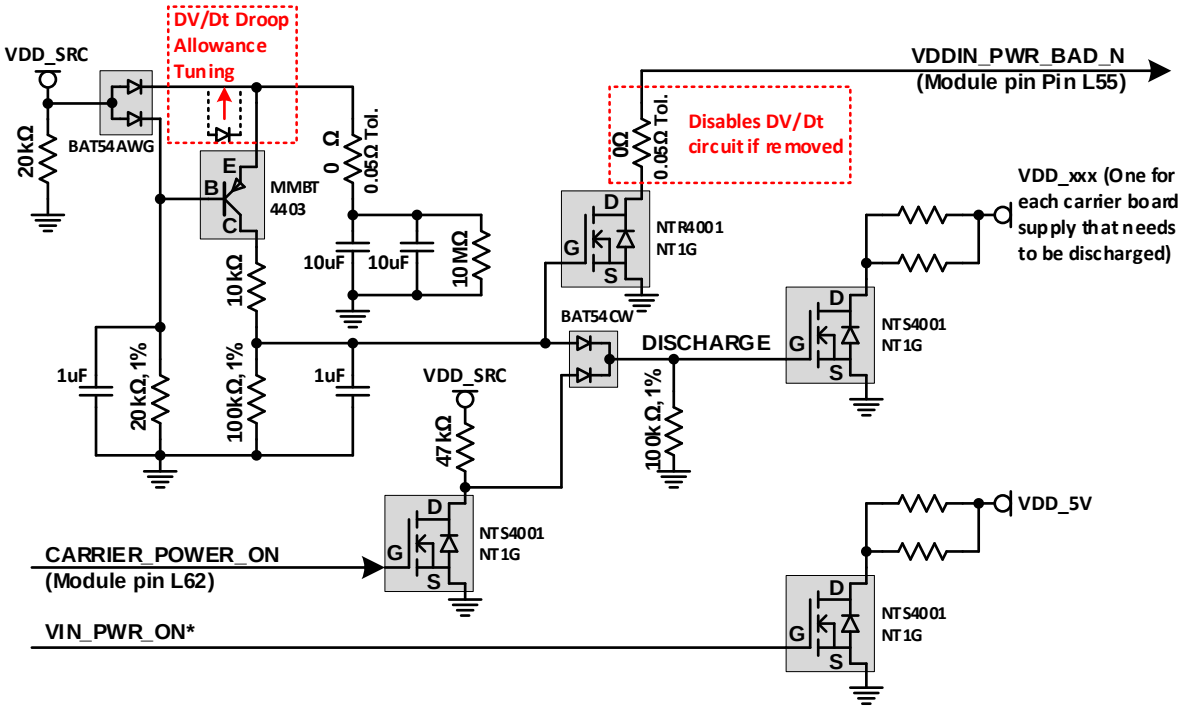
maintain the voltage level within 0.5V of nominal when large current changes occur, then either the supply may need to be improved or it may be necessary to modify the DV/Dt circuit. Supply changes could include:

- Improve supply to respond better to large fluctuations in power. If the improvements keep any droops to less than ~0.5V, the DV/Dt circuit may work as intended and provide the most margin for proper power-down sequencing during sudden power loss cases. This solution is highly recommended over making modifications that compromise the DV/Dt circuit.
- Use a higher voltage. Jetson AGX Xavier supports from 9V to 20V on the SYS_VIN_HV input. The higher the voltage used, the lower the current at the input. When large power changes occur during heavy computational loads, the effect on the supply voltage will be lowest when the input voltage is near the maximum.

Modifications to the DV/Dt circuit include two options shown in Figure 5-12.

- Remove the resistor in series with VDDIN_PWR_BAD_N which would disable completely the DV/Dt circuit. This would mean that during a sudden power removal case, the input supply voltage would have to drop to the level that would trigger the VIN loss detection circuit (see Section 5.6.1 "Power Loss Detection") which is ~7V to 8V. This change would remove all benefits of the DV/Dt circuit and make it more difficult to meet power-off sequencing requirements during sudden power removal cases. This should be a last resort fix.
- Add an additional diode in the path from VDD_SRC to the Emitter to allow for more voltage droop before triggering the DV/Dt circuit and shutting down the system. By default, the droop allowed is ~0.5V. By adding one diode, an additional 0.6V-0.7V droop would be allowed. This will reduce the benefit that the DV/Dt circuit provides and should be avoided if possible or kept to a minimum (one additional diode).

Figure 5-12. Power Discharge



Note: The resistor values in the discharge circuit for each rail should be tuned to bring the rail down in the proper timeframe.

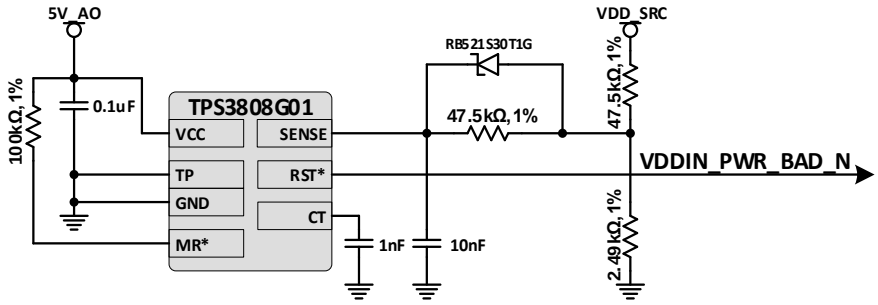
5.6 Power and Voltage Monitoring

This section describes the power and voltage monitoring for Jetson AGX Xavier.

5.6.1 Power Loss Detection

The circuit in Figure 5-13 is implemented on the NVIDIA Jetson AGX Xavier carrier board to detect a loss or unacceptable droop on the main power input (VCC_SRC).

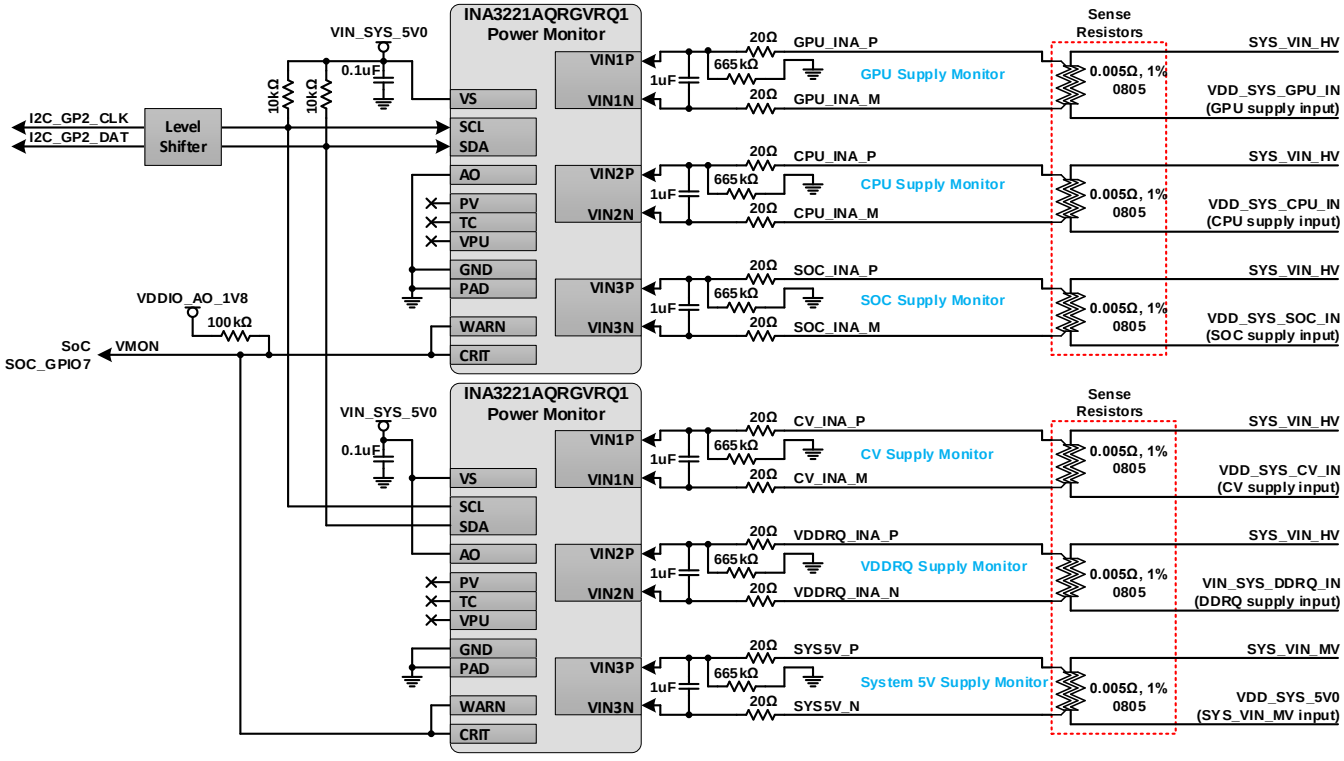
Figure 5-13. VIN Loss Detection Circuit



5.6.2 Power Monitor

Power monitors are provided on Jetson AGX Xavier. These monitor the VDD_GPU, VDD_CPU, VDD_SOC (Core), VDD_CV, VDD_DDRQ and SYS_VIN_MV Supplies. The monitors will toggle a WARN (Warning) or CRIT (Critical) output, depending on the power "seen" at the sense resistors and the thresholds set for each supply. This output is connected to the SOC_GPIO7 pin. The I2C address for the top power monitor (GPU/CPU/SOC) is 7'H40, and for the bottom power monitor (CV, VDDRQ, SYS_VIN_MV) is 7'H41).

Figure 5-14. Power Monitor



5.7 Deep Sleep or SC7

Jetson AGX Xavier supports a low power state called Deep Sleep or SC7. This can be entered under software control, and exited using various mechanisms, including wake capable pins that are listed in Table 5-8.

Table 5-8. Jetson AGX Xavier Signal Wake Events

Potential Wake Event (Reference Design Signal)	Module Pin Assigned	Wake #
PCIe Wake Request (PEX_WAKE_N)	PEX_WAKE_N	Wake01
SD Card Data 1 (SDCARD_D1)	SDCARD_D1	Wake03
Backlight PWM (BKLIGHT_PWM)	GPIO27	Wake04
GPIO 0 (CVB_GPIO0)	GPIO02	Wake08
System Overcurrent Control (SYSTEM_OC#)	SYSTEM_OC_N	Wake10
GPIO 1 (CVB_GPIO1)	GPIO11	Wake12
GPIO 3 (GPIO3/SD_WP)	GPIO29	Wake13
GPIO 2(CVB_GPIO2)	GPIO12	Wake15
Ethernet SMA MDIO (RGMII_SMA_MDIO)	RGMII_SMA_MDIO	Wake17
Ethernet Interrupt (ENET_INT)	ENET_INT	Wake20
I2C General Purpose 3 Data (I2C_GP3_DAT)	I2C3_DAT	Wake21
I2C General Purpose 4 Data (I2C_GP4_DAT)	I2C4_DAT	Wake22
Safe State (SAFE_STATE)	GPIO31	Wake25
Voltage Monitor (VMON)	VCOMP_ALERT_N	Wake26
Ethernet RX Control (RGMII_RX_CTL)	RGMII_RX_CTL	Wake28
Power On (POWER_ON)	POWER_BTN_N	Wake29
GPU Fault (GPU_FAULT)	GPIO01	Wake30
I2C General Purpose 1 Data (I2C_GP1_DAT)	I2C1_DAT	Wake31
PCIe L5 Clock Request (PEX_L5_CLKREQ_N)	PEX_L5_CLKREQ_N	Wake32
Board Identification 1 (BOARD_ID1)	UART1_CTS	Wake33
GPIO Expander 0 Interrupt (GPIO_EXP0_INT)	GPIO32	Wake34
USB OTG Identification (USB_OTG_ID)	GPIO30	Wake35
GPIO Expander 1 Interrupt (GPIO_EXP1_INT)	GPIO33	Wake36
GPIO Expander 2 Interrupt (GPIO_EXP2_INT)	GPIO34	Wake37
Watchdog Timer Reset Output (WDT_RESET_OUT)	WDT_RESET_OUT_N	Wake38
SPI 2 Chip Select 0 (SPI2_CS0#)	SPI2_CS0_N	Wake39
GPIO 5(CVB_GPIO5)	GPIO17	Wake40
I2C General Purpose 2 Data (I2C_GP4_DAT)	I2C2_DAT	Wake41
CAN 1 Data Input (CAN1_DIN)	CAN1_DIN	Wake42
CAN 0 Data Input (CAN0_DIN)	CAN0_DIN	Wake43
SPI 3 Clock (SPI3_CLK)	SPI3_CLK	Wake44
SPI 1 Chip Select 0 (SPI1_CS0#)	SPI1_CS0_N	Wake45
CAN 0 GPIO 1 (CAN0_GPIO1)	GPIO07	Wake46
CAN1 GPIO 1 (CAN1_GPIO1)	GPIO10	Wake48
SPI 1 Chip Select 1 (SPI1_CS1#)	SPI1_CS1_N	Wake50
Fan Tachometer (FAN_TACH)	FAN_TACH	Wake51
UART 1 Clear to Send (UART1_CTS)	UART2_CTS	Wake52
UART 2 Clear to Send (UART2_CTS)	UART5_CTS	Wake53
PCIe L1 Clock Request (PEX_L1_CLKREQ_N)	PEX_L1_CLKREQ_N	Wake54

Potential Wake Event (Reference Design Signal)	Module Pin Assigned	Wake #
SPI 3 Chip Select 0 (SPI3_CS0#)	SPI3_CS0_N	Wake56
SPI 3 Chip Select 1 (SPI3_CS1#)	SPI3_CS1_N	Wake58
Discrete GPU Alert (DGPU_ALERT)	GPIO03	Wake59
DP 0 Hot-Plug-Detect (DP0_HPD)	DP0_HPD	Wake60
USB VBUS Enable 0 (USB_VBUS_EN0)	GPIO22	Wake61
USB VBUS Enable 1 (USB_VBUS_EN1)	GPIO23	Wake62
DP 1 Hot-Plug-Detect (DP1_HPD)	DP1_HPD	Wake63
PCIe L3 Clock Request (PEX_L3_CLKREQ_N)	PEX_L3_CLKREQ_N	Wake65
GPIO 6(CVB_GPIO6)	GPIO24	Wake66
Force Recovery (FORCE_RECOVERY)	FORCE_RECOVERY_N	Wake67
Sleep (SLEEP#)	STANDBY_REQ_N	Wake68
Battery Low (BATLOW#)	GPIO28	Wake69
HDMI Consumer Electronics Control (HDMI_CEC)	HDMI_CEC	Wake70
DP 2 Hot-Plug-Detect (DP2_HPD)	DP2_HPD	Wake71

Chapter 6. General Routing Guidelines

6.1 Signal Name Conventions

The following conventions are used in describing the signals for Jetson AGX Xavier:

- Signal names use a mnemonic to represent the function of the signal. For example, Secure Digital Interface #3 Command signal is represented as SDCARD_CMD, written in bold to distinguish it from other text. All active low signals are identified by a # or an underscore followed by capital N (_N) after the signal name. For example, RESET_IN# indicates an active low signal. Active high signals do not have the underscore-N (_N) after the signal names. For example, SDCARD_CMD indicates an active high signal. Differential signals are identified as a pair with the same names that end with _P and _N, just P and N or + and - (for positive and negative, respectively). For example, USB1_DP and USB1_DN indicate a differential signal pair.
- I/O Type The signal I/O type is represented as a code to indicate the operational characteristics of the signal. The following table lists the I/O codes used in the signal description tables.

Table 6-1. Signal Type Codes

Code	Definition
A	Analog
DIFF I/O	Bidirectional Differential Input/Output
DIFF IN	Differential Input
DIFF OUT	Differential Output
I/O	Bidirectional Input/Output
I	Input
O	Output
OD	Open Drain Output
I/OD	Bidirectional Input / Open Drain Output
P	Power

6.2 Routing Guideline Format

The routing guidelines have the following format to specify how a signal should be routed.

- Breakout traces are traces routed from a BGA or other pin array, either to a point beyond the array, or to another layer where full normal spacing guidelines can be met. Breakout trace delay limited to 500 mils unless otherwise specified.
- After breakout, signal should be routed according to specified impedance for differential, single-ended, or both (for example: HDMI). Trace spacing to other signals also specified.
- Follow max and min trace delays where specified. Trace delays are typically shown in mm or in terms of signal delay in pico-seconds (ps) or both.
  - For differential signals, trace spacing to other signals must be larger of specified × dielectric height or inter-pair spacing
  - Spacing to other signals/pairs cannot be smaller than spacing between complementary signals (intra-pair).
  - Total trace delay depends on signal velocity which is different between outer (microstrip) and inner (stripline) layers of a PCB.

6.3 Signal Routing Conventions

Throughout this design guide, the following signal routing conventions are used:

SE Impedance (/ Diff Impedance) at x Dielectric Height Spacing

- Single-ended (SE) impedance of trace (along with differential impedance for diff pairs) is achieved by spacing requirement. Spacing is multiple of dielectric height. Dielectric height is typically different for microstrip and stripline. Note: 1 mil = 1/1000th of an inch.

Note: Trace spacing requirement applies to SE traces or differential pairs to other SE traces or differential pairs. It does not apply to traces making up a differential pair. For this case, spacing/trace widths are chosen to meet differential impedance requirement.

6.4 Routing Guidelines

Pay close attention when routing high speed interfaces, such as HDMI/DP, USB 3.1, PCIe or DSI/CSI. Each of these interfaces has strict routing rules for the trace impedance, width, spacing, total delay, and delay/flight time matching. The following guidelines provide an overview of the routing guidelines and notations used in this design guide.

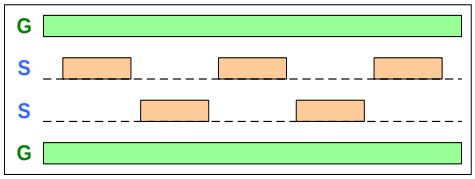
- Controlled Impedance
  Each interface has different trace impedance requirements and spacing to other traces. It is up to designer to calculate trace width and spacing required to achieve specified single-ended (SE) and differential (Diff) impedances. Unless otherwise noted, trace impedance values are ±15%.

- Max Trace Lengths/Delays
  Trace lengths/delays should include main PCB routing and any additional routing on a Flex/ secondary PCB segment connected to main PCB. The max length/delay should be from Jetson AGX Xavier to the actual connector (i.e. USB, HDMI, SD Card, etc.) or device (i.e. onboard USB device, Display driver IC, camera imager IC, etc.)
- Trace Delay/Flight Time Matching
  Signal flight time is the time it takes for a signal to propagate from one end (driver) to the other end (receiver). One way to get same flight time for signal within signal group is to match trace lengths within specified delay in the signal group.
  - Total trace delay = Carrier PCB trace delay only. Do not exceed maximum trace delay specified.
  - For six layers or more, it is recommended to match trace delays based on flight time of signals. For example, outer-layer signal velocity could be 150 psi (ps/inch) and inner-layer 175 psi. If one signal is routed 10 inches on outer layer and second signal is routed 10 inches in inner layer, difference in flight time between two signals will be 300 ps! That is a big difference if required matching is 15 ps (trace delay matching). To fix this, inner trace needs to be 1.7 inches shorter or outer trace needs to be 2 inches longer.
  - In this design guide, terms such as intra-pair and inter-pair are used when describing differential pair delay. Intra-pair refers to matching traces within differential pair (for example, true to complement trace matching). Inter-pair matching refers to matching differential pairs average delays to other differential pairs average delays.

6.5 General PCB Routing Guidelines

For GSSG stack-up to minimize crosstalk, signal should be routed in such a way that they are not on top of each other in two routing layers (Figure 6-1).

Figure 6-1. Signal Routing Example



Do not route other signals or power traces and areas directly under or over critical high-speed interface signals.

Note: The requirements detailed in the interface signal routing requirements tables must be met for all interfaces implemented or proper operation cannot be guaranteed.

Chapter 7. USB, PCIe, and UFS

Jetson AGX Xavier facilitates multiple high-speed interfaces to be brought out on the module in different configurations. The tables show the configurations that have been used on the developer kit.

Table 7-1. USB 2.0 Pin Descriptions

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
F13	USB0_N	USB0_DN	USB 2.0 Port 0 Data	UART-USB Bridge or USB Type C Connector (J512)	Bidir	USB2 Diff pair	–	0
F12	USB0_P	USB0_DP						
C10	USB1_N	USB1_DN	USB 2.0, Port 1 Data	USB Type C Connector (J513)	Bidir	USB2 Diff pair	–	0
C11	USB1_P	USB1_DP						
A11	USB2_N	USB2_DN	USB 2.0, Port 2 Data	M.2 Key E Connector	Bidir	USB2 Diff pair	–	0
A10	USB2_P	USB2_DP						
G10	USB3_N	USB3_DN	USB 2.0, Port 3 Data	USB / eSATA Connector (USB 2.0)	Bidir	USB2 Diff pair	–	0
G11	USB3_P	USB3_DP						

Notes:

1. In the Type/Dir column, Output is from Jetson AGX Xavier. Input is to Jetson AGX Xavier. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Table 7-2. UPHY Data Lane Pin Descriptions USB 3.1, PCIe, and UFS

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
A23	UPHY_RX0_N	PEX_RX0_N	UPHY Receive 0. PCIe x1 controller #1.	eSATA Bridge	Input	UPHY Diff Pair, AC-Coupled on carrier board if direct connect to device.	–	z
A22	UPHY_RX0_P	PEX_RX0_P						
C22	UPHY_RX1_N	PEX_RX1_N	UPHY Receive 1. USB 3.1 port 2.	USB Type C Alt Mode Switch #1			–	z
C23	UPHY_RX1_P	PEX_RX1_P						
B20	UPHY_RX2_N	PEX_RX2_N	UPHY Receive 2. PCIe x4 controller #0, lane 0.	M.2 Key M Connector			–	z
B21	UPHY_RX2_P	PEX_RX2_P						

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
D21	UPHY_RX3_N	PEX_RX3_N	UPHY Receive 3. PCIe x4 controller #0, lane 1.				–	z
D20	UPHY_RX3_P	PEX_RX3_P						
A19	UPHY_RX4_N	PEX_RX4_N	UPHY Receive 4. PCIe x4 controller #0, lane 2.				–	z
A18	UPHY_RX4_P	PEX_RX4_P						
C18	UPHY_RX5_N	PEX_RX5_N	UPHY Receive 5. PCIe x4 controller #0, lane 3.				–	z
C19	UPHY_RX5_P	PEX_RX5_P						
B17	UPHY_RX6_N	PEX_RX6_N	UPHY Receive 6. USB 3.1 port 0.	USB Type C Alt Mode Switch #2			–	z
B16	UPHY_RX6_P	PEX_RX6_P						
D17	UPHY_RX7_N	PEX_RX7_N	UPHY Receive 7. PCIe x1 controller #3.	M.2 Key E Connector			–	z
D16	UPHY_RX7_P	PEX_RX7_P						
A14	UPHY_RX8_N	PEX_RX8_N	UPHY Receive 8. PCIe x2 controller #4, lane 0.	Unused			–	z
A15	UPHY_RX8_P	PEX_RX8_P						
C14	UPHY_RX9_N	PEX_RX9_N	UPHY Receive 9. PCIe x2 controller #4, lane 1.				–	z
C15	UPHY_RX9_P	PEX_RX9_P						
B13	UPHY_RX10_N	PEX_RX10_N	UPHY Receive 10. UFS lane.	Micro SD / UFS Card Socket		UPHY Diff Pair	–	z
B12	UPHY_RX10_P	PEX_RX10_P						
D13	UPHY_RX11_N	PEX_RX11_N	UPHY Receive 11. USB 3.1 port 3.	USB / eSATA Connector (USB 3.0)		UPHY Diff Pair, AC-Coupled on carrier board if direct connect to device.	–	z
D12	UPHY_RX11_P	PEX_RX11_P						
J23	UPHY_TX0_N	PEX_TX0_N	UPHY Transmit 0. PCIe x1 controller #1.	eSATA Bridge	Output	UPHY Diff Pair, AC-Coupled on carrier board	–	z
J22	UPHY_TX0_P	PEX_TX0_P						
G22	UPHY_TX1_N	PEX_TX1_N	UPHY Transmit 1. USB 3.1 port 2.	USB Type C Alt Mode Switch #1			–	z
G23	UPHY_TX1_P	PEX_TX1_P						
K20	UPHY_TX2_N	PEX_TX2_N	UPHY Transmit 2. PCIe x4 controller #0, lane 0.	M.2 Key M Connector			–	z
K21	UPHY_TX2_P	PEX_TX2_P						
H21	UPHY_TX3_N	PEX_TX3_N	UPHY Transmit 3. PCIe x4 controller #0, lane 1.				–	z
H20	UPHY_TX3_P	PEX_TX3_P						
J19	UPHY_TX4_N	PEX_TX4_N	UPHY Transmit 4. PCIe x4 controller #0, lane 2.				–	z
J18	UPHY_TX4_P	PEX_TX4_P						
G18	UPHY_TX5_N	PEX_TX5_N	UPHY Transmit 5. PCIe x4 controller #0, lane 3.				–	z
G19	UPHY_TX5_P	PEX_TX5_P						
K16	UPHY_TX6_N	PEX_TX6_N	UPHY Transmit 6. USB 3.1 port 0.	USB Type C Alt Mode Switch #2			–	z
K17	UPHY_TX6_P	PEX_TX6_P						
H17	UPHY_TX7_N	PEX_TX7_N	UPHY Transmit 7. PCIe x1 controller #3.	M.2 Key E Connector			–	z
H16	UPHY_TX7_P	PEX_TX7_P						
J15	UPHY_TX8_N	PEX_TX8_N	UPHY Transmit 8. PCIe x2 controller #4, lane 0.	Unused			–	z
J14	UPHY_TX8_P	PEX_TX8_P						
G14	UPHY_TX9_N	PEX_TX9_N	UPHY Transmit 9. PCIe x2 controller #4, lane 1.				–	z
G15	UPHY_TX9_P	PEX_TX9_P						
K12	UPHY_TX10_N	PEX_TX10_N	UPHY Transmit 10. UFS lane.	Micro SD / UFS Card Socket		UPHY Diff Pair	–	z
K13	UPHY_TX10_P	PEX_TX10_P						
H13	UPHY_TX11_N	PEX_TX11_N	UPHY Transmit 11. USB 3.1 port 3.	USB / eSATA Connector (USB 3.0)		UPHY Diff Pair, AC-Coupled on carrier board	–	z
H12	UPHY_TX11_P	PEX_TX11_P						

Notes:

1. In the Type/Dir column, Output is from Jetson AGX Xavier. Input is to Jetson AGX Xavier. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Table 7-3. NVHS for PCIe x8 Data Lan Pin Descriptions

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
D25	NVHS0_SLVS_RX0_N	NVHS0_RX0_N	PCIe/SLVS 0 Receive Lane 0. PCIe x8 controller #5 or SLVS, lane 0.	PCIe x16 Connector	Input	UPHY/SLVS Diff Pair, AC-Coupled on carrier board for PCIe if direct connect to device	–	z
D24	NVHS0_SLVS_RX0_P	NVHS0_RX0_P						
B24	NVHS0_SLVS_RX1_N	NVHS0_RX1_N	PCIe/SLVS 0 Receive Lane 1. PCIe x8 controller #5 or SLVS, lane 1.				–	z
B25	NVHS0_SLVS_RX1_P	NVHS0_RX1_P						
C26	NVHS0_SLVS_RX2_N	NVHS0_RX2_N	PCIe/SLVS 0 Receive Lane 2. PCIe x8 controller #5 or SLVS, lane 2.				–	z
C27	NVHS0_SLVS_RX2_P	NVHS0_RX2_P						
A27	NVHS0_SLVS_RX3_N	NVHS0_RX3_N	PCIe/SLVS 0 Receive Lane 3. PCIe x8 controller #5 or SLVS, lane 3.				–	z
A26	NVHS0_SLVS_RX3_P	NVHS0_RX3_P						
D29	NVHS0_SLVS_RX4_N	NVHS0_RX4_N	PCIe/SLVS 0 Receive Lane 4. PCIe x8 controller #5 or SLVS, lane 4.				–	z
D28	NVHS0_SLVS_RX4_P	NVHS0_RX4_P						
B28	NVHS0_SLVS_RX5_N	NVHS0_RX5_N	PCIe/SLVS 0 Receive Lane 5. PCIe x8 controller #5 or SLVS, lane 5.				–	z
B29	NVHS0_SLVS_RX5_P	NVHS0_RX5_P						
C30	NVHS0_SLVS_RX6_N	NVHS0_RX6_N	PCIe/SLVS 0 Receive Lane 6. PCIe x8 controller #5 or SLVS, lane 6.				–	z
C31	NVHS0_SLVS_RX6_P	NVHS0_RX6_P						
A31	NVHS0_SLVS_RX7_N	NVHS0_RX7_N	PCIe/SLVS 0 Receive Lane 7. PCIe x8 controller #5 or SLVS, lane 7.				–	z
A30	NVHS0_SLVS_RX7_P	NVHS0_RX7_P						
H25	NVHS0_TX0_N	NVHS0_TX0_N	PCIe Transmit Lane 0. PCIe x8 controller #5, lane 0.		Output	UPHY Diff Pair, AC-Coupled on carrier board	–	z
H24	NVHS0_TX0_P	NVHS0_TX0_P						
K24	NVHS0_TX1_N	NVHS0_TX1_N	PCIe Transmit Lane 1. PCIe x8 controller #5, lane 1.				–	z
K25	NVHS0_TX1_P	NVHS0_TX1_P						
G26	NVHS0_TX2_N	NVHS0_TX2_N	PCIe Transmit Lane 2. PCIe x8 controller #5, lane 2.				–	z
G27	NVHS0_TX2_P	NVHS0_TX2_P						
J27	NVHS0_TX3_N	NVHS0_TX3_N	PCIe Transmit Lane 3. PCIe x8 controller #5, lane 3.				–	z
J26	NVHS0_TX3_P	NVHS0_TX3_P						
H29	NVHS0_TX4_N	NVHS0_TX4_N	PCIe Transmit Lane 4. PCIe x8 controller #5, lane 4.				–	z
H28	NVHS0_TX4_P	NVHS0_TX4_P						
K28	NVHS0_TX5_N	NVHS0_TX5_N	PCIe Transmit Lane 5. PCIe x8 controller #5, lane 5.				–	z
K29	NVHS0_TX5_P	NVHS0_TX5_P						
G30	NVHS0_TX6_N	NVHS0_TX6_N	PCIe Transmit Lane 6. PCIe x8 controller #5, lane 6.				–	z
G31	NVHS0_TX6_P	NVHS0_TX6_P						
J31	NVHS0_TX7_N	NVHS0_TX7_N	PCIe Transmit Lane 7. PCIe x8 controller #5, lane 7.				–	z
J30	NVHS0_TX7_P	NVHS0_TX7_P						

Notes:

1. In the Type/Dir column, Output is from Jetson AGX Xavier. Input is to Jetson AGX Xavier. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Table 7-4. PCIe Clock and Control Pin Descriptions

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
E14	PEX_CLK0_N	PEX_CLK0N	PCIe 0 Reference Clock for controller #0.	M.2 Key M Connector	Output	PCIe Diff Pair	–	0
E15	PEX_CLK0_P	PEX_CLK0P						
E11	PEX_L0_ CLKREQ_N	PEX_L0_ CLKREQ_N	PCIe 0 Clock Request for controller #0. Pulled to 3.3V through 47.5kΩ resistor on-module.		Input	Open-Drain – 1.8V (3.3V tolerant)	DD	z
D10	PEX_L0_RST_N	PEX_L0_RST_N	PCIe 0 Reset for controller #0. Pulled to 3.3V through 4.75kΩ resistor on-module.		Output		DD	0
F17	PEX_CLK1_N	PEX_CLK1N	PCIe 1 Reference Clock for controller #1.	eSATA Bridge	Output	PCIe Diff Pair	–	0
F16	PEX_CLK1_P	PEX_CLK1P						
D9	PEX_L1_ CLKREQ_N	PEX_L1_ CLKREQ_N	PCIe 1 Clock Request for controller #1. Pulled to 3.3V through 47.5kΩ resistor on-module.	Unused	Input	Open-Drain – 1.8V (3.3V tolerant)	DD	z
B9	PEX_L1_RST_N	PEX_L1_RST_N	PCIe 1 Reset for controller #1. Pulled to 3.3V through 4.75kΩ resistor on-module.	eSATA Bridge	Output		DD	0
F21	PEX_CLK3_N	PEX_CLK3N	PCIe 3 Reference Clock for controller #3.	M.2 Key E Connector	Output	Diff pair	–	0
F20	PEX_CLK3_P	PEX_CLK3P						
J10	PEX_L3_ CLKREQ_N	PEX_L3_ CLKREQ_N	PCIe 3 Clock Request for controller #3. Pulled to 3.3V through 47.5kΩ resistor on-module.		Input	Open-Drain – 1.8V (3.3V tolerant)	DD	z
K9	PEX_L3_RST_N	PEX_L3_RST_N	PCIe 3 Reset for controller #3. Pulled to 3.3V through 4.75kΩ resistor on-module.		Output		DD	0
E22	PEX_CLK4_N	PEX_CLK4N	PCIe 4 Reference Clock for controller #4,	Unused	Output	Diff pair	–	0
E23	PEX_CLK4_P	PEX_CLK4P						
G8	PEX_L4_ CLKREQ_N	PEX_L4_ CLKREQ_N	PCIe 4 Clock Request for controller #4. Pulled to 3.3V through 47.5kΩ resistor on-module.		Input	Open-Drain – 1.8V (3.3V tolerant)	DD	z
J9	PEX_L4_RST_N	PEX_L4_RST_N	PCIe 4 Reset for controller #4. Pulled to 3.3V through 4.75kΩ resistor on-module.		Output		DD	0
F25	PEX_CLK5_N	PEX_CLK5N	PCIe 5 Reference Clock for controller #5 when Jetson AGX Xavier is Root Port. Unused when Jetson AGX Xavier used as Endpoint.	PCIe x16 Connector	Output	Diff pair	–	0
F24	PEX_CLK5_P	PEX_CLK5P						
C8	PEX_L5_ CLKREQ_N	PEX_L5_ CLKREQ_N	PCIe 5 Clock Request for controller #5. Input when Jetson AGX Xavier is Root Port. Output when Jetson AGX Xavier is Endpoint. Pulled to 3.3V through 47.5kΩ resistor on-module.		Input	Open-Drain – 1.8V (3.3V tolerant)	DD	z
H10	PEX_L5_RST_N	PEX_L5_RST_N	PCIe 5 Reset. Output when Jetson AGX Xavier is Root Port. Input when Jetson AGX Xavier is Endpoint. Pulled to 3.3V through 4.75kΩ resistor on-module.		Bidir		DD	0
E31	NVHS0_SLVS_REFCLK0_N	NVHS0_REFCLK_N	PCIe/SLVS Reference Clock 0. Unused if controller #5 (NVHS[7:0] lanes) configured as Root Port. Receives 100Mhz clock if configured as Endpoint.		Input	UPHY/SLVS Diff Pair	–	z
E30	NVHS0_SLVS_REFCLK0_P	NVHS0_REFCLK_P						
E26	UPHY_ REFCLK1_N	PEX_REFCLK1_N	UPHY Reference Clock 1. Unused.	Unused	Input	UPHY Diff Pair	–	z
E27	UPHY_ REFCLK1_P	PEX_REFCLK1_P						
F29	UPHY_ REFCLK2_N	PEX_REFCLK2_N	UPHY Reference Clock 2. Unused.				–	z
F28	UPHY_ REFCLK2_P	PEX_REFCLK2_P						

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
A8	PEX_WAKE_N	PEX_WAKE_N	PCIe Wake. Wake signal shared by all PCIe interfaces. Pulled to 3.3V through 47.5kΩ resistor on-module.	PCIe x16 Connector and M.2 Key E and Connector	Input	Open-Drain – 1.8V (3.3V tolerant)	DD	z

Notes:

1. In the Type/Dir column, Output is from Jetson AGX Xavier. Input is to Jetson AGX Xavier. Bidir is for Bidirectional signals.
2. The direction shown in this table for PEX_Lx_RST_N, PEX_Lx_CLKREQ_N and PCIE_WAKE_N signals is true when used for those PCIe functions. Otherwise if used as GPIOs, the direction is bidirectional.
3. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
4. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Table 7-5. UFS and Miscellaneous USB Control Pin Descriptions

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
A6	UFS0_REF_CLK	UFS0_REF_CLK	UFS Reference Clock	Micro SD / UFS Card Socket	Output	CMOS – 1.2V	LV_CZ	0
C6	UFS0_RST_N	UFS0_RST	UFS Reset	Micro SD / UFS Card Socket	Output	CMOS – 1.2V	LV_CZ	0
A62	GPIO10	CAN1_WAKE	GPIO	USB PD Controller Interrupt	Bidir	CMOS – 3.3V	CZ	z
F54	GPIO22	USB_VBUS_EN0	GPIO	VDD_5V_SATA Load Switch Enable	Output	CMOS – 1.8V	DD	0

Table 7-6. USB 3.1, PCIe and UFS Lane Mapping Configurations

Jetson AGX Xavier Lanes			UPHY0	UPHY1	UPHY[5:2]	UPHY6	UPHY7	UPHY[9:8]	UPHY10	UPHY11	NVHS[7:0]
Avail. Outputs from Jetson AGX Xavier											
USB 3.1	PCIe	UFS									
3	2 x1, 1 x2, 1 x4 & 1 x8	1 x1	PCIe x1 (C1)	USB 3.1 (P2)	PCIe x4 (C0)	USB 3.1 (P0)	PCIe x1 (C3)	PCIe x2 (C4)	UFS x1 (0)	USB 3.1 (P3)	PCIe x8 (C5)

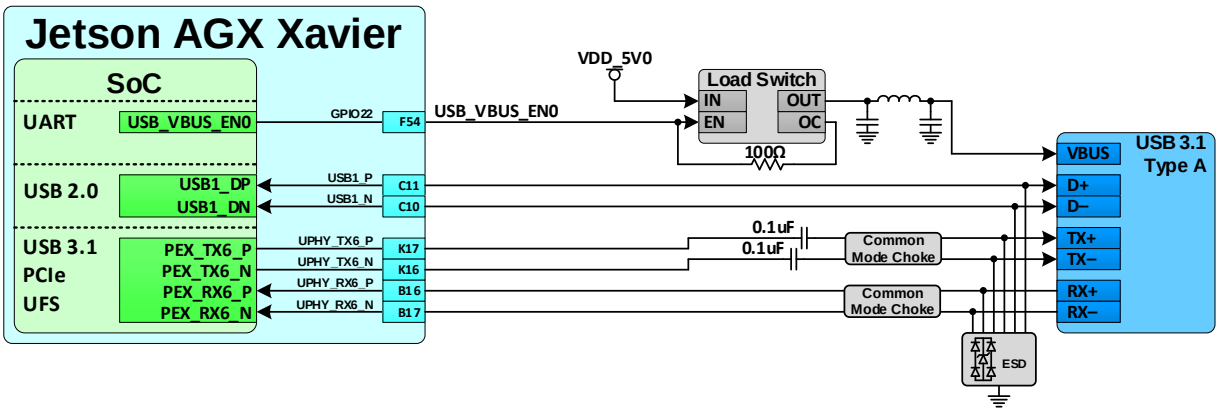
7.1 USB

Jetson AGX Xavier supports up to four USB 2.0 ports and up to three USB 3.1 ports. There are examples in this section to either implement a simple USB 3.1/2.0 connection to a USB 3.1 Type A connector or to replicate the USB Type C connections used on the NVIDIA Developer Kit. Designs that intend to follow the NVIDIA Developer Kit carrier board design and include the Type C PD Controller (CYPD4226) need to replicate the circuitry on the latest P2822 carrier board exactly. NVIDIA will provide the binary and the customer should get the flashing instructions from Cypress. If the design requires a simpler solution (Type A or similar), then refer to the software adaptation guide for information.

Notes:

- Some non-compliant USB 3.0 devices may fail unless USB 3.1 Gen2 is disabled.
- See Section 15.1 "USB Recover Mode" for requirements for USB recovery mode.

Figure 7-1. Simple USB Type A Connection Example



Type C connections are based on the NVIDIA carrier board design. Additional interface assignments shown in Figure 7-2 are also based on the carrier board usage.

Designs that intend to follow the NVIDIA carrier board design and include the Type C PD Controller (CYPD4226 - U513 on NVIDIA carrier board) need to replicate the circuitry on the latest P2822 carrier board exactly. NVIDIA will provide the binary and the customer should get the flashing instructions from Cypress.

If the CYPD4226 PD controller is implemented in a design, it is recommended that test points be included that connect to the SW_CLK, SW_IO and XRES pins as well as VDD_AO. These would be required to flash the binary during manufacturing.

Figure 7-2. Jetson AGX Xavier Carrier Board Design USB Type C Connection Example

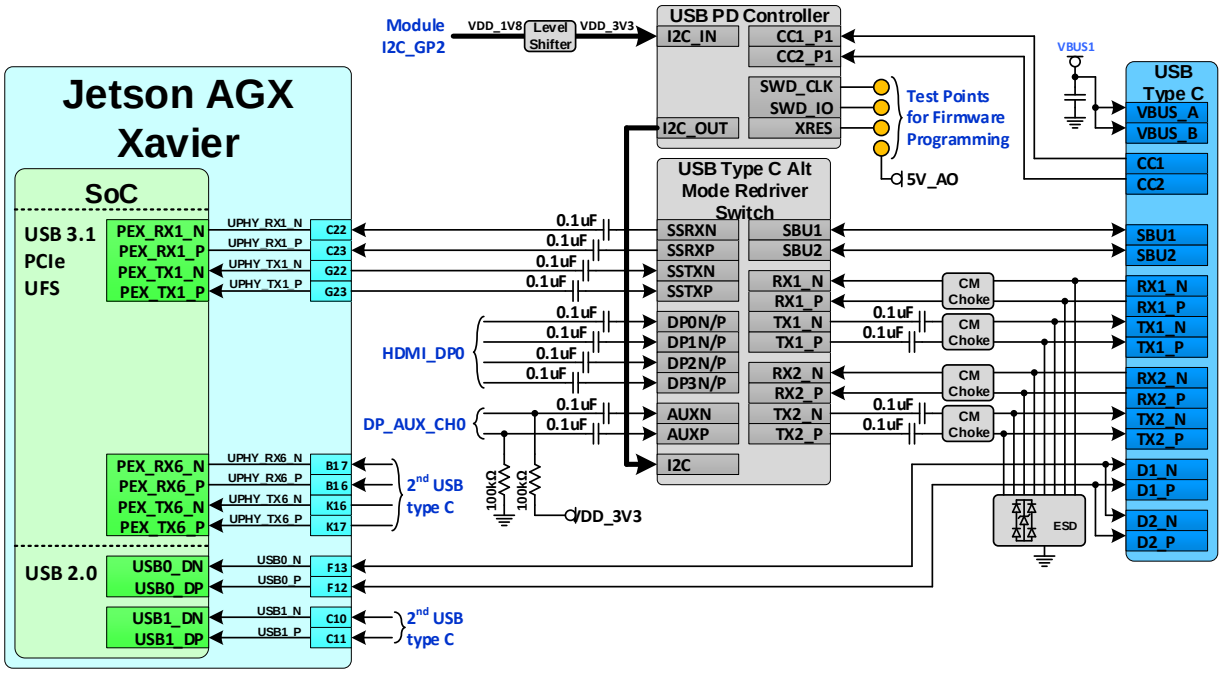
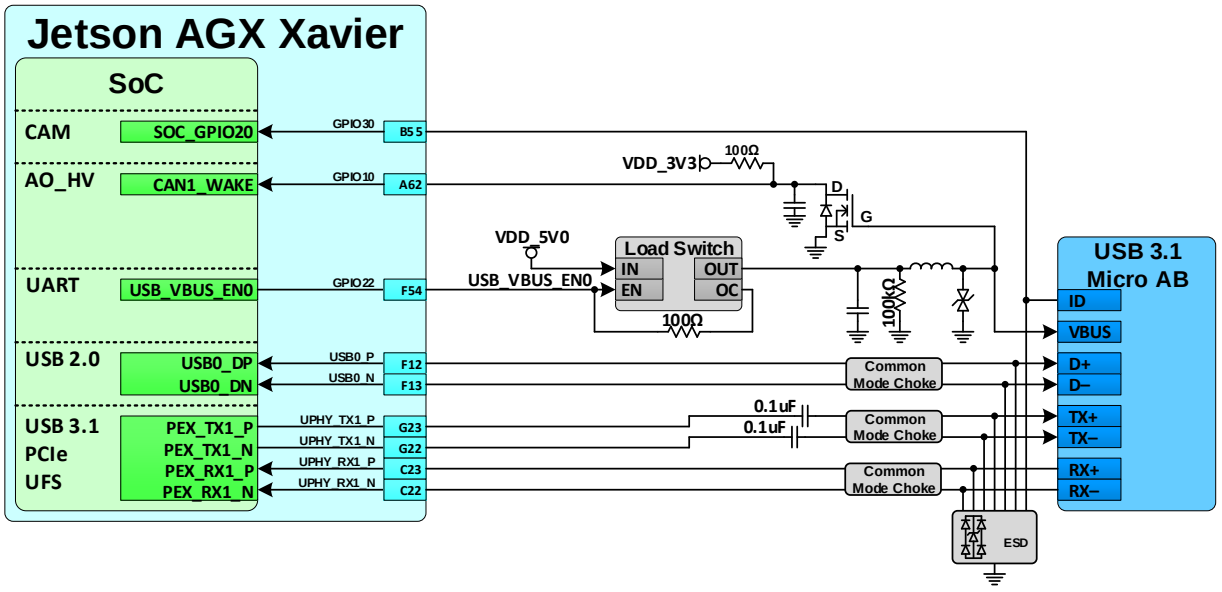


Figure 7-3. USB 3.1 USB Micro AB Connection Example



Notes:

- See the USB.org statement regarding the phasing out of support for the USB 3.x Micro-B and Micro-AB connector certifications after February 28th, 2021.
- GPIO30 shown in Figure 7-3 connected to the connector ID pin is used for the M.2 Key E Alert function on the NVIDIA carrier board. If both functions are required, another GPIO will be required for one of the functions.

7.1.1 USB 2.0 Design Guidelines

These requirements apply to the USB 2.0 controller PHY interfaces: USB[3:0]

Table 7-7. USB 2.0 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency (High Speed): Bit Rate/UI period/Freq.	480/2.083/240	Mbps/ns/MHz	
Max Loading: High Speed / Full Speed / Low Speed	10 / 150 / 600	pF	
Reference plane	GND		
Trace Impedance: Diff pair / Single Ended	90 / 50	Ω	±15%
Max Trace Delay With CMC or SW (Microstrip / Stripline) Without CMC or SW (Microstrip / Stripline)	 900/1050 (6) 1350/1575 (9)	ps (in)	Prop delay assumption: 175ps/in. for stripline, 150ps/in. for microstrip). See Note 3
Max Intra-Pair Skew between USBx_P and USBx_N	7.5	ps	

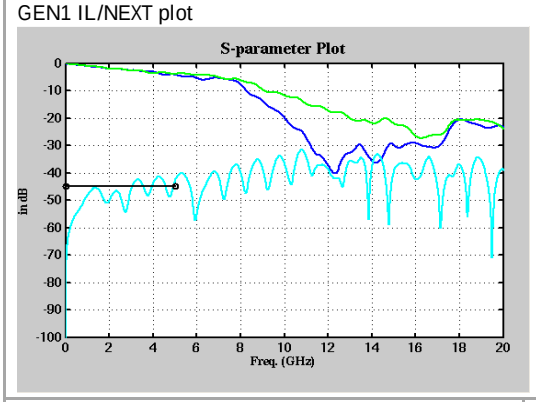
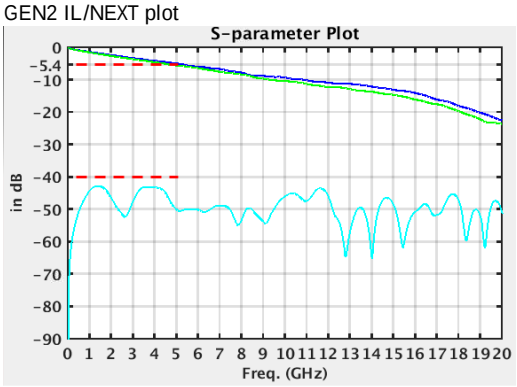
Notes:

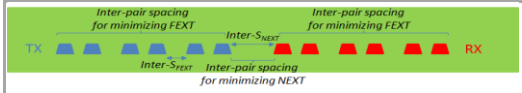
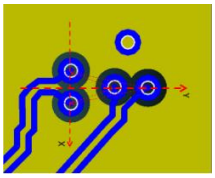
1. If portion of route is over a flex cable this length should be included in the Max Trace Delay/Length calculation and 85Ω Differential pair trace impedance is recommended.
2. Up to 4 signal Vias can share a single GND return Via.
3. CMC = Common-Mode-Choke. SW = Analog Switch
4. Adjustments to the USB drive strength, slew rate, termination value settings should not be necessary, but if any are made, they MUST be done as an offset to default values instead of overwriting those values.

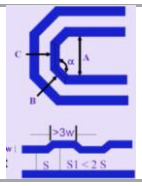
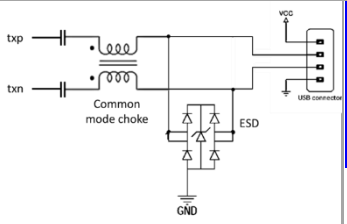
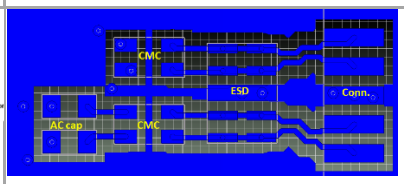
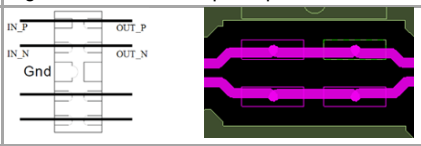
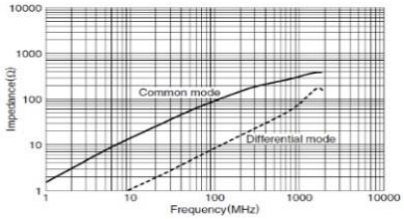
7.1.2 USB 3.1 Design Guidelines

The following requirements apply to the USB 3.1 PHY interfaces.

Table 7-8. USB 3.1 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Data Rate / UI period GEN1 GEN2	 5.0 / 200 10.0 / 100	 Gbps / ps	Device mode supports GEN1 speed only.
Max Number of Loads	1	load	
Termination	90 differential	Ω	On-die termination at TX and RX
Insertion Loss (IL) Host GEN1 (Type C) GEN1 (Type A) GEN2 (Single role host mode) Device GEN1 (Type C) GEN1 (Micro AB) GEN2 Host/GEN1 Device (dual role mode) Resonance Dip Frequency	 ⩾ -2 ⩾ -7 TBD ⩾ -2 ⩾ -1 ⩾ -5.4 > 8	 dB dB dB dB dB dB GHz	 @ 2.5GHz @ 2.5GHz @ 5GHz @ 2.5GHz @ 2.5GHz @ 5GHz (Host) / 2.5GHz (Device) The resonance dip could be caused by a via stub for layer transition or trace stub for co-layout.
Time-domain Reflectometer (TDR) Dip GEN1 GEN2	 75 75	 Ω	 @ Tr = 200ps (10%-90%) @ Tr = 61ps (10%-90%)
Near End Crosstalk (NEXT)	⩽ -45	dB	DC – 5GHz per each TX-RX NEXT
GEN1 IL/NEXT plot 		GEN2 IL/NEXT plot 	
Impedance			
Trace Impedance: Diff pair / Single Ended	85 / 43	Ω	±15%. Intrinsic Zdf, does not account for coupling from other trace pairs
Reference plane	GND		

Parameter	Requirement	Units	Notes
Trace Length/Skew			
Trace loss characteristic: GEN1 GEN2	 < 0.7 < 0.9	 dB/in	 @ 2.5GHz @ 5GHz
• The following max length is derived based on the trace loss characteristic above. The length constraint must be re-defined if loss characteristic is changed. • The trace loss profile for Gen2 support is based on the dielectric material EM370(5). See the loss plots in the sheet "USB3 LOSS BUDGET" • Note that microstrip loss could be similar to stripline due to humidity effect			
Breakout Region – Max length	11	mm	Minimum trace width and spacing
Max Trace Length GEN1 Host GEN1 Device GEN2 Host or Device	 152 (1014) 50.8 (234) 127 (850)	 mm (ps)	Stripline (6.7ps/mm) assumed
Max Intra-Pair Skew (RX/TX_N to RX/TX_P)	0.15 (1)	mm (ps)	Do not perform length matching within breakout region. Trace length matching should be done before discontinuities. See Note 2
Differential pair uncoupled length	6.29 (41.9)	mm (ps)	
Trace Spacing for TX/RX Non-Interleaving			
TX-RX Xtalk is very critical in PCB trace routing. The ideal solution is to route TX and RX on different layers.			
If routing on the same layer, strongly recommend not interleaving TX and RX lanes			
If have to have interleaving routing in breakout, all the inter-pair spacing should follow the rule of inter-S_{NEXT} (between TX/RX pair spacing)			
The breakout trace width is suggested to be the minimum to increase inter-pair spacing			
Do not perform serpentine routing for intra-pair skew compensation in the breakout region			
			
Min Inter-SNEXT (between TX/RX) Breakout Main-route	 4.85x 3x	 Dielectric height	This is the recommended dimensions for meeting the NEXT requirement. Stripline structure in a GSSG structure is assumed (holds in broadside-coupled stripline structure)
Max length Breakout (L_{BRK}) Main-route	 11 Max trace length - L_{BRK}	 mm	
Trace Spacing for TX/RX Interleaving			
Max Pair-pair spacing, Spacing to plane and SMT pad, and Spacing to unrelated high-speed signals Microstrip . Stripline	 4x / 3x	 Dielectric height	
Via			
Via proximity (Signal via to GND return via)	< 3.8 (24)	mm (ps)	See note 1
Topology	Y-pattern is recommended Keep symmetry		Y-pattern helps with Xtalk suppression. It can also reduce the limit of the pair-pair distance. Review needed (NEXT/FEXT check) if via placement does not use Y-pattern. 
GND via	Place GND via as symmetrically as possible to data pair vias. Up to 4 signal vias (2 diff pairs) can share a single GND return via		GND via is used to maintain return path, while its Xtalk suppression is limited

Parameter	Requirement	Units	Notes
Max # of Vias PTH vias Micro Vias	 4 if all vias are PTH via Not limited		 As long as total channel loss meets IL spec
Max Via Stub Length	0.4	mm	long via stub requires review (IL and resonance dip check)
Serpentine			
Min bend angle	135	deg (a)	
Dimension Min A Spacing Min B, C Length Min Jog Width	 4x 1.5x 3x	Trace width	S1 must be taken care in order to consider Xtalk to adjacent pair 
Add-on Components			
Placement order	SoC – AC capacitor – Common mode choke – ESD – Device/Connector		
			
AC Cap			
Value: Min/Max	0.075 / 0.2	uF	Only required for TX pair when routed to connector
Location (max length to adjacent discontinuity)	8	mm	Discontinuity is connector, via, or component pad
Voiding	GND/PWR void under/above cap is preferred		Voiding is required if AC cap size is 0603 or larger
ESD			
Max Junction capacitance (IO to GND)	0.8	pF	e.g. SEMTECH RClamp0524p
Footprint	Pad should be on the net – not trace stub		
Location (max length to adjacent discontinuity)	8	mm	Discontinuity is connector, via, or component pad
Common-Mode Choke			
Common-mode impedance @ 100MHz Min/Max	65/90	Ω	TDK ACM2012D-900-2P
Max Rdc	0.3	Ω	
Differential TDR impedance	90	Ω @TR-200ps (10%-90%)	
Min Sdd21 @ 2.5GHz	2.22	dB	
Max Scc21 @ 2.5GHz	19.2	dB	
Location	8	mm	

Parameter	Requirement	Units	Notes
FPC (Additional length of Flexible Printed Circuit Board)			
The FPC routing should be included for PCB trace calculations (max length, etc.)			
Characteristic Impedance	Same as PCB		
Loss characteristic	Strongly recommend to be same as PCB or better		If worse than PCB, the PCB and FPC length must be re-estimated
Connector			
SMT Connector GND Voiding			GND plane under signal pad should be voided. Size of void should be the same size as the pad.
Connector type			Connector used must be USB-IF certified

Notes:

1. Up to 4 signal Vias can share a single **GND** return Via
2. Recommend trace length matching to <1ps before Vias or any discontinuity to minimize common mode conversion.
3. Place **GND** Vias as symmetrically as possible to data pair Vias.

7.1.3 Common USB Routing Guidelines

If routing to USB device or USB connector includes a flex or 2nd PCB, the total routing including all PCBs and flexes must be used for the max trace and skew calculations.

Keep critical USB related traces away from other signal traces or unrelated power traces and areas or power supply components.

Table 7-9. USB 2.0 Signal Connections

Module Pin Name	Type	Termination	Description
USB[3:0]_N/P	DIFF I/O	90Ω common-mode chokes close to connector. ESD Protection between choke and connector on each line to GND	USB Differential Data Pair: Connect to USB connector, Mini-Card Socket, Hub or another device on the PCB.

Table 7-10. USB 3.1 Signal Connections

Module Pin Name	Type	Termination	Description
UPHY_TX6_N/P (USB 3.1 Port #0) UPHY_TX1_N/P (USB 3.1 Port #2) UPHY_TX11_N/P (USB 3.1 Port #3)	DIFF Out	Series 0.1uF caps. Common-mode chokes and ESD protection if these are used.	USB 3.1 Differential Transmit Data Pairs: Connect to USB 3.1 connectors, hubs or other devices on the PCB.
UPHY_RX6_N/P (USB 3.1 Port #0) UPHY_RX1_N/P (USB 3.1 Port #2) UPHY_RX11_N/P (USB 3.1 Port #3)	DIFF In	If routed directly to a peripheral on the board, AC caps are needed for the peripheral TX lines. Common-mode chokes and ESD protection, if these are used.	USB 3.1 Differential Receive Data Pairs: Connect to USB 3.1 connectors, hubs or other devices on the PCB.

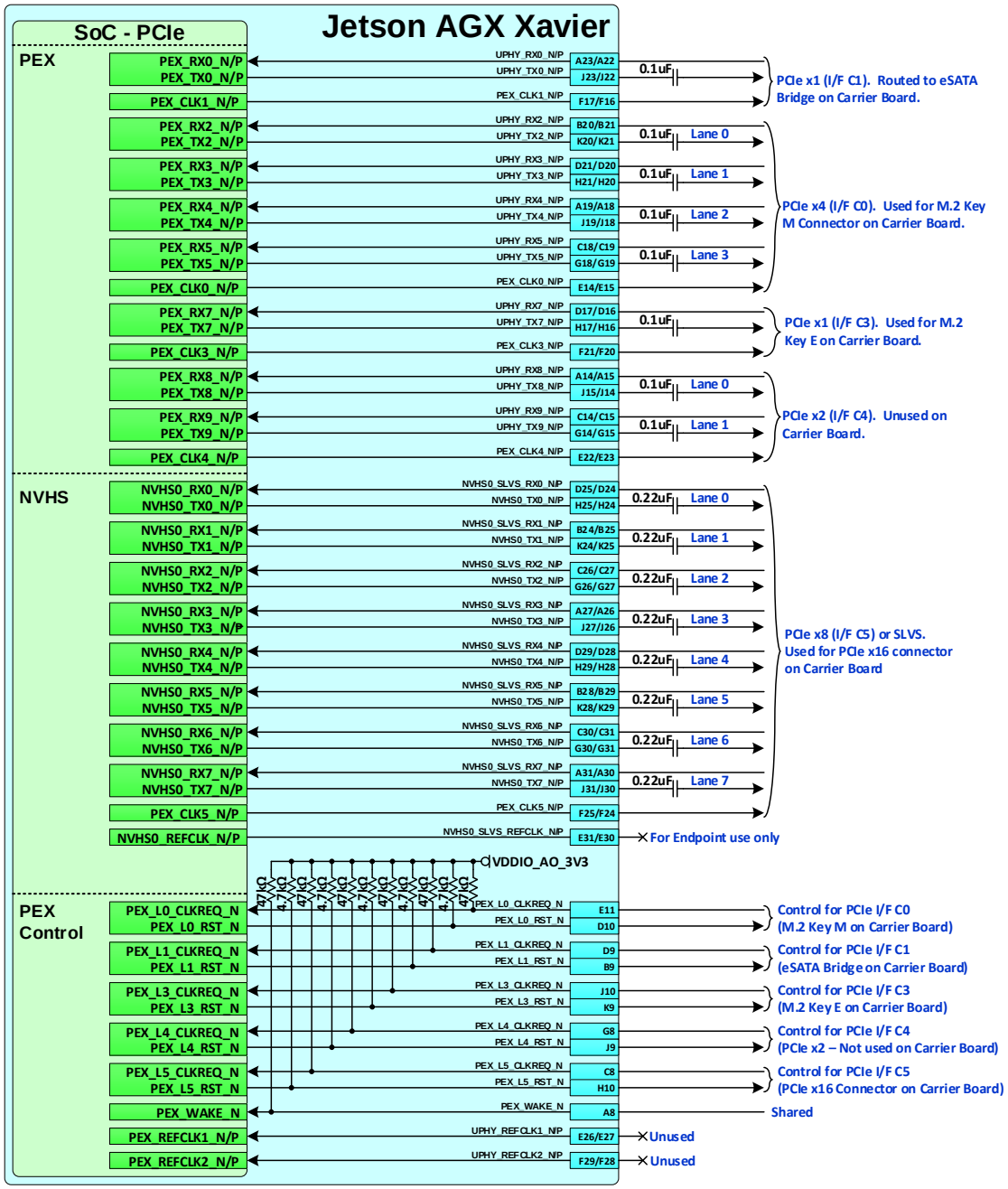
Table 7-11. Recommended USB Observation Test Points for Initial Boards

Test Points Recommended	Location
One for each of the USB 2.0 data lines (USBx_N/P)	Near Jetson AGX Xavier connector and USB device. USB connector pins can serve as test points.
One for each of the USB 3.1 output lines used (TXn_N/P)	Near USB device. USB connector pins can serve as test points
One for each of the USB 3.1 input lines (RXn_N/P)	Near Jetson AGX Xavier connector.

7.2 PCI Express

Jetson AGX Xavier provides 16 lanes that can be used for PCIe, USB 3.1, and UFS. See the Jetson AGX Xavier USB 3.1, PCIe and UFS Lane Mapping Configurations table for details on which are available for PCIe use. Root port is supported on all PCIe interfaces. Endpoint mode is supported on Interface C5 only. Figure 7-4 shows all the PCIe interfaces configured as Root Ports. Figure 7-5 shows C5 configured as an Endpoint.

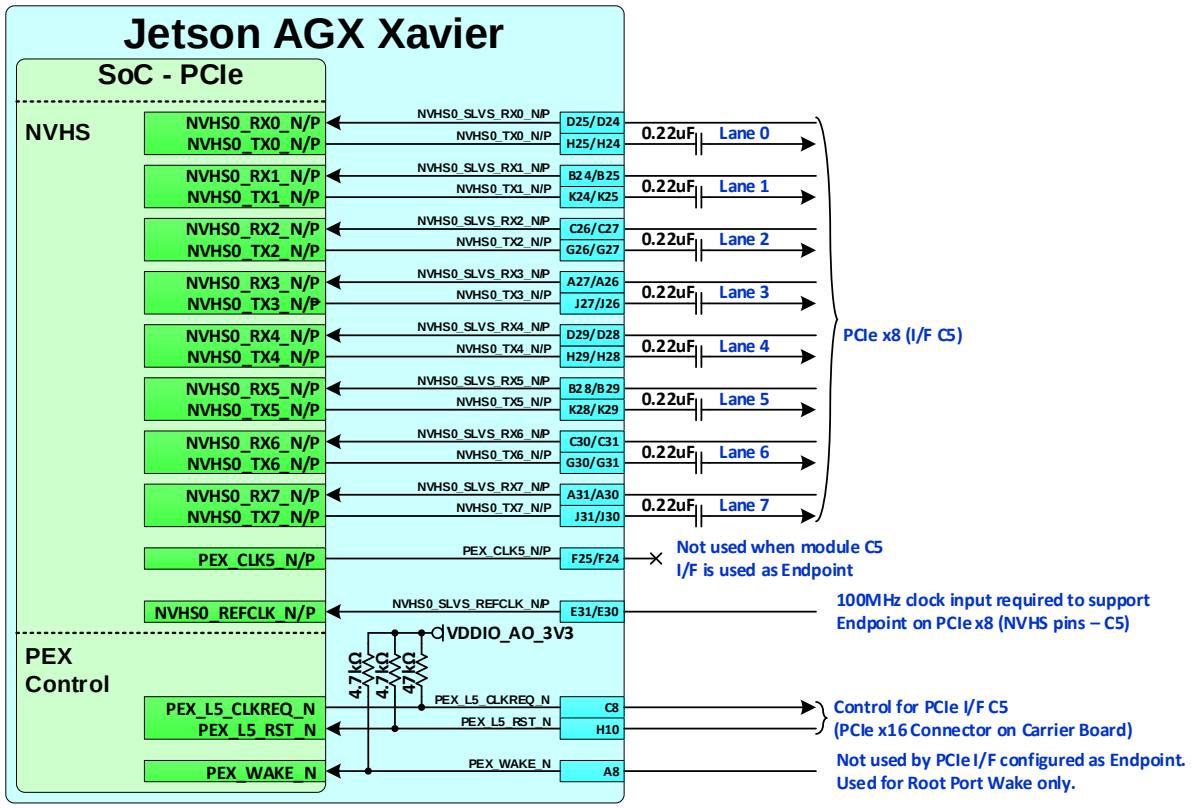
Figure 7-4. PCIe Root Port Connection Example



Notes:

- AC Capacitors required on RX lines on carrier board if connected directly to device. They are not placed on the carrier board if connected to a PCIe connector. In that cases, the AC caps are on the PCIe add-in board.
- See design guidelines for correct AC capacitor values.
- The PCIe REFCLK inputs and PCIEx_CLK clock outputs comply to the PCIe CEM specification "REFCLK DC Specifications and AC Timing Requirements." The clocks are HCSL compatible.

Figure 7-5. PCIe Endpoint Connection Example



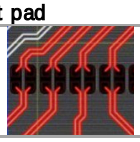
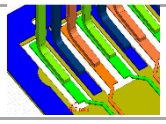
Note: See "Notes" under Figure 7-4.

7.2.1 PCIe Design Guidelines up to Gen3

The following table details the PCIe design guidelines up to Gen3. See Section 7.2.2 for design guidelines regarding PCIe Gen4.

Table 7-12. PCIe Interface Signal Routing Requirements up to Gen3

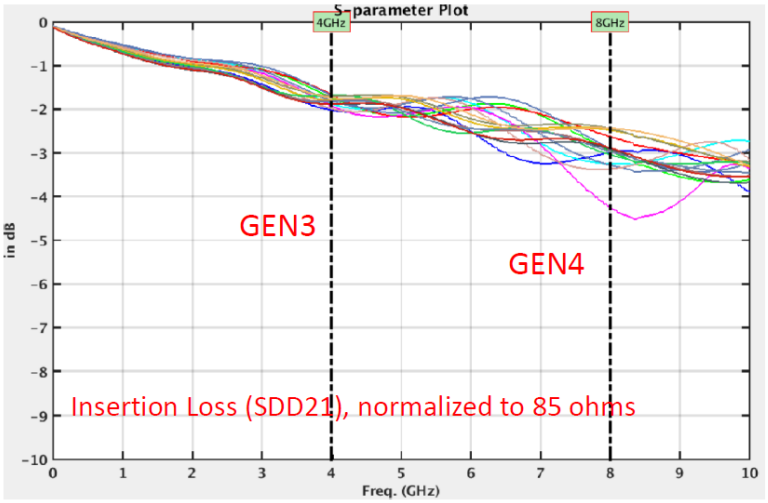
Parameter	Requirement	Units	Notes
Specification			
Data Rate / UI Period	5.0 / 200	Gbps / ps	2.5GHz, half-rate architecture
Configuration / Device Organization	1	Load	
Topology	Point-point		Unidirectional, differential
Termination	50	Ω	To **GND** Single Ended for P and N
Impedance			
Trace Impedance differential / Single Ended	85 / 50	Ω	±15%. See note 1
Reference plane	GND		
Spacing			
Trace Spacing (Stripline/Microstrip) Pair – Pair To plane and capacitor pad To unrelated high-speed signals	 3x / 4x 3x / 4x 3x / 4x	Dielectric	TX and RX should not be routed on the same layer. See Note 2.
Length/Skew			
Breakout region (Max Length)	41.9	ps	Minimum width and spacing. 4x or wider dielectric height spacing is preferred
Trace loss budget (for carrier board routing) Routing direct to device Routing to PCIe/M.2 connector	 -11.5 -7.5	dB/in	@ 4GHz (See TBD), Loss: GEN3 budget – module – end device – safety margin (-22dB + 3.5.dB + 4dB + 3dB) Loss: GEN3 budget – module – end device – safety margin (-28dB + 4.24dB + 8dB + 3dB)
Max trace length (delay) Direct to device on carrier board Stripline Microstrip Routed to PCIe or M.2 connector Stripline Microstrip	 15.3 (2680) 14.4 (2160) 10 (1750) 9.4 (1400)	in (ps)	Mid-loss PCB of 0.8dB/in (Microstrip) or 0.75dB/in (Stripline) is used. Also, 175ps/in for Stripline routing and 150ps/in for Microstrip.
Max PCB via distance from the BGA	41.9	ps	Max distance from BGA ball to first PCB via.
PCB within pair (intra-pair) skew	0.075 (0.5)	mm (ps)	Do trace length matching before hitting discontinuities
Within pair (intra-pair) matching between subsequent discontinuities	0.075 (0.5)	mm (ps)	
Differential pair uncoupled length	41.9	ps	
Via			
Via placement	Place GND vias as symmetrically as possible to data pair vias. GND via distance should be placed less than 1x the diff pair via pitch		
Max # of Vias PTH Vias Micro-Vias	 2 for TX traces and 2 for RX trace No requirement		
Max Via stub length	0.4	mm	Longer via stubs would require review
Routing signals over antipads	Not allowed		

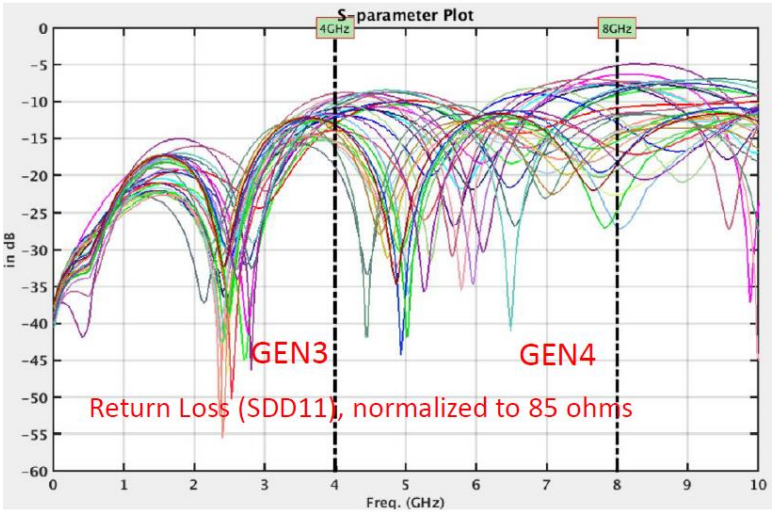
Parameter	Requirement	Units	Notes
AC Cap			
Value GEN1/GEN2: Min/Max GEN3: Min/Max	 0.075 / 0.265 0.176 / 0.265	**uF**	**0.1uF or 0.22uF recommended for GEN1 or GEN2. 0.22uF recommended for GEN3. Only required for TX pair when routed to connector**
Location (max length to adjacent discontinuity)	8	**mm**	**Discontinuity such as edge finger, component pad**
Voiding	Voiding the plane directly under the pad 3-4 mils larger than the pad size is recommended.		
Serpentine (See USB 3.1 Guidelines)			
Connector			
Voiding	**Voiding the plane directly under the pad 5.7 mils larger than the pad size is recommended.**		
Keep critical PCIe traces such as PEX_TX/RX, TERMP etc. away from other signal traces or unrelated power traces/areas or power supply components			

Notes:

1. The PCIe spec. has 40-60Ω absolute min/max trace impedance, which can be used instead of the 50Ω, ± 15%.
2. If routing in the same layer is necessary, route group TX and RX separately without mixing RX/TX routes and keep distance between nearest TX/RX trace and RX to other signals 3x RX-RX separation.
3. For trace loss >= 0.7dB/in @ 2.5GHz, the max trace length should be 7 inches. To reduce trace loss, ensure the loss tangent of the dielectric material and roughness of the metal are tightly controlled.
4. The average of the differential signals is used for length matching.
5. Do length matching before Via transitions to different layers or any discontinuity to minimize common mode conversion.

Figure 7-6. Insertion Loss S-Parameter Plot (SDD21)

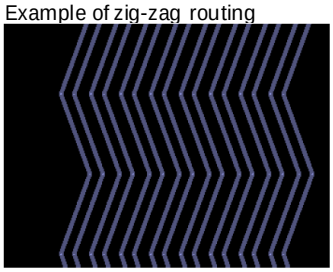




7.2.2 PCIe Gen4 Design Guidelines

The following table details the PCIe design guidelines for Gen4.

Table 7-13. PCIe Gen4 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Data Rate / UI Period	16.0 / 62.5	Gbps / ps	8.0GHz, half-rate architecture
Topology	Point-point		Unidirectional, differential. Driven by 100MHz common reference clock
Termination	43	Ω	To **GND** Single Ended for P and N
Impedance			
Trace Impedance differential / Single Ended	 85 / 50	 Ω	±15%
Reference plane	GND		
Fiber-weave effect	• Use spread-glass (denser weave) instead of regular-glass (sparse weave) to minimize intra-pair skew • Use zig-zag route instead of straight to minimize skew, this is a mandatory for PCIe gen4 design		Example of zig-zag routing 
Spacing			
Trace Spacing (Stripline) Pair – Pair To plane and capacitor pad To unrelated high-speed signals	 4x 4x 4x	Dielectric	TX and RX should not be routed on the same layer. If this is required in a design, they should not be interleaved, and the spacing between the closest RX and TX lanes must be 9x Dielectric spacing.
Length/Skew			
Breakout region (Max Length)	41.9	ps	Minimum width and spacing. 4x or wider dielectric height spacing is preferred
Trace loss budget (for carrier board routing) Routing direct to device Routing to PCIe/M.2 connector	 -16 -10.5	dB/in	@ 4GHz (See TBD), Loss: GEN4 budget – module – end device – safety margin (-28dB + 5dB + 4dB + 3dB) Loss: GEN3 budget – module – end device – safety margin (-28dB + 5dB + 9.5dB + 3dB)
Max trace length (delay) Direct to device on carrier board Stripline Microstrip Routed to PCIe or M.2 connector Stripline Microstrip	 11.9 (2070) 10.9 (1630) 7.8 (1360) 7.1 (1070)	 in (ps)	Mid-loss PCB of 1.47dB/in (Microstrip) or 1.35dB/in (Stripline) is used. Also, 175ps/in for Stripline routing and 150ps/in for Microstrip.
Max PCB via distance from the Device/Connector	41.9	ps	Max distance from Device ball or Connector pin to first PCB via.
PCB within pair (intra-pair) skew	0.15 (0.5)	mm (ps)	Do trace length matching before hitting discontinuities.

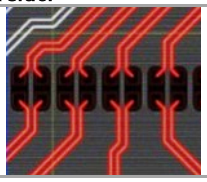
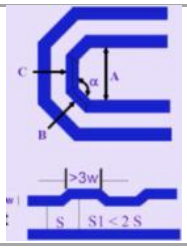
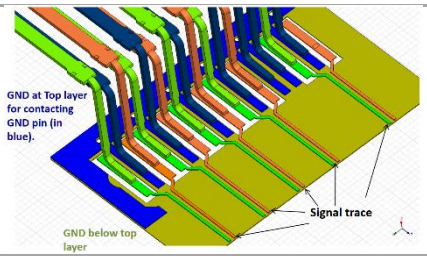
Parameter	Requirement	Units	Notes
Within pair (intra-pair) matching between subsequent discontinuities	0.15 (0.5)	mm (ps)	
Differential pair uncoupled length	41.9	ps	
Via			
Via placement	Place **GND** vias as symmetrically as possible to data pair vias. **GND** via distance should be placed less than 1x the diff pair via pitch		
Max # of Vias	4		Use micro via or back drilled via - no via stub allowed.
Max Via stub length	na		Not Allowed
AC Cap			
Value Min/Max	0.22	**uF**	**20%, 0402 X5R or better. Only required for TX pair when routed to connector. Place close to TX side.**
Voiding	Voiding the plane directly under the pad 3-4 mils larger than the pad size is required.		
Serpentine (See USB 3.1 Guidelines)			
Serpentine			
Min bend angle	**135**	**deg (a)**	**S1 must be taken care in order to consider Xtalk to adjacent pair** 
Dimension **Min A Spacing** **Min B, C Length** **Min Jog Width**	 **4x** **1.5x** **3x**	 **Trace width**	
MIsc.			
GND fill rule	**Remove unwanted GND fill that is either floating or act like antenna**		
Connector			
Voiding	**Void all layers of golden finger area under the pad 5.7 mils larger than the pad size is recommended.**		
Keep critical PCIe traces such as PEX_TX/RX, TERMP etc. away from other signal traces or unrelated power traces/areas or power supply components			

Table 7-14. PCIe Signal Connections Module I/Fs Configured as Root Ports

Module Pin Name	Type	Termination	Description
PCIe Interface #C0 (x4 used for M.2 Key M on Carrier Board)			
UPHY_TX[5:2]_P/N	DIFF OUT	Series Caps (see Design Guideline for value)	**Differential Transmit Data Pairs: Connect to TX_P/N pins of PCIe connector or RX_P/N pin of PCIe device through AC caps.**
UPHY_RX[5:2]_P/N	DIFF IN	Series Caps (see Design Guideline for value) if device on main PCB.	**Differential Receive Data Pairs: Connect to RX_P/N pins of PCIe connector or TX_P/N pin of PCIe device through AC caps.**
PEX_CLK0_P/N	DIFF OUT		**Differential Reference Clock Output: Connect to REFCLK_P/N pins** of PCIe device/connector
PEX_L0_CLKREQ_N	I/O	47KΩ pullup on module to **VDDIO_AO_3V3**.	**PEX Clock Request for PEX_CLK0:** Connect to **CLKREQ** pin on device/connector.
PEX_L0_RST_N	O	4.7KΩ pullup on module to **VDDIO_AO_3V3**	**PEX Reset:** Connect to **PERST** pin on device/connector.
UPHY_REFCLK1_N/P	DIFF IN		**Differential Reference Clock 1 Pair: Unused.**
PCIe Interface #C1 (x1 used for eSATA bridge on Carrier Board)			
UPHY_TX0_P/N	DIFF OUT	Series Capacitor (see Design Guideline for value)	**Differential Transmit Data Pairs: Connect to TX+/– pins of PCIe connector or RX_+/– pin of PCIe device through AC caps.**
UPHY_RX0_P/N	DIFF IN	Series Capacitor (see Design Guideline for value) if device on main PCB.	**Differential Receive Data Pairs: Connect to RX_+/– pins of PCIe connector or TX_+/– pin of PCIe device through AC caps.**
PEX_CLK1_P/N	DIFF OUT		**Differential Reference Clock Output: Connect to REFCLK_+/– pins** of PCIe device/connector.
PEX_L1_CLKREQ_N	I/O	47KΩ pullup on module to **VDDIO_AO_3V3**.	**PEX Clock Request for PEX_CLK1:** Connect to **CLKREQ** pin on device/connector(s)
PEX_L1_RST_N	O	4.7KΩ pullup on module to **VDDIO_AO_3V3**	**PEX Reset:** Connect to **PERST** pin on device/connector.
PCIe Interface #C3 (x1 used for M.2 Key E on Carrier Board)			
UPHY_TX7_P/N	DIFF OUT	Series Caps (see Design Guideline for value)	**Differential Transmit Data Pairs: Connect to TX_P/N pins of PCIe connector or RX_P/N pin of PCIe device through AC caps.**
UPHY_RX7_P/N	DIFF IN	Series Caps (see Design Guideline for value) if device on main PCB.	**Differential Receive Data Pairs: Connect to RX_P/N pins of PCIe connector or TX_P/N pin of PCIe device through AC caps.**
PEX_CLK3_P/N	DIFF OUT		**Differential Reference Clock Output: Connect to REFCLK_P/N pins** of PCIe device/connector
PEX_L3_CLKREQ_N	I/O	47KΩ pullup on module to **VDDIO_AO_3V3**.	**PEX Clock Request for PEX_CLK3:** Connect to **CLKREQ** pin on device/connector.
PEX_L3_RST_N	O	4.7KΩ pullup on module to **VDDIO_AO_3V3**	**PEX Reset:** Connect to **PERST** pin on device/connector.
PCIe Interface #C4 (x2 – Not used on Carrier Board)			
UPHY_TX[9:8]_P/N	DIFF OUT	Series Caps (see Design Guideline for value)	**Differential Transmit Data Pairs: Connect to TX_P/N pins of PCIe connector or RX_P/N pin of PCIe device through AC caps.**
UPHY_RX[9:8]_P/N	DIFF IN	Series Caps (see Design Guideline for value) if device on main PCB.	**Differential Receive Data Pairs: Connect to RX_P/N pins of PCIe connector or TX_P/N pin of PCIe device through AC caps.**
PEX_CLK4_P/N	DIFF OUT		**Differential Reference Clock Output: Connect to REFCLK_P/N pins** of PCIe device/connector.
PEX_L4_CLKREQ_N	I/O	47KΩ pullup on module to **VDDIO_AO_3V3**.	**PEX Clock Request for PEX_CLK4:** Connect to **CLKREQ** pin on device/connector.
PEX_L4_RST_N	O	4.7KΩ pullup on module to **VDDIO_AO_3V3**	**PEX Reset:** Connect to **PERST** pin on device/connector.
UPHY_REFCLK2_N/P	DIFF IN		**Differential Reference Clock 2 Pair: Unused.**

Module Pin Name	Type	Termination	Description
PCIe Interface #C5 (x8 – Routed to lower 8 lanes of PCIe x16 connector)			
NVHS0_TX[7:0]_P/N	DIFF OUT	Series Caps (see Design Guideline for value)	**Differential Transmit Data Pairs: Connect to TX_P/N pins of PCIe connector or RX_P/N pin of PCIe device through AC caps.**
NVHS0_SLVS_RX[7:0]_P/N	DIFF IN	Series Caps (see Design Guideline for value) if device on main PCB.	**Differential Receive Data Pairs: Connect to RX_P/N pins of PCIe connector or TX_P/N pin of PCIe device through AC caps.**
PEX_CLK5_P/N	DIFF OUT		**Differential Reference Clock Output: Connect to REFCLK_P/N pins** of PCIe device/connector.
PEX_L5_CLKREQ_N	I/O	47KΩ pullup on module to **VDDIO_AO_3V3**.	**PEX Clock Request for PEX_CLK5:** Connect to **CLKREQ** pin on device/connector.
PEX_L5_RST_N	O	4.7KΩ pullup on module to **VDDIO_AO_3V3**	**PEX Reset:** Connect to **PERST** pin on device/connector.
NVHS0_SLVS_ REFCLK_N/P	DIFF IN		**Differential Reference Clock Pair for NVHS0_SLVS (Controller #5) interface. Unused when PCIe interface on NVHS pins is configured as Root Port.**
PEX_WAKE_N	I	47KΩ pullup to **VDDIO_AO_3V3** on Module.	**PEX Wake:** Connect to **WAKE** pins on devices or connectors

Note: Check the "Supported USB 3.1 PEX and UFS Interface Mapping" tables earlier in this section for PCIe IF mapping options.

Table 7-15. PCIe Signal Connections Module I/F Configured as Endpoint

Module Pin Name	Type	Termination	Description
PCIe Interface #C5 (Up to x8)			
NVHS0_TX[7:0]_P/N	DIFF OUT	Series Caps (see Design Guideline for value)	**Differential Transmit Data Pairs**: Connect to TX_P/N pins of PCIe connector or **RX_P/N** pin of PCIe device through AC caps.
NVHS0_SLVS_RX[7:0]_P/N	DIFF IN	Series Caps (see Design Guideline for value) if device on main PCB.	**Differential Receive Data Pairs**: Connect to RX_P/N pins of PCIe connector or **TX_P/N** pin of PCIe device through AC caps.
PEX_CLK5_P/N	DIFF OUT		**Differential Reference Clock Output: Unused when interface #C5 is used as Endpoint.**
PEX_L5_CLKREQ_N	I/O	47KΩ pullup on module to **VDDIO_AO_3V3**.	**PEX Clock Request for PEX_CLK5:** Connect to **CLKREQ** pin on device/connector.
PEX_L5_RST_N	I	4.7KΩ pullup on module to **VDDIO_AO_3V3**	**PEX Reset:** Connect to **PERST** pin on device/connector.
NVHS0_SLVS_REFCLK_N/P	DIFF IN		**Differential Reference Clock Pair for NVHS0_SLVS (Controller #5) interface. Connect 100MHz differential clock source to the REFCLK pins when the PCIe interface on NVHS pins is configured as Endpoint.**
PEX_WAKE_N	I	47KΩ pullup to **VDDIO_AO_3V3** on Module.	**PEX Wake:** Unused for interfaces configured as Endpoint

Note: Check the "Supported USB 3.1 PEX and UFS Interface Mapping" tables earlier in this section for PCIe IF mapping options.

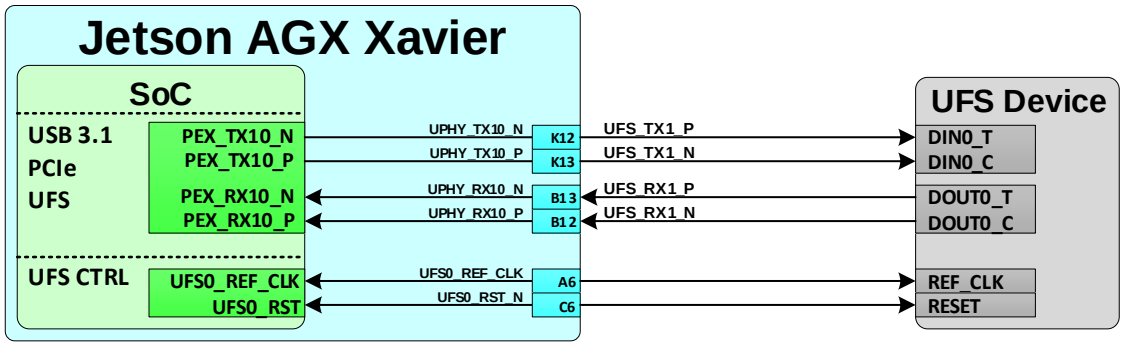
Table 7-16. Recommended PCIe Observation Test Points for Initial Boards

Test Points Recommended	Location
One for each of the PCIe TX_+/– output lines used.	Near PCIe device. Connector pins may serve as test points if accessible.
One for each of the PCIe RX_+/– input lines used.	Near Jetson AGX Xavier connector.

7.3 UFS

Jetson AGX Xavier supports a x1 lane UFS interface.

Figure 7-7. UFS Connections Example



7.3.1 UFS Design Guidelines

The following tables gives the signal routing requirements for the UFS interface.

Table 7-17. UFS Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Max Rate HS-GEAR1 (A-Series/B-Series) HS-GEAR2(A-Series/B-Series) HS-GEAR3(A-Series/B-Series)	 1248 / 1457.6 2496 / 2915.2 4992 / 5830.4	Mbps	
Configuration / Device Organization	1	Load	
Topology	Point-point		Unidirectional, 100Ω Differential
Termination	100	Ω	Differential on die termination at TX/RX
Impedance			
Trace Impedance: Differential / Single Ended	100 / 50	Ω	±15%. See note 1
Reference plane	**GND**		
Spacing			
Trace Spacing (Stripline/Microstrip) Pair – Pair To plane and capacitor pad To unrelated high-speed signals	 3x / 4x 3x / 4x 3x / 4x	Dielectric	
Length/Skew			
Breakout region (Max Length)	41.9	ps	Minimum width and spacing. 4x or wider dielectric height spacing is preferred
Max trace length Stripline Microstrip	 4 (700) 4 (600)	In (ps)	

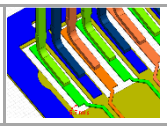
Parameter	Requirement	Units	Notes
Max PCB within pair (intra-pair) skew	0.15 (0.5)	mm (ps)	
Max Pair to Pair skew Tightly coupled case Nominally coupled case	 33 100	ps	
Within pair (intra-pair) matching between subsequent discontinuities	0.15 (0.5)	mm (ps)	Do trace length matching before hitting discontinuities
Differential pair uncoupled length	41.9	ps	
Via			
Via placement	Place GND vias as symmetrically as possible to data pair vias. GND via distance should be placed less than 1x the diff pair via pitch		
Max # of Vias PTH Vias Micro-Vias	 2 No requirement		
Max Via stub length	0.4	mm	Longer via stubs would require review
Discontinuity			
Voiding	Voiding the plane directly under the pad 5.7 mils larger than the pad size is recommended.		
General			
Keep critical PCIe traces such as PEX_TX/RX, TERMP etc. away from other signal traces or unrelated power traces/areas or power supply components			

Table 7-18. UFS Signal Connections

Ball Name (Function)	Type	Termination	Description
UPHY_TX10_P/N (UFS_TX0_P/N)	DIFF OUT		Differential Transmit Data Pairs: Connect to DIN0_T/C pins of UFS device
UFS0_REF_CLK	O		UFS Reference Clock: Connect to REF_CLK pin on device.
UFS0_RST	O		UFS Reset: Connect to RST pin on device

Note: Due to the power connections on the module, the SoC UFS sideband signal interface (UFS0_REF_CLK and UFS0_RST) supports 1.2V operation only. If higher voltage is required by the connected UFS device, level shifters will be needed.

Chapter 8. Gigabit Ethernet

Jetson AGX Xavier provides an RGMII interface to support GBit Ethernet functionality. The Ethernet PHY, magnetics and RJ45 connector are implemented on the carrier board.

Table 8-1. Jetson AGX Xavier Gigabit Ethernet Pin Descriptions

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
J5	ENET_INT	SOC_GPIO08	Ethernet Interrupt	Ethernet PHY	Input	CMOS – 1.8V	ST	pd
H5	ENET_RST_N	SOC_GPIO09	Ethernet Reset	Ethernet PHY	Output	CMOS – 1.8V	ST	pd
C4	RGMII_RD0	EQOS_RD0	Ethernet Receive data bit 0	Ethernet PHY	Input	CMOS – 1.8V	LV_CZ	z
K6	RGMII_RD1	EQOS_RD1	Ethernet Receive data bit 1	Ethernet PHY	Input	CMOS – 1.8V	LV_CZ	z
H6	RGMII_RD2	EQOS_RD2	Ethernet Receive data bit 2	Ethernet PHY	Input	CMOS – 1.8V	LV_CZ	z
E5	RGMII_RD3	EQOS_RD3	Ethernet Receive data bit 3	Ethernet PHY	Input	CMOS – 1.8V	LV_CZ	z
D5	RGMII_RX_CTL	EQOS_RX_CTL	Ethernet Receive Control	Ethernet PHY	Input	CMOS – 1.8V	LV_CZ	z
C5	RGMII_RXC	EQOS_RXC	Ethernet Receive Clock	Ethernet PHY	Input	CMOS – 1.8V	LV_CZ	z
E6	RGMII_SMA_MDC	EQOS_SMA_MDC	Ethernet Management Clock	Ethernet PHY	Output	CMOS – 1.8V	LV_CZ	z
E7	RGMII_SMA_MDIO	EQOS_SMA_MDIO	Ethernet Management Data	Ethernet PHY	Bidir	CMOS – 1.8V	LV_CZ	pu
J6	RGMII_TD0	EQOS_TD0	Ethernet Transmit data bit 0	Ethernet PHY	Output	CMOS – 1.8V	LV_CZ	z
G5	RGMII_TD1	EQOS_TD1	Ethernet Transmit data bit 1	Ethernet PHY	Output	CMOS – 1.8V	LV_CZ	z
J7	RGMII_TD2	EQOS_TD2	Ethernet Transmit data bit 2	Ethernet PHY	Output	CMOS – 1.8V	LV_CZ	z
G6	RGMII_TD3	EQOS_TD3	Ethernet Transmit data bit 3	Ethernet PHY	Output	CMOS – 1.8V	LV_CZ	z
K7	RGMII_TX_CTL	EQOS_TX_CTL	Ethernet Transmit Control	Ethernet PHY	Output	CMOS – 1.8V	LV_CZ	z
B5	RGMII_TXC	EQOS_TXC	Ethernet Transmit Clock	Ethernet PHY	Output	CMOS – 1.8V	LV_CZ	Z

Notes:

1. In the Type/Dir column, Output is from Jetson AGX Xavier. Input is to Jetson AGX Xavier. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Figure 8-1. Ethernet Connections

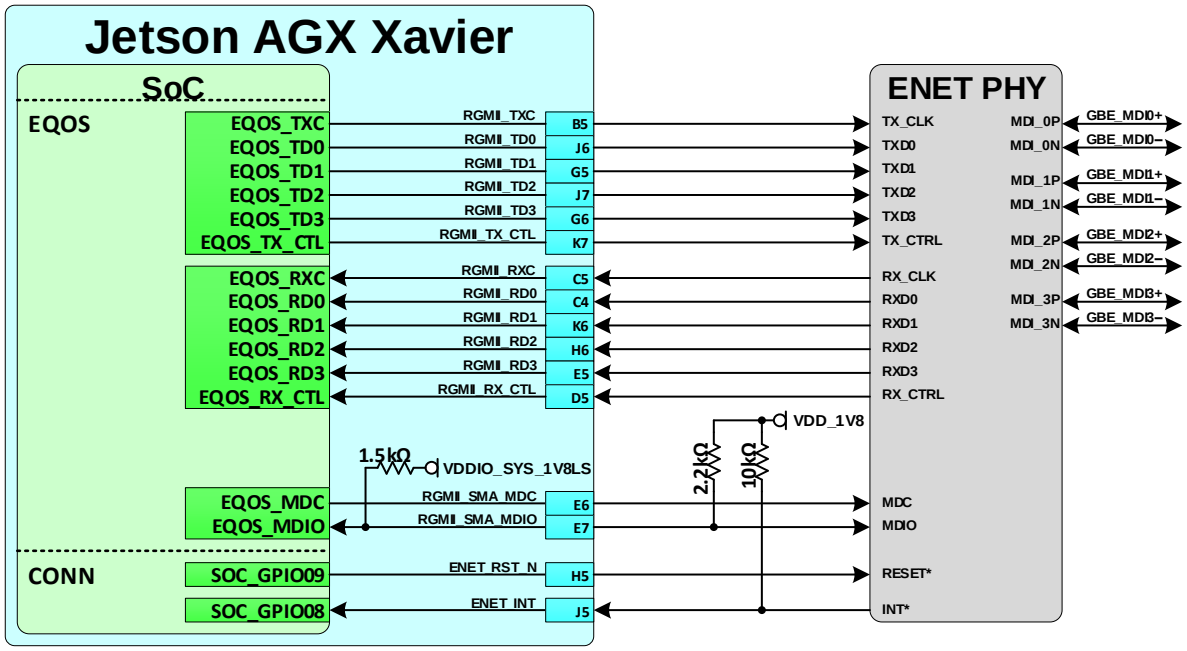
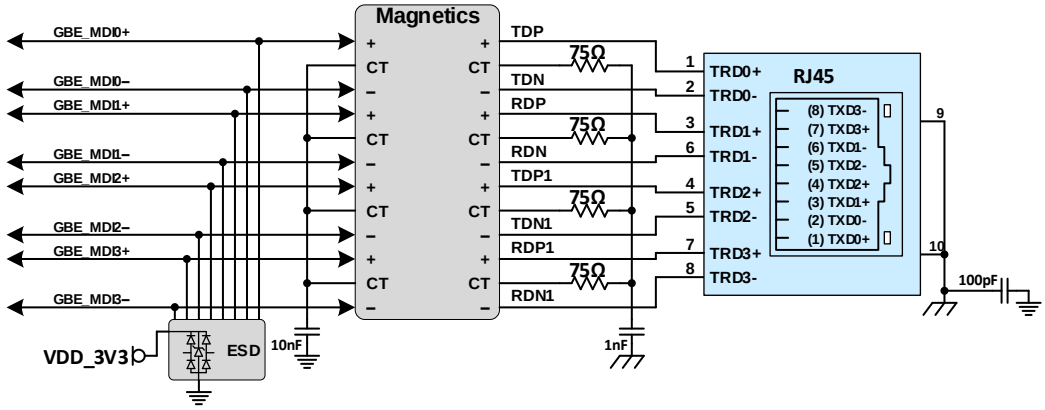


Figure 8-2. Gigabit Ethernet Magnetics and RJ45 Connections



Note: The connections in Figure 8-2 match those used on the carrier board and are shown for reference.

Table 8-2. RGMII Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency	125	MHz	
Topology	Point to point		Unidirectional, source terminated, source synchronous
Reference plane	GND or PWR		See note 1
Max PCB breakout delay	5 (30)	mm (ps)	
Trace Impedance	45-50	Ω	±15%
Via proximity (Signal via to GND return via)	< 3.8 (24)	mm (ps)	See note 2
Trace spacing: Microstrip / Stripline	4x / 3x	dielectric	
Max Trace Length/Delay	175 (1200)	mm (ps)	
Max Trace Delay Skew Between Clock and Data	4.8 (30)	mm (ps)	
Isolation of TX and RX CLK signals	One of the following options for **TX_CLK** and **RX_CLK** signals: 1. **GND** shielding from each other and any other signal, or 2. >5x spacing from each other and any other signal, or 3. Routed on separate layers from each other and any other signal		
Isolation of TX and RX groups	One of the following options for **TX** signal and **RX** signal groups: 1. **GND** shielding from each other, or 2. >5x spacing from each other, or 3. Routed on separate layers from each other		
Noise Coupling Avoidance	Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components		

Notes:

1. If PWR, add 2x 0201 100nF and 2x 0402 4.7uF decoupling capacitors between PWR and GND for return current
2. Up to 4 signal vias can share a single GND return via

Table 8-3. Ethernet MDI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Reference plane	GND		
Trace Impedance: Diff pair / Single Ended	100 / 50	Ω	±15%. Differential impedance target is 100Ω. 90Ω can be used if 100Ω is not achievable
Min Trace Spacing (Pair-Pair)	0.763	mm	
Max Trace Length	109 (690)	mm (ps)	
Max Within Pair (Intra-Pair) Skew	0.15 (1)	mm (ps)	
Number of Vias	minimum		Ideally there should be no vias, but if required for breakout to Ethernet controller or magnetics, keep very close to either device.

Table 8-4. Ethernet Signal Connections

Module Pin Name	Type	Termination	Description
RGMII_TXC	O		**RGMI Transmit Clock: Connect to TXCLK pin on GbE Transceiver.**
RGMII_TD[3:0]	O		**RGMI Transmit Data: Connect to TXD[3:0] pins on GbE Transceiver.**
RGMII_TX_CTL	O		**RGMI Transmit Control: Connect to TXEN pin on GbE Transceiver.**
RGMII_RXC	I		**RGMI Receive Clock: Connect to RXCLK pin on GbE Transceiver.**
RGMII_RD[3:0]	I		**RGMI Receive Data: Connect to RXD[3:0] pins on GbE Transceiver.**
RGMII_RX_CTL	I		**RGMI Receive Control: Connect to RXDV pin on GbE Transceiver.**
RGMII_MDC	O		**MDC: Connect to MDC pin on GbE Transceiver.**
RGMII_MDIO	I/O	2.2kΩ pull-up to VDD_1V8	**MDIO: Connect to MDIO pin on GbE Transceiver.**
ENET_RST_N	O		**Ethernet Reset: Connect to Reset input on Ethernet PHY.**
ENET_INT	I	10kΩ pull-up to VDD_1V8	**Ethernet Interrupt: Connect to Interrupt output on Ethernet PHY.**
GBE_MDI[3:0]+/−	DIFF I/O	ESD device to GND per signal	**Gigabit Ethernet MDI IF Pairs: Connect to Magnetics** +/− pins

Table 8-5. Recommended Gigabit Ethernet Observation Test Points for Initial Boards

Test Points Recommended	Location
One for each of the RGMII lines.	
One for each of the **MDI[3:0]+/−** lines.	Near Jetson AGX Xavier connector and magnetics device.

Chapter 9. Display

Jetson AGX Xavier includes three interfaces (HDMI_DP[2:0]). Each can support eDP / DP or HDMI. See the *Jetson AGX Xavier Data Sheet* for the maximum resolutions supported.

Table 9-1. Jetson AGX Xavier HDMI, eDP, and DP Pin Description

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
H48	HDMI_DP0_TX0_N	HDMI_DP0_TXDN0	DisplayPort 0 Lane 0– or HDMI Lane 2–	USB Type C Conn. J512 (via Alt Mode Switch)	Output	Diff pair, AC-Coupled on carrier board	–	z
H49	HDMI_DP0_TX0_P	HDMI_DP0_TXDP0	DisplayPort 0 Lane 0+ or HDMI Lane 2+				–	z
G50	HDMI_DP0_TX1_N	HDMI_DP0_TXDN1	DisplayPort 0 Lane 1– or HDMI Lane 1–				–	z
G51	HDMI_DP0_TX1_P	HDMI_DP0_TXDP1	DisplayPort 0 Lane 1+or HDMI Lane 1+				–	z
J48	HDMI_DP0_TX2_N	HDMI_DP0_TXDN2	DisplayPort 0 Lane 2– or HDMI Lane 0–				–	z
J47	HDMI_DP0_TX2_P	HDMI_DP0_TXDP2	DisplayPort 0 Lane 2+ or HDMI Lane 0+				–	z
K47	HDMI_DP0_TX3_N	HDMI_DP0_TXDN3	DisplayPort 0 Lane 3– or HDMI Clk Lane–				–	z
K46	HDMI_DP0_TX3_P	HDMI_DP0_TXDP3	DisplayPort 0 Lane 3+ or HDMI Clk Lane+				–	z
F51	DP0_AUX_CH_N	DP_AUX_CH0_N	DisplayPort 0 Aux– or HDMI DDC SDA		Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC/I2C)	DP_AUX	z
F52	DP0_AUX_CH_P	DP_AUX_CH0_P	DisplayPort 0 Aux+ or HDMI DDC SCL				DP_AUX	z
K52	DP0_HPD	DP_AUX_CH0_HPD	DisplayPort/HDMI 0 Hot Plug Detect		Input	CMOS – 1.8V	DD	pd
A48	HDMI_DP1_TX0_N	HDMI_DP1_TXDN0	DisplayPort 1 Lane 0– or HDMI Lane 2–	USB Type C Conn. J513 (via Alt Mode Switch)	Output	Diff pair, AC-Coupled on carrier board	–	z
A47	HDMI_DP1_TX0_P	HDMI_DP1_TXDP0	DisplayPort 1 Lane 0+ or HDMI Lane 2+				–	z
B48	HDMI_DP1_TX1_N	HDMI_DP1_TXDN1	DisplayPort 1 Lane 1– or HDMI Lane 1–				–	z
B49	HDMI_DP1_TX1_P	HDMI_DP1_TXDP1	DisplayPort 1 Lane 1+ or HDMI Lane 1+				–	z
D48	HDMI_DP1_TX2_N	HDMI_DP1_TXDN2	DisplayPort 1 Lane 2– or HDMI Lane 0–				–	z
D49	HDMI_DP1_TX2_P	HDMI_DP1_TXDP2	DisplayPort 1 Lane 2+ or HDMI Lane 0+				–	z
E51	HDMI_DP1_TX3_N	HDMI_DP1_TXDN3	DisplayPort 1 Lane 3– or HDMI Clk Lane–				–	z

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
E50	HDMI_DP1_TX3_P	HDMI_DP1_TXDP3	DisplayPort 1 Lane 3+ or HDMI Clk Lane+				–	z
J53	DP1_AUX_CH_N	DP_AUX_CH1_N	DisplayPort 1 Aux– or HDMI DDC SDA		Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC/I2C)	DP_AUX	z
J52	DP1_AUX_CH_P	DP_AUX_CH1_P	DisplayPort 1 Aux+ or HDMI DDC SCL				DP_AUX	z
K51	DP1_HPD	DP_AUX_CH1_HPD	DisplayPort/HDMI 1 Hot Plug Detect		Input	CMOS – 1.8V	DD	pd
D52	HDMI_DP2_TX0_N	HDMI_DP2_TXDN0	DisplayPort 2 Lane 0– or HDMI Lane 2–	HDMI Connector	Output	Diff pair, AC-Coupled on carrier board	–	z
D51	HDMI_DP2_TX0_P	HDMI_DP2_TXDP0	DisplayPort 2 Lane 0+ or HDMI Lane 2+				–	z
B52	HDMI_DP2_TX1_N	HDMI_DP2_TXDN1	DisplayPort 2 Lane 1– or HDMI Lane 1–				–	z
B51	HDMI_DP2_TX1_P	HDMI_DP2_TXDP1	DisplayPort 2 Lane 1+ or HDMI Lane 1+				–	z
A50	HDMI_DP2_TX2_N	HDMI_DP2_TXDN2	DisplayPort 2 Lane 2– or HDMI Lane 0–				–	z
A51	HDMI_DP2_TX2_P	HDMI_DP2_TXDP2	DisplayPort 2 Lane 2+ or HDMI Lane 0+				–	z
C50	HDMI_DP2_TX3_N	HDMI_DP2_TXDN3	DisplayPort 2 Lane 3– or HDMI Clk Lane–				–	z
C51	HDMI_DP2_TX3_P	HDMI_DP2_TXDP3	DisplayPort 2 Lane 3+ or HDMI Clk Lane+				–	z
G54	DP2_AUX_CH_N	DP_AUX_CH2_N	DisplayPort 2 Aux– or HDMI DDC SDA		Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC/I2C)	DP_AUX	z
G53	DP2_AUX_CH_P	DP_AUX_CH2_P	DisplayPort 2 Aux+ or HDMI DDC SCL				DP_AUX	z
K50	DP2_HPD	DP_AUX_CH2_HPD	DisplayPort/HDMI 2 Hot Plug Detect		Input	CMOS – 1.8V	DD	pd
J50	HDMI_CEC	HDMI_CEC	HDMI CEC		Bidir	Open Drain, 1.8V (3.3V tolerant – See note)	DD	z

Notes:

1. Although HDMI_CEC is 3.3V tolerant, there is a pull-up on the module to 1.8V on the pin. Any pull-up to 3.3V on the carrier board should be weak. It is recommended that the value be no stronger than the 162kΩ used on the P2922 reference design
2. In the Type/Dir column, Output is from Jetson AGX Xavier. Input is to Jetson AGX Xavier. Bidir is for Bidirectional signals.
3. The direction shown in this table for DPx_HPD is true when used for Hot-plug Detect. Otherwise if used as GPIOs, the direction is bidirectional.
4. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
5. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

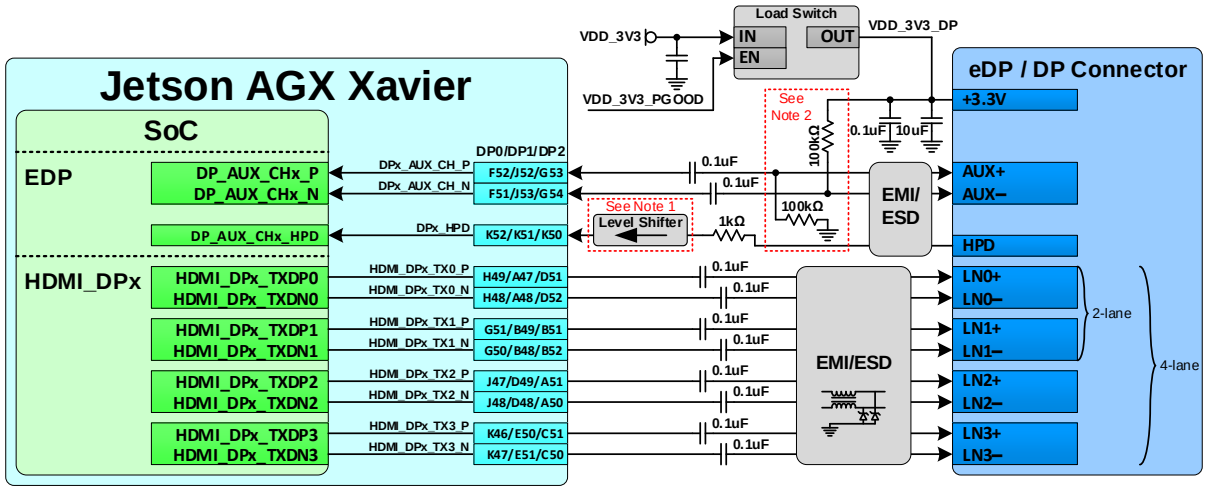
Table 9-2. DP and HDMI Pin Mapping

Module Pin Name	Module Pin #s	SoC Pin Name	SoC Pin #s	HDMI	DP
HDMI_DP0					
HDMI_DP0_TX0_P	H49	HDMI_DP0_TXDP0	C44	TXD2_P	TXD0_P
HDMI_DP0_TX0_N	H48	HDMI_DP0_TXDN0	D44	TXD2_N	TXD0_N
HDMI_DP0_TX1_P	G51	HDMI_DP0_TXDP1	D43	TXD1_P	TXD1_P
HDMI_DP0_TX1_N	G50	HDMI_DP0_TXDN1	E43	TXD1_N	TXD1_N
HDMI_DP0_TX2_P	J47	HDMI_DP0_TXDP2	C42	TXD0_P	TXD2_P
HDMI_DP0_TX2_N	J48	HDMI_DP0_TXDN2	D42	TXD0_N	TXD2_N
HDMI_DP0_TX3_P	K46	HDMI_DP0_TXDP3	A41	TXC_P	TXD3_P
HDMI_DP0_TX3_N	K47	HDMI_DP0_TXDN3	A42	TXC_N	TXD3_N
HDMI_DP1					
HDMI_DP1_TX0_P	A47	HDMI_DP1_TXDP0	F41	TXD2_P	TXD0_P
HDMI_DP1_TX0_N	A48	HDMI_DP1_TXDN0	G41	TXD2_N	TXD0_N
HDMI_DP1_TX1_P	B49	HDMI_DP1_TXDP1	H40	TXD1_P	TXD1_P
HDMI_DP1_TX1_N	B48	HDMI_DP1_TXDN1	G40	TXD1_N	TXD1_N
HDMI_DP1_TX2_P	D49	HDMI_DP1_TXDP2	J41	TXD0_P	TXD2_P
HDMI_DP1_TX2_N	D48	HDMI_DP1_TXDN2	K41	TXD0_N	TXD2_N
HDMI_DP1_TX3_P	E50	HDMI_DP1_TXDP3	H42	TXC_P	TXD3_P
HDMI_DP1_TX3_N	E51	HDMI_DP1_TXDN3	J42	TXC_N	TXD3_N
HDMI_DP2					
HDMI_DP2_TX0_P	D51	HDMI_DP2_TXDP0	F45	TXD2_P	TXD0_P
HDMI_DP2_TX0_N	D52	HDMI_DP2_TXDN0	G45	TXD2_N	TXD0_N
HDMI_DP2_TX1_P	B51	HDMI_DP2_TXDP1	F44	TXD1_P	TXD1_P
HDMI_DP2_TX1_N	B52	HDMI_DP2_TXDN1	G44	TXD1_N	TXD1_N
HDMI_DP2_TX2_P	A51	HDMI_DP2_TXDP2	H43	TXD0_P	TXD2_P
HDMI_DP2_TX2_N	A50	HDMI_DP2_TXDN2	G43	TXD0_N	TXD2_N
HDMI_DP2_TX3_P	C51	HDMI_DP2_TXDP3	G42	TXC_P	TXD3_P
HDMI_DP2_TX3_N	C50	HDMI_DP2_TXDN3	F42	TXC_N	TXD3_N

9.1 DP and eDP

Figure 9-1 shows the connection example for the DP and eDP connectors.

Figure 9-1. DP and eDP Connection Example



Notes:

1. A Level shifter is required on HPD to avoid the pin from being driven when the module is off. The level shifter must be non-inverting (preserve polarity of the signal from the display).
2. Pull-up/down only required for DP - not for eDP.
3. If EMI devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing and electrical requirements of the DisplayPort specification for the modes to be supported. Any ESD solution must also maintain signal integrity and meet the DisplayPort requirements for the modes to be supported.

9.1.1 DP and eDP Routing Guidelines

Figure 9-2 shows the topology for DisplayPort and embedded DisplayPort. Table 9-3 shows the signal routing requirements including DP_AUX.

Figure 9-2. DP and eDP Differential Main Link Topology

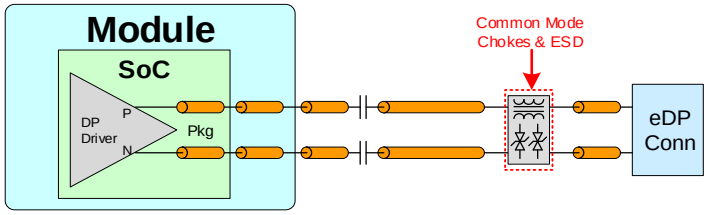
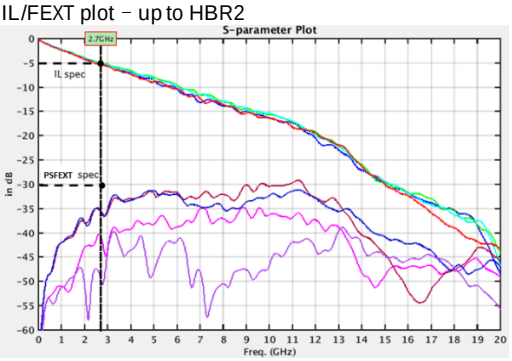
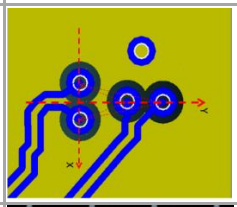
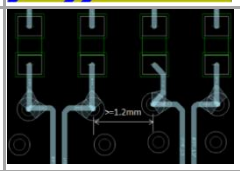


Table 9-3. DP and eDP Main Link Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Max Data Rate / Min UI HBR2 HBR RBR	 5.4 / 185 2.7 / 370 1.62 / 617	 Gbps / ps	Per data lane
Number of Loads / Topology	1	load	Point-Point, Differential, Unidirectional
Termination	100	Ω	On die at TX/RX
Electrical Specification			
Insertion Loss E-HBR @ 0.675GHz PBR 0.68GHz HBR 1.35GHz HBR2 @ 2.7GHz	 <=0.7 <=0.7 <=1.2 <=2.4	 dB dB dB dB	
Resonance dip frequency	>8	GHz	
TDR dip	>85	Ω	@ Tr-200ps (10%-90%)
FEXT @ DC @ 2.7GHz	 <= -40dB <= -30dB	IL/FEXT plot – up to HBR2 	
Impedance			
Trace Impedance (Diff pair)	100 90 85	Ω (±10%)	100Ω is the spec. target. 95/85Ω are implementation options (Zdiff does not account for trace coupling) 95Ω should be used to support DP-HDMI co-layout as HDMI 2.0 requires 100Ω impedance (see HDMI section for addition of series resistor Rs). 85Ω can be used if eDP/DP only and is preferable as it can provide better trace loss characteristic performance. See Note 1.
Reference Plane	**GND**		
Trace Length, Spacing and Skew			
Trace loss characteristic @ 2.7GHz	< 0.81	dB/in	The following max length is derived based on this characteristic. The length constraint must be re-defined if loss characteristic is changed.
Max PCB Via dist. from module conn. **RBR/HBR** **HBR2**	No requirement 7.63 (0.3)	 mm (in)	
Max trace length from module to connector **RBR/HBR** (Stripline / Microstrip) **HBR2** (Stripline) **HBR2** (Microstrip, 5x / 7x)	 215 (1137.5)/(975) 101.6 (700) 89 (525) / 101.6 (600)	mm (ps)	175ps/inch assumption for Stripline, 150ps/inch for Microstrip.

Parameter	Requirement	Units	Notes
Trace spacing (Pair-Pair) Stripline Microstrip (**HBR/RBR**) Microstrip (**HBR2**)	 3x 4x 5x to 7x	 dielectric	
Trace spacing (Main Link to AUX): Stripline/Microstrip	3x / 5x	dielectric	
Max Intra-pair (within pair) Skew	0.15 (1)	mm (ps)	Do not perform length matching within breakout region Do trace length matching before hitting discontinuity (i.e. matching to <1ps before the vias or any discontinuity to minimize common mode conversion).
Max Inter-pair (pair-pair) Skew	150	ps	
Via			
Max GND transition Via distance	< 1x	diff pair pitch	For signals switching reference layers, add symmetrical GND stitching Via near signal Vias.
Impedance dip Recommended via dimension for impedance control Drill/Pad Antipad Via pitch	≥97 ≥92 200/400 >840 ≥880	Ω @ 200ps Ω @ 35ps um um um	The via dimension must be required for the HDMI-DP co-layout condition.
Topology	Y-pattern is recommended keep symmetry Xtalk suppression is best using the Y-pattern. It can also reduce the limit of pair-pair distance.		
	For in-line via, the distance from a via of one lane to the adjacent via from other lane >= 1.2 mm center-center.		
GND via	Place GND via as symmetrically as possible to data pair vias. Up to 4 signal vias (2 diff pairs) can share a single GND return via		GND via is used to maintain return path, while its Xtalk suppression is limited
Max # of Vias PTH vias Micro Vias	 4 if all vias are PTH via Not limited as long as total channel loss meets IL spec		
Max Via Stub Length	0.4	mm	
AC Cap			
Value	0.1	uF	Discrete 0402
Max Dist. from AC cap to connector **RBR/HBR** **HBR2**	 No requirement 0.5	in	
Voiding **RBR/HBR** **HBR2**	 No requirement Voiding required		**HBR2**: Voiding the plane directly under the pad 3-4 mils larger than the pad size is recommended.
Serpentine (See USB 3.1 Guidelines)			

Parameter	Requirement	Units	Notes
Connector			
Voiding RBR/HBR HBR2	 No requirement Voiding required		HBR2: Standard DP Connector: Voiding requirement is stack-up dependent. For typical stack-ups, voiding on the layer under the connector pad is required to be 5.7mil larger than the connector pad.
General			
Keep critical PCIe traces such as PEX_TX/RX, TERMP etc. away from other signal traces or unrelated power traces/areas or power supply components			

Notes:

1. For eDP/DP, the spec puts a higher priority on the trace loss characteristic than on the impedance. However, before selecting 85Ω for impedance, it is important to make sure the selected stack-up, material and trace dimension can achieve the needed low loss characteristic.
2. The average of the differential signals is used for length matching.
3. Do not perform length matching within breakout region. Recommend doing trace length matching to <1ps before vias or any discontinuity to minimize common mode conversion

Table 9-4. DP and eDP Signal Connections

Module Pin Name	Type	Termination	Description
HDMI_DPx_TX[3:0]_P/N	O	Series 0.1uF capacitors on all lines	DP/eDP Differential CLK/Data Lanes: Connect to matching pins on display connector. See DP/HDMI Pin Mapping and connection diagram for details.
DPx_AUX_CH_P/N	I/OD	Series 0.1uF capacitors	DP/eDP: Auxiliary Channels: Connect to AUX_CH+/– on display connector.
DPx_HPD	I		DP/eDP: Hot Plug Detect: Connect to HPD pin on display connector.

Table 9-5. Recommended DP and eDP Observation Test Points for Initial Boards

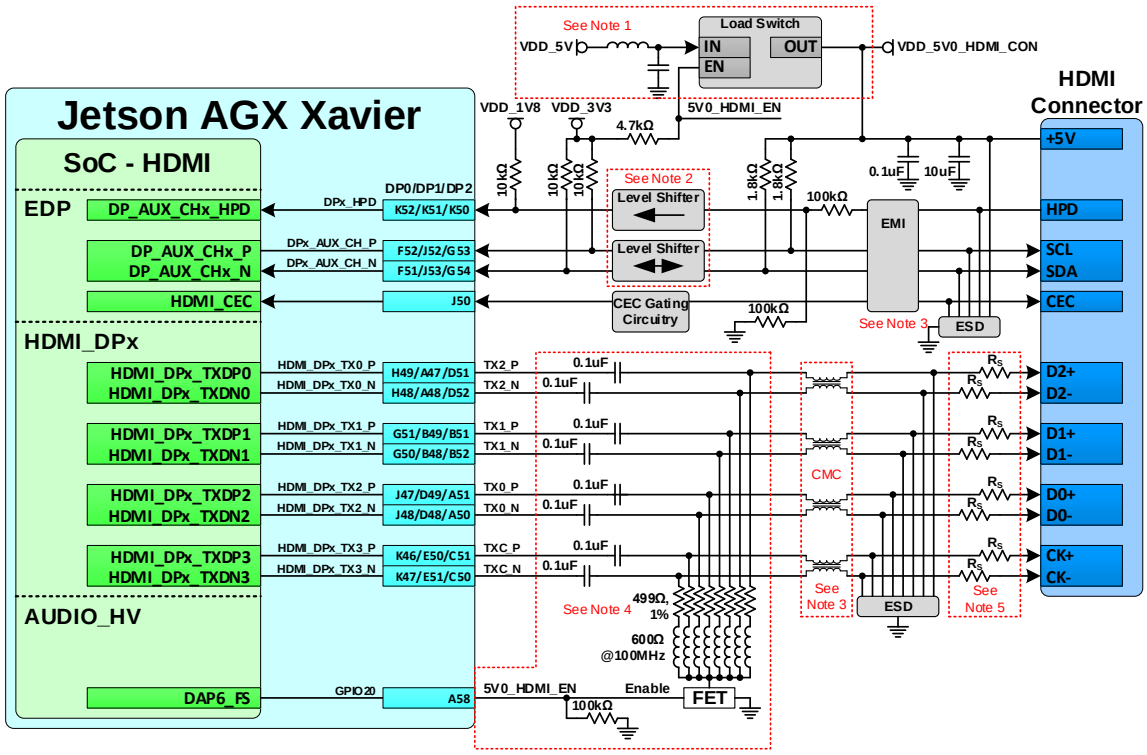
Test Points Recommended	Location
One for each signal line.	Near display connector. Connector pins can be used if accessible.

Note: Test points must be done carefully to minimize signal integrity impact. Avoid stubs and keep pads small and near signal traces

9.2 HDMI

A standard DP 1.2a or HDMI v2.0 interface is supported. These share the same set of interface pins, so either DisplayPort or HDMI can be supported natively.

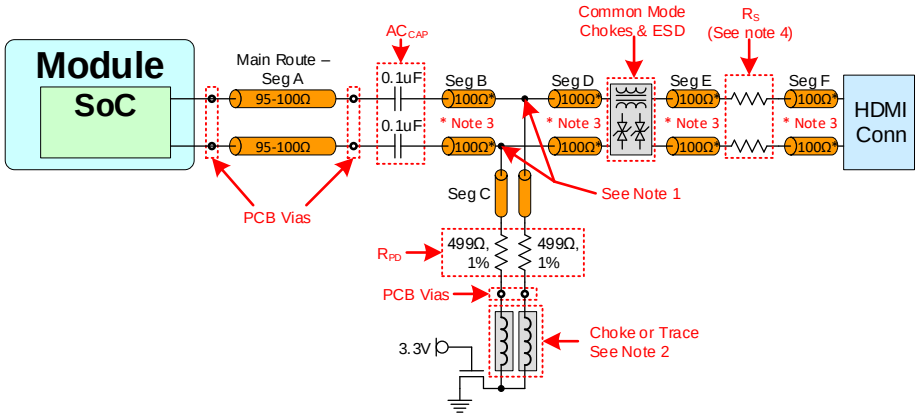
Figure 9-3. HDMI Connection Example



Notes:

1. The load switch circuit shown is intended to remove power to the HDMI connector and related circuitry to avoid backdrive on signals to the module. Other mechanisms may be used but must prevent module pins being driven when the module is off.
2. Level shifters required on DDC/HPD. Jetson AGX Xavier pads are not 5V tolerant and cannot directly meet HDMI VIL/VIH requirements. HPD level shifter can be non-inverting or inverting.
3. If EMI/ESD devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing and electrical requirements of the HDMI specification for the modes to be supported. ee requirements and recommendations in the related sections of Table 9-6.
4. The HDMI_DP_TXx pads are native DP pads and require series AC capacitors (ACCAP) and pull-downs (RPD) to be HDMI compliant. The 499Ω, 1% pull-downs must be disabled when SoC is off to meet the HDMI VOFF requirement. The enable to the FET, enables the pull-downs when the HDMI interface is to be used. Chokes between pull-downs and FET are required for Standard Technology designs and recommended for HDI designs.
5. Series resistors RS are required. See the RS section of Table 9-6 for details.

Figure 9-4. HDMI CLK and Data Topology

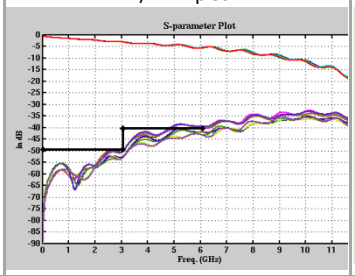
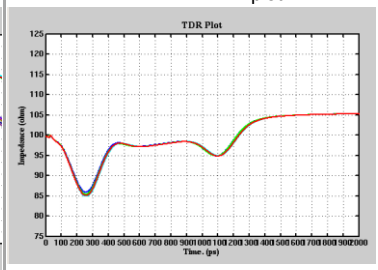


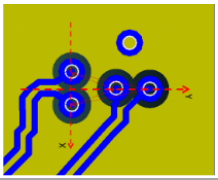
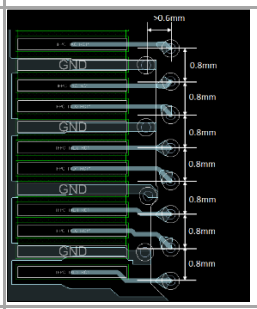
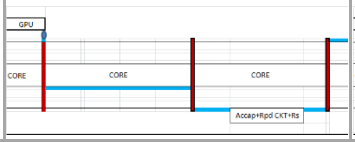
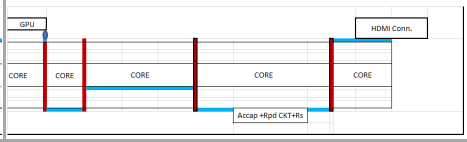
Notes:

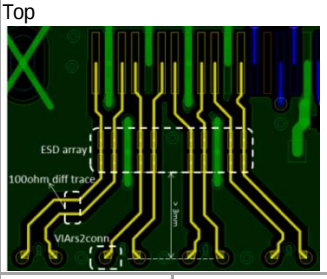
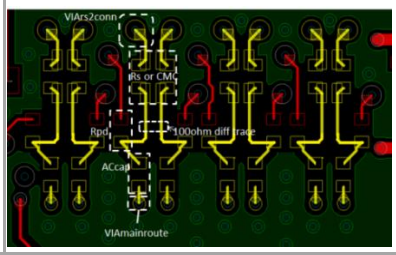
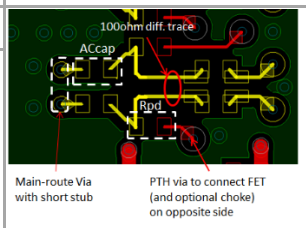
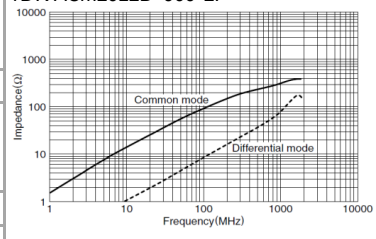
1. RPD pad must be on the main trace. RPD and ACCAP must be on same layer.
2. Chokes (600 Ω @ 100 MHz) or narrow traces (1 uH@DC-100 MHz) between pull-downs and FET are required for Standard Technology (through-hole) designs and recommended for HDI designs.
3. The trace after the main-route via should be routed on the top or bottom layer of the PCB, and either with 100 ohm differential impedance, or as uncoupled 50 ohm Single Ended traces.
4. RS series resistor is required. See the RS section of Table 9-6 for details.

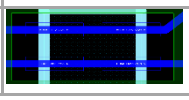
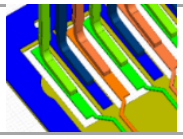
Table 9-6. HDMI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Max Frequency / UI	5.94 / 168	Gbps / ps	Per lane – not total link bandwidth
Topology	Point to point		Unidirectional, Differential
Termination At Receiver On-board	 100 500	 Ω	Differential To **3.3V** at receiver To **GND** near connector

Parameter	Requirement	Units	Notes
Electrical Specification			
IL resonance dip frequency	<= 1.7 <= 2 <= 3 < 6 > 12	dB @ 1GHz dB @ 1.5GHz dB @ 3GHz dB @ 6GHz GHz	
TDR dip	>= 85	Ω @ Tr=200ps	10%-90%. If TDR dip is 75~85ohm that dip width should < 250ps
FEXT (PSFEXT)	<= -50 <= -40 <= -40	dB at DC dB at 3GHz dB at 6GHz	PSNEXT is derived from an algebraic summation of the individual NEXT effects on each pair by the other pairs
	IL/FEXT plot 		TDR plot 
Impedance			
Trace Impedance Diff pair	100	Ω	±10%. Target is 100Ω. 95Ω for the breakout & main route is an implementation option.
Reference plane	GND		
Trace Length, Spacing and Skew			
Trace loss characteristic:	< 0.8 < 0.4	dB/in. @ 3GHz dB/in. @ 1.5GHz	The max length is derived based on this characteristic. The length constraint must be re-defined if the loss characteristic is changed.
Trace spacing (Pair-Pair) Stripline Microstrip: pre 1.4b Microstrip: 1.4b/2.0	3x 4x 5x to 7x	dielectric	For Stripline, this is 3x of the thinner of above and below.
Trace spacing (Main Link to DDC) Stripline Microstrip	 3x 5x	dielectric	For Stripline, this is 3x of the thinner of above and below.
Max Total Delay (1.4b/2.0 - up to 5.94Gbps) Stripline Microstrip (5x spacing) Microstrip (7x spacing)	 63.5/2.5 (437) 50.8/2.0 (300) 63.5/2.5 (375)	 mm/in (ps)	Propagation delay: 175ps/in. for stripline, 150ps/in. for microstrip).
Max Intra-Pair (within pair) Skew	0.15 (1)	Mm (ps)	See Notes 1, 2 and 3
Max Inter-Pair (pair to pair) Skew	150	ps	See Notes 1, 2 and 3
Max **GND** transition Via distance	1x	Diff pair via pitch	For signals switching reference layers, add one or two ground stitching vias. It is recommended they be symmetrical to signal vias.

Parameter	Requirement	Units	Notes
Via			
Topology	Y-pattern is recommended keep symmetry		Xtalk suppression is the best by Y-pattern. Also it can reduce the limit of pair-pair distance. Need review (NEXT/FEXT check) if via placement is not Y-pattern. 
Minimum Impedance dip Recommended via dimension for impedance control Drill/Pad Antipad Via pitch	≥97 ≥92 200/400 >840 ≥880	Ω @ 200ps Ω @ 35ps um um um	
GND via	Place GND via as symmetrically as possible to data pair vias. Up to 4 signal vias (2 diff pairs) can share a single GND return via		GND via is used to maintain return path, while its Xtalk suppression is limited
Connector pin via	The break-in trace to the connector pin via should be routed on the BOTTOM in order to avoid via stub effect Equal spacing (0.8mm) between adjacent signal vias. The x-axis distance between signal and GND via should be > 0.6mm		
Max # of Vias PTH vias Micro Vias	 4 if all vias are PTH via Not limited as long as total channel loss meets IL spec		
	No breakout: ⩽ 3 vias 		breakout on the same layer as main trunk: ⩽ 4 vias 
Max Via Stub Length	0.4	mm	long via stub requires review (IL and resonance dip check)
Serpentine (See USB 3.1 Guidelines)			
Topology (See Figure 9-4)			
The main-route via dimensions should comply with the via structure rules (See Via section)			
For the connector pin vias, follow the rules for the connector pin vias (See Via section)			
The traces after main-route via should be routed as 100Ω differential or as uncoupled 50ohm Single-ended traces on PCB Top or Bottom.			
Max distance from RPD to main trace (seg B)	1	mm	
Max distance from AC cap to RPD stubbing point (seg A)	~0	mm	
Max distance between ESD and signal via	3	mm	

Parameter	Requirement	Units	Notes
Add-on Components			
Example of a case where space is limited for placing components.	Top 		Bottom 
AC CAP			
Value	0.1	uF	
Max via distance from BGA	7.62 (52.5)	mm (ps)	
Location	must be placed before pull-down resistor		The distance between the AC cap and the HDMI connector is not restricted.
Placement PTH design Micro-Via design	 Place cap on bottom layer if main-route above core Place cap on top layer if main-route below core Not Restricted		
Void	GND (or PWR) void under/above the cap is needed. Void size = SMT area + 1x dielectric height keepout distance		
Pull-down Resistor (R_{PD}), choke/FET			
Value	500	Ω	
Location.	Must be placed after AC cap		
Layer of placement	Same layer as AC cap. The FET and choke can be placed on the opposite layer thru a PTH via		
Choke between RPD & FET Choke Max Trace Rdc Max Trace length	 600 or 1 ≤20 4	 Ω@100MHz uH@DC-100MHz mΩ mm	Can be choke or Trace. Recommended option for HDMI2.0 HF1-9 improvement.
Void	GND/PWR void under/above cap is preferred		
Common-Mode Choke (Stuffing option – not added unless EMI issue is seen)			
Common-mode impedance @ 100MHz Min Max	 65 90	 Ω	TDK ACM2012D-900-2P 
RDC	<=0.3ohm		
Differential TDR impedance	90ohm +/-15% @ Tr=200ps (10%-90%)		
Min Sdd21 @ 2.5GHz	2.22	dB	
Max Scc21 @ 2.5GHz	19.2	dB	
Location	Close to any adjacent discontinuity (< 8mm) – such as connector, via, etc.		

Parameter	Requirement	Units	Notes
ESD (On-chip protection diode is able to withstand 2kV HMM. External ESD is optional. Designs should include ESD footprint as a stuffing option)			
Max junction capacitance (IO to GND)	0.35	pF	e.g. ON-semiconductor ESD8040
Footprint	Pad right on the net instead of trace stub		
Location	After pull-down resistor/CMC and before RS		
Void	GND/PWR void under/above the cap is needed. Void size = 1mm x 2mm for 1 pair		
Series Resistor (R_S) – Series resistor on P/N path for HDMI 2.0 (Mandatory)			
Value	⩽ 6	Ω	± 10%. 0ohm is acceptable if the design passes the HDMI2.0 HF1-9 test. Otherwise, adjust the RS value to ensure the HDMI2.0 tests pass: Eye diagram, Vlow test and HF1-9 TDR test
Location	After all components and before HDMI connector		
Void	GND/PWR void under/above the RS device is needed. Void size = SMT area + 1x dielectric height keepout distance.		
Connector			
Connector Voiding	Voiding the ground below the signal lanes 0.1448(5.7mil) larger than the pin itself		
General			
Routing over Voids	Routing over voids not allowed except void around device ball/pin the signal is routed to.		
Noise Coupling	Keep critical HDMI related traces including differential clock/data traces and RSET trace away from other signal traces or unrelated power traces/areas or power supply components		

Notes:

1. The average of the differential signals is used for length matching.
2. Do not perform length matching within breakout region. Recommend doing trace length matching to <1ps before vias or any discontinuity to minimize common mode conversion
3. If routing includes a flex or 2nd PCB, the max trace delay and skew calculations must include all the PCBs/flex routing. Solutions with flex/2nd PCB may not achieve maximum frequency operation.

Table 9-7. HDMI Signal Connections

Module Pin Name	Type	Termination (See Note on ESD)	Description
HDMI_DPx_TX3_N/P	DIFF OUT	0.1uF series ACCAP → 500Ω RPD (controlled by FET) → EMI/ESD (if required), ≤6Ω RS (series resistor)	HDMI Differential Clock: Connect to C−/C+ and pins on HDMI connector
HDMI_DPx_TX[2:0]_N/P	DIFF OUT		HDMI Differential Data: Connect to D[2:0]+/− pins. See Table 9-2 and connection diagram.
DPx_HPD	I	Jetson AGX Xavier to Connector: 10kΩ PU to 1.8V → level shifter → 100kΩ series resistor. 100kΩ to GND on connector side.	HDMI Hot Plug Detect: Connect to HPD pin on HDMI Connector
HDMI_CEC	I/OD	Gating circuitry, See connection figure or reference schematics for details.	HDMI Consumer Electronics Control: Connect to CEC on HDMI Connector through circuitry.
DPx_AUX_CH_N/P	I/OD	From Jetson AGX Xavier to Connector: 10kΩ PU to 3.3V → level shifter → 1.8kΩ PU to 5V → connector pin	HDMI: DDC Interface – Clock and Data: Connect DPx_AUX_CH+ to SCL and DPx_AUX_CH− to SDA on HDMI connector
HDMI 5V Supply	P	Adequate decoupling (0.1uF and 10uF recommended) on supply near connector.	HDMI 5V supply to connector: Connect to +5V on HDMI connector.

Note: Any ESD and/or EMI solutions must support targeted modes (frequencies).

Table 9-8. Recommended HDMI and DP Observation Test Points for Initial Boards

Test Points Recommended	Location
One for each signal line.	Near display connector. Connector pins can be used if accessible.

Note: Test points must be done carefully to minimize signal integrity impact. Avoid stubs and keep pads small and near signal traces.

Chapter 10. Video Input

Jetson AGX Xavier provides multiple MIPI CSI D-PHY or C-PHY interfaces for cameras. In addition, an 8-lane SLVS camera interface is supported.

10.1 MIPI CSI

Jetson AGX Xavier supports four MIPI CSI x4 bricks, allowing a variety of device types and combinations to be supported. Up to 4 quad lane cameras or four dual lane cameras plus two quad lane cameras or 6 dual lane cameras (total of 6 in any configuration) are available. Both MIPI D-PHY and C-PHY modes are supported. In D-PHY mode, each data channel has peak bandwidth of up to 2.5Gbps. For C-PHY, each lane (Trio) supports up to 1.7 Gsps.

Note: Maximum data rate may be limited by use case and memory bandwidth.

Table 10-1. Jetson AGX Xavier CSI Pin Description

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
F42	CSI0_CLK_N	CSI_A_CLK_N	Camera, CSI 0: DPHY Clock–, CPHY 01:C	Camera Connector	Input	MIPI D-PHY/C-PHY	–	z
F43	CSI0_CLK_P	CSI_A_CLK_P	Camera, CSI 0: DPHY Clock+. CPHY 00:C				–	z
E41	CSI0_D0_N	CSI_A_D0_N	Camera, CSI 0: DPHY Data 0–. CPHY 00:B				–	z
E42	CSI0_D0_P	CSI_A_D0_P	Camera, CSI 0: DPHY Data 0+. CPHY 00:A				–	z
E38	CSI0_D1_N	CSI_A_D1_N	Camera, CSI 0: DPHY Data 1–. CPHY 01:B				–	z
E39	CSI0_D1_P	CSI_A_D1_P	Camera, CSI 0: DPHY Data 1+. CPHY 01:A				–	z
H42	CSI1_CLK_N	CSI_B_CLK_N	Camera, CSI 1: DPHY Clock–, CPHY 11:C				–	z
H43	CSI1_CLK_P	CSI_B_CLK_P	Camera, CSI 1: DPHY Clock+. CPHY 10:C				–	z
G42	CSI1_D0_N	CSI_B_D0_N	Camera, CSI 1: DPHY Data 0–. CPHY 10:B				–	z
G41	CSI1_D0_P	CSI_B_D0_P	Camera, CSI 1: DPHY Data 0+. CPHY 10:A				–	z
J42	CSI1_D1_N	CSI_B_D1_N	Camera, CSI 1: DPHY Data 1–. CPHY 11:B				–	z
J41	CSI1_D1_P	CSI_B_D1_P	Camera, CSI 1: DPHY Data 1+. CPHY 11:A				–	z
B42	CSI2_CLK_N	CSI_C_CLK_N	Camera, CSI 2: DPHY Clock–, CPHY 21:C				–	z
B43	CSI2_CLK_P	CSI_C_CLK_P	Camera, CSI 2: DPHY Clock+. CPHY 20:C				–	z
A42	CSI2_D0_N	CSI_C_D0_N	Camera, CSI 2: DPHY Data 0–. CPHY 20:B				–	z
A41	CSI2_D0_P	CSI_C_D0_P	Camera, CSI 2: DPHY Data 0+. CPHY 20:A				–	z
C41	CSI2_D1_N	CSI_C_D1_N	Camera, CSI 2: DPHY Data 1–. CPHY 21:B				–	z
C42	CSI2_D1_P	CSI_C_D1_P	Camera, CSI 2: DPHY Data 1+. CPHY 21:A				–	z

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
F45	CSI3_CLK_N	CSI_D_CLK_N	Camera, CSI 3: DPHY Clock–, CPHY31:C				–	z
F46	CSI3_CLK_P	CSI_D_CLK_P	Camera, CSI 3: DPHY Clock+. CPHY 30:C				–	z
E44	CSI3_D0_N	CSI_D_D0_N	Camera, CSI 3: DPHY Data 0–. CPHY 30:B				–	z
E45	CSI3_D0_P	CSI_D_D0_P	Camera, CSI 3: DPHY Data 0+. CPHY 30:A				–	z
G45	CSI3_D1_N	CSI_D_D1_N	Camera, CSI 3: DPHY Data 1–. CPHY 31:B				–	z
G44	CSI3_D1_P	CSI_D_D1_P	Camera, CSI 3: DPHY Data 1+. CPHY 31:A				–	z
F49	CSI4_CLK_N	CSI_E_CLK_N	Camera, CSI 4: DPHY Clock–, CPHY 41:C				–	z
F48	CSI4_CLK_P	CSI_E_CLK_P	Camera, CSI 4: DPHY Clock+. CPHY 40:C				–	z
G47	CSI4_D0_N	CSI_E_D0_N	Camera, CSI 4: DPHY Data 0–. CPHY 40:B				–	z
G48	CSI4_D0_P	CSI_E_D0_P	Camera, CSI 4: DPHY Data 0+. CPHY 40:A				–	z
E48	CSI4_D1_N	CSI_E_D1_N	Camera, CSI 4: DPHY Data 1–. CPHY 41:B				–	z
E47	CSI4_D1_P	CSI_E_D1_P	Camera, CSI 4: DPHY Data 1+. CPHY 41:A				–	z
C45	CSI5_CLK_N	CSI_F_CLK_N	Camera, CSI 5: DPHY Clock–, CPHY 51:C				–	z
C44	CSI5_CLK_P	CSI_F_CLK_P	Camera, CSI 5: DPHY Clock+. CPHY 50:C				–	z
D43	CSI5_D0_N	CSI_F_D0_N	Camera, CSI 5: DPHY Data 0–. CPHY 50:B				–	z
D42	CSI5_D0_P	CSI_F_D0_P	Camera, CSI 5: DPHY Data 0+. CPHY 50:A				–	z
D45	CSI5_D1_N	CSI_F_D1_N	Camera, CSI 5: DPHY Data 1–. CPHY 51:B				–	z
D46	CSI5_D1_P	CSI_F_D1_P	Camera, CSI 5: DPHY Data 1+. CPHY 51:A				–	z
J45	CSI6_CLK_N	CSI_G_CLK_N	Camera, CSI 6: DPHY Clock–, CPHY 61:C				–	z
J44	CSI6_CLK_P	CSI_G_CLK_P	Camera, CSI 6: DPHY Clock+. CPHY 60:C				–	z
K43	CSI6_D0_N	CSI_G_D0_N	Camera, CSI 6: DPHY Data 0–. CPHY 60:B				–	z
K44	CSI6_D0_P	CSI_G_D0_P	Camera, CSI 6: DPHY Data 0+. CPHY 60:A				–	z
H45	CSI6_D1_N	CSI_G_D1_N	Camera, CSI 6: DPHY Data 1–. CPHY 61:B				–	z
H46	CSI6_D1_P	CSI_G_D1_P	Camera, CSI 6: DPHY Data 1+. CPHY 61:A				–	z
B46	CSI7_CLK_N	CSI_H_CLK_N	Camera, CSI 7: DPHY Clock–, CPHY 71:C				–	z
B45	CSI7_CLK_P	CSI_H_CLK_P	Camera, CSI 7: DPHY Clock+. CPHY 70:C				–	z
A45	CSI7_D0_N	CSI_H_D0_N	Camera, CSI 7: DPHY Data 0–. CPHY 70:B				–	z
A44	CSI7_D0_P	CSI_H_D0_P	Camera, CSI 7: DPHY Data 0+. CPHY 70:A				–	z
C48	CSI7_D1_N	CSI_H_D1_N	Camera, CSI 7: DPHY Data 1–. CPHY 71:B				–	z
C47	CSI7_D1_P	CSI_H_D1_P	Camera, CSI 7: DPHY Data 1+. CPHY 71:A				–	z

Notes:

1. The C-PHY pin mappings are programmable. The mappings shown in the table above are the default. The Xavier Series SoC Technical Reference Manual includes information on the mapping (swizzling) for C-PHY (See the NVCSI_CIL_B_POLARITY_SWIZZLE_CTRL_0 register for details).
2. In the Type/Dir column, Output is from Jetson AGX Xavier. Input is to Jetson AGX Xavier. Bidir is for Bidirectional signals.
3. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
4. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Table 10-2. Jetson AGX Xavier Camera Miscellaneous Pin Description

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
J54	MCLK02	EXTPERIPH1_CLK	Camera 0 Master Clock	Camera Connector	Output	CMOS – 1.8V	ST	pd
H53	MCLK03	EXTPERIPH2_CLK	Camera 1 Master Clock				ST	pd
H55	MCLK04	SOC_GPIO41	Camera 2 Master Clock				DD	pd
L57	MCLK05	SOC_GPIO42	Camera 2 Master Clock	Expansion Connector			DD	pd
F53	I2C3_CLK	CAM_I2C_SCL	General I2C 3 Clock	Camera Connector	Bidir	Open-Drain – 1.8V	DD	z
E53	I2C3_DAT	CAM_I2C_SDA	General I2C 3 Data				DD	z
F10	GPIO15	DAP5_SCLK	GPIO / Digital Speaker Output Clock	Camera Connector (Camera 1 Powerdown)	Output	CMOS – 1.8V	ST	pd
F9	GPIO16	DAP5_DOUT	GPIO / Digital Speaker Output Data	Camera Connector (Camera 1 Reset)			ST	pd
K49	GPIO25	SOC_GPIO50	GPIO	Camera Connector (VDD_SYS Enable)			ST	pd
F56	GPIO36	SOC_GPIO53	GPIO	Camera AVDD Enable			ST	pd
L49	UART4_CTS	UART4_CTS	GPIO	Camera Connector (Camera 0 Powerdown)			ST	pu
L5	UART4_TX	UART4_TX	GPIO	Camera Connector (Camera 0 Reset)			ST	pd

Notes:

1. In the Type/Dir column, Output is from Jetson AGX Xavier. Input is to Jetson AGX Xavier. Bidir is for Bidirectional signals.
2. The direction shown in this table for MCLKx, GPIO[16:15], and UART4x is true when used for those functions. These pins are GPIOs and can support input or output (bidirectional).
3. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
4. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Table 10-3. CSI Configurations D-PHY Mode

Signal Name	x2 Configurations						x4 Configurations			
	#1	#2	#3	#4	#5	#6	#1	#2	#3	#4
CSI_0_D0_P/N	Data						Data			
CSI_0_D1_P/N										
CSI_1_D0_P/N		Data								
CSI_1_D1_P/N										
CSI_2_D0_P/N			Data					Data		
CSI_2_D1_P/N										
CSI_3_D0_P/N				Data						
CSI_3_D1_P/N										
CSI_4_D0_P/N					Data				Data	
CSI_4_D1_P/N										
CSI_5_D0_P/N										
CSI_5_D1_P/N										

Signal Name	x2 Configurations						x4 Configurations			
	#1	#2	#3	#4	#5	#6	#1	#2	#3	#4
CSI_6_D0_P/N						Data				Data
CSI_6_D1_P/N										
CSI_7_D0_P/N										
CSI_7_D1_P/N										
CSI_0_CLK_P/N	Clk						Clk			
CSI_1_CLK_P/N		Clk								
CSI_2_CLK_P/N			Clk					Clk		
CSI_3_CLK_P/N				Clk						
CSI_4_CLK_P/N					Clk				Clk	
CSI_5_CLK_P/N										
CSI_6_CLK_P/N[1]						Clk				Clk
CSI_7_CLK_P/N[1]										

Notes:

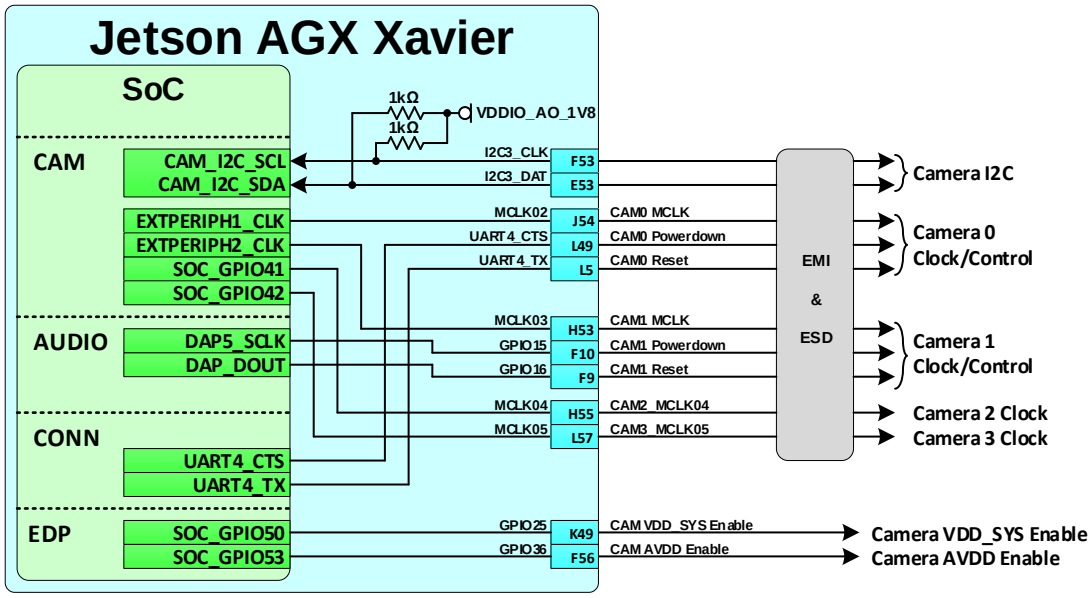
1. Each 2-lane option shown in this table can also be used for one single lane camera as well.
2. Combinations of 1, 2 and 4-lane cameras are supported, as long as any 4-lane cameras match one of the four configurations.

Table 10-4. CSI Configurations C-PHY Mode

		2-Trio Configs						4-Trio Configs			
Camera # / SoC Balls	C-PHY Lanes	#1	#2	#3	#4	#5	#6	#1	#2	#3	#4
CSI_0_CLK_P, CSI_0_D0_P/N	0:0	√						√			
CSI_0_CLK_N, CSI_0_D1_P/N	0:1	√						√			
CSI_1_CLK_P. CSI_1_D0_P/N	1:0		√					√			
CSI_1_CLK_N, CSI_1_D1_P/N	1:1		√					√			
CSI_2_CLK_P, CSI_2_D0_P/N	2:0			√					√		
CSI_2_CLK_N, CSI_2_D1_P/N	2:1			√					√		
CSI_3_CLK_P, CSI_3_D0_P/N	3:0				√				√		
CSI_3_CLK_N, CSI_3_D1_P/N	3:1				√				√		
CSI_4_CLK_P, CSI_4_D0_P/N	4:0					√				√	
CSI_4_CLK_N, CSI_4_D1_P/N	4:1					√				√	
CSI_5_CLK_P, CSI_5_D0_P/N	5:0									√	
CSI_5_CLK_N, CSI_5_D1_P/N	5:1									√	
CSI_6_CLK_P, CSI_6_D0_P/N	6:0						√				√
CSI_6_CLK_N, CSI_6_D1_P/N	6:1						√				√
CSI_7_CLK_P, CSI_7_D0_P/N	7:0										√
CSI_7_CLK_N, CSI_7_D1_P/N	7:1										√

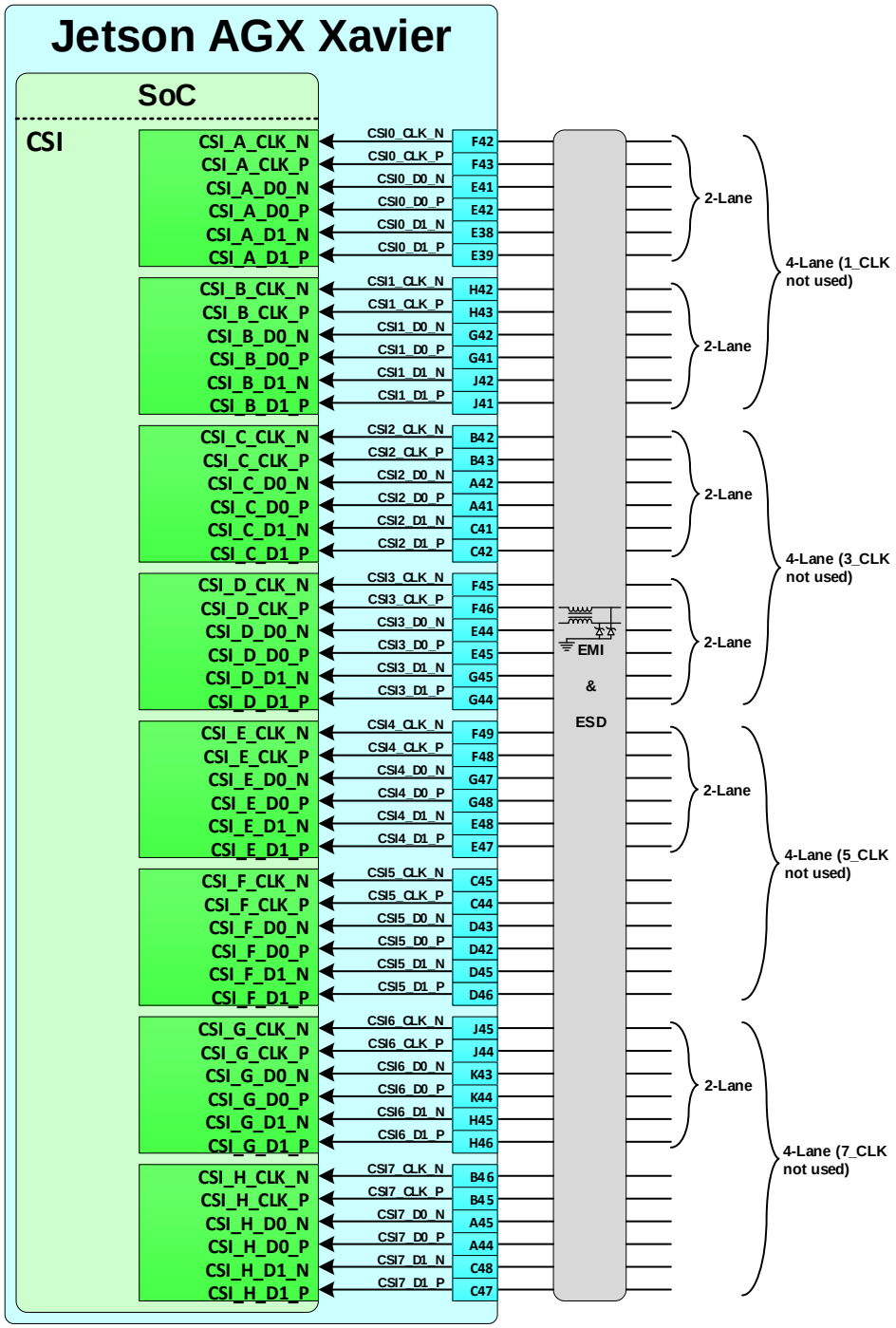
Notes: Each x2 configurations can also be used for one single lane camera (x1 configuration) as well.
Configurations can coexist to support a mix of x1, x2 and x4 lanes, as long as each signal is not shared between multiple configurations.

Figure 10-1. Camera Control Connections



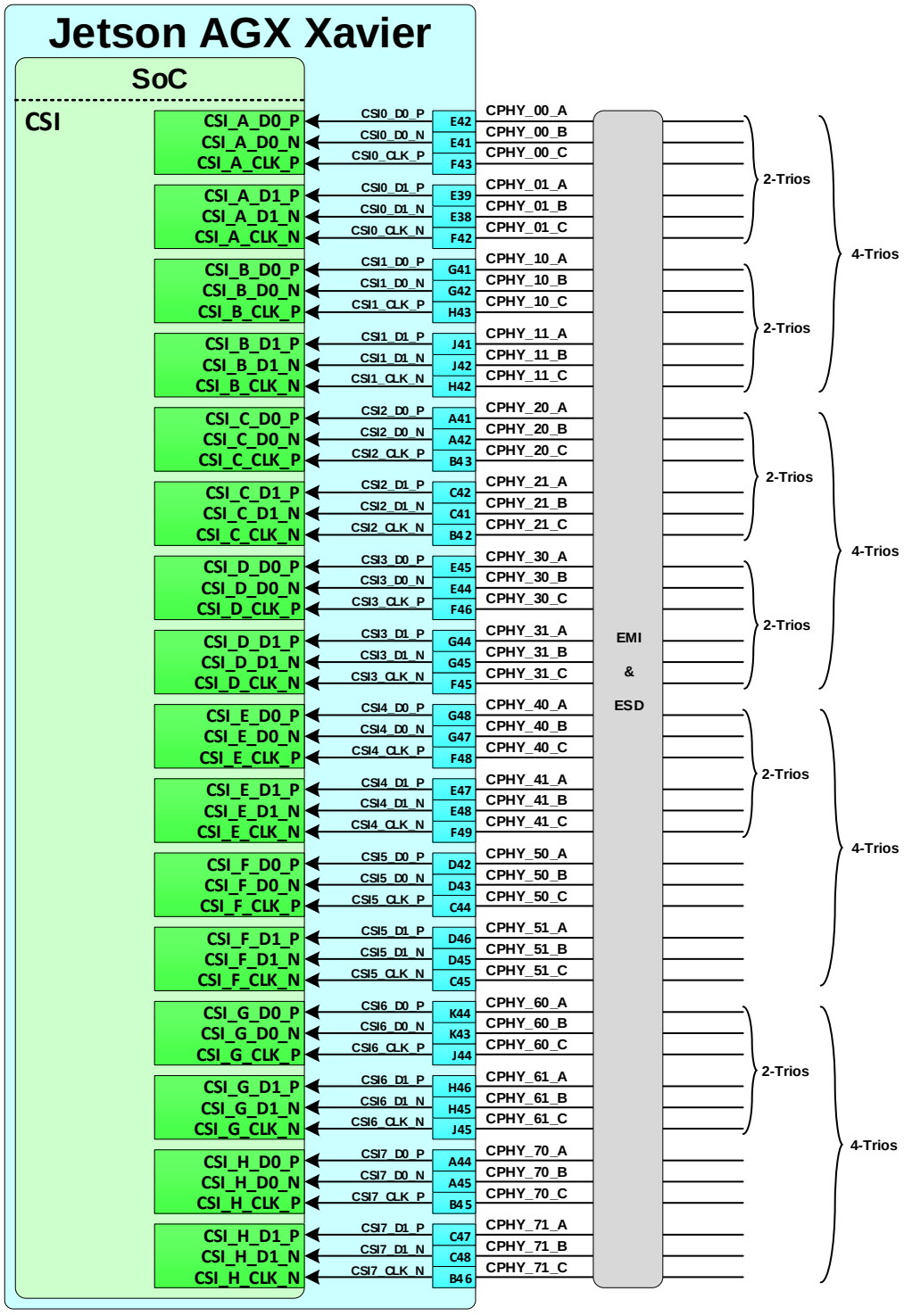
Note: Any EMI/ESD devices must be tuned to minimize impact to signal quality and meet the timing and Vil/Vih requirements at the receiver and maintain signal quality and meet requirements for the frequencies supported by the design.

Figure 10-2. Camera CSI D-PHY Connections



Note: Any EMI/ESD devices must be tuned to minimize impact to signal quality and meet the timing and Vil/Vih requirements at the receiver and maintain signal quality and meet requirements for the frequencies supported by the design.

Figure 10-3. Camera CSI C-PHY Connections



10.1.1 CSI D-PHY Design Guidelines

Table 10-5 details the signal routing requirements for CSI D-PHY interface.

Table 10-5. MIPI CSI D-PHY Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate (per data lane) for High-Speed mode Max Frequency (for Low Power mode)	2.5 10	Gbps MHz	
Number of Loads	1	load	
Max Loading (per pin)	**10**	pF	
Reference plane	GND		
Breakout Region Impedance (Single Ended)	45-50	Ω	±15%
Max PCB breakout delay	48	ps	
Trace Impedance Diff pair / Single Ended	90-100 / 45-50	Ω	
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note 1
Trace spacing - Microstrip / Stripline	2x / 2x	dielectric	
Max Insertion loss 1 Gbps 1.5 Gbps 2.5 Gbps	 3.10 2.96 2.17	 dB	
Max trace delay / length (Stripline/Microstrip) 1 Gbps 1.5 Gbps 2.5 Gbps	 3000 (435) / 2610 (435) 2242 (325) / 1953 (325) 1173 (170) / 1018 (170)	 ps (mm)	
Max Intra-pair Skew	1	ps	See Note 2
Max Trace Delay Skew between **DQ** & **CLK** 1 / 1.5 / 2.5 Gbps	 40/26.7/16	 ps	See Note 2
Noise Coupling Avoidance	Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components		

Notes:

1. Up to 4 signal vias can share a single GND return via
2. If routing to device includes a flex or 2nd PCB, the max trace and skew calculations must include all the PCBs/flex routing

10.1.2 CSI C-PHY Mode Design Guidelines

Table 10-6 details the signal routing requirements for CSI C-PHY interface.

Table 10-6. MIPI CSI C-PHY Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate (per trio)	1.7	Gsps	See note 1 and 2
Topology	Point-Point		With RX Common Mode cap to GND
Termination	Fully ODT (on-die)		50ohms SE to common mode cap
Max Loading (per pin)	2	pF	Single ended
Trace Impedance - Differential / Single Ended	90-100 / 45-50	Ω	±15%
Reference Plane	GND		
Max PCB breakout Length/Delay	5 (30)	mm (ps)	
Via proximity (Signal via to GND return via)	< 2	mm	
Intra Trio Trace spacing - Microstrip / Stripline	2x / 3x	dielectric	Recommendation
Inter Trio Trace spacing - Microstrip / Stripline	2x / 3x	dielectric	Recommend routing with loosely coupled differential impedance.
Max Trace Length total Direct from module conn. to device pins 1.7Gsps 1.3Gsps One conn. between module conn. and device 1.7Gsps 1.3GSps Two conn. between module conn. and device 1.3Gsps	 180 330 100 250 150	mm	
Max Intra-Trio Skew (Within Trios)	3	ps	A or B pin to C pin skew.
Max Inter-Trio Skew (between Trios)	55	ps	
Routing Layer Restrictions	A trio must route completely on the same layer. This means that both Trio0 and Trio1 would need to route on the same layer due to DPHY Compatibility (e.g. D0P/D0N must route on the same layer as CLKP/CLKN and thus so must D1P/D1N)		
Noise Coupling Avoidance	Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components		

Notes:

1. Bit rate in bps is 2.286 * Gsps.
2. Maximum data rate may be limited by use case / memory bandwidth.

Table 10-7. MIPI CSI Signal Connections

Module Pin Name	Type	Termination	Description
CSI[7:0]_CLK+/−	DIFF IN	See note	**CSI Differential Clocks: Connect to clock pins of camera. See the CSI configurations tables for details**
CSI[7:0]_D[1:0]+/−	DIFF IN	See note	**CSI Differential Data Lanes: Connect to data pins of camera. See the CSI configurations tables for details**

Note: Depending on the mechanical design of the platform and camera modules, ESD protection may be necessary. In addition, EMI control may be needed. Both are shown in the Camera Connection Example diagram. Any EMI/ESD solution must be compatible with the frequency required by the design.

Table 10-8. Miscellaneous MIPI Camera Connections

Module Pin Name (Camera Function)	Type	Termination	Description
I2C3_CLK **I2C3_DAT**	O I/O	1kΩ Pull-ups **VDD_1V8** (on Jetson AGX Xavier). See note related to EMI/ESD under MIPI CSI Signal Connections tables.	**Camera I2C Interface: Connect to I2C SCL and SDA pins of imager**
MCLK02 (CAM0 MCLK) **MCLK03 (CAM1 MCLK)** **MCLK04 (CAM2 MCLK)** **MCLK05 (CAM3 MCLK)**	O	See note related to EMI/ESD under MIPI CSI Signal Connections tables.	**Camera Master Clocks:** Connect to Camera reference clock inputs.
GPIO15 (CAM1 PWDN) **UART4_CTS (CAM0 PWDN)**	I/O		**Camera Power Control signals (or GPIOs [1:0])**: Connect to power down pins on camera(s).
GPIO16 (CAM1 RST) **UART4_TX (CAM0 RST)**	O		**Camera Resets:** Connect to reset pin on any cameras with this function.
GPIO25 (VDD_SYS Enable)	O		**Camera VDD_SYS Enable:** Connect to appropriate camera supply.
GPIO36 (AVDD Enable)	O		**Camera AVDD Enable:** Connect to appropriate analog camera supply.

Table 10-9. Recommended CSI Observation Test Points for Initial Boards

Test Points Recommended	Location
One per signal line.	Near Jetson AGX Xavier pins

Note: Test points must be done carefully to minimize signal integrity impact. Avoid stubs and keep pads small and near signal traces.

10.2 SLVS Camera Interface

Jetson AGX Xavier provides an SLVS-EC interface which shares pins with a PCIe x8 interface on the NVHS0_SLVS_RX[7:0] pins of the module.

Note: SLVS is not supported on JAXi.

Table 10-10. Jetson AGX Xavier SLVS EC Camera Pin Description

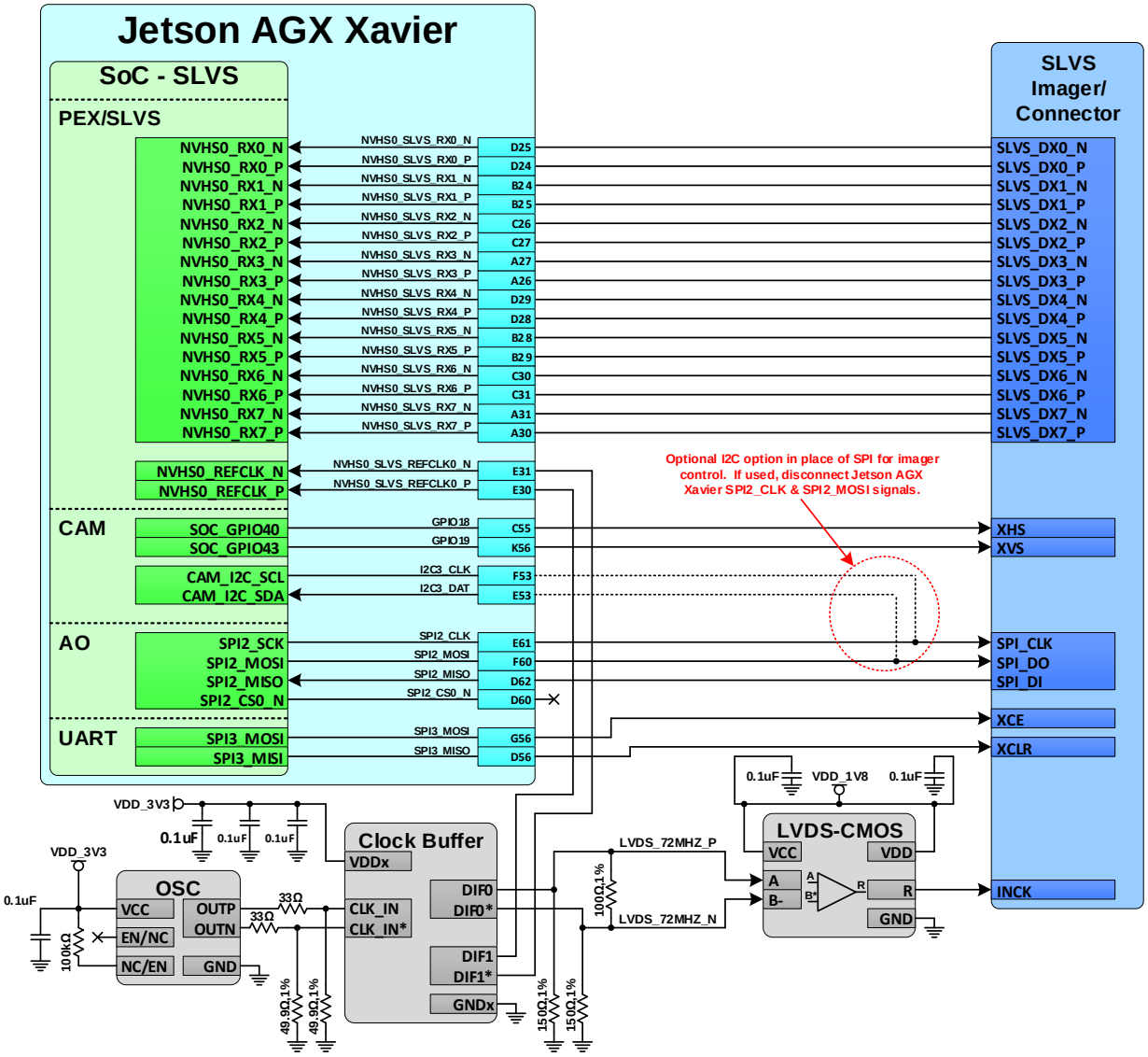
Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
E31	NVHS0_SLVS_REFCLK0_N	NVHS0_REFCLK_N	NVHS Reference Clock 0 used when Jetson AGX Xavier is an Endpoint or when NVHS0_SLVS pins are used for SLVS-EC interface.	PCIe x16 Connector after mux	Input	UPHY/SLVS Diff Pair	–	z
E30	NVHS0_SLVS_REFCLK0_P	NVHS0_REFCLK_P					–	z
D25	NVHS0_SLVS_RX0_N	NVHS0_RX0_N	PCIe/SLVS Receive Lane 0	PCIe x16 Connector	Input	UPHY/SLVS Diff Pair, AC-Coupled on carrier board if PCIe and direct	–	z
D24	NVHS0_SLVS_RX0_P	NVHS0_RX0_P					–	z

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
B24	NVHS0_SLVS_RX1_N	NVHS0_RX1_N	PCIe/SLVS Receive Lane 1			connect to device.	–	z
B25	NVHS0_SLVS_RX1_P	NVHS0_RX1_P					–	z
C26	NVHS0_SLVS_RX2_N	NVHS0_RX2_N	PCIe/SLVS Receive Lane 2				–	z
C27	NVHS0_SLVS_RX2_P	NVHS0_RX2_P					–	z
A27	NVHS0_SLVS_RX3_N	NVHS0_RX3_N	PCIe/SLVS Receive Lane 3				–	z
A26	NVHS0_SLVS_RX3_P	NVHS0_RX3_P					–	z
D29	NVHS0_SLVS_RX4_N	NVHS0_RX4_N	PCIe/SLVS Receive Lane 4				–	z
D28	NVHS0_SLVS_RX4_P	NVHS0_RX4_P					–	z
B28	NVHS0_SLVS_RX5_N	NVHS0_RX5_N	PCIe/SLVS Receive Lane 5				–	z
B29	NVHS0_SLVS_RX5_P	NVHS0_RX5_P					–	z
C30	NVHS0_SLVS_RX6_N	NVHS0_RX6_N	PCIe/SLVS Receive Lane 6				–	z
C31	NVHS0_SLVS_RX6_P	NVHS0_RX6_P					–	z
A31	NVHS0_SLVS_RX7_N	NVHS0_RX7_N	PCIe/SLVS Receive Lane 7				–	z
A30	NVHS0_SLVS_RX7_P	NVHS0_RX7_P					–	z
C55	GPIO18	SOC_GPIO40	SLVS Horizontal sync	PCIe x16 Connector	Output	CMOS – 1.8V (3.3V tolerant)	DD	pd
K56	GPIO19	SOC_GPIO43	SLVS Vertical Sync		Output	CMOS – 1.8V (3.3V tolerant)	DD	pd
K57	PWM01	SOC_GPIO44	SLVS Focus	40-pin Expansion Header	Output	CMOS – 1.8V (3.3V tolerant)	DD	pd
H52	GPIO27	SOC_GPIO54	SLVS Iris		Output	CMOS – 1.8V	ST	pd
D56	SPI3_MISO	SPI3_MISO	GPIO or SLVS XCLR	Unused but connected to TRST* on PCIe x16 connector	Output	CMOS – 1.8V (3.3V tolerant)	DD	pd
G56	SPI3_MOSI	SPI3_MOSI	GPIO or SLVS XCE	Unused, but connected to PEX_WAKE_N on PCIe x16 conn.	Output	CMOS – 1.8V (3.3V tolerant)	DD	pd

Notes:

1. Direct lane mapping (RX[7:0] to DX[7:0] shown in the table. Reverse mapping (RX[7:0] to DX[0:7]) has also been verified.
2. The direction of the control signals in the table are for SLVS usage. If used as GPIOs, they support input or output (bidirectional).
3. In the Type/Dir column, Output is from Jetson AGX Xavier. Input is to Jetson AGX Xavier. Bidir is for Bidirectional signals.
4. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
5. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Figure 10-4. SLVS Connections



Note: Direct lane mapping (RX[7:0] to DX[7:0] shown in Figure 10-4. Reverse mapping (RX[7:0] to DX[0:7]) has also been verified.

10.2.1 SLVS Design Guidelines

Table 10-11 shows the SLVS interface signal routing requirements.

Table 10-11. SLVS Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate	2.4	Gbps	
Max Insertion Loss (SDD21)			
0GHz	-0.88	dB	
1.25GHz	-2.8		
2.5GHz	-4.1		
5.0GHz	-6.6		
Max Return Loss (SDD11)			
0GHz	-25	dB	
1.25GHz	-18		
2.5GHz	-15		
5.0GHz	-10		
Max Crosstalk (PSFEXT)			
0GHz	-50	dB	
1.25GHz	-50		
2.5GHz	-45		
5.0GHz	-45		
Reference plane	GND		
Trace Impedance – Diff pair / Single Ended	85	Ω	±15%
Trace spacing			
Between Differential Pairs	6x	dielectric	
To other signal traces	6x		
Max Intra-pair Skew	4	ps	See Note
Noise Coupling Avoidance	Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components		

Note: If routing to device includes a flex or 2nd PCB, the skew calculations must include all the PCBs/flex routing

Table 10-12. SLVS Camera Signal Connections

Module Pin Name	Type	Termination	Description
NVHS0_SLVS_RX[7:0]_N/P	DIFF IN		SLVS Differential Data Lanes: Connect lanes [7:0] to matching [7:0] pins on SLVS device/connector. Reverse connections ([7:0] to SLVS device/connector [0:7]).
NVHS0_SLVS_REFCLK_N/P	DIFF IN		SLVS Differential Reference Clock: Connect to second output (DIF1 in figure) of a suitable clock buffer.
GPIO18 (XHS)	O		Horizontal Sync: Connect to matching pins of SLVS device/connector
GPIO19 (XVS)	O		Vertical Sync: Connect to matching pins of SLVS device/connector
SPI2_CLK SPI2_MOSI SPI2_MISO	O O I		SPI #2 Clock, Master Out / Slave In and Master In / Slave Out: Connect to matching pins on SLVS device/connector (CLK to CLK, MOSI to MOSI and MISO to MISO)
I2C3_CLK I2C3_DAT	I/OD I/OD		I2C #3: Optional alternative control interface. Connect to matching pins of SLVS device/connector instead of SPI.
SPI3_MOSI (XCE)	O		Chip Enable: Connect to matching pins of SLVS device/connector
SPI3_MISO (XCLR)	O		Clear: Connect to matching pins of SLVS device/connector

Table 10-13. Non-Module SLVS Reference Clock Connections

Function	Type	Termination	Description
OSC_OUTN/P	DIFF OUT	33Ω series resistors and 49.9Ω, 1% pulldowns to GND on each line.	Reference Clock Differential Oscillator Outputs: Connect differential oscillator output to matching pins on differential clock buffer pins.
CLOCK_BUFFER_DIF0	DIFF OUT	150Ω, 1% pulldowns to GND on each line. 100Ω resistor between the P/N lines.	Differential Clock Buffer Output #1: Connect to LVDS-CMOS device inputs.
LVDS-CMOS Output	O		LVDS-CMOS converter output: Connect to SLVS device/connector input clock (INCK in figure)

Chapter 11. SDIO and SD Card

Jetson AGX Xavier has two SD/MMC interfaces. One is used on Jetson AGX Xavier for eMMC for boot and storage and one is brought to the connector pins for SD Card or SDIO use.

Table 11-1. SDIO, SD Card, and eMMC Interface Mapping

Module Pins	SoC Interface	Width	Usage
SDCARD_CLK	SDMMC1	4-bit	Micro SD / UFS Card socket
na	SDMMC4	8-bit	eMMC device on Module

Table 11-2. Jetson AGX Xavier SDMMC Pin Descriptions

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
B6	SDCARD_CLK	SDMMC1_CLK	SD Card (or SDIO) Clock	Micro SD / UFS Card Socket	Output	CMOS – 3.3V/1.8V	CZ	pd
A5	SDCARD_CMD	SDMMC1_CMD	SD Card (or SDIO) Command		Bidir		CZ	pd
E8	SDCARD_D0	SDMMC1_DAT0	SD Card (or SDIO) Data 0				CZ	pd
F8	SDCARD_D1	SDMMC1_DAT1	SD Card (or SDIO) Data 1				CZ	pd
A4	SDCARD_D2	SDMMC1_DAT2	SD Card (or SDIO) Data 2				CZ	pd
D6	SDCARD_D3	SDMMC1_DAT3	SD Card (or SDIO) Data 3				CZ	pd
B58	GPIO21	DAP6_SCLK	GPIO	SD Power Switch On	Output	CMOS – 3.3V	CZ	pd
L6	GPIO02	SOC_GPIO11	GPIO	SD Card socket (SD Detect)	Bidir	CMOS – 1.8V	ST	pd

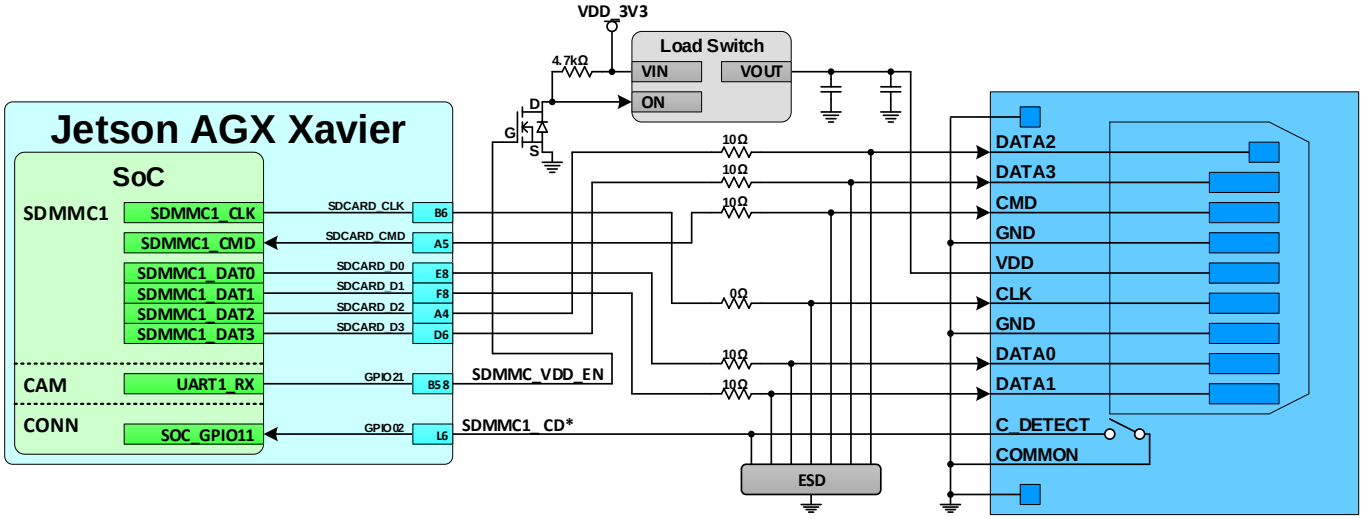
Notes:

1. In the Type/Dir column, Output is from Jetson AGX Xavier. Input is to Jetson AGX Xavier. Bidir is for Bidirectional signals.
2. The direction shown in the table above for SDCard_CLK and GPIO21 is true when used for those functions. If used as a GPIO, the pin supports input or output (bidirectional).
3. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
4. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

11.1 SD Card

Figure 11-1 shows a Micro SD card socket connection example. Internal pull-up resistors are used for SDCARD Data/CMD lines. External pull-ups are not required and cannot be used due to the internal pad voltage selection.

Figure 11-1. Micro SD Card Socket Connection Example



Notes:

1. If EMI and/or ESD devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing and Vil/Vih requirements at the receiver and maintain signal quality and meet requirements for the frequencies supported by the design.
2. Supply (load switch, etc) used to provide power to the SD Card must be current limited if the supply is shorted to GND.

Table 11-3. SDCARD Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency 3.3V Signaling			See Note 1
DS	25 (12.5)	MHz (MB/s)	
HS	50 (25)		
Max Frequency 1.8V Signaling			
SDR12	25 (12.5)		
SDR25	50 (25)		
SDR50	100 (50)		
SDR104	208 (104)		
DDR50	50 (50)		
Topology	Point to point		
Reference plane	**GND** or **PWR**		See Note 2
Trace Impedance	50	Ω	±15%. 45Ω optional depending on stack-up

Parameter	Requirement	Units	Notes
Max Via Count PTH HDI	 **4** **10**		Independand of stackup layers Depends on stackup layers
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	Up to 4 signal Vias can share 1 **GND** return Via
Trace spacing – Microstrip / Stripline	4x / 3x	dielectric	
Trace length SDR50 / SDR25 / SDR12 / HS / DS Min Max SDR104 / DDR50 Min Max	 **16 (100)** **139 (876)** **16 (100)** **83 (521)**	 mm (ps)	
Max Trace Delay Skew in/between **CLK** and **CMD/DAT** SDR50 / SDR25 / SDR12 / HS / DS SDR104 / DDR50	 14 (87.5) 2 (12.5)	 Mm (ps)	See Note 3
Noise Coupling Avoidance	Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components		

Notes:

1. Actual frequencies may be lower due to clock source/divider limitations.
2. If PWR, 0.01uF decoupling cap required for return current.
3. If routing to SD Card socket includes a flex or 2nd PCB, max trace and skew calculations must include PCB and flex routing.

Table 11-4. SD Card Loading vs. Drive Type

General SD Card Compliance	Parameter	Value	Units	Notes
C_{CARD} (C_{DIE}+C_{PKG})	Min	5	pF	Spec best case value
	Max	10	pF	Spec worst case value
Drive Type	A	33	Ω	UHS50 Card = optional, UHS104 Card = mandatory
	B	50	Ω	UHS50 Card = mandatory, UHS104 Card = mandatory
	C	66	Ω	UHS50 Card = optional, UHS104 Card = mandatory
	D	100	Ω	UHS50 Card = optional, UHS104 Card = mandatory
F_{MAX} (CLK base frequency)	SDR104	208	MHz	Single data rate up to 104MB/sec
	DDR50	50	MHz	Double data rate up to 50MB/sec
	SDR50	100	MHz	Single data rate up to 50MB/sec
	SDR25	50	MHz	Single data rate up to 25MB/sec
	SDR12	25	MHz	Single data rate up to 12.5MB/sec
	HS	50	MHz	Single data rate up to 25MB/sec
	DS	25	MHz	Single data rate up to 12.5MB/sec
C_{LOAD} (C_{CARD}+C_{EQ}) (CLK freq = 208MHz)	Drive Type = A	21	pF	Total load capacitance supported
	Drive Type = B	15	pF	Total load capacitance supported
	Drive Type = C	11	pF	Total load capacitance supported
	Drive Type = D	22	pF	Possibly 22pF+ depending on host system
C_{LOAD} (C_{CARD}+C_{EQ}) (CLK freq = 100/50/25MHz)	Drive Type = A	43	pF	Total load capacitance supported
	Drive Type = B	30	pF	Total load capacitance supported
	Drive Type = C	23	pF	Total load capacitance supported
	Drive Type = D	22	pF	Possibly 22pF+ depending on host system

Table 11-5. SDCARD Signal Connections

Function Signal Name	Type	Termination	Description
SDCARD_CLK	O	See note for EMI/ESD	SDIO/SD Card Clock: Connect to CLK pin of device or socket
SDCARD_CMD	I/O	See note for EMI/ESD	SDIO/SDMMC Command: Connect to CMD pin of device/socket
SDCARD_D[3:0]	I/O		SDIO/SDMMC Data: Connect to Data pins of device or socket
GPIO02 (SDCARD_CD#)	I		SDIO Card Detect: Connect to CD/C_DETECT pin on socket if required.
GPIO21 (SDCARD_VDD_EN)	O		SDIO Supply/Load Switch Enable: Connect to enable of supply/load switch supplying VDD on SD Card socket.

Note: EMI/ESD may be required for SDIO when used as the SD Card socket interface. Any EMI/ESD device used must be able to meet signal timing/quality requirements.

Table 11-6. Recommended SDCARD Observation Test Points for Initial Boards

Test Points Recommended	Location
One for SDCARD_CLK line.	Near Device/Connector pin. SD connector pin can be used for device end if accessible.
One SDCARD_DATx line and one for SDCARD_CMD.	Near Jetson AGX Xavier and Device pins. SD connector pin can be used for device end if accessible.

Chapter 12. Audio

Jetson AGX Xavier brings several PCM/I2S audio interfaces to the module pins and includes a flexible audio-port switching architecture. In addition, digital microphone and speaker interfaces are provided.

Table 12-1. Jetson AGX Xavier Audio Pin Description

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
H9	MCLK01	AUD_MCLK	Audio Codec Master Clock	Audio Codec	Output	CMOS – 1.8V	ST	pd
D61	I2C4_CLK	GEN8_I2C_SCL	General I2C 4 Clock	Audio Codec & Camera Connector	Bidir	Open-Drain – 1.8V	DD	z
E60	I2C4_DAT	GEN8_I2C_SDA	General I2C 4 Data				DD	z
L14	I2S1_CLK	DAP1_SCLK	I2S Audio Port 1 Clock	Audio Codec	Bidir	CMOS – 1.8V	ST	pd
D8	I2S1_FS	DAP1_FS	I2S Audio Port 1 Left/Right Clock	Audio Codec	Bidir		ST	pd
H8	I2S1_SDIN	DAP1_DIN	I2S Audio Port 1 Data In	Audio Codec	Input		ST	pd
C7	I2S1_SDOUT	DAP1_DOUT	I2S Audio Port 1 Data Out	Audio Codec	Output		ST	pd
G4	I2S2_CLK	DAP2_SCLK	I2S Audio Port 2 Clock	BT Audio	Bidir		ST	pd
F6	I2S2_DIN	DAP2_DIN	I2S Audio Port 2 Data In	BT Audio	Input		ST	pd
F5	I2S2_DOUT	DAP2_DOUT	I2S Audio Port 2 Data Out	BT Audio	Output		ST	pd
E4	I2S2_FS	DAP2_FS	I2S Audio Port 2 Left/Right Clock	BT Audio	Bidir		ST	pd
J59	I2S3_DIN	DAP4_DIN	I2S Audio Port 3 Data In	M.2 Key E	Input	CMOS – 3.3V	CZ	pd
K59	I2S3_DOUT	DAP4_DOUT	I2S Audio Port 3 Data Out	M.2 Key E	Output		CZ	pd
C60	I2S3_FS	DAP4_FS	I2S Audio Port 3 Left/Right Clock	M.2 Key E	Bidir		CZ	pd
C59	I2S3_SCLK	DAP4_SCLK	I2S Audio Port 3 Clock	M.2 Key E	Bidir		CZ	pd
B58	GPIO21	DAP6_SCLK	JAX: I2S Audio Port 6 Clock JAXi: No I2S support. GPIO only.	Not assigned	Bidir		CZ	pd
A58	GPIO20	DAP6_FS	JAX: I2S Audio Port 6 Left/Right Clock JAXi: No I2S support. GPIO only.	Not assigned	Bidir		CZ	pd
A59	GPIO05	DAP6_DOUT	JAX: I2S Audio Port 6 Data Out JAXi: Not supported. Pin pulled low on the module.	Not assigned	Output		CZ	pd
B59	GPIO04	DAP6_DIN	JAX: I2S Audio Port 6 Data In JAXi: No I2S support. GPIO only.	Not assigned	Input		CZ	pd
B8	GPIO11	SOC_GPIO30	GPIO	Audio Codec Interrupt	Bidir	CMOS – 1.8V	ST	pd
B62	GPIO08	CAN1_STB	GPIO / Digital Mic Input Data	Expansion Connector (AO DMIC In Data)	Bidir	CMOS – 3.3V	CZ	pd
C61	GPIO09	CAN1_EN	GPIO / Digital Mic Input Clock	Expansion Connector (AO DMIC In Clock)	Bidir		CZ	Z
F10	GPIO15	DAP5_SCLK	GPIO / Digital Speaker Output Clock	Camera Connector (Camera 1 Powerdown)	Bidir	CMOS – 1.8V	ST	pd

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
F9	GPIO16	DAP5_DOUT	GPIO / Digital Speaker Output Data	Camera Connector (Camera 1 Reset)	Output		ST	Pd

Notes:

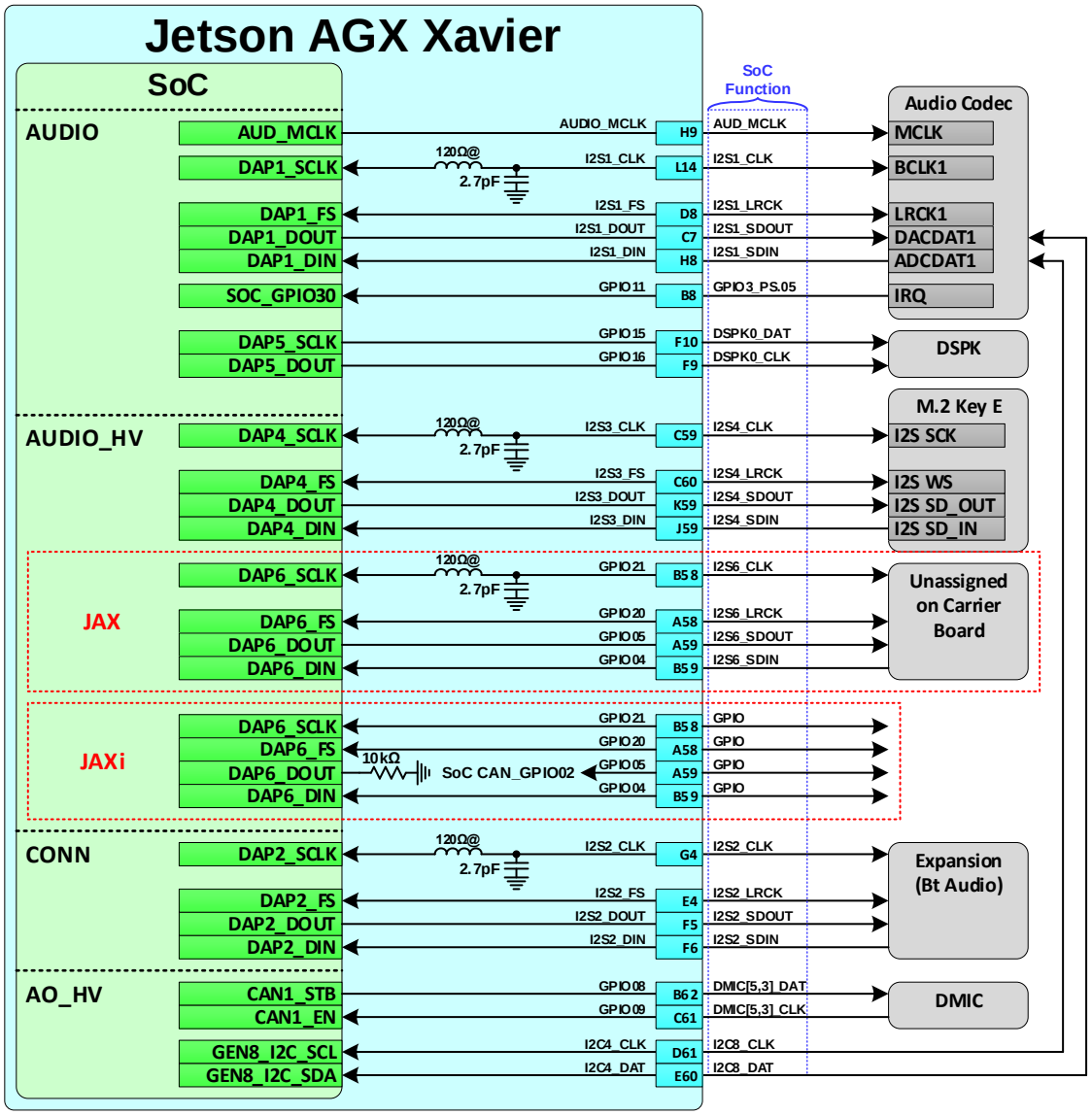
1. In the Type/Dir column, Output is from Jetson AGX Xavier. Input is to Jetson AGX Xavier. Bidir is for Bidirectional signals.
2. The direction indicated for MCLKx, I2Sx, and GPIOx are associated with their use as I2S or MCLK signals. The pins support GPIO functionality, so support both input and output operation (bidirectional).
3. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
4. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

When possible, the following assignments should be used for the I2Sx interfaces.

Table 12-2. I2S Interface Mapping

Module Pins (SoC Functions)	Xavier I/O Block	Typical Usage (Usage on NVIDIA Carrier Board)
I2S1 (I2S1)	AUDIO	Audio Codec
I2S2 (I2S2)	CONN	Bt Audio
I2S3 (I2S4)	AUDIO_HV	M.2 Key E
JAX: GPIO[21:20,05:04] (I2S6) JAXi: Only GPIO support on GPIO[04,20,21]. I2S6 Data Out not brought out (tied low on module)	AUDIO_HV	Unassigned

Figure 12-1. Audio Device Connections



Notes: The I2S interfaces can be used in either Master or Slave mode.

A capacitor from DAPn_FS to GND should be included if SoC an I2S slave and the edge_cntrl configuration = 1 (SDATA driven on positive edge of SCLK). The value of the capacitor should be chosen to provide a minimum of 2ns hold time for the DAPn_FS edge after the rising edge of DAPn_SCLK.

12.1.1 I2S Design Guidelines

The following table details the signal routing requirements for the I2S interface.

Table 12-3. I2S Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Configuration / Device Organization	1	load	
Max Loading	8	pF	
Reference plane	GND		
Breakout Region Impedance	Min width/spacing		
Trace Impedance	50	Ω	±20%
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note 1
Trace spacing - Microstrip or Stripline	2x	dielectric	
Max Trace Delay	3600 (~22)	ps (in)	
Max Trace Delay Skew between **SCLK** and SDATA_**OUT/IN**	250 (~1.6")	ps (in)	

Note: Up to 4 signal Vias can share a single GND return Via

Table 12-4. I2S and Miscellaneous Codec Signal Connections

Module Pin Name (Xavier Function)	Type	Termination	Description
I2S1_SCLK (I2S1_CLK) I2S2_SCLK (I2S2_CLK) I2S3_SCLK (I2S4_CLK) JAX: GPIO21 (I2S6_CLK) JAXi: No I2S support. GPIO only.	I/O	120Ω Bead in series and 2.7pF capacitor to GND (on Jetson AGX Xavier).	I2S Serial Clock: Connect to I2S/PCM CLK pin of audio device.
I2S1_FS (I2S1_LRCK) I2S2_FS (I2S2_LRCK) I2S3_FS (I2S4_LRCK) JAX: GPIO20 (I2S6_LRCK) JAXi: No I2S support. GPIO only.	I/O		I2S Left/Right Clock: Connect to Left/Right Clock pin of audio device.
I2S1_DOUT (I2S1_SDOUT) I2S2_DOUT (I2S2_SDOUT) I2S3_DOUT (I2S4_SDOUT) JAX: GPIO05 (I2S6_SDOUT) JAXi: No I2S support. GPIO05 connected to CAN0_GPIO02 on module.	I/O		I2S Data Output: Connect to Data Input pin of audio device.

Module Pin Name (Xavier Function)	Type	Termination	Description
I2S1_DIN (I2S1_SDIN) I2S2_DIN (I2S2_SDIN) I2S3_DIN (I2S4_SDIN) JAX: GPIO04 (I2S6_SDIN) JAXi: No I2S support. GPIO only.	I		I2S Data Input: Connect to Data Output pin of audio device.
AUD_MCLK	O		Audio Codec Master Clock: Connect to clock pin of Audio Codec.
GPIO20_AUD_INT	I		Audio Interrupt: Connect to interrupt pin of Audio Codec.

12.1.2 DMIC Design Guidelines

The following table details the signal routing requirements for the DMIC interface.

Table 12-5. DMIC Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Clock Frequency/Period	12/83.33	MHz/ns	
Data Bit-rate/Period (DDR24)	24/41.66	Mbps/ns	
Configuration / Device Organization	1	load	
Topology	Point to Point		
Reference plane	**GND**		
Trace Impedance	45-50	Ω	±20%
Via proximity (Signal via to GND return via)	< 3.8 (24)	mm (ps)	See Note
Trace spacing – Microstrip / Stripline	2x / 2x	dielectric	
Max Trace Delay	1280	ps	
Max Trace Delay Skew between **CLK** and **DAT**	150	ps	

Note: Up to 4 signal vias can share a single GND return via.

Table 12-6. DMIC Signal Connections

Module Pin Name (Xavier Function)	Type	Termination	Description
GPIO09 (DMIC[5 or 3]_CLK)	O		Digital Microphone Clock: Connect to clock pin of DMIC device
GPIO08 (DMIC[5 or 3]_DAT)	I		Digital Microphone Data: Connect to data pin of DMIC device

Chapter 13. Miscellaneous Interfaces

13.1 I2C

The SoC has nine I2C controllers. Jetson AGX Xavier brings eight of the I2C interfaces out, which are shown in the following tables. The assignments in Table 13-2 should be used for the I2C interfaces:

Table 13-1. Jetson AGX Xavier I2C Pin Description

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
K5	I2C1_CLK	GEN1_I2C_SCL	General I2C 1 Clock	ID EEPROM	Bidir	Open-Drain – 1.8V	DD	z
L8	I2C1_DAT	GEN1_I2C_SDA	General I2C 1 Data				DD	z
J61	I2C2_CLK	GEN2_I2C_SCL	General I2C 2 Clock	Various			DD	z
K61	I2C2_DAT	GEN2_I2C_SDA	General I2C 2 Data				DD	z
F53	I2C3_CLK	CAM_I2C_SCL	General I2C 3 Clock	Camera Connector			DD	z
E53	I2C3_DAT	CAM_I2C_SDA	General I2C 3 Data				DD	z
D61	I2C4_CLK	GEN8_I2C_SCL	General I2C 4 Clock	Audio Codec and Camera Connector			DD	z
E60	I2C4_DAT	GEN8_I2C_SDA	General I2C 4 Data				DD	z
A53	I2C5_CLK	DP_AUX_CH3_P	General I2C 5 Clock	Expansion Connector			DD	z
C53	I2C5_DAT	DP_AUX_CH3_N	General I2C 5 Data				DD	z
F51	DP0_AUX_CH_N	DP_AUX_CH0_N	DisplayPort 0 Aux– or HDMI DDC SDA	USB Type C Conn. J512 (via Alt Mode Switch)		AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC/I2C)	DP_AUX	z
F52	DP0_AUX_CH_P	DP_AUX_CH0_P	DisplayPort 0 Aux+ or HDMI DDC SCL				DP_AUX	z
J53	DP1_AUX_CH_N	DP_AUX_CH1_N	DisplayPort 1 Aux– or HDMI DDC SDA	USB Type C Conn. J513 (via Alt Mode Switch)			DP_AUX	z
J52	DP1_AUX_CH_P	DP_AUX_CH1_P	DisplayPort 1 Aux+ or HDMI DDC SCL				DP_AUX	z
G54	DP2_AUX_CH_N	DP_AUX_CH2_N	DisplayPort 2 Aux– or HDMI DDC SDA	HDMI Connector			DP_AUX	z
G53	DP2_AUX_CH_P	DP_AUX_CH2_P	DisplayPort 2 Aux+ or HDMI DDC SCL				DP_AUX	Z

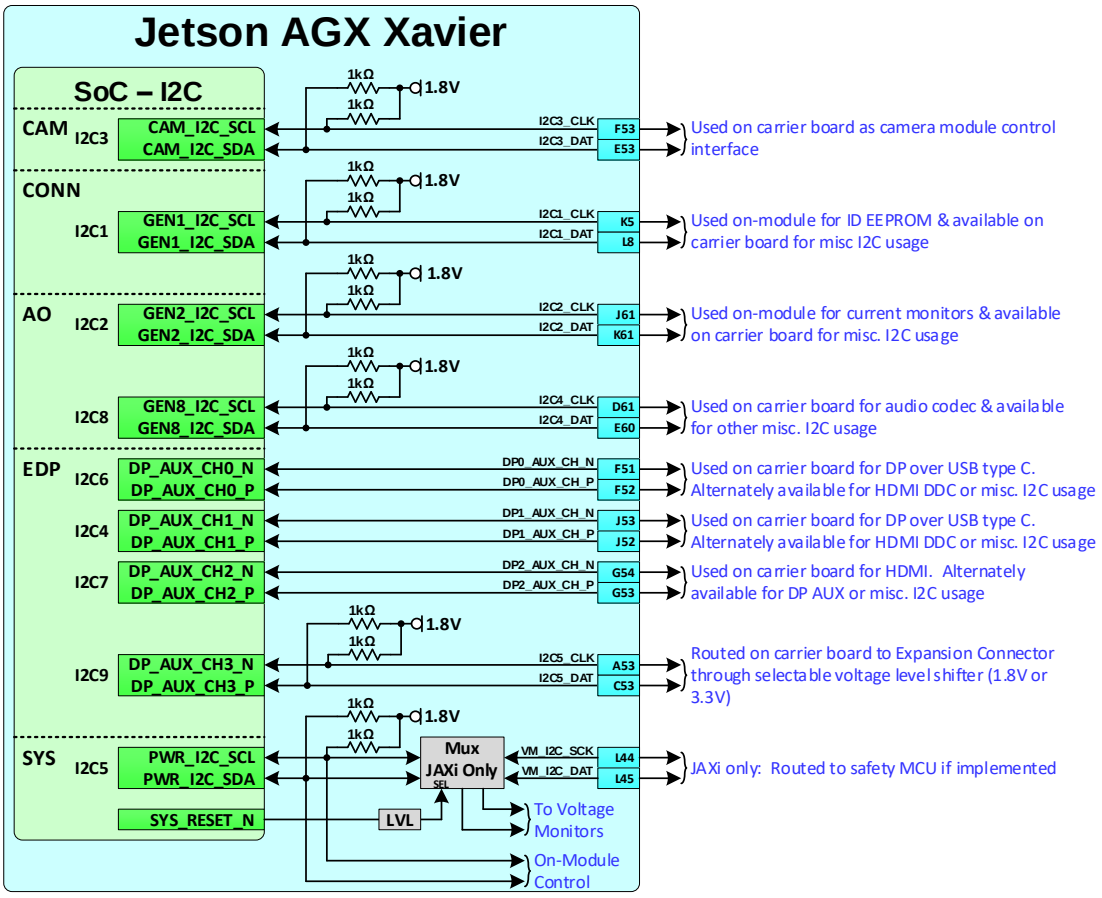
Notes:

1. In the Type/Dir column, Output is from Jetson AGX Xavier. Input is to Jetson AGX Xavier. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Table 13-2. I2C Interface Mapping

Ctrlr	Module Pin Names (Xavier Pins)	Usage on Module	Xavier Block	On-Module Pull-up/voltage
I2C1	I2C1_CLK/DAT	ID EEPROM (7h50)	CONN	1KΩ to 1.8V
I2C2	I2C2_CLK/DAT	Current Monitors (7H40 and 7H41)	AO	1KΩ to 1.8V
I2C3	I2C3_CLK/DAT		CAM	1KΩ to 1.8V
I2C4	DP1_AUX_CH_N/P		EDP	1KΩ to 1.8V
I2C5	(PWR_I2C_SCL/SDA) On-module only	System control. On JAXi only, routed to mux with VM_I2C. Output of mux controls to voltage monitors. VM_I2C controls monitors when Xavier reset is low. PWR_I2C when reset is high.	SYS	1KΩ to 1.8V
I2C6	DP0_AUX_CH_N/P		EDP	None
I2C7	DP2_AUX_CH_N/P		EDP	None
I2C8	I2C4_CLK/DAT		AO	1KΩ to 1.8V
I2C9	I2C5_CLK/DAT		EDP	1KΩ to 1.8V
na	VM_I2C_SCK_DAT	See I2C5 row Usage on Module description.	na	None

Figure 13-1. I2C Connections



Note: If I2C interfaces are routed to M.2 Key E or Key M connectors, it is recommended that 0Ω series resistors be included to allow these to be disconnected. Some M.2 Key E and Key M cards can cause conflicts with other devices connected to the I2C interfaces.

13.1.1 I2C Design Guidelines

Care must be taken to ensure I2C peripherals on same I2C bus connected to Jetson AGX Xavier do not have duplicate addresses. Addresses can be in two forms: 7-bit, with the Read/Write bit removed or 8-bit including the Read/Write bit. Be sure to compare I2C device addresses using the same form (all 7-bit or all 8-bit format).

Table 13-3. I2C Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency - Standard-mode / Fm / Fm+	100 / 400 / 1000	kHz	See Note 1
Topology	Single ended, bi-directional, multiple masters/slaves		
Max Loading - Standard-mode / Fm / Fm+	400	pF	Total of all loads
Reference plane	**GND** or **PWR**		
Trace Impedance	50 – 60	Ω	±15%
Trace Spacing	1x	dielectric	
Max Trace Delay Standard Mode Fm & Fm+	 3400 (~20) 1700 (~10)	 ps (in)	

Notes:

1. Fm = Fast-mode, Fm+ = Fast-mode Plus
2. Avoid routing I2C signals near noisy traces, supplies or components such as a switching power regulator.
3. No requirement for decoupling caps for PWR reference

Table 13-4. I2C Signal Connections

Module Pin Name	Type	Termination	Description
I2C1_CLK/DAT	I/OD	1kΩ pull-ups to 1.8V on module	**General I2C 1 Clock\Data. Connect to CLK/Data pins of 1.8V devices**
I2C2_CLK/DAT	I/OD	1kΩ pull-ups to 1.8V on module	**General I2C 2 Clock\Data. Connect to CLK/Data pins of 1.8V devices.**
I2C3_CLK/DAT	I/OD	1kΩ pull-ups to 1.8V on module	**General I2C 3 Clock\Data. Connect to CLK/Data pins of 1.8V devices**
I2C4_CLK/DAT	I/OD	1kΩ pull-ups to 1.8V on module	**General I2C 4 Clock\Data. Connect to CLK/Data pins of 1.8V devices.**
I2C5_CLK/DAT	I/OD	1kΩ pull-ups to 1.8V on module	**General I2C 5 Clock\Data. Connect to CLK/Data pins of 1.8V devices.**
DP0_AUX_CH_P/N	I/OD	See eDP/HDMI/DP sections for correct termination	**DP_AUX Channel (eDP/DP) or DDC I2C 2 Clock and Data (HDMI). Connect to AUX_CH_P/N** (DP) or **SCL/SDA** (HDMI). Alternately available as I2C IF.
DP1_AUX_CH_P/N	I/OD	See eDP/HDMI/DP sections for correct termination	**DP_AUX Channel (eDP/DP) or DDC I2C 2 Clock and Data (HDMI). Connect to AUX_CH_P/N** (DP) or **SCL/SDA** (HDMI). Alternately available as I2C IF.
DP2_AUX_CH_P/N	I/OD	See eDP/HDMI/DP sections for correct termination	**DP_AUX Channel (eDP/DP) or DDC I2C 2 Clock and Data (HDMI). Connect to AUX_CH_P/N** (DP) or **SCL/SDA** (HDMI). Alternately available as I2C IF.
VM_I2C_CLK/DAT (JAXi only)	I/OD	1kΩ pull-ups to 1.8V on module	**Voltage Monitor I2C Clock\Data. Connects to safety MCU CLK/Data pins if implemented.**

Notes:

1. If some devices require a different voltage level than others connected to the same I2C bus, level shifters are required.
2. For I2C interfaces that are pulled up to 1.8V, disable the E_IO_HV option for these pads. For I2C interfaces that are pulled up to 3.3V, enable the E_IO_HV option. The E_IO_HV option is selected in the Pinmux registers.

13.1.2 De-bounce

The following table contain the allowable De-bounce settings for the various I2C modes.

Table 13-5. De-bounce Settings – Fast Mode Plus, Fast Mode, and Standard Mode

I2C Mode	Clock Source	Source Clock Freq	I2C Source Divisor	Sm/Fm Divisor	De-bounce Value	I2C SCL Freq
Fm+	PLLP_OUT0	408MHz	5 (0x04)	10 (0x9)	0	1016KHz
					5:1	905.8KHz
					7:6	816KHz
Fm	PLLP_OUT0	408MHz	5 (0x4)	26 (0x19)	7:0	392KHz
Sm	PLLP_OUT0	408MHz	20 (0x13)	26 (0x19)	7:0	98KHz

Note: sm = standard mode

13.2 SPI

Jetson AGX Xavier brings out three of the SoC SPI interfaces. For JAXi, SPI2 is routed to the safety MCU if implemented.

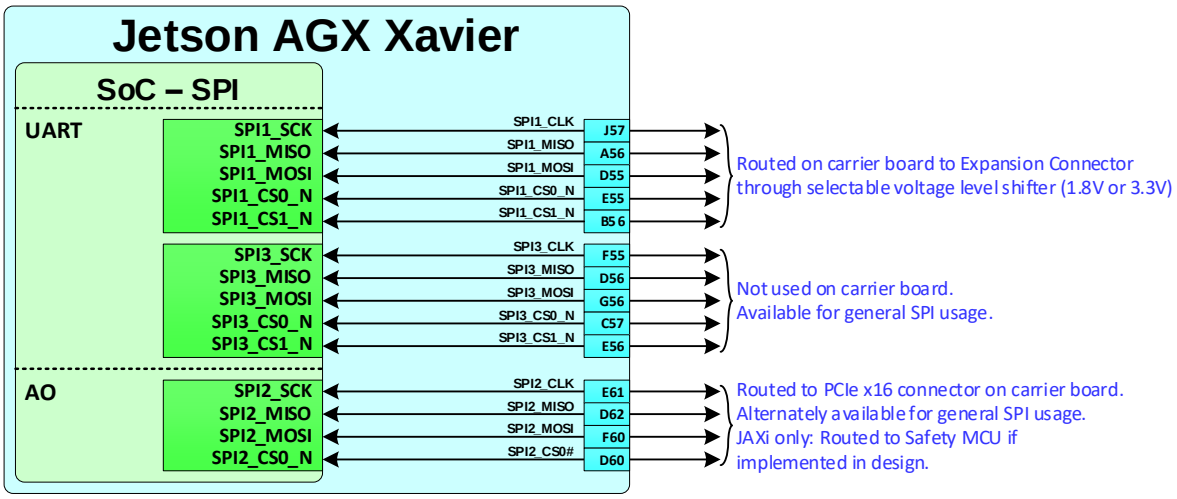
Table 13-6. Jetson AGX Xavier SPI Pin Description

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Codes	Power-on Reset
J57	SPI1_CLK	SPI1_SCK	SPI 1 Clock	Expansion Connector	Bidir	CMOS – 1.8V	ST	pd
E55	SPI1_CS0_N	SPI1_CS0	SPI 1 Chip Select 0				ST	pu
B56	SPI1_CS1_N	SPI1_CS1	SPI 1 Chip Select 1				ST	pu
A56	SPI1_MISO	SPI1_MISO	SPI 1 Master In / Slave Out				ST	pu
D55	SPI1_MOSI	SPI1_MOSI	SPI 1 Master Out / Slave In				ST	pu
E61	SPI2_CLK	SPI2_SCK	SPI 2 Clock (see note 5)	PCIe x16 Connector			DD	pd
D60	SPI2_CS0_N	SPI2_CS0	SPI 2 Chip Select 0				DD	z
D62	SPI2_MISO	SPI2_MISO	SPI 2 Master In / Slave Out				DD	pd
F60	SPI2_MOSI	SPI2_MOSI	SPI 2 Master Out / Slave In				DD	pd
F55	SPI3_CLK	SPI3_SCK	SPI 3 Clock	Not used			DD	pd
C57	SPI3_CS0_N	SPI3_CS0	SPI 3 Chip Select 0				DD	z
E56	SPI3_CS1_N	SPI3_CS1	SPI 3 Chip Select 1				DD	z
D56	SPI3_MISO	SPI3_MISO	SPI 3 Master In / Slave Out	PCIe x16 Connector (SLVS_XCLR)			DD	pd
G56	SPI3_MOSI	SPI3_MOSI	SPI 3 Master Out / Slave In	PCIe x16 Connector (SLVS_XCE)			DD	pd

Notes:

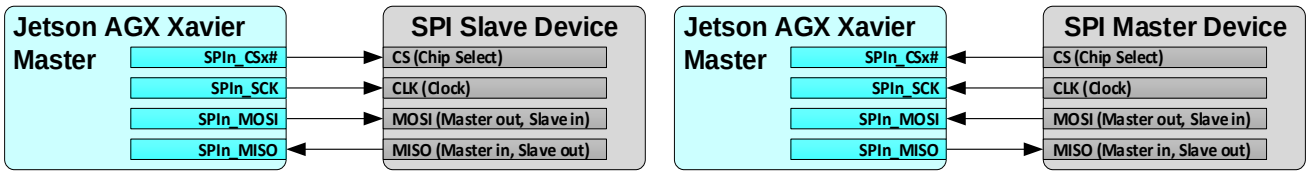
1. The Direction depends on whether Xavier is the master or slave. If Xavier is master, the clock, chip select and MOSI are outputs and MISO is an input. If Xavier is slave, the clock, chip select and MOSI are inputs and MISO is an output.
2. In the Type/Dir column, Output is from Jetson AGX Xavier. Input is to Jetson AGX Xavier. Bidir is for Bidirectional signals.
3. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
4. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.
5. JAXi only: SPI2 routed to safety MCU if implemented in design.

Figure 13-2. SPI Connections



The following figure shows the basic SPI connections.

Figure 13-3. Basic SPI Master and Slave Connections



13.2.1 SPI Design Guidelines

The following figures show the SPI topologies.

Figure 13-4. SPI Point-Point Topology

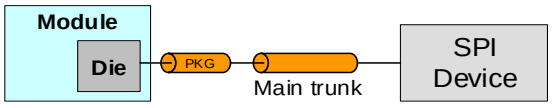


Figure 13-5. SPI Star Topologies

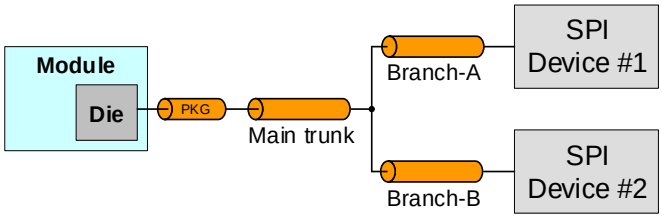


Figure 13-6. SPI Daisy Topologies

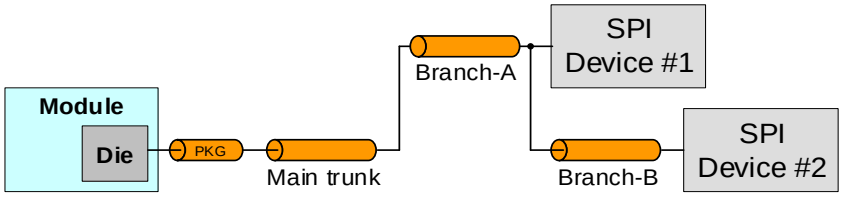


Table 13-7. SPI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency	65	MHz	
Configuration / Device Organization	3	load	
Max Loading (total of all loads)	15	pF	
Reference plane	GND		
Breakout Region Impedance	Minimum width & spacing		
Max PCB breakout delay	75	ps	
Trace Impedance	50 – 60	Ω	±15%
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note
Trace spacing - Microstrip / Stripline	4x / 3x	dielectric	
Max Trace Length/Delay (PCB Main Trunk) For **MOSI, MISO, SCK** and **CS** Point-Point 2x-Load Star/Daisy	 125 (787) 50 (314)	 mm (ps)	
Max Trace Length/Delay (Branch-A) for **MOSI, MISO, SCK** and **CS:** 2x-Load Star/Daisy	75 (472)	mm (ps)	
Max Trace Length/Delay (Branch-B) for **MOSI, MISO, SCK** and **CS:** 2x-Load Star/Daisy	75 (472)	mm (ps)	
Max Trace Length/Delay Skew from **MOSI, MISO** and **CS** to **SCK**	16 (100)	mm (ps)	At any point

Note: Up to 4 signal vias can share a single GND return via.

Table 13-8. SPI Signal Connections

Module Pin Names	Type	Termination	Description
SPI[3:1]_CLK	I/O		**SPI Clock.: Connect to Peripheral CLK pin(s)**
SPI[3:1]_MOSI	I/O		**SPI Data Output: Connect to Slave Peripheral MOSI pin(s)**
SPI[3:1]_MISO	I/O		**SPI Data Input: Connect to Slave Peripheral MISO pin(s)**
SPI[3:1]_CS[1:0]_N, SPI2_CS0_N	I/O		**SPI Chip Selects.: Connect one CS_N pin per SPI IF to each Slave Peripheral CS pin**

Note: JAXi only: SPI2 routed to safety MCU if implemented in design

Table 13-9. Recommended SPI Observation Test Points for Initial Boards

Test Points Recommended	Location
One for each SPI signal line used	Near Jetson AGX Xavier and Device pins.

13.3 UART

Jetson AGX Xavier brings five UARTs out to the main connector. See Figure 13-7 for typical assignments of the UARTs.

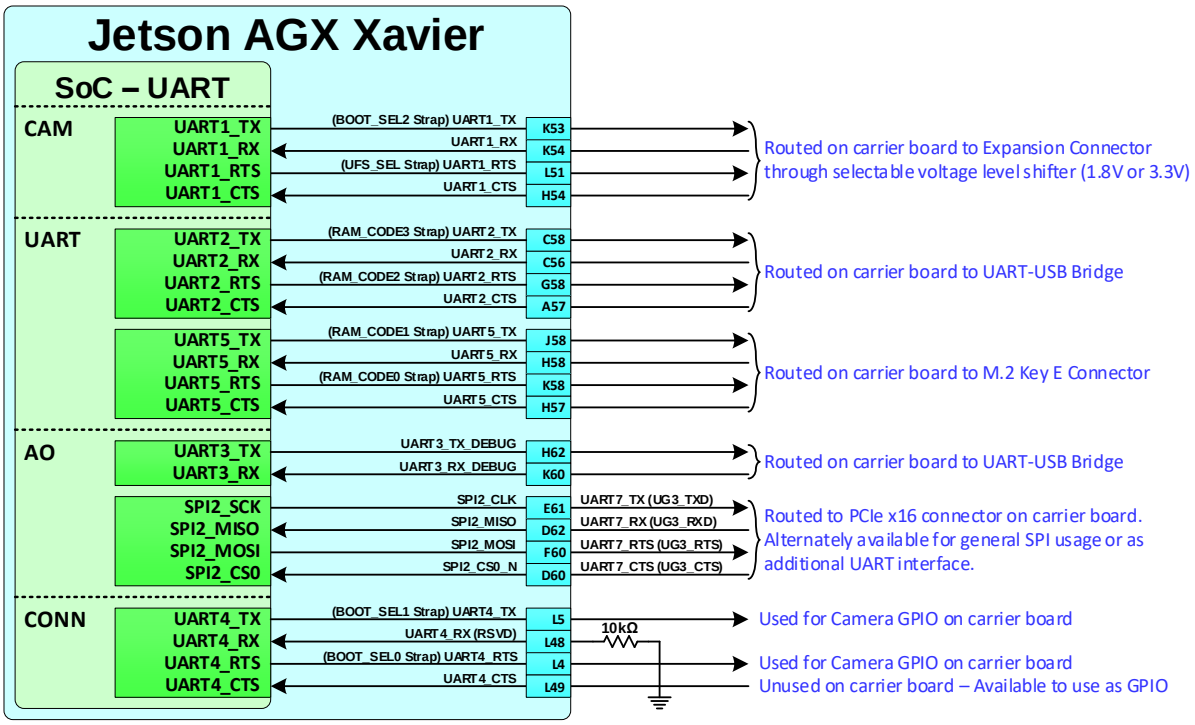
Table 13-10. Jetson AGX Xavier UART Pin Description

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Codes	Power-on Reset
K54	UART1_RX	UART1_RX	UART 1 Receive	Expansion Connector via level shifter	Input	CMOS – 1.8V	DD	z
K53	UART1_TX	UART1_TX	UART 1 Transmit		Output		DD	pd
H54	UART1_CTS	UART1_CTS	UART 1 Clear to Send		Input		ST	pu
L51	UART1_RTS	UART1_RTS	UART 1 Request to Send		Output		ST	pd
C56	UART2_RX	UART2_RX	UART 2 Receive	UART-USB (MicroB) Bridge	Input		DD	pd
C58	UART2_TX	UART2_TX	UART 2 Transmit		Output		DD	pd
A57	UART2_CTS	UART2_CTS	UART 2 Clear to Send		Input		ST	pu
G58	UART2_RTS	UART2_RTS	UART 2 Request to Send		Output		ST	pd
K60	UART3_RX_DEBUG	UART3_RX	Debug UART Receive		Input		DD	pd
H62	UART3_TX_DEBUG	UART3_TX	Debug UART Transmit		Output		DD	pd
H58	UART5_RX	UART5_RX	UART 5 Receive	M.2 Key E Connector	Input		ST	pd
J58	UART5_TX	UART5_TX	UART 5 Transmit		Output		ST	pd
H57	UART5_CTS	UART5_CTS	UART 5 Clear to Send		Input		ST	pu
K58	UART5_RTS	UART5_RTS	UART 5 Request to Send		Output		ST	pd
E61	SPI2_CLK (UART7_TX)	SPI2_SCK	SPI 2 Clock or UART 7 Transmit	PCIe x16 Connector	Bidir		DD	pd
D60	SPI2_CS0_N (UART7_CTS)	SPI2_CS0	SPI 2 Chip Select 0 or UART 7 Clear to Send		Bidir		DD	z
D62	SPI2_MISO (UART7_RX)	SPI2_MISO	SPI 2 Master In / Slave Out or UART 7 Receive		Bidir		DD	pd
F60	SPI2_MOSI (UART7_RTS)	SPI2_MOSI	SPI 2 Master Out / Slave In or UART 7 Return to Send		Bidir		DD	Pd

Notes:

1. In the Type/Dir column, Output is from Jetson AGX Xavier. Input is to Jetson AGX Xavier. Bidir is for Bidirectional signals.
2. The direction indicated for the UART pins is true when used for that function. Otherwise, these pins support GPIO functionality and can support both input and output (bidirectional).
3. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
4. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Figure 13-7. Jetson AGX Xavier UART Connections



Notes: UART4 pins do not support UART functionality and UART4_RX pin is reserved and must be tied to GND through a 10kΩ resistor. See the routing requirements in

Table 13-12. UART4_TX, UART4_RTS and UART4_CTS are available for use as GPIOs.

Care must be taken that any of the UART pins with straps associated with them are not pulled up/down or driven up/down by connected devices that would affect the strap level at power-on.

Table 13-11. UART Signal Connections

Module Pin Name	Type	Termination	Description
UART[5,2:1]_TX, UART3_TX_DEBUG and SPI2_CLK (UART7_TX)	O		UART Transmit: Connect to Peripheral RXD pin of device
UART[5,2:1]_RX, UART3_RX_DEBUG and SPI2_MISO (UART7_RX)	I		UART Receive: Connect to Peripheral TXD pin of device
UART[5,2:1]_CTS and SPI2_CS0_N (UART7_CTS)	I		UART Clear to Send: Connect to Peripheral RTS_N pin of device
UART[5,2:1]_RTS and SPI2_MOSI (UART7_RTS)	O		UART Request to Send: Connect to Peripheral CTS pin of device

Table 13-12. Reserved UART4_RX Routing Requirements

Parameter	Requirement	Units	Notes
Minimum Trace spacing to other signals	3x (4x preferred)	dielectric	
Minimum distance from UART4_RX Plated-through hole (PTH) and other signal PTHs.	1.5	mm	
Trace Length to resistor to GND	5-15	mm	

13.4 CAN

Jetson AGX Xavier brings two controlled area network (CAN) interfaces out to the main connector.

Table 13-13. Jetson AGX Xavier CAN Pin Description

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
F58	CAN0_DIN	CAN0_DIN	CAN 0 Receive	Expansion Header	Input	CMOS 3.3V	CZ	pu
D59	CAN0_DOUT	CAN0_DOUT	CAN 0 Transmit		Output		CZ	pu
B61	CAN1_DIN	CAN1_DIN	CAN 1 Receive		Input		CZ	pu
H61	CAN1_DOUT	CAN1_DOUT	CAN 1 Transmit		Output		CZ	pu
B62	GPIO08	CAN1_STB	GPIO / Digital Mic Input Data		Input		CZ	pd
C61	GPIO09	CAN1_EN	GPIO / Digital Mic Input Clock		Output		CZ	z
E59	GPIO06	CAN0_EN	GPIO	PCIe REFCLK mux Select	Output		CZ	z
F59	GPIO07	CAN0_WAKE	GPIO	Unused	Input		CZ	z
A62	GPIO10	CAN1_WAKE	GPIO	USB PD Controller Interrupt	Input		CZ	z

Notes:

1. In the Type/Dir column, Output is from Jetson AGX Xavier. Input is to Jetson AGX Xavier. Bidir is for Bidirectional signals.
2. The direction indicated for the CAN signals are associated with that usage. The pins support GPIO functionality, so support both input and output operation (bidirectional).
3. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
4. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Figure 13-8. Jetson AGX Xavier CAN Connections

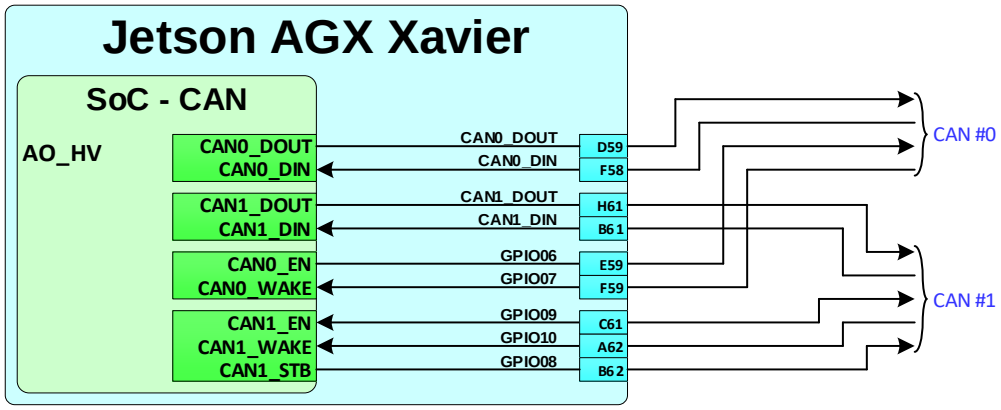


Table 13-14. CAN Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate / Frequency	5	Mbps / MHz	
Configuration / Device Organization	1	load	
Reference plane	GND		
Trace Impedance	50	Ω	±15%
Via proximity (Signal via to GND return via)	< 3.8 (24)	mm (ps)	
Trace spacing - Microstrip / Stripline	4x / 3x	dielectric	
Max Trace Length (for RX and TX only)	223 (1360)	mm (ps)	
Max Trace Length/Delay Skew from RX to TX	8 (50)	mm (ps)	

Table 13-15. CAN Signal Connections

Module Pin Name (Function)	Type	Termination	Description
CANx_DOUT	O		CAN Data Output: Connect to matching pin of device
CANx_DIN	I		CAN Input: Connect to Peripheral pin of device
GPIO06 (CAN0_EN) GPIO09 (CAN1_EN)	O		CAN Enable: Connect to matching pin of device
GPIO08 (CAN1_STB)	O		CAN 1 Standby: Connect to matching pin of device
GPIO07 (CAN0_WAKE) GPIO10 (CAN1_WAKE)	I		CAN Wake: Connect to matching pin of device

Chapter 14. Fan

Jetson AGX Xavier provides PWM and Tachometer functionality for controlling a fan as part of the thermal solution. Information on the PWM and Tachometer pins and functions can be found in the following locations:

- *Jetson AGX Xavier Module Pin Mux*:
  - This is used to configure the FAN_PWM and FAN_TACH pins. The FAN_PWM pin is configured as GP_PWM4. The FAN_TACH pin is configured as NV_THERM_FAN_TACH.
- *Xavier Technical Reference Manual*:
  - Functional descriptions and related registers can be found in the TRM for the FAN_PWM (PWM chapter) and FAN_TACH (Tachometer chapter) functions.
- *Jetson AGX Xavier Developer Kit Carrier Board Specification*:
  - The document contains the maximum current capability of the VDD_5V supply in the Interface Power chapter. The fan is powered by this supply on the Jetson AGX Xavier Developer Kit carrier board.

Table 14-1. Jetson AGX Xavier Fan Pin Description

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Codes	Power-on Reset
K62	FAN_PWM	TOUCH_CLK	Fan Pulse Width Modulation signal	Fan Circuit/Connector	Output	CMOS – 1.8V	ST	pd
E54	FAN_TACH	SOC_GPIO22	Fan Tachometer signal	Fan Circuit/Connector	Input		ST	pd

Notes:

1. In the Type/Dir column, Output is from Jetson AGX Xavier. Input is to Jetson AGX Xavier. Bidir is for Bidirectional signals.
2. The direction indicated for FANx is associated with their use as Fan PWM/Tach. The pins support GPIO functionality, so support both input and output operation (bidirectional).
3. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
4. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Figure 14-1. Jetson AGX Xavier Fan Connection Example

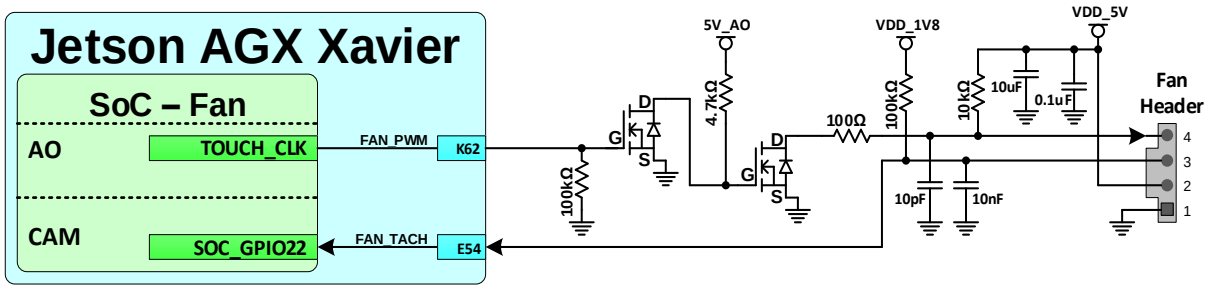


Table 14-2. Fan Signal Connections

Module Pin Name	Type	Termination	Description
FAN_PWM	O	100kΩ pulldown to GND.	Fan Pulse Width Modulation: Connect through FET as shown in the Jetson AGX Xavier Fan Connections figure.
FAN_TACH	I	100kohm pullup to VDD_1V8	Fan Tachometer: Connect to TACH pin on fan connector.

Chapter 15. Debug and Strapping

This chapter covers the interfaces that are provided for debug & development as well as covering SoC pin strapping and boundary scan.

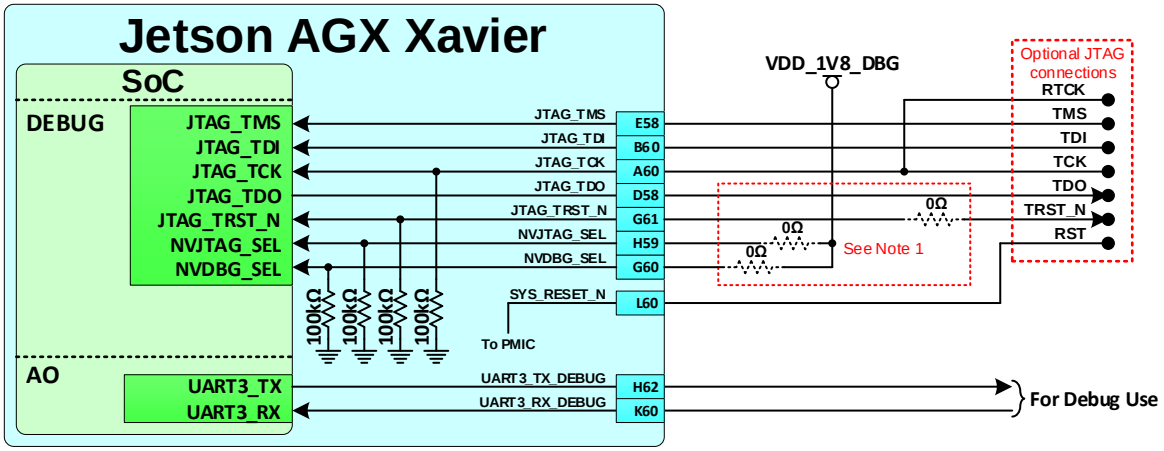
15.1 USB Recovery Mode

USB Recovery mode provides an alternate boot device (USB). In this mode, the system is connected to a host system and boots over USB. This is used when a new image needs to be flashed, or for debug purposes. To enter USB recovery mode, the FORCE_RECOVERY_N pin is held low when the system is powered on. FORCE_RECOVERY_N is the SoC RCM0 strap. Recovery mode can operate in either USB 2.0 or USB 2.0 + USB 3.1 modes. Recovery mode using USB 2.0 is from interface USB0_N/P only. For USB 3.1 recovery mode, the system will first enter USB 2.0 recovery mode using USB0_N/P and then SW configures the transition to use the USB 3.1 interface for the remainder of the flashing process. The USB 3.1 recovery mode interface must come from the UPHY_TX1/RX1_P/N pins. See the USB section (Section 0) for an example connection figures that shows USB0 and PEX_TX1/RX1_PN connected to either a USB Type C connector or a USB Micro AB SS connector. In the example, a 5V power switch output connects to the VBUS pin on the connector. This supply is disabled by default in our reference design, so there is no contention with the 5V from the host system VBUS supply. If the supply on the Xavier system is present and enabled, the VBUS pin should not be connected from the host (special cable with VBUS disconnected).

15.2 JTAG and Debug UART

The following figure shows the JTAG and UART debug connections.

Figure 15-1. JTAG and UART Debug Connections

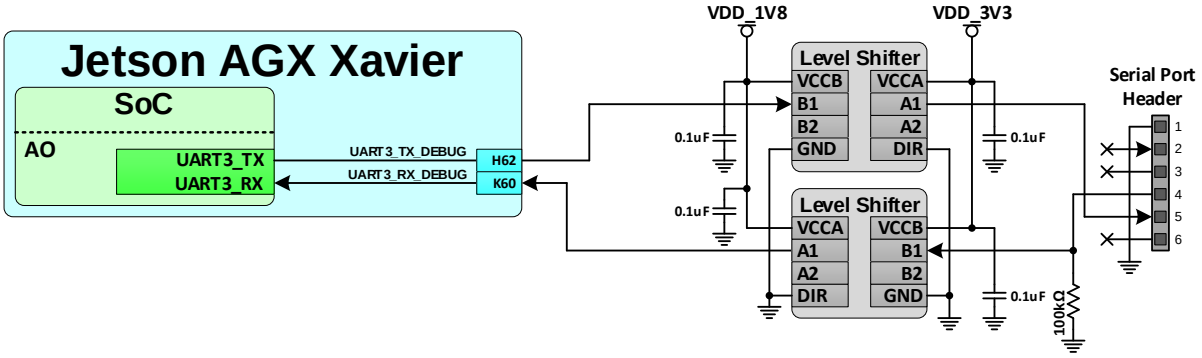


Notes:

1. NVJTAG_SEL and JTAG_TRST_N must be low for normal operation and pulled to 1.8V for Boundary Scan Mode. NVDBG is left unconnected (pulled down on module) for normal operation and pulled to 1.8V for alternate debug modes (debug over USB, etc.). for Boundary Scan test mode, JTAG_TRST_N must be driven high in the proper sequence. See the *Xavier Boundary Scan Requirements and Usage* document for details.
2. Check preferred JTAG debugger documentation for JTAG PU/PD recommendations.

The Jetson AGX Xavier Developer Kit carrier board reference design implements a USB to UART bridge. A simpler option is shown in the following figure. The UART3_DEBUG interface is shown routed to a 6-pin header through level shifters.

Figure 15-2. Simple Debug UART Header Connections



15.2.1 JTAG

JTAG is not required but may be useful for new design bring up or for boundary scan.

Table 15-1. Jetson AGX Xavier JTAG Pin Description

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
A60	JTAG_TCK	JTAG_TCK	JTAG Test Clock. Pulled to GND through 100kΩ resistor on module.	JTAG Connector	Input	CMOS – 1.8V	JT_RST	z
B60	JTAG_TDI	JTAG_TDI	JTAG Test Data In				JT_RST	pu
D58	JTAG_TDO	JTAG_TDO	JTAG Test Data Out		Output		ST	z
E58	JTAG_TMS	JTAG_TMS	JTAG Test Mode Select		Input		JT_RST	pu
G61	JTAG_TRST_N	JTAG_TRST_N	JTAG Test Reset. Low for normal operation or ARM JTAG debug mode. High for scan test mode. Pulled to GND through 100kΩ resistor on module.	Unused	Input		JT_RST	pd
G60	NVDBG_SEL	NVDBG_SEL	NVIDIA Debug Select. Pulled to GND through 100kΩ resistor on module.	Unused – Driven to GND	Input		JT_RST	z
H59	NVJTAG_SEL	NVJTAG_SEL	NVIDIA JTAG Select. Low for normal operation or ARM JTAG debug mode. High for scan test mode. Pulled to GND through 100kΩ resistor on module.		Input		JT_RST	z

Notes:

1. In the Type/Dir column, Output is from Jetson AGX Xavier. Input is to Jetson AGX Xavier. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Table 15-2. JTAG Signal Connections

Module Pin Name (other)	Type	Termination	Description
JTAG_TMS	I		**JTAG Mode Select: Connect to TMS pin of connector**
JTAG_TCK	I	100kΩ to **GND on module**	**JTAG Clock: Connect to TCK pin of connector**
JTAG_TDO	O		**JTAG Data Out: Connect to TDO pin of connector**
JTAG_TDI	I		**JTAG Data In: Connect to TDI pin of connector**
JTAG_RTCK	I		**JTAG Return Clock: Connect to RTCK pin of connector**
JTAG_TRST_N	I	100kΩ to **GND and 0.1uF to GND on module**	**JTAG General Purpose Pin #0: Leave unconnected for normal or ARM JTAG operation.** Connect to **TRST** pin of connector or similar for Boundary Scan test mode. See the *Xavier Boundary Scan Requirements and Usage* document for details.

Module Pin Name (other)	Type	Termination	Description
NVJTAG_SEL		100kΩ to GND on module	NVIDIA JTAG Select: Used as select Normal operation: Must be low, so leave unconnected (on-module pulldown will keep low). Scan test mode: Connect NVJTAG_SEL to VDD_1V8. See the Boundary Scan Test Mode section and the Xavier Boundary Scan Requirements and Usage document for details.
NVDBG_SEL		100kΩ to GND on module	NVIDIA Debug Select: Used as select Normal operation: Leave series resistor from NVDBG_SEL not stuffed. Advanced Debug modes: Connect NVDBG_SEL to VDD_1V8 (install 0Ω resistor as shown).

15.2.2 Debug UART

Jetson AGX Xavier provides UART3_DEBUG for debug purposes. The connections are described in the following table.

Table 15-3. Debug UART Connections

Module Pin Name	Type	Termination	Description
UART3_TX_DEBUG	O		UART Transmit: Connect to RX pin of serial device
UART3_RX_DEBUG	I	If level shifter implemented, 100kΩ to supply on the non-Jetson AGX Xavier side of the device.	UART Receive: Connect to TX pin of serial device

15.3 Strapping Pins

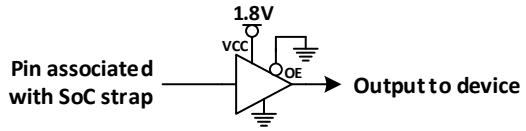
Jetson AGX Xavier has one strap (FORCE_RECOVERY_N) that is intended to be used on the carrier board. That strap is used to enter Force Recovery mode (held low during power-on). The other straps mentioned in this section are for use on the module by NVIDIA only. Their state at power-on must not be affected by any connections on the carrier board. The carrier board design should guarantee a high-z on the pins during boot. The pins that are associated with SoC straps (besides FORCE_RECOVERY_N) are as follows:

STANDBY_REQ_N
UART1_TX
UART1_RTS
GPIO33
UART2_TX
UART2_RTS
UART4_TX
UART4_RTS
UART5_RTS
UART5_TX

Note: GPIO12 is used on JAXi only as the BOOT_CHAIN_SELECT strap. This strap selects between two boot chain options if needed. This pin is connected to a Safety MCU GPIO (if implemented in a design). The MCU drives the level of the strap when JAXi is powered on to determine which of two boot chains will be used.

Figure 15-3 shows an example of a buffer used to isolate the signals from any of the pins listed from the device they are connected to on the carrier board.

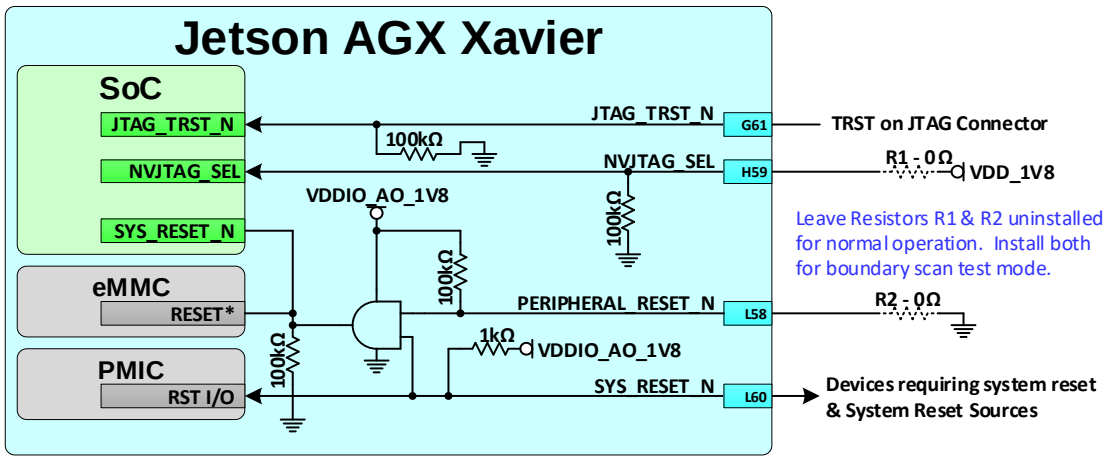
Figure 15-3. Example Buffer Between Pin Associated with SoC Strap and Connected Device



15.4 Boundary Scan Test Mode

To support Boundary Scan Test mode, the SoC NVJTAG_SEL pin must be pulled high and The SoC must be held in reset without resetting the PMIC. This is done using the PERIPHERAL_RESET_N pin on the module. The following figure illustrates this. Other requirements related to supporting boundary scan test mode are described in the *Xavier Boundary Scan Requirements and Usage* document.

Figure 15-4. Boundary Scan Connections



15.5 Safety MCU JAXi Only

Jetson JAXi Xavier adds support for a safety MCU in the system for designs that require this. The following connections are intended to use with a safety MCU.

- SPI2
- VM_I2C (Voltage Monitor I2C)
- VM_INT_N (Voltage Monitor Interrupt)
- GPIO31 (SAFESTATE)
- GPIO12 (BOOT_CHAIN_SELECT strap)
- NC_O3 (TEMP_THERM_OUT
- EQOS / RGMII (Ethernet)

The pin descriptions for several of the signals involved with a safety MCU design are shown in the following table. For SPI and RGMII (Ethernet) pin descriptions, see the respective sections earlier in this design guide.

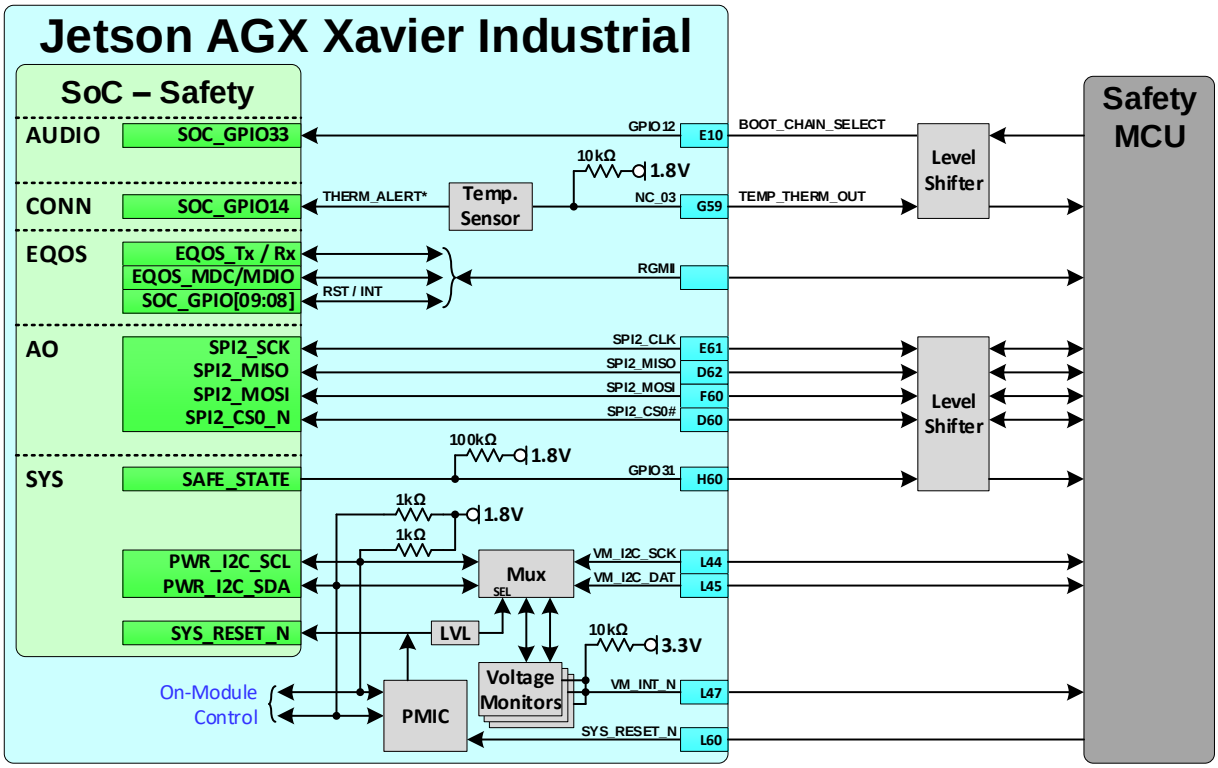
Table 15-4. Safety MCU Related Partial Pin Descriptions

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on NVIDIA Carrier Board	Direction	Pin Type	MPIO Pad Code	Power-on Reset
L44	VM_I2C_SCK	na	JAXi only: Connects to safety MCU on carrier board if implemented. Routed on module to mux with PWR_I2C. Mux select connected to SoC reset. Output of mux controls on-module voltage monitors. VM_I2C controls when reset is active (low).	Unused	Bidir	Open Drain, 3.3V	–	–
L45	VM_I2C_DAT	na			Bidir	Open Drain, 3.3V	–	–
L47	VM_INT_N	na	Interrupt from on-module voltage monitors. Connects to safety MCU if implemented.		Output	Open Drain, 3.3V	–	–
H60	GPIO31	SAFE_STATE	GPIO. For JAXi only, routed to the safety MCU.	Micro SD / UFS Card Socket (UFS Detect)	Bidir	CMOS – 1.8V	DD	z
E10	GPIO12 (BOOT_CHAIN_SELECT strap)	SOC_GPIO33	JAXi only, used as a strap at power-on to select from two boot chains. Driven by the Safety MCU if implemented.	M.2 Key E Connector (M2 Wake AP)	Bidir	CMOS – 1.8V	ST	pu
G59	NC_03 (TEMP_THERM_OUT)	–	Connects to on-module temperature sensor THERM* output. 10kΩ pullup to 1.8V on module.	Unused	Output	Open Drain, 1.8V	–	–

Notes:

1. In the Type/Dir column, Output is from Jetson AGX Xavier. Input is to Jetson AGX Xavier. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Figure 15-5. Safety MCU Connections



Chapter 16. Pads

16.1 MPIO Pad Behavior when Associated Power Rail is Enabled

Jetson AGX Xavier CZ (see note) type MPIOs pins may glitch when the associated power rail is enabled or disabled. Designers should take this into account. MPIOs of this type that must maintain a low state even while the power rail is being ramped up or down may require special handling. The "Pin Descriptions" section of *Jetson AGX Xavier Data Sheet* includes the pin type information.

16.2 Schmitt Trigger Usage

The MPIO pins have an option to enable or disable Schmitt Trigger mode on a per-pin basis. This mode is recommended for pins used for edge-sensitive functions such as input clocks, or other functions where each edge detected will affect the operation of a device. Schmitt Trigger mode provides better noise immunity and can help avoid extra edges from being "seen" by the SoC inputs. Input clocks include the I2S and SPI clocks when SoC is in slave mode. The FAN_TACH pin is another input that could be affected by noise on the signal edges. The SDCARD_CLK pin, while used to output the SD clock, also samples the clock at the input to help with read timing. Therefore, the pin may benefit from enabling Schmitt Trigger mode. Care should be taken if the Schmitt Trigger mode setting is changed from the default initialization mode as this can have an effect on interface timing.

16.3 Pins Pulled and Driven During Power-on

Jetson AGX Xavier is powered up before the carrier board (See Power Sequencing section). Some of the pins are pulled or driven high either by The SoC or by pull-up resistors on the module. The pins on Jetson AGX Xavier that are pulled/driven high by The SoC can be found in the Module Pinmux spreadsheet. The pins that have pull-up resistors on the module are listed in the Jetson AGX Xavier Signal Terminations section of the Design Checklist chapter. Care must be taken on the carrier board design to ensure that any of these pins that connect to

devices on the carrier board (or devices connected to the carrier board) do not cause damage or excessive leakage to those devices. Some of the ways to avoid issues with sensitive devices are:

- External pull-downs on the carrier board that are strong enough to keep the signals low are one solution, given that this does not affect the function of the pin. This will not work pins actively driven high by default.
- Buffers or level shifters can be used to separate the signals from devices that may be affected. The buffer and shifter should be disabled until the device power is enabled.

16.4 Pad Drive Strength

The following table provides the maximum MPIO pad output drive current when the pad is configured for the maximum DRVUP/DRVDN values (11111b). The MPIO pad types include the ST, DD, CZ and LV_CZ type pads. The pad types can be found in the *Jetson AGX Xavier Module Data Sheet*.

Table 16-1. MPIO Maximum Output Drive Current

IOL/IOH	Pad Type	VOL	VOH
+/- 1mA	ST	0.15*VDD	0.825*VDD
+/- 1mA	DD	0.15*VDD	0.8*VDD
+/- 1mA	CZ (1.8V mode)	0.15*VDD	0.85*VDD
+/- 1mA	CZ (3.3V mode)	0.15*VDD	0.85*VDD
+/- 1mA	LV_CZ	0.15*VDD	0.85*VDD
+/- 2mA	ST	0.15*VDD	0.7*VDD
+/- 2mA	DD	0.175*VDD	0.7*VDD
+/- 2mA	CZ (1.8V mode)	0.25*VDD	0.75*VDD
+/- 2mA	CZ (3.3V mode)	0.15*VDD	0.75*VDD
+/- 2mA	LV_CZ	0.25*VDD	0.75*VDD

Chapter 17. Unused Interface Terminations

17.1 Unused MPIO Interfaces

The following Jetson AGX Xavier pins (and groups of pins) are Jetson AGX Xavier MPIO (Multi-purpose Standard CMOS Pad) pins that support either special function IOs (SFIO) and/or GPIO capabilities. Any unused pins or portions of pin groups listed in the following table that are not used can be left unconnected.

Table 17-1. Unused MPIO Pins and Pin Groups

Module Pins / Pin Groups		Module Pins / Pin Groups
I2Sx, AUD_MCLK, DSPKx, DMICx		GP_PWMx
SDMMCx		CCLAx
MIPI_TRC_x		SCE_SAFE_STATE
EQOSx		SOC_THERMx
QSPIx		PMICINTR
Ux3_x		GPIO_AO_RET
I2Cx		WDT_RESET_x
SPIx		TOUCH_x
CANx		EXTPERIPHx
VGPx		IGPUx
SLVSx		SATA_LED_ACTIVE
IQCx		NV_THERMx
UFSx		ISTCTRLx
PEx, PEX_CLKx		DCx
DP_AUXx		DGPU_x

17.2 Unused SFIO Interface Pins

See the "Unused SFIO (Special Function I/O) Interface Pins" section in the pin description checklist attached to this design guide.

To access the attached file, click the Attachment icon on the left-hand toolbar on this PDF (using Adobe Acrobat Reader or Adobe Acrobat). Select the file and use the Tool Bar options (Open, Save) to retrieve the documents.
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Chapter 18. Design and Bring-up Checklists

The design checklist is intended to help ensure that the correct connections have been made in a design. The check items describe connections for the various interfaces and the "Same/Diff/NA" column is intended to be used to indicate whether the design matches the check item description, is different, or is not applicable to the design.

The bring-up checklist is intended to provide basic items to check during bring-up for power delivery and the various interfaces used in a design.

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Chapter 19. General Layout Guidelines

Trace and via characteristics play an important role in signal integrity and power distribution on Jetson AGX Xavier. Vias can have a strong impact on power distribution and signal noise, so careful planning must take place to ensure designs meet NVIDIA's via requirements. Trace length and impedance determine signal propagation time and reflections, both of which can greatly improve or reduce the performance of Jetson AGX Xavier. Trace and via requirements for each signal type can be found in the corresponding chapter; this chapter provides general guidelines for via and trace placement.

19.1 Via Guidelines

The number of vias in the path of a given signal, power supply line, or ground line can greatly affect the performance of the trace. Via placement can make differences in current carrying capability, signal integrity (due to reflections and attenuation), and noise generation, all of which can impact the overall performance of the trace. The following guidelines provide basic advice for proper use of vias.

19.1.1 Via Count and Trace Width

As a rule, each ampere of current requires at least two micro-vias.

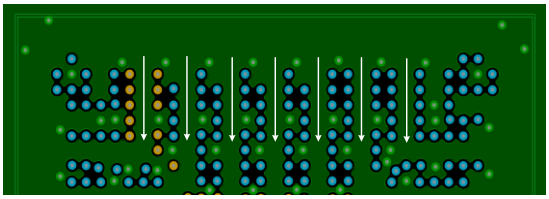
19.1.2 Via Placement

If vias are not placed carefully, they can severely degrade the robustness of a board's power plane. In standard deigns that do not use blind or buried vias, construction of a via entails drilling a hole that cuts into the power and ground planes. Thus, incorrect via placement affects the amount of copper available to carry current to the power balls of the IC.

19.1.3 Via Placement and Power and Ground Corridors

Vias should be placed so that sufficiently wide power corridors are created for good power distribution, as show in Figure 19-1.

Figure 19-1. Via Placement for Good Power Distribution



Care should also be taken to avoid use of "thermal spokes" (also referred to as "thermal relief") on power and ground vias. Thermal spokes are not necessary for surface-mount components, and the narrow spoke widths contribute to increased inductance. The metal on the inner layers between vias may not be flooded with copper if enough spacing is not provided. The diminished spacing creates a blockage and forces the current to find another path due to lack of copper, as shown in Figure 19-2 and Figure 19-3. This leads to power delivery issues and impedance discontinuities when traces are routed over these plane voids.

Figure 19-2. Good Current Flow Resulting from Correct Via Placement

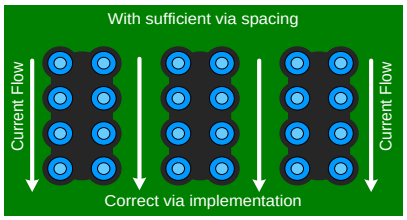
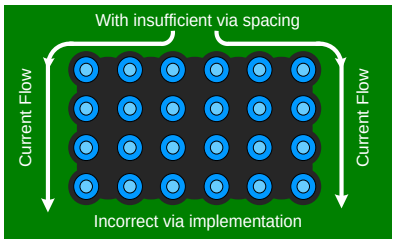


Figure 19-3. Poor Current Flow Resulting from Incorrect Via Placement



In general, a dense via population should be avoided and good PCB design principles and analysis should be applied.

19.2 Connecting Vias

To be effective, vias must be connected properly to the signal and power planes. Poor via connections make the capacitor and power planes less effective, leading to increased cost due to the need for additional capacitors to achieve equivalent performance. This not only impacts the Bill of Materials (BOM) cost of the design, but it can greatly impact quality and reliability of the design.

19.3 Trace Guidelines

Trace length and impedance play a critical role in signal integrity between the driver and the receiver on Jetson AGX Xavier. Signal trace requirements are determined by the driver characteristics, source characteristics, and signal frequency of the propagating signal.

19.3.1 Layer Stack-Up

The number of layers required is determined by the number of memory signal layers needed to achieve the desired performance, and the number of power rails required to achieve the optimum power delivery/noise floor. For example, high-performance boards require four memory signal routing layers, with at least two GND planes for reference. This comes to six layers; add another two for power, which gives eight layers minimum. Reduction from eight to six layers starts the trade-off of cost versus performance.

Power and GND planes usually serve two purposes in PCB design: power distribution and providing a signal reference for high-speed signals.

Either the power or the ground planes can be used for high-speed signal reference; this is particularly common for low-cost designs with a low layer count. When both power and GND are used for signal reference, make sure you minimize the reference plane transition for all high-speed signals. Decoupling caps or transition vias should be added close to the reference plane transitions.

19.3.2 Trace Length

The maximum trace length for a given signal is determined by the maximum allowable propagation delay and impedance for the signal. Higher frequency signals must be treated as transmission lines (see Chapter 21 “Transmission Line Primer”) to determine proper trace characteristics for a signal.

All signals on the graphics card maintain different trace guidelines. Refer to the corresponding signal chapter in the design guide to determine the guidelines for the signal.

Chapter 20. Stack-Ups

20.1 Reference Design Stack-ups

This section details the reference design stack-ups.

20.1.1 Importance of Stack-up Definition

Stack-ups define the number and order of board layers. Stack-up definition is critical to the following design:

- Circuit routability
- Signal quality
- Cost

20.1.2 Impact of Stack-up Definition on Design

- Stack-Up Impact on Circuit Routability
  If there are insufficient layers to maintain proper signal spacing, prevent discontinuities in reference planes, obstruct flow of sufficient current, or avoid extra vias, circuit routing can become unnecessarily complex. Layer count must be minimally appropriate for the circuit.
- Stack-Up Impact on Signal Quality
  Both layer count and layer order impact signal integrity. Proper inter-signal spacing must be achievable. Via count for critical signals must be minimized. Current commensurate with the performance of the board must be carried. Critical signals must be adjacent to major and minor reference planes and adhere to proximity constraints with respect to those planes. The recommended NVIDIA stack-ups achieve these requirements for the signal speeds supported by the board.
- Stack-Up Impact on Cost
  While defining extra layers can facilitate excellent signal integrity, current handling capability and routability, extra layers can impede the goal of hitting cost targets. The art of stack-up definition is achieving all technical and reliability circuit requirements in a cost-efficient manner. The recommended NVIDIA stack-ups achieve these requirements with efficient use of board layers.

Chapter 21. Transmission Line Primer

21.1 Basic Board Level Transmission Line Theory

NVIDIA maintains strict guidelines for high-frequency PCB transmission lines to ensure optimal signal integrity for data transmission. This section provides a brief primer into basic board-level transmission line theory.

21.1.1 Characteristics

The most important PCB transmission line characteristics are listed in the following bullets:

- Trace width/height, PCB height and dielectric constant, and layer stack-up affect the characteristic trace impedance of a transmission line.

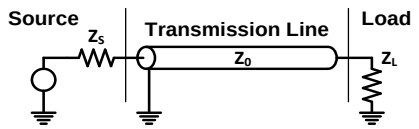
$$Z_0 \cong \left(\frac{L}{C}\right)^{1/2}$$

- Signal rise time is proportional to the transmission line impedance and load capacitance.

$$RiseTime \cong \left(\frac{Z_0 * R_{Term}}{Z_0 + R_{Term}}\right) * C_{Load}$$

- Real transmission lines (Figure 21-1) have non-zero resistances that lead to attenuation and distortion, creating signal integrity issues.

Figure 21-1. Typical Transmission Lin Circuit



Transmission lines are used to "transmit" the source signal to the load or destination with as little signal degradation or reflection as possible. For this reason, it is important to design the high-speed signal transmission line to fall within characteristic guidelines based on the signal speed and type.

21.2 Physical Transmission Line Types

The two primary transmission line types often used for Jetson AGX Xavier board designs are:

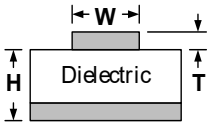
- Microstrip transmission line (Figure 21-2)
- Stripline transmission line (Figure 21-3)

The following sections describe each type of transmission.

21.2.1 Microstrip Transmission Line

Figure 21-2 describes the microstrip transmission line.

Figure 21-2. Microstrip Transmission Line



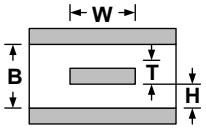
$$Z_0 = \left(\frac{87}{\sqrt{Er + 1.414}}\right) \ln\left(\frac{5.98H}{0.8W + T}\right)$$

- Z0: Impedance
- W: Trace width (inches)
- T: Trace thickness (inches)
- Er: Dielectric constant of substrate
- H: Distance between signal and reference plane

21.2.2 Stripline Transmission Line

Figure 21-3 describes the microstrip transmission line.

Figure 21-3. Stripline Transmission Line



$$Z_0 = \left(\frac{60}{\sqrt{Er}}\right) \ln\left(\frac{4H}{0.67\pi W\left(0.8 + \frac{T}{W}\right)}\right)$$

- Z0: Impedance
- W: Trace width (inches)
- T: Trace thickness (inches)
- Er: Dielectric constant of substrate
- H: Distance between signal and reference plane

21.3 Drive Characteristics

Driver characteristics are important to the integrity and maximum speed of the signal. The following points identify key driver equations and concepts used to improve signal integrity and transmission speed.

- The driver (source) has resistive output impedance Z_S, which causes only a fraction of the signal voltage to propagate down the transmission line to the receiver (load).
  - Transfer function at source:

$$T1 = \frac{Z_0}{Z_S + Z_0}$$

  - Driver strength is inversely proportional to the source impedance, Z_S.
- Z_S also acts as the source termination, which helps dampen reflection.
  - Source reflection coefficient:

$$R1 = \frac{(Z_S - Z_0)}{(Z_S + Z_0)}$$

21.4 Receiver Characteristics

Receiver characteristics are important to the integrity and detectability of the signal. The following points identify key receiver concepts and equations for optimum signal integrity at the final destination.

- The receiver acts as a capacitive load and often has a high load impedance, Z_L.
- Unterminated transmission lines cause overshoot and reflection at the receiver, which can cause data corruption.
  - Output transfer function at load:

$$T2 = \frac{2 * Z_L}{Z_L + Z_0}$$

  - Load reflection coefficient:

$$R2 = \frac{(Z_L - Z_0)}{(Z_L + Z_0)}$$

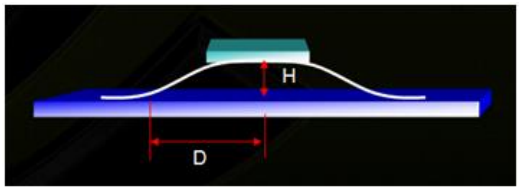
- Load impedance can be lowered with a termination resistor (R_{Term}) placed at the end of the transmission line.
  - Reflection is minimized when Z_L matches Z_0

21.5 Transmission Lines and Reference Planes

Defining an appropriate reference plane is vital to transmission line performance due to crosstalk and EMI issues. The following points explore appropriate reference plane identification and characteristics for optimal signal integrity:

- Transmission line return current (Figure 21-4)
  - High-speed return current follows the path of least inductance.
  - The lowest inductance path for a transmission line is right underneath the transmission line; i(D) is proportional to:

Figure 21-4. Transmission Line Height



- Transmission line return current:
  - High-speed return current follows the path of least inductance.
  - The lowest inductance path for a transmission line is the portion of the line closest to the dielectric surface; i(D) is proportional to

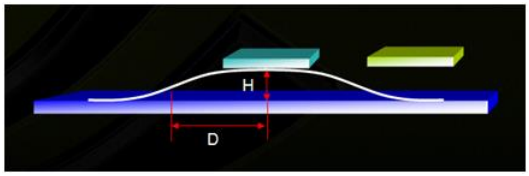
$$\frac{1}{\left(1+\left(\frac{D}{H}\right)^2\right)}$$

- Crosstalk on solid reference plane (Figure 21-5):
  - Crosstalk is caused by the mutual inductance of two parallel traces.
  - Crosstalk at the second trace is proportional to

$$\frac{1}{\left(1+\left(\frac{D}{H}\right)^2\right)}$$

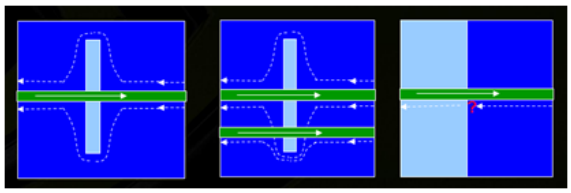
  - The signals need to be properly spaced to minimize crosstalk

Figure 21-5. Crosstalk on Reference Plane



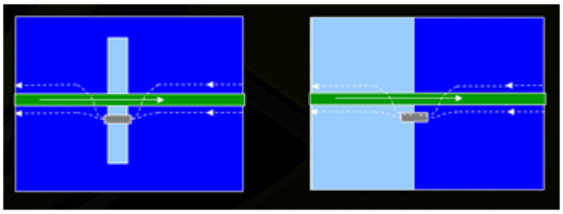
- Reference plane selection
  - Solid ground is preferred as reference plane.
  - Solid power can be used as reference plane with decoupling capacitors near driver and receiver.
  - Reference plane cuts and layer changes need to be avoided.
- Power plane cut example (Figure 21-6)
  - Power plane cuts will cause EMI issues.
  - Power plane cuts also induce crosstalk to adjacent signals.

Figure 21-6. Power Plane Cuts Example



- When cut is unavoidable:
  - Place decoupling capacitors near transition.
  - Place transition near source or receiver when decoupling capacitors are abundant (Figure 21-7).

Figure 21-7. Power Plane Cuts Example when Decouple Capacitors are abundant



- When signal changes plane:
  - Try not to change the reference plane, if possible.
  - When a reference plane switches to different power rail, a stitching capacitor is required (Figure 21-8).
  - When the same ground and power reference plane changes to a different layer, a stitching via is required (Figure 21-9).

Figure 21-8. Switching Reference Planes

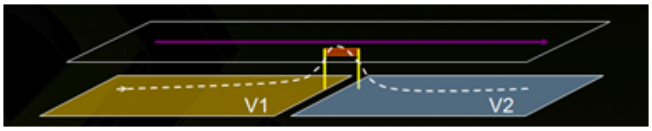
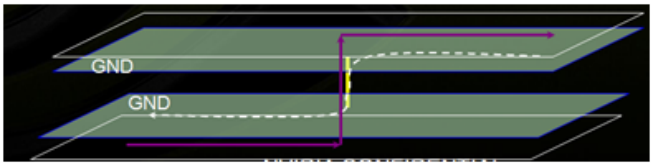


Figure 21-9. Reference Plane Switch Using Via



Chapter 22. Design Guideline Glossary

The design guidelines include various terms. The following descriptions are intended to show what these terms mean and how they should be applied to a design.

- Trace Delay
  - Max Breakout Delay
    Routing on Component layer: Maximum Trace Delay from module connector pin to point beyond pin array where normal trace spacing/impedance can be met. Routing passes to layer other than Component layer: Beyond this, normal trace spacing/impedance must be met.
  - Max Total Trace Delay
    Trace from module connector pin to device pin. This must include routing on the main PCB and any other Flex or secondary PCB. Delay is from the module connector to the final connector and device.
- Intra and Inter Pair Skews
  - Intra Pair Skew within Pair
    Difference in delay between two traces in differential pair: Shorter routes may require indirect path to equalize delays.
  - Inter Pair Skew Pair-to-Pair
    Difference between two (or possibly more) differential pairs.
- Impedance and Spacing
- Microstrip vs. Stripline
    - Microstrip: Traces next to single reference plane.
    - Stripline: Traces between two reference planes.
  - Trace Impedance
    Impedance of trace determined by width and height of trace, distance from reference plane, and dielectric constant of PCB material. For differential traces, space between pair of traces is also a factor.
  - Board Trace Spacing and Spacing to other Nets
    Minimum distance between two traces. Usually specified in terms of dielectric height which is distance from trace to reference layers.
  - Pair to Pair Spacing
    Spacing between differential traces.

- Breakout Spacing
  Possible exception to board trace spacing where different spacing rules are allowed under module connector pin in order to escape from the pin array. Outside device boundary, normal spacing rules apply.

- Reference Return
  - Ground Reference Return Via and Via proximity (signal to reference)
    - Signals changing layers and reference GND planes need similar return current path.
    - Accomplished by adding via, tying both GND layers together.
  - Via proximity (signal to refeference) is distance between signal and reference return vias.
    - GND reference via for Differential Pair.
    - Where a differential pair changes GND reference layers, return via should be placed close to and between signal vias (example to right).
  - Signal to return via ratio
    Number of Ground Return vias per Signal vias. For critical IFs, ratio is usually 1:1. For less critical IFs, several trace vias can share fewer return vias (i.e. 3:2 – 3 trace vias and 2 return vias).
  - Slots in Ground Reference Layer
    - When traces cross slots in adjacent power or ground plane.
    - Return current has longer path around slot.
    - Longer slots result in larger loop areas.
    - Avoid slots in GND planes or do not route across them.
  - Routing over Split Power Layer Reference Layers
    - When traces cross different power areas on power plane.
      - Return current must find longer path - usually a distant bypass cap.
      - If possible, route traces with solid plane (GND or PWR) or keep routes across single area.
    - If traces must cross two or more power areas, use stitching capacitors.
      - Placing one cap across two PWR areas near where traces cross area boundaries provides high-frequency path for return current.
      - Cap value typically 0.1uF and should ideally be within 0.1" of crossing.

Chapter 23. Jetson AGX Xavier Pin Description

The Jetson AGX Xavier pin description is attached to this design guide.

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