NVIDIA Jetson AGX Xavier Series Camera Module

Hardware Design Guide

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Document History

DG-09364-001_v1.3

Version	Date	Description of Change
1.0	May 8, 2019	Initial Release
1.1	June 14, 2019	Updated to include all of Jetson AGX Xavier series modules
1.2	May 26, 2020	Updated Chapter 1 "Introduction" Updated and reorganized Chapter 2 "MIPI CSI Camera Module" Added new chapter (Chapter 3) covering SLVS
1.3	June 8, 2021	• Updated Chapter 1: Introduction • Updated and reorganized Chapter 2: MIPI CSI Camera Module • Added Chapter 3: GMSL Interposer Board

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Chapter 1. Introduction

This design guide contains recommendations and guidelines for engineers to follow to create a product that is optimized to achieve the best performance from camera related interfaces supported on the NVIDIA® Jetson AGX Xavier™ Developer Kit carrier board or on a custom carrier board.

The Jetson AGX Xavier Series modules all support MIPI CSI. The Jetson AGX Xavier Series modules except Jetson AGX Xavier Industrial also support the SLVS-EC camera interface. On the Jetson AGX Xavier Developer Kit carrier board, the CSI interface is routed to the 120-pin camera connector (J509). The SLVS-EC interface is routed to the x16 PCIe connector and share pins with an 8-lane PCIe interface on the Jetson AGX Xavier Developer Kit carrier board. The following sections describe how to design camera modules for these two interfaces.

1.1 References

Refer to the following documents or models for more information. Always use the latest revision of all documents.

- *Jetson AGX Xavier Developer Kit Carrier Board Specification*
- *Jetson AGX Xavier Series OEM Product Design Guide*

Note: References to Jetson AGX Xavier apply to any of the Jetson AGX Xavier series of modules.

1.2 Abbreviations and Definitions

Table 1-1 lists the abbreviations that may be used throughout this design guide and their definitions.

Table 1-1. Abbreviations and Definitions

Abbreviation	Definition
ADDR	Address
AF	Auto Focus
B2B	Board-to-Board
CSI	MIPI spec. Camera Serial Interface
EEPROM	Electrically Erasable Programmable Read Only Memory
GPIO	General Purpose Input/Output
FM	Fast Mode of I2C (400 MHz)
I2C	Inter IC
MUX	Multiplexer
LDO	Low Dropout (voltage regulator)
XTAL	Crystal Oscillator
SLVS-EC	Scalable Low Voltage Signaling Embedded Clock

Chapter 2. MIPI CSI Camera Module

This chapter is mostly concerned with connecting cameras to the Jetson AGX Xavier Developer Kit carrier board camera connector (J509) which supports MIPI CSI. Much of the information would also apply to a custom carrier board design, but it would be up to the designer to decide on an interposer connector/pinout (if implemented), I2C addressing, whether to implement an EEPROM, and mechanical requirements.

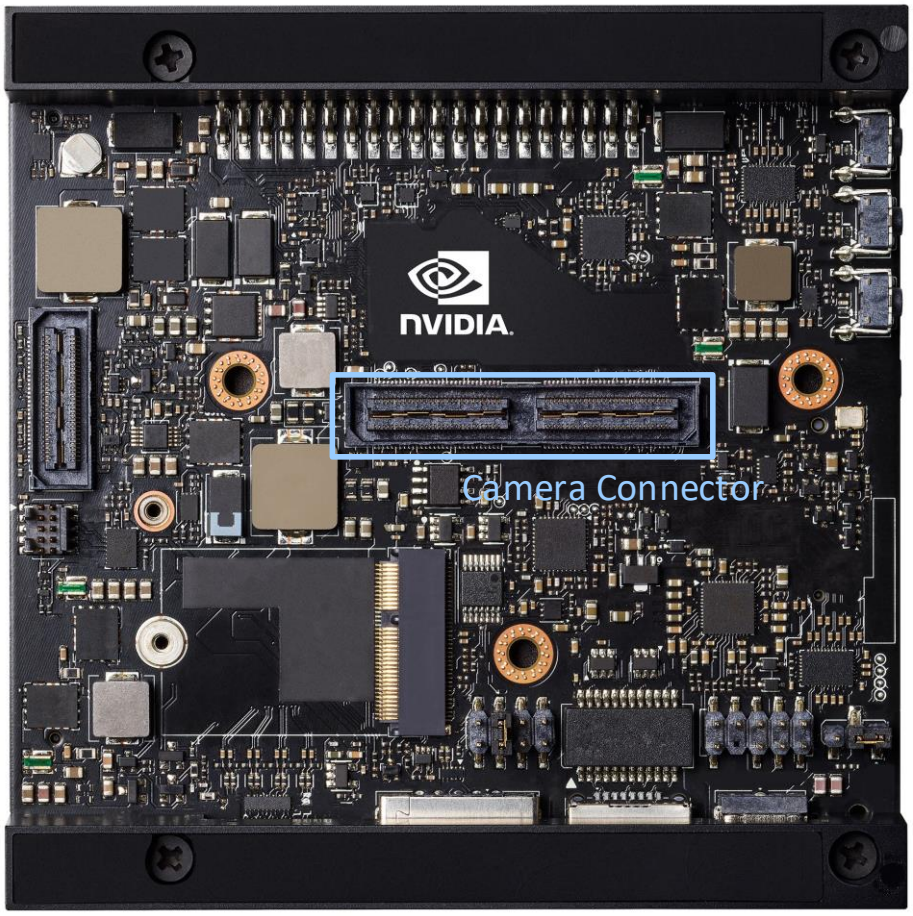
Items to be checked:

- Power distribution and usage
- I2C addressing
- EEPROM selection and control
- Pinout table
- Mechanical (connector and board outline)

2.1 System Setup

- Jetson AGX Xavier Developer Kit
- Camera Interposer Module- support from 1 to 6 CSI cameras
  - Up to 36 cameras can be supported by using an aggregator and the NVIDIA® Xavier™ virtual channel feature
  - Alternately, a GMSL de-serializer module
- Camera Sensor Module(s)

Figure 2-1. Jetson AGX Xavier Developer Kit Carrier Board



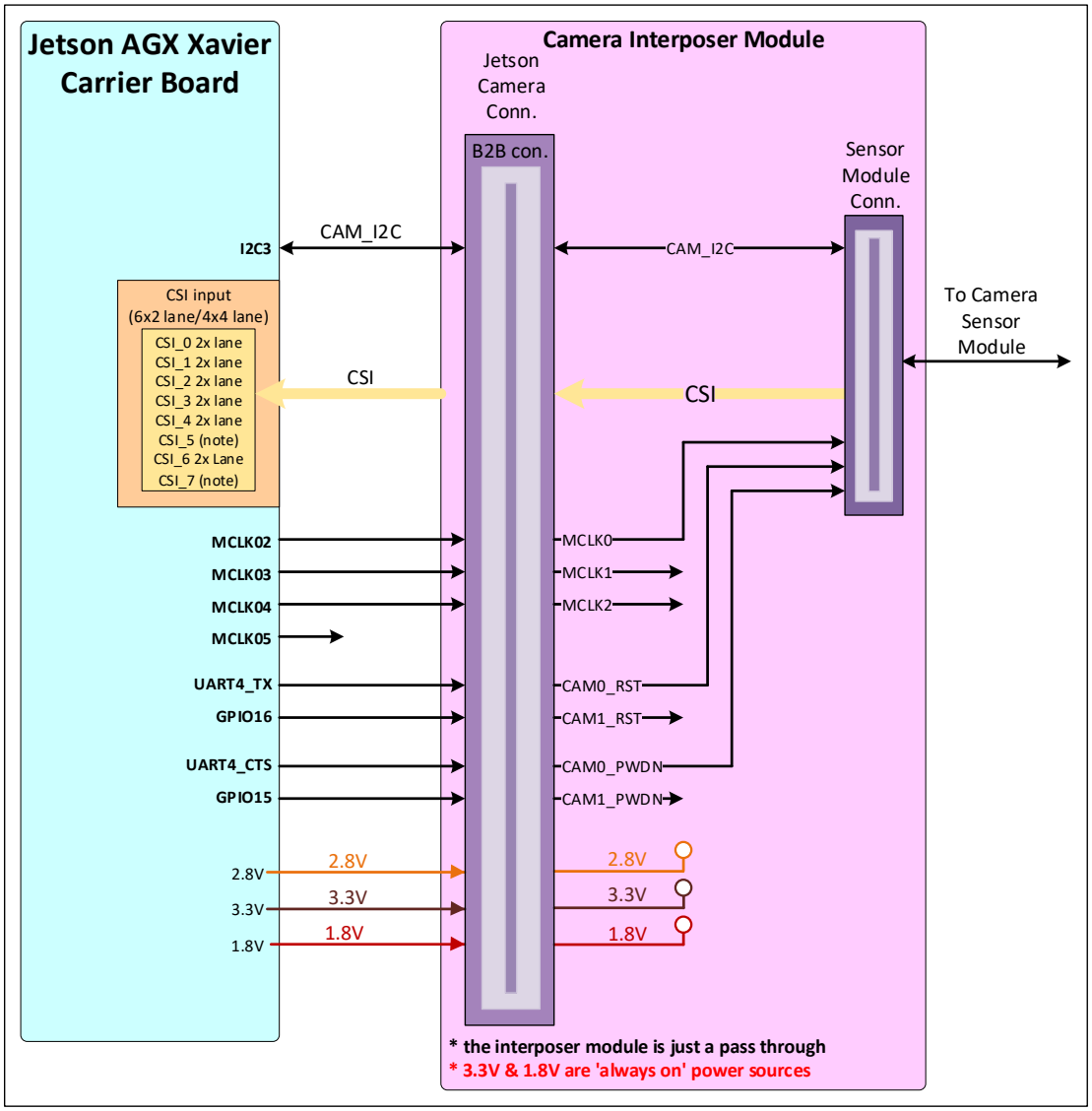
2.2 CSI Camera Interposer Module

The section details the camera interposer module for Jetson AGX Xavier series.

2.2.1 Single Camera Case

When using a single camera sensor, the camera interposer module will be a simple pass-through to the camera sensor module, with no EEPROM or I2C MUX on the interposer.

Figure 2-2. Single Camera Case Block Diagram



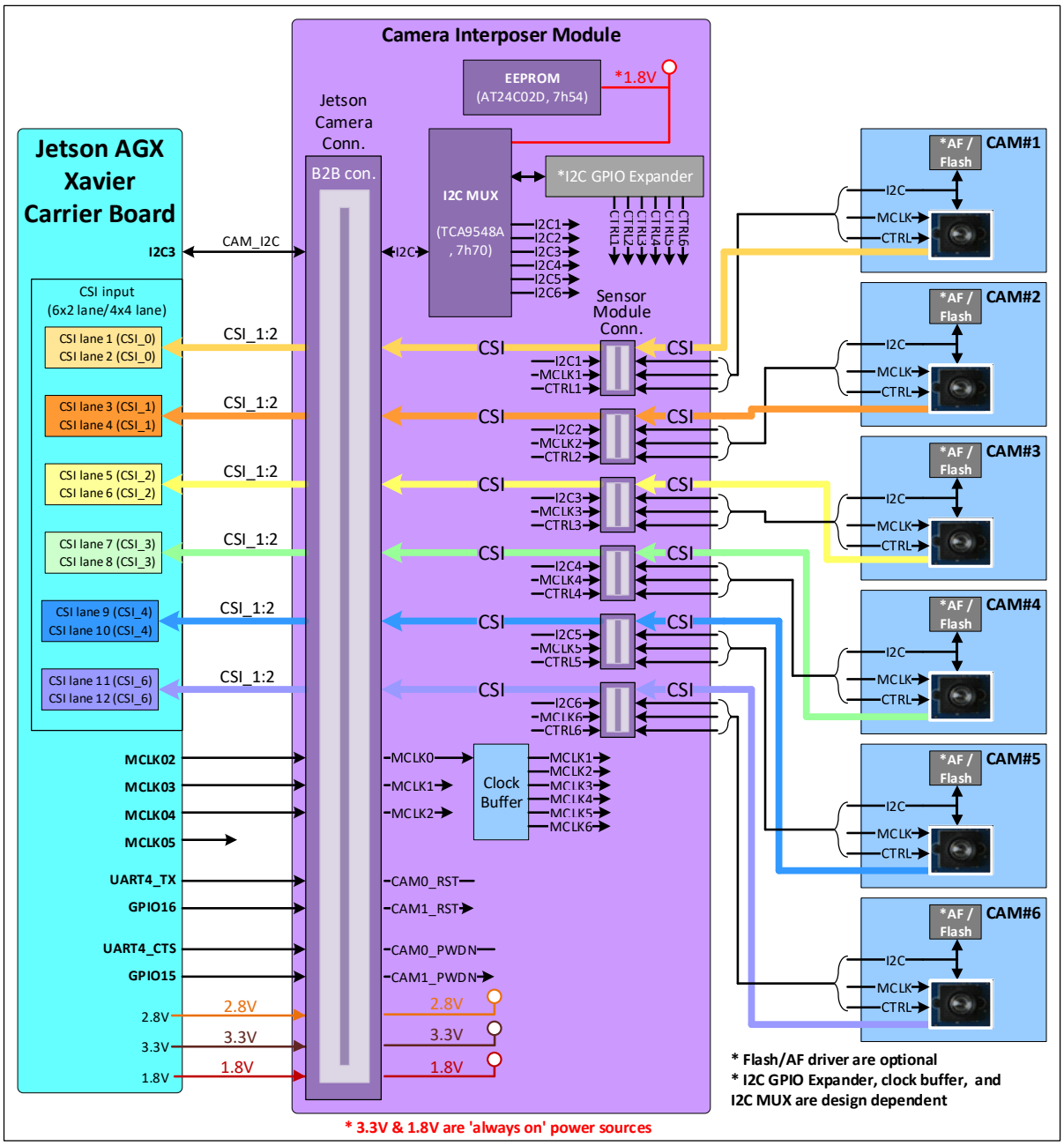
2.2.2 Multiple Camera Case

When multiple camera sensors are used (up to 6 CSI interfaces) with the developer kit, a camera interposer module with EEPROM is required. The EEPROM stores board/module IDs and information about the I2C mux that the software needs to perform camera auto detection.

An I2C mux or expander would be required on the camera interposer if some or all the camera sensors have the same I2C addresses. An MCLK clock buffer may also be needed to help with signal integrity. These are optional and depend on the design requirements. The following figure is a block diagram for a multiple camera use case. It shows the EEPROM, I2C muxes,

and MCLK buffer and a GPIO expander on the interposer board. In addition, each module shows an Auto Focus (AF) / Flash block. These are optional features.

Figure 2-3. Multiple Camera Case Block Diagram

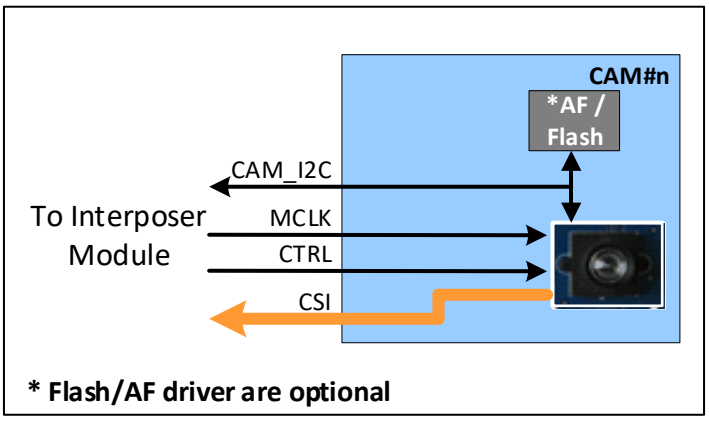


Note: The clock buffer shown in the figure is only to create separate clocks for the various modules. Full clock synchronization is beyond the scope of this use case.

2.2.3 Camera Sensor Module

Figure 2-4 is the block diagram for a camera sensor module when there are multiple camera sensors.

Figure 2-4. Camera Sensor Module Block Diagram



2.2.4 Jetson Camera Connector Pinout Table

This section contains the pinout table which provides the camera's connector pins listing and description.

Table 2-1. Jetson Camera Connector 2 x 60 Pinout

Pin	Signal Name	Description	Type/Dir	(V)	Pin	Signal Name	Description	Type/Dir	(V)
1	CSI_0_D0_P	CSI 0 Lane 0	Output	1.2	2	CSI1_D0_P	CSI 1 Lane 0	Output	1.2
3	CSI_0_D0_N		Output	1.2	4	CSI1_D0_N		Output	1.2
5	GND	Ground	Ground	0	6	GND	Ground	Ground	0
7	CSI_0_D0_P	CSI 0 Clock	Output	1.2	8	CSI1_CLK_P	CSI 1 Clock	Output	1.2
9	CSI_0_D0_N		Output	1.2	10	CSI1_CLK_N		Output	1.2
11	GND	Ground	Ground	0	12	GND	Ground	Ground	0
13	CSI0_D1_P	CSI 0 Lane 1	Output	1.2	14	CSI1_D1_P	CSI 1 Lane 1	Output	1.2
15	CSI0_D1_N		Output	1.2	16	CSI1_D1_N		Output	1.2
17	GND	Ground	Ground	0	18	GND	Ground	Ground	0
19	CSI2_D0_P	CSI 2 Lane 0	Output	1.2	20	CSI3_D0_P	CSI 3 Lane 0	Output	1.2
21	CSI2_D0_N		Output	1.2	22	CSI3_D0_N		Output	1.2
23	GND	Ground	Ground	0	24	GND	Ground	Ground	0
25	CSI2_CLK_P	CSI 2 Clock	Output	1.2	26	CSI3_CLK_P	CSI 3 Clock	Output	1.2
27	CSI2_CLK_N		Output	1.2	28	CSI3_CLK_N		Output	1.2

Pin	Signal Name	Description	Type/Dir	(V)	Pin	Signal Name	Description	Type/Dir	(V)
29	GND	Ground	Ground	0	30	GND	Ground	Ground	0
31	CSI2_D1_P	CSI 2 Lane 1	Output	1.2	32	CSI3_D1_P	CSI 3 Lane 1	Output	1.2
33	CSI2_D1_N		Output	1.2	34	CSI3_D1_N		Output	1.2
35	GND	Ground	Ground	0	36	GND	Ground	Ground	0
37	CSI4_D0_P	CSI 4 Lane 0	Output	1.2	38	CSI6_D0_P	CSI 6 Lane 0	Output	1.2
39	CSI4_D0_N		Output	1.2	40	CSI6_D0_N		Output	1.2
41	GND	Ground	Ground	0	42	GND	Ground	Ground	0
43	CSI4_CLK_P	CSI 4 Clock	Output	1.2	44	CSI6_CLK_P	CSI 6 Clock	Output	1.2
45	CSI4_CLK_N		Output	1.2	46	CSI6_CLK_N		Output	1.2
47	GND	Ground	Ground	0	48	GND	Ground	Ground	0
49	CSI4_D1_P	CSI 4 Lane 1	Output	1.2	50	CSI6_D1_P	CSI 6 Lane 1	Output	1.2
51	CSI4_D1_N		Output	1.2	52	CSI6_D1_N		Output	1.2
53	GND	Ground	Ground		54	GND	Ground	Ground	0
55	DVDD_CAM_ LV	Unused camera supply pin	Power		56	DVDD_CAM_ LV	Unused camera supply pin	Power	
57					58				
59	CSI5_D0_P	CSI 5 Lane 0	Output	1.2	60	CSI7_D0_P	CSI 7 Lane 0	Output	1.2
61	CSI5_D0_N		Output	1.2	62	CSI7_D0_N		Output	1.2
63	GND	Ground	Ground	0	64	GND	Ground	Ground	0
65	CSI5_CLK_P	CSI 5 Clock	Output	1.2	66	CSI7_CLK_P	CSI 7 Clock	Output	1.2
67	CSI5_CLK_N		Output	1.2	68	CSI7_CLK_N		Output	1.2
69	GND	Ground	Ground	0	70	GND	Ground	Ground	0
71	CSI5_D1_P	CSI 5 Lane 1	Output	1.2	72	CSI7_D1_P	CSI 7 Lane 1	Output	1.2
73	CSI5_D1_N		Output	1.2	74	CSI7_D1_N		Output	1.2
75	I2C_GP3_CLK	Camera I2C clock	Bidir	1.8	76	NC	Unused	Unused	–
77	I2C_GP3_DAT	Camera I2C data	Bidir	1.8	78	NC	Unused	Unused	–
79	GND	Ground	Ground	0	80	GND	Ground	Ground	0
81	AVDD_CAM	2.8V Camera supply (LDO)	Power	2.8	82	AVDD_CAM_ 2V8	2.8V Analog Camera supply	Power	2.8
83					84	NC	Unused	Unused	–
85	NC	Unused	Unused	–	86	NC	Unused	Unused	–
87	I2C_GP2_CLK	General Purpose I2C #2 Clock	Bidir/OD	1.8	88	CAM1_ MCLK03	Camera #1 Master Clock	Input	1.8
89	I2C_GP2_DAT	General Purpose I2C #2 Data	Bidir/OD	1.8	90	GPIO15_ CAM1_PWDN	Camera #1 Powerdown	Input	1.8

Pin	Signal Name	Description	Type/Dir	(V)	Pin	Signal Name	Description	Type/Dir	(V)
91	CAM0_ MCLK02	Camera #0 Master Clock	Input	1.8	**92**	GPIO16_ CAM1_RST	Camera #1 Reset	Input	1.8
93	CAM0_PWDN	Camera #0 Powerdown	Input	1.8	**94**	CAM2_ MCLK04	Camera #2 Master Clock	Input	1.8
95	CAM0_RST	Camera #0 Reset	Input	1.8	**96**	NC	Unused	Unused	–
97	NC	Unused	Unused		**98**	NC	Unused	Unused	–
99	GND	Ground	Ground	0	**100**	GND	Ground	Ground	0
101	DVDD_CAM_ IO	Unused Camera supply pin	Power		**102**	VDD_1V8	1.8V Camera supply.	Power	1.8
103	NC	Unused	Unused		**104**	NC	Unused	Unused	–
105	I2C_GP4_CLK	General I2C #4 Clock	Bidir/OD	1.8	**106**	NC	Unused	Unused	–
107	I2C_GP4_DAT	General I2C #4 Data	Bidir/OD	1.8	**108**	VDD_3V3	3.3V supply	Power	3.3
109	NC	Unused	Unused	–	**110**				
111	NC	Unused	Unused	–	**112**	NC	Unused	Unused	–
113	NC	Unused	Unused	–	**114**	NC	Unused	Unused	–
115	GND	Ground	Ground	0	**116**	GND	Ground	Ground	0
117	NC	Unused	Unused	–	**118**	VDD_3V3	3.3V supply	Power	3.3
119	GPIO25_VDD_ SYS_EN	System power enable	Input	1.8	**120**				

Legend Ground | Power | Reserved

Note: In the Type/Dir column, Output is to from the camera module. Input is to the camera module. Bidir is for bidirectional signals. OD is for Open-Drain.

2.2.5 Camera Module Power

Power sources from the NVIDIA® Jetson® connector are listed in Table 2-2.

Table 2-2. Power Source

Net Name	Specification	Note
VDD_3V3	3.3V, with the current coming from four pins, all of which are on a single "row" (see note for maximum current).	This is an 'always on' power, so it is not recommended to use it as a power source requiring power sequence.
AVDD_CAM_2V8	2.8V, with the current coming from three pins, one of which is on the same "row" as the 3.3V pins and the other two on another "row" (see note for maximum current).	2.8V analog power. Derived by an LDO on the NVIDIA Carrier Board and enabled by the Jetson AGX Xavier GPIO36 signal.
VDD_1V8	1.8V, with the current coming from a single pin on the same "row" as the 3.3V pins and one 2.8V pin (see note for maximum current).	This is an 'always on' power, so it is not recommended to use it as a power source requiring power sequence.

Note: The Samtec connector specification limits the current to 2A per pin (one pin powered per row). A row is defined as each of the 30 pin segments per side. Since there are six power pins assigned to the row 62-120 (even pins), these should be limited to 2A total maximum. If this current is not enough for the requirements of a camera module design, an external supply may be needed, or the designer should get approval from Samtec before exceeding 2A per row. If an external supply is used, care must be taken that pins common with the Jetson AGX Xavier module or developer kit carrier board are not powered before the developer kit is fully powered.

Proper power sequence is required in order not to damage the Jetson module.

- All camera powers except 1.8V for EEPROM should be 'Off' by default
- Powers should be controlled by Jetson AGX Xavier

2.2.6 I2C Address

This section provides the I2C address description for the camera interposer module and camera sensor module. The I2C addresses shown in the following table are what were used on the camera interposer and module boards designed by NVIDIA. These specific I2C addresses are not required. If the I2C address for the EEPROM device is different, this will need to be added to the address list in the EEPROM Manager. The I2C address for the I2C mux is stored in the EEPROM.

Table 2-3. I2C Address

Jetson Carrier Board	Camera Interposer Module		Each Camera Sensor Module	
CAM_I2C	EEPROM, AT24C02D	7'h54	*Flash driver IC (optional)	
	I2CMUX, TCA9546A	7'h70	*Auto focus driver (optional)	
	*I2C GPIO Expander (optional)			

2.2.7 CSI Camera Module Components

This section details the components for the Jetson AGX Xavier Series camera module.

2.2.7.1 Camera Module EEPROM

Camera modules intended to be compatible with the developer kit must implement the EEPROM on the interposer board or camera module for single module designs. For product-specific implementations incorporating the Jetson module, the EEPROM can be omitted and initialization mechanism is the responsibility of the partner/customer.

- Camera interposer module EEPROM power rail should be 'ON' by default
- Features:
  - 2-Kbit (256 × 8)
  - I2C-compatible up to 400 KHz (FM) at 1.8V
  - AT24C02D from Atmel is recommended
- The EEPROMs allow Jetson to dynamically detect the interposer board and the camera module(s) connected to it, and to load the corresponding device tree files

Table 2-4. EEPROM Structure

EEPROM Byte Absolute Address	Description	Data	Comments
Byte - 0	Version - Major	0x00	Major Version of BoardID Contents (Integer) - increments on backwards-incompatible changes
Byte - 1	Version - Minor	0x02	Minor Version of BoardID Contents (Integer) - increments on backwards-compatible changes within Major Version
Byte - 2 thru 19	RESERVED	0xFF	
Byte - 20 Thru 49	Product Part Number		Asset Tracker for Customer board design: Byte-20 = 0xCC, Bytes 21-49: Customer assigned unique string with zero-termination. Eg: Company Name/Stock Ticker followed by design/rev. This field should contain characters A-Z, a-z, 0-9 and dash ONLY (Eg: NVDA-12345)
Byte - 50 Thru 88	RESERVED	0xFF	
User Data Section			
Byte - 89	Camera Interposer Board I2C MUX-1	0x70	I2C MUX-1 7-bit Address
Byte - 90		0x01	I2C MUX Type (Refer to the rows below for Type Code Vs Part# Mapping)
Byte - 91 thru 254	RESERVED	0xFF	
Byte - 255	CRC		CRC-8 Computed for Bytes 0 thru 254.
I2C MUX Type Code Vs Part# Mapping			
MUX Type Code	Part#		Description
1	TCA9548A		8 Channel I2C MUX

2.2.7.2 I2C MUX

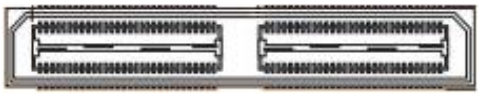
An I2C Mux is only required if there are multiple devices on the same I2C bus that have the same I2C slave address. Camera modules intended to be compatible with the developer kit must use an I2C mux that is compatible with the one MUX type listed in the EEPROM. For product-specific implementations incorporating the Jetson module, the partner/customer can choose the MUX of their choice but will be responsible for the software support.

- I2C MUX must be used to isolate all camera sensor modules
- Features:
  - 4-Channel outputs
  - I2C-compatible up to 400 KHz (FM) at 1.8V
  - TCA9548PWR from TI is recommended

2.2.7.3 Jetson Camera Connector

The Board to Board (B2B) connector on the Jetson AGX Xavier carrier board is the Samtec QSH-060-01-H-D-A-K-TR.

Figure 2-5. Jetson Camera Connector



Mating terminal connector to be used: QTH-060-xx-F(H)-D-A-x

- xx = 01 for 5.00 mm B2B spacing
- xx = 02 for 8.00 mm B2B spacing
- xx = 03 for 11.00 mm B2B spacing
- xx = 04 for 16.00 mm B2B spacing

2.2.8 Optional

This section details the options for the camera module.

2.2.8.1 I2C GPIO Expander

- An I2C GPIO expander can be used to expand control signals for camera sensor module(s)
- Features:
  - 8-bit bi-directional GPIO expansion
  - I2C-compatible up to 400 KHz (FM) at 1.8V

2.2.8.2 Clock Buffer and XTAL

- There are two clock outputs from the Jetson module:
  - MCLK0
  - MCLK1
- It is recommended to use the clocks from Jetson, but a clock buffer can be used to drive multiple clocks from a single source
- An external Crystal can be used if dynamic frequency switching from the AP is not needed for the sensor

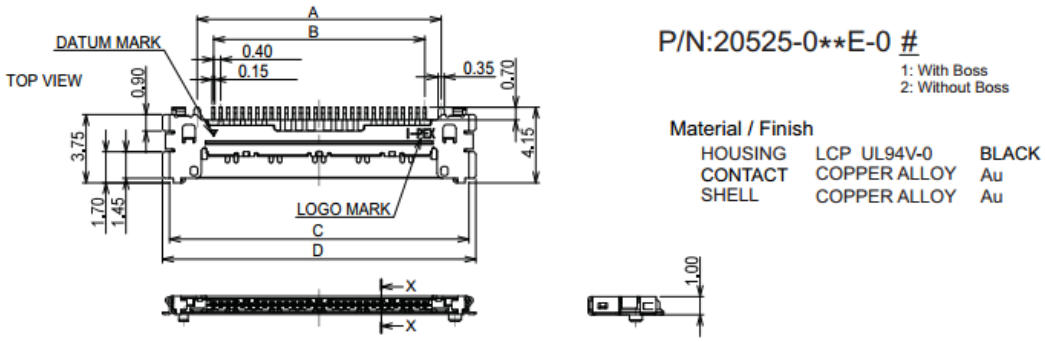
2.2.9 Example

The following example is a six, 2-CSI Lane camera configuration. See Figure 2-3. Other configurations are possible including 4-CSI lane camera configurations with up to four cameras, or more than 6 cameras with the use of an aggregator and the virtual channel feature supported by Jetson AGX Xavier.

- Example setup with up to 6 cameras with 2 CSI lane cameras
- Six cables with plug are also needed to connect interposer module to sensor modules
- Each connector needs to accommodate the following signals
  - Powers (as needed):
    - VDD_3V3
    - AVDD_CAM_2V8
    - VDD_1V8
  - CSI_CLK and CSI_DATA: 2 data lanes each
  - MCLK from the module (possibly through a buffer) or clock from local XTAL(s) on interposer or camera modules
  - CAM_I2C (CLK, DAT)
  - CAM_RST and CAM_PWDN (as required by camera modules)
  - Other control signals as needed
- Ex) I-PEX connector
  - Ex. 20525-030-02C

Figure 2 8 is an example connector between the camera sensor module and the camera interposer module.

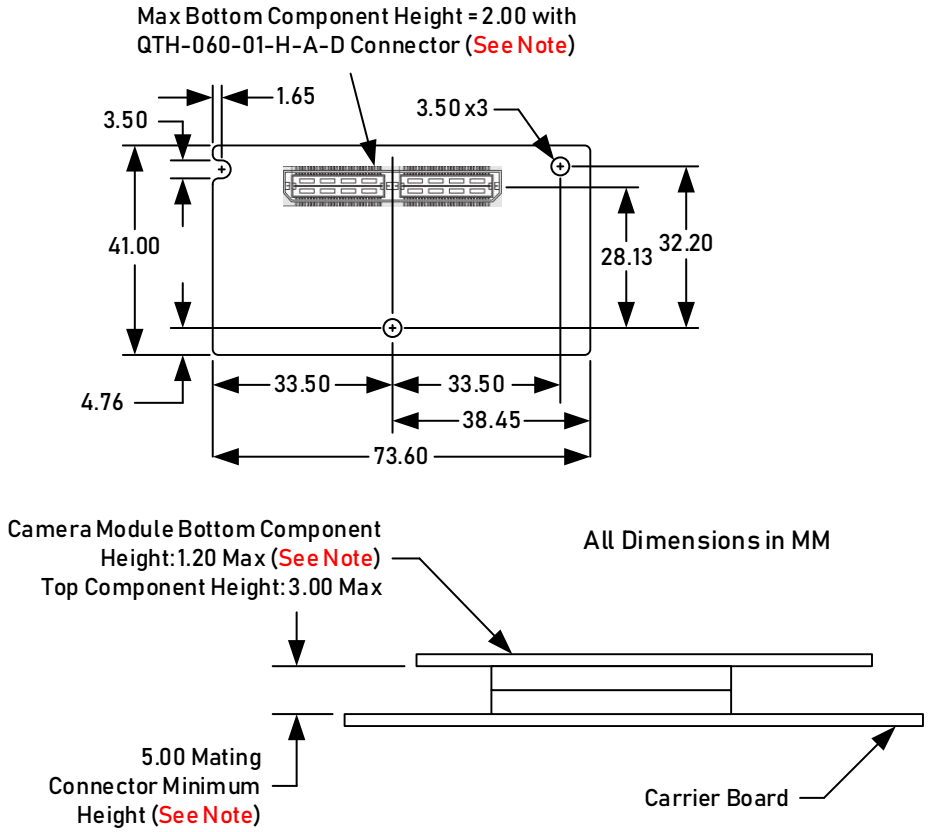
Figure 2-6. I-PEX 30-Pin Connector



2.3 Mechanical

The recommended outline for an interposer module if used with the NVIDIA Jetson AGX Xavier Developer Kit is shown in Figure 2-7. This outline will also ensure compatibility with future Developer Kits that use the same camera connector.

Figure 2-7. Recommended Interposer Module Outline



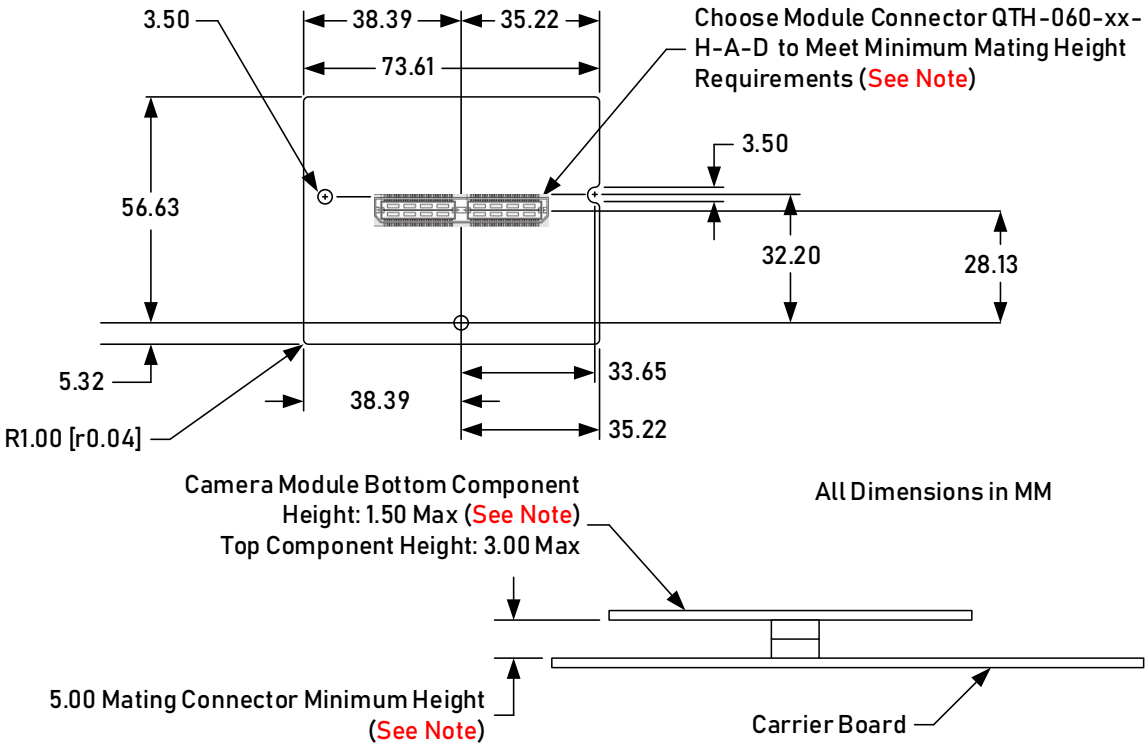
Note: The bottom component height maximum allowed depends on the camera module connector used:

- QTH-060-01-H-A-D (5.00 mm Spacing) = 1.2 mm maximum bottom component height
- QTH-060-02-H-A-D (8.00 mm Spacing) = 4.2 mm maximum bottom component height
- QTH-060-03-H-A-D (11.00 mm Spacing) = 7.2 mm maximum bottom component height
- QTH-060-04-H-A-D (16.00 mm Spacing) = 12.2 mm maximum bottom component height

A larger interposer board could be used with the Jetson AGX Xavier Developer Kit carrier board but may not be compatible with future Developer Kits supporting the same connector. The mechanical limits shown in Figure 2-7 will ensure the interposer module will fit on a Jetson AGX Xavier Developer Kit carrier board if the mating connector used is the minimum height (QTH-060-01-H-A-D with 5.00 mm board to board spacing) and the maximum component height on the bottom of the module is 1.5 mm. If taller versions of the connector

are used, the outline could be extended and/or the maximum component height below the module can be increased. If the QTH-060-03-H-A-D (11.00 mm spacing) or QTH-060-04-H-A-D (16.00 mm spacing) connectors are used on the module, the board size is not limited (depending on the height of the components on the bottom of the module), although the feet on the Jetson AGX Xavier Developer Kit may have to be removed.

Figure 2-8. Mechanical Limits Interposer Module Outline



Note: See note under Figure 2-7

Chapter 3. GMSL Interposer Board

An alternative to connecting CSI cameras directly to Jetson AGX Xavier, is to use a GMSL link with a serializer at the camera end and a de-serializer near Jetson. This allows for much longer distances between the camera and the Jetson AGX Xavier platform. This section provides guidelines for designing an interposer board including a GMSL de-serializer to be plugged in the Developer Kit carrier board camera connector (J509). The information provided here should also help with the design of a custom design integrating a GMSL de-serializer.

Note: The Maxim MAX96712 GMSL to CSI de-serializer is used as an example in this section. If a different de-serializer is used, the signal mapping, control interfaces and signals may be different.

Items to be checked:

- Signal mapping from camera connector to de-serializer
- Control signals and interfaces
- Camera connector pinout (see previous section)
- Mechanical dimension requirements (see previous section)
- Power distribution and usage (see previous section)

3.1 System Setup

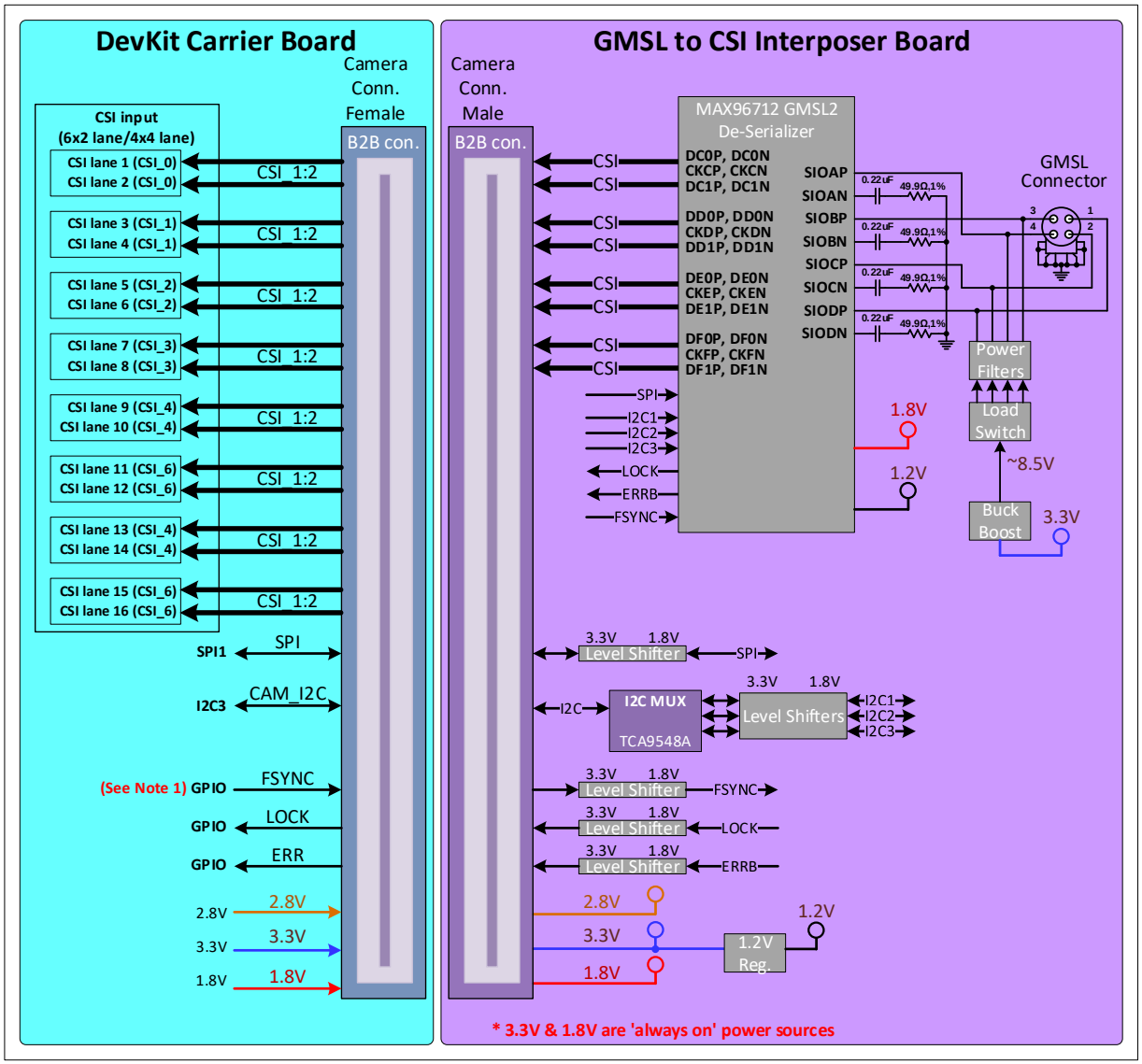
The system setup includes:

- Jetson AGX Xavier Developer Kit
- Camera Interposer Module with GMSL de-serializer
  - Up to 36 cameras can be supported by using an aggregator and the NVIDIA® Xavier™ virtual channel feature
- GMSL Camera Sensor Module(s)

3.2 GMSL Interposer Board/Module

The section details the camera interposer module for Jetson AGX Xavier series.

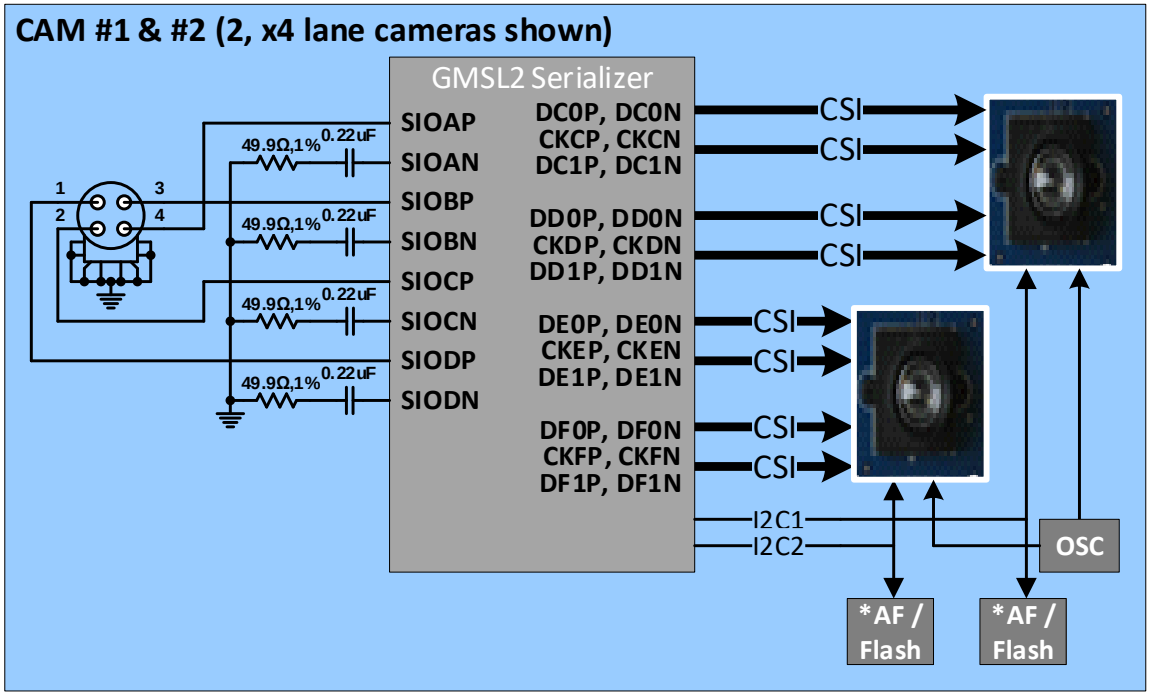
Figure 3-1. GMSL Interposer Board Example



3.2.1 GMSL Camera Sensor Module

Figure 3-2 is the block diagram for a GMSL camera sensor module.

Figure 3-2. GMSL Camera Sensor Module Block Diagram

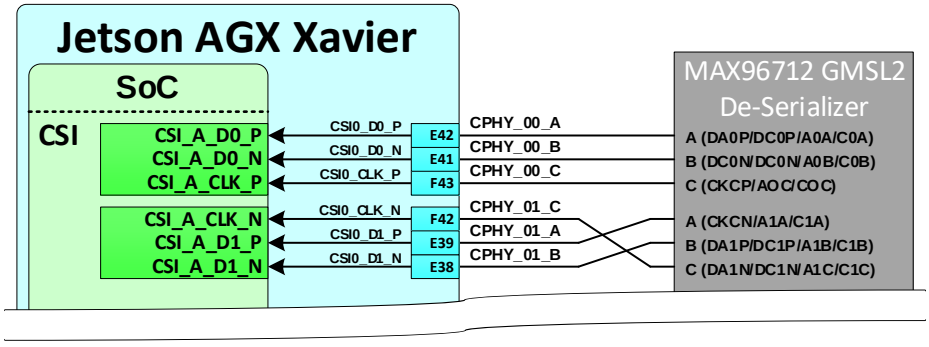


3.3 Jetson to De-Serializer Connections

Jetson AGX Xavier supports MIPI CSI D-PHY and C-PHY modes. The MAX96712 device is designed to support either type of CSI camera. If a design requires support for both D-PHY and C-PHY cameras, the CSI signal from Jetson AGX Xavier must be routed in a specific way. See Mapping #2 in Table 3-2: Xavier to Serializer C-PHY Signal Mapping.
If only C-PHY cameras need to be supported, the signals can be routed either to match Mapping #1 (match default Xavier output) or Mapping #2.
If the signals are routed to match Mapping #1, the internal Xavier C-PHY swizzle registers need to be configured to remap to match Mapping #2. Xavier does not support this flexible swizzling of the signals in D-PHY mode.

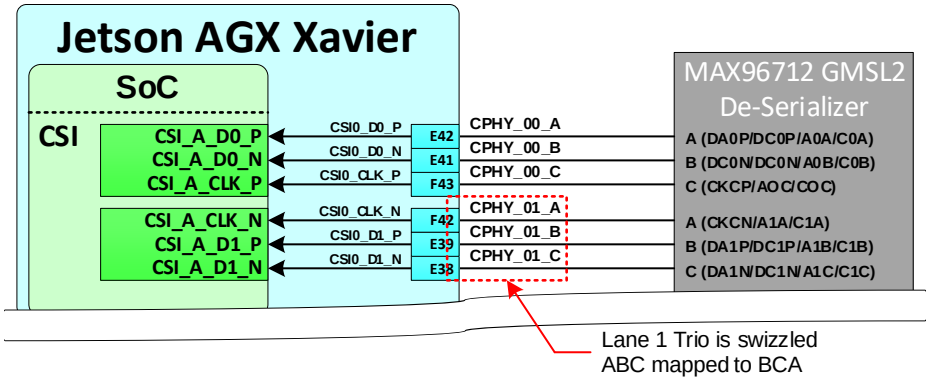
Figure 3-3 and Figure 3-4 show both approaches.

Figure 3-3. Signal Routing Using Default Xavier Mapping



Note: This signal routing connects the Xavier default signals to the Maxim de-serializer. This will work for both D-PHY and C-PHY cameras on the other end of the GMSL link.

Figure 3-4. Signal Routing with Xavier C-PHY Swizzle Mapping



Note: Since Xavier only supports the signal swizzling shown above for C-PHY mode, this method will not work if D-PHY cameras will be used on the other side of the GMSL link. The swizzle registers should be set as follows:

- POLARITY_SWIZZLE_CPHY0_A (control for lane 0): 000 = ABC to ABC
- POLARITY_SWIZZLE_CPHY1_A (control for lane 1): 010 = ABC to BCA

Table 3-1 lists the Xavier Swizzle register fields. For C-PHY, there are 6 options for either of the upper (lane 1) and lower (lane 0). For D-PHY there are only options to swap the polarity of the signals. The table also lists the options. These can be found in the Jetson AGX Xavier Technical Reference Manual.

Note: Note that the swizzling can only remap all trios in lane 0 or lane1 of each 2-lane block the same.

Table 3-1. Xavier Internal CSI Swizzle Register Bit Fields

NVCSI_PHY_0_NVCSI_CIL_A_POLARITY_SWIZZLE_CTRL_0		
Bit	Reset	Description
13:11	0x0	POLARITY_SWIZZLE_CPHY1_A: Polarity Swizzle control for Lane A1 in CPHY mode. valid only in CPHY mode 000 - A B C --> A B C 001 - A B C --> A C B 010 - A B C --> B C A 011 - A B C --> B A C 100 - A B C --> C A B 101 - A B C --> C B A
10:8	0x0	POLARITY_SWIZZLE_CPHY0_A: Polarity Swizzle control for Lane A0 in CPHY mode. valid only in CPHY mode 000 - A B C --> A B C 001 - A B C --> A C B 010 - A B C --> B C A 011 - A B C --> B A C 100 - A B C --> C A B 101 - A B C --> C B A
1	0x0	POLARITY_SWIZZLE_DPHY1_A: Polarity Swizzle control for Lane A1. register bit valid only in DPHY mode.
0	0x0	POLARITY_SWIZZLE_DPHY0_A: Polarity Swizzle control for Lane A1. register bit valid only in DPHY mode.

3.3.1 CSI Connections

Table 3-2 shows the two mappings described previously. Mapping #1 is the default signal mapping for Xavier. Mapping #2 matches the requirements for the MAX96712 de-serializer.

Table 3-2. Xavier to Serializer C-PHY Signal Mapping

Signal Name	Mapping #1	Mapping #2		Signal Name	Mapping #1	Mapping #2
CSI_A_D0_P	CPHY_A0_A	CPHY_A0_A		CSI_E_D0_P	CPHY_E0_A	CPHY_E0_A
CSI_A_D0_N	CPHY_A0_B	CPHY_A0_B		CSI_E_D0_N	CPHY_E0_B	CPHY_E0_B
CSI_A_CLK_P	CPHY_A0_C	CPHY_A0_C		CSI_E_CLK_P	CPHY_E0_C	CPHY_E0_C
CSI_A_D1_P	CPHY_A1_A	CPHY_A1_B		CSI_E_D1_P	CPHY_E1_A	CPHY_E1_B
CSI_A_D1_N	CPHY_A1_B	CPHY_A1_C		CSI_E_D1_N	CPHY_E1_B	CPHY_E1_C
CSI_A_CLK_N	CPHY_A1_C	CPHY_A1_A		CSI_E_CLK_N	CPHY_E1_C	CPHY_E1_A
CSI_B_D0_P	CPHY_B0_A	CPHY_B0_A		CSI_F_D0_P	CPHY_F0_A	CPHY_F0_A
CSI_B_D0_N	CPHY_B0_B	CPHY_B0_B		CSI_F_D0_N	CPHY_F0_B	CPHY_F0_B
CSI_B_CLK_P	CPHY_B0_C	CPHY_B0_C		CSI_F_CLK_P	CPHY_F0_C	CPHY_F0_C
CSI_B_D1_P	CPHY_B1_A	CPHY_B1_B		CSI_F_D1_P	CPHY_F1_A	CPHY_F1_B
CSI_B_D1_N	CPHY_B1_B	CPHY_B1_C		CSI_F_D1_N	CPHY_F1_B	CPHY_F1_C
CSI_B_CLK_N	CPHY_B1_C	CPHY_B1_A		CSI_F_CLK_N	CPHY_F1_C	CPHY_F1_A
CSI_C_D0_P	CPHY_C0_A	CPHY_C0_A		CSI_G_D0_P	CPHY_G0_A	CPHY_G0_A
CSI_C_D0_N	CPHY_C0_B	CPHY_C0_B		CSI_G_D0_N	CPHY_G0_B	CPHY_G0_B
CSI_C_CLK_P	CPHY_C0_C	CPHY_C0_C		CSI_G_CLK_P	CPHY_G0_C	CPHY_G0_C
CSI_C_D1_P	CPHY_C1_A	CPHY_C1_B		CSI_G_D1_P	CPHY_G1_A	CPHY_G1_B
CSI_C_D1_N	CPHY_C1_B	CPHY_C1_C		CSI_G_D1_N	CPHY_G1_B	CPHY_G1_C
CSI_C_CLK_N	CPHY_C1_C	CPHY_C1_A		CSI_G_CLK_N	CPHY_G1_C	CPHY_G1_A
CSI_D_D0_P	CPHY_D0_A	CPHY_D0_A		CSI_H_D0_P	CPHY_H0_A	CPHY_H0_A
CSI_D_D0_N	CPHY_D0_B	CPHY_D0_B		CSI_H_D0_N	CPHY_H0_B	CPHY_H0_B
CSI_D_CLK_P	CPHY_D0_C	CPHY_D0_C		CSI_H_CLK_P	CPHY_H0_C	CPHY_H0_C
CSI_D_D1_P	CPHY_D1_A	CPHY_D1_B		CSI_H_D1_P	CPHY_H1_A	CPHY_H1_B
CSI_D_D1_N	CPHY_D1_B	CPHY_D1_C		CSI_H_D1_N	CPHY_H1_B	CPHY_H1_C
CSI_D_CLK_N	CPHY_D1_C	CPHY_D1_A		CSI_H_CLK_N	CPHY_H1_C	CPHY_H1_A

3.4 Control Signals/Interfaces

The de-serializer used as reference is the MAX96712 device; it has several interfaces and control signals including I2C, SPI, FSYNC, ERRB, LOCK, and PWDNB.

These are described in the following sections

3.4.1 I2C

I2C is used as the control interface for the Maxim device as well as an option to pass through the GMSL link to control cameras. There are three I2C interfaces on the MAX96712 de-serializer. An I2C Mux can be used to supply the I2C interfaces. One option is to use the TCA9548PWR from TI, which is mentioned earlier in this document.

3.4.2 SPI

SPI is another interface that can be passed through the GMSL2 link for camera control. The MAX96712 supports up to two SPI interfaces, each with up to two chip selects. The Jetson AGX Xavier DevKit does not route SPI to the camera connector, so this option is available only to custom carrier board designs. If used, it is recommended that Jetson AGX Xavier is the master and the de-serializer is the slave.

3.4.3 Control/Handshake Signals

Signals for control and handshake with the de-serializer can be connected to available GPIOs on Jetson AGX Xavier. The DevKit camera connector has several available GPIO pins listed in Table 3-3. These are all 1.8V only pins.

Table 3-3. GPIO Pin Description

Pin #	Pin Name
Pin 88	Pin 88 (MCLK03
Pin 90	GPIO15
Pin 91	MCLK02
Pin 92	GPIO16
Pin 93	UART4_CTS
Pin 94	MCLK04
Pin 95	UART4_TX
Pin 119	GPIO25

The MAX96712 has control signals such as LOCK, ERRB, PWDNB and FRSYNC. These can each be connected to one of the above GPIOs on the camera connector, or other available GPIOs for a custom carrier board design. The FRSYNC signal can be used in three ways listed below. For the first two cases, any GPIO will work. For the last one that requires PWM functionality, a Jetson pin supporting this must be used. The DevKit camera connector does not have a pin with PWM capability.

- If FSYNC needs to be a periodic signal but does not need high accuracy (in terms of jitter), then SW can be used with a GPIO signal already on the 120-pin camera connector (of devkit).
- If FSYNC is a one-shot signal, a GPIO can be used
- If FSYNC needs to be a periodic signal with low jitter, PWM can be used. PWM functionality is supported on the pins listed below. See the Pinmux or Technical Reference Manual for more information.
  - GPIO35 (GP_PWM5)
  - FAN_PWM (GP_PWM4)
  - PWM01 (GP_PWM8)
  - GPIO27 (GP_PWM1)

Chapter 4. SLVS-EC Camera

4.1 SLVS Camera Connections for Developer Kit

This section is to be used when designing a camera module for use with the Jetson AGX Xavier Developer Kit carrier board PCIe x16 connector (J6) which supports SLVS (shared with PCIe interface).

Note: SLVS is supported by Jetson AGX Xavier, but not Jetson AGX Xavier Industrial (JAXi)

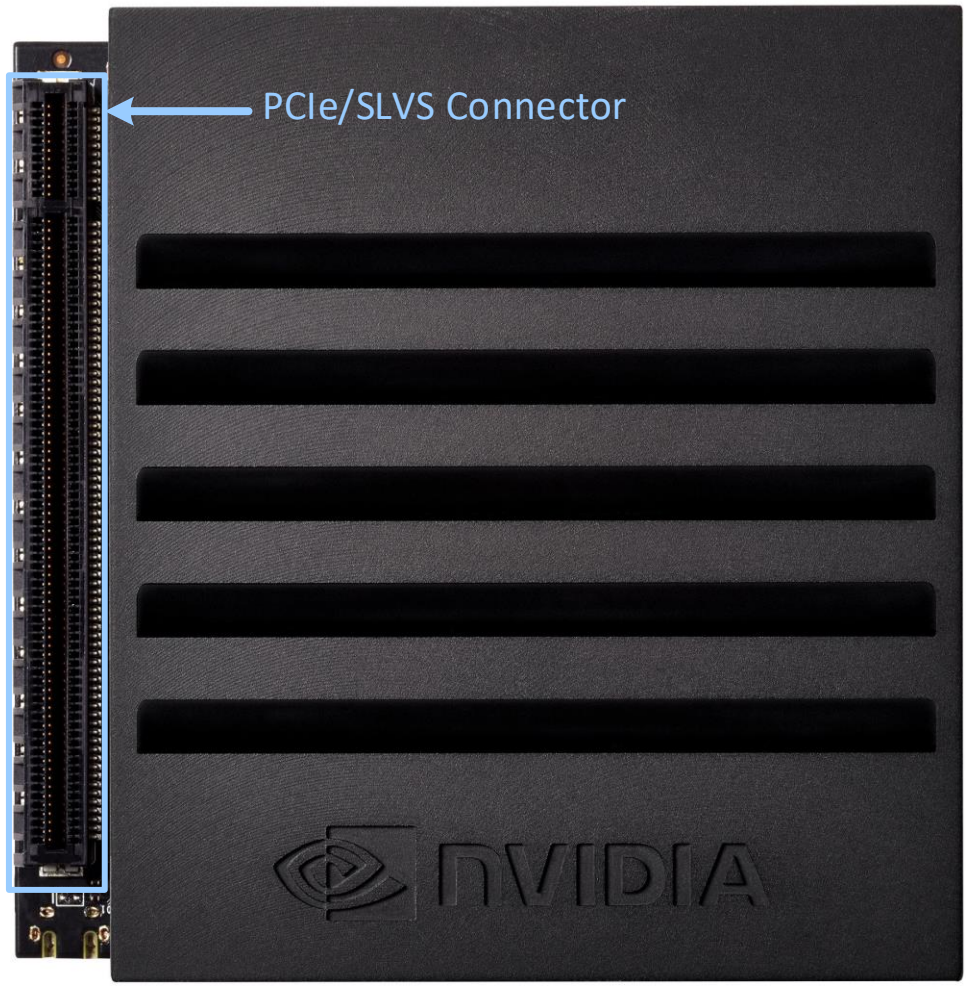
Items to be checked:

- Power distribution and usage
- I2C addressing (If required)
- EEPROM selection and control
- Pinout table
- Mechanical: connector and board outline

4.1.1 System Setup

- Jetson AGX Xavier Developer Kit
- SLVS Camera Board/Interposer Module
- SLVS Camera Sensor Module

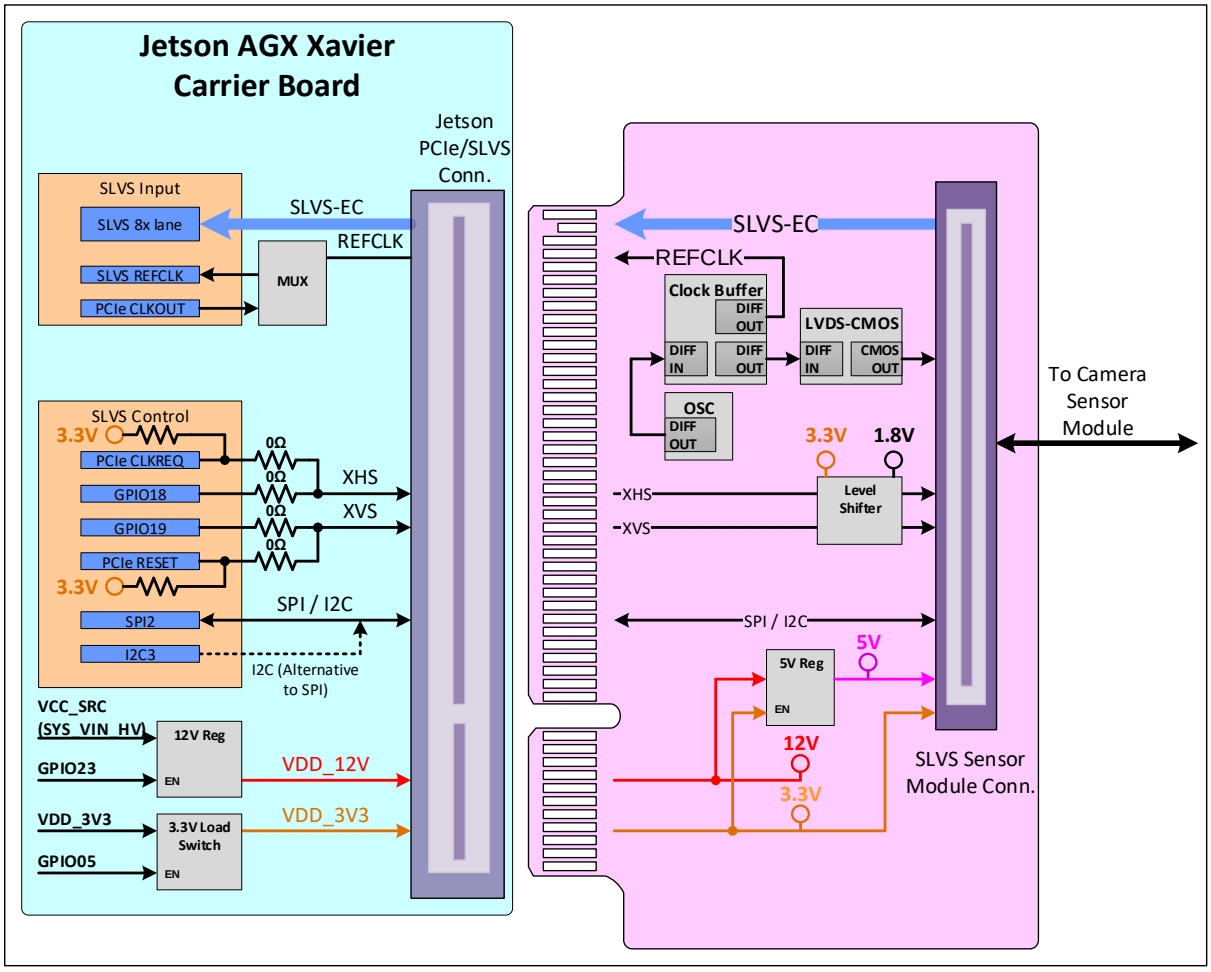
Figure 4-1. Jetson AGX Xavier Developer Kit Carrier Board



4.1.2 SLVS Developer Kit Camera Connections

This section covers the connections required for a SLVS board to plug into the Jetson AGX Xavier Developer Kit carrier board or for a board/module to connect to a custom carrier board designed around Jetson AGX Xavier.

Figure 4-2. Developer Kit SLVS Camera Connection Block Diagram



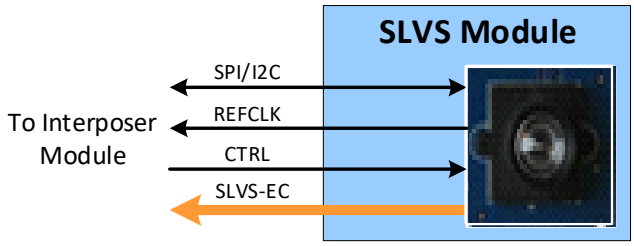
Note:

- A SLVS board designed to plug into the PCIe connector on the Jetson AGX Xavier Developer Kit carrier board must implement level shifters on the XHS and XVS signals as these are connected to PCIe CLKREQ and RST signals on the carrier board that are pulled to 3.3V.
- For details related to the oscillator, clock buffer and LVDS-CMOS converter circuit, see the Custom Carrier Board section.

4.1.3 SLVS Camera Sensor Module

Figure 4-3 is a block diagram for a camera sensor module when there are multiple camera sensors.

Figure 4-3. SLVS Camera Sensor Module Block Diagram



4.1.4 Developer Kit SLVS Connector Pinout Tables

This section contains the pinout table which provides the camera's connector pins listing and description.

Table 4-1. Developer Kit SLVS Connector Pinout

Pin #	Module Pin Name	Module Pin #s	Usage/Description	Type/ Direction	Pin #	Module Pin Name	Module Pin #s	Usage/Description	Type/ Direction
A1	–	–	Ground	Ground	**B1**	–	–	12V Supply	Power
A2	–	–	12V Supply	Power	**B2**				
A3					**B3**				
A4	–	–	Ground	Ground	**B4**	–	–	Ground	Ground
A5	SPI2_SCK	E61	SPI 2 Clock	Output	**B5**	I2C_GP0_CLK		General I2C #0 Clock	Bidir/OD
A6	SPI2_MISO	D62	SPI 2 Master In/Slave Out	Input	**B6**	I2C_GP0_DAT		General I2C #0 Data	Bidir/OD
A7	SPI2_MOSI	F60	SPI 2 Master Out/Slave In	Output	**B7**	–	–	Ground	Ground
A8	SPI2_CS0	D60	SPI 2 Chip Select #0	Output	**B8**	–	–	3.3V supply	Power
A9	–	–	3.3V supply	Power	**B9**	SPI3_MISI	D56	SLVS XCLR	Output
A10					**B10**	–	–	3.3V Auxiliary supply	Power
A11	PEX_L5_RST_N GPIO19 (See Note 1)	H10 K56	PCIe Lane 0 Reset	Output	**B11**	PEX_WAKE_N SPI3_MOSI	A8 G56	PCIe Wake (Shared) SLVS XCE	Input
A12	–	–	Ground	Ground	**B12**	PEX_L5_CLKREQ_N GPIO18 (See Note 3)	C8 C55	PCIe (#5) Clock Req. SLVS XHS	Bidir
A13	PEX_CLK5_P (Note 2) NVHS_SLVS_REFCLK_P	F24 E30	PCIe (#5) Ref Clock Output or SLVS Ref Clock Input	See Usage/ Desc	**B13**	–	–	Ground	Ground
A14	PEX_CLK5_N (Note 2) NVHS_SLVS_REFCLK_N	F25 E31			**B14**	NVHS0_TX0_P	H24	PCIe (#5) Lane 0 Transmit	Output
A15	–	–	Ground	Ground	**B15**	NVHS0_TX0_N	H25		
A16	NVHS0_SLVS_RX0_P	D24	PCIe (#5) or SLVS Lane 0 Receive	Input	**B16**	–	–	Ground	Ground
A17	NVHS0_SLVS_RX0_N	D25			**B17**	–	–	PRSNT2 – No connect	NC
A18	–	–	Ground	Ground	**B18**	–	–	Ground	Ground
A19	–	–	Reserved	Reserved	**B19**	NVHS0_TX1_P	K25	PCIe (#5) Lane 1 Transmit	Output
A20	–	–	Ground	Ground	**B20**	NVHS0_TX1_N	K24		
A21	NVHS0_SLVS_RX1_P	B25	PCIe (#5) or SLVS Lane 1 Receive	Input	**B21**	–	–	Ground	Ground
A22	NVHS0_SLVS_RX1_N	B24			**B22**				

Pin #	Module Pin Name	Module Pin #s	Usage/Description	Type/ Direction	Pin #	Module Pin Name	Module Pin #s	Usage/Description	Type/ Direction
A23	–	–	Ground	Ground	**B23**	NVHS0_TX2_P	G27	PCIe (#5) Lane 2 Transmit	Output
A24					**B24**	NVHS0_TX2_N	G26		
A25	NVHS0_SLVS_RX2_P	C27	PCIe (#5) or SLVS Lane 2 Receive	Input	**B25**	–	–	Ground	Ground
A26	NVHS0_SLVS_RX2_N	C26			**B26**				
A27	–	–	Ground	Ground	**B27**	NVHS0_TX3_P	J26	PCIe (#5) Lane 3 Transmit	Output
A28					**B28**	NVHS0_TX3_N	J27		
A29	NVHS0_SLVS_RX3_P	A26	PCIe (#5) or SLVS Lane 3 Receive	Input	**B29**	–	–	Ground	Ground
A30	NVHS0_SLVS_RX3_N	A27			**B30**	PWM01	K57	SLVS Focus PWM	Output
A31	–	–	Ground	Ground	**B31**	–	–	PRSNT2 – No connect	NC
A32	GPIO27	H52	SLVS IRIS PWM	Output	**B32**	–	–	Ground	Ground
A33	–	–	Reserved	Reserved	**B33**	NVHS0_TX4_P	H28	PCIe (#5) Lane 4 Transmit	Output
A34	–	–	Ground	Ground	**B34**	NVHS0_TX4_N	H29		
A35	NVHS0_SLVS_RX4_P	D28	PCIe (#5) or SLVS Lane 4 Receive	Input	**B35**	–	–	Ground	Ground
A36	NVHS0_SLVS_RX4_N	D29			**B36**				
A37	–	–	Ground	Ground	**B37**	NVHS0_TX5_P	K29	PCIe (#5) Lane 5 Transmit	Output
A38					**B38**	NVHS0_TX5_N	K28		
A39	NVHS0_SLVS_RX5_P	B29	PCIe (#5) or SLVS Lane 5 Receive	Input	**B39**	–	–	Ground	Ground
A40	NVHS0_SLVS_RX5_N	B28			**B40**				
A41	–	–	Ground	Ground	**B41**	NVHS0_TX6_P	G31	PCIe (#5) Lane 6 Transmit	Output
A42					**B42**	NVHS0_TX6_N	G30		
A43	NVHS0_SLVS_RX6_P	C31	PCIe (#5) or SLVS Lane 6 Receive	Input	**B43**	–	–	Ground	Ground
A44	NVHS0_SLVS_RX6_N	C30			**B44**				
A45	–	–	Ground	Ground	**B45**	NVHS0_TX7_P	J30	PCIe (#5) Lane 7 Transmit	Output
					B46	NVHS0_TX7_N	J31		
A47	NVHS0_SLVS_RX7_P	A30	PCIe (#5) or SLVS Lane 7 Receive	Input	**B47**	–	–	Ground	Ground
A48	NVHS0_SLVS_RX7_N	A31			**B48**	–	–	PRSNT2 – No connect	NC
A49	–	–	Ground	Ground	**B49**	–	–	Ground	Ground

Notes:

1. PEX_L5_RST_N and GPIO19, PEX_L5_CLKREQ_N and GPIO18, PEX_WAKE_N and SPI3_MOSI are tied together on the carrier board and the PCIe control signals are pulled to 3.3V on the module. If any of these SLVS control signals operate at 1.8V on the camera module, level shifters will be required.
2. The selection for either PEX_CLK5_P/N or NVHS_SLVS_REFCLK_P/N is determined by a mux on the carrier board. The mux is controlled by the module GPIO6 pin (low = PEX_CLK5, high = SLVS_REFCLK.
3. This table shows only the PCIe x8 section of the connector as this is the only portion used. The rest of the x16 signal connections are no-connects (except GND pins).
4. In the Type/Dir column, Output is to the PCIe connector. Input is from the PCIe connector. Bidir is for bidirectional signals.

Legend	Ground	Power	Reserved

4.1.5 SLVS Power

Power sources from the NVIDIA Jetson connector are listed in Table 4-2.

Table 4-2. SLVS Power Source

Connector Pin Name	Net Name	Specification	Note
+12V	VDD_12V	12.0V, 3A maximum supported across the five +12V power pins.	This power rail is enabled by the GPIO05 signal from the module. The enable defaults to on.
+3.3V	PEX_3V3	3.3V, 3A maximum supported across the three +3.3V power pins.	This power rail is enabled by the GPIO27 signal from the module. The enable defaults to on.
+3.3VAUX	VDD_3V3	3.3V, 1A maximum supported on the single +3.3VAUX power pin.	This is an 'always on' power, so it is not recommended to use it as a power source requiring power sequence.

Since the power supplies in Table 4-2 are all on by default, if the SLVS camera or associated circuitry requires any specific power sequencing, this should be handled on the interposer board.

4.1.6 SLVS Components

This section details the components for SLVS camera module.

4.1.6.1 SLVS EEPROM

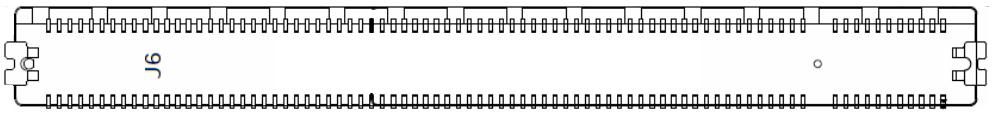
SLVS Camera boards or modules are not required to include an EEPROM but can be included to allow Jetson to dynamically detect the interposer board/camera module. If implemented, the following requirements should be met:

- Camera interposer module EEPROM power rail should be 'ON' by default
- Features:
  - 2-Kbit (256 × 8)
  - I2C-compatible up to 400 KHz (FM) at 1.8V
  - AT24C02D from Atmel is recommended
- The EEPROM structure is the same as in Table 2-4 in Chapter 2.

4.1.6.2 Jetson SLVS Camera Connector

The PCIe connector on the Jetson AGX Xavier carrier board is an Amphenol 10146065-113Y0LF.

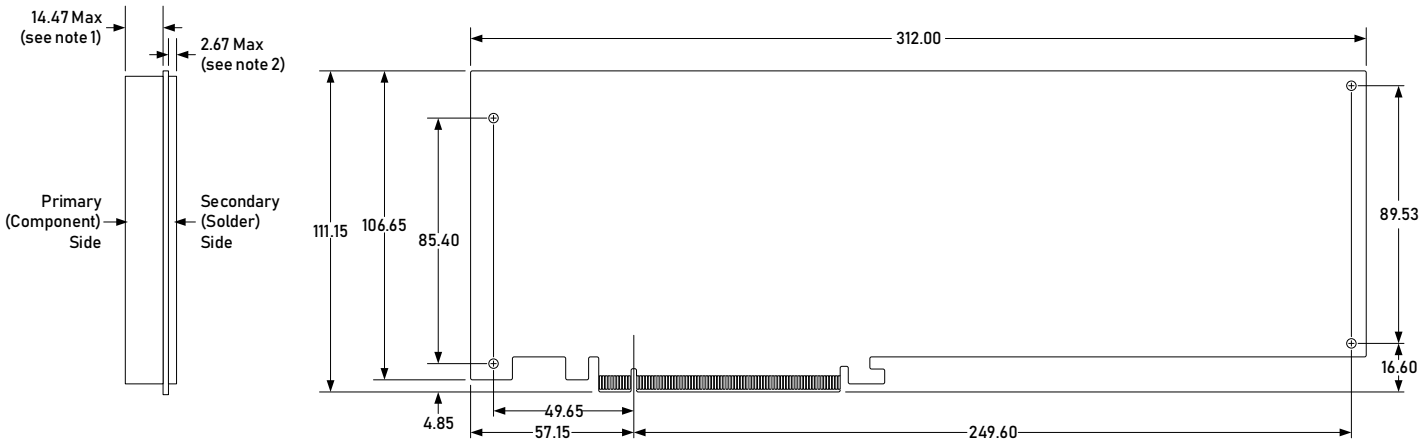
Figure 4-4. Jetson SLVS PCIe Form Factor Camera Connector



4.1.7 SLVS Mechanical

The NVIDIA Jetson AGX Xavier Developer Kit supports a standard PCIe x16 connector and can support up to a full size PCIe card. The following figure shows some of the PCIe specification dimensions for a full-size x16 card. Only the x8 portion of the connector is used. The figure is shown as a reference only. An actual SLVS card could use just x8 fingers and be smaller than what is shown. There are no obstructions that would preclude having the board exceed the dimensions shown for length or height.

Figure 4-5. PCIe Form Factor Interposer Module Dimensions



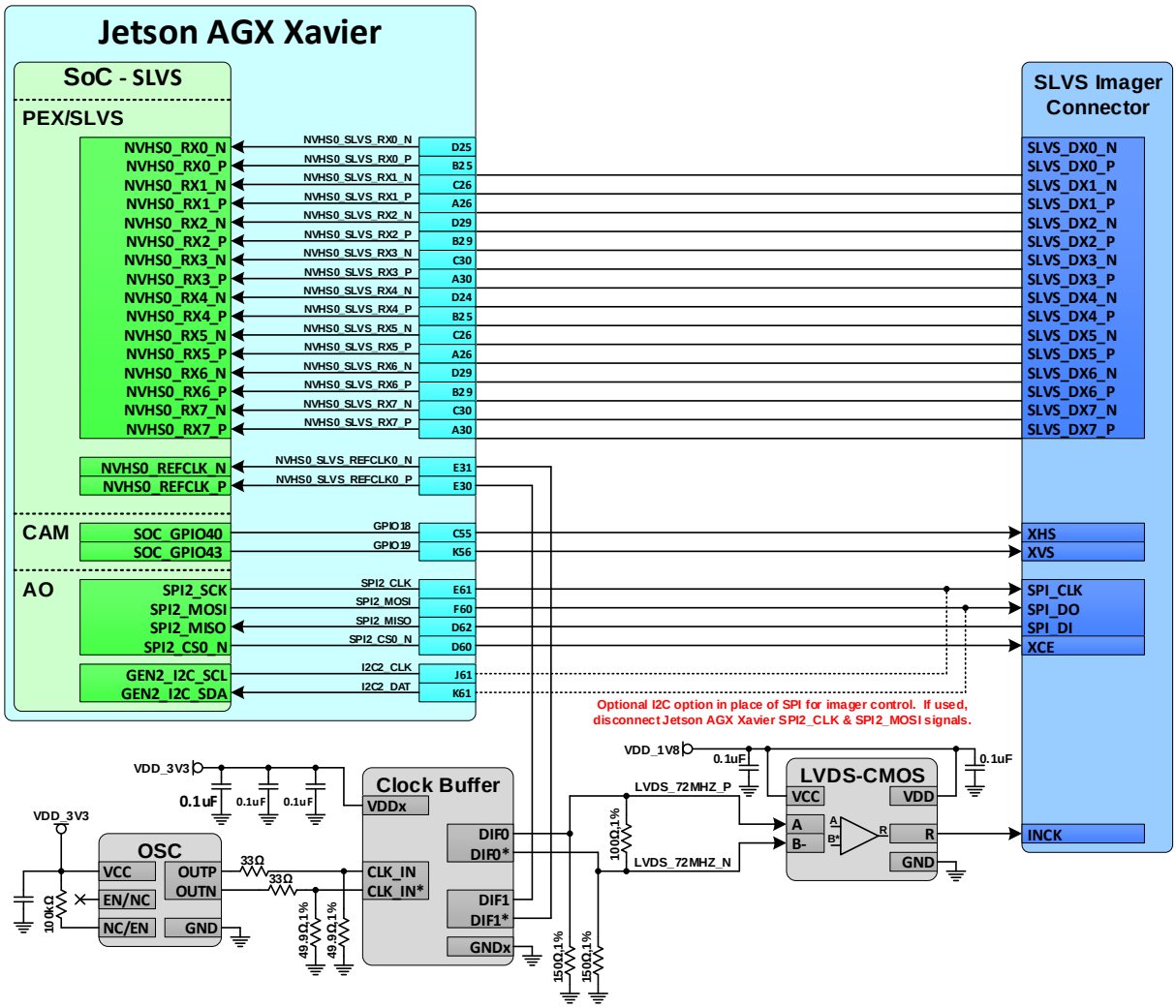
Notes:

1. This is the maximum allowed for a single slot PCIe card, but a triple slot card can be up to 55.12 mm max. Since the component side of the board faces away from the developer kit, the height restrictions do not need to be met.
2. The PCIe board solder side faces the developer kit heat sink. There is ~7 mm between the back of the board to the heat sink, so the solder side max height restriction could be violated somewhat, but components should be kept from getting too close to the heat sink to avoid possible thermal or electrical shorting issues.

4.2 SLVS Connections for Customer Carrier Board

The following figure shows the connections required for a custom carrier board.

Figure 4-6. Custom Carrier Board SLVS Camera Connection Details



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