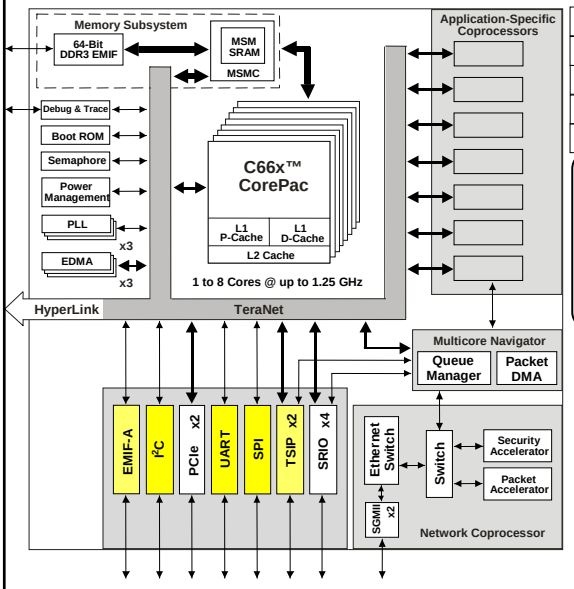
KeyStone Training

External Interfaces: EMIF-A, UART, I²C, SPI, and TSIP

External Interfaces



CorePac & Memory Subsystem
Memory Expansion
Multicore Navigator
Network Coprocessor
External Interfaces

- EMIF-A for booting and logging
- SPI for boot operations
- UART for development/testing
- I²C for EPROM at 400 Kbps
- Telecommunications Serial Port (TSIP) x2 for media applications

Agenda

- External Memory Interface (EMIF-A)
- Universal Asynchronous Receiver/Transmitter (UART)
- Inter-IC Control Module (I2C)
- Serial Port Interface (SPI)
- Telecommunications Serial Port (TSIP)

External Memory Interface (EMIF-A)

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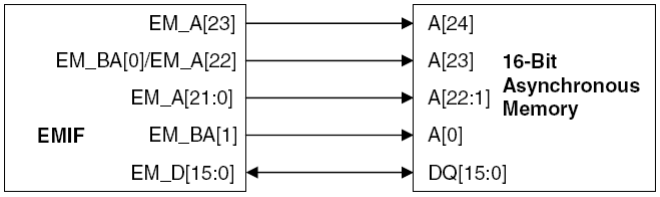
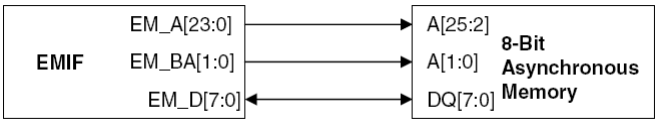
EMIF-A (Media Applications Only)

- Used for booting, logging, etc.
  - Supports NAND flash memory up to 256 MB.
  - Supports NOR flash up to 16 MB
  - Supports asynchronous SRAM mode up to 1MB
  - SDRAM support is not available.
  - OneNand support is not available.
- The EMIF controller supports a 16-bit interface:
  - 4x CE (Chip Enable) pins
  - 1x write strobe
  - 1x read strobe
  - 1x read/write enable pin
  - 2x BE (Big Endian) pins
  - 16 data pins
  - 24 address pins
  - 2x wait pins
- For the EMIF interface, topologies supported are 2 x 8 and 1 x 16 asynchronous devices.

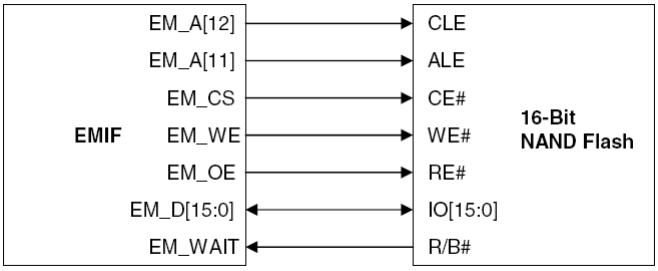
EMIF-A 16-bit SRAM Connection



EMIF-A 8-bit SRAM Connection



EMIF-A 16-bit NAND Connection



- EM_***A[23:0]*** = ***vbusp_address[25:2]***.
- ***Address bit 12th for CLE.***
- ***Address bit 11th for ALE.***
- ***Example:*** 0x70004000 for toggling CLE to be 1.
- ***Example:*** 0x70002000 for toggling ALE to be 1.

EMIF-A Memory Map

- The EMIF-A is connected to the CPU/3 main switch fabric via a VBUSM:P bridge performing 2:1 clock conversion and a CPU/6 32-bit VBUSP SCR which is shared by SPI, BOOTROM and all KeyStone masters are allowed to access this module.
- Default Memory Map
  - 0x20C00000~0x20C000FF
    - EMIF-A Config
  - 0x70000000~73FFFFFF (64MB)
    - EMIF-A CS2 Data Memory-CE2
  - 0x74000000~77FFFFFF
    - EMIF-A CS3 Data Memory-CE3
  - 0x78000000~7BFFFFFF
    - EMIF-A CS4 Data Memory-CE4
  - 0x7C000000~7FFFFFFF
    - EMIF-A CS5 Data Memory-CE5

EMIF-A: Events, Power, Clocking

- The memory type for each CE space is programmable. Default memory type is NOR flash.
- The EMIF-A has no DMA events. There is a single interrupt from the module which is routed to chip-level INTC.
- EMIF-A is inside always-on power domain.
- EMIF-A + SPI share a same clock domain. When not used, it can be clocked gated to save power.
- EMIF-A gets CPU/6 clock and the fastest memory expected to be used is the NOR flash. The maximum expected input (memory write) data rate is 356 Mbps. The maximum expected output (memory read) data rate is 320 Mbps. The data can flow in one direction only at a time.
- Boot mode for NAND/NOR flashes occurs through EMIF-A on KeyStone devices for media applications.

Universal Asynchronous Receiver/Transmitter (UART)

- External Memory Interface (EMIF-A)
- Universal Asynchronous Receiver/Transmitter (UART)
- Inter-IC Control Module (I2C)
- Serial Port Interface (SPI)
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UART Overview

- UART performs serial-to-parallel conversion on data received from a peripheral device or modem, and parallel-to-serial conversion on data received from the DSP side. The following baud rates will be supported for UART: 2.4K, 4.8K, 9.6K, 19.2K, 38.4K, 56K and 128K baud rates.
- Only the following 4 UART pins will be pinned out in the device: UART_RXD, UART_TXD, UART_CTS and UART_RTS. All the remaining UART pins will not be pinned out.
- The UART has a single 32-bit VBUSP slave port that is connected to CFG SCR (CPU/6). This is used for both data and configuration accesses. All masters have access to this port.
- Default Memory Map
  - 0x02540000~0x0254003F
    - UART Config/Data
- There are three events from the UART - Transmit event (UTXEVT), receive event (URXEVT) and the interrupt (UARTINT). Transmit and receive events are routed to TPCC directly and GEMs via the chip level INTC. UART interrupt is routed to GEMs via the chip level INTC.
- UART is inside always-on power domain and clock domain.

Inter-IC Control Module (I2C)

- External Memory Interface (EMIF-A)
- Universal Asynchronous Receiver/Transmitter (UART)
- Inter-IC Control Module (I2C)
- Serial Port Interface (SPI)
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I^2C Overview (1/2)

- The I^2C module supports both master and slave operation, allowing the CorePac to directly access slave devices through the I^2C interface or respond to externally generated commands.
  - Supports 400 Kbps throughput
  - Supports full 7-bit address field
  - Supports EEPROM size of 4 Mbit
  - No support for GPIO mode
  - No support for High-Speed (HS) mode
  - No support for 10-bit device addressing mode
- The I^2C has a single 32-bit VBUSP port for register access.
  - Provides access to the MMRs and data
  - Connected to the CPU/6 CFG TeraNet
- Default Memory Map
  - 0x02530000~0x0253007F
    - I2C Config&Data

I²C Overview (2/2)

- The I²C generates three event types:
  - Transmit event
  - Receive event
  - Interrupt event
- I²C event routing:
  - Transmit and receive events are routed to TPCC directly and CorePac via the chip level INTC.
  - The I2C interrupt is routed to CorePac through the chip-level INTC.
- I²C power and clocking:
  - Always-on power domain
  - Always-on clock domain
- I²C master and slave boot are supported.

Serial Port Interface (SPI)

- External Memory Interface (EMIF-A)
- Universal Asynchronous Receiver/Transmitter (UART)
- Inter-IC Control Module (I2C)
- Serial Port Interface (SPI)
- Telecommunications Serial Port (TSIP)

SPI Overview (1/2)

- The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (2 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI may be used to connect to serial flash memory devices for booting.
  - Operates at up to 66 MHz
  - Supports two chip selects
  - Supports master mode
  - No support for GPIO mode
  - No support for SPI slave mode
  - No support for SPIENA pin
- The SPI has a single 32-bit VBUSP port for register access at 1/6 the CPU frequency. This is used for access to the MMRs and data. The SPI is connected to the CPU/3 TeraNet SCR via a VBUSM:P bridge performing 2:1 clock conversion and a CPU/6 32-bit VBUSP TeraNet SCR which is shared by SPI, BOOTROM and EMIF-A.
- Default Memory Map
  - 0x20BF0000~0x20BF01FF
    - SPI Config&Data

SPI Overview (2/2)

- SPI has two error events and two DMA events.
- SPI receives a CPU/6 clock and the throughput is 57 Mbps.
- SPI is inside always-on power domain. EMIF-A + SPI share a same clock domain. When not used, it can be clocked gated to save power.
- SPI boot is supported.

Telecommunications Serial Port (TSIP)

- External Memory Interface (EMIF-A)
- Universal Asynchronous Receiver/Transmitter (UART)
- Inter-IC Control Module (I2C)
- Serial Port Interface (SPI)
- Telecommunications Serial Port (TSIP)

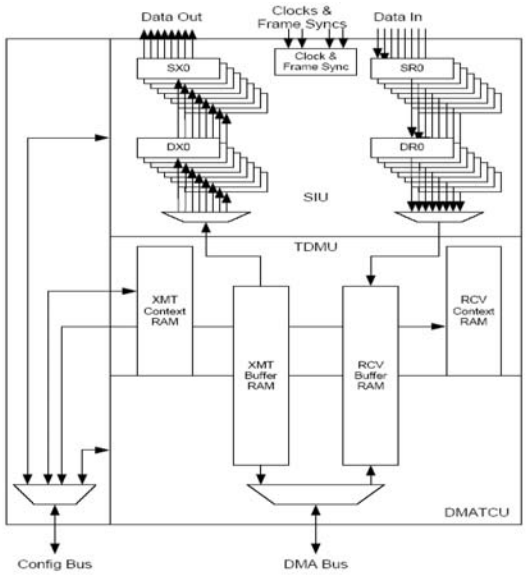
TSIP Overview (1/2)

- 2x TSIP are available only on KeyStone devices for media applications
  - Supports 1024 DS0s per TSIP
  - Supports 2, 4, or 8 lanes at 32.768, 16.384, or 8.192 Mbps per lane
- Two clock and frame sync inputs:
  - One receive clock
  - One transmit clock
- Redundant/common clocking
  - One receive/transmit clock
  - Second clock as backup
- Eight DMA channels per direction
  - Independent timeslot enable/disable per channel
  - A-law and m-law support on per timeslot basis
- Frame and SuperFrame interrupts
- 20-pin external interface

TSIP Overview (2/2)

- The TSIP has a single 32-bit VBUSP port for register access at the CPU/3 CFG crossbar frequency.
  - Used for access to the MMRs and data
  - Connected to main CPU/3 CFG TeraNet through a small CFG TeraNet, which multiplexes accesses with other similar configuration interfaces on the small CFG TeraNet
  - All masters are allowed access.
- TSIP has one 32-bit VBUM master port connected to CPU/3 Main TeraNet.
- Default Memory Map:
  - 0x01E00000~0x01E3FFFF
    - TSIP0 Config
  - 0x01E80000~0x01EBFFFF
    - TSIP1 Config
- TSIP is inside an always-on power domain.
- TSIP has a dedicated clock domain. When not used, it can be clocked gated to save power.
- TSIP receives a CPU/6 clock and the maximum wire-line rate for each TSIP module is 1024 timeslots per frame x 8-bits per timeslot x 8 kHz frame rate = 64 Mbps in each direction simultaneously.

TSIP Architecture



TSIP Interface

- At the standard rate and default configuration there are 8 transmit and 8 receive links that are active.
- Each serial interface link supports up to 128 8-bit timeslots.
- Number of active links are configurable.
- Maximum data rate is related to the number of enabled links.
- Data rate is configurable by enabling/disabling timeslots.
- The next few slides give examples on time slot assignment.

TSIP: H-MVIP Format Example (E1)

Timeslot Number	First E1 TS Number	Second E1 TS Number	Third E1 TS Number	Fourth E1 TS Number
0-3	0	0	0	0
4-7	1	1	1	1
7-11	2	2	2	2
12-15	3	3	3	3
16-19	4	4	4	4
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
120-123	30	30	30	30
124-127	31	31	31	31

TSIP: H-MVIP Format Example (T1)

Timeslot Number	First T1 DS0 Number	Second T1 DS0 Number	Third T1 DS0 Number	Fourth T1 DS0 Number
0-3	Undefined	Undefined	Undefined	Undefined
4-7	1	1	1	1
8-11	2	2	2	2
12-15	3	3	3	3
16-19	Undefined	Undefined	Undefined	Undefined
20-23	4	4	4	4
24-27	5	5	5	5
28-31	6	6	6	6
32-35	Undefined	Undefined	Undefined	Undefined
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
108-111	21	21	21	21
112-115	Undefined	Undefined	Undefined	Undefined
116-119	22	22	22	22
120-123	23	23	23	23
124-127	24	24	24	24

TSIP Example

FRAME SYNC REFERENCE			
L0-000 E1-1-00	L1-000 E1-5-00	L0-001 E1-2-00	L1-001 E1-6-00
L0-002 E1-3-00	L1-002 E1-7-00	L0-003 E1-4-00	L1-003 E1-8-00
L0-004 E1-1-01	L1-004 E1-5-01	L0-005 E1-2-01	L1-005 E1-6-01
L1-122 E1-7-30	L1-123 E1-8-30	Dummy	Dummy
FRAME SYNC REFERENCE			

- Consider a simple example using two H-MVIP links with E1 frames and one DMA channel.
  - TS0 from all E1 frames are enabled.
  - TS1 from the first two E1 frames on each link are enabled.
  - TS30 from the last two E1 frames on the second link are enabled.
- Naming convention
  - Ln is the link number
  - E1-nn is the frame number
  - -tt is the timeslot number on the E1 frame
  - -ttt is the timeslot number on the link.

TSIP in a Multicore Environment (1/2)

- TSIP Configuration MMRs can be accessed by any CorePac through TeraNet. Normally, one CorePac handles TSIP configuration.
- In TSIP, there are eight channels of both transmit and receive for a total of sixteen channels. One transmit and one receive channel are dedicated to each CorePac.
- For each transmit channel, the timeslot context is defined to support enable/disable control of all timeslots on all of the TSIP serial outputs.
- For each receive channel, the timeslot context control is defined to support enable/disable control of all timeslots on all of the TSIP serial inputs.

TSIP in a Multicore Environment (2/2)

- Each channel has a channel bitmap consisting of 64 32-bit words of memory for a total of 2048 bits. Each pair of bits controls the enable/disable state of a physical timeslot.
- Based on the channel bitmap setting, each channel transmits or receives assigned timeslots.
- All channels can enable the same physical timeslot, which means that the same data may be written to memories resulting in a multicast of the data.
- Source and destination addresses are programmable for the DMA engine inside TSIP.
  - For example, CorePac0 programs its L2 memory location as the destination address for receive.
  - TSIP DMA channel 0 (assigned to CorePac0) copies data in enabled timeslots (configured through bitmap setting) to CorePac0 L2 memory.
- Each CorePac receives interrupts triggered on an assigned channel.

For More Information

- Refer to the documentation for each interface:
  - External Memory Interface (EMIF-A) User Guide
    http://www.ti.com/lit/SPRUGZ3
  - Universal Asynchronous Receiver/Transmitter (UART) User Guide
    http://www.ti.com/lit/SPRUGP1
  - Inter-IC Control Module (I2C) User Guide
    http://www.ti.com/lit/SPRUGV3
  - Serial Port Interface (SPI) User Guide
    http://www.ti.com/lit/SPRUGP2
  - Telecommunications Serial Port (TSIP) User Guide
    http://www.ti.com/lit/SPRUGY4
- For questions regarding topics covered in this training, visit the support forums at the TI E2E Community website.