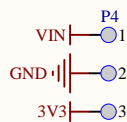


Conexão IO Externo



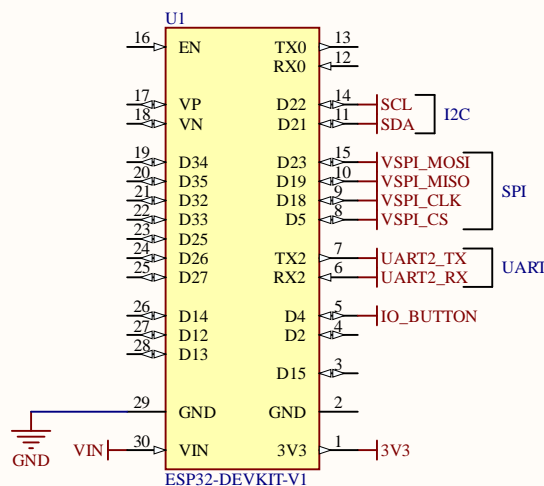
IO para retirar o ESP32 do modo hibernação

Alimentação Externa - 5V

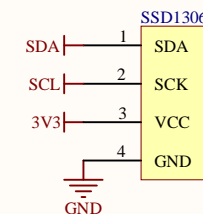


Pinos para alimentação externa de até 5V
e conexão com GND e pino 3V3

ESP32 -DOIT-DEVKIT-V1

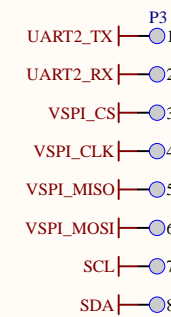


Display OLED 128 X 32



Pinos de conexão para o display



Conector para os pinos de comunicação



Conexões para o tipo de protocolo de
conexão escolhida (SPI, I2C e UART)

Copyright CNPEM 2022.

This documentation describes Open Hardware and is licensed under the CERN OHL S v2. You may redistribute and modify this documentation under the terms of the CERN OHL S v2. (<https://www.ohwr.org/cernohl>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL S v2 for applicable conditions.

Title: uSimar_PCB_V0.SchDoc		 CNPEM Centro Nacional de Pesquisas em Energia e Materiais	 SEI Sistemas Eletrônicos Instrumentação	ENT - AIS - SEI Sistemas Eletrônicos Instrumentação
Drawn by: Bruno Oliveira	Revision: v0.0			
Project: PCB_Project_uSimar_V0.PrjPcb				
Date: 31/01/2023	Time: 08:54:16			
Sheet 1 of 1				
File: C:\Users\Public\Documents\Altium\Projeto_uSIMAR_git(usimar-hw)\pcb\uSimar_PCB_V0.SchDoc				