

Design and Implementation of a Radiation Hardened High Output Current Transconductance Amplifier

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(Signature)



Abstract



Zusammenfassung



Acknowledgments



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1 Introduction

1.1 Novel DC Current Transformer

1.2 Specification

1.3 Technology

2 Theory

2.1 The Operational Transconductance Amplifier

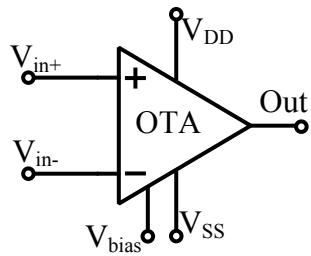


Figure 2.1.: Symbol of an OTA

2.1.1 Different Topologies

Conventional Current Mirror OTA

Super Class AB OTA

Folded Cascode OTA

2.2 The Opeartional Amplifier

2.2.1 Miller Compensation OP AMP

2.2.2 OP AMP as a Voltage Buffer



3 Design and Implementation

3.1 The Gm/Id Methodology

3.2 OTA Design

3.2.1 Schematic

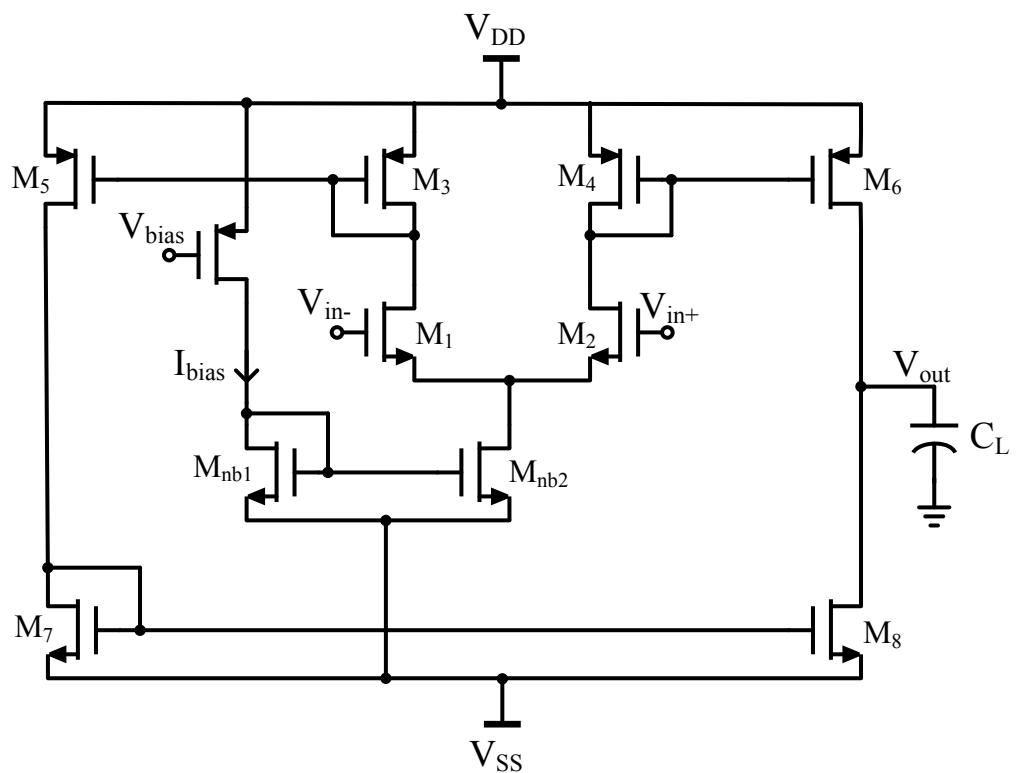


Figure 3.1.: Schematic of the OTA Designed

Transistor	Width	Length	Multiplier
M1	8u	500n	5
M2	8u	500n	5
M3	35u	500n	1
M4	35u	500n	1
M5	28u	500n	3
M6	35u	500n	3
M7	35u	500n	18
M8	33u	500n	18
M9	10u	500n	4
MnB1	20u	500n	8
MnB2	20u	500n	8

Table 3.1.: Dimensions of the Transistors of the designed OTA

3.2.2 Test Setup

DC Analysis

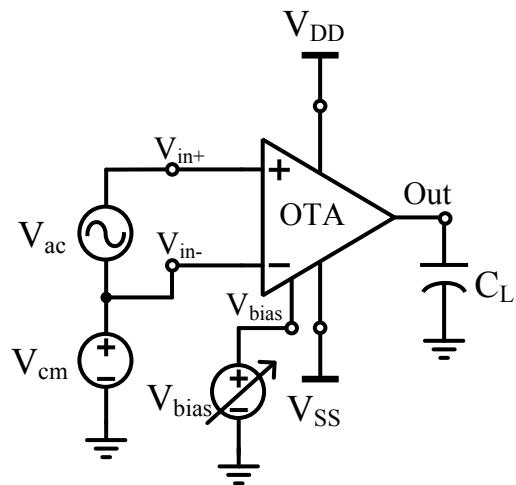


Figure 3.2.: OTA Test setup for AC, DC and Noise Analysis

Vbias (mV)	150	200	300	400	500	600	700
Output DC Bias (mV)	13.68	-16.43	-78.96	-144.6	-213.3	-285.2	-360.3

Table 3.2.: Output DC Bias Point of the OTA

AC Analysis

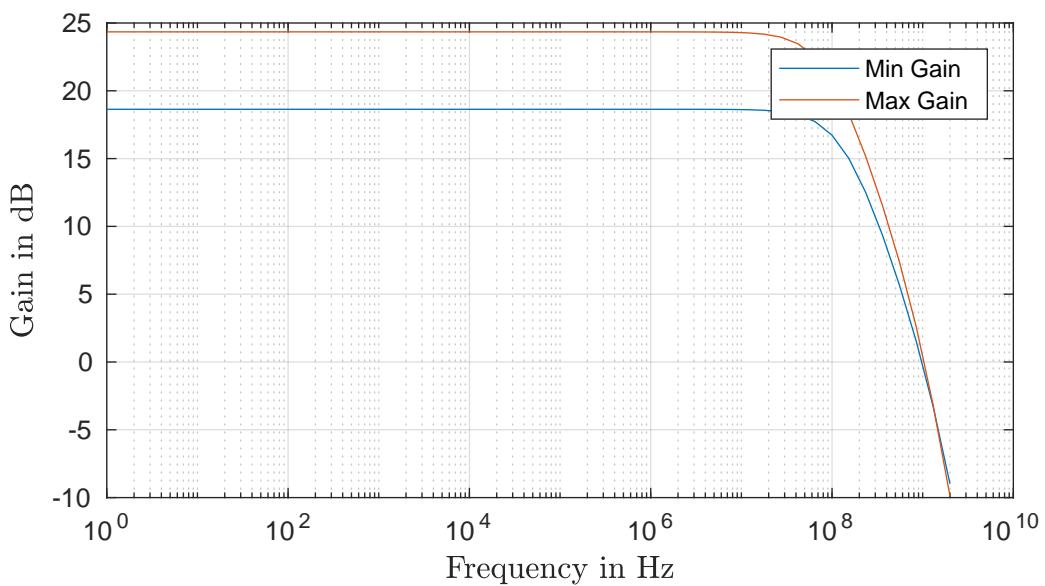


Figure 3.3.: OTA Plot of Gain vs Frequency for different Vbias

Vbias (mV)	150	200	300	400	500	600	700
Open Loop Gain (dB)	18.64	19.46	20.9	22.05	22.96	23.7	24.35
Phase Margin (degrees)	63.3	60.63	55.96	52.42	49.91	48.12	46.72
Bandwidth (MHz)	135	130.7	122.2	113.7	105	96.63	89.19

Table 3.3.: Open Loop Gain, Phase Margin and Bandwidth of the OTA

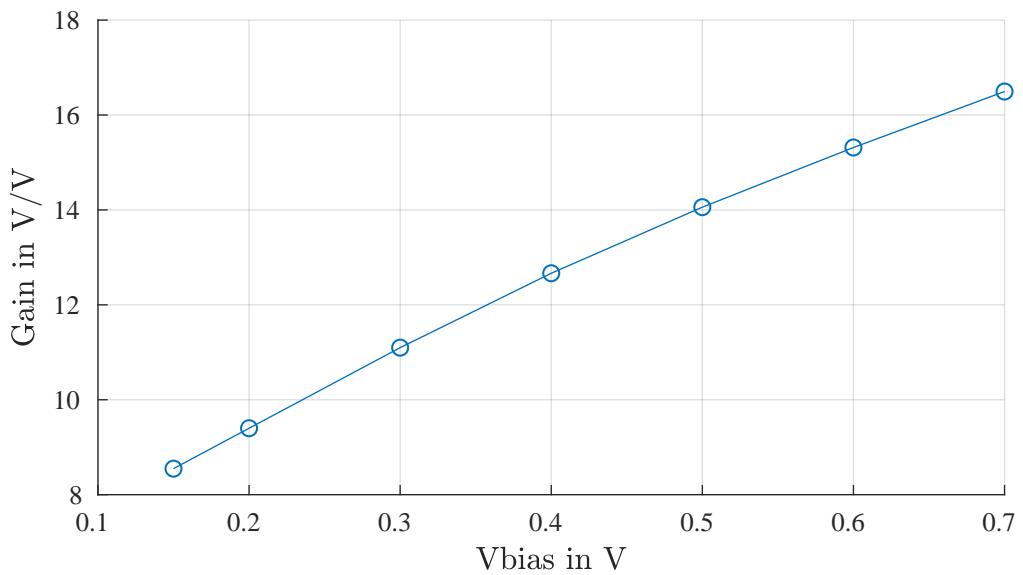


Figure 3.4.: OTA Plot of Gain vs Vbias

Vbias (mV)	150	200	300	400	500	600	700
DC Gain (V/V)	8.548	9.4	11.1	12.67	14.06	15.31	16.49

Table 3.4.: Absolute values of DC Gain of the OTA

Noise Analysis

Vbias (mV)	150	200	300	400	500	600	700
Input Referred Noise (nV/sqrt(Hz))	46.36	43.73	39.83	37.29	35.57	34.31	33.28

Table 3.5.: Input Referred Noise of the OTA

Transient Analysis - Sine Input

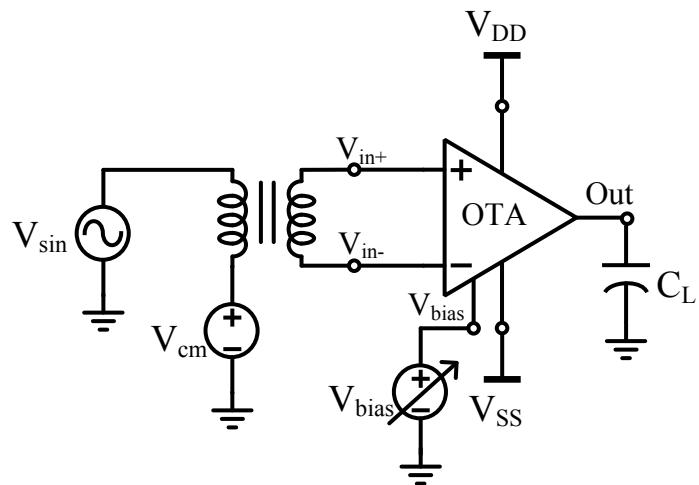


Figure 3.5.: OTA Test setup for Transient Analysis - Sine Wave Input

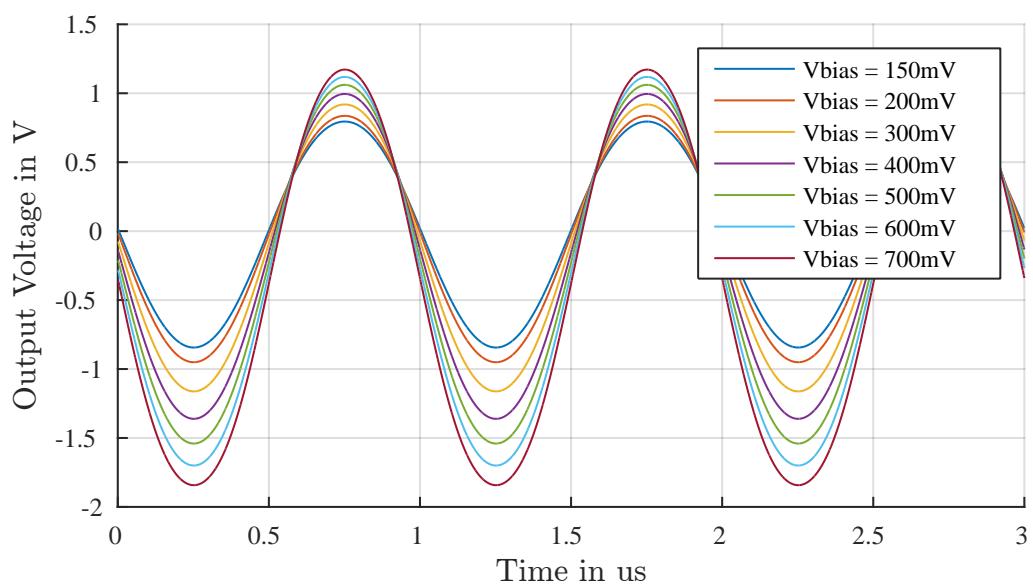


Figure 3.6.: OTA Output Voltage for vs time for different V_{bias}

Vbias (mV)	150	200	300	400	500	600	700
Vout Max (V)	0.7949	0.8362	0.9188	0.995	1.061	1.119	1.172
Vout Min (V)	-0.844	-0.9505	-1.162	-1.361	-1.54	-1.7	-1.842
Vout Swing (V)	1.639	1.787	2.081	2.356	2.601	2.818	3.014
HD2 (dBc)	-44.83	-44.28	-43.86	-44.74	-47.97	-60.86	-48.75
HD3 (dBc)	-52.15	-49.69	-46.13	-43.87	-42.24	-40.78	-39.32

Table 3.6.: Transient Parameters of the OTA

Transient Analysis - Square Input

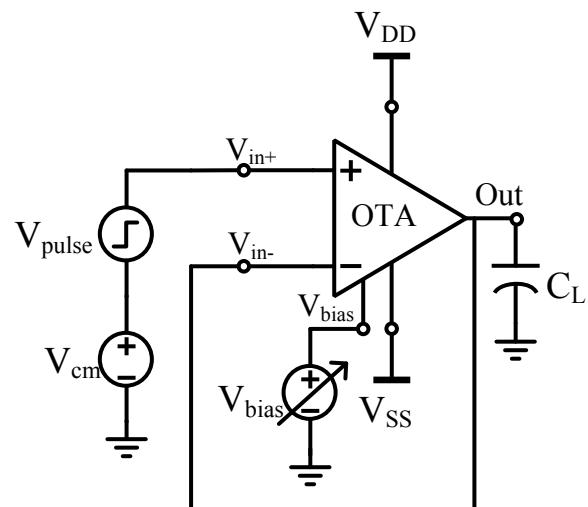


Figure 3.7.: OTA Test setup for Transient Analysis - Square Wave Input

Vbias (mV)	150	200	300	400	500	600	700
Slew Rate Rising Edge (V/us)	386.9	407.8	452.9	501.9	547.6	585.4	609.3
Slew Rate Falling Edge (V/us)	-389	-413.8	-469.4	-523.5	-570.5	-605.7	-626.4

Table 3.7.: Slew Rate of the OTA

AC Analysis - PSRR

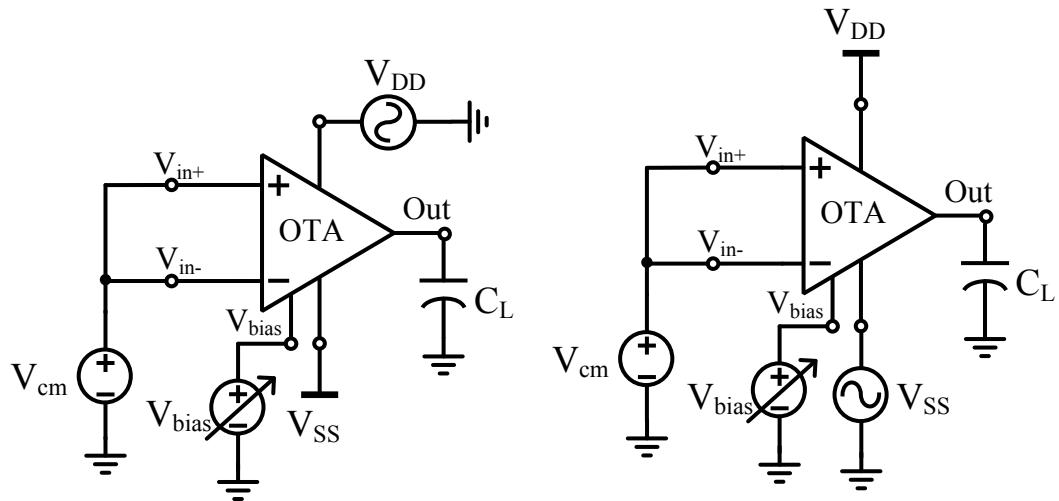


Figure 3.8.: OTA Test setup for calculating PSRR

V_{bias} (mV)	150	200	300	400	500	600	700
PSRR (VDD Supply) (nA/V)	234.6	236.9	241.6	246.7	252.2	258	264.3
PSRR (VSS Supply) (nA/V)	254.5	256.5	260.4	264.2	267.9	271.5	274.9

Table 3.8.: Power Supply Rejection Ratio of the OTA

AC Analysis - Input Impedance

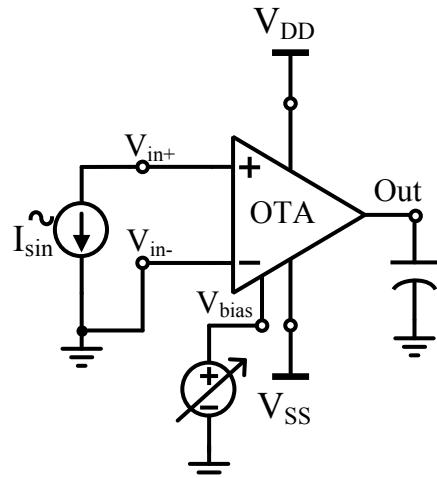


Figure 3.9.: OTA Test setup for calculating Input Impedance

Vbias (mV)	150	200	300	400	500	600	700
Input Impedance (Mega Ohms)	3.38	3.388	3.403	3.419	3.434	3.45	3.467

Table 3.9.: Input Impedance of the OTA

AC Analysis - Output Impedance

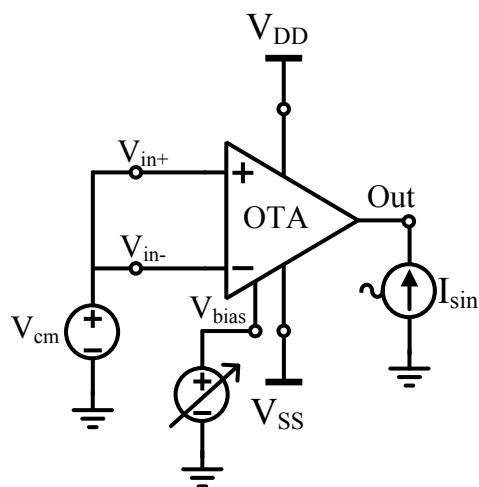


Figure 3.10.: OTA Test setup for calculating Output Impedance

Vbias (mV)	150	200	300	400	500	600	700
Input Impedance (kilo Ohms)	1.262	1.3	1.382	1.473	1.577	1.697	1.837

Table 3.10.: Output Impedance of the OTA

3.3 OP AMP Design

3.3.1 Schematic

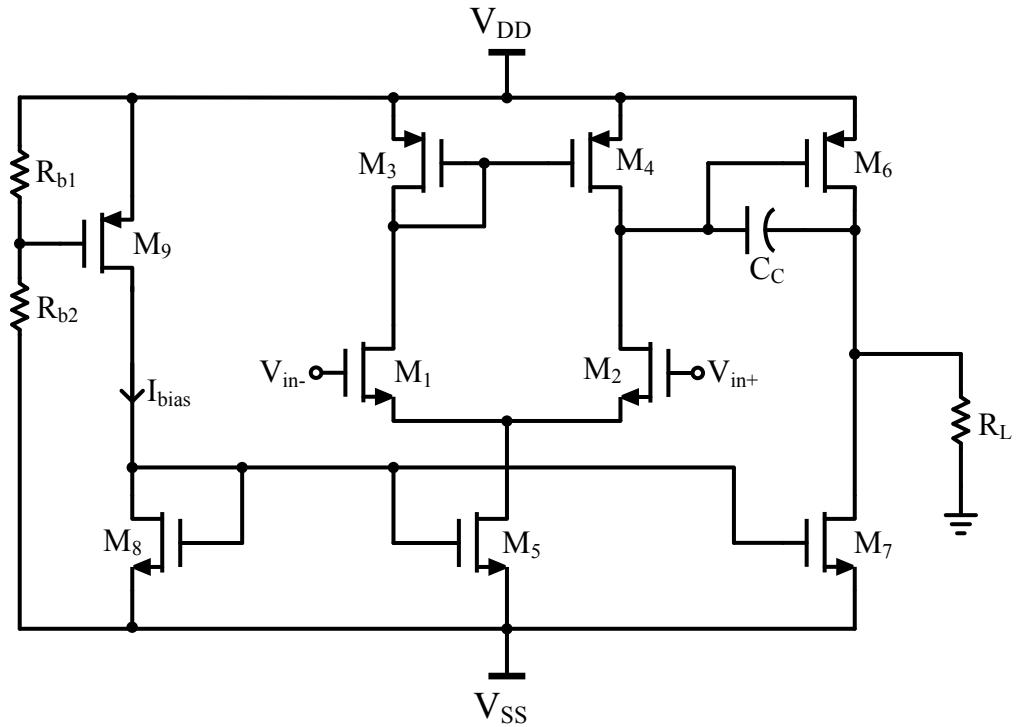


Figure 3.11.: Schematic of the OPAMP Designed

Transistor	Width	Length	Multiplier
M1	5u	500n	2
M2	5u	500n	2
M3	30u	500n	1
M4	30u	500n	1
M5	2u	500n	1
M6	85u	500n	55
M7	50u	500n	48
M8	2u	500n	1
M9	700n	500n	1

Table 3.11.: Dimensions of the Transistors of the designed OPAMP

3.3.2 Test Setup

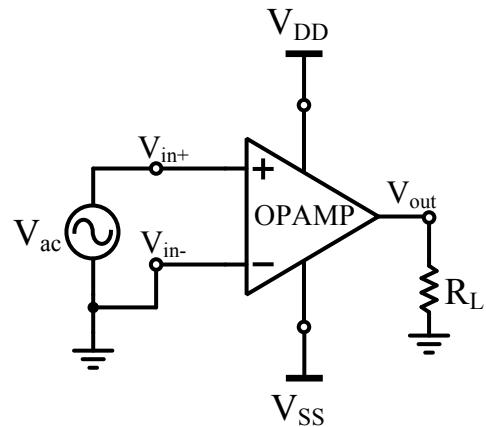


Figure 3.12.: OPAMP Test setup for AC, DC and Noise Analysis

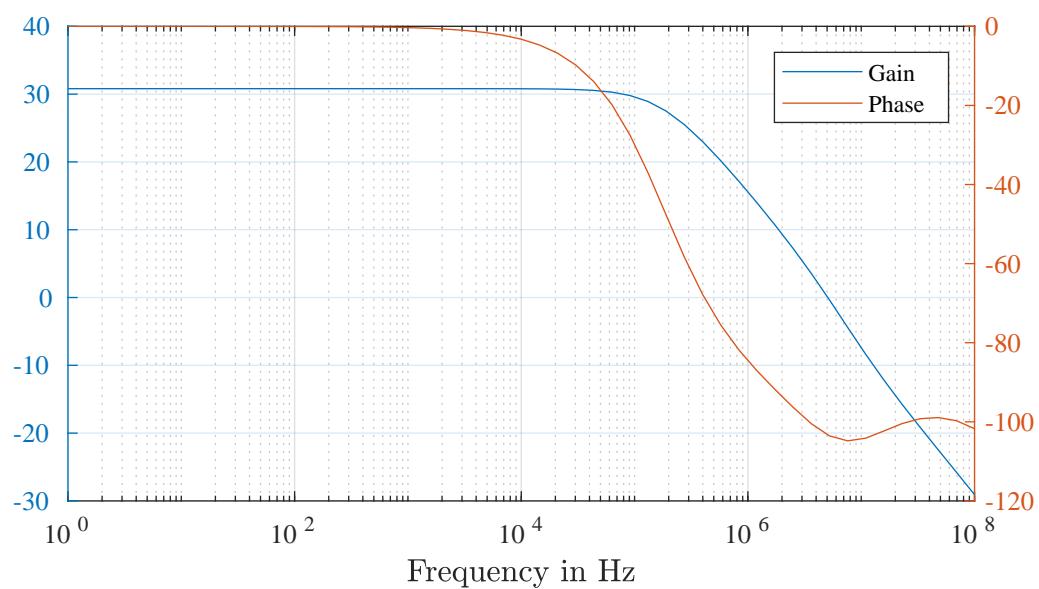


Figure 3.13.: OPAMP Plot of Gain and Phase vs Frequency

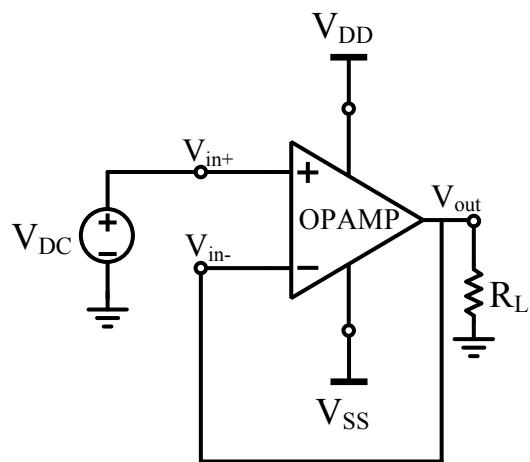


Figure 3.14.: OPAMP Test setup for calculating ICMR

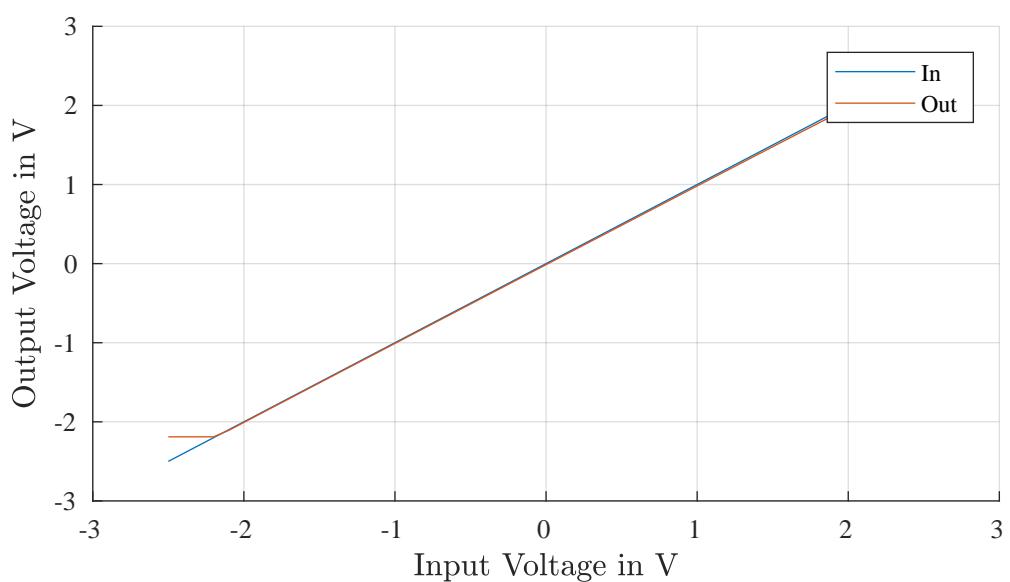


Figure 3.15.: OPAMP Plot of ICMR vs Vin

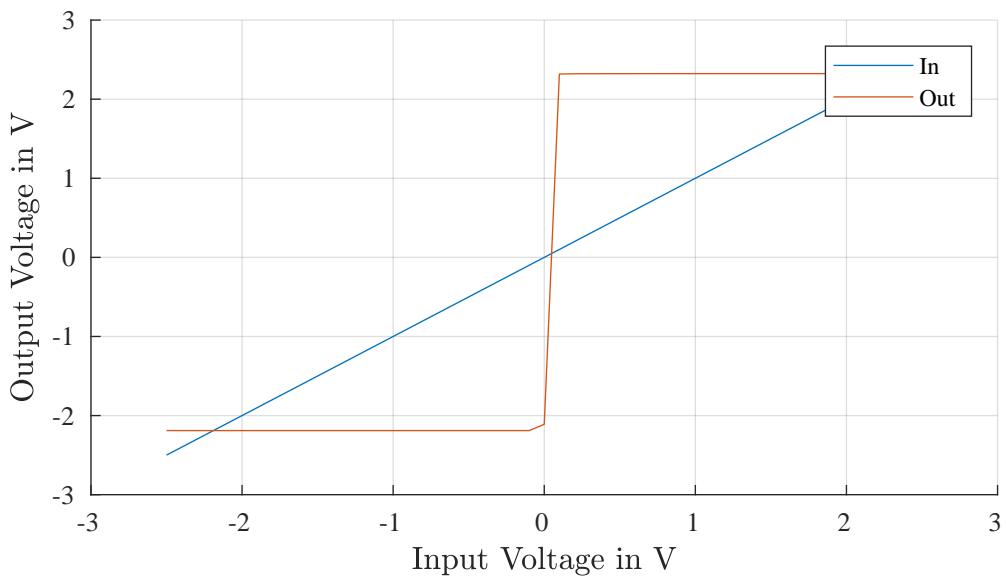


Figure 3.16.: OPAMP Plot of Output Voltage Swing vs V_{in}

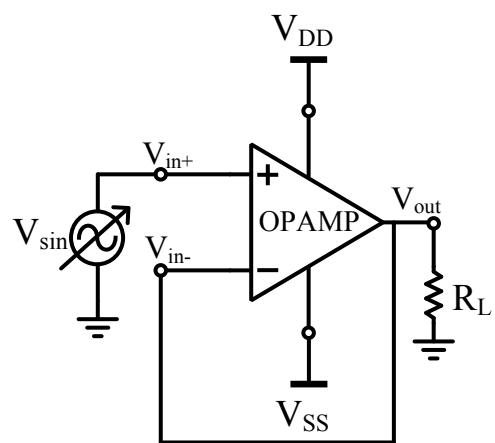


Figure 3.17.: Test setup for Transient Analysis - Sine Wave Input

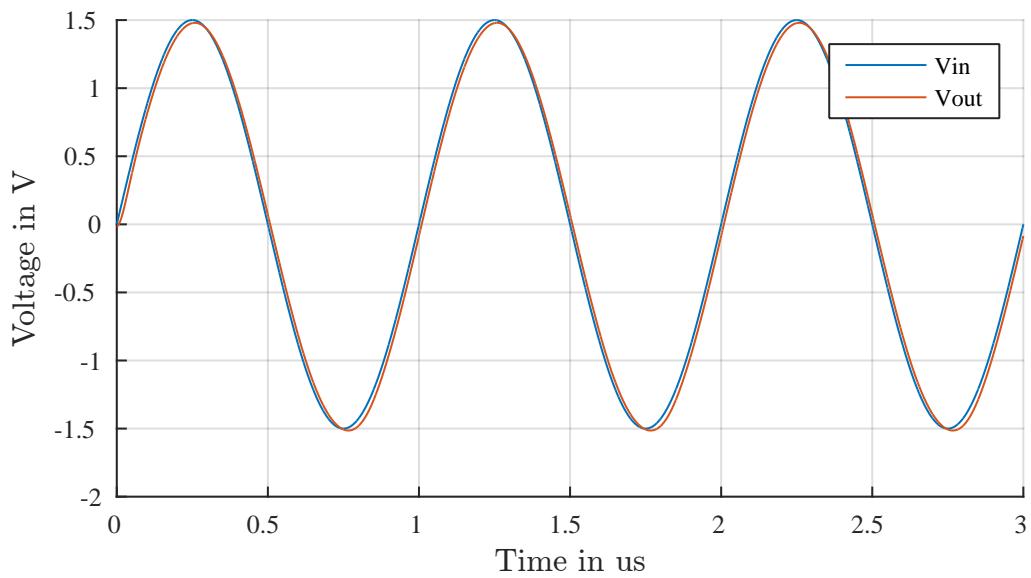


Figure 3.18.: OPAMP Plot of Output Voltage vs time

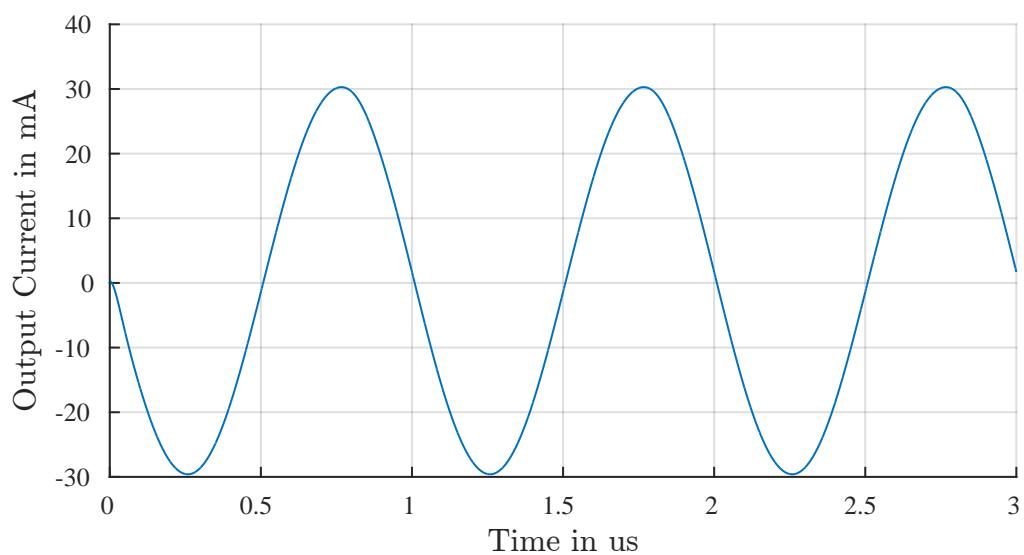


Figure 3.19.: OPAMP Plot of Ourput Current vs time

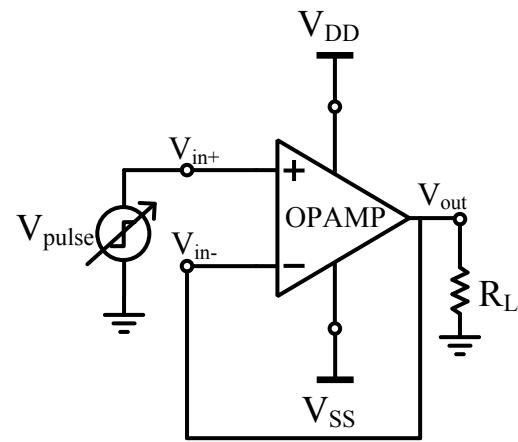


Figure 3.20.: Test setup for Transient Analysis - Square Wave Input

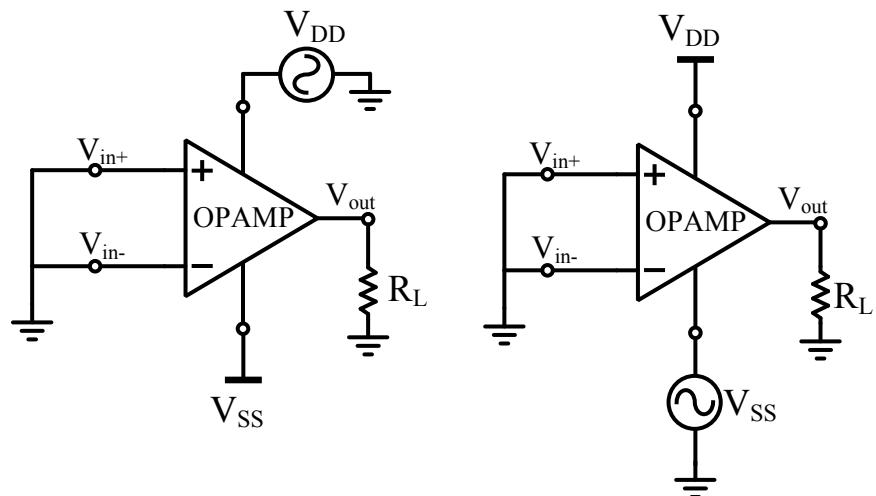


Figure 3.21.: Test setup for calculating PSRR

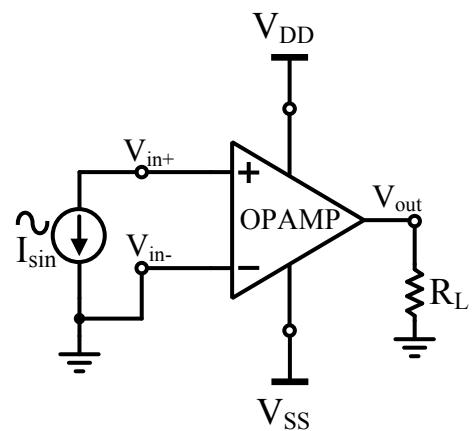


Figure 3.22.: Test setup for calculating Input Impedance

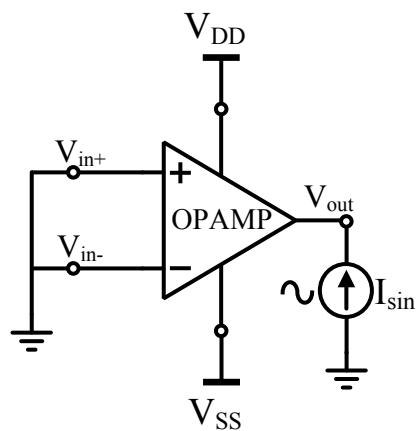


Figure 3.23.: Test setup for calculating Output Impedance

Parameter	Value
Open Loop Gain	30.8 dB
Gain Bandwidth Product	6.2 MHz
Phase Margin	76.79
ICMR (min)	-2.19 V
ICMR (max)	2.089 V
Output Current (max)	-29.6 mA
Output Current (min)	30.28 mA
Output Voltage Swing	-2.19 .. 2.089
Slew Rate	10 V/us
PSRR (VDD)	30.96 uA/V
PSRR (VSS)	138.8 uA/V
Input Impedance	9.04 MOhms
Output Impedance	4.167 Ohms

Table 3.12.: Simulation Results of the OPAMP

3.4 The Complete Design

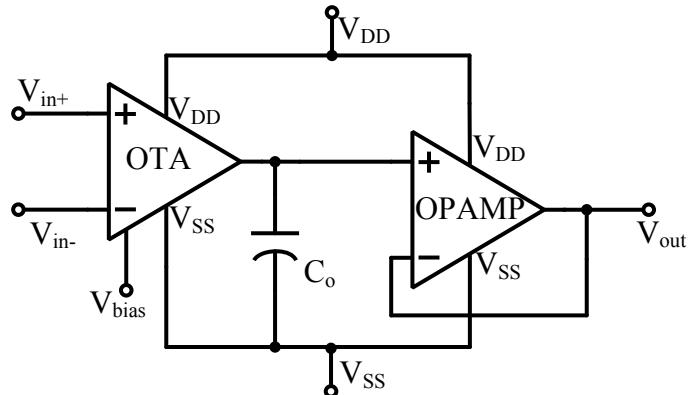


Figure 3.24.: Block Diagram of the Overall System

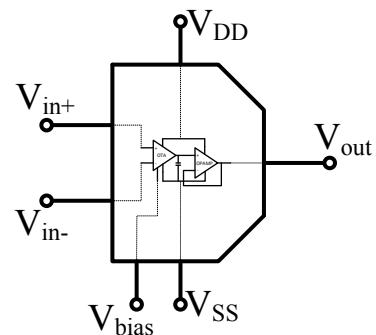


Figure 3.25.: Schematic Symbol for the Overall System

3.4.1 Schematic

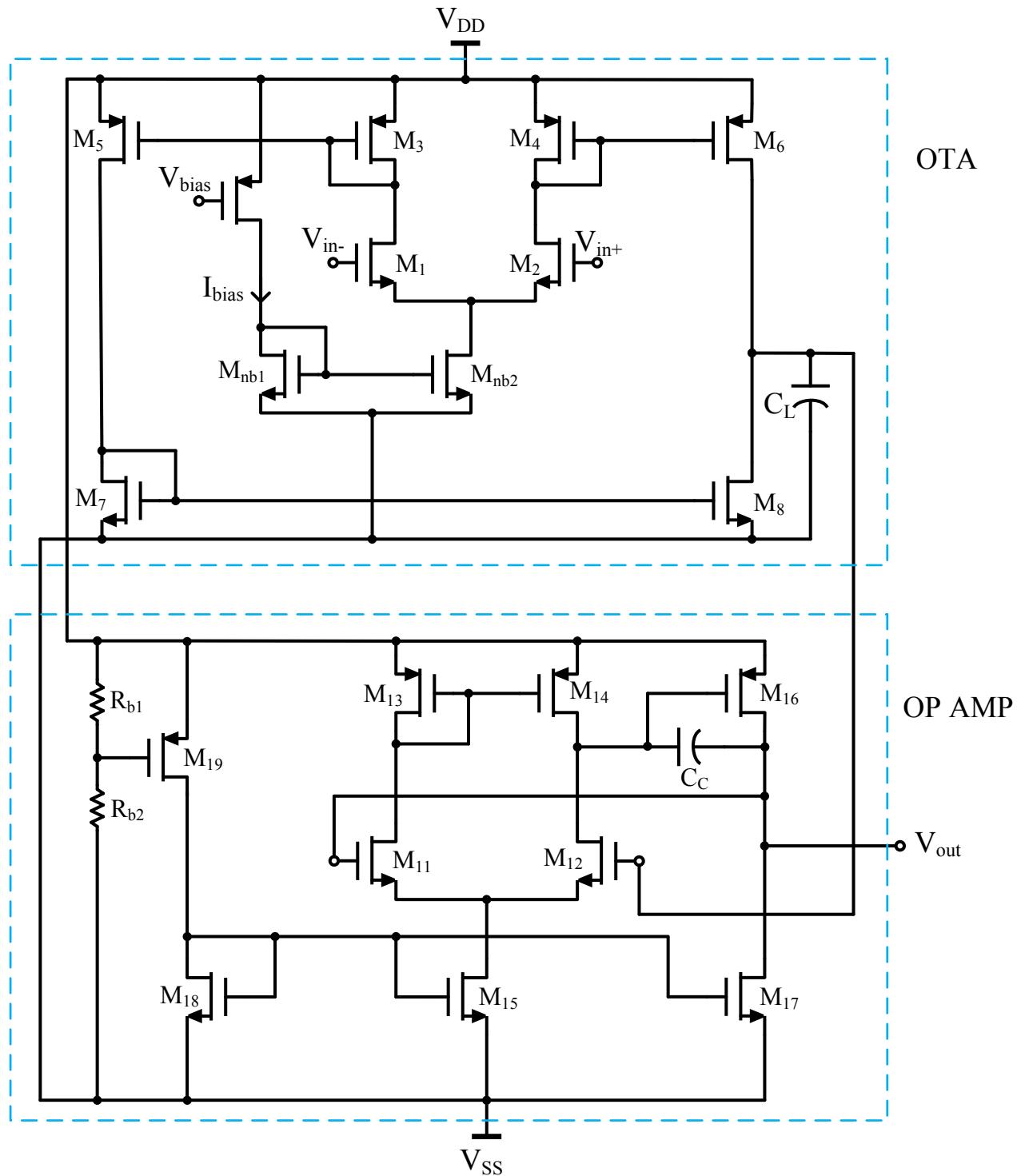


Figure 3.26.: Schematic Diagram for the Overall System



4 Simulation Results

4.1 DC Analysis

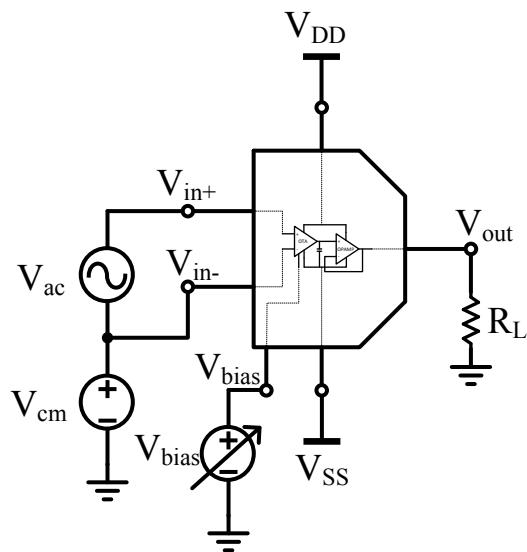


Figure 4.1.: Test setup for DC Analysis

Vbias (mV)	Output DC Bias (mV)
150	180.1
200	148.4
250	115.8
300	82.28
350	47.83
400	12.45
450	-23.86
500	-61.08
550	-99.24
600	-138.3
650	-178.4
700	-219.3

Table 4.1.: DC Bias Point at the output of the circuit

4.2 AC Analysis

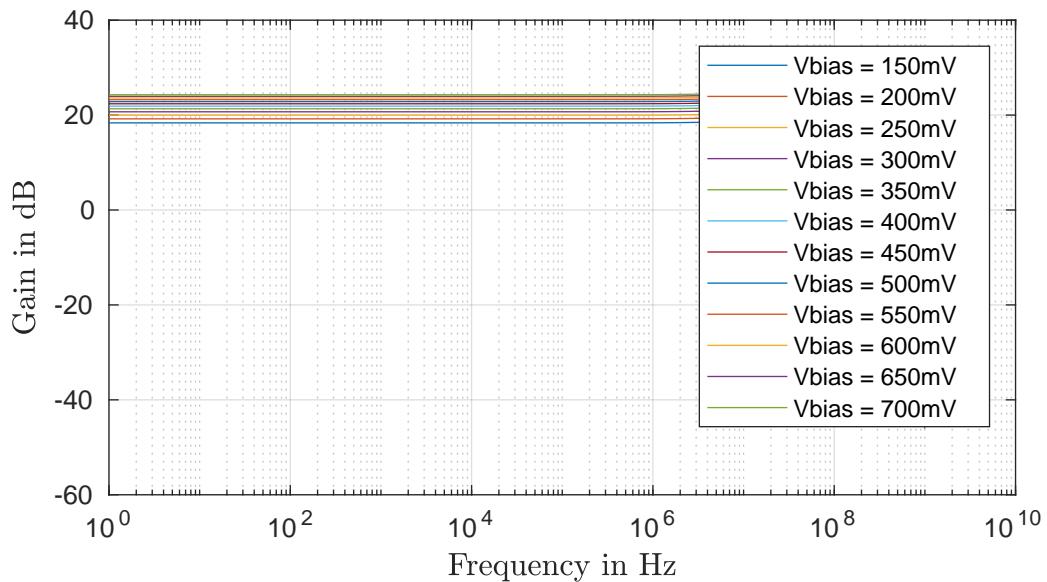


Figure 4.2.: Plot of Gain vs Frequency for different Vbias

Vbias (mV)	DC Gain (dB)	Bandwidth (MHz)	Phase Margin
150	18.5	14.43	55.49
200	19.34	14.38	51.37
250	20.13	14.34	47.76
300	20.83	14.29	45.08
350	21.46	14.24	42.55
400	22.02	14.19	40.19
450	22.52	14.14	38
500	22.97	14.08	35.97
550	23.38	14.01	34.08
600	23.75	13.95	32.31
650	24.1	13.88	30.63
700	24.43	13.8	29.02

Table 4.2.: DC Gain, Bandwidth and Phase Margin of the Overall System

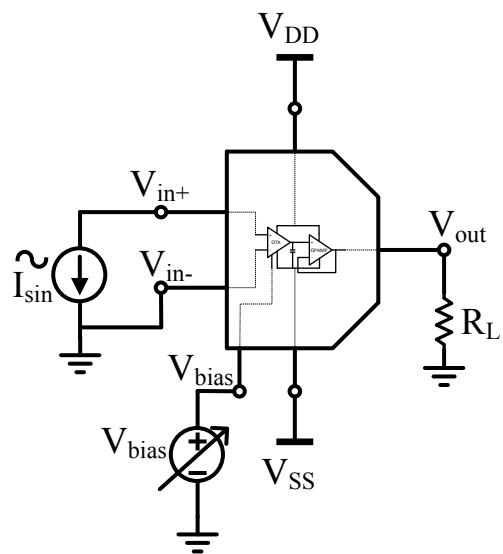


Figure 4.3.: Test setup to measure Input Impedance

Vbias (mV)	Input Impedance (Mega Ohms)
150	3.394
200	3.402
250	3.41
300	3.418
350	3.425
400	3.433
450	3.44
500	3.448
550	3.456
600	3.464
650	3.473
700	3.482

Table 4.3.: Input Impedance of the Overall System

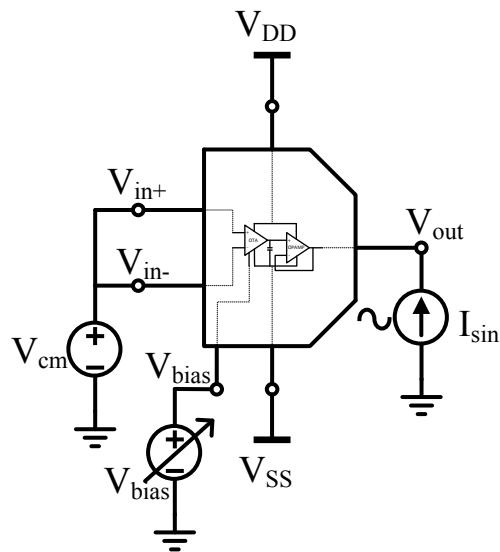


Figure 4.4.: Test setup to measure Output Impedance

Vbias (mV)	Output Impedance (Ohms)
150	0.9415
200	0.9434
250	0.9453
300	0.9474
350	0.9495
400	0.9517
450	0.9541
500	0.9565
550	0.9591
600	0.9618
650	0.9646
700	0.9675

Table 4.4.: Output Impedance of the Overall System

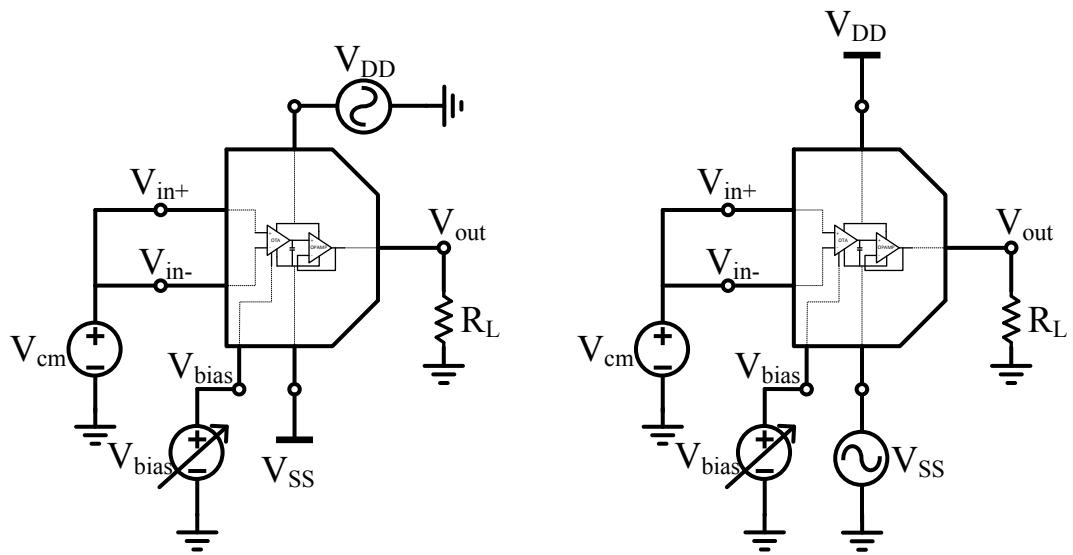


Figure 4.5.: Test setup to measure PSRR

Vbias (mV)	PSRR (VDD)(uA/V)	PSRR (VSS)(uA/V)
150	97.76	93.69
200	89.66	85.77
250	82.86	79.11
300	77.26	73.59
350	72.68	69.04
400	68.93	65.28
450	65.84	62.18
500	63.27	59.53
550	61.1	57.26
600	59.22	55.28
650	57.59	53.52
700	56.13	51.92

Table 4.5.: PSRR of the Overall System

4.3 Transient Analysis

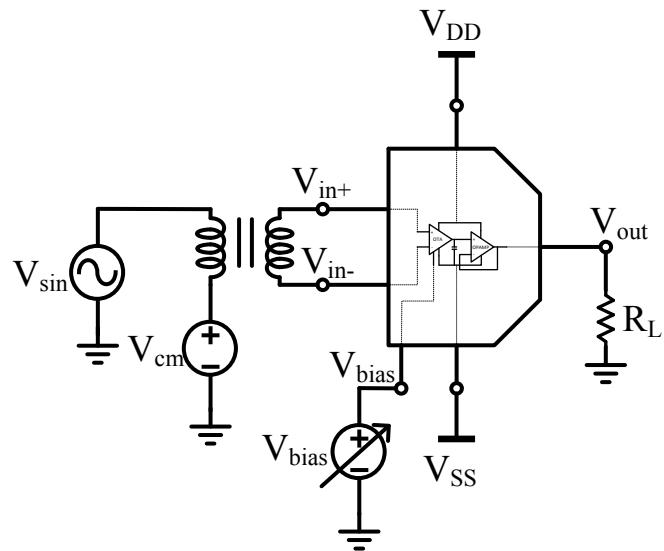


Figure 4.6.: Test setup for Transient Analysis - Sine Wave input

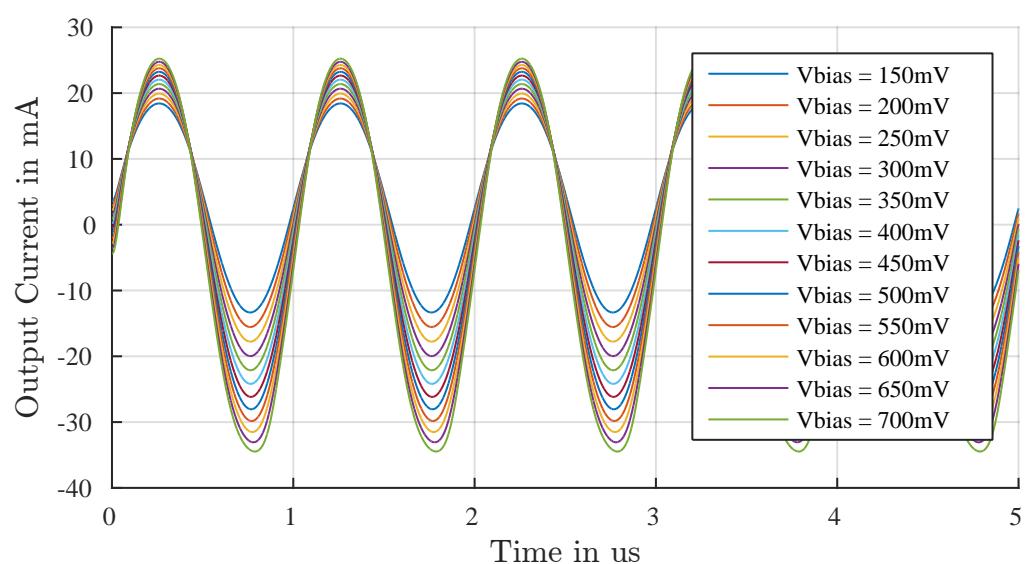


Figure 4.7.: Plot of Output Current vs time for different V_{bias}

Vbias (mV)	Iout Max(mA)	Iout Min(mA)	Iout p2p (mA)	HD2 (dBc)	HD3 (dBc)
150	18.43	-13.34	31.77	-37.14	-48.17
200	19.17	-15.55	34.72	-36.62	-45.67
250	19.93	-17.77	37.7	-35.65	-43.65
300	20.67	-19.97	40.64	-35.15	-42.07
350	21.38	-22.12	43.49	-34.84	-40.83
400	22.04	-24.19	46.23	-34.72	-39.85
450	22.66	-26.17	48.83	-34.8	-39.01
500	23.24	-28.05	51.29	-35.08	-38.24
550	23.77	-29.83	53.6	-35.54	-37.42
600	24.28	-31.51	55.79	-36.13	-36.47
650	24.76	-33.07	57.83	-36.61	-35.24
700	25.24	-34.47	59.71	-36.44	-33.61

Table 4.6.: Transient Parameters of the Overall System

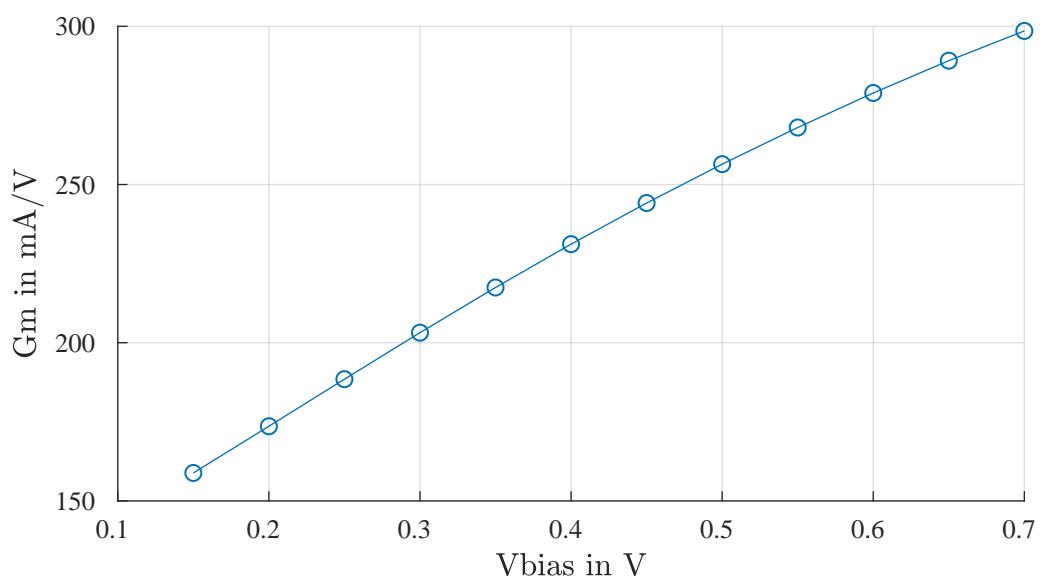


Figure 4.8.: Plot of Gm vs Vbias

Vbias (mV)	Transconductance (mA/V)
150	158.8
200	173.6
250	188.5
300	203.2
350	217.5
400	231.2
450	244.2
500	256.4
550	268
600	278.9
650	289.1
700	298.5

Table 4.7.: Transconductance Gain of the Overall System

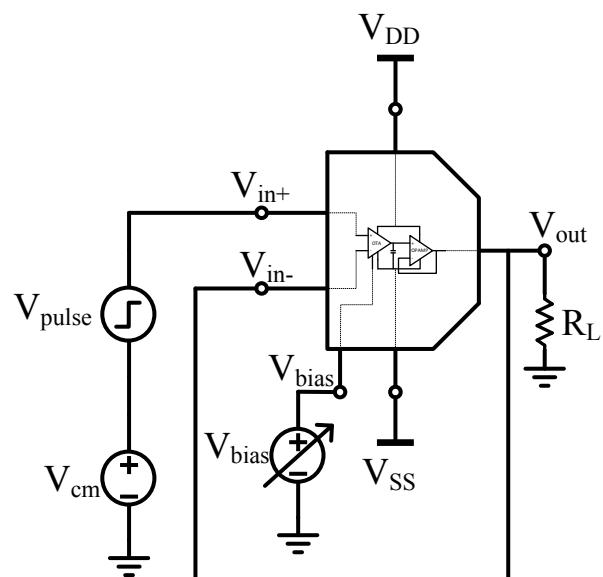


Figure 4.9.: Test setup for Transient Analysis - Square Wave input

Vbias (mV)	Slew Rate (Rising Edge)(V/us)	Slew Rate (Falling Edge)(V/us)
150	6.985	-8.73
200	7.505	-9.779
250	8.042	-10.68
300	8.581	-11.34
350	9.095	-11.66
400	9.561	-11.7
450	9.954	-11.6
500	10.27	-11.45
550	10.49	-11.3
600	10.65	-11.14
650	10.76	-10.99
700	10.82	-10.84

Table 4.8.: Slew Rate of the Overall System

4.4 Noise Analysis

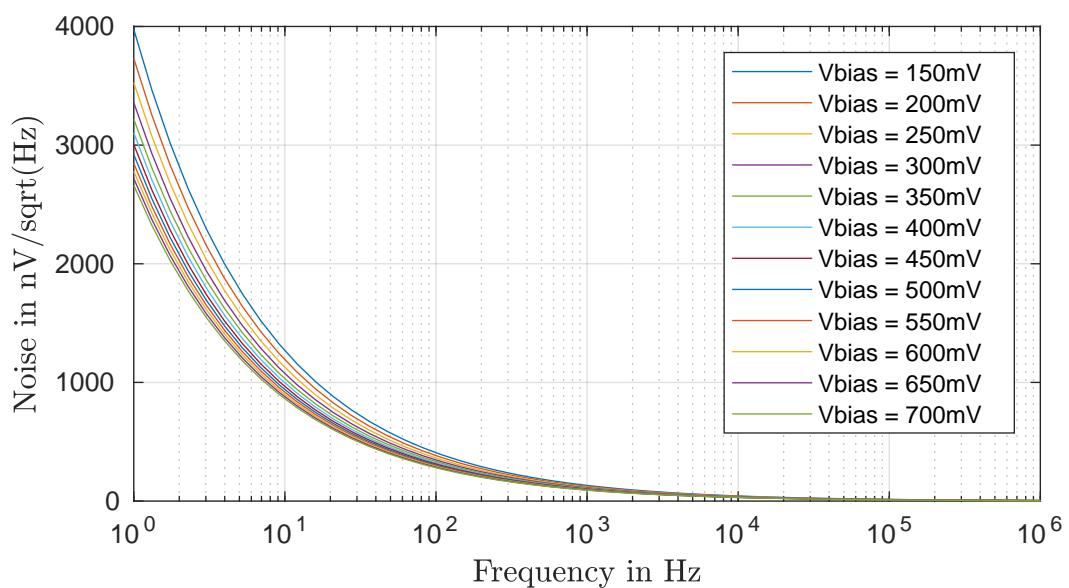


Figure 4.10.: Plot of Input Referred Noise vs Frequency for different Vbias

4.5 Programmable Load

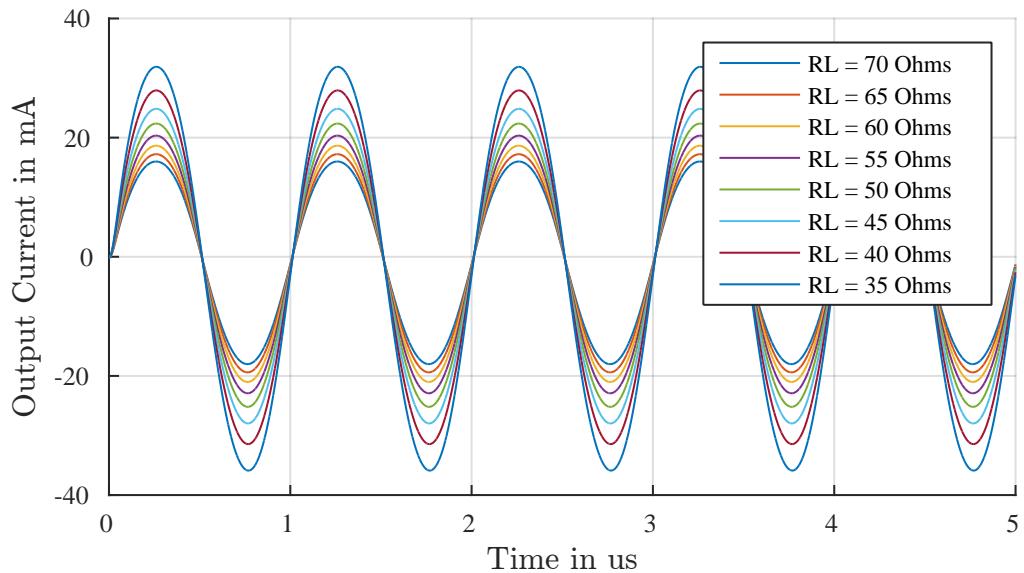


Figure 4.11.: Plot of Output Current vs Time for different RL

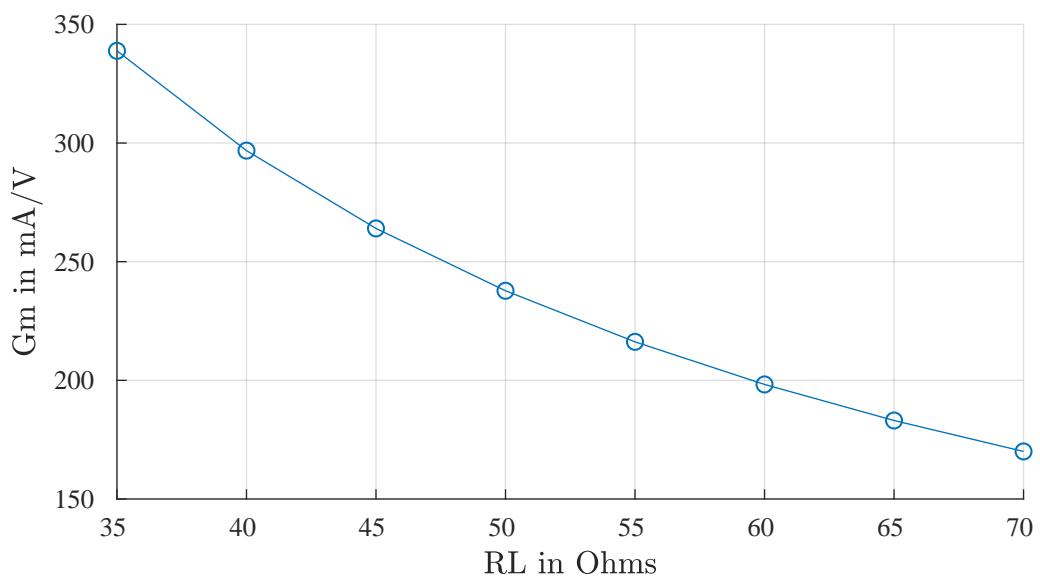


Figure 4.12.: Plot of Output Current vs time for different RL

4.6 Corner Simulation

4.6.1 Process Variation

4.6.2 Process and Supply Variation

4.6.3 Process, Voltage and Temperature (PVT) variation

4.6.4 Summary of PVT Corner Analysis



5 Conclusion

5.1 Summary of Results

5.2 Outlook



A Appendix

