

Design and Implementation of a Radiation Hardened High Output Current Transconductance Amplifier

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Abstract

This thesis details the design and implementation of a radiation hardened high output current transconductance amplifier which can provide currents in the range of $\pm 15\text{mA}$ to $\pm 30\text{mA}$ across a 50Ω load resistor for a linear input voltage range of $\pm 100\text{mV}$. An external voltage that controls the bias current is the programmable parameter of the system and it ranges from 150mV to 700mV . The design and implementation was carried in Cadence Virtuoso Design Environment using XT018 SOI technology from XFAB, to make the design radiation hard. The system consists of two stages - the conventional current mirror based Operational Transconductance Amplifier, which is used as a programmable stage followed by a two-stage Miller compensated Operational Amplifier, which is used as a voltage buffer that generates high currents. Two different design approaches are presented. The first of which is - with the bias current of the first stage being the programmable parameter. The bias current is controlled by a PMOS transistor whose gate voltage is an input of the system. Another design approach is presented with the load being a programmable parameter. For this case, the bias voltage is kept at a constant value of 450mV and the load resistor is varied from 35Ω to 70Ω . The operating bandwidth of the system is 13MHz . The whole system is intended to be used as part of a Closed-loop Novel DC Current Transformer circuit by providing a feedback current that cancels the change in magnetic field of the ion-beam. As a consequence, the linearity and the sensitivity of the current transformer is improved. The system is simulated at all control settings and across PVT corners to verify its robustness. Simulation results based on schematic level design are presented.



Zusammenfassung

In dieser Arbeit wird der Entwurf und die Implementierung eines strahlungsgehärteten Transkonduktanzverstärkers mit hohem Ausgangsstrom beschrieben, der Schiene-zu-Schiene-Ströme zwischen 15 mA und 30 mA über einen 50Ω Lastwiderstand für einen linearen Eingangsspannungsbereich von 100 mV liefern kann. Eine externe Spannung, die den Vorstrom steuert, ist der programmierbare Parameter des Systems und reicht von 150 mV bis 700 mV. Das Design und die Implementation wurden in Cadence Virtuoso Design Environment unter Verwendung der XT018 SOI-Technologie von XFAB durchgeführt, um die Designstrahlung zu erschweren. Das System besteht aus zwei Stufen - dem konventionellen, auf einem Stromspiegel basierenden, betrieblichen Transkonduktanzverstärker, der als programmierbare Stufe verwendet wird, gefolgt von einem zweistufigen Miller-kompensierten Operationsverstärker, der als Spannungspuffer verwendet wird, der hohe Ströme erzeugt. Es werden zwei unterschiedliche Designansätze vorgestellt. Die erste davon ist - wobei der Vorspannungsstrom der ersten Stufe der programmierbare Parameter ist. Der Vorspannungsstrom wird von einem PMOS-Transistor gesteuert, dessen Gatespannung ein Eingang des Systems ist. Es werden zwei unterschiedliche Designansätze vorgestellt, wobei die Lastwiderstand ein programmierbarer Parameter ist. In diesem Fall wird die Vorspannung auf einem konstanten Wert von 450 mV gehalten und die Last variiert von 35Ω bis 70Ω . Die Betriebsbandbreite des Systems beträgt 13 MHz. Das gesamte System ist als Teil eines geschlossenen DC-Stromwandlerkreises mit geschlossenem Regelkreis vorgesehen, indem ein Rückkopplungsstrom bereitgestellt wird, der die Änderung des Magnetfelds des Ionenstrahls aufhebt. Infolgedessen werden die Linearität und die Empfindlichkeit des Stromwandlers verbessert. Das System wird bei allen Steuereinstellungen und an allen PVT-Ecken simuliert, um seine Robustheit zu überprüfen. Dargestellt werden Simulationsergebnisse basierend auf dem Design der Schmetikebene.



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Contents

Declaration of Authorship	i
Abstract	i
Zusammenfassung	iii
Acknowledgments	v
List of Figures	xi
List of Tables	xvii
1 Introduction	1
1.1 Motivation	2
1.2 Specification	3
1.3 Technology	4
2 Theory	5
2.1 The Operational Transconductance Amplifier	5
2.1.1 Conventional Current Mirror OTA	5
2.1.2 Other Topologies	7
2.2 The Opeartional Amplifier	8
2.2.1 Miller Compensation OP AMP	8
2.3 The Gm/Id Methodology	10
3 Operational Transconductance Amplifier	17
3.1 Design and Implementaion	17
3.1.1 Schematic	23
3.2 Test Setup	25
3.2.1 DC Analysis	25
3.2.2 AC Analysis	25
3.2.3 Noise Analysis	29
3.2.4 Transient Analysis	30
3.3 Summary	31
4 Operational Amplifier	33
4.1 Design and Implementation	33
4.1.1 Schematic	34
4.2 Test Setup	36
4.2.1 DC Analysis	37
4.2.2 AC Analysis	37

4.2.3	Transient Analysis	39
4.3	Summary	40
5	Overall System	41
5.1	Schematic	41
5.2	Test Setup	43
5.2.1	DC Analysis	44
5.2.2	AC Analysis	44
5.2.3	Transient Analysis	47
5.2.4	Noise Analysis	50
5.3	Programmable Load	51
5.4	Summary of Results	54
6	Corner Simulations	55
6.1	Process Variation	55
6.2	Process and Supply Variation	60
6.3	Process, Voltage and Temperature (PVT) variation	65
6.4	Summary of PVT Corner Analysis	79
7	Conclusion	81
7.1	Summary of Results	82
7.2	Outlook	82
A	Appendix	83
A.1	Corner Simulation	83
A.2	Conventional OTA with PMOS Input	115
A.3	3-stage Topology	115
8	Bibliography	117

List of Figures

1.1	Closed Loop Novel-DC Current Transformer [1]	2
2.1	Symbol of an OTA	5
2.2	Schematic of a Conventional Current Mirror OTA	6
2.3	Symbol of an OP AMP	8
2.4	Schematic of a Two-stage Miller Compensation OP AMP	9
2.5	Square Law Methodology	10
2.6	Gm/ID Methodology	11
2.7	Setup for simulating GmID parameters	11
2.8	G_m/I_D vs V_{ov}	12
2.9	f_T vs G_m/I_D	12
2.10	$f_T G_m/I_D$ vs G_m/I_D	13
2.11	G_m/G_{ds} vs G_m/I_D	14
2.12	I_D vs V_{ov}	14
3.1	Overview of Commercial OTA OPA860	17
3.2	Schematic of a Self-Cascode MOSFET	18
3.3	Block Diagram of Feed Forward Miller Compensation OTA	19
3.4	Block Diagram of Feed Forward OTA without Miller Capacitor	20
3.5	Super Class-AB OTA with a Cascode Voltage Flipped Follower	21
3.6	Schematic of the OTA Designed	24
3.7	Test bench setup for OTA	26
3.8	OTA Plot of Gain vs Frequency for different Vbias	27
3.9	OTA Plot of Gain vs Vbias	28

3.10	OTA Output Voltage for vs time for different Vbias	30
4.1	Behavior Modelling of Ideal OP AMP	33
4.2	Schematic of the OPAMP Designed	35
4.3	Test bench setup for OP AMP	36
4.4	OPAMP Plot of Gain and Phase vs Frequency	38
4.5	OPAMP Plot of Ourput Current vs time	39
5.1	Block Diagram of the Overall System	41
5.2	Schematic Diagram for the Overall System	42
5.3	Test setup for DC Analysis	43
5.4	Schematic Symbol for the Overall System	44
5.5	Plot of Gain vs Frequency for different V_{bias}	45
5.6	Plot of Output Current vs time for different V_{bias}	48
5.7	Plot of Gm vs V_{bias}	49
5.8	Plot of Input Referred Noise vs Frequency for different V_{bias}	50
5.9	Plot of Output Current vs Time for different RL	52
5.10	Plot of Transconductance vs RL	53
6.1	Histogram of System Gain due to Process Variation at $V_{bias}=150\text{mV}$	56
6.2	Histogram of System Bandwidth due to Process Variation at $V_{bias}=150\text{mV}$	56
6.3	Histogram of Maximum Output Current due to Process Variation at $V_{bias}=150\text{mV}$	57
6.4	Histogram of Minimum Output Current due to Process Variation at $V_{bias}=150\text{mV}$	57
6.5	Histogram of System Gain due to Process Variation at $V_{bias}=700\text{mV}$	58
6.6	Histogram of System Bandwidth due to Process Variation at $V_{bias}=700\text{mV}$	58
6.7	Histogram of Maximum Output Current due to Process Variation at $V_{bias}=700\text{mV}$	59
6.8	Histogram of Minimum Output Current due to Process Variation at $V_{bias}=700\text{mV}$	59
6.9	Histogram of System Gain due to Process and Supply Variation at $V_{bias}=150\text{mV}$	60

6.10 Histogram of System Bandwidth due to Process and Supply Variation at $V_{bias}=150\text{mV}$	61
6.11 Histogram of Maximum Output Current due to Process and Supply Variation at $V_{bias}=150\text{mV}$	61
6.12 Histogram of Minimum Output Current due to Process and Supply Variation at $V_{bias}=150\text{mV}$	62
6.13 Histogram of Transconductance due to Process and Supply Variation at $V_{bias}=150\text{mV}$	62
6.14 Histogram of System Gain due to Process and Supply Variation at $V_{bias}=700\text{mV}$	63
6.15 Histogram of System Bandwidth due to Process and Supply Variation at $V_{bias}=700\text{mV}$	63
6.16 Histogram of Maximum Output Current due to Process and Supply Variation at $V_{bias}=700\text{mV}$	64
6.17 Histogram of Minimum Output Current due to Process and Supply Variation at $V_{bias}=700\text{mV}$	64
6.18 Histogram of Transconductance due to Process and Supply Variation at $V_{bias}=700\text{mV}$	65
6.19 Histogram of Input Referred Noise due to Process and Supply Variation at $V_{bias}=400\text{mV}$	65
6.20 Histogram of System Gain due to PVT Variation at $V_{bias}=150\text{mV}$	66
6.21 Histogram of System Bandwidth due to PVT Variation at $V_{bias}=150\text{mV}$	67
6.22 Histogram of Maximum Output Current due to PVT Variation at $V_{bias}=150\text{mV}$	67
6.23 Histogram of Minimum Output Current due to PVT Variation at $V_{bias}=150\text{mV}$	68
6.24 Histogram of Transconductance due to PVT Variation at $V_{bias}=150\text{mV}$	68
6.25 Histogram of HD2 due to PVT Variation at $V_{bias}=150\text{mV}$	69
6.26 Histogram of HD3 due to PVT at $V_{bias}=150\text{mV}$	69
6.27 Histogram of Input Referred Noise due to PVT Variation at $V_{bias}=150\text{mV}$	70
6.28 Histogram of Input Impedance due to PVT Variation at $V_{bias}=150\text{mV}$	70
6.29 Histogram of Output Impedance due to PVT Variation at $V_{bias}=150\text{mV}$	71
6.30 Histogram of PSRR(V_{DD}) due to PVT Variation at $V_{bias}=150\text{mV}$	71
6.31 Histogram of PSRR(V_{SS}) due to PVT Variation at $V_{bias}=150\text{mV}$	72
6.32 Histogram of System Gain due to PVT Variation at $V_{bias}=700\text{mV}$	73
6.33 Histogram of System Bandwidth due to PVT Variation at $V_{bias}=700\text{mV}$	73
6.34 Histogram of Maximum Output Current due to PVT Variation at $V_{bias}=700\text{mV}$	74
6.35 Histogram of Minimum Output Current due to PVT Variation at $V_{bias}=700\text{mV}$	74

6.36 Histogram of Transconductance due to PVT Variation at $V_{bias}=700\text{mV}$	75
6.37 Histogram of HD2 due to PVT Variation at $V_{bias}=700\text{mV}$	75
6.38 Histogram of HD3 due to PVT Variation at $V_{bias}=700\text{mV}$	76
6.39 Histogram of Input Referred Noise due to PVT Variation at $V_{bias}=400\text{mV}$	76
6.40 Histogram of Input Impedance due to PVT Variation at $V_{bias}=700\text{mV}$	77
6.41 Histogram of Output Impedance due to Process and Supply Variation at $V_{bias}=700\text{mV}$	77
6.42 Histogram of PSRR(V_{DD}) due to PVT Variation at $V_{bias}=700\text{mV}$	78
6.43 Histogram of PSRR(V_{SS}) due to PVT Variation at $V_{bias}=700\text{mV}$	78
A.1 Histogram of HD2 due to Process Variation at $V_{bias}=150\text{mV}$	83
A.2 Histogram of HD3 due to Process Variation at $V_{bias}=150\text{mV}$	84
A.3 Histogram of Input Referred Noise due to Process Variation at $V_{bias}=150\text{mV}$	84
A.4 Histogram of Input Impedance due to Process Variation at $V_{bias}=150\text{mV}$	85
A.5 Histogram of Output Impedance due to Process Variation at $V_{bias}=150\text{mV}$	85
A.6 Histogram of PSRR(V_{DD}) due to Process Variation at $V_{bias}=150\text{mV}$	86
A.7 Histogram of PSRR(V_{SS}) due to Process Variation at $V_{bias}=150\text{mV}$	86
A.8 Histogram of System Gain due to Process Variation at $V_{bias}=400\text{mV}$	87
A.9 Histogram of System Bandwidth due to Process Variation at $V_{bias}=400\text{mV}$	87
A.10 Histogram of Maximum Output Current due to Process Variation at $V_{bias}=400\text{mV}$	88
A.11 Histogram of Minimum Output Current due to Process Variation at $V_{bias}=400\text{mV}$	88
A.12 Histogram of Transconductance due to Process Variation at $V_{bias}=400\text{mV}$	89
A.13 Histogram of HD2 due to Process Variation at $V_{bias}=400\text{mV}$	89
A.14 Histogram of HD3 due to Process Variation at $V_{bias}=400\text{mV}$	90
A.15 Histogram of Input Referred Noise due to Process Variation at $V_{bias}=400\text{mV}$	90
A.16 Histogram of Input Impedance due to Process Variation at $V_{bias}=400\text{mV}$	91
A.17 Histogram of Output Impedance due to Process Variation at $V_{bias}=400\text{mV}$	91

A.18 Histogram of PSRR(V_{DD}) due to Process Variation at $V_{bias}=400\text{mV}$	92
A.19 Histogram of PSRR(V_{SS}) due to Process Variation at $V_{bias}=400\text{mV}$	92
A.20 Histogram of HD2 due to Process Variation at $V_{bias}=700\text{mV}$	93
A.21 Histogram of HD3 due to Process Variation at $V_{bias}=700\text{mV}$	93
A.22 Histogram of Input Referred Noise due to Process Variation at $V_{bias}=400\text{mV}$	94
A.23 Histogram of Input Impedance due to Process Variation at $V_{bias}=700\text{mV}$	94
A.24 Histogram of Output Impedance due to Process Variation at $V_{bias}=700\text{mV}$	95
A.25 Histogram of PSRR(V_{DD}) due to Process Variation at $V_{bias}=700\text{mV}$	95
A.26 Histogram of PSRR(V_{SS}) due to Process Variation at $V_{bias}=700\text{mV}$	96
A.27 Histogram of HD2 due to Process and Supply Variation at $V_{bias}=150\text{mV}$	96
A.28 Histogram of HD3 due to Process and Supply Variation at $V_{bias}=150\text{mV}$	97
A.29 Histogram of Input Referred Noise due to Process and Supply Variation at $V_{bias}=150\text{mV}$. . .	97
A.30 Histogram of Input Impedance due to Process and Supply Variation at $V_{bias}=150\text{mV}$	98
A.31 Histogram of Output Impedance due to Process and Supply Variation at $V_{bias}=150\text{mV}$. . .	98
A.32 Histogram of PSRR(V_{DD}) due to Process and Supply Variation at $V_{bias}=150\text{mV}$	99
A.33 Histogram of PSRR(V_{SS}) due to Process and Supply Variation at $V_{bias}=150\text{mV}$	99
A.34 Histogram of System Gain due to Process and Supply Variation at $V_{bias}=400\text{mV}$	100
A.35 Histogram of System Bandwidth due to Process and Supply Variation at $V_{bias}=400\text{mV}$. . .	100
A.36 Histogram of Maximum Output Current due to Process and Supply Variation at $V_{bias}=400\text{mV}$	101
A.37 Histogram of Minimum Output Current due to Process and Supply Variation at $V_{bias}=400\text{mV}$	101
A.38 Histogram of Transconductance due to Process and Supply Variation at $V_{bias}=400\text{mV}$. . .	102
A.39 Histogram of HD2 due to Process and Supply Variation at $V_{bias}=400\text{mV}$	102
A.40 Histogram of HD3 due to Process and Supply Variation at $V_{bias}=400\text{mV}$	103
A.41 Histogram of Input Referred Noise due to Process and Supply Variation at $V_{bias}=400\text{mV}$. . .	103
A.42 Histogram of Input Impedance due to Process and Supply Variation at $V_{bias}=400\text{mV}$	104
A.43 Histogram of Output Impedance due to Process and Supply Variation at $V_{bias}=400\text{mV}$. . .	104

A.44 Histogram of PSRR(V_{DD}) due to Process and Supply Variation at $V_{bias}=400\text{mV}$	105
A.45 Histogram of PSRR(V_{SS}) due to Process and Supply Variation at $V_{bias}=400\text{mV}$	105
A.46 Histogram of HD2 due to Process and Supply Variation at $V_{bias}=700\text{mV}$	106
A.47 Histogram of HD3 due to Process and Supply Variation at $V_{bias}=700\text{mV}$	106
A.48 Histogram of Input Impedance due to Process and Supply Variation at $V_{bias}=700\text{mV}$	107
A.49 Histogram of Output Impedance due to Process and Supply Variation at $V_{bias}=700\text{mV}$	107
A.50 Histogram of PSRR(V_{DD}) due to Process and Supply Variation at $V_{bias}=700\text{mV}$	108
A.51 Histogram of PSRR(V_{SS}) due to Process and Supply Variation at $V_{bias}=700\text{mV}$	108
A.52 Histogram of System Gain due to PVT Variation at $V_{bias}=400\text{mV}$	109
A.53 Histogram of System Bandwidth due to PVT Variation at $V_{bias}=400\text{mV}$	109
A.54 Histogram of Maximum Output Current due to PVT Variation at $V_{bias}=400\text{mV}$	110
A.55 Histogram of Minimum Output Current due to PVT Variation at $V_{bias}=400\text{mV}$	110
A.56 Histogram of Transconductance due to PVT Variation at $V_{bias}=400\text{mV}$	111
A.57 Histogram of HD2 due to PVT Variation at $V_{bias}=400\text{mV}$	111
A.58 Histogram of HD3 due to PVT Variation at $V_{bias}=400\text{mV}$	112
A.59 Histogram of Input Referred Noise due to PVT Variation at $V_{bias}=400\text{mV}$	112
A.60 Histogram of Input Impedance due to PVT Variation at $V_{bias}=400\text{mV}$	113
A.61 Histogram of Output Impedance due to PVT Variation at $V_{bias}=400\text{mV}$	113
A.62 Histogram of PSRR(V_{DD}) due to PVT Variation at $V_{bias}=400\text{mV}$	114
A.63 Histogram of PSRR(V_{SS}) due to PVT Variation at $V_{bias}=400\text{mV}$	114
A.64 Conventional Current Mirror OTA with PMOS Input	115
A.65 3 stage design with an Emitter Follower	115

List of Tables

1.1	Specifications of the Design	3
1.2	Components used as part of XT018 technology	4
3.1	Comparison of OTA Topologies	23
3.2	Dimensions of the Transistors of the designed OTA	24
3.3	Output DC Bias Point of the OTA	25
3.4	Open Loop Gain, Phase Margin and Bandwidth of the OTA	27
3.5	Absolute values of DC Gain of the OTA	28
3.6	Power Supply Rejection Ratio of the OTA	28
3.7	Input Impedance of the OTA	29
3.8	Output Impedance of the OTA	29
3.9	Input Referred Noise of the OTA	30
3.10	Transient Parameters of the OTA	31
3.11	Slew Rate of the OTA	31
3.12	Simulation Results of the OTA	31
4.1	Specifications of the OPAMP to be designed	34
4.2	Dimensions of the Transistors of the designed OPAMP	35
4.3	DC Analysis	37
4.4	Gain and Unity Bandwidth of the OP AMP	38
4.5	PSRR of the OP AMP	38
4.6	Simlation Results of the OPAMP	40
5.1	DC Bias Point at the output of the circuit	44

5.2	DC Gain, Bandwidth and Phase Margin of the Overall System	45
5.3	Input Impedance of the Overall System	46
5.4	Output Impedance of the Overall System	47
5.5	PSRR of the Overall System	47
5.6	Transient Parameters of the Overall System	48
5.7	Transconductance Gain of the Overall System	49
5.8	Slew Rate of the Overall System	50
5.9	Input Referred Noise of the Overall System	51
5.10	AC Parameters of the Overall System for a programmable load - 1	51
5.11	AC Parameters of the Overall System for a programmable load - 2	52
5.12	Maximum and Minimum Output Currents for a programmable load	52
5.13	Transient Parameters of the Overall System for a programmable load	53
5.14	Summary of Results	54
6.1	Different Corners for MOS Transistors in XT018 Technology	55
6.2	PVT Corners for $V_{bias} = 150\text{mV}$	79
6.3	PVT Corners for $V_{bias} = 700\text{mV}$	79
7.1	Specification vs Results	82

1 Introduction

Over the last ten years, the electronics industry has exploded. The largest portion of the total worldwide sales is dominated by the MOS market. Composed primarily of memory, micro and logic sales, the total combined MOS revenue contributed approximately 75 percent of the worldwide sales [2], illustrating the strength of CMOS technology. CMOS technology currently continues to mature, with minimum feature sizes now approaching 10nm. This has resulted in development in process technologies and have allowed design of circuits using devices running at lower currents, lower voltages and at higher unity gain frequencies. This has done signal processing world a great deal of good, resulting in creation of amplifiers with high speed and converters operating under low voltage conditions.

The necessity for high voltage integrated circuits, capable of driving high currents, remains greater than ever before, with countless applications related to emerging technologies [3]. There are numerous applications of high current amplifiers which can be used in any signal processing context involving driving loads which require high current. One of the common applications is in the Current Transformer circuit.

Operational Transconductance Amplifier(OTA) is a building block for most of the analog circuits with linear input-output characteristics. Operational Amplifiers (OP AMP) too are used as a basic building block in implementing a variety of analog applications such as amplifiers, summers, differentiators, integrators, etc to a more complicated applications like Oscillators.

For more than 50 years, silicon-on-insulator (SOI) technologies have been developed for radiation-hardened military and space applications. The use of SOI has been motivated by the full dielectric isolation of individual transistors, which prevents latchup. Many efforts have been made to reduce the parasitic structures and very high levels of radiation hardness have been achieved [4]. In addition, major chip manufacturers are now producing SOI technologies for many nonhardened high performance or low-power applications.

This document describes the design and implementation of such a radiation hard transconductance amplifier, which is used in a DC current transformer. The report is structured as follows: First, the concept of Closed Loop DC Current Transformer is introduced. Then, the theory of the building blocks of the design along with the design methodology are provided. After that, the design and implementation of each of these building blocks done in Cadence Virtuoso environment is documented in separate chapters. The corner simulation results of the design and the conclusion of the thesis work are documented in the subsequent chapters of this document.

1.1 Motivation

DC Current Transformers (DCCTs) are known as non-intercepting standard tools for online beam current measurement in synchrotrons and storage rings [5]. In general, the measurement principle of commonly used DCCTs is to introduce a modulating AC signal for a pair of ferromagnetic toroid [6]. Currently a Novel DCCT (NDCCT) based on modern magnetic field sensors is under development at *GSI Helmholtz Centre for Heavy Ion Research*. The closed-loop NDCCT Design can be considered as an extension to the primary design proposed by GSI [6]. A feedback loop was designed to improve the linearity and sensitivity of the NDCCT. Figure 1.1 shows the closed loop NDCCT structure [1]. The main objective is to provide a feedback current that cancels the magnetic field of the ion-beam inside the air gap. This measurement principle is referred to as "Zero-flux" and it is currently used in commercial DCCT. This zero-flux results in improvement of the linearity and sensitivity of the current transformer.

The change in magnetic field will be sensed by the TMR (Tunneling Magneto Resistance) sensor and a proportional small voltage is produced. This voltage is amplified by a Voltage amplifier and is converted to a feedback current I_{FB} by the OTA. This current flows through the N turns winding wire terminated with a resistive load. The main task of the OTA is to amplify a small AC voltage and produce a high current that drives a resistive load and cancels the magnetic field of the ion-beam.

Prior to this thesis, as a proof of concept [1], a Closed Loop NDCCT was constructed with the commercial OTAs - OPA860 and OPA861 [7]. 4 of those ICs in parallel to get a good understanding of the requirements from the OTA in terms of specifications and results with a dual bipolar power supply of 5V and -5V.

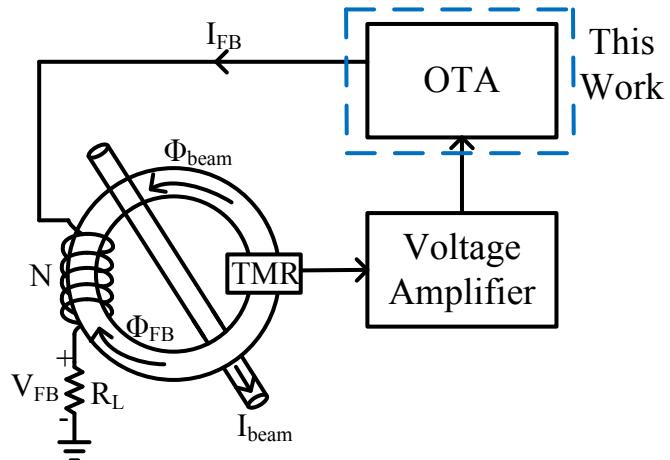


Figure 1.1.: Closed Loop Novel-DC Current Transformer [1]

1.2 Specification

As the transconductance amplifier will be a part of the NDCCT, the specifications of the design were obtained from the commercial OTAs OPA860 and OPA861, which were simulated as on a PCB with a power supply of 5V and -5V as part of the N-DCCT in a closed loop. Since the OTA is being targeted for multiple applications - a closed loop DCCT and also for an Analog to Digital Converter (ADC), it is important to make the design programmable. The specifications are tabulated in detail in Table 1.1.

Parameter	Value/Specification
Circuit Design	Programmable via I/V/external R or C
Transconductance Gain(Gm)	75 .. 140 mA/V
Linear Input Voltage Range	± 200 mV
Output Current Range	± 15 mA .. ± 30 mA
Bandwidth	10 MHz
Slew Rate	± 900 V/ μ s
Rise/Fall time	4.4 ns
Input Referred Noise	3 nV/ \sqrt{Hz} @few KHz
Input Impedance	0.5 M Ω
Output Impedance	55 K Ω
HD2	Less than -75 dBc
HD3	Less than -80 dBc
Open Loop Voltage Gain	Not less than +5 V/V
PSRR	± 20 μ A/V

Table 1.1.: Specifications of the Design

Remarks:

- Supply Voltage: 5V
- Max Load Resistance: 1k Ω
- Technology to be used: XT018 from XFAB

1.3 Technology

The technology used for designing the building blocks of the system is the XT018 technology. The XT018 series is XFAB's 0.18-micron Module High-voltage SOI CMOS Technology. It combines the benefits of SOI wafers with Deep Trench Isolation and those of a State of the art six metal layers 0.18-micron process[8]. The technology related component names used as part of the circuit design are as tabulated in Table 1.2.

Component	Name	Description
PMOS	pe5	5V PMOS
NMOS	ne5	5V NMOS
Resistor	rmtop	Top Metal Resistor
Capacitor	cmm4t	Single MIM Capacitor

Table 1.2.: Components used as part of XT018 technology

Silicon on insulator (SOI) technology refers to the use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrates in semiconductor manufacturing [9], especially microelectronics, to reduce parasitic device capacitance, thereby improving performance. The result is up to 30 percent lower power consumption, 20 percent higher performance and 15 percent higher density than the traditional bulk CMOS at the same feature size. SOI-based devices differ from conventional silicon-built devices in that the silicon junction is above an electrical insulator, typically silicon dioxide or sapphire. SOI inherently eliminates latchup [10], which can occur in CMOS devices due to parasitic conditions in which at least one transistor acts as a Silicon controlled rectifier (SCR). And since XT018 is an SOI technology, it is chosen to design the amplifier.

Radiation hardening is the act of making electronic components and systems resistant to damage or malfunctions caused by ionizing radiation (particle radiation and high-energy electromagnetic radiation), such as those encountered in outer space and high-altitude flight, around nuclear reactors and particle accelerators, or during nuclear accidents or nuclear warfare [11]. Most semiconductor electronic components are susceptible to radiation damage; radiation-hardened components are based on their non-hardened equivalents, with some design and manufacturing variations that reduce the susceptibility to radiation damage [12].

2 Theory

2.1 The Operational Transconductance Amplifier

The operational transconductance amplifier (OTA) is basically an op-amp without an output buffer [2]. An OTA can be defined as an amplifier where all the nodes are low impedance except the input and output nodes. A schematic symbol of an OTA is shown in Figure.2.1. OTAs are generally programmable usually through the bias current that is provided to a differential amplifier. In the symbol, a bias voltage is being used as a programmable input. This bias voltage in turn controls the bias current of the amplifier.

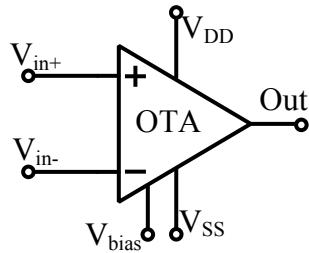


Figure 2.1.: Symbol of an OTA

2.1.1 Conventional Current Mirror OTA

The schematic of a conventional current mirror based OTA is as shown in Figure.2.2. The OTA employs a differential input pair in conjunction with three current mirrors. The differential input pair comprises of transistors M_1 and M_2 . The differential pair is biased by the current mirror formed by M_{nB1} and M_{nB2} . PMOS current mirrors formed by M_3 , M_5 and M_4 , M_6 reflect currents generated in the differential pair onto the output shell. The current generated by the mirror formed by M_3 and M_5 is reflected to the output via the NMOS current mirror formed by M_7 and M_8 . The current mirror gain factor is K . Increase in K will increase the slew rate and gain bandwidth along with the output current of the conventional OTA at the cost of increased area, static power dissipation and a decrease in phase margin.

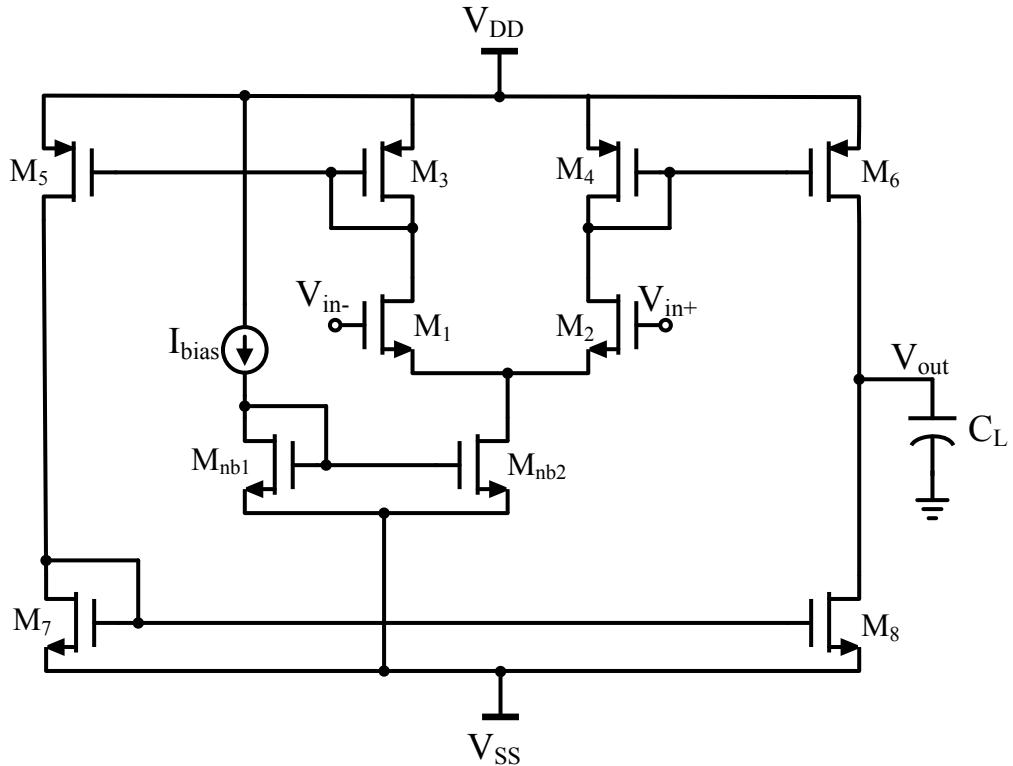


Figure 2.2.: Schematic of a Conventional Current Mirror OTA

Common mode signals are ideally rejected. i.e., when $V_{in+} = V_{in-}$, $I_{out} = 0$. A differential input signal will generate an output current proportional to the applied differential voltage based on the transconductance of the differential pair. And that is why OTA is known as Voltage controlled Current Source. Although the output stage is push-pull structure, the conventional OTA is only capable for producing an output current with a maximum amplitude equal to the bias current in the output shell, provided the current mirror gain is unity, i.e., $K=1$. For this reason, conventional OTA is referred to as a Class A amplifier.

The conventional OTA does not employ an output buffer and hence is only capable of driving capacitive loads and the capacitive load consumes all the current generated in the circuit. The gain of the OTA ($G_m R_o$) is dependent on the large output resistance of the output shell of the OTA formed by the transistors M_3 to M_8 . The output resistance is reduced to $G_m R_o // R_L \approx G_m R_L$ if a parallel resistive load R_L is applied.

Let us consider a hypothetical scenario that we do not need a resistive load to be driven as part of the system. In other words, we have a capacitive load as part of the specification. An advantage of this would be the fact that the need of an output buffer is eliminated and thereby the static power dissipation and the area occupied is reduced. But on the downside, the amplifier behaviour for the output current would be like that of a band pass filter. So this scenario will not be useful as the specification demands a bandwidth of 10MHz as the overall system would be targetting low frequency applications. So a capacitive load will limit the output current only to a certain band of frequencies and hence it will not make sense to just use a one stage design. This gives rise to design an output buffer for the OTA.

An output buffer can either be a voltage buffer or a current buffer depending on how the OTA is designed. A current buffer, for example, is used to hold the output current of the OTA at the output of the buffer. So any amplification needed for this current would in turn give rise to the need of another stage, making the design complicated. In this case usually a current feedback amplifiers are designed which theoretically has a low input impedance non-inverting terminal input and a high input impedance inverting terminal input. So the OTA output would directly be connected to this non-inverting terminal and with the use of internal buffers, the output current follows the input current.

In this work, however, a voltage buffer amplifier is designed. Therefore, the OTA is used as a programmable block to control the output voltage rather than the output current.

2.1.2 Other Topologies

The Conventional OTA considered in the previous section is a Class A type of amplifier. These amplifiers can produce output currents that are equal to the bias currents for a unity current mirror gain. Need for high speed and high current with low power dissipation gave rise to research in Class AB Amplifiers. There are many topologies of the Class AB type OTAs that are classified based on their structure as:

- Folded Cascode OTA [13]
- Telescopic OTA [14]
- Local Common Mode Feedback OTA [15]
- Cascode Voltage Flipped Follower based OTA [16]

One of the figures of merit to compare these OTAs is the Current Enhancement factor (CE). $CE = I_{out_max}/2I_{bias}$. Class A amplifiers typically have a CE of 1. Class AB OTAs have a high CE value [17]. A family of OTA denoted as *SuperClass – ABOTA* have remarkably large CE values. Typical value of CE ranges from 100 to 500 depending on the implementation of the Class-AB differential pair and the output branches. Cascode Voltage Flipped Follower based OTA is one such example of a Super Class-AB OTA. These OTAs have the largest reported CE in literature. Some of the OTA designs considered are explained in the next chapter.

2.2 The Operational Amplifier

The operational amplifier (OP AMP) is a fundamental building block in analog integrated circuit design. A typical symbol of an OP AMP is as shown in Figure 2.3. It consists of differential input terminals - inverting (V_{in-}) and non-inverting (V_{in+}), a positive supply pin (V_{DD}) and a negative/ground supply pin (V_{SS}) and the output terminal (V_{out}). Simple OP AMPS are generally used as Summing amplifier, differentiator, integrator, transimpedance amplifier, and so on. OP AMPS with vastly different levels of complexity are used to realize functions ranging from dc bias generation to high-speed amplification or filtering.

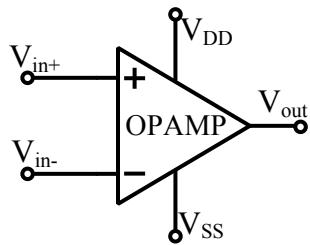


Figure 2.3.: Symbol of an OP AMP

OP AMPS are voltage controlled voltage sources, much to the contrary of OTAs, which are voltage controlled current sources. Design of an OP AMP consists of determining the specifications, selecting the device sizes and biasing conditions, compensating the op-amp for stability, simulating and characterizing the open loop gain, the input common mode range, common mode rejection ratio, power supply rejection ratio, output votlage range, current sourcing/sinking capability and power dissipation [18]. OP AMPS are used as a voltage buffer whenever there is a need to drive resistive loads or a combination of capacitive load and a resistive load.

2.2.1 Miller Compensation OP AMP

The schematic of the a two-stage Miller Compensation OP AMP is as shown in Figure 2.4. First stage of the OP AMP is the differential amplifier formed by the transistors $M_1 - M_5$ and M_8 . The second stage of the OP AMP is the Common Source amplifier formed by the transistors M_6 and M_7 . Compensation Capacitor or Miller Capacitor denoted by C_C is used for the splitting of the poles of the two stages thereby providing stability and also controlling the bandwidth and the slew rate.

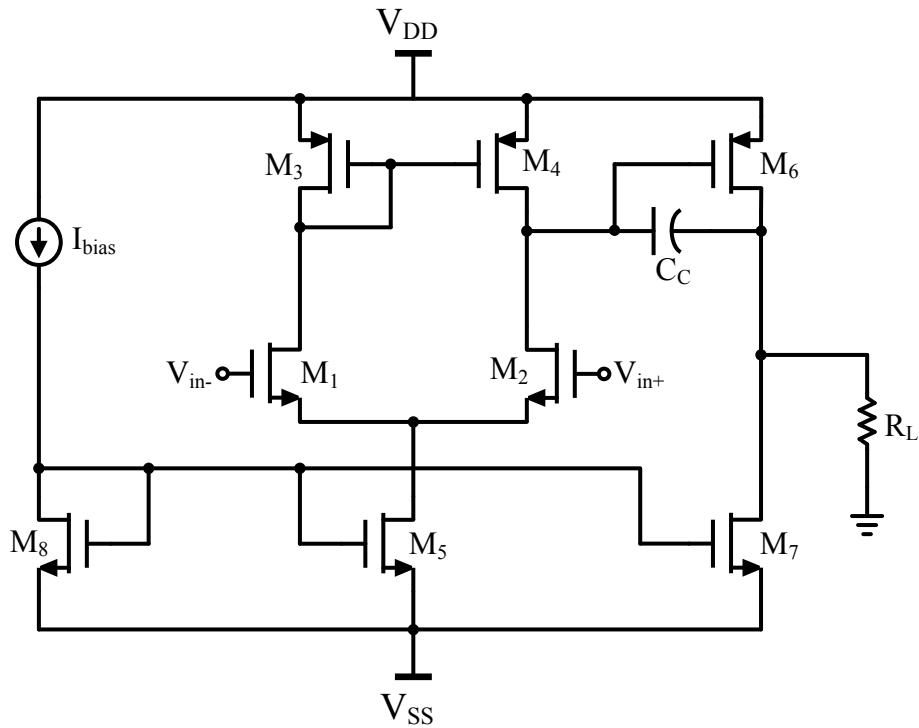


Figure 2.4.: Schematic of a Two-stage Miller Compensation OP AMP

The biasing to the differential input pair is provided by the current mirror formed by M_5 and M_8 . The selection of the bias current, I_{bias} is determined by gain, ICMR, CMRR, power dissipation, noise, slew rate and matching considerations. If slew-rate is of concern, a cross-coupled differential amplifier should be considered for the first stage. The second stage common source amplifier is used to provide an additional gain to the overall OP AMP since the gain provided by the differential pair is usually not large enough. It is known that OP AMPs have infinitely large open loop gain. This second stage also provided a current boosting since M_7 forms a current mirror with M_8 and the dimensions of M_7 are usually larger than M_8 , thereby setting the current at the output of the OP AMP. The best use of these OP AMPs are made as part of voltage buffers. i.e., the OP AMP is connected in unity gain configuration by providing a direct feedback from the output terminal to the non-inverting terminal.

2.3 The Gm/Id Methodology

Good analog design is an art, not a science. Best work are still done on napkins and not on EDA tools, i.e., using Hand Calculations. However in recent times, in most cases at least, the equations which were once valid have become inadequate. The ability of these equations are limited to only certain cases [19]. The famous equation for I_{ds} is naturally the first thing that comes to mind when someone says Square Law, which is given by

$$I_{ds} = \frac{\mu \cdot C_{ox} \cdot W}{2 \cdot L} \cdot (V_{gs} - V_{th})^2$$

The square law becomes linear in short-channel limit [20] and thus they are suitable only for long channel MOSFETs. The block diagram in Figure.2.5 [21] indicates the failure in Square law, especially in deep submicron technologies.

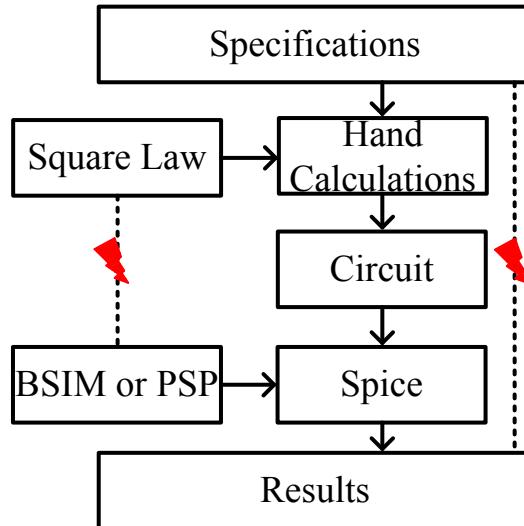


Figure 2.5.: Square Law Methodology

The ratio W/L is directly proportional to the transconductance (g_m) and inversely proportional to the overdrive voltage. With g_m fixed, smaller overdrive voltage translates to a wider MOSFET and thus larger C_{gs} . Thereby, the overdrive voltage is not a good design parameter. The values obtained from hand calculations for short channel MOSFETs are far away from accuracy according to the requirements and thus there will be a huge gap in the spice simulation results and the specifications. The reason why this methodology has still not been a disaster is that fact that it over-predicts the V_{dsat} , but keeps the transistors in saturation. Micropower design techniques, on the other hand, exploit weak inversion models.

The G_m/I_D methodology on the other hand, is fundamentally more practical than theoretical. It is based on a unified synthesis methodology in all the regions of operation of a MOSFET. This methodology uses pre-computed spice data in hand calculation, thereby providing accurate results. The diagram in Figure.2.6 shows that this methodology uses design tables which are pre-computed and using those tables, the hand calculations are made, which are rather simple and straight forward.

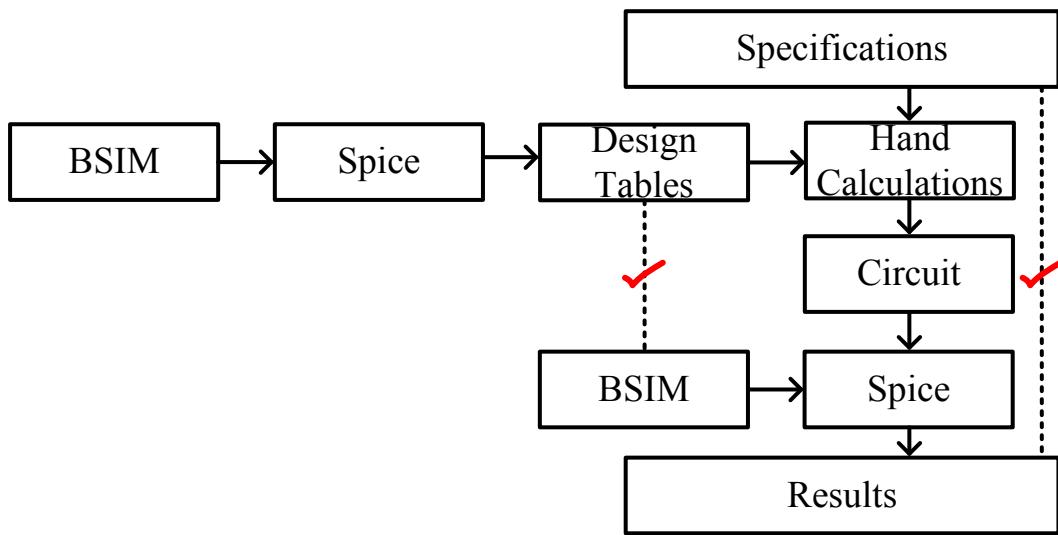


Figure 2.6.: Gm/ID Methodology

To obtain the design tables, we need to look at a transistor in terms of width-independent figures of merit that are linked to the design specification. The design trade-offs have to be considered in terms of MOSFET's inversion level by using G_m/I_D as a proxy [22]. What we really need from a MOSFET is - Large g_m without investing much current and without having large C_{gs} . To quantify how good of a job our transistor does, we can define certain "figures of merit". The figures of merit considered as part of this work for G_m/I_D methodology are G_m/I_D , f_T (transit frequency), G_m/G_{ds} (intrinsic gain), I_D (drain current), f_TG_m/I_D (design trade-off). The circuit in Figure 2.7 is used to simulate these figures of merit parameters that are necessary to make design decisions. The width of the transistor M_0 is set to $5\mu\text{m}$ and the length is kept as a variable. The value of V_{ds} is set to a value that is half of the value of the power supply. As part of this work, the supply we use is $+2.5\text{V}$ and -2.5V . So technically we have a voltage difference of 5V and therefore, the value of V_{ds} is set to 2.5V .

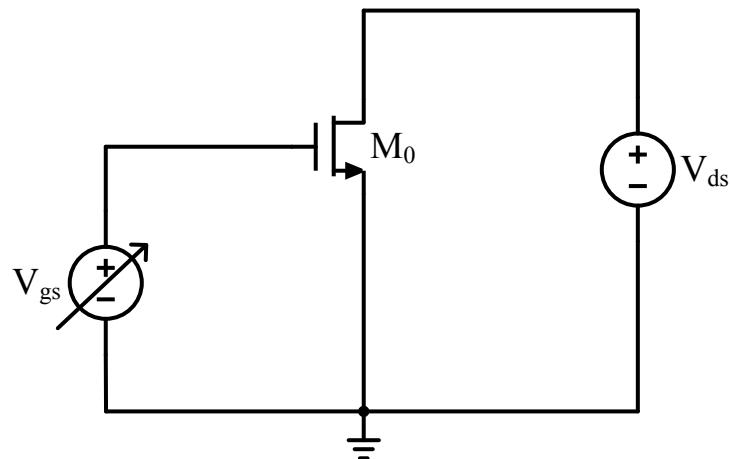


Figure 2.7.: Setup for simulating GmID parameters

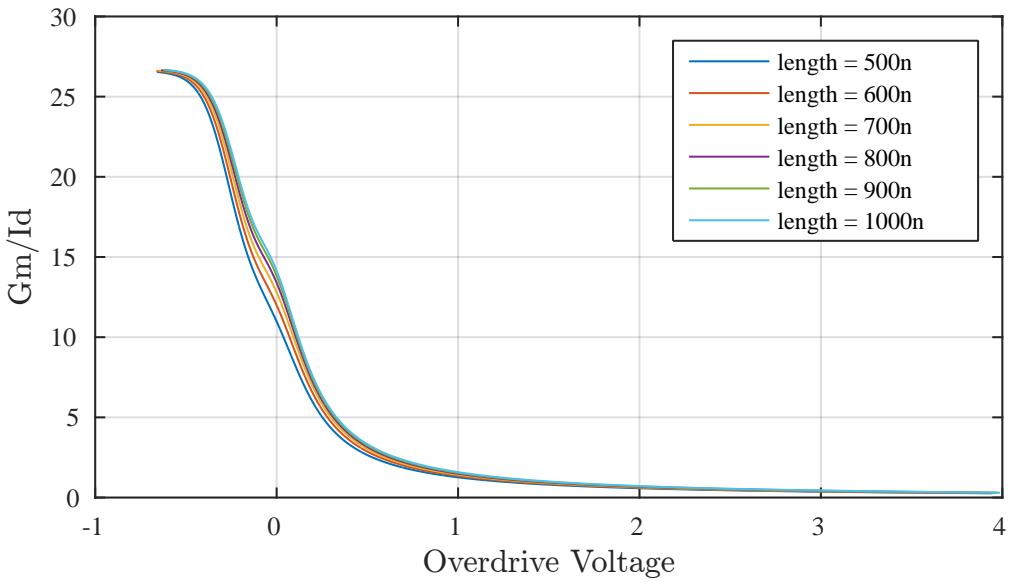


Figure 2.8.: G_m/I_D vs V_{ov}

The plot of G_m/I_D versus the Overdrive voltage for different lengths is shown in Figure 2.8. The value of G_m/I_D is very high when the overdrive voltage is less than zero, i.e., when the transistor is in weak inversion. The gain starts dropping with increase in overdrive voltage and it becomes close to zero and constant and that is where the transistor goes into strong inversion. The response to variation in length is minimal for this parameter.

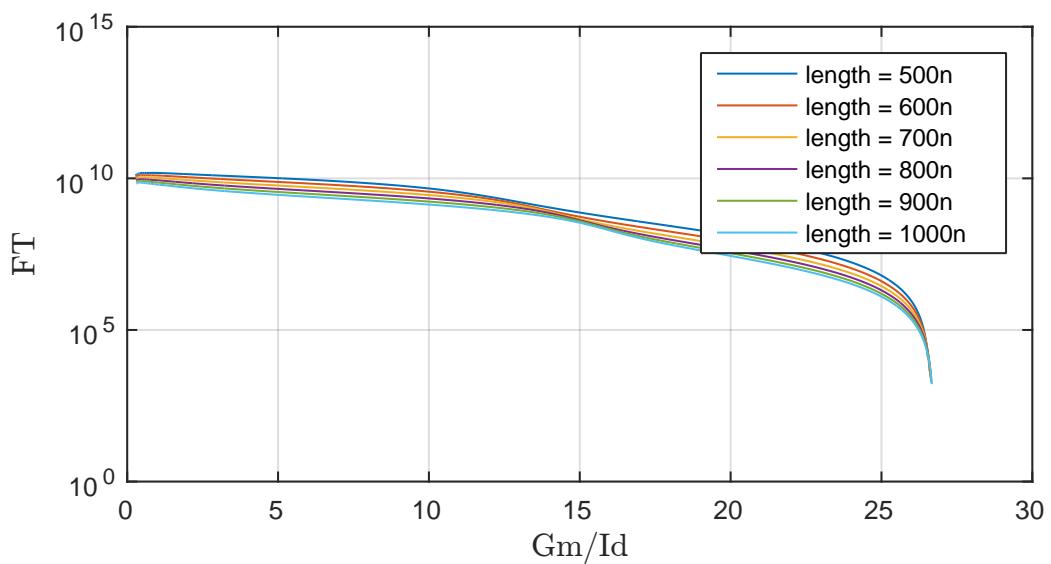


Figure 2.9.: f_T vs G_m/I_D

Transit frequency is defined as the ratio of the transconductance G_m to its gate to source capacitance C_{gs} . The plot of transit frequency against G_m/I_D for different lengths is as shown in Figure 2.9. This figure of merit is used to indicate the speed of operation of the MOSFET. And from the plot, it can be seen that the speed is high when the value of G_m/I_D is low. So this is quite the opposite to the gain parameter that was discussed with the previous plot. So here we have our first trade-off between high gain and high speed.

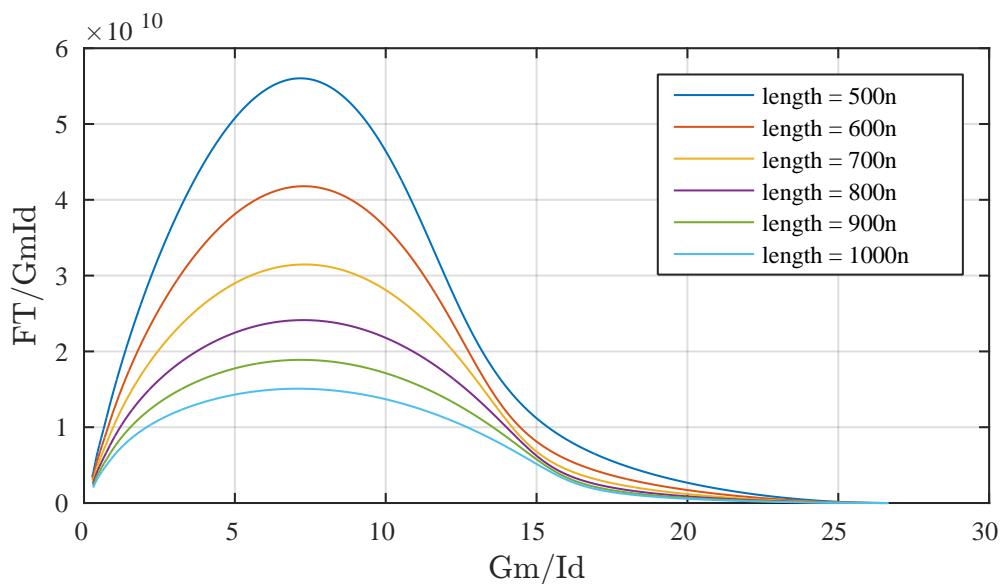


Figure 2.10.: $f_T G_m/I_D$ vs G_m/I_D

To evaluate the trade-off mentioned above, the product of the two figures of merit are considered and then plotted against the G_m/I_D parameter and is plotted as shown in Figure 2.10. The product is highest in moderate inversion. And this is called as the sweet spot and this provides the best possible trade-off between gain and speed. This is something that the mainstream methods like Square Law fail to provide because these methods generally assume strong inversion.

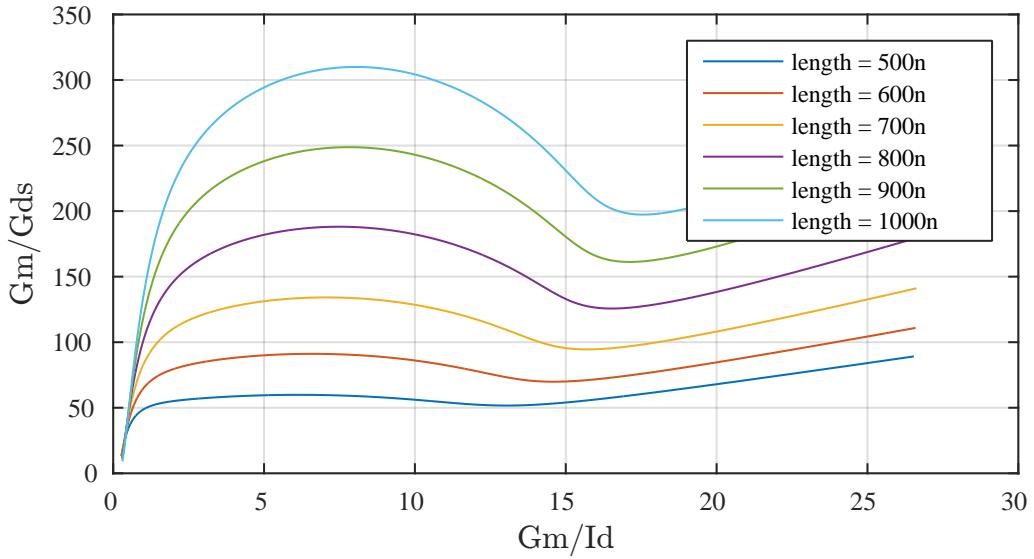


Figure 2.11.: G_m/G_{ds} vs G_m/I_D

The intrinsic gain G_m/G_{ds} is plotted against G_m/I_D as shown in Figure.2.11. This along with Figure.2.9 form a powerful tool in choosing the value of the channel length that meets the gain requirements. The plot in Figure.2.8 did not show too much of a variation with respect to length. But using this plot it is easy to decide the channel length of the transistor. It is clear that the smallest channel length in moderate inversion provide the highest gain with a decent trade-off with respect to speed, i.e., transist frequency.

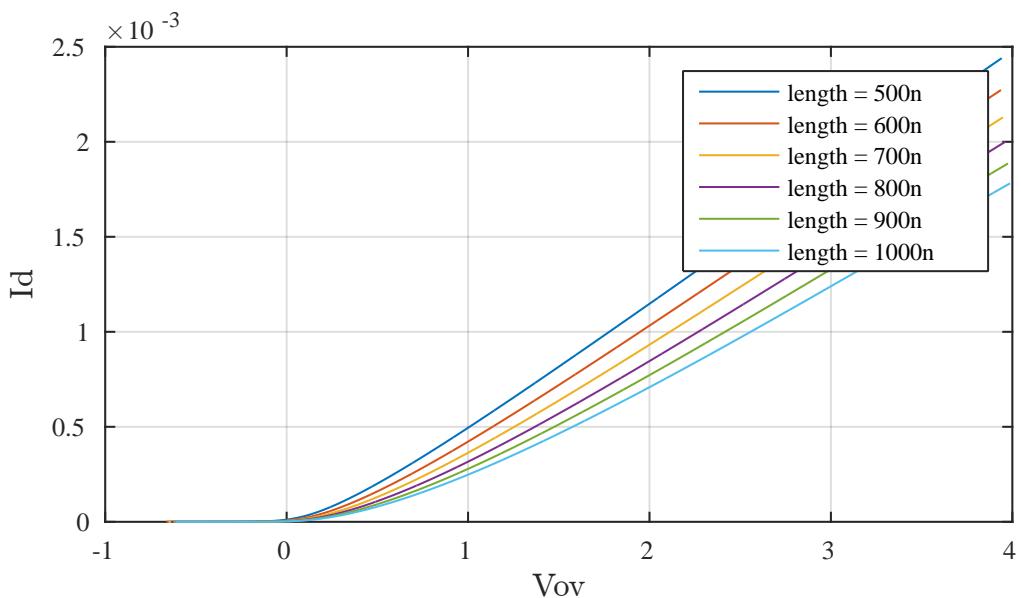


Figure 2.12.: I_D vs V_{ov}

The final plot we have here is to choose the drain current for the overdrive voltage needed. It is as shown in Figure 2.12. Ultimately, it is the overdrive voltage that determines the region of operation of the transistor. So with the overdrive voltage known and the length of the transistor decided, the drain current can be easily chosen.

An important thing not to forget is that the figures of merit simulated and plotted are independent of variation in the width of the transistor. So once, the other parameters are decided, the value of W can be chose using the I_d/W plot. The steps involved in the general design flow of this methodology is summarized below.

- Determine G_m from (design objectives)
- Pick the channel length L
 - Short channel \rightarrow high f_T (high speed)
 - Long channel \rightarrow high intrinsic gain
- Pick G_m/I_D (or f_T)
 - Large $G_m/I_D \rightarrow$ low power, large signal swing
 - Small $G_m/I_D \rightarrow$ high f_T (high speed)
- Determine I_D (from G_m and G_m/I_D)
- Determine W (from I_D/W)

There are many other possibilities to design using this methodology and this depends the specifications, constraints and objectives. However, as part of this thesis the steps mentioned above are followed and the plots discussed above are used to design the differential pair of transistors for all the stages of the system. And the other transistors' dimensions were finalized using simulations.



3 Operational Transconductance Amplifier

3.1 Design and Implementation

OTAs are versatile building blocks that offer a wide bandwidth for many types of amplifiers. OTA can work in a voltage mode as well as a current mode. As part of this work, the OTA is used in voltage mode. Most circuits for the OTA of a given application consists of variation on a few basic types. And because OTAs have a wide range of applications, there are several different topologies that are useful for these applications. The typical topologies were studied as part of this thesis and an overview at a system level for each of them is provided in the subsequent sections.

Commercial OTA

OPA860 by Texas Instruments is one of the most popular commercial OTA in the market. The design document [23] of OPA860 compares OTA to a 3 terminal transistor - a high impedance input(base), low impedance inout(emitter) and a current output(collector). OTA is therefore bipolar and self-biased. Being self-biased simplifies the design process and reduces component count. The overview of the OTA is as shown in Figure 3.1. The transconductance of the OTA can be adjusted using an external resistor, allowing bandwidth, quiscent current and gain trade-offs to be optimized. Reducing or increasing the size of the OTA controls the bandwidth, AC behavior and transconductance. With a fixed external resistor, the quiscent current increases with increase in temperature. The variation of the current with temperature holds the transconductance of the OTA relatively constant with temperature.

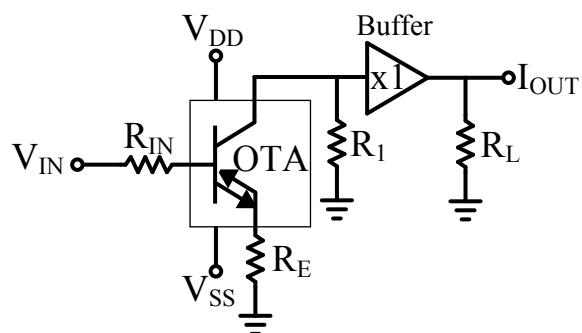


Figure 3.1.: Overview of Commercial OTA OPA860

The commercial OTA in review, can operate in 2 modes - Voltage mode and Current mode. In voltage mode, it can operate in 3 states - common emitter, common base and common collector. In current mode, it is useful for analog communication such as current amplifier, current differentiator, current integrator and current summer. The output offset voltage is usually very close to zero for an OTA.

Having stated all these facts, this commercial OTA is an amplifier based on BJTs. Considering the high power dissipation and high input current noise of a BJT based amplifier, it is not suitable for our system.

However, the concept of having an OTA and an output buffer [24] is something that can be pondered upon.

Self-Cascode OTA

An intriguing concept of Self-Cascode can be used to achieve very high gain for a low supply voltage. A high gain 2-stage self cascode OTA for a 1V supply was researched as part of [25]. A self-cascode MOSFET (SCMOS) has a similar geometrical structure to a regular MOSFET. But still, the transconductance, and the output resistance of an SCMOS are much better than its conventional counterpart. A regular channel requires a long channel for high gain and a short channel for high speed. With the same channel length of a regular MOS, an SCMOS will provide a much higher gain without compromising the speed. An SCMOS is formed where a regular MOSFET will be replaced by two transistors whose gates are tied together, as shown in Figure.3.2. The two transistors have same widths. The operating regions of M_1 and M_2 depend upon the common gate voltage of the SCMOS. If V_g is greater than V_{th} of both the MOSFETs, then M_1 and M_2 operate in linear and saturation region respectively. With a bulk bias, the threshold voltage of the drain transistor (M_2) decreases. This increases the V_{ds} of M_1 , resulting in moving of its operating point from linear to edge of saturation, i.e., moderate inversion. And this is where the gain is high. Suppose both transistors are operating in saturation, the maximum output resistance can be achieved but the voltage swing is considerably reduced.

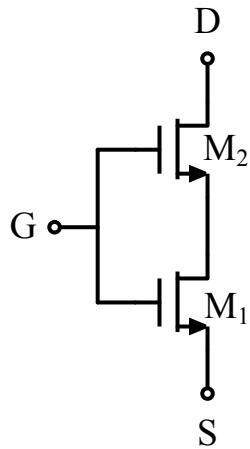


Figure 3.2.: Schematic of a Self-Cascode MOSFET

In the context of an OTA, consider a conventional OTA with their regular MOSFETs replaced by SCMOS. To improve the gain of the OTA, positive feedback is created by cross coupling the bulk terminals of the input stage load transistors. Smaller channel length CMOS requires scaling down of power supply to maintain reliability of the circuit. A dual function gate MOSFET with a focus on increasing output resistance and transconductance is equivalent to a self cascode structure. A floating gate MOSFET is another alternative to the conventional techniques used to enhance DC gain. But, both these techniques require complicated fabrication steps. On the other hand, a current shunt technique can be applied to a self-cascode OTA to increase its gain. But this has reduced phase margin and requires compensation circuit even for a single stage.

A self-cascode OTA is very helpful in achieving a high gain for low power supplies. But give the nature of our system, and the fact that the OTA to be designed as part of this system is to be an open loop amplifier,

a very high gain is something that is suitable for the system in order to avoid saturation at the output as the headroom for output transistors would be very less. Another possible drawback is that the self-cascode OTA exhibits a slew rate that is lesser than the conventional OTA because the output current is low. But in case our system had to work in a closed loop, then this concept of self-cascode would have been a better fit.

2-stage Feed Forward Miller Compensation OTA

The system level diagram of a feed-forward Miller compensated OTA is shown in Figure.3.3. The g_{m1} and g_{m2} are input and output stage of the OTA and g_{mf} is the feed-forward path from input to output node. The implementation is based on feed-forward technique proposed in [26]. There is no concept of pole splitting. The location of poles is mainly dependent on the internal node impedance and parasitic capacitance. It is difficult to estimate the parasitic capacitances and it makes the design complex. Therefore the dominant and non-dominant pole locations will change when the OTA is configured in a closed loop. But using Miller compensation, the poles can be placed at desired locations.

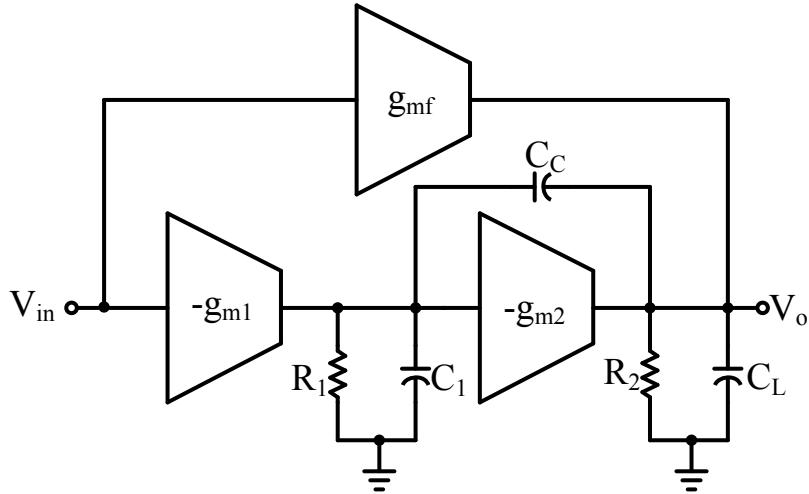


Figure 3.3.: Block Diagram of Feed Forward Miller Compensation OTA

This topology of OTA is considered to consume less power than the conventional Miller compensation OTA. Feed forward compensation technique gives wider bandwidth as compared to the Miller OTA and is much more easier to stabilize. However the overall bandwidth is lesser than what a conventional current mirror based OTA can provide. Current replicating branch with scaled down transistors can be used to implement a push-pull output stage that gives the maximum output current several times higher than that of bias current. Cascoding and gain boosting are conventional techniques for gain enhancement. But for low voltage designs, these techniques are not suitable due to limited head room. Cascading multiple gain stages is another alternative for the gain enhancement. But in a closed loop, the amplifier becomes unstable due to high impedance nodes at each stage, which produces negative phase shift and degrades the overall phase margin. To overcome this, the multi-stage amplifier needs a compensation circuit to achieve a minimum phase margin for stability.

The results of this topology were interesting and encouraging. But that fact that needs multiple stages and compensation circuitry just for a OTA without a buffer, makes it complex in spite of the encouraging remedies. So weighing the pros and cons of the topology and comparing it with other OTAs in review,

this topology was deemed to be a bit too much for our requirements and question of feasibility comes into picture.

A robust Feed Forward scheme without Miller capacitance

This scheme uses a positive phase shift of left hand plane (LHP) zeros caused by the feedforward path to cancel the negative phase shift of poles to attain good phase margin. The two-stage path increases the low frequency gain further while the feed forward single stage amplifier makes the circuit faster. The amplifier bandwidth is not compromised by the absence of the traditional pole-splitting effect of Miller compensation capacitor, resulting in a high gain wide-band amplifier [27].

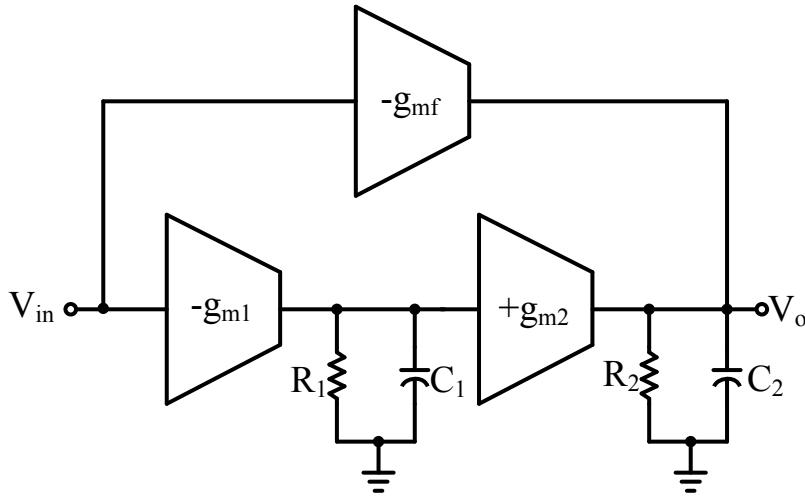


Figure 3.4.: Block Diagram of Feed Forward OTA without Miller Capacitor

Amplifiers with high-gain generally use multi-stage designs. And transistors with long channel length are chosen and biased at low current levels. Amplifiers with high-bandwidth use single-stage designs with short channel length transistors biased at high current levels. In a Miller compensated amplifier, due to the Miller effect, the dominant pole is pushed towards lower frequencies, resulting in lower bandwidth. Along with this, the phase response is degraded with a RHP zero. A nulling resistor is used to cancel the effect of this RHP zero. The pole-zero pair is created at high frequencies to avoid the slow settling components associated with pole-zero cancellation at low frequencies.

This scheme results in an amplifier with high gain and fast response. Bandwidth improvement is due to the fact that poles are not split. There could be substantial reduction in the area and power as there is no Miller compensation capacitor. As part of the circuit realization, the second and feed-forward stage should not have any dominant pole before overall frequency for gain bandwidth. Pole-zero cancellation should occur at high frequencies for best settling time performance. The first stage in this scheme is usually designed to have a high gain and a small load capacitance. The second and feedforward stages should be optimized for high bandwidth and medium gain performance.

This topology offers several advantages over the other topologies reviewed during the design phase. Some aspects to be careful about are - the feed-forward stage has to be optimized to make sure the pole-zero cancellation occurs at high frequency otherwise there is a possibility of having an unstable system. Another drawback as in the previous case is the complexity of the circuit given that this scheme was initially intended

to work for a single input design. Having two different pairs to transistors that need biasing at its gate terminals along with the complexity of the design, makes the programmability of the circuit a mystery. And since that is an integral part of our specification, this scheme might not be entirely suitable for our design despite offering more advantages than disadvantages.

Super Class AB OTA

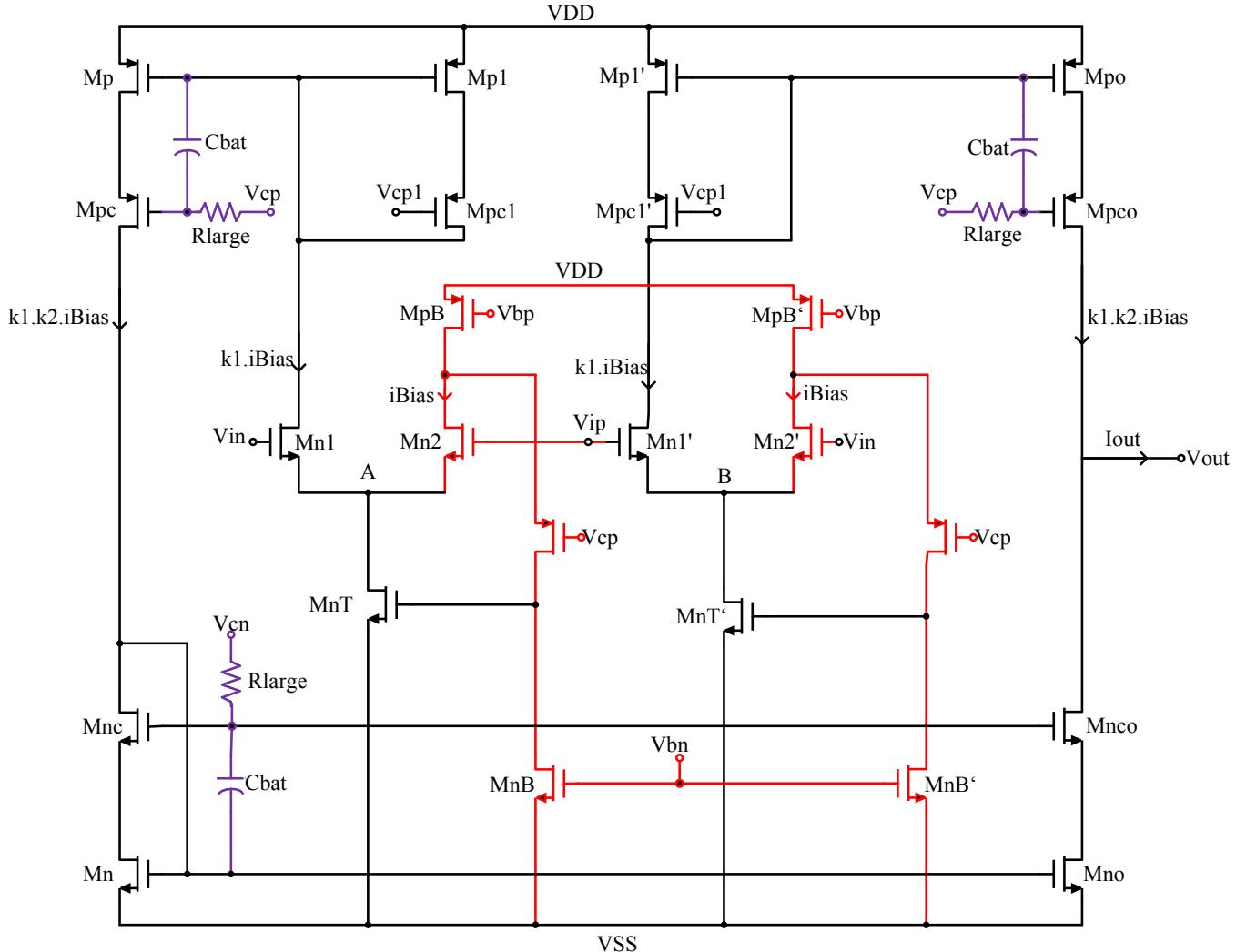


Figure 3.5.: Super Class-AB OTA with a Cascode Voltage Flipped Follower

The schematic of a Super Class AB OTA based on a Cascode Voltage Flipped Follower is as shown in Figure 3.5. It uses a Class-AB differential pair to boost the bias current by a factor of k_1 . Typical values of k_1 range from 30 to 60 depending on the implementation of the Class-AB differential pair and supply voltages. An additional current boosting by a factor of k_2 is obtained in the output branches. The typical values of k_2 range from 3-8. Using cascode transistors maximum output current and subsequently the CE values are reduced. But lack of cascode transistors results in very low open loop gain. Therefore, a simple power efficient technique is used that allows the use of cascode transistors in order to achieve even higher open loop gain and gain bandwidth by maintaining a large CE value. This is done with the help of dynamically biasing the cascode transistors using RC networks (indicated in purple in the figure) [16].

The capacitor C_{bat} acts as a floating battery for dynamic operations that transfers variations in the gate voltages of mirror transistors to the gate of the cascode transistors. This increases the V_{DS} of the mirror transistors allowing high output currents. Cascode Voltage Flipped Follower (indicated in red in the figure) is characterized by high input swing and can operate over a wide range of supply voltages. It uses local shunt feedback to provide nodes A and B with very low impedance.

Taking into account the complexity, output current requirements and load requirements, this design will not be considered further as part of this research work. The reason being - a high current output of this Class AB OTA would give rise to another output buffer. And the capacitors needed to consume such a high current would be in the order of several pico Farads. Having such a big capacitor inside an IC is not recommended. Also, considering how complex CMOS Current Feedback Amplifiers are, it is wise to stick to a simpler design that does the same work but with some minor trade-offs.

Conventional Current Mirror OTA

Two separate designs - OTA with PMOS Differential pair and OTA with NMOS Differential pair were designed and simulated in Cadence to get a good understanding of the circuit parameters and how the differential pair impact them.

Generally, amplifiers with PMOS transistors used as differential input offer high linearity, low flicker ($1/f$) noise. A possible reason to choose PMOS transistors as a differential pair comes from the necessity to reduce the influence of the substrate noise. The two transistors are in an N-well and the well is connected to the supply voltage that any substrate interference coupled via the parasitic capacitance to substrate is decoupled to the VDD line [28]. P-channels typically have less flicker noise ($1/f$ noise) caused by the carriers randomly entering and leaving traps introduced by defects near the semiconductor surface. Since the majority charge carriers are holes in PMOS, there are less potential to be trapped in surface states.

Having stated all these facts, NMOS input transistors would be better in terms of transconductance gain, and hence thermal noise and the bandwidth of the amplifier. An important fact considered in the selection of the type of differential pair is that the OTA in this system is being used in an open loop. This means that the gain of the OTA has to be limited in order to avoid saturation at the crests and troughs at the output of the OTA.

PMOS transistors exhibit their low noise behaviour due to the fact that PMOS transistors are usually bigger (higher W/L ratio) than an NMOS pair. Since we need a small open loop gain, we cannot afford to have big transistors at the input that cause the output to saturate. Along with this, it was also seen that, the range of bias currents needed to obtain a similar range of voltage swing was much wider in case of PMOS than NMOS. Since this indirectly results in a high power dissipation in the 1st stage itself, it was concluded to use the NMOS based design as part of this Thesis work.

Comparison of Topologies

Topology	Advantages	Disadvantages
Commercial OTA OPA860	Simple design, wide bandwidth, high gain	BJT based design; high power consumption, high input current noise
Self Cascode OTA	High gain for low supplies; good tradeoff between high gain and high speed	low output current, Low slew rate; High gain in an open loop will cause saturation
Feed forward compensation with Miller Capacitance	Wide bandwidth; less power dissipation	Unstable when cascaded. Need for compensation circuitry
Robust feed forward compensation without Miller Capacitance	Area and power reduction; enhanced bandwidth	Need to optimize feed forward stage for pole-zero cancellation at high frequencies; Complex circuit
Super Class AB OTA	High current in a single stage; No open loop degradation	3 RC circuits mean increased area and power consumption; Complex input stage; High output capacitance
Conventional Current Mirror OTA	Simple Design; Easy to achieve programmability	Multiple branches lead to higher power dissipation; Output current and Slew Rate are limited

Table 3.1.: Comparison of OTA Topologies

3.1.1 Schematic

Figure.3.6 [15] shows the schematic of the OTA used as part of this Thesis. As mentioned above, the differential amplifier is formed by the NMOS pair M_1 and M_2 and dimensions of the differential pair was fixed using the figures of merit of the G_m/I_D methodology. The bias current I_{bias} to the differential pair is provided by the current mirror formed by M_{nB1} and M_{nB2} which is in turn controlled by the PMOS transistor M_9 whose gate voltage V_{bias} is the programmable variable of the OTA and the entire system. This bias voltage is inversely proportional to the bias current flowing through each branch of the OTA.

From the Table.3.2, it can be seen that the current mirror gain for the current mirrors formed by M_3 , M_5 and M_4 , M_6 is 3. It can also be noted that the transistors M_5 and M_8 are not symmetric with respect to their counterparts. This is designed so to make sure the DC bias point at the output of the OTA is close to 0V, which is the mid point of V_{DD} and V_{SS} . Changing the bias current of an amplifier, will automatically change the DC bias point at its output. Since we are using the OTA as a programmable block, it is important to have an output which is symmetric over 0. Even though it is not entirely possible, making these two transistors a little assymetric or uneven would close the gap between the bias points for highest and lowest bias currents. Initailly during the design phase, the load capacitance value was set at 1pF. Since it was necessary to have a second stage for the OTA, it only made sense to have a smaller capacitor as it would be going as part of the IC. Keeping that in mind and simulating the OTA with the OP AMP, the load capacitance is set at 50fF in order to achieve the required bandwidth and a stable enough system across various values of V_{bias} .

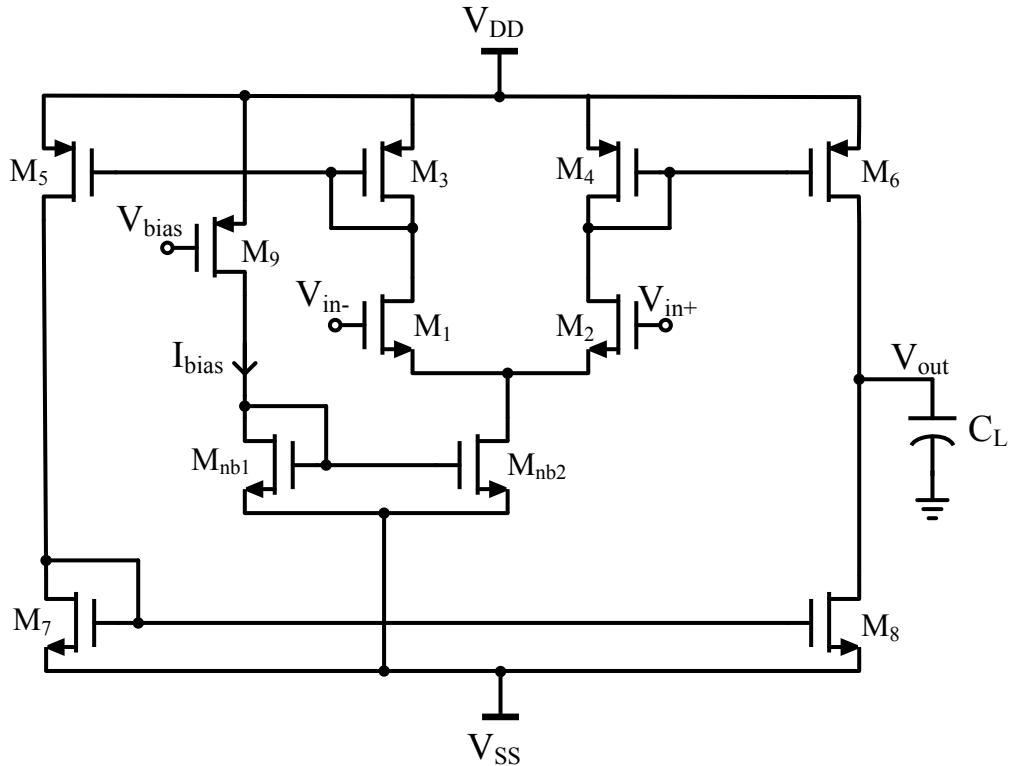


Figure 3.6.: Schematic of the OTA Designed

Transistor	Width(μm)	Length(nm)	Multiplier
M1, M2	8	500n	5
M3, M4	35	500n	1
M5	28	500n	3
M6	35	500n	3
M7	35	500n	18
M8	33	500n	18
M9	10	500n	4
MnB1, MnB2	20	500n	8

Table 3.2.: Dimensions of the Transistors of the designed OTA

3.2 Test Setup

The test bench setup for the operation transconductance amplifier is as shown in Figure 3.7. All the analyses are carried out under a standard temperature of 27°C , typical mean conditions for the NMOS transistors, PMOS transistors, capacitors and resistors unless explicitly mentioned otherwise. The *ocean* script containing all the expressions to measure the various parameters of the OTA are attached in the Appendix. In the following subsections, the results of these parameters are discussed using DC Analysis, AC Analysis, Transient Analysis and Noise Analysis separately.

3.2.1 DC Analysis

The test bench in Figure.3.7(a) and (b) are used to perform the DC analysis. The test bench in (a) is used to measure the DC bias point at the output of the OTA. Since the programmable input indirectly controls the bias current, the DC bias at the output consequentially changes as the current flowing through the output branches is a function of a bias current due to the current mirror configuration between the adaptive load and the output shell. So for large bias currents, the DC bias point is a higher value and vice versa.

$$V_{DD} = 2.5V; V_{SS} = -2.5V; V_{cm} = 1.95V; V_{bias} = 150mV \text{ to } 700mV; C_L = 50fF.$$

Vbias (mV)	150	200	300	400	500	600	700
Output DC Bias (mV)	13.68	-16.43	-78.96	-144.6	-213.3	-285.2	-360.3

Table 3.3.: Output DC Bias Point of the OTA

The output DC bias points for various values of V_{bias} is tabulated in Table3.3. The DC voltage at the output decreases with the increase in bias voltage or decrease in bias current. The test bench in (b) is used to check the offset voltage of the OTA. With a varying DC bias, there will be different offset voltage for each V_{bias} which does not make sense since the offset voltage is usually a single value.

3.2.2 AC Analysis

The test bench in Figure.3.7(a),(c),(d),(g) and (h) is used to analyse the small signal parameters of the OTA.

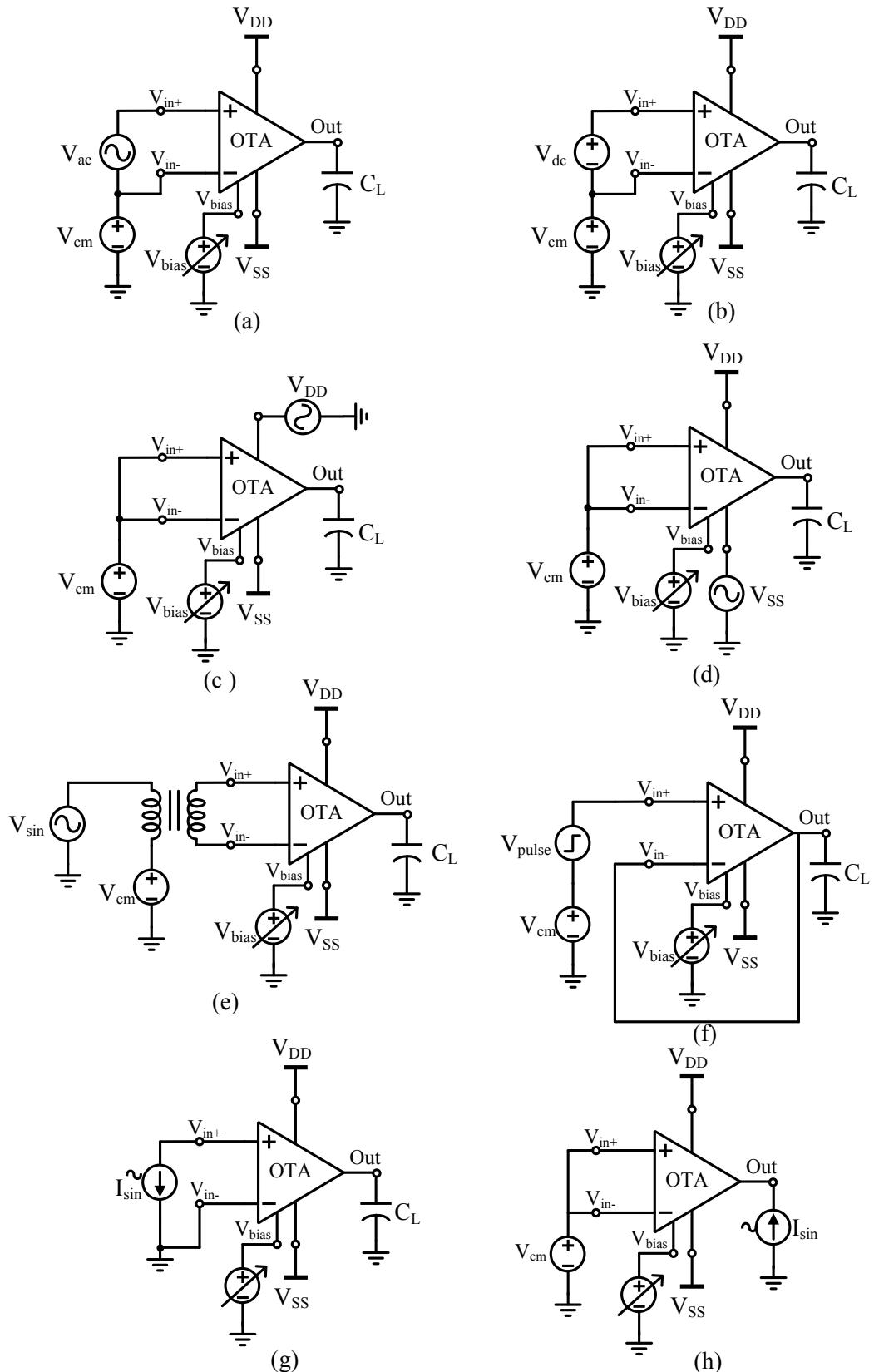


Figure 3.7.: Test bench setup for OTA

(a)Bias, Gain, Bandwidth, Input Referred Noise; (b)Offset; (c)PSRR(V_{DD}); (d)PSRR(V_{SS}); (e)Transient - Sine; (f)Transient - Square; (g)Input Impedance; (h)Output Impedance

Gain, Bandwidth and Phase Margin

Consider the Figure 3.7(a) with the circuit conditions:

$$V_{DD} = 2.5V; V_{SS} = -2.5V; V_{cm} = 1.95V; V_{bias} = 150mV \text{ to } 700mV; V_{ac} = 1V; C_L = 50fF.$$

$$\text{Gain in dB} = 20\log_{10} \frac{V_{out}}{V_{in}}$$

Figure 3.8 shows the semilog plot of Gain for maximum and minimum V_{bias} . The plots for the other values of V_{bias} are not shown here for simplicity.

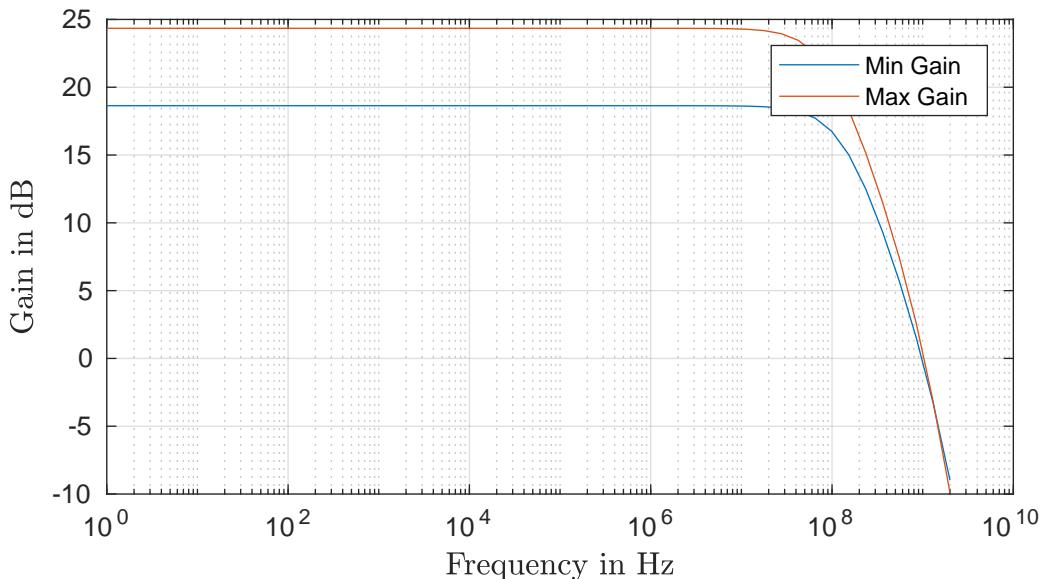


Figure 3.8.: OTA Plot of Gain vs Frequency for different V_{bias}

The variation of open loop gain of the OTA, its bandwidth and the phase margin with respect to V_{bias} is tabulated in Table 3.4. The bandwidth is kept at a high value in order to make sure that the dominant poles of the first and second stages are sufficiently far from each other so as to obtain a stable system for operation. The maximum open loop gain for this system is 23.7dB. Any value beyond this will cause the amplifier to saturate at the crests and troughs of the output voltage.

V_{bias} (mV)	150	200	300	400	500	600	700
Open Loop Gain (dB)	18.64	19.46	20.9	22.05	22.96	23.7	24.35
Phase Margin (degrees)	63.3	60.63	55.96	52.42	49.91	48.12	46.72
Bandwidth (MHz)	135	130.7	122.2	113.7	105	96.63	89.19

Table 3.4.: Open Loop Gain, Phase Margin and Bandwidth of the OTA

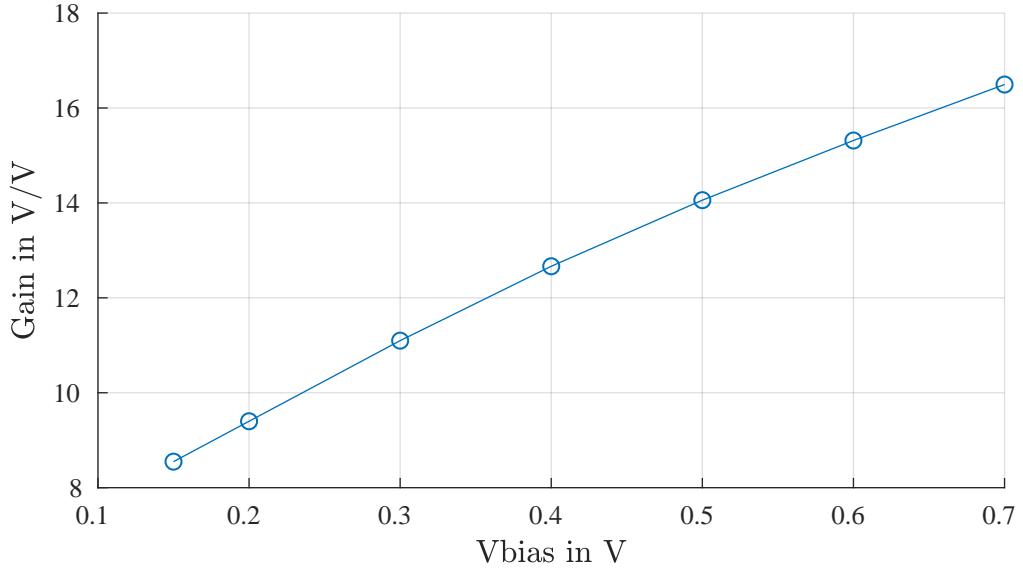


Figure 3.9.: OTA Plot of Gain vs Vbias

On the same lines, the variation of absolute value of gain with respect to different values of V_{bias} is seen in Figure 3.9 tabulated in Table 3.5. The reason to choose the values of V_{bias} are evident from this table and that is because it provides us a gain in the ratio of almost 1:2 for those values of V_{bias} . As seen from the table of specifications that we need a transconductance in the ratio of 1:1.8 or something close to that.

Vbias (mV)	150	200	300	400	500	600	700
DC Gain (V/V)	8.548	9.4	11.1	12.67	14.06	15.31	16.49

Table 3.5.: Absolute values of DC Gain of the OTA

PSRR

Figure 3.7(c) is the test setup to measure PSRR for a change in V_{DD} and similarly the one in Figure 3.7(d) is used to measure PSRR for a change in V_{SS} . The circuit conditions are:

$$V_{DD} = 2.5V; ACMagnitude = 1V; V_{SS} = -2.5V; V_{cm} = 1.95V; V_{bias} = 150mV \text{ to } 700mV; C_L = 50fF.$$

The variation of PSRR with respect to V_{bias} is tabulated in Table 3.6. The PSRR is fairly low in the range of nA/V and increases only slightly with increase in V_{bias} .

Vbias (mV)	150	200	300	400	500	600	700
PSRR (VDD Supply) (nA/V)	234.6	236.9	241.6	246.7	252.2	258	264.3
PSRR (VSS Supply) (nA/V)	254.5	256.5	260.4	264.2	267.9	271.5	274.9

Table 3.6.: Power Supply Rejection Ratio of the OTA

Input Impedance

OTAs generally exhibit a very high input impedance. And to measure this parameter, an AC current source with a magnitude of 1A is connected to the non-inverting terminal of the OTA. And the input impedance is given by the ratio of the AC voltage to the AC current at the input of the OTA. Since the current at the input is 1A, the magnitude of the input voltage will be the value of the input impedance in Ohms at that particular frequency. Since the OTA operation is carried out at 1MHz, the voltage at 1MHz is considered to obtain the value of Input Impedance. Figure.3.7(g) shows the test bench to measure the input impedance, with the circuit conditions:

$$V_{DD} = 2.5V; V_{SS} = -2.5V; V_{bias} = 150mV \text{ to } 700mV; C_L = 50fF; I_{sin magnitude} = 1A.$$

The variation of input impedance with respect to V_{bias} is tabulated in Table.3.7. The variation is quite small and it increases slightly with an increase in bias voltage and is in the order of Mega Ohms.

Vbias (mV)	150	200	300	400	500	600	700
Input Impedance ($M\Omega$)	3.38	3.388	3.403	3.419	3.434	3.45	3.467

Table 3.7.: Input Impedance of the OTA

Output Impedance

The output impedance is measured with a help of a current source with unity magnitude at the output instead of a Capacitive load. The differential inputs are connected in a common mode configuration. The test bench to measure the output impedance of the OTA is as shown in Figure.3.7(h).

$$V_{DD} = 2.5V; V_{SS} = -2.5V; V_{cm} = 1.95V; V_{bias} = 150mV \text{ to } 700mV; I_{sin magnitude} = 1A.$$

As discussed in the theory chapter, OTAs generally have high output impedance. And its variation with respect to V_{bias} is tabulated in the Table.3.8

Vbias (mV)	150	200	300	400	500	600	700
Output Impedance ($k\Omega$)	1.262	1.3	1.382	1.473	1.577	1.697	1.837

Table 3.8.: Output Impedance of the OTA

3.2.3 Noise Analysis

Once again, we use the same test bench as shown in Figure.3.7(a) to perform the noise analysis. As mentioned in the previous sections of this chapter, the NMOS differential pair exhibits high flicker noise, also known as $1/f$ noise. This noise is significant at low frequencies. At moderate and high frequencies, the effect of thermal or white noise is much more dominant and hence flicker noise becomes less significant at those frequencies.

The variation of the input referred noise with respect to V_{bias} is tabulated in Table.3.9. With increase in V_{bias} , the input referred noise decreases. This is because the gain increases with increase in V_{bias} and

consequently input referred noise decreases. This also converges to the fact that the input referred noise decreases with bigger dimensions of the differential pair, and thereby contributing to a higher gain.

Vbias (mV)	150	200	300	400	500	600	700
Input Referred Noise (nV/ \sqrt{Hz})	46.36	43.73	39.83	37.29	35.57	34.31	33.28

Table 3.9.: Input Referred Noise of the OTA

3.2.4 Transient Analysis

For the OTA designed, the transient analysis is performed for sine wave input and square wave input. The test bench in Figure.3.7(e) and (f) is used to perform the transient analysis of the designed OTA.

Sine Input

The test bench in Figure.3.7(e) is used to measure the transient parameters for a sine wave input with the circuit conditions as shown below. An ideal balun is used at the input to provide a differential voltage to the terminals. The voltages are 180^0 out of phase with each other.

$V_{DD} = 2.5V; V_{SS} = -2.5V; V_{cm} = 1.95V; V_{bias} = 150mV \text{ to } 700mV; V_{sin amplitude} = 100mV; frequency = 1MHz; C_L = 50fF$.

The transient simulation is carried out for $3\mu s$. The sinusoidal output with respect to time is shown in Figure.3.10 for different values of V_{bias} . As we know from the AC analysis, the gain varies in the ratio of 1:2 and thereby, here we have the peak-to-peak voltages varying in the same ratio. And as discussed in the DC Analysis, the DC bias points at the output are close to zero but not exactly at 0 for all the V_{bias} values.

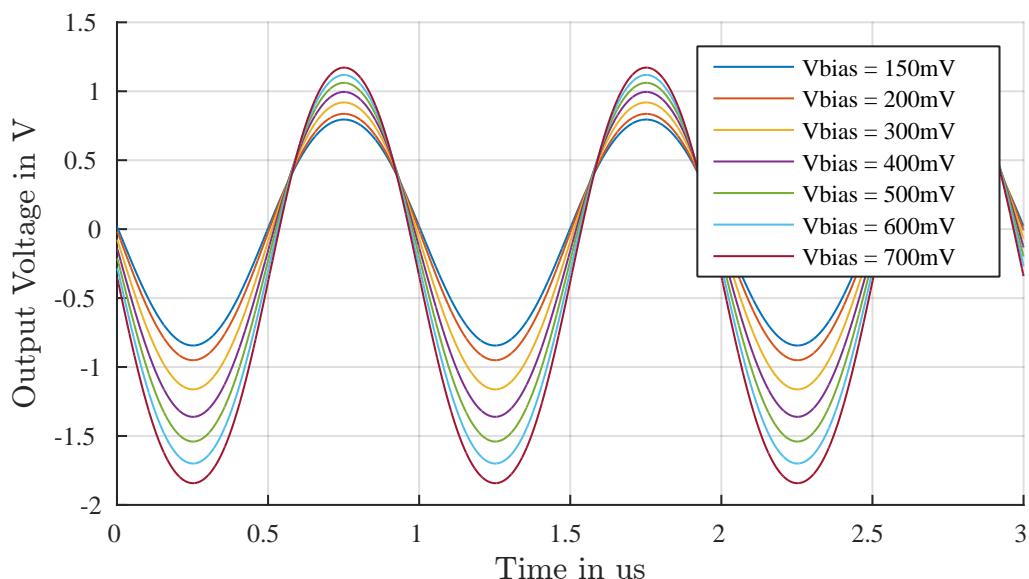


Figure 3.10.: OTA Output Voltage for vs time for different Vbias

Table 3.10 shows the variation of different transient parameters with respect to V_{bias} . The voltage swing varies from 1.639 to 3.014 which is almost in the ratio of 1:2. HD3 worsens with increase in V_{bias} and on the contrary, improves. Although, it is seen that the HD2 again starts to worsen beyond 600mV of V_{bias} .

Vbias (mV)	150	200	300	400	500	600	700
Vout Max (V)	0.7949	0.8362	0.9188	0.995	1.061	1.119	1.172
Vout Min (V)	-0.844	-0.9505	-1.162	-1.361	-1.54	-1.7	-1.842
Vout Swing (V)	1.639	1.787	2.081	2.356	2.601	2.818	3.014
HD2 (dBc)	-44.83	-44.28	-43.86	-44.74	-47.97	-60.86	-48.75
HD3 (dBc)	-52.15	-49.69	-46.13	-43.87	-42.24	-40.78	-39.32

Table 3.10.: Transient Parameters of the OTA

Square Input

The test bench in Figure.(f) is used to measure the transient parameters for a square wave input. Slew rate is the rate of change of output voltage. It is also defined as the ratio of bias current to load capacitance.

$V_{DD} = 2.5V$; $V_{SS} = -2.5V$; $V_{cm} = 1.95V$; $V_{bias} = 150mV$ to $700mV$; $V_{pulse} V_1 = 100mV$; $V_2 = -100mV$; $PulseWidth = 49.7ns$; $Period = 100ns$; $RiseTime = 300ps$; $Falltime = 300ps$; $C_L = 50fF$.

The slew rate, both for the rising edge and the falling edge is tabulated in the Table 3.11. The OTA is reasonably fast enough high V_{bias} voltages.

Vbias (mV)	150	200	300	400	500	600	700
Slew Rate Rising Edge (V/us)	386.9	407.8	452.9	501.9	547.6	585.4	609.3
Slew Rate Falling Edge (V/us)	-389	-413.8	-469.4	-523.5	-570.5	-605.7	-626.4

Table 3.11.: Slew Rate of the OTA

3.3 Summary

Parameter	Programmable Voltage
Linear Input Voltage Range	± 100 mV
Bandwidth	89.19 .. 135 MHz
Slew Rate	$\pm 386.6 .. 609.3$ V/ μ s
Input Referred Noise	33.28 .. 46.64 nV/ \sqrt{Hz} @1MHz
Input Impedance	3.38 .. 3.467 M Ω
Output Impedance	1.262 .. 1.837 K Ω
Output Voltage Swing	1.6389 .. 3.014 V
HD2	-43.86 .. -60.86 dBc
HD3	-39.32 .. -52.15 dBc
Open Loop Voltage Gain	8.548 .. 16.49 V/V
PSRR	234.6 .. 274.9 nA/V

Table 3.12.: Simulation Results of the OTA

Conclusion

The objective of the first stage of the system was to design a programmable operational transconductance amplifier. The OTA was used in voltage mode. Different topologies were considered and the best fit according to the requirements and the complexity was chosen - the conventional current mirror based OTA. The initial design challenge was choosing the topology of the overall system - whether a single stage would be sufficient or a two stage is necessary. With a single stage, the OTA can only drive capacitive loads and for high currents, a large value of load capacitance is necessary and thus reducing the overall bandwidth for the output current. Using the OTA in voltage meant that the output voltage swing variation should be in the ratio of 1:1.8 (Transconductance specification). To achieve this ratio, the range of bias current chosen came down to the effects of DC bias voltage at the output and also the gain of the OTA. Having done all these, the output voltage swing requirement from the first stage was achieved but with a $\pm 100\text{mV}$ linear input voltage range. The operating bandwidth of the system was higher than the required specification so that it makes up for the dominant pole of the second stage.

4 Operational Amplifier

This chapter deals with the design and implementation of an operational amplifier as a second stage. OP AMPS are fundamental building blocks in analog IC design. OP AMPS can work in different configurations like - Adder, Integrator, Differentiator, Buffer. And also in inverting and non-inverting configurations. As part of this work, the OP AMP specifications were obtained from simulations and using those specifications, the OP AMP was designed and tested for all parameters.

4.1 Design and Implementation

With the gain of the first stage sufficiently high enough, the second stage is used just as a buffer. The high impedance output of the operational transconductance amplifier has to be converted to a low impedance output in order to drive a resistive load instead of a pure capacitive load. As a first step, the specifications of the OP AMP have to be decided. We have the results from the first stage OTA and since the output of the OTA is directly provided to the input of the op amp, we can use the OTA to generate the specifications of the op amp. Some of the parameters like the input common mode range and the output voltage swing can be directly obtained by looking at the output of the OTA. But some of the key parameters like the open loop gain, gain bandwidth product, slew rate, etc., need simulations to reach our requirement. The output impedance, the output current range specifications can be directly taken from the system specifications tabulated in Chapter 1.

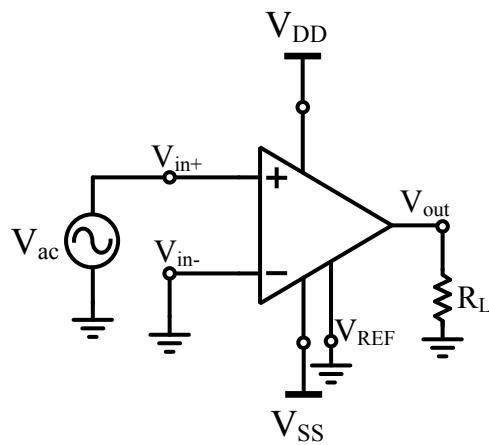


Figure 4.1.: Behavior Modelling of Ideal OP AMP

Cadence Virtuoso offers a few basic libraries and ahdlLib (analog hdl library) is one of them. The ahdlLib offers an ideal op amp which can be used for behavior modelling to sweep gain, unity bandwidth, input impedance, and slew rate. The test setup for this modelling is as shown in Figure 4.1. The V_{REF} reference voltage is typically used to set the DC level of the OP AMP. Generally, the middle voltage between V_{DD} and V_{SS} is the value set for V_{REF} . And in this case, as we have a dual bipolar supply, the V_{REF} is grounded. The other behavioral inputs to these are the open loop gain, unity gain bandwidth, input impedance, output impedance, bias current, slew rate, maximum output current. The open loop gain, unity gain bandwidth,

slew rate are swept over a wide range of values with input impedance a value much higher than the output impedance of the OTA. The bias current is set to zero and the maximum output current is left unset. The OTA designed is cascaded with the ideal OP AMP by connecting the output pin of the OTA to the non-inverting terminal of the ideal OP AMP. The unity gain bandwidth of the OP AMP that provides the overall system bandwidth that matches the specification is is the unity bandwidth with which the OP AMP has to be designed. And likewise, the value of gain that stabilizes the overall system is the open loop gain of the op amp to be designed. Following the steps above, the specifications of the OP AMP to be designed are tabulated below.

Parameter	Value
Open Loop Gain	30 dB
Gain Bandwidth Product	6 MHz
ICMR (min)	-1.85 V
ICMR (max)	1.2 V
Output Voltage Swing	-2 .. 2
Slew Rate	900 V/us
Input Impedance	10 MΩ
Output Impedance	55 KΩ

Table 4.1.: Specifications of the OPAMP to be designed

The two-stage circuit architecture has historically been the most popular approach to op amp design [29]. The main reason for that being it can provides a very high gain and a high output swing. The two stages refer to the number of gain stages in the op amp. An optional output buffer to the op amp can be used as a third stage.

Optimal compensation of op amps are arguably one of the most difficult parts of a design. Two most popular approaches are dominant pole compensation and lead compensation. Compensation capacitor between the output of the gain stages causes pole-splitting and achieves dominant pole compensation. This capacitor is known as Miller capacitor and the op amp is called as a two stage Miller compensation op amp. With the use of this compensation capacitor, the location of the poles can be chosen and thereby the bandwidth of the op amp can be set according to our requirements. This is important because the we need a 6MHz unity gain bandwidth from the OP AMP to meet our requirements and to get a stable enough system.

4.1.1 Schematic

The schematic of the Miller compensation op amp is as shown in the Figure.4.2. The bias current to the differential pair is provided through the current mirror pair of M_5 and M_8 . The bias current is controlled through the transistor M_9 whose gate voltage is provided by the voltage divider formed by the resistors R_{b1} and R_{b2} . The adaptive load for the differential stage is formed by the current mirror pair M_3 and M_4 . The second stage is the common source amplifier formed by the transistors M_6 and M_7 . C_C is the compensation capacitor connected between the output of the two stages of the amplifier [30]. The phase margin can be set by adjusting the value of this capacitor. Smaller the capacitor, higher the phase margin of the op amp. The dimensions of the differential pair are chosen with the help of the graphs generated using the G_m/I_D methodology to obtain the a moderate gain and required unity gain bandwidth. The adaptive load sets the maximum input common mode voltage and M_5 sets the minimum input common mode voltage. The output voltage range is set by the common source amplifier and therefore the open loop gain. M_6 is tweaked to alter the gain of the op amp. Alternatively the gain is also increased by decreasing the bias current. And then in order to maintain the voltage swing, the W/L ratios of some transistors need tuning as well.

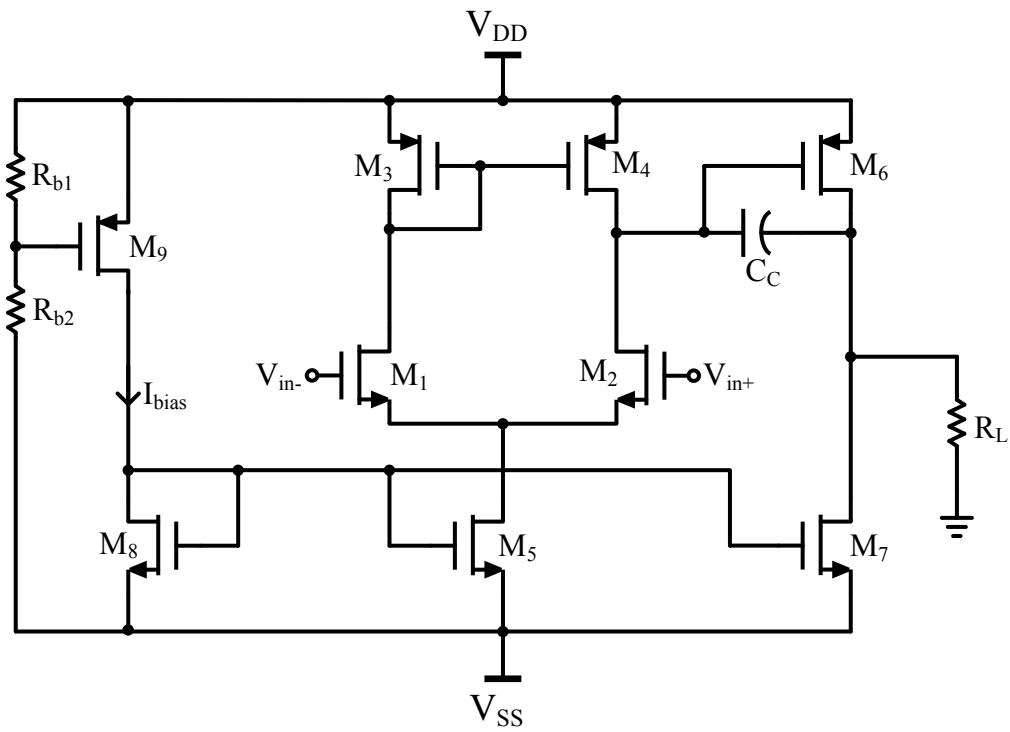


Figure 4.2.: Schematic of the OPAMP Designed

The dimensions of the transistors are tabulated in Table 4.2. One can easily recognize that the transistors at the output are significantly large. This is designed so to make sure the op amp provides a very high current and thereby avoiding a common collector amplifier at the output of the op amp to amplify the output current. The compensation capacitance value is 50fF.

Transistor	Width(μm)	Length(nm)	Multiplier
M1, M2	5	500	2
M3, M4	30	500	1
M5, M8	2	500	1
M6	85	500	55
M7	50	500	48
M9	0.7	500	1

Table 4.2.: Dimensions of the Transistors of the designed OPAMP

4.2 Test Setup

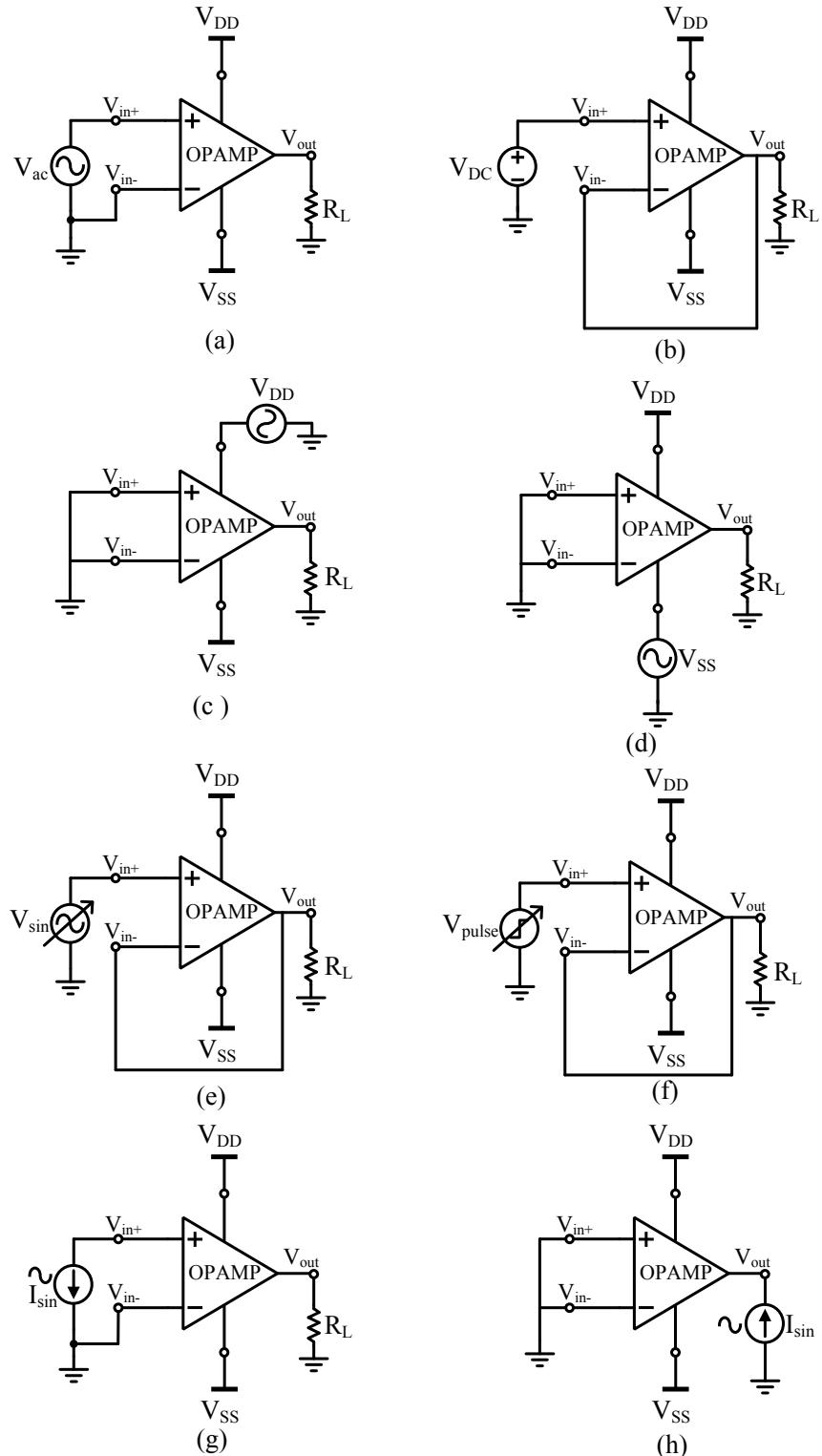


Figure 4.3.: Test bench setup for OP AMP

- (a) Bias, Gain, Bandwidth; (b) ICMR; (c) PSRR(V_{DD}); (d) PSRR(V_{SS}); (e) Transient - Sine; (f) Transient - Square; (g) Input Impedance; (h) Output Impedance

The test bench setup for the operation transconductance amplifier is as shown in Figure.4.3. All the analyses are carried out under a standard temperature of 27_0C , typical mean conditions for the NMOS transistors, PMOS transistors, capacitors and resistors unless explicitly mentioned otherwise. The *ocean* script containing all the expressions to measure the various parameters of the OP AMP are attached in the Appendix. In the following subsections, the results of these parameters are discussed using DC Analysis, AC Analysis, Transient Analysis and Noise Analysis separately.

4.2.1 DC Analysis

The OP AMP is not separately biased. The DC level at the output of the OTA cannot be filtered out using a coupling capacitor as the OTA is already driving a capacitive load. Therefore the common mode voltage of the OP AMP will be the DC output bias of the OTA. Considering that the OP AMP is connected in a buffer configuration, the output of the OP AMP will have the same DC level as the output of the OTA. As part of the DC analysis, the input common mode range and the output voltage swing is calculated. In the test circuit in Figure.4.3(b), the input DC voltage is varied from V_{SS} to V_{DD} and the voltage range in the linear range varies from -2.19V to 2.089V. Similarly the output voltage swing is calculated without the negative feedback and is found to be -2.19V and 2.323V.

$$V_{DD} = 2.5V; V_{SS} = -2.5V; V_{DC} = -2.5V \text{ to } 2.5V; R_L = 50\Omega.$$

Parameter	Value
ICMR (min)	-2.19 V
ICMR (max)	2.089 V
Output Voltage Swing	-2.19 .. 2.323V

Table 4.3.: DC Analysis

4.2.2 AC Analysis

The test bench in Figure.4.3(a),(c),(d),(g) and (h) is used to analyse the small signal parameters of the OP AMP.

Gain and Unity Bandwidth

The test bench used to measure the parameters - gain and unity gain bandwidth is as shown in Figure.4.3(a). The op amp is configured in an open loop. The DC biasing to the differential transistor pair is provided by the output of the OTA, which is centred around 0V.

The plot of the open loop gain and the phase of the op amp is as shown in the Figure.4.4. The open loop gain of the op amp is 30.8dB. The gain bandwidth product is 6.2MHz and correspondingly the phase margin is 76.79^0 .

$$V_{DD} = 2.5V; V_{SS} = -2.5V; V_{ac magnitude} = 1 V; R_L = 50\Omega.$$

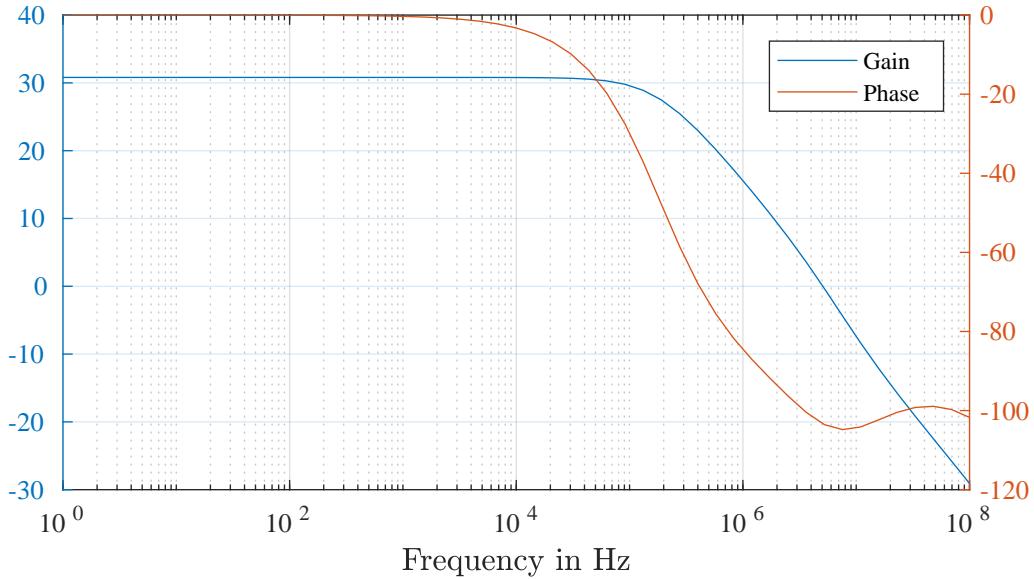


Figure 4.4.: OPAMP Plot of Gain and Phase vs Frequency

Parameter	Value
Open Loop Gain	30.8 dB
Phase Margin	76.79 degrees
Unity Gain Bandwidth	6.2 MHz

Table 4.4.: Gain and Unity Bandwidth of the OP AMP

PSRR

The PSRR of the OTA in the first stage was in the range of nA/V and hence negligible. However, the op amp designed exhibits a relatively high value of PSRR. This is due to the bulky transistors at the output stage. The test bench to measure the PSRR of the op amp is as shown in the Figure 4.3(c) and (d); (c) is used to measure PSRR for a change in V_{DD} and similarly, (d) is used to measure PSRR for a change in V_{SS} .

$V_{DD} = 2.5V$; $V_{SS} = -2.5V$; $V_{ac\ magnitude} = 1 V$; $R_L = 50\Omega$.

Parameter	Value
PSRR(V_{DD})	$30.96 \mu A/V$
PSRR(V_{SS})	$138.8 \mu A/V$

Table 4.5.: PSRR of the OP AMP

Input and Output Impedance

The test bench to calculate the input impedance is shown in 4.3(g). A unity current source is connected to the non-inverting terminal of the op amp and the voltage at that terminal is measured which in turn is the magnitude of the input impedance of the op amp.

To have a stable system, it is important that input impedance of the second stage is higher than the output impedance of the first stage. Given that the output impedance of the OTA is generally high, the input impedance of the op amp becomes a very important parameter. And the input impedance is found to be $9.04M\Omega$.

$$V_{DD} = 2.5V; V_{SS} = -2.5V; I_{sin magnitude} = 1A.$$

Op amps are known to have zero or very low output impedance. Along with this theoretical fact, the op amp in this work is designed to have very high output currents, so it is expected to have a very low output impedance. The test bench to calculate the output impedance is shown in 4.3(h). The value of the output impedance is measured to be 4.167Ω .

4.2.3 Transient Analysis

The test bench to perform the transient analysis is as shown in the Figure 4.3(e). The op amp is connected in a negative feedback configuration so as to analyse its behavior as a voltage buffer.

$$V_{DD} = 2.5V; V_{SS} = -2.5V; V_{sin amplitude} = 1.5V; frequency = 1MHz; R_L = 50\Omega.$$

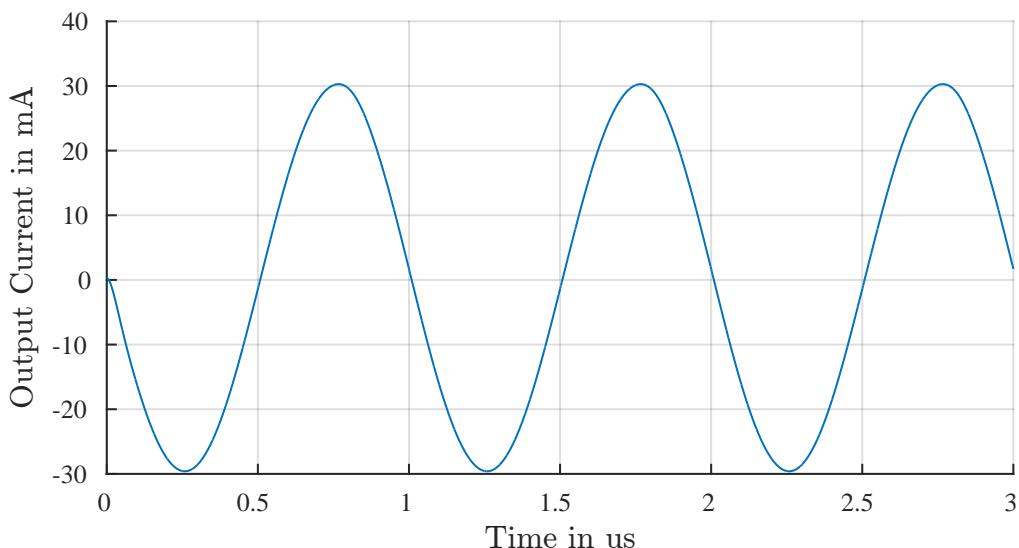


Figure 4.5.: OPAMP Plot of Ourput Current vs time

The output current of the op amp is effectively the current flowing through the load resistor R_L . The plot of current versus time is as shown in the Figure.4.5. The current is 180° out of phase with the voltage and it ranges from -30mA to 30mA for a 50Ω load and 3V peak to peak input voltage.

4.3 Summary

The values of all the parameters of the op amp discussed so far have been tabulated in Table.4.6

Parameter	Value
Open Loop Gain	30.8 dB
Gain Bandwidth Product	6.2 MHz
Phase Margin	76.79
ICMR (min)	-2.19 V
ICMR (max)	2.089 V
Output Current (max)	-29.6 mA
Output Current (min)	30.28 mA
Output Voltage Swing	-2.19 .. 2.323
Slew Rate	10 V/us
PSRR (V_{DD})	30.96 uA/V
PSRR (V_{DD})	138.8 uA/V
Input Impedance	9.04 MOhms
Output Impedance	4.167 Ohms

Table 4.6.: Simulation Results of the OPAMP

Conclusion

The objective of the second stage of the system was to design an operational amplifier. The OP AMP was used in a unity gain configuration. A two stage Miller compensation topology was used to design the OP AMP. The results of the OTA were used to generate the specifications of the OP AMP with the help of the ideal OP AMP from the ahdl library from Cadence. The OP AMP produces a high current at the output stage because of the bulky dimensions of the transistors in common source amplifier. Having such a wide range of ICMR was challenging. The unity gain bandwidth was adjusted using the compensation capacitance at 6MHz. The value of load resistance was set at 50Ω so that it can be driven by a high current.

5 Overall System

With the OTA and OP AMP already designed, the overall system is merely a cascade of the two stages. In this chapter, the architecture of the overall system is presented and the simulations are carried out in a way similar to that of the previous two chapters. Two design approaches are presented for the programmability of the overall system. The first of which, as discussed is with an external voltage, V_{bias} being the programmable variable with a fixed load resistance. And the second design approach with a fixed value of V_{bias} and the programmable variable being the load resistance R_L .

The block diagram of the two stage design with an OTA and an OP AMP is as shown in Figure 5.1. The other end of the capacitor of the first stage is connected to the negative power supply instead of ground since we have only two levels of power supply in the IC (-2.5V and 2.5V). Both the stages use the same power supply. The output of the OTA is directly connected to the non-inverting terminal of the OP AMP without any DC isolation.

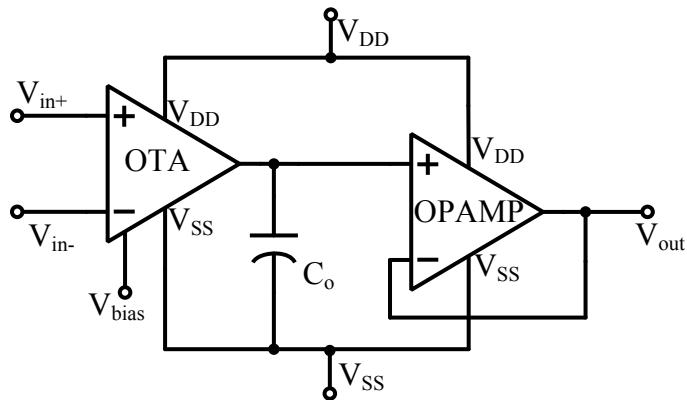


Figure 5.1.: Block Diagram of the Overall System

5.1 Schematic

The transistor level schematic of the overall system is as shown in the Figure 5.2. The upper portion of the schematic is the OTA and the bottom portion is the OP AMP. Note the feedback connection of the OP AMP and the connection between the OTA and the OP AMP.

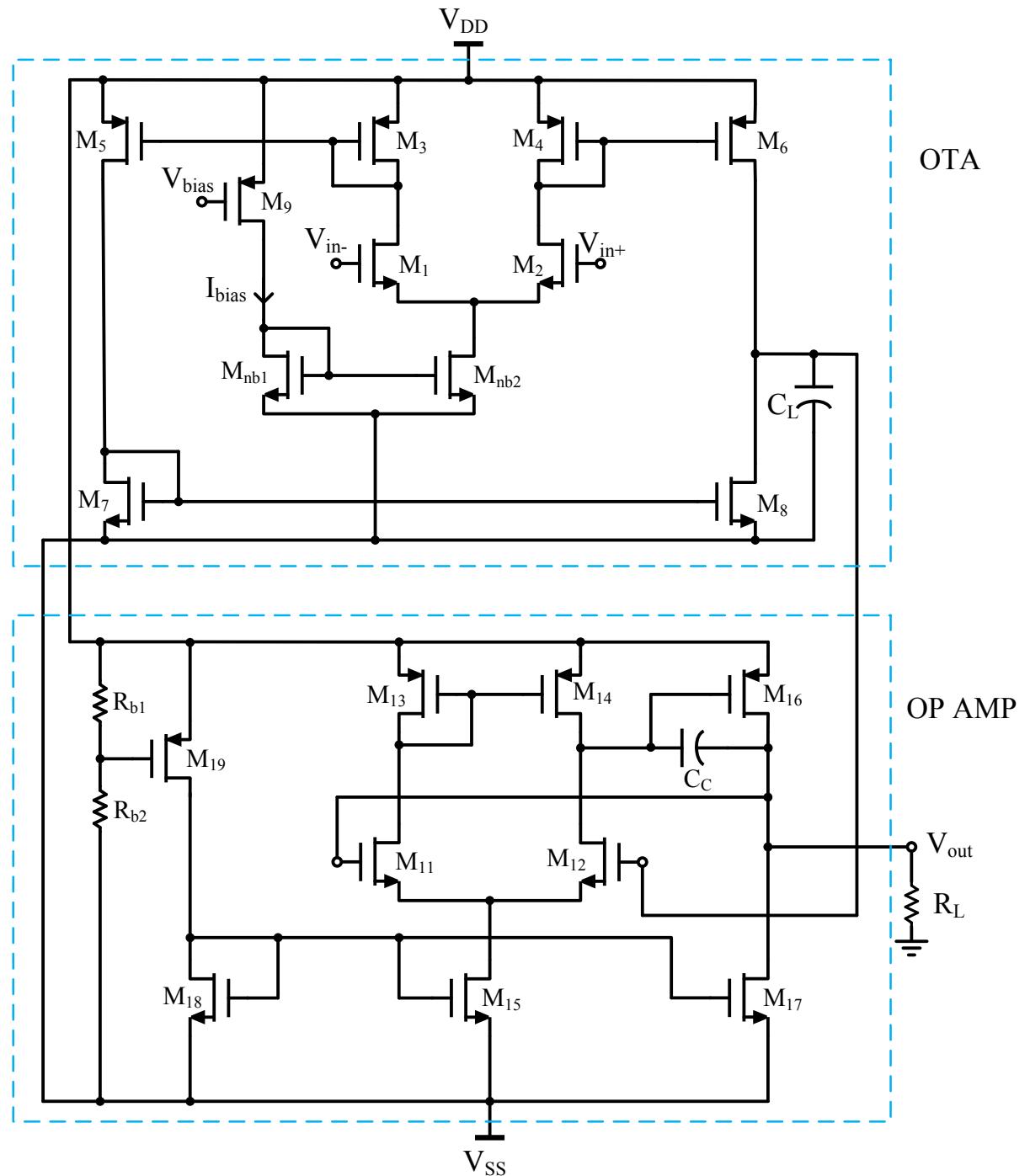


Figure 5.2.: Schematic Diagram for the Overall System

5.2 Test Setup

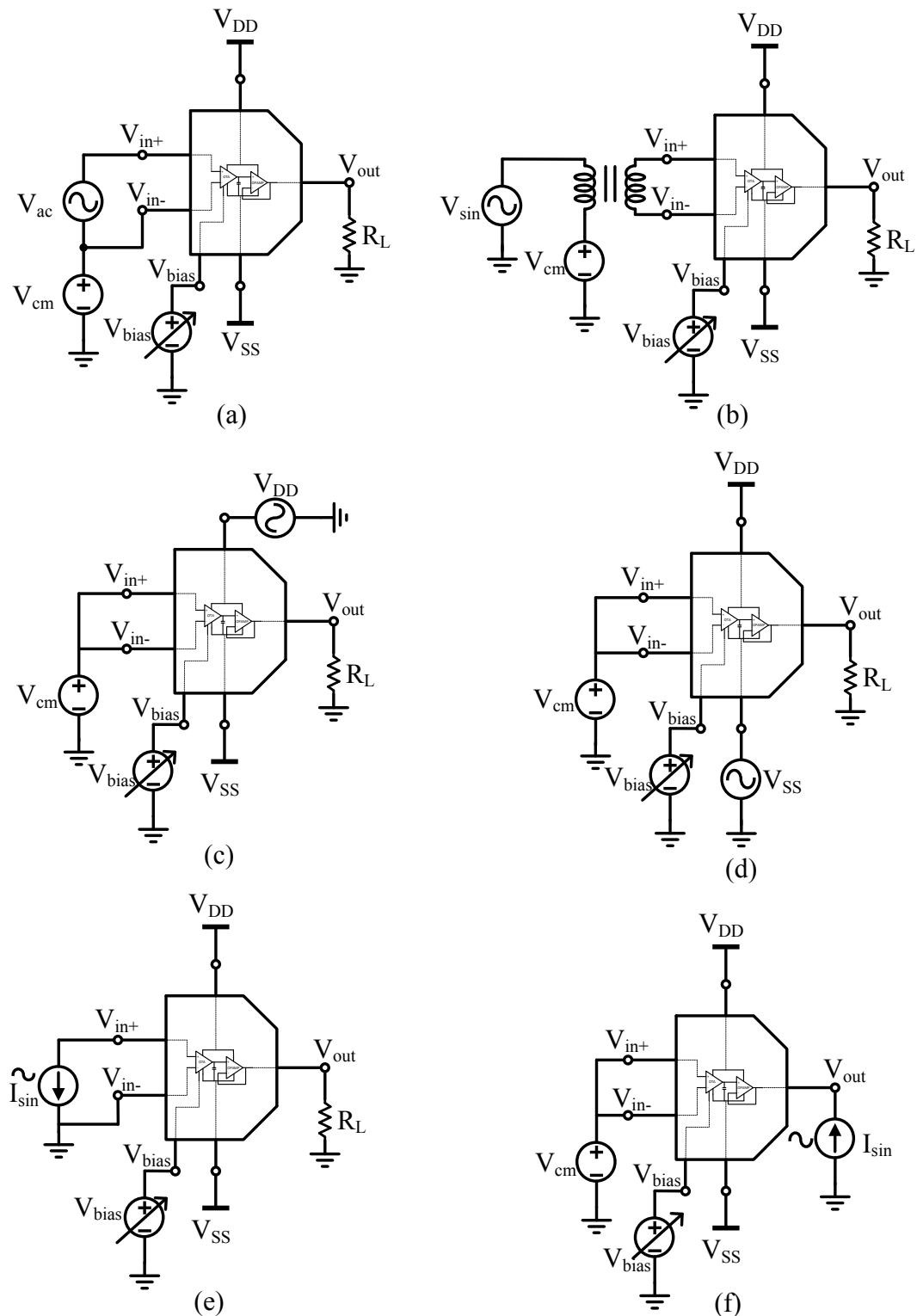


Figure 5.3.: Test setup for DC Analysis

(a) Bias, Gain, Bandwidth, Input Referred Noise; (b) Transient - Sine; (c) PSRR(V_{DD}); (d) PSRR(V_{SS});
 (e) Input Impedance; (f) Output Impedance

The schematic symbol for the overall system is as indicated in Figure.5.4. The block diagram of the system is drawn inside to get an understanding of the configuration.

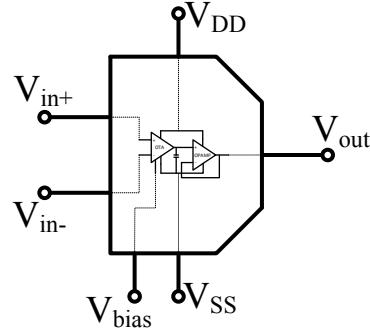


Figure 5.4.: Schematic Symbol for the Overall System

5.2.1 DC Analysis

The test bench to perform the DC analysis is as shown in the Figure.5.3(a).

$$V_{DD} = 2.5V; V_{SS} = -2.5V; V_{cm} = 1.95V; V_{bias} = 150\text{mV to } 700\text{mV}; V_{ac} = 1V; R_L = 50\Omega.$$

The DC Bias point at the output of the system is tabulated in the Table.5.1. Output DC bias points are almost symmetric around 0V and vary from 180.1mV to -219.3mV.

V_{bias} (mV)	Output DC Bias (mV)
150	180.1
200	148.4
250	115.8
300	82.28
350	47.83
400	12.45
450	-23.86
500	-61.08
550	-99.24
600	-138.3
650	-178.4
700	-219.3

Table 5.1.: DC Bias Point at the output of the circuit

5.2.2 AC Analysis

The test bench in Figure.3.7(a),(c),(d),(e) and (f) is used to analyse the small signal parameters of the OTA.

Gain and Bandwidth

The test bench in Figure.5.3(a) is used to measure the gain and operating bandwidth of the system. The magnitude of the AC source is set to 1V and as mentioned in the previous chapter, the voltage at the output will be the gain of the overall system.

The plot of gain for different values of V_{bias} is as shown in the Figure.5.5. The value of the open loop gain is between 18dB and 25dB.

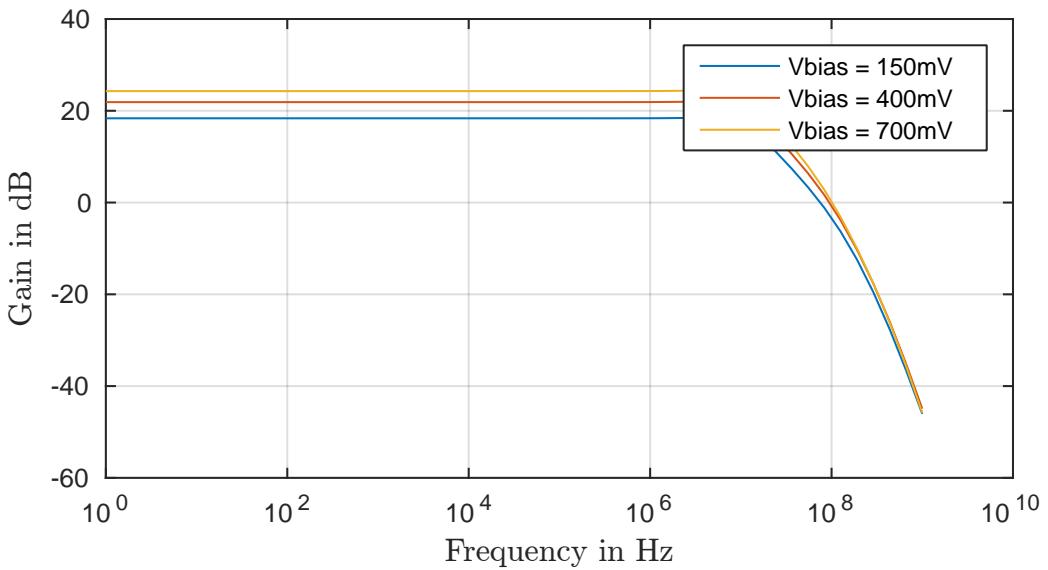


Figure 5.5.: Plot of Gain vs Frequency for different V_{bias}

V_{bias} (mV)	DC Gain (dB)	Bandwidth (MHz)	Phase Margin
150	18.5	14.43	55.49
200	19.34	14.38	51.37
250	20.13	14.34	47.76
300	20.83	14.29	45.08
350	21.46	14.24	42.55
400	22.02	14.19	40.19
450	22.52	14.14	38
500	22.97	14.08	35.97
550	23.38	14.01	34.08
600	23.75	13.95	32.31
650	24.1	13.88	30.63
700	24.43	13.8	29.02

Table 5.2.: DC Gain, Bandwidth and Phase Margin of the Overall System

The results of the AC analysis are tabulated in Table.5.2. The bandwidth is fairly constant at around 14MHz. But the phase margin starting to drop just a tad below 30 with a V_{bias} of 700mV and beyond.

Input Impedance

The test bench in Figure.5.3(e) is used to measure the input impedance of the system. The concept for measurement is same as in the case of the OTA. The voltage at the non-inverting terminal will be the magnitude of the input impedance of the overall system because the magnitude of the current from the AC source is 1A.

$$V_{DD} = 2.5V; V_{SS} = -2.5V; V_{bias} = 150\text{mV to } 700\text{mV}; I_{sin magnitude} = 1\text{A}; R_L = 50\Omega.$$

The value of input impedance with respect to V_{bias} is tabulated in Table.5.3. It is clear that the input impedance of the overall system is same as the input impedance of the OTA in the first stage.

V_{bias} (mV)	Input Impedance ($M\Omega$)
150	3.394
200	3.402
250	3.41
300	3.418
350	3.425
400	3.433
450	3.44
500	3.448
550	3.456
600	3.464
650	3.473
700	3.482

Table 5.3.: Input Impedance of the Overall System

Output Impedance

On the same lines, the test bench for measuring the output impedance is as shown in the Figure.5.3(f). The resistive load is replaced by a current source which tries to pull out 1A of current from the circuit and thereby the voltage at the output turning out to be the magnitude of the output impedance of the system.

$$V_{DD} = 2.5V; V_{SS} = -2.5V; V_{cm} = 1.95V; V_{bias} = 150\text{mV to } 700\text{mV}; I_{sin magnitude} = 1\text{A}.$$

The value of the output impedance is very low because of the output buffer and there is a small variation of output impedance with change in V_{bias} and is tabulated in Table.5.4. The values are between 0.94Ω and 1Ω .

V_{bias} (mV)	Output Impedance (Ω)
150	0.9415
200	0.9434
250	0.9453
300	0.9474
350	0.9495
400	0.9517
450	0.9541
500	0.9565
550	0.9591
600	0.9618
650	0.9646
700	0.9675

Table 5.4.: Output Impedance of the Overall System

PSRR

The next important parameter is the Power Supply Rejection Ratio. It was seen in the previous chapter that the PSRR of the second stage is much more significant than the first stage. Figure.5.3(c) and (d) shows the test bench used to measure the PSRR for V_{DD} and V_{SS} respectively.

$$V_{DD} = 2.5V; V_{SS} = -2.5V; V_{cm} = 1.95V; V_{bias} = 150\text{mV to } 700\text{mV}; V_{ac\text{magnitude}} = 1V; R_L = 50\Omega.$$

The variation of PSRR against V_{bias} is tabulated below in Table.5.5. PSRR is high for high bias currents or low values of V_{bias} and it decreases with increase in V_{bias} . PSRR is generally expressed in terms of dB. But from the specifications, it is seen that the parameter has to be expressed in uA/V as part of this work.

V_{bias} (mV)	PSRR (VDD)(uA/V)	PSRR (VSS)(uA/V)
150	97.76	93.69
200	89.66	85.77
250	82.86	79.11
300	77.26	73.59
350	72.68	69.04
400	68.93	65.28
450	65.84	62.18
500	63.27	59.53
550	61.1	57.26
600	59.22	55.28
650	57.59	53.52
700	56.13	51.92

Table 5.5.: PSRR of the Overall System

5.2.3 Transient Analysis

The transient analysis is divided in to two parts. The first part involves simulation with a sine wave input and the second part involves simulation with a square wave input.

Sine Wave

The test bench for transient analysis with a sine wave input for the system is as shown in Figure.5.3(b).

$V_{DD} = 2.5V$; $V_{SS} = -2.5V$; $V_{cm} = 1.95V$; V_{bias} = 150mV to 700mV; $V_{sin amplitude} = 100mV$; $R_L = 50\Omega$.

The plot of output current against time for different values of V_{bias} is as shown in the Figure.5.6. The peaks are not symmetric around zero, however it is made sure that the peak-to-peak current values range from 30mA to 60mA.

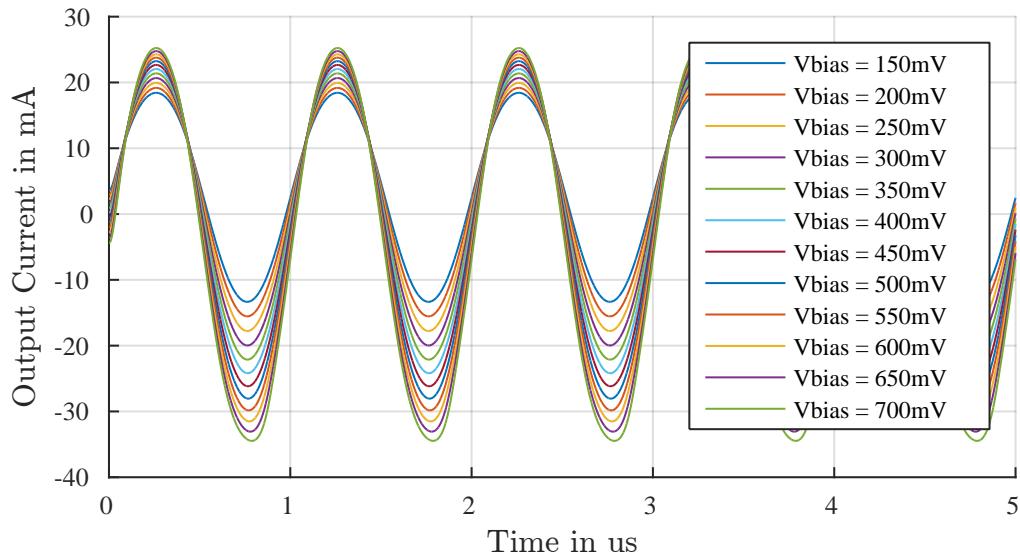


Figure 5.6.: Plot of Output Current vs time for different V_{bias}

V_{bias} (mV)	Iout Max(mA)	Iout Min(mA)	Iout p2p(mA)	HD2 (dBc)	HD3 (dBc)
150	18.43	-13.34	31.77	-37.14	-48.17
200	19.17	-15.55	34.72	-36.62	-45.67
250	19.93	-17.77	37.7	-35.65	-43.65
300	20.67	-19.97	40.64	-35.15	-42.07
350	21.38	-22.12	43.49	-34.84	-40.83
400	22.04	-24.19	46.23	-34.72	-39.85
450	22.66	-26.17	48.83	-34.8	-39.01
500	23.24	-28.05	51.29	-35.08	-38.24
550	23.77	-29.83	53.6	-35.54	-37.42
600	24.28	-31.51	55.79	-36.13	-36.47
650	24.76	-33.07	57.83	-36.61	-35.24
700	25.24	-34.47	59.71	-36.44	-33.61

Table 5.6.: Transient Parameters of the Overall System

Table.5.6 gives a better picture of the sinusoidal plots shown above. The HD2 and HD3 values are less than 30 dBc. However, the HD3 seems to take a turn towards the worse with increase in V_{bias} . So for V_{bias} values beyond 700mV, the output starts clipping at the trough of the current wave.

Once the peak-to-peak value of current is obtained, we can use that to calculate the transconductance of the system for different V_{bias} values. Since the output current is not symmetric around 0A, the the value half of peak-to-peak current is considered. That divided by the input voltage (100mV peak) would give us the required transconductance value. Figure.5.7 shows the plot of transconductance against V_{bias} .

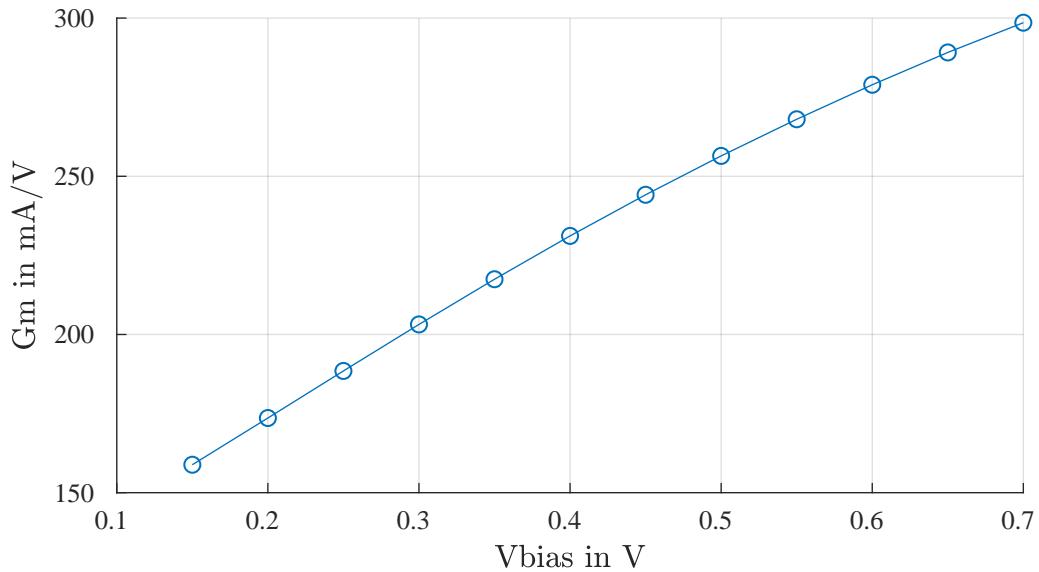


Figure 5.7.: Plot of G_m vs V_{bias}

V_{bias} (mV)	Transconductance (mA/V)
150	158.8
200	173.6
250	188.5
300	203.2
350	217.5
400	231.2
450	244.2
500	256.4
550	268
600	278.9
650	289.1
700	298.5

Table 5.7.: Transconductance Gain of the Overall System

The transconductance value for each V_{bias} used to plot the Figure.5.7 is tabulated in Table.5.7.

Square Wave

The second part of the transient analysis is performed with a square wave input. The slew rate for the rising edge and the falling edge is tabulated in the Table 5.8. The slew rate suffers due to the fact that the OP AMP designed exhibits a very low slew rate.

V_{bias} (mV)	Slew Rate (Rising Edge)(V/us)	Slew Rate (Falling Edge)(V/us)
150	6.985	-8.73
200	7.505	-9.779
250	8.042	-10.68
300	8.581	-11.34
350	9.095	-11.66
400	9.561	-11.7
450	9.954	-11.6
500	10.27	-11.45
550	10.49	-11.3
600	10.65	-11.14
650	10.76	-10.99
700	10.82	-10.84

Table 5.8.: Slew Rate of the Overall System

5.2.4 Noise Analysis

The test bench to perform the noise analysis is same as the test bench used for AC analysis in Figure..5.3(a). The input referred noise of the first stage is far more significant for the overall system than the second stage.

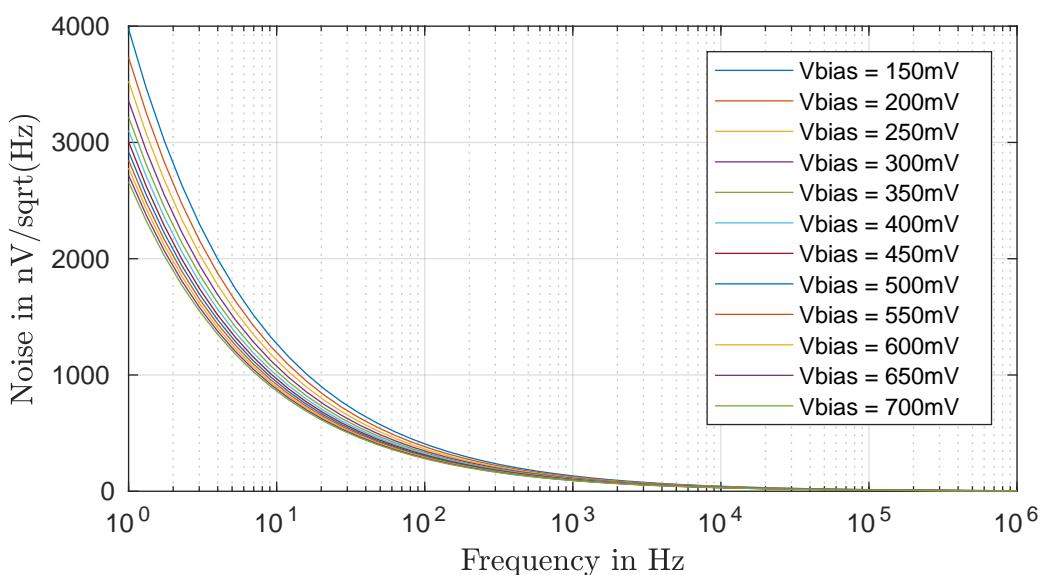


Figure 5.8.: Plot of Input Referred Noise vs Frequency for different V_{bias}

The Bode plot of the input referred noise for different values of V_{bias} is shown in the Figure.5.8. It is clear that the type of noise is 1/f noise or the Flicker noise. The magnitude of the input referred noise is very high for low frequencies and it reduces significantly in moderate and high frequencies when White noise starts to dominate. The value of input referred noise at 1MHz for different V_{bias} is tabulated in the Table.5.9.

V_{bias} (mV)	Input Referred Noise (nV/sqrt(Hz))
150	46.64
200	43.93
250	41.71
300	39.91
350	38.46
400	37.29
450	36.33
500	35.52
550	34.82
600	34.21
650	33.66
700	33.16

Table 5.9.: Input Referred Noise of the Overall System

5.3 Programmable Load

Another way to make the overall system programmable is to have a programmable load. Having a Resistive load that varies would imply that the current flowing through the load is controlled. So, for the following analyses, the V_{bias} is made constant and set a value of 425mV.

Table.5.10 shows the variation of DC Gain, bandwidth, phase margin and transconductance with varying load. The gain hardly changes with the changing load. The variation in bandwidth is just 1.8MHz between the minimum and maximum load. The transconductance however, shows variation in a range that is expected.

RL (Ω)	DC Gain(dB)	Bandwidth(MHz)	Phase Margin	Transconductance(mA/V)
35	22.2	13.13	40.97	338.9
40	22.22	13.55	40.22	296.8
45	22.25	13.88	39.6	264
50	22.28	14.16	39.08	237.7
55	22.3	14.4	38.63	216.2
60	22.32	14.6	38.24	198.3
65	22.34	14.77	37.9	183.1
70	22.35	14.92	37.6	170

Table 5.10.: AC Parameters of the Overall System for a programmable load - 1

Table.5.11 shows the tabulation of values for the parameters that are independent of the variation in load resistance.

Parameter	Value
Input Impedance $M(\Omega)$	3.436
Output Impedance (Ω)	0.953
PSRR (VDD)(uA/V)	67.32
PSRR (VSS)(uA/V)	63.65
Input Referred Noise (nV/ \sqrt{Hz})	36.79

Table 5.11.: AC Parameters of the Overall System for a programmable load - 2

The transient analysis of the system with a programmable load shows a clear picture of how effective the system is. Since the bias voltage or the bias current doesn't change, the DC bias point at the output of the system remains unchanged. Therefore, we get a symmetrical waveform around 0A. The plot in Figure.5.9 shows the output current plot for different values of load resistance.

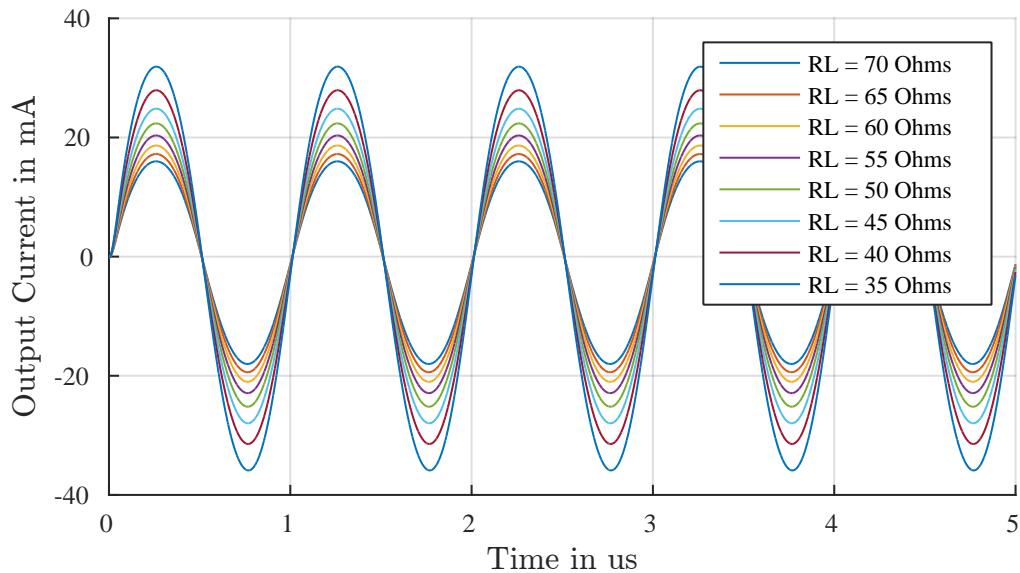


Figure 5.9.: Plot of Output Current vs Time for different RL

RL (Ω)	Iout(max)(mA)	Iout(min)(mA)	Iout(p2p)(mA)
35	31.89	-35.89	67.77
40	27.92	-31.44	59.36
45	24.83	-27.97	52.8
50	22.36	-25.19	47.55
55	20.33	-22.91	43.24
60	18.65	-21.01	39.65
65	17.22	-19.4	36.61
70	15.99	-18.02	34.01

Table 5.12.: Maximum and Minimum Output Currents for a programmable load

Table.5.12 contains tabulation from the plot in Figure.5.9. Output current is the most significant parameter that gets affected by a variable load.

Parameter	Value
HD2 (dBc)	-34.6
HD3 (dBc)	-39.4
Slew Rate (Rising Edge)(V/us)	10.28
Slew Rate (Falling Edge)(V/us)	-10.45

Table 5.13.: Transient Parameters of the Overall System for a programmable load

Table.5.13 shows the values of the parameters that are constant with a varying load. HD2 and HD3 are less than -30dBc. The plot of transconductance versus the load resistance is shown in Figure.5.10

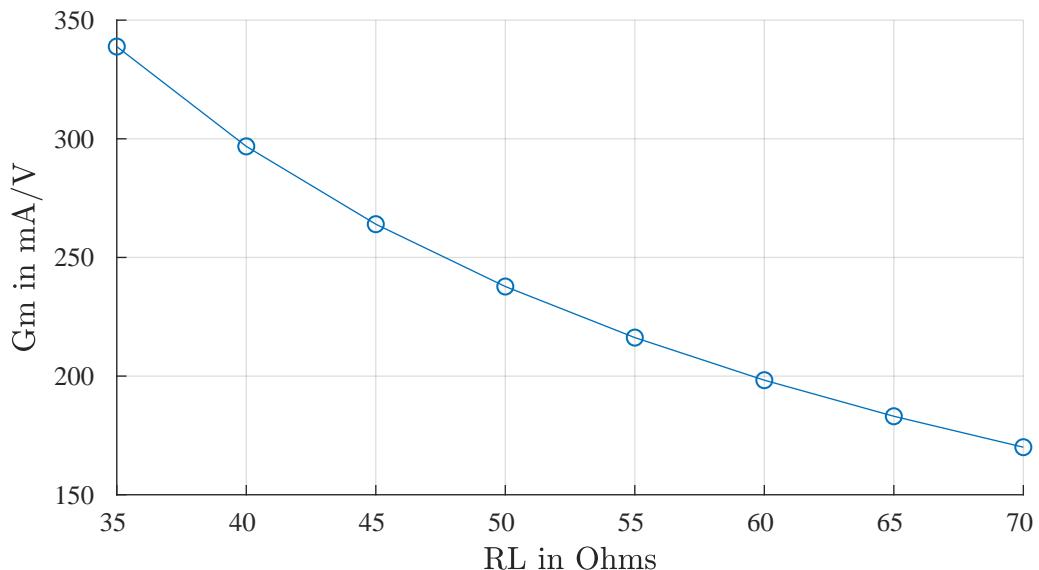


Figure 5.10.: Plot of Transconductance vs RL

5.4 Summary of Results

Parameter	Programmable Voltage	Programmable Resistor
Transconductance Gain(Gm)	158.8 .. 298.5 mA/V	170 .. 338.9 mA/V
Linear Input Voltage Range	± 100 mV	± 100 mV
Output Current Range	+18 mA .. -13 mA	+15 mA .. -18 mA
Bandwidth	13.8 MHz	13.13 MHz
Slew Rate	± 10.82 V/ μ s	± 10.28 V/ μ s
Rise/Fall time	22.7 ns	23.5 ns
Input Referred Noise	46.64 nV/ \sqrt{Hz} @1MHz	36.79 nV/ \sqrt{Hz} @1MHz
Input Impedance	3.394 M Ω	3.436 M Ω
Output Impedance	0.9415 Ω	0.953 Ω
HD2	-34.72 dBc	-34.6 dBc
HD3	-33.61 dBc	-39.4 dBc
Open Loop Voltage Gain	8.41 V/V	12.9 V/V
PSRR	97.76 μ A/V	67.32 μ A/V

Table 5.14.: Summary of Results

Conclusion

The overall architecture of the system and two design approaches were presented as part of this chapter. An external voltage to the OTA in the first stage controls the output current of the OP AMP and the variation of all other parameters with respect to V_{bias} was discussed. And similarly, the variation with respect to a programmable load was also discussed and presented. The stability of the system tends to deteriorate for the first case when V_{bias} is at its highest value. Both design approaches were successful in achieving the high current and bandwidth as required. The slew rate of the system is slow due to the OP AMP. The output impedance of the system is low owing to the high current at the final stage.

6 Corner Simulations

Corner analysis is performed to simulate the circuit's performance against a set of parameters belonging to extreme manufacturing variations. Corner simulations are performed to verify that the circuit works at all possible conditions of process, supply voltage and temperature. Analog circuit designs that perform sufficiently well across these corners are to be considered a robust design.

6.1 Process Variation

Process variation is the naturally occurring variation in the attributes of transistors (length, widths, oxide thickness) when ICs are fabricated. In general there are 5 corners - tt, ff, ss, fs, sf. Transistors can be typical, fast or slow. The first letter indicates the PMOS and the second letter indicates the NMOS. However, as part of XT018 technology, the corners are termed as - tm, wp, ws, wo, wz. The meaning and their translation to the general conventions are described in Table 6.1. The process corners of Capacitors and Resistors too follow a similar naming convention but with only 3 corners - tm (typical), wp(minimum), ws(maximum).

Corner	Expansion	Translation
tm	Typical Mean Condition	tt
wp	Worst Case Power Condition	ff
ws	Worst Case Speed Condition	ss
wo	Worst Case One Condition	fs
wz	Worst Case Zero Condition	sf

Table 6.1.: Different Corners for MOS Transistors in XT018 Technology

A total of 45 corners are simulated for 2 values of V_{bias} - 150mV and 700mV. The results are presented in the subsequent sections.

Lowest V_{bias}

At the lowest V_{bias} , the mean values of all parameters satisfy the requirement. In the worst corner, the positive peak of the current goes below 10mA but the negative peak is still under -15mA. So the current swing is decreased.

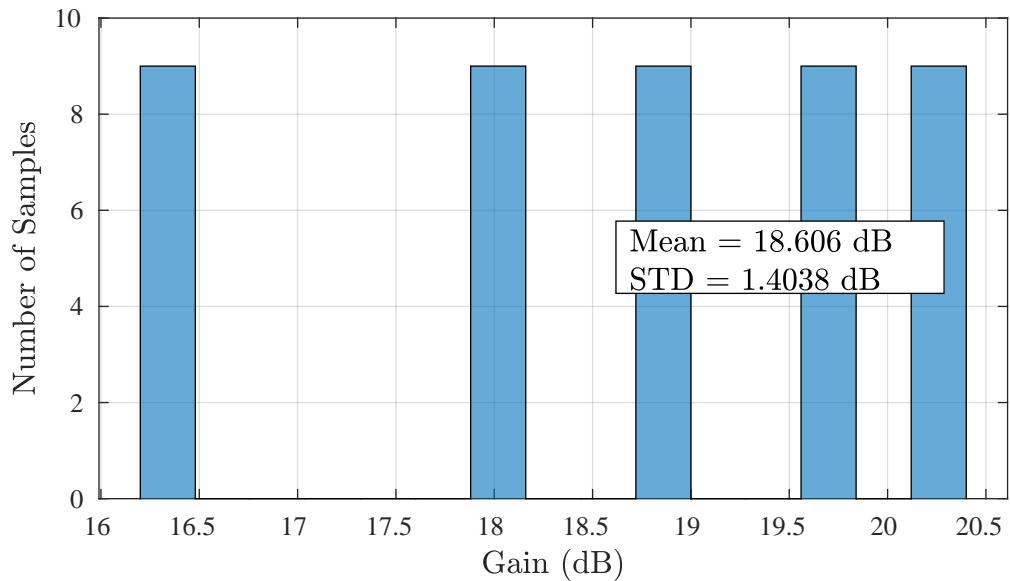


Figure 6.1.: Histogram of System Gain due to Process Variation at $V_{bias}=150\text{mV}$

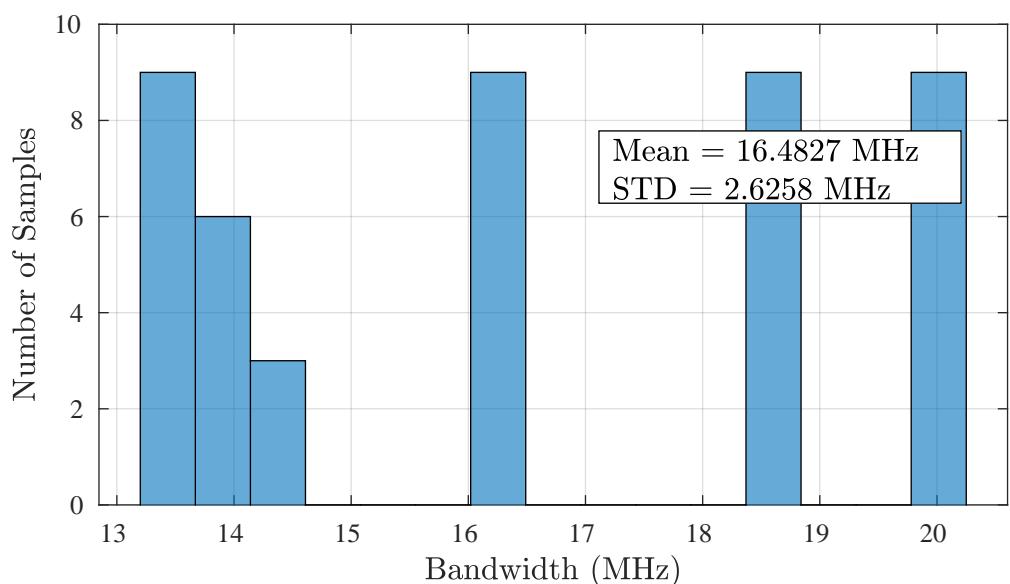


Figure 6.2.: Histogram of System Bandwidth due to Process Variation at $V_{bias}=150\text{mV}$

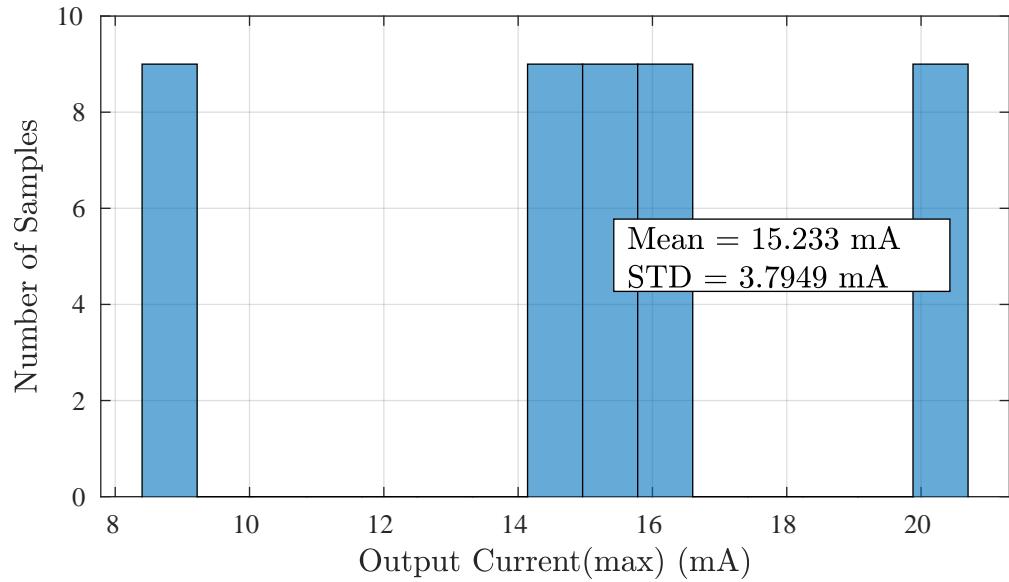


Figure 6.3.: Histogram of Maximum Output Current due to Process Variation at $V_{bias}=150\text{mV}$

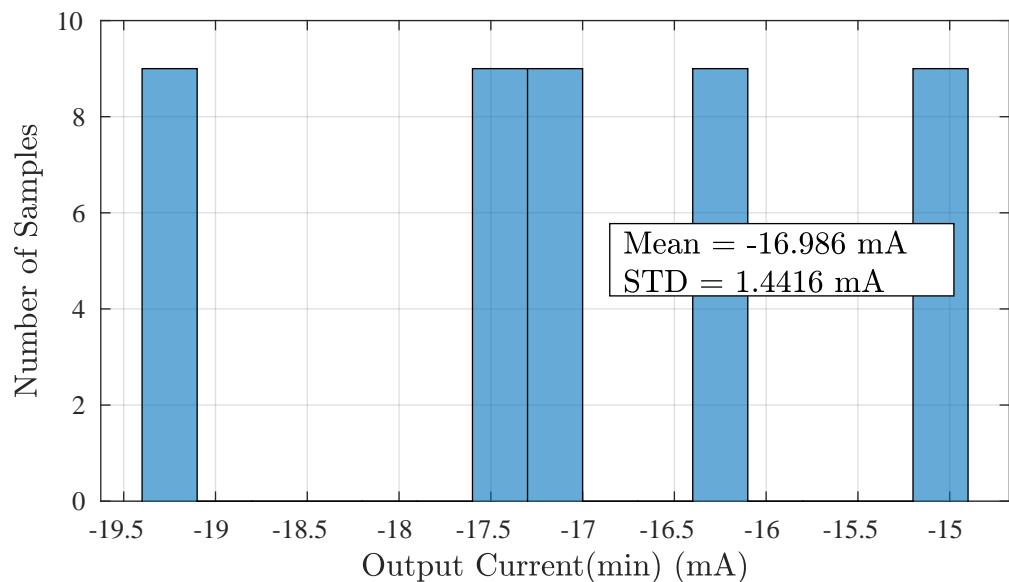


Figure 6.4.: Histogram of Minimum Output Current due to Process Variation at $V_{bias}=150\text{mV}$

Highest V_{bias}

At the highest V_{bias} , the mean values of the parameters meet the requirements. At the worst corner, the positive peak of the output current slips to 20mA but the peak to peak current is still under the requirement. Since the spread is smaller for all parameters, none of them fail to meet the requirements.

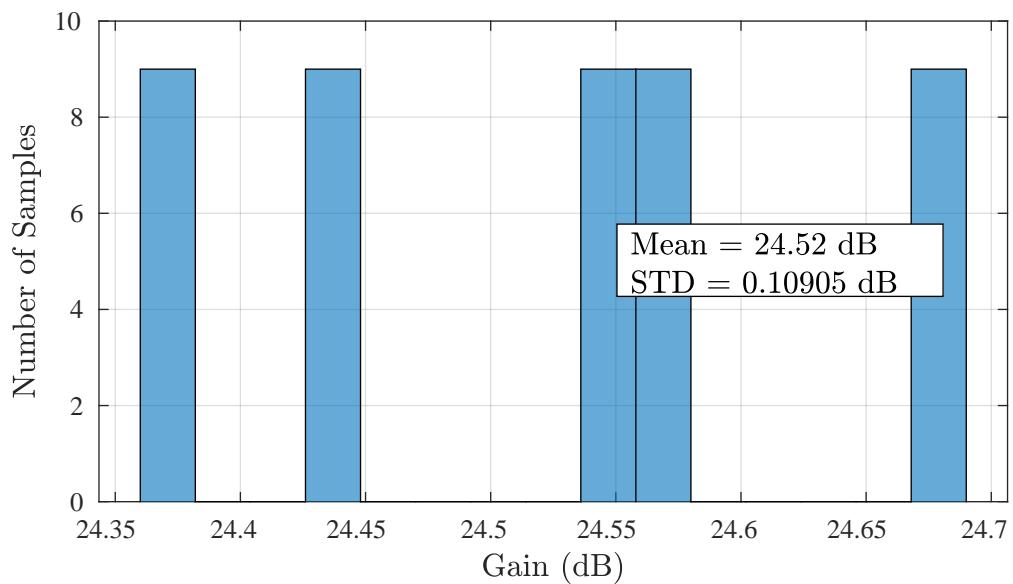


Figure 6.5.: Histogram of System Gain due to Process Variation at $V_{bias}=700\text{mV}$

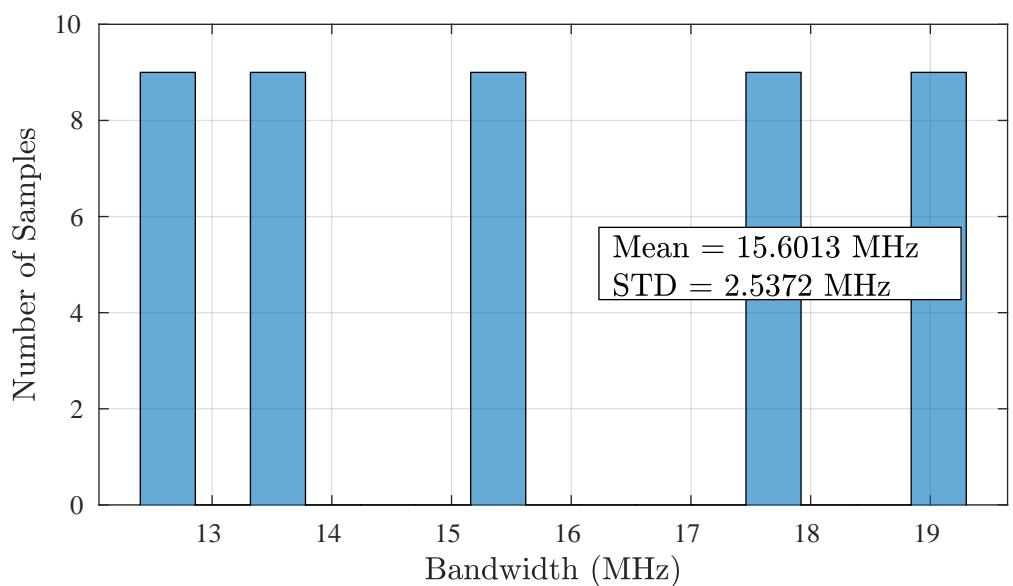


Figure 6.6.: Histogram of System Bandwidth due to Process Variation at $V_{bias}=700\text{mV}$

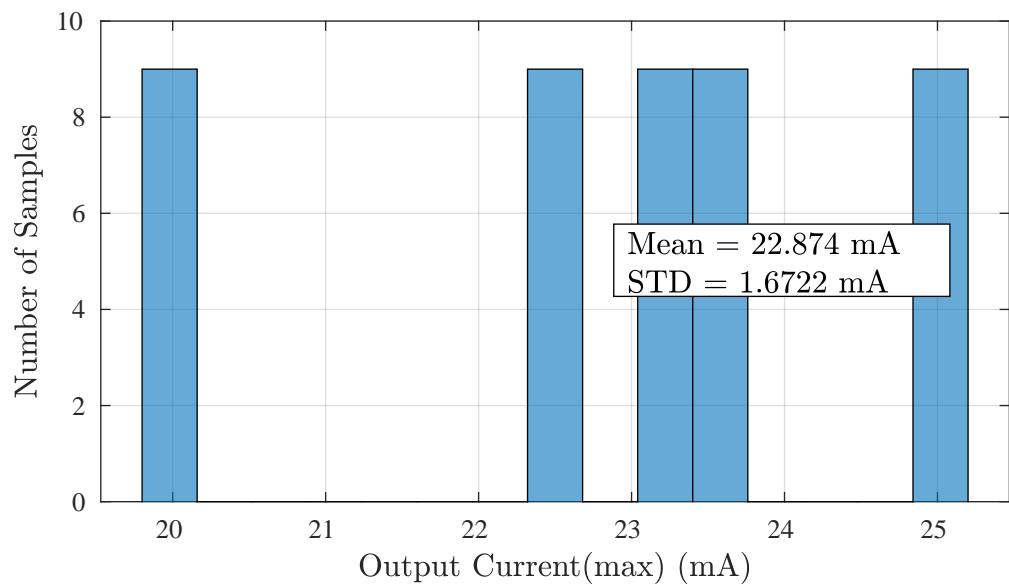


Figure 6.7.: Histogram of Maximum Output Current due to Process Variation at $V_{bias}=700\text{mV}$

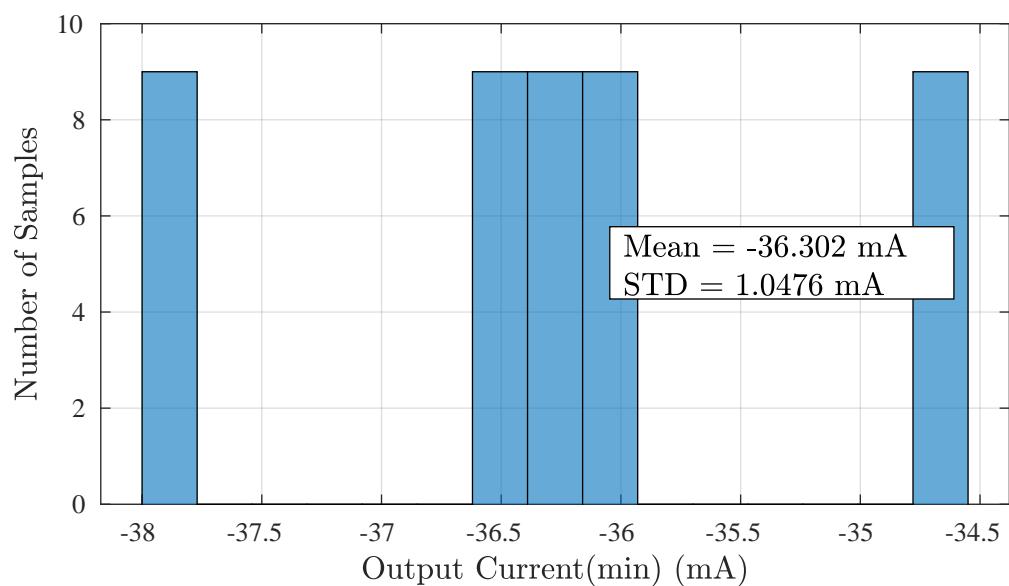


Figure 6.8.: Histogram of Minimum Output Current due to Process Variation at $V_{bias}=700\text{mV}$

6.2 Process and Supply Variation

In addition to process variation, the system responds to power supply variations too. 3 different corners are obtained by evaluating the power supply with $\pm 10\%$ from the nominal value. Therefore, we get 3 corners for V_{DD} - 2.5V, 2.25V, 2.75V and 3 corners for V_{SS} - -2.5V, -2.25V, -2.75V. The total number of corners in this case are 405. And the results are discussed in the subsequent sections.

Lowest V_{bias}

Additional variation in power supply increases the spread in the histogram with samples for gain at 12dB and as high as 21dB. The mean values of all parameters are well within their specified range. But the positive peak output current value drops to a negative value for the worst case. The negative output current for the same case is at -10mA which makes the peak to peak current of 9mA, which is little far from what is required.

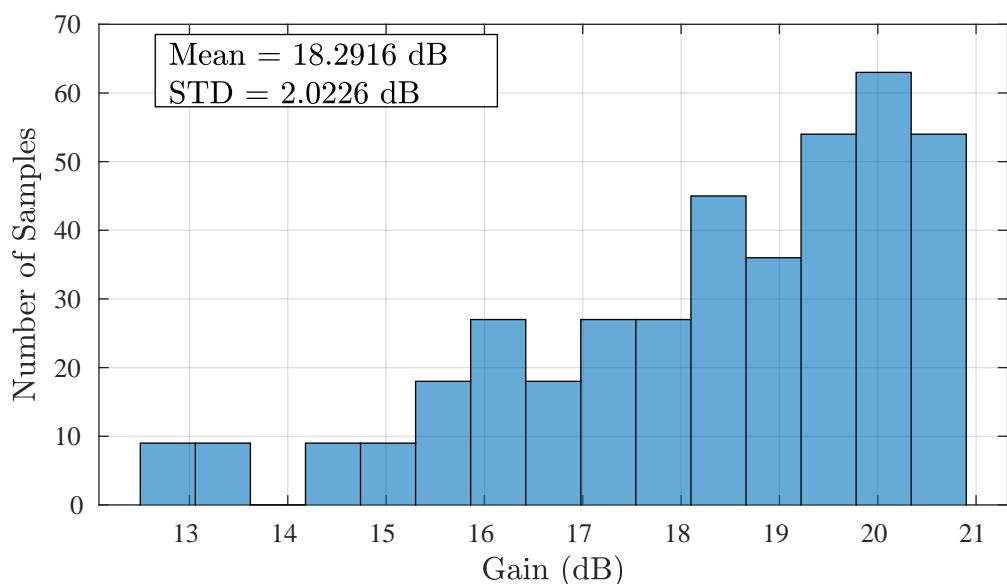


Figure 6.9.: Histogram of System Gain due to Process and Supply Variation at $V_{bias}=150\text{mV}$

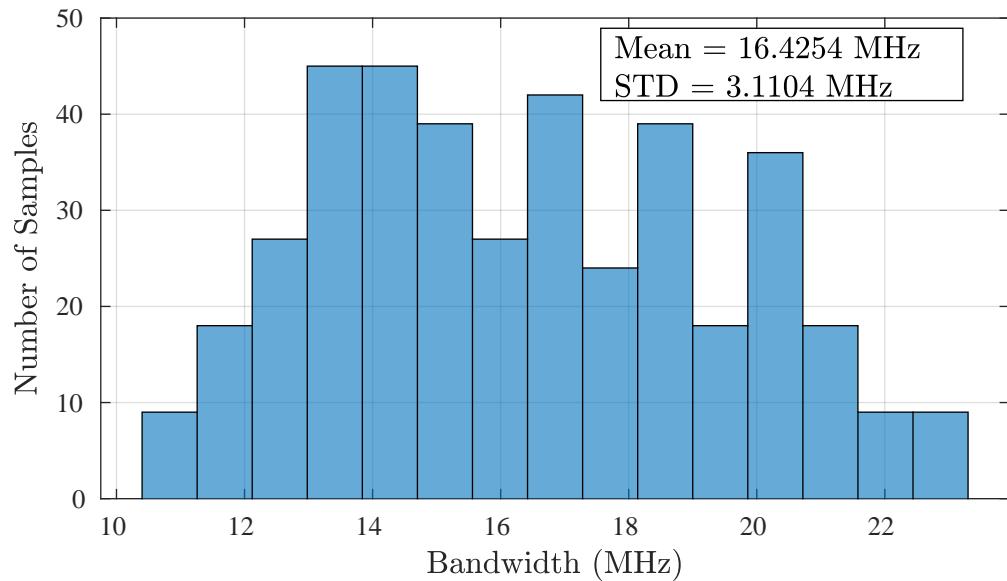


Figure 6.10.: Histogram of System Bandwidth due to Process and Supply Variation at $V_{bias}=150\text{mV}$

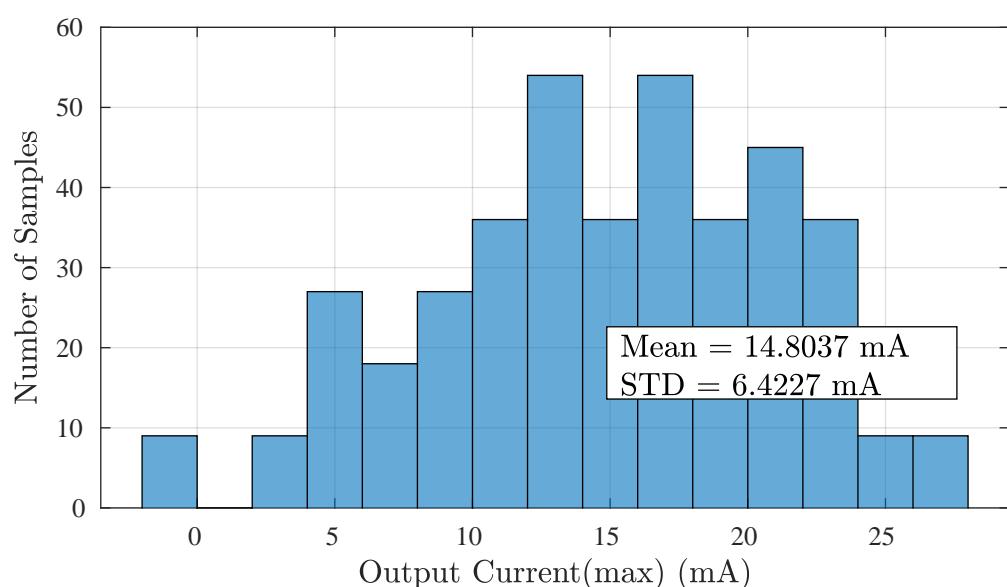


Figure 6.11.: Histogram of Maximum Output Current due to Process and Supply Variation at $V_{bias}=150\text{mV}$

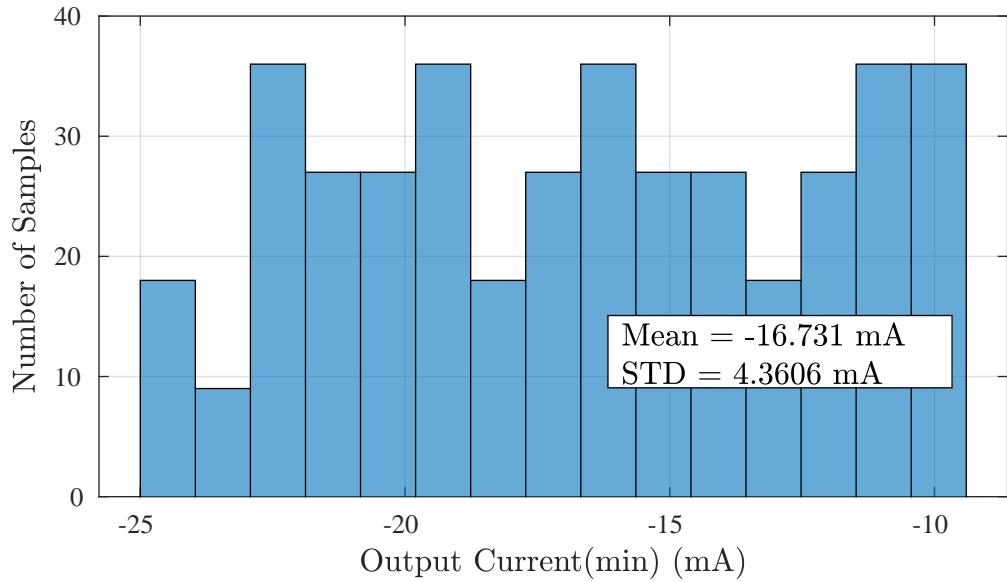


Figure 6.12.: Histogram of Minimum Output Current due to Process and Supply Variation at $V_{bias}=150mV$

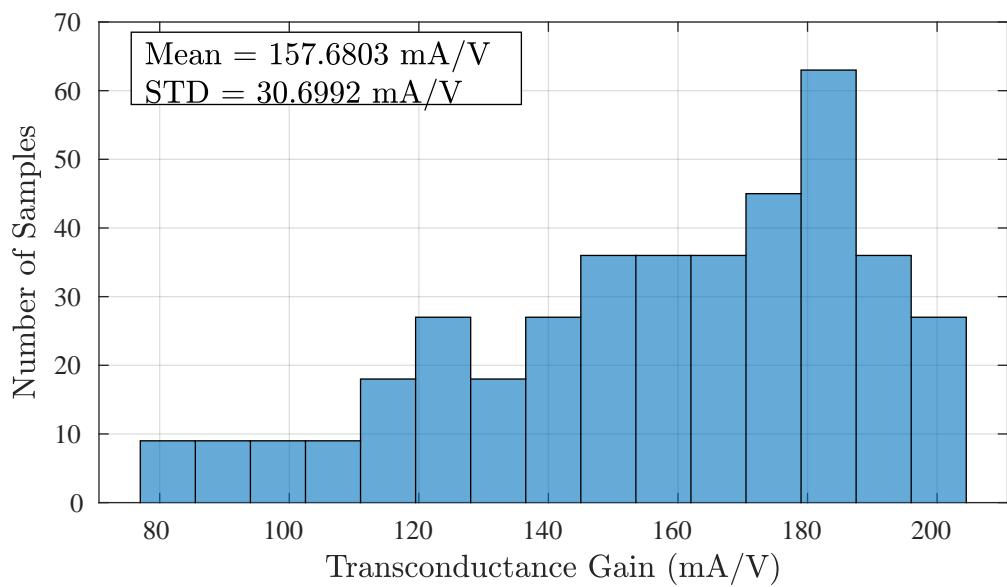


Figure 6.13.: Histogram of Transconductance due to Process and Supply Variation at $V_{bias}=150mV$

Highest V_{bias}

The spread is wide for the bandwidth but even in the worst corner, the bandwidth is above 10MHz and the mean value being 15MHz. The spread for the gain is comparatively smaller with the mean value being

24.5dB and the standard deviation of 0.62dB. The slow corners are once again the worst case corners with the positive current peak dropping 16mA from a mean value of 22mA.

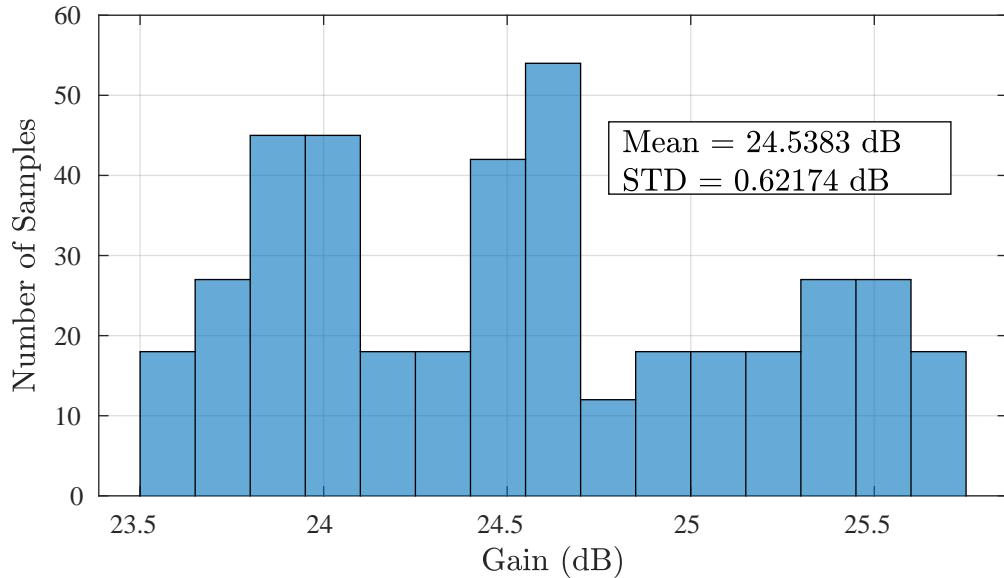


Figure 6.14.: Histogram of System Gain due to Process and Supply Variation at $V_{bias}=700\text{mV}$

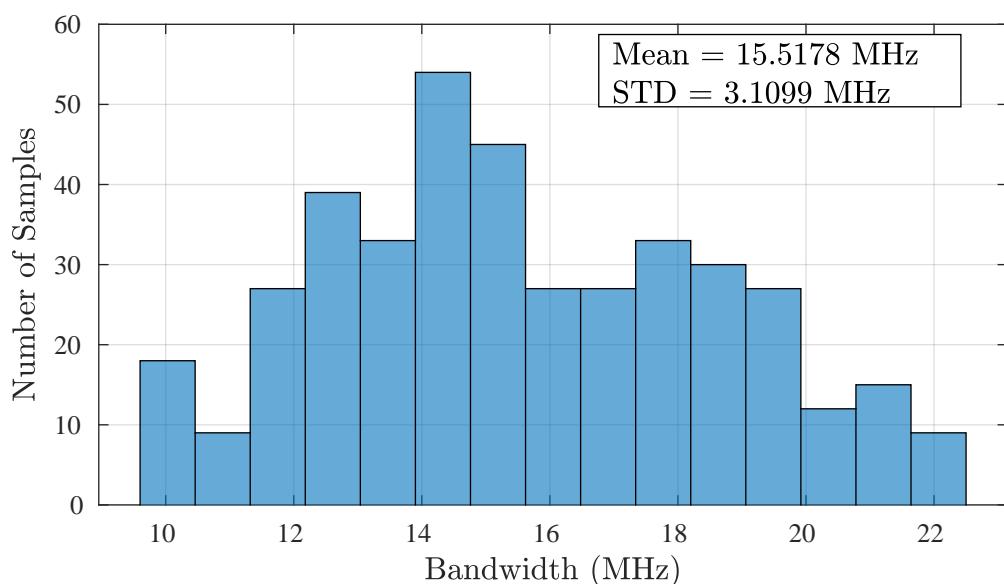


Figure 6.15.: Histogram of System Bandwidth due to Process and Supply Variation at $V_{bias}=700\text{mV}$

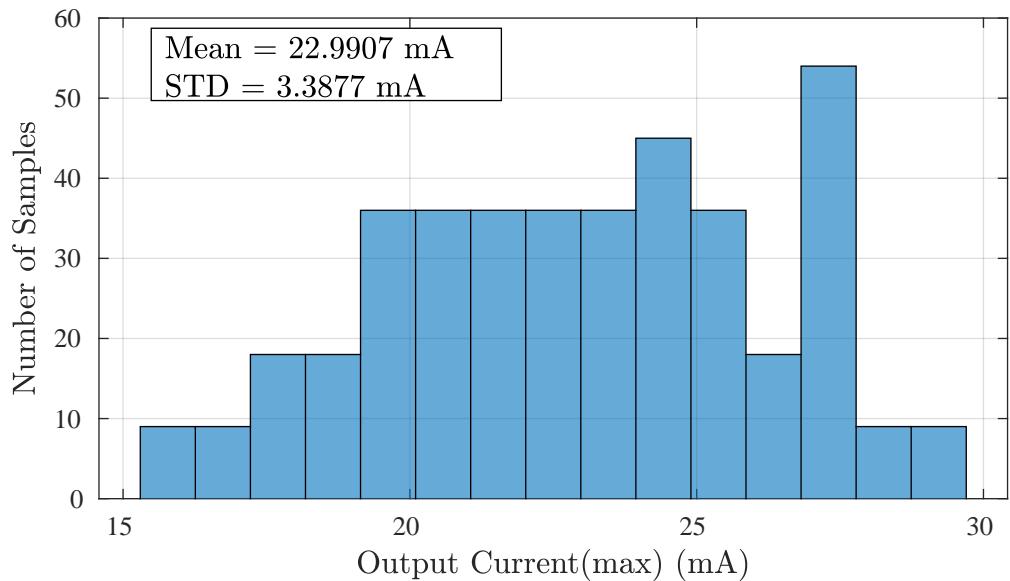


Figure 6.16.: Histogram of Maximum Output Current due to Process and Supply Variation at $V_{bias}=700\text{mV}$

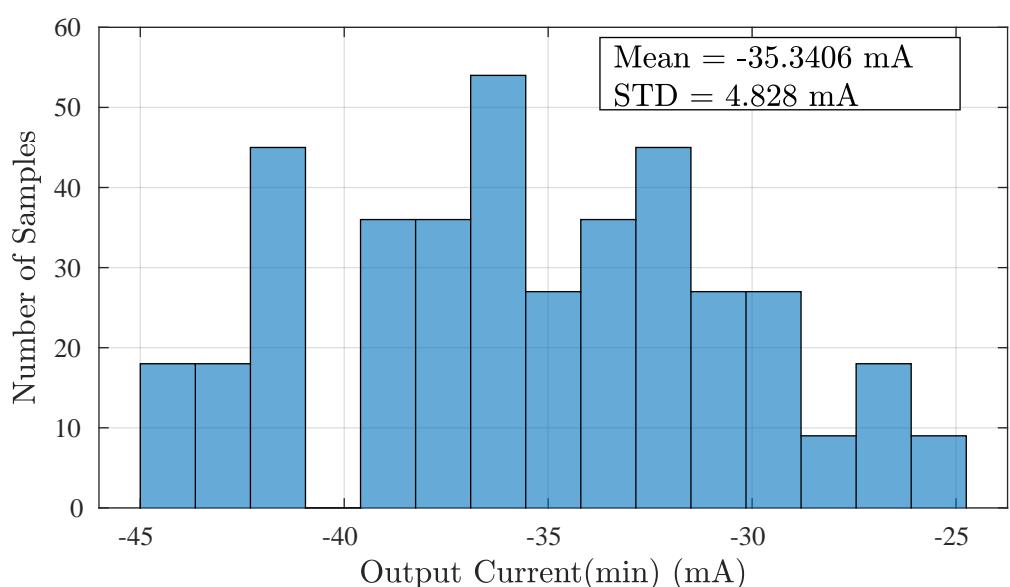


Figure 6.17.: Histogram of Minimum Output Current due to Process and Supply Variation at $V_{bias}=700\text{mV}$

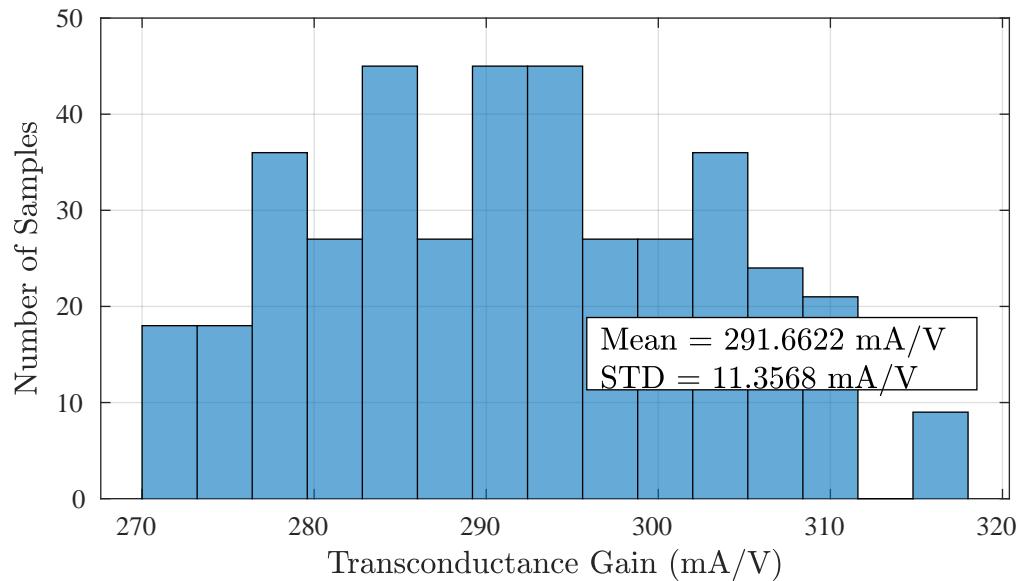


Figure 6.18.: Histogram of Transconductance due to Process and Supply Variation at $V_{bias}=700\text{mV}$

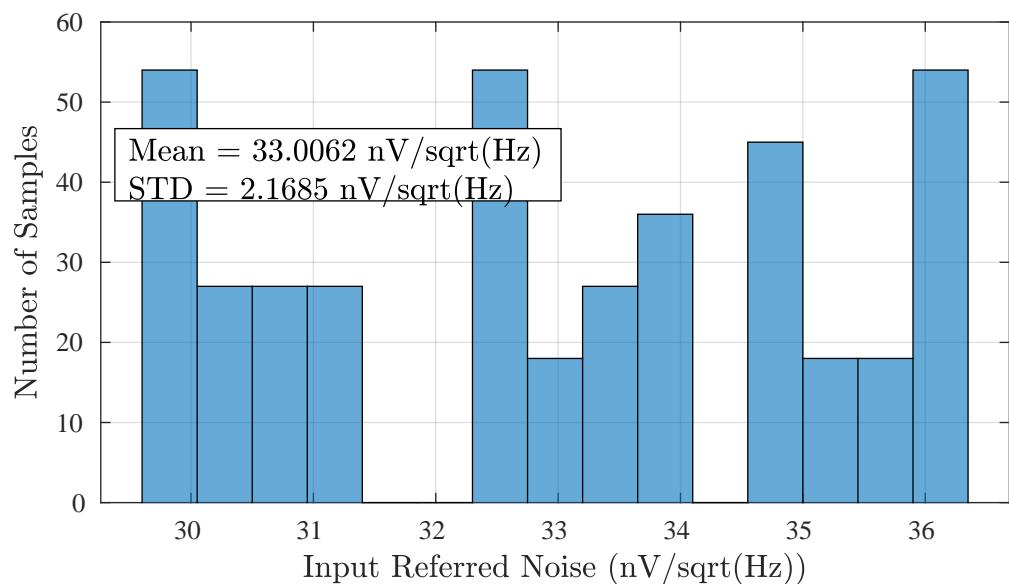


Figure 6.19.: Histogram of Input Referred Noise due to Process and Supply Variation at $V_{bias}=400\text{mV}$

6.3 Process, Voltage and Temperature (PVT) variation

Another possible variation is seen in the temperature parameter. The PVT corner simulations are performed at the following corners:

- All Process corners mentioned in Section 4.6.1.
- $\pm 10\%$ variations of V_{DD} i.e., 2.5V, 2.25V, 2.75V and V_{SS} i.e., -2.5V, -2.25V, -2.75V.
- Three temperature conditions: -25^0C , 25^0C and 80^0C .

Therefore, there are 1215 corners in total. The results are provided in the subsequent sections.

Lowest V_{bias}

With all the variations included, it is observed that the worst case is caused by the supply variations and the temperature variation has lower effect than the supply variation. The worst case corners are still affected by the voltage but with normal spread. The mean gain is 18.3dB with a standard deviation of 2.1dB. The bandwidth too has a wide spread like the gain histogram and at the worst case, it falls just a tad below 10MHz with the mean and standard deviation being 16MHz and 4MHz respectively. The HD2 and HD3 values are less than -30dBc even for worst cases. The PSRR however, at worst case, goes to a value beyond $160\mu\text{A/V}$

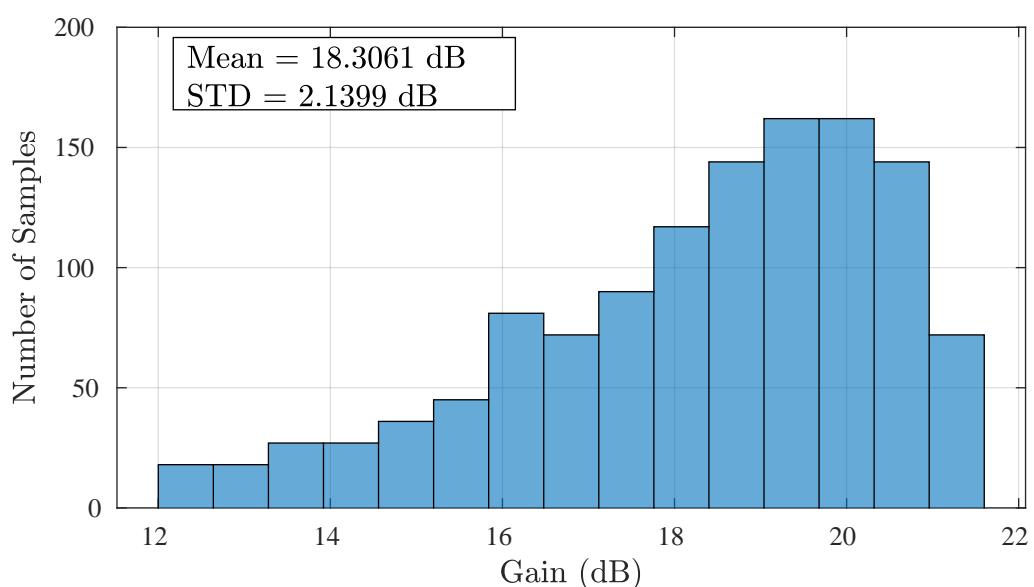


Figure 6.20.: Histogram of System Gain due to PVT Variation at $V_{bias}=150\text{mV}$

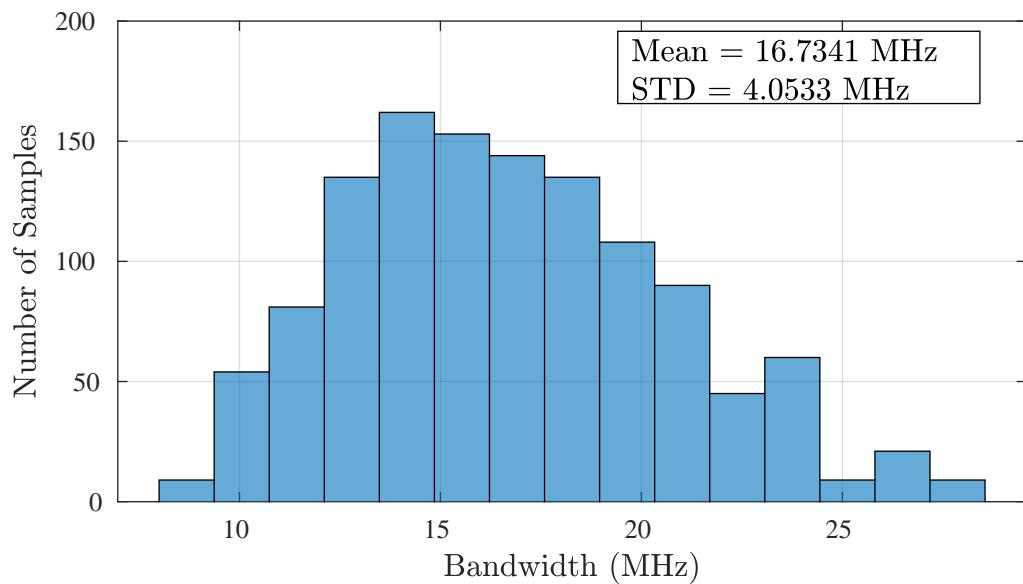


Figure 6.21.: Histogram of System Bandwidth due to PVT Variation at $V_{bias}=150\text{mV}$

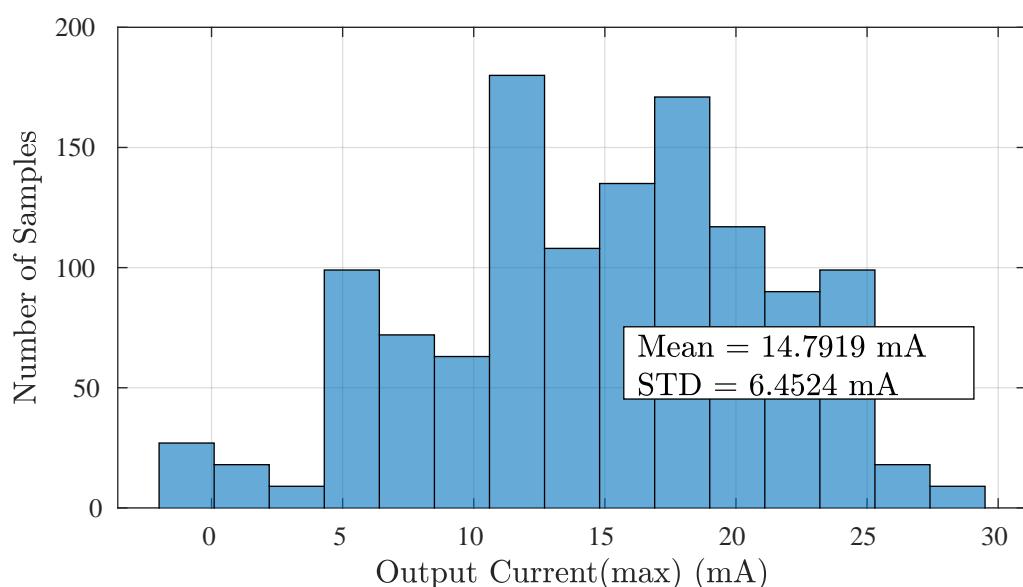


Figure 6.22.: Histogram of Maximum Output Current due to PVT Variation at $V_{bias}=150\text{mV}$

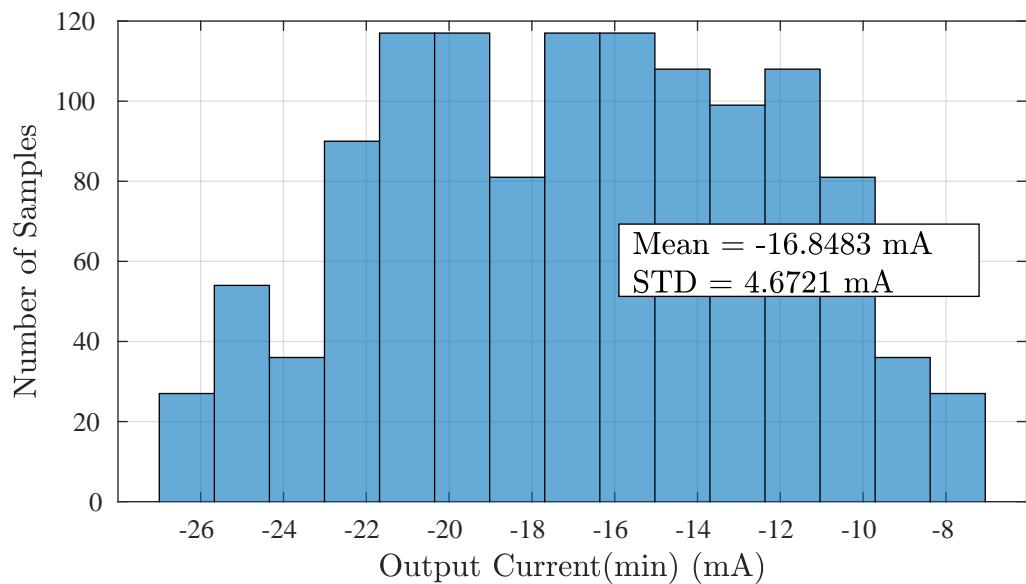


Figure 6.23.: Histogram of Minimum Output Current due to PVT Variation at $V_{bias}=150\text{mV}$

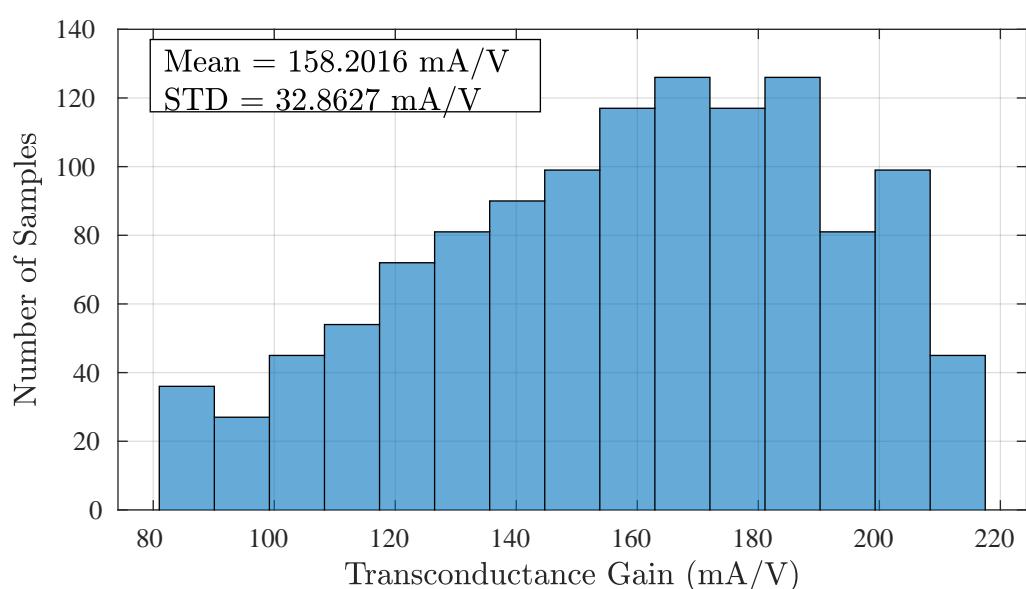


Figure 6.24.: Histogram of Transconductance due to PVT Variation at $V_{bias}=150\text{mV}$

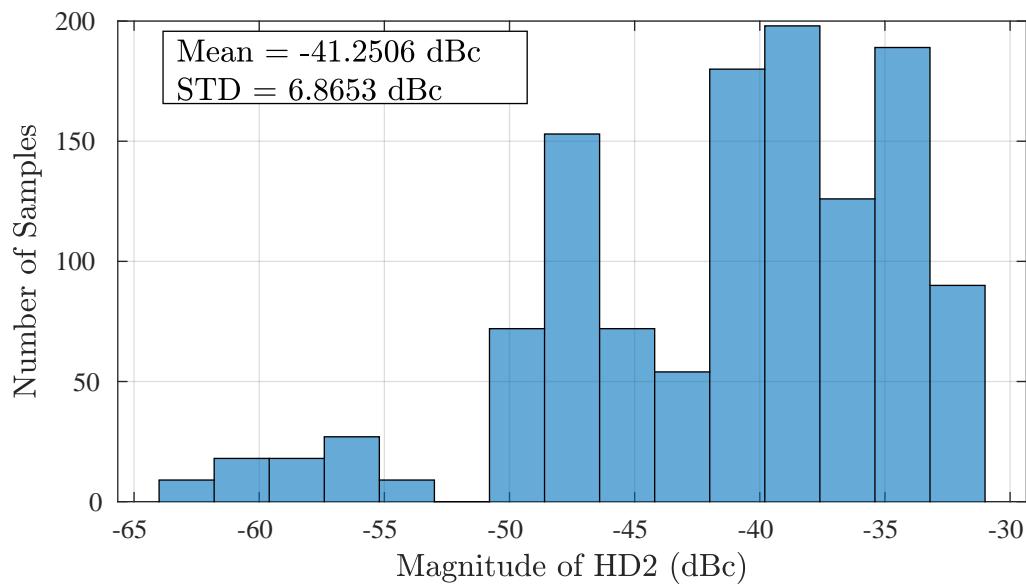


Figure 6.25.: Histogram of HD2 due to PVT Variation at $V_{bias}=150\text{mV}$

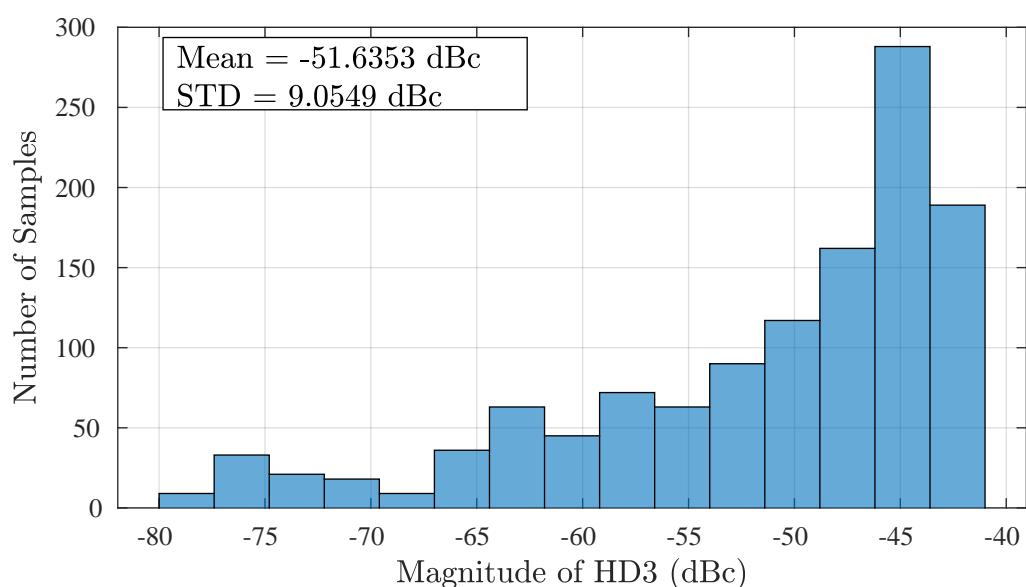


Figure 6.26.: Histogram of HD3 due to PVT at $V_{bias}=150\text{mV}$

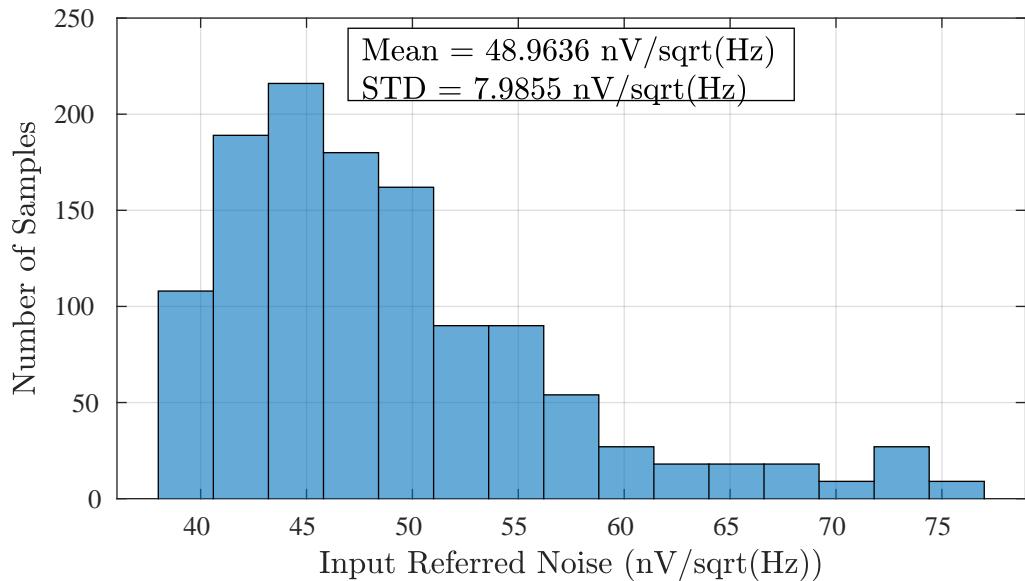


Figure 6.27.: Histogram of Input Referred Noise due to PVT Variation at $V_{bias}=150\text{mV}$

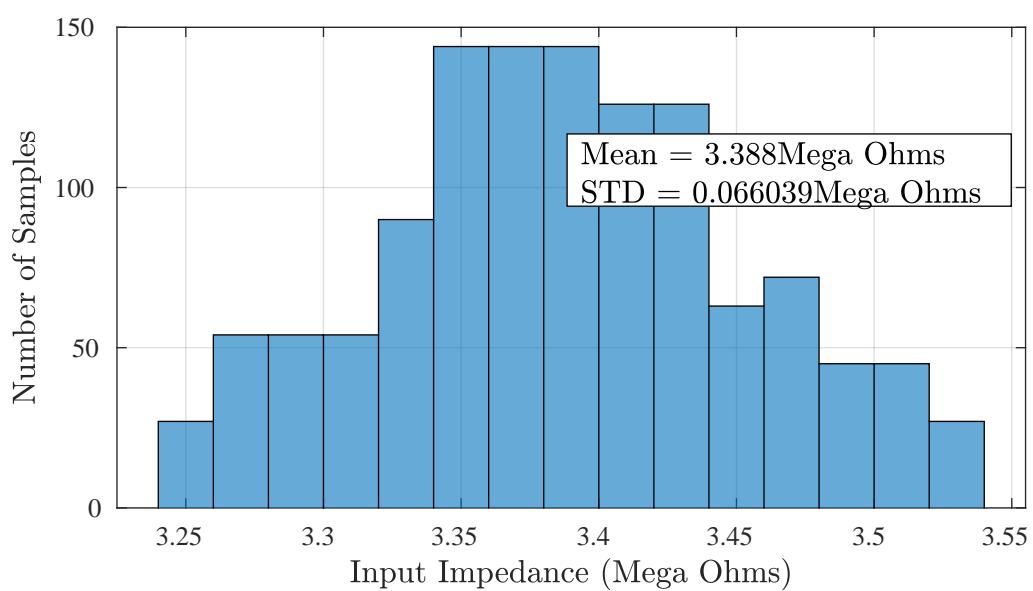


Figure 6.28.: Histogram of Input Impedance due to PVT Variation at $V_{bias}=150\text{mV}$

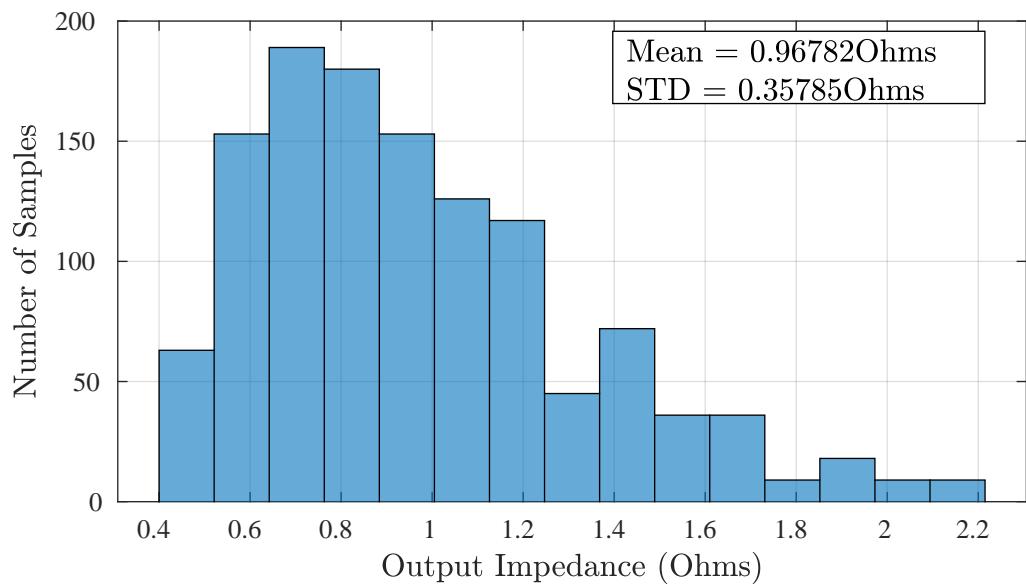


Figure 6.29.: Histogram of Output Impedance due to PVT Variation at $V_{bias}=150\text{mV}$

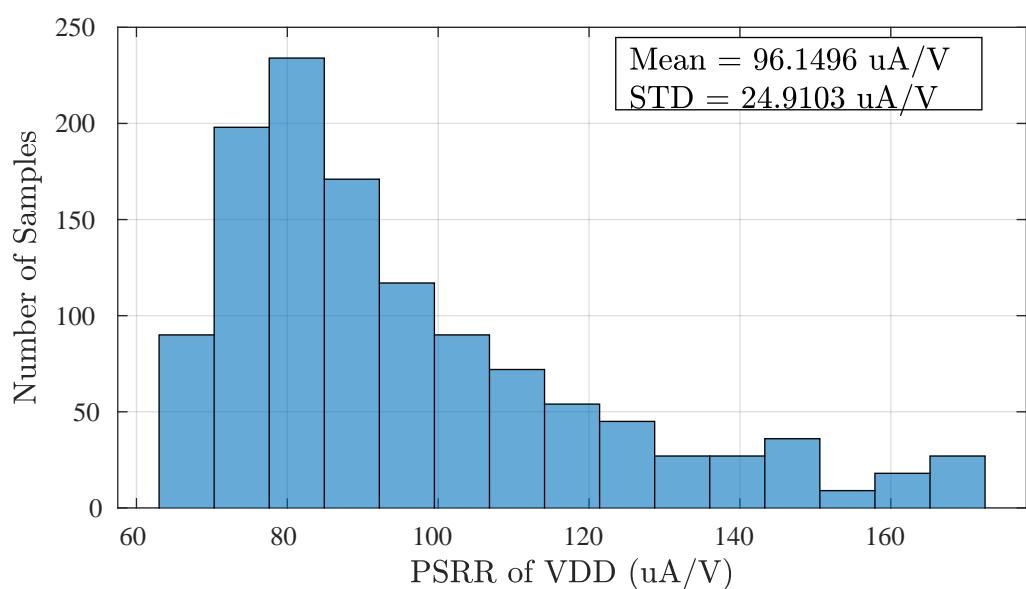


Figure 6.30.: Histogram of PSRR(V_{DD}) due to PVT Variation at $V_{bias}=150\text{mV}$

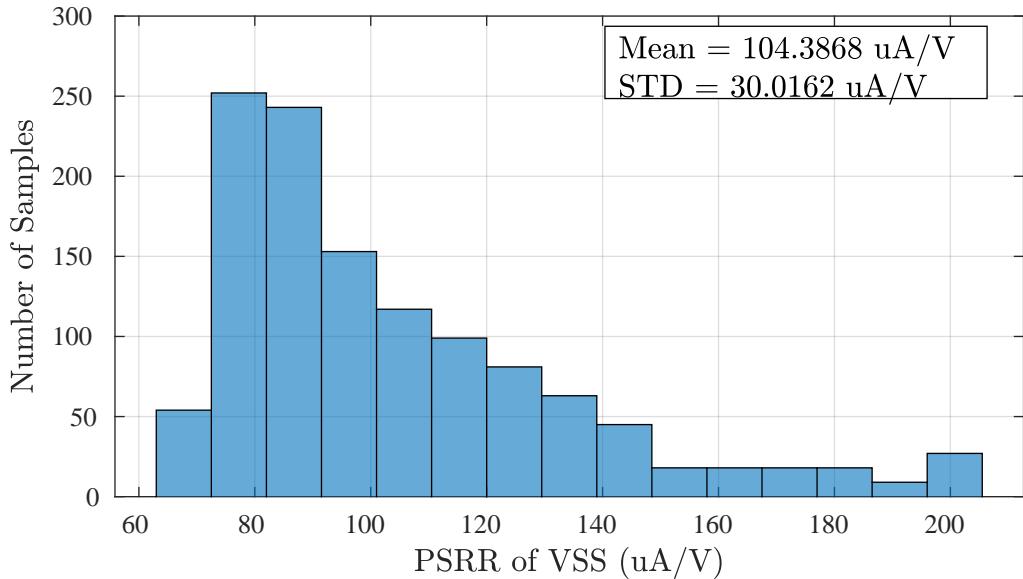


Figure 6.31.: Histogram of PSRR(V_{SS}) due to PVT Variation at $V_{bias}=150\text{mV}$

Highest V_{bias}

For the highest V_{bias} , the mean gain is around 24dB with a standard deviation of 0.7dB. The spread for the gain histogram is comparatively narrower in comparison to the lowest V_{bias} . Once again the bandwidth just falls short of 10MHz for the worst case corner. The mean values of the currents are 23mA and -35mA. But at the worst case corner, the peak-to-peak current is as low as 40mA. The mean values of HD2 and HD3 are below -30dBc but they rise above the -30dBc mark for slow corners. The input referred noise spread is much smaller for highest V_{bias} with a mean value of $32.985\text{nV}/\sqrt{\text{Hz}}$.

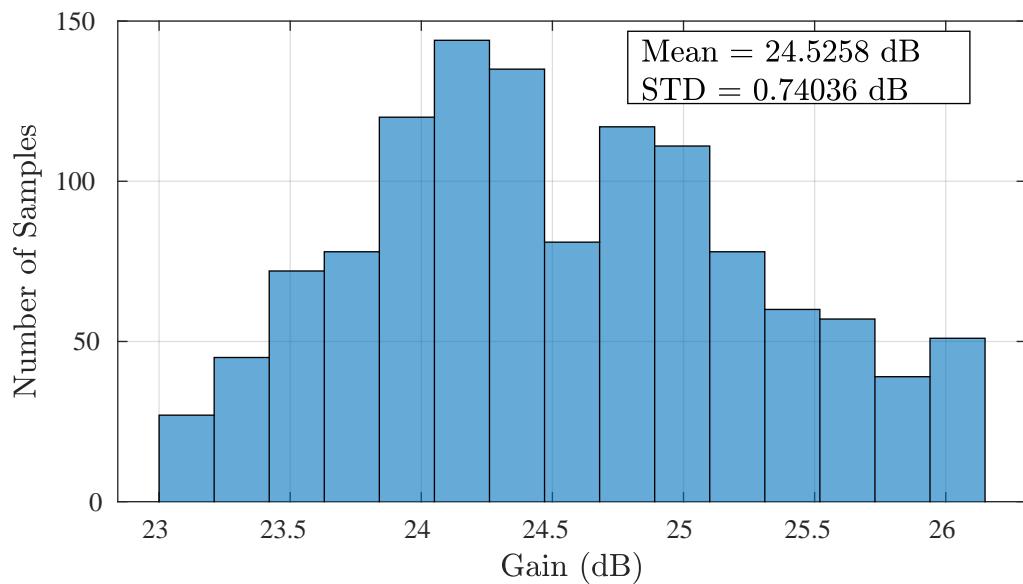


Figure 6.32.: Histogram of System Gain due to PVT Variation at $V_{bias}=700\text{mV}$

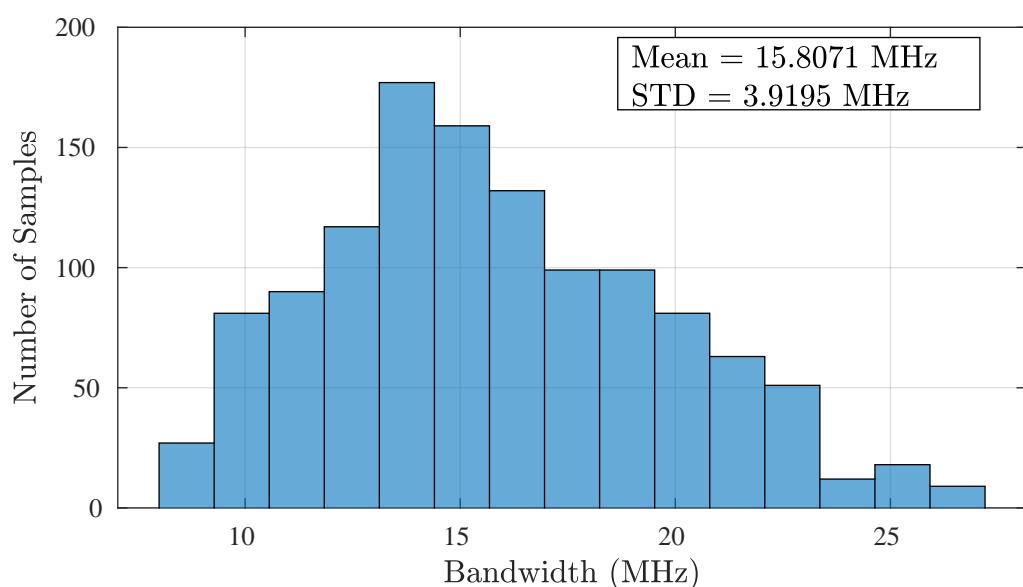


Figure 6.33.: Histogram of System Bandwidth due to PVT Variation at $V_{bias}=700\text{mV}$

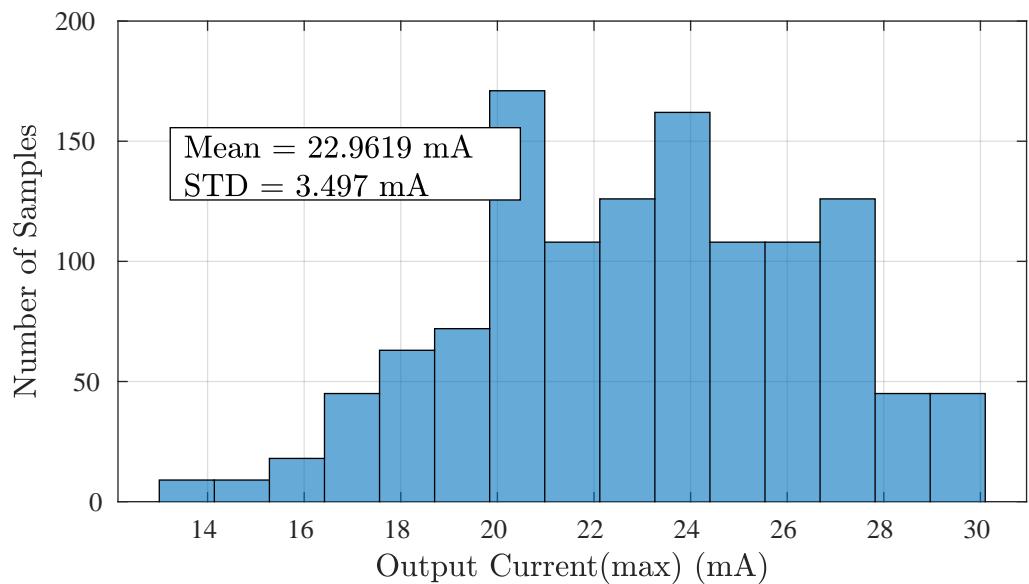


Figure 6.34.: Histogram of Maximum Output Current due to PVT Variation at $V_{bias}=700\text{mV}$

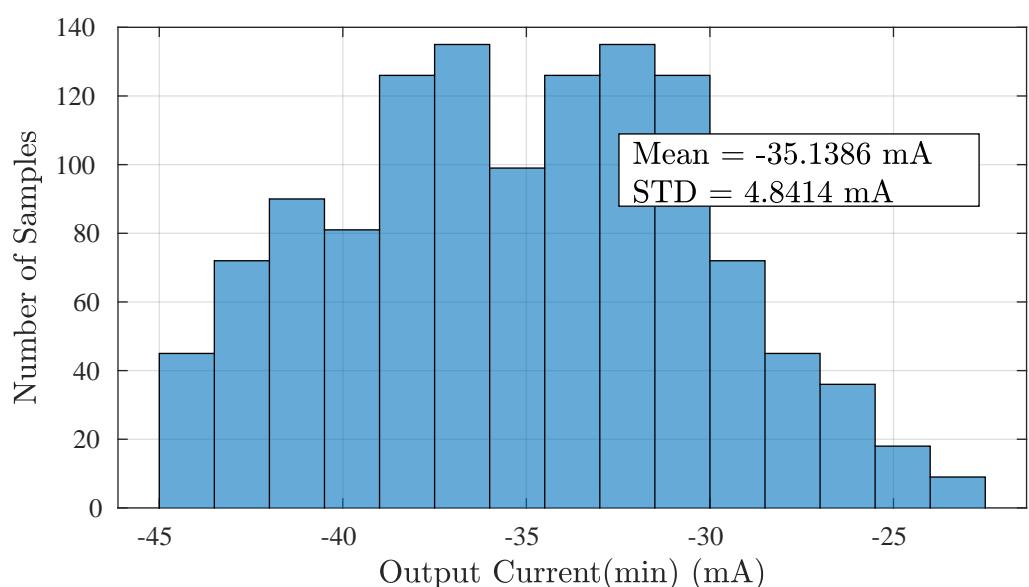


Figure 6.35.: Histogram of Minimum Output Current due to PVT Variation at $V_{bias}=700\text{mV}$

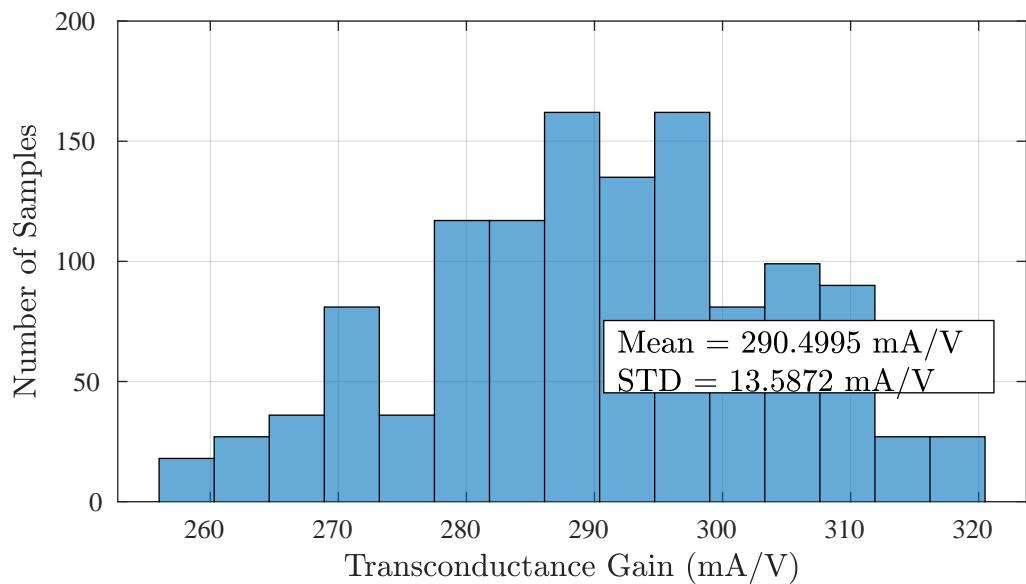


Figure 6.36.: Histogram of Transconductance due to PVT Variation at $V_{bias}=700\text{mV}$

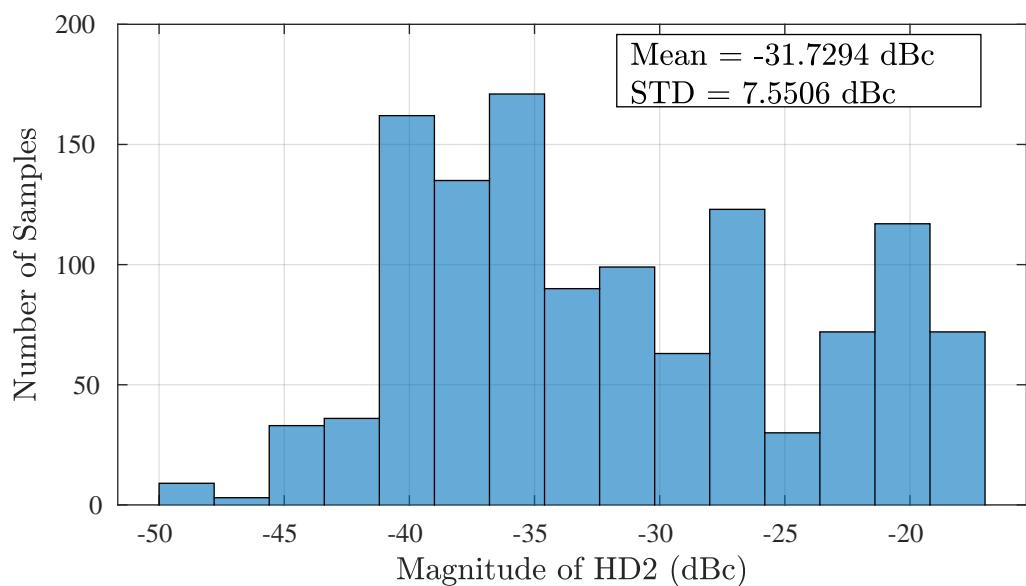


Figure 6.37.: Histogram of HD2 due to PVT Variation at $V_{bias}=700\text{mV}$

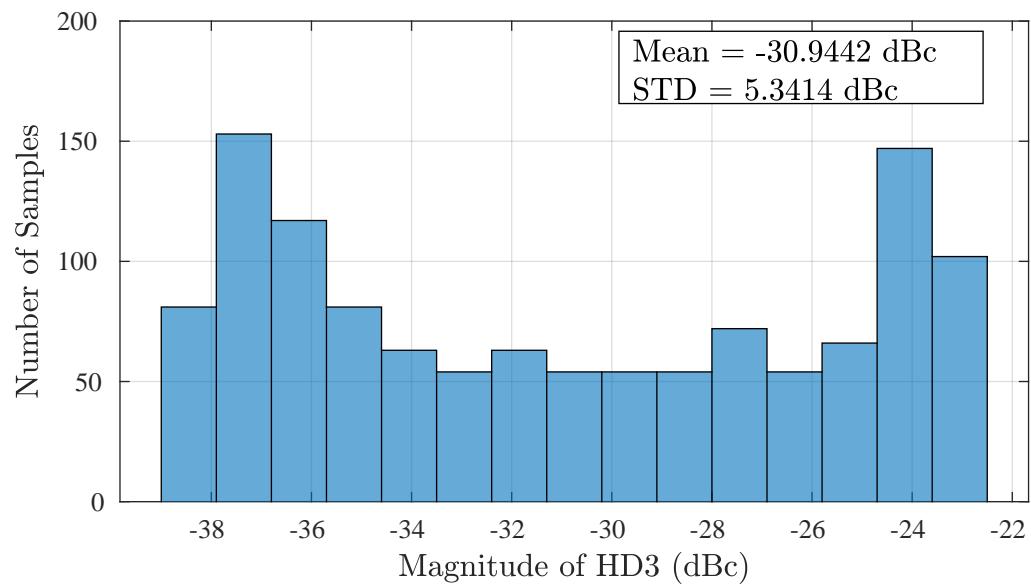


Figure 6.38.: Histogram of HD3 due to PVT Variation at $V_{bias}=700\text{mV}$

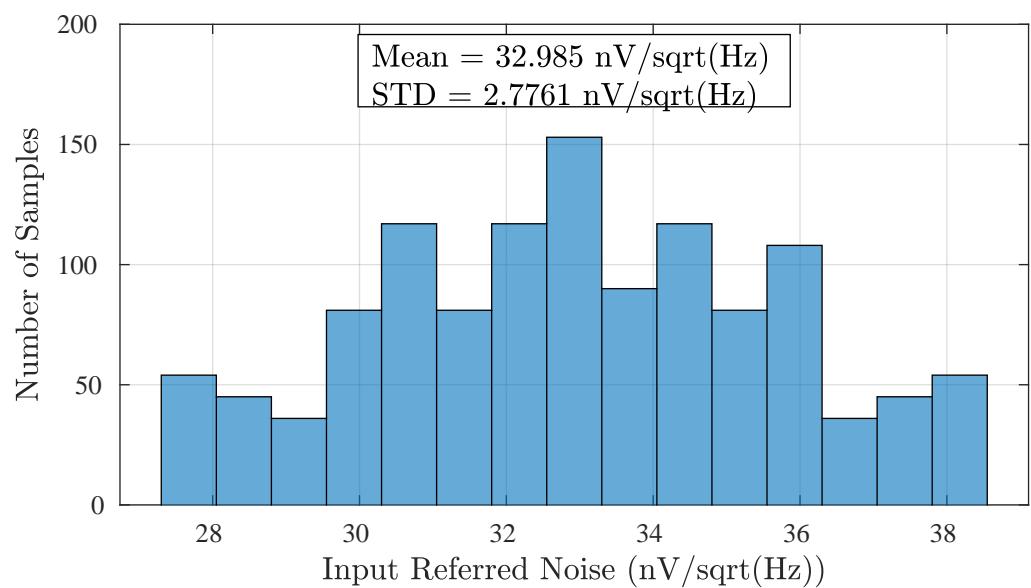


Figure 6.39.: Histogram of Input Referred Noise due to PVT Variation at $V_{bias}=400\text{mV}$

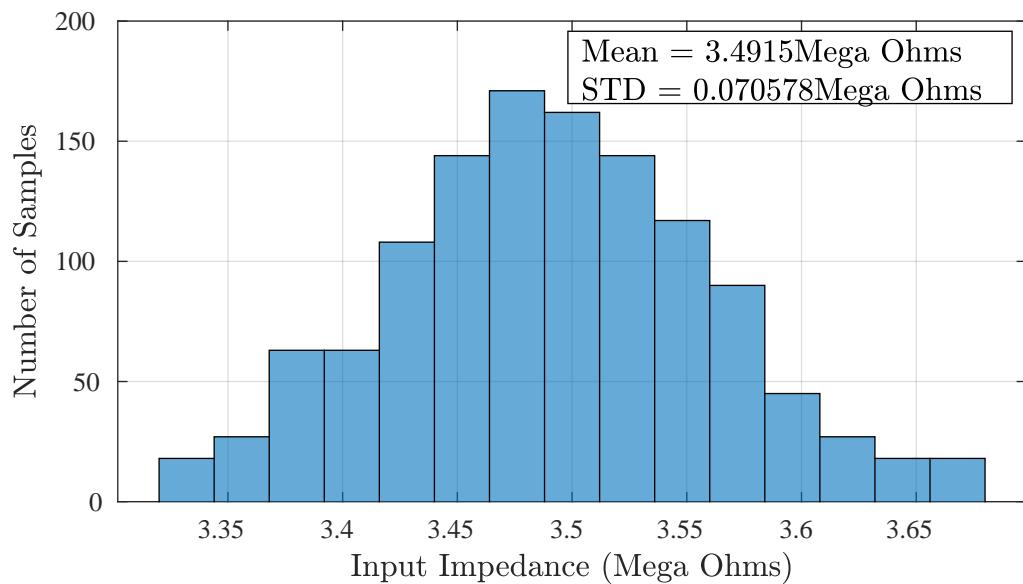


Figure 6.40.: Histogram of Input Impedance due to PVT Variation at $V_{bias}=700\text{mV}$

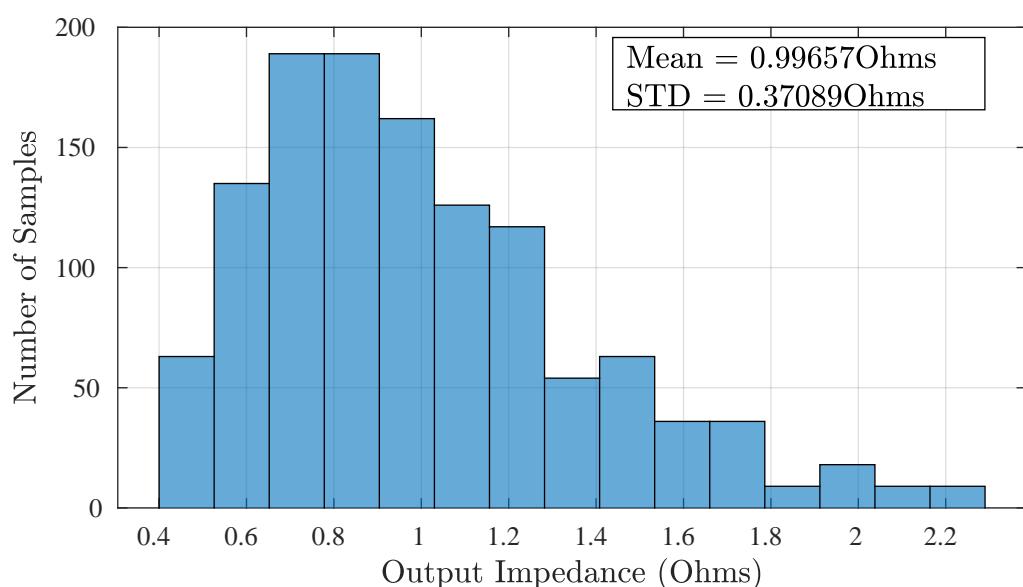


Figure 6.41.: Histogram of Output Impedance due to Process and Supply Variation at $V_{bias}=700\text{mV}$

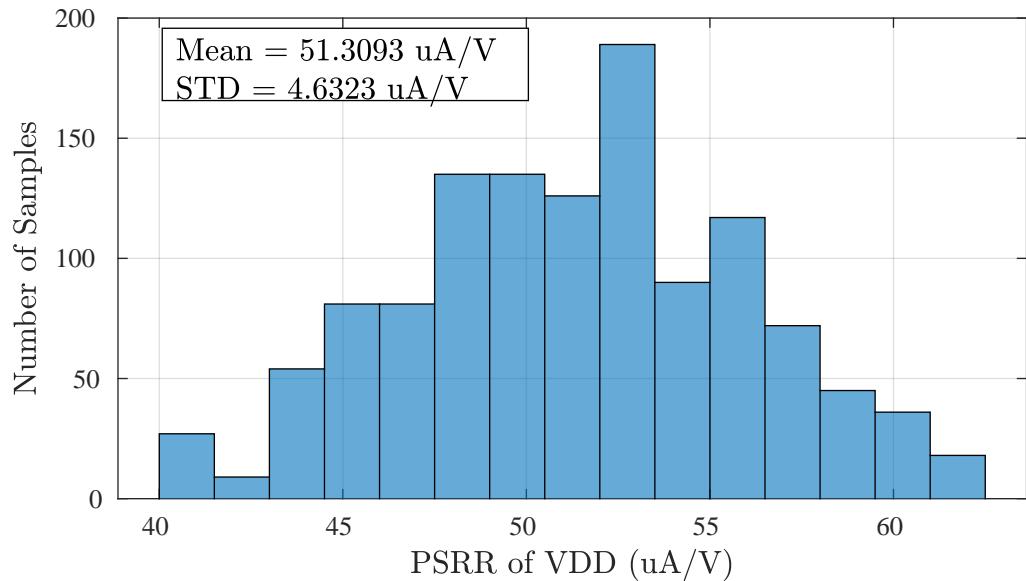


Figure 6.42.: Histogram of PSRR(V_{DD}) due to PVT Variation at $V_{bias}=700\text{mV}$

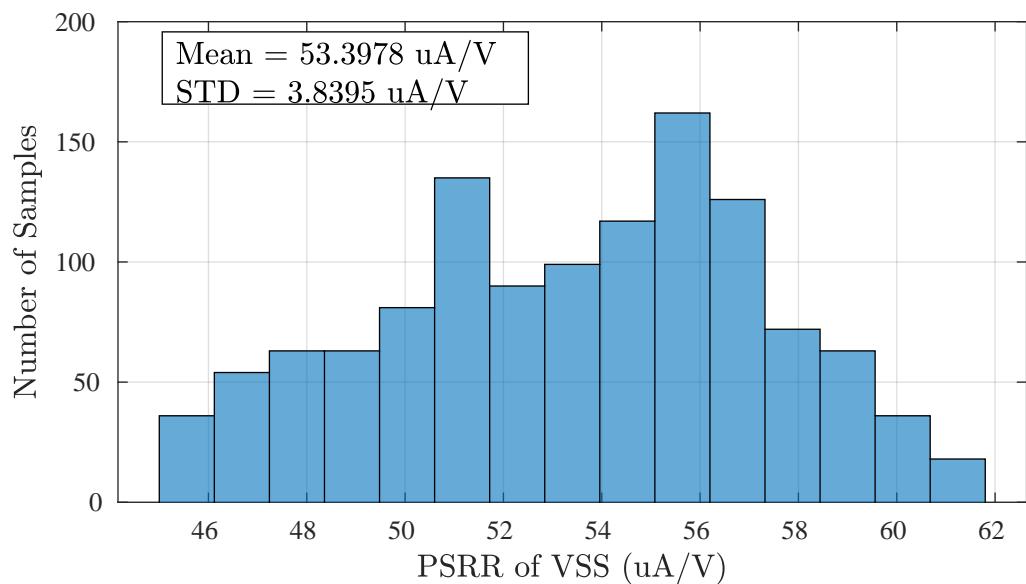


Figure 6.43.: Histogram of PSRR(V_{SS}) due to PVT Variation at $V_{bias}=700\text{mV}$

6.4 Summary of PVT Corner Analysis

The summary of all PVT corners of the lowest and highest V_{bias} is presented in this section. As seen in the previous sections, the current is worst at lowest V_{bias} , with a value of -1.62mA. The worst case open loop gain of the OTA is 12dB for the lowest V_{bias} . The mean values of all the parameters are very close to the typical or nominal case.

Parameter	Min	Max	Mean
Transconductance Gain(Gm)	81 mA/V	241 mA/V	158.2 mA/V
Output Current(+)	-1.626 mA	28.01 mA	14.79 mA
Output Current(-)	-28.41 mA	-7.123 mA	-16.84 mA
Bandwidth	8.858 MHz	28.46 MHz	16.7 MHz
Input Referred Noise	36.62 nV/ \sqrt{Hz}	75.85 nV/ \sqrt{Hz}	48.96 nV/ \sqrt{Hz}
Input Impedance	3.241 M Ω	3.352 M Ω	3.388 M Ω
Output Impedance	0.418 Ω	2.207 Ω	0.968 Ω
HD2	-63.12 dBc	-31.12 dBc	-41.2 dBc
HD3	-78.03 dBc	-39.28 dBc	-51.6 dBc
Open Loop Voltage Gain	12.3 dB	22.51 dB	18.3 dB
PSRR	61.04 μ A/V	205.1 μ A/V	96.14 μ A/V

Table 6.2.: PVT Corners for $V_{bias} = 150$ mV

Parameter	Min	Max	Mean
Transconductance Gain(Gm)	241.7 mA/V	319.3 mA/V	290.49 mA/V
Output Current(+)	13.6 mA	29.99 mA	22.96 mA
Output Current(-)	-44.21 mA	-23.01 mA	-35.13 mA
Bandwidth	8.235 MHz	27.15 MHz	15.8 MHz
Input Referred Noise	27.62 nV/ \sqrt{Hz}	38.52 nV/ \sqrt{Hz}	32.985 nV/ \sqrt{Hz}
Input Impedance	3.327 M Ω	3.675 M Ω	3.49 M Ω
Output Impedance	0.427 Ω	2.287 Ω	0.996 Ω
HD2	-48.93 dBc	-18.36 dBc	-31.72 dBc
HD3	-39.28 dBc	-22.5 dBc	-30.94 dBc
Open Loop Voltage Gain	22.5 dB	26.14 dB	24.52 dB
PSRR	40.76 μ A/V	64.63 μ A/V	51.3 μ A/V

Table 6.3.: PVT Corners for $V_{bias} = 700$ mV



7 Conclusion

As part of a closed loop DC current transformer, it was required to design a programmable Operational Transconductance Amplifier that generates a current of $\pm 15\text{mA}$ and drives a resistive load. Different topologies of OTAs were considered and evaluated by weighing their pros and cons with respect to the specifications. A high output current transconductance amplifier was designed and implemented using the XT018 SOI technology from XFAB. The amplifier consists of two stages -

1. A programmable operational transconductance amplifier that is based on conventional current mirror technique. The output voltage is controlled by an external voltage that indirectly controls the bias current.
2. An operational amplifier based on the two-stage Miller compensation technique is used as a voltage buffer. This stage produces high currents due the bulky dimensions of the common source amplifier.

Using the G_m/I_D methodology, the dimensions of the differential pair were set at an optimal value in moderate saturation for both the stages of the system. Setting the bias voltage at the output of the first stage is a challenging task in itself, given that the variable parameter - external voltage causes a variation in the DC bias output voltage. To keep the variation to a minimum, the bias currents were chosen in the milliAmpere range and the output shell of the OTA was designed to be assymetric. The OP AMP was designed to have a wide ICMR and produce a high current that drives a resistive load. The range of currents produced by this system is from $\pm 15\text{mA}$ to $\pm 30\text{mA}$. The programmable parameter - the external bias voltage is swept from 150mV to 700mV and the output is measured across a 50Ω load resistor. For this setup, the DC bias voltage at the output of the amplifier is not a constant as the variable parameter is the bias current. However, the design is tweaked in such a way that the variation is kept to a minimum. Another design approach is presented with a fixed external voltage, a fixed bias current but a variable load resistor. In this case, the same range of output current is obtained for an external bias voltage of 450mV and the load varying from 35Ω to 70Ω . The advantage of this approach over the previous approach is the fact that the DC Bias voltage at the output does not vary with variation in the programmable resistor.

7.1 Summary of Results

Parameter	Value/Specification	Programmable Voltage	Programmable Resistor
Circuit Design	Programmability	External Voltage V_{bias}	Load Resistor R_L
Transconductance Gain(Gm)	75 .. 140 mA/V	158.8 .. 298.5 mA/V	170 .. 338.9 mA/V
Linear Input Voltage Range	± 200 mV	± 100 mV	± 100 mV
Output Current Range	± 15 mA	+18 mA .. -13 mA	+15 mA .. -18 mA
Bandwidth	10 MHz	13.8 MHz	13.13 MHz
Slew Rate	± 900 V/ μ s	± 10.82 V/ μ s	± 10.28 V/ μ s
Rise/Fall time	4.4 ns	22.7 ns	23.5 ns
Input Referred Noise	3 nV/ \sqrt{Hz} @few KHz	46.64 nV/ \sqrt{Hz} @1MHz	36.79 nV/ \sqrt{Hz} @1MHz
Input Impedance	0.5 M Ω	3.394 M Ω	3.436 M Ω
Output Impedance	55 K Ω	0.9415 Ω	0.953 Ω
HD2	Less than -75 dBc	-34.72 dBc	-34.6 dBc
HD3	Less than -80 dBc	-33.61 dBc	-39.4 dBc
Open Loop Voltage Gain	Not less than +5 V/V	8.41 V/V	12.9 V/V
PSRR	± 20 μ A/V	97.76 μ A/V	67.32 μ A/V

Table 7.1.: Specification vs Results

Table 7.1 summarizes the results of the overall system and compares it with the actual specifications. First thing here to note is the linear input voltage range. Due to varying bias currents of the OTA, the gain keeps varying too. And to avoid saturation, the gain must be low. But OTAs in general have very high gain than a conventional OP AMP. So for this reason, to avoid saturation at the output, the input voltage range is reduced to 100mV instead of 200mV. And consequently, the transconductance parameter is double of what was required. Had the dimensions of the differential pair been smaller, then the input referred noise would shoot up further. Since the input referred noise is already high, the linear input voltage range had to be compromised. The other specifications are picked from the commercial OTA OPA860 (citation), which is a BJT based OTA with a low output impedance buffer. The power supply for the commercial OTA was observed to be +5V and -5V. In this work, the power supplies to be used are -2.5V and 2.5V. So the headroom for the transistors to utilize is much lesser. The OTA being used in an open loop implies that the gain cannot be high. So there is a trade off between input referred noise and the gain. Consequently the operating bandwidth gets effected. The key thing here is to note the output impedance requirement. Ideally, current sources have infinite output impedance. Practically however, for an amplifier with an output buffer, a high impedance at the output nodes is impractical to achieve.

7.2 Outlook

The amplifier designed has been simulated at all corners. The OTA can be used to test the Closed loop NDCCT. There is no second thought that there is room for improvement and further optimization of the amplifier to better meet the specifications. But this needs more research, and implementation of blocks like slew rate enhancer, current feedback amplifier, and possibly an emitter follower to amplify the current further if necessary.



A Appendix

A.1 Corner Simulation

Process Variation - Overall System: Lowest V_{bias}

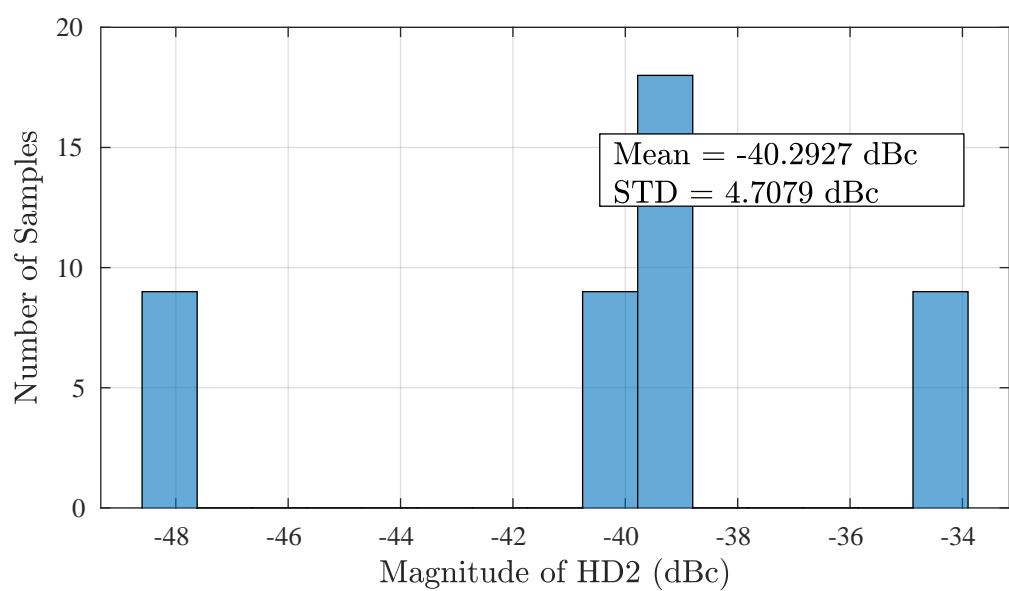


Figure A.1.: Histogram of HD2 due to Process Variation at $V_{bias}=150\text{mV}$

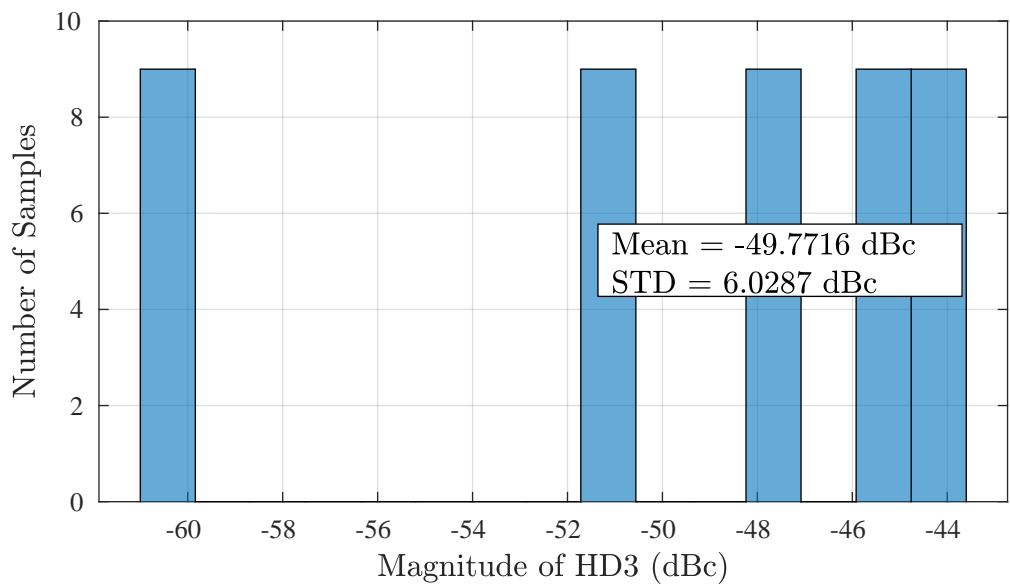


Figure A.2.: Histogram of HD3 due to Process Variation at $V_{bias}=150\text{mV}$

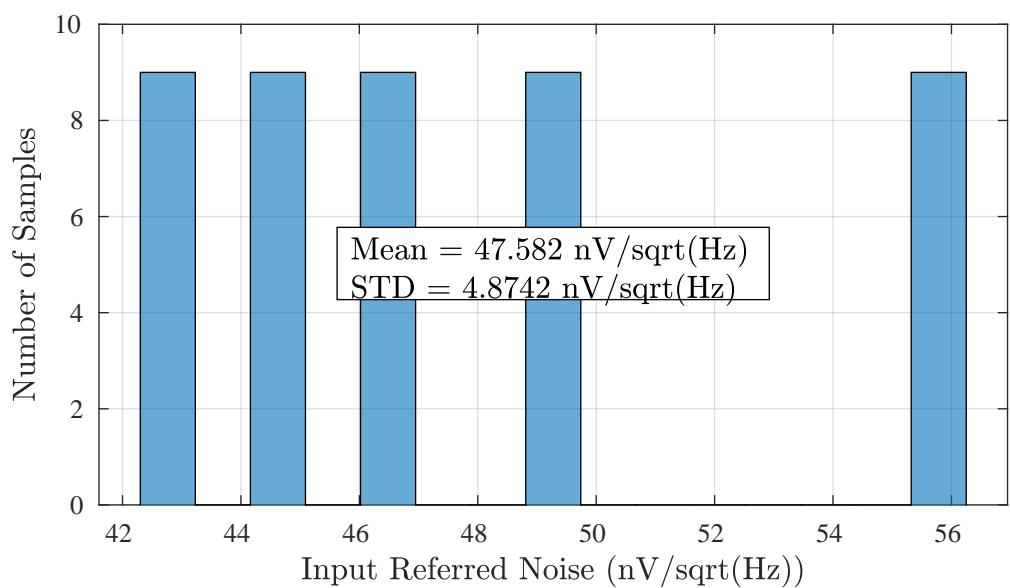


Figure A.3.: Histogram of Input Referred Noise due to Process Variation at $V_{bias}=150\text{mV}$

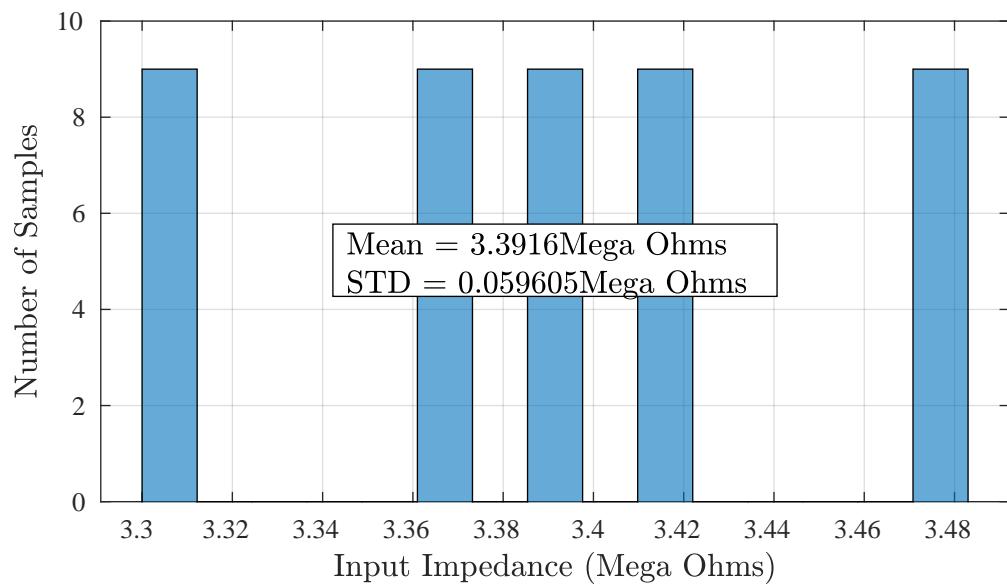


Figure A.4.: Histogram of Input Impedance due to Process Variation at $V_{bias}=150\text{mV}$

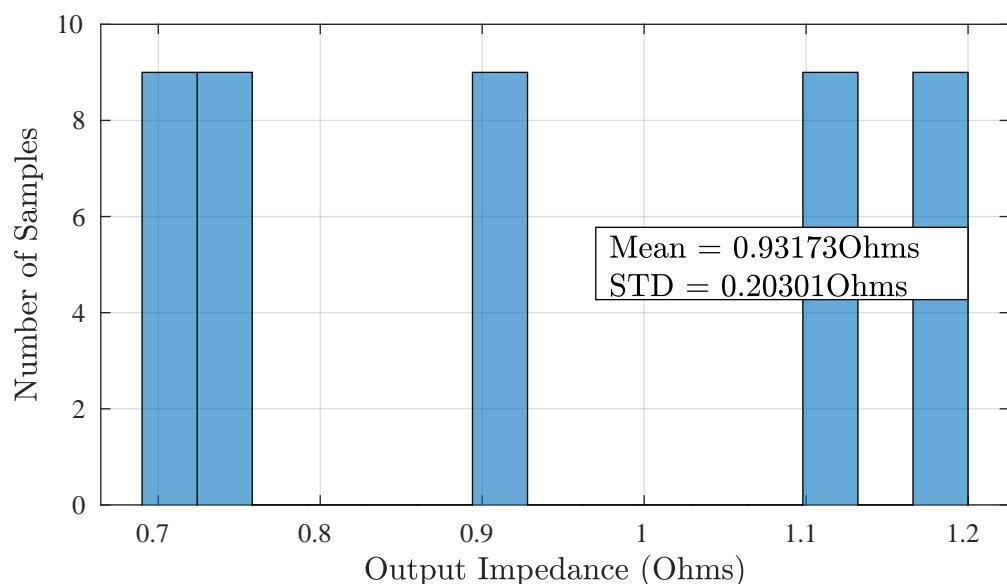


Figure A.5.: Histogram of Output Impedance due to Process Variation at $V_{bias}=150\text{mV}$

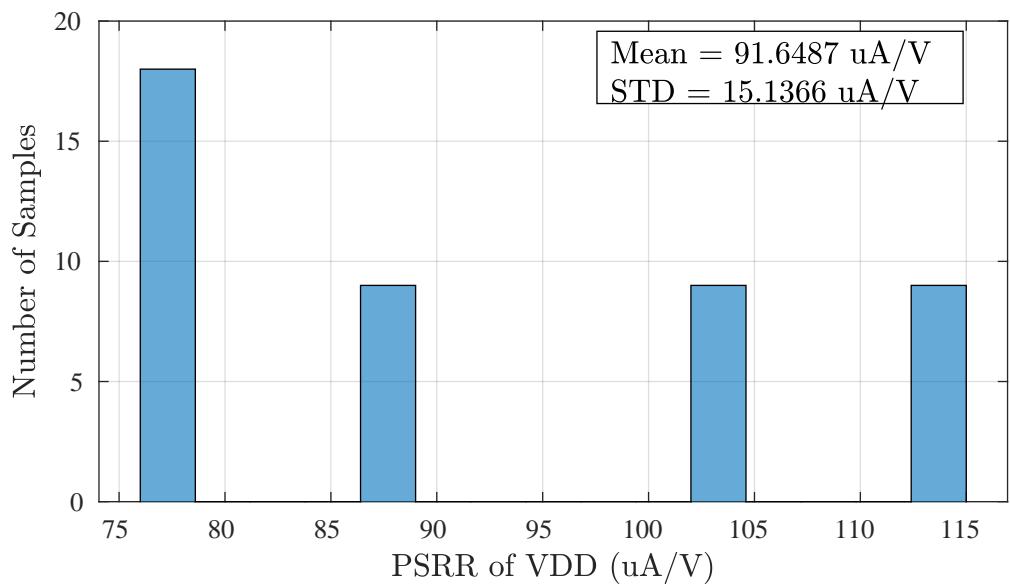


Figure A.6.: Histogram of PSRR(V_{DD}) due to Process Variation at $V_{bias}=150\text{mV}$

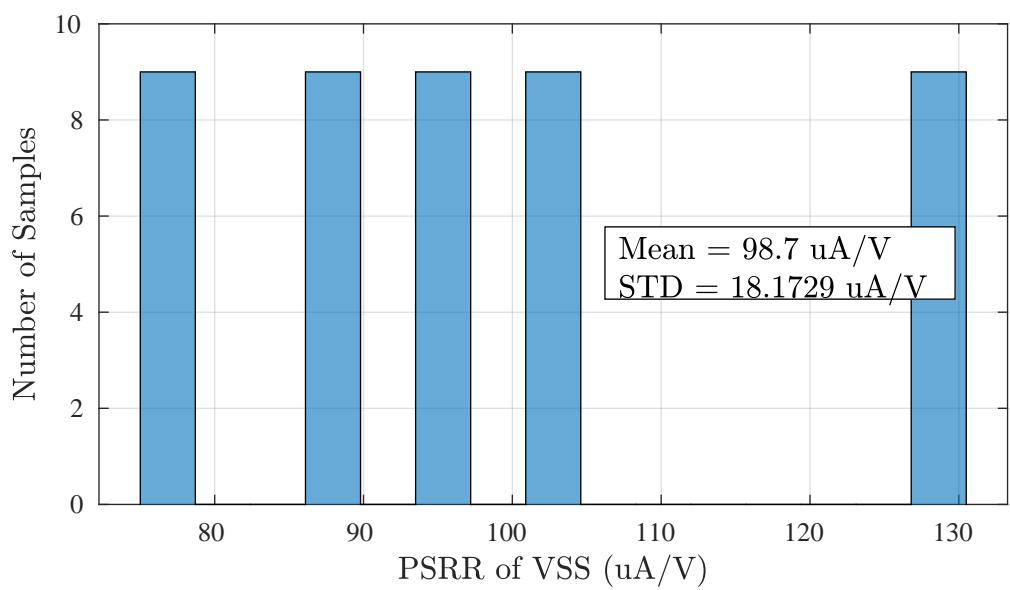


Figure A.7.: Histogram of PSRR(V_{SS}) due to Process Variation at $V_{bias}=150\text{mV}$

Process Variation - Overall System: Middle V_{bias}

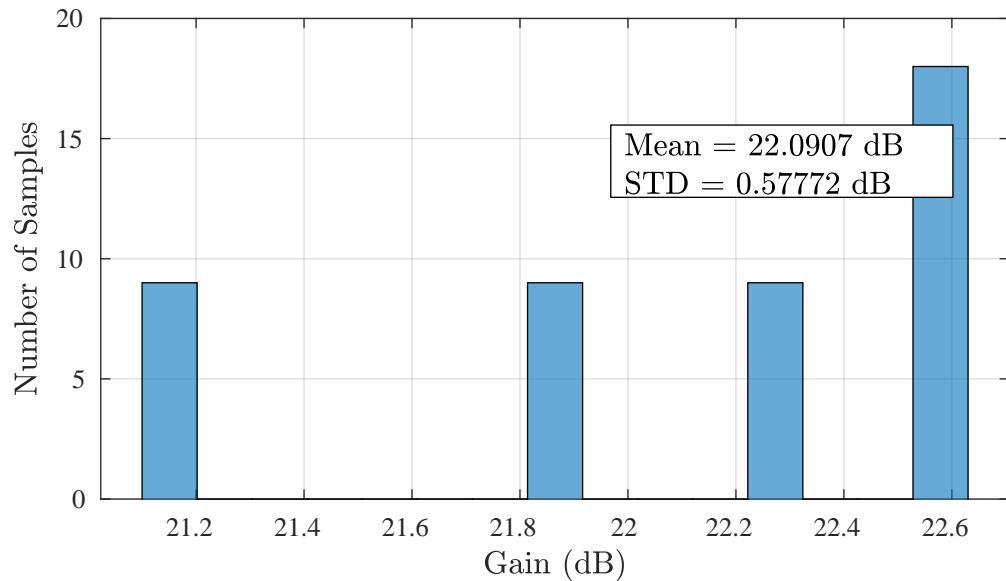


Figure A.8.: Histogram of System Gain due to Process Variation at $V_{bias}=400\text{mV}$

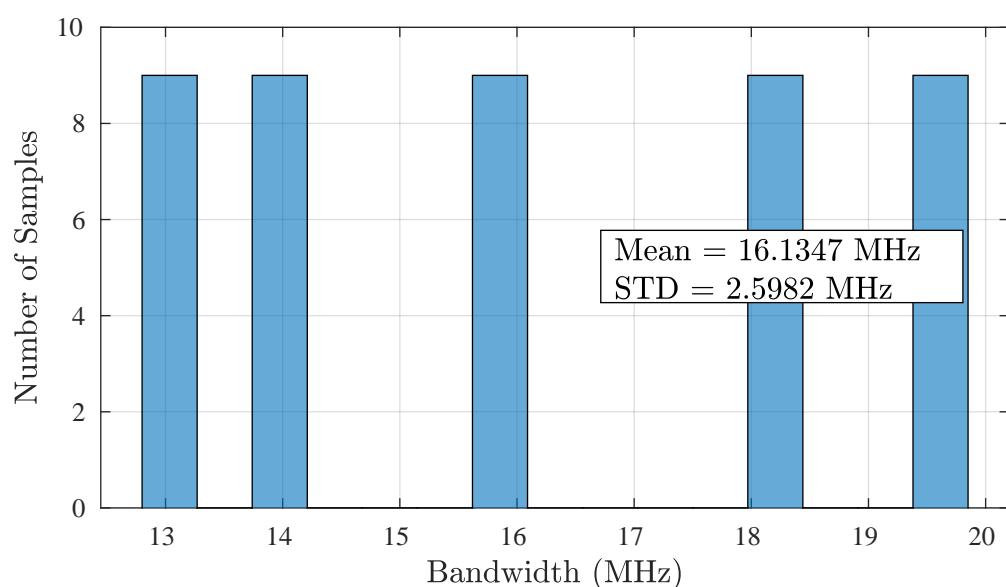


Figure A.9.: Histogram of System Bandwidth due to Process Variation at $V_{bias}=400\text{mV}$

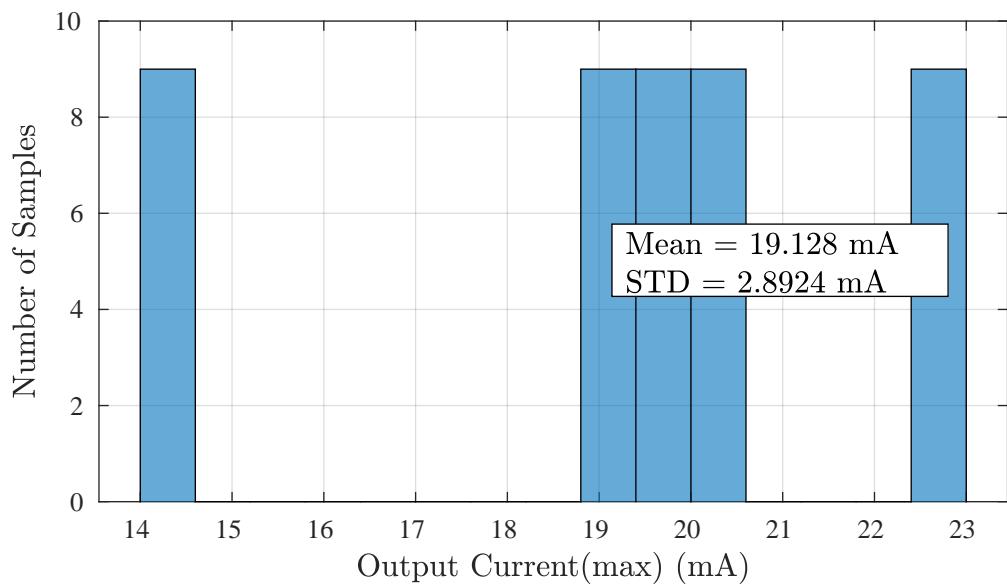


Figure A.10.: Histogram of Maximum Output Current due to Process Variation at $V_{bias}=400\text{mV}$

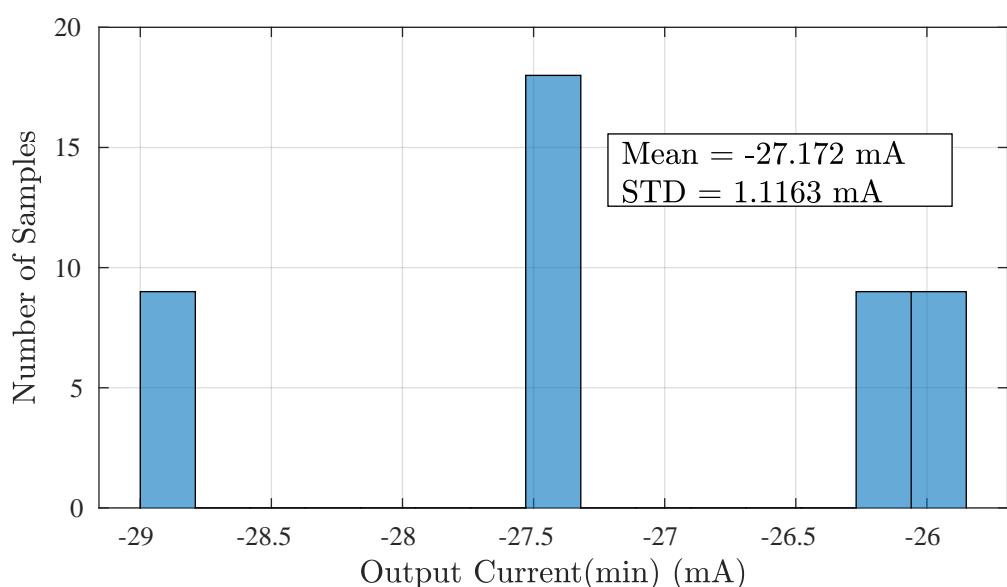


Figure A.11.: Histogram of Minimum Output Current due to Process Variation at $V_{bias}=400\text{mV}$

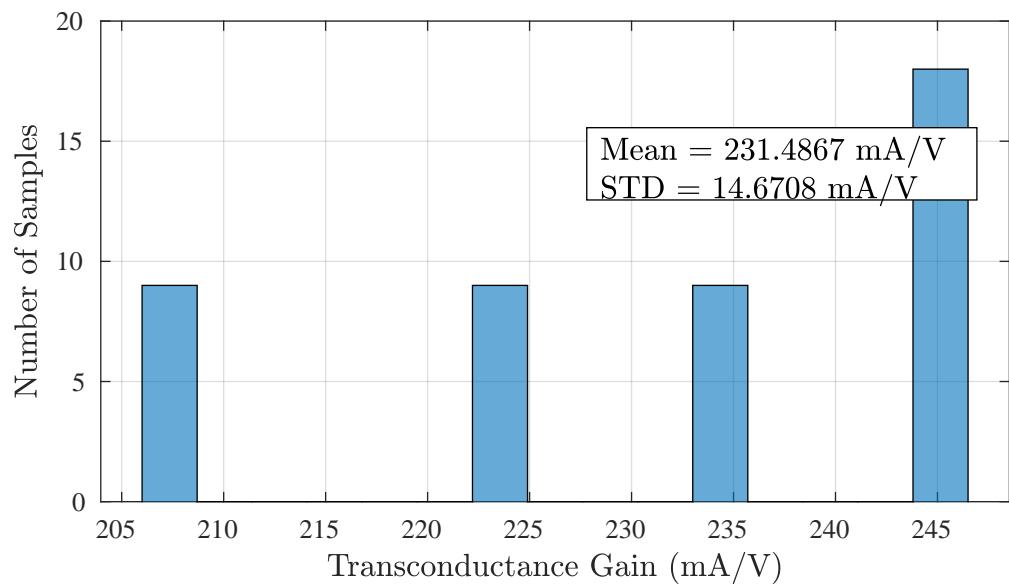


Figure A.12.: Histogram of Transconductance due to Process Variation at $V_{bias}=400\text{mV}$

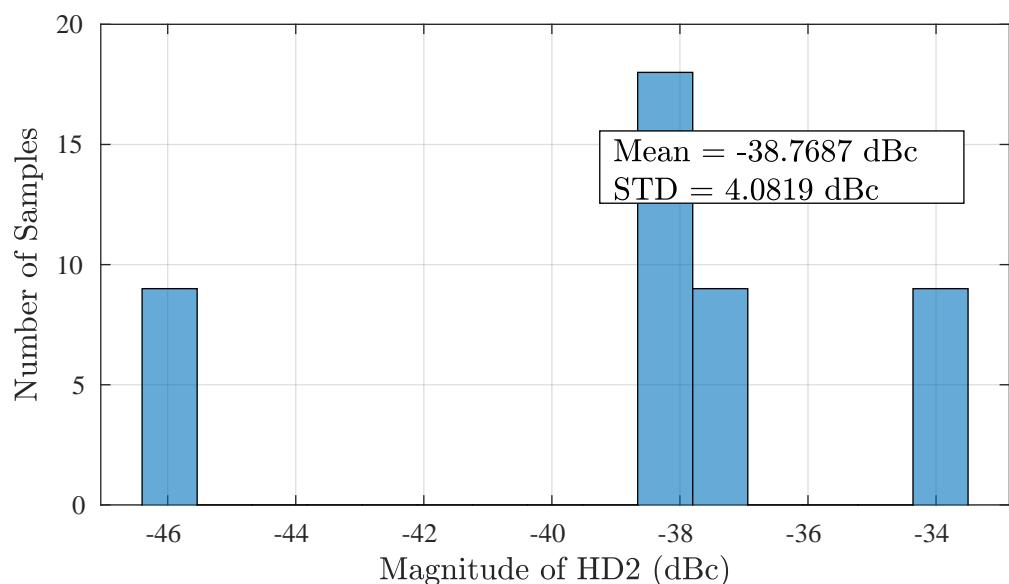


Figure A.13.: Histogram of HD2 due to Process Variation at $V_{bias}=400\text{mV}$

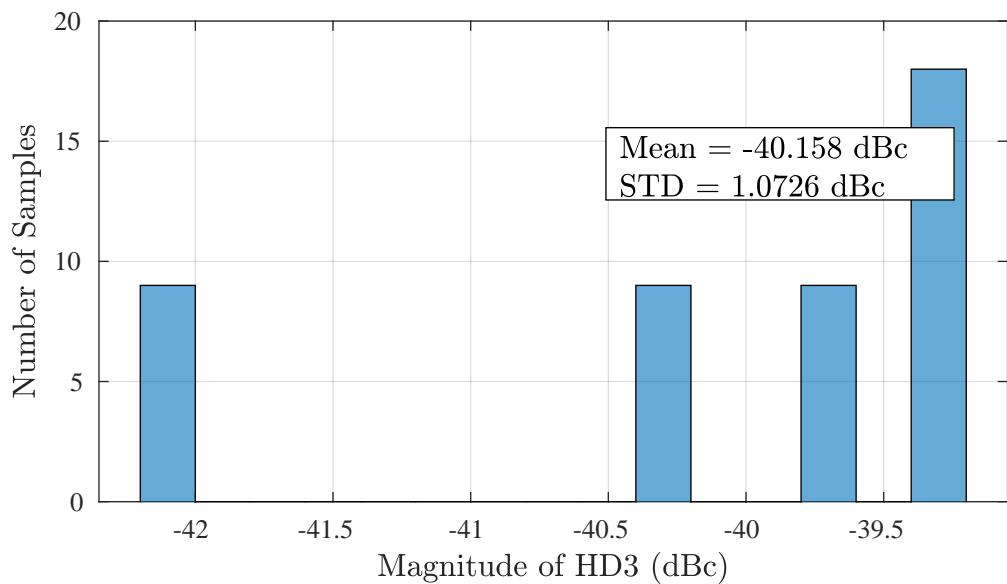


Figure A.14.: Histogram of HD3 due to Process Variation at $V_{bias}=400\text{mV}$

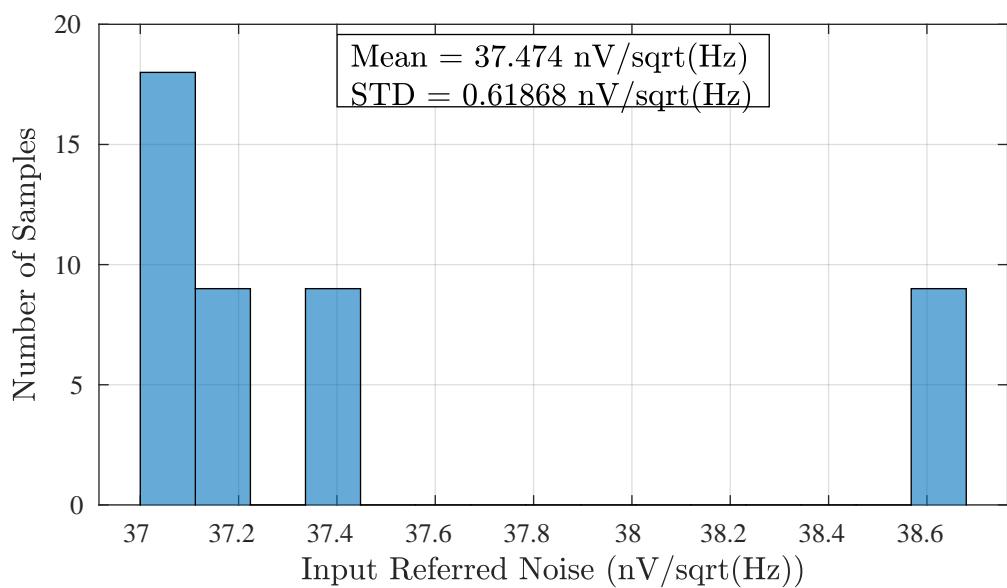


Figure A.15.: Histogram of Input Referred Noise due to Process Variation at $V_{bias}=400\text{mV}$

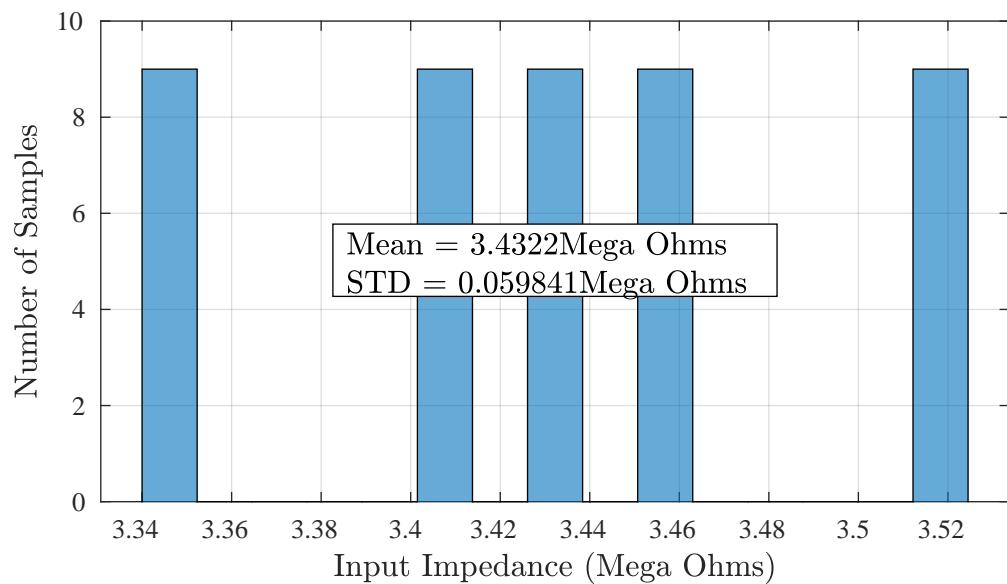


Figure A.16.: Histogram of Input Impedance due to Process Variation at $V_{bias}=400\text{mV}$

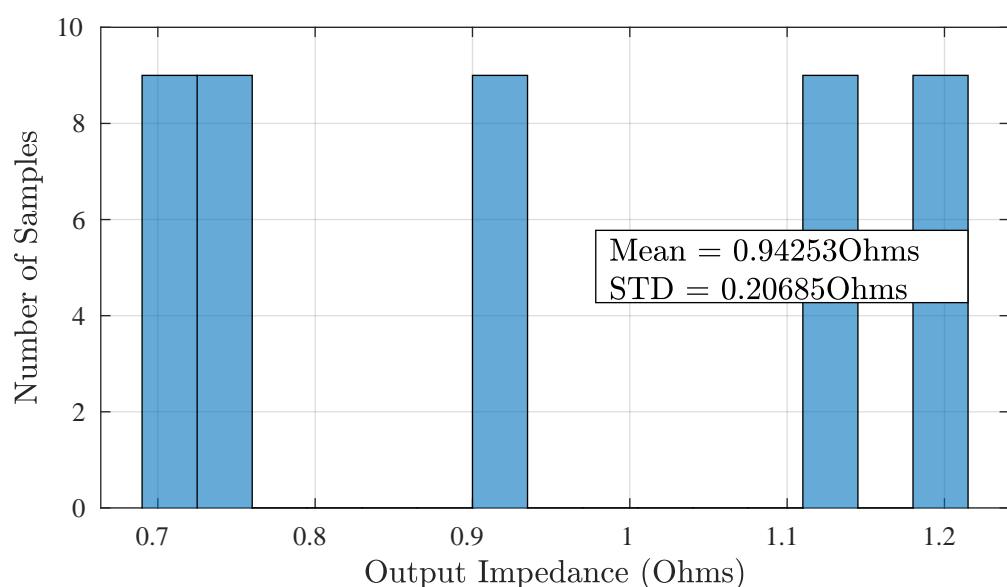


Figure A.17.: Histogram of Output Impedance due to Process Variation at $V_{bias}=400\text{mV}$

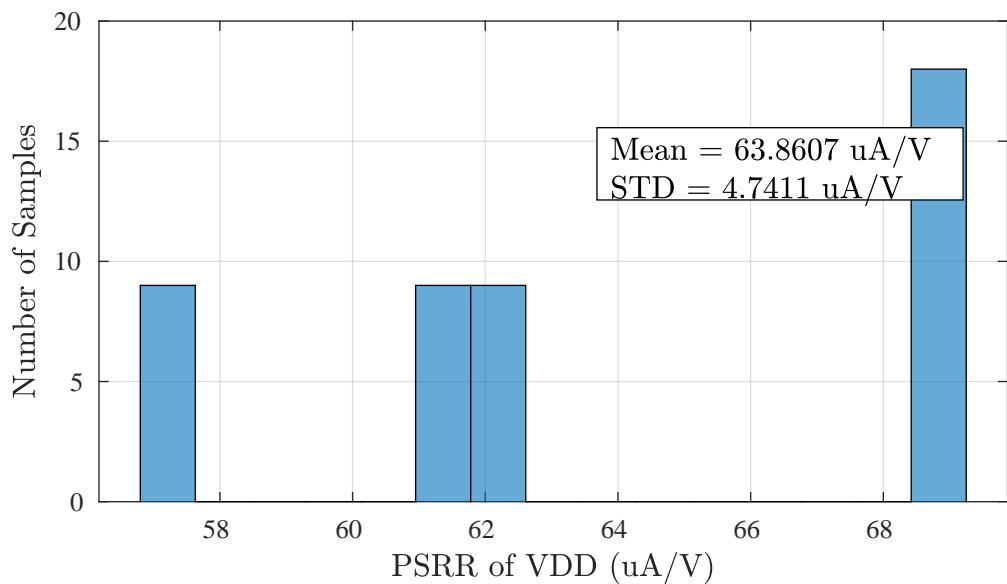


Figure A.18.: Histogram of PSRR(V_{DD}) due to Process Variation at $V_{bias}=400\text{mV}$

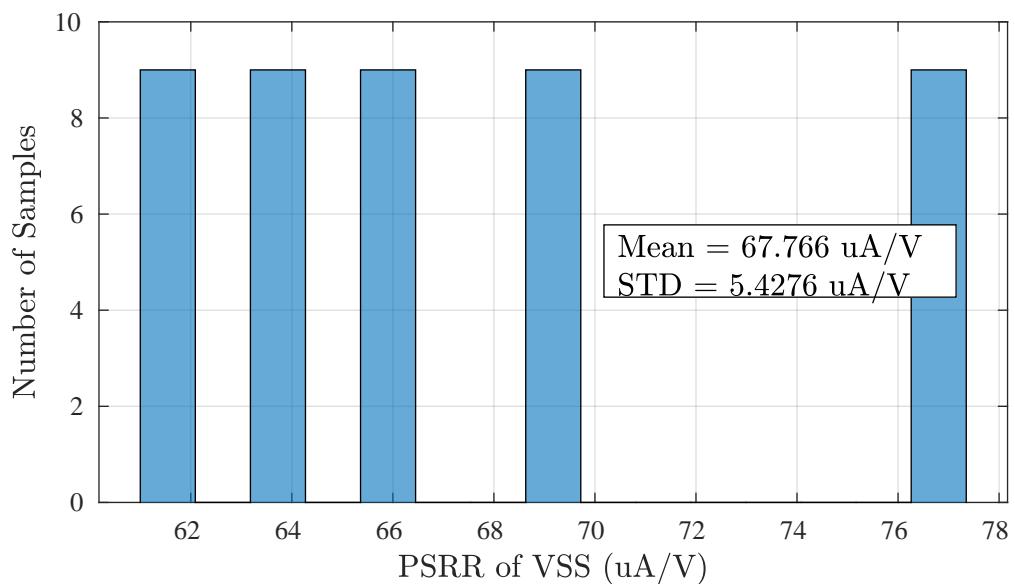


Figure A.19.: Histogram of PSRR(V_{SS}) due to Process Variation at $V_{bias}=400\text{mV}$

Process Variation - Overall System: Highest V_{bias}

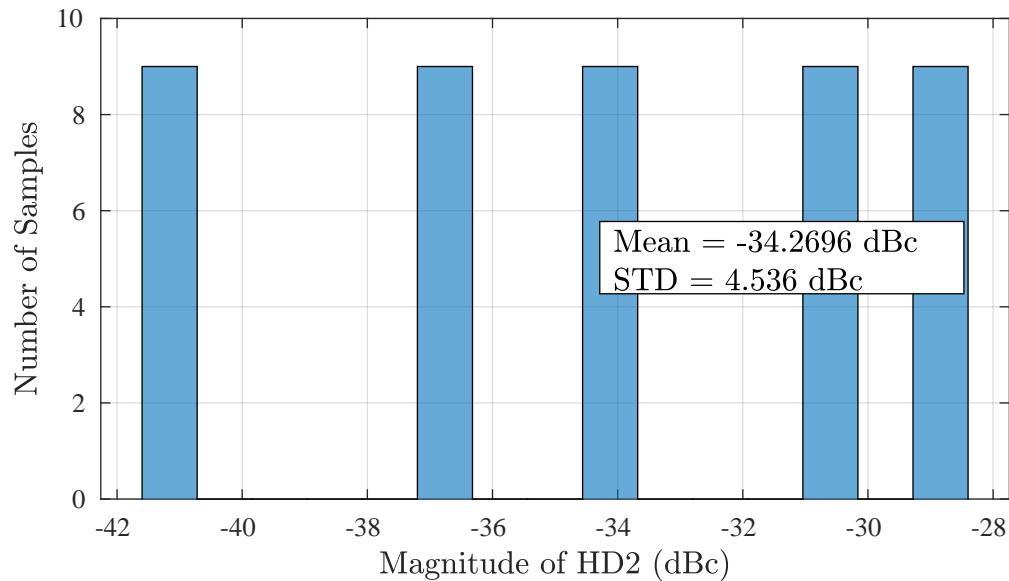


Figure A.20.: Histogram of HD2 due to Process Variation at $V_{bias}=700\text{mV}$

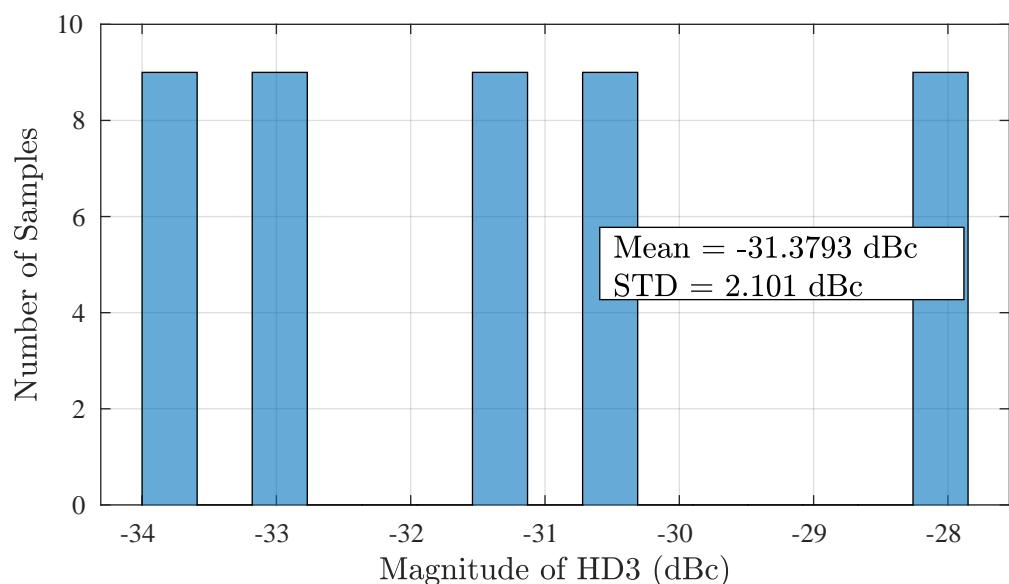


Figure A.21.: Histogram of HD3 due to Process Variation at $V_{bias}=700\text{mV}$

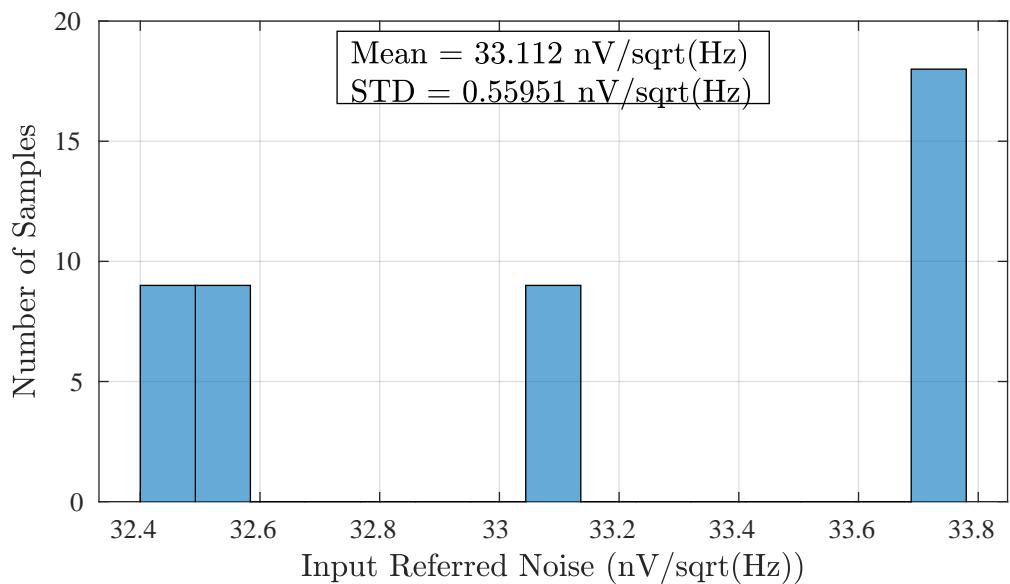


Figure A.22.: Histogram of Input Referred Noise due to Process Variation at $V_{bias}=400\text{mV}$

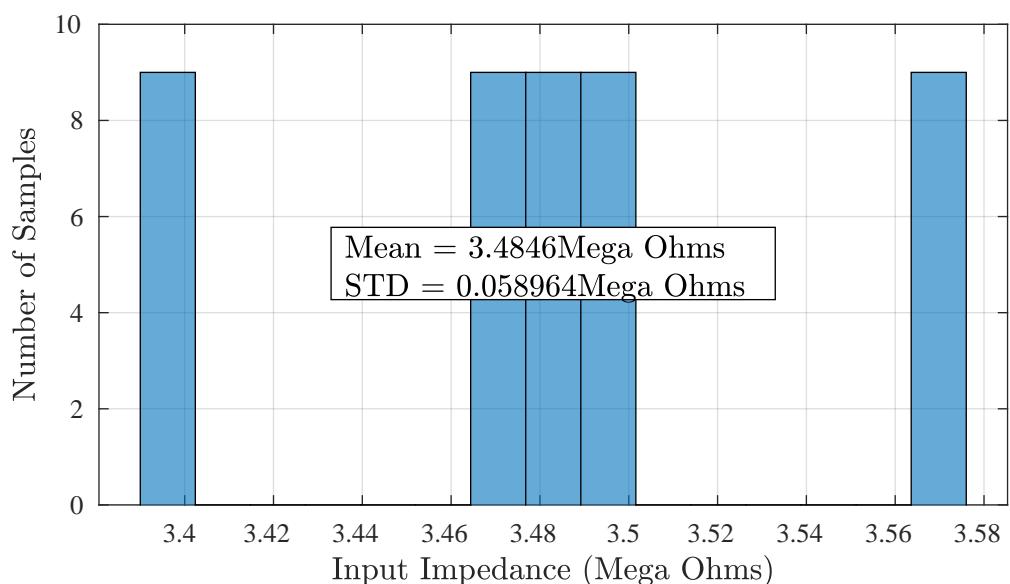


Figure A.23.: Histogram of Input Impedance due to Process Variation at $V_{bias}=700\text{mV}$

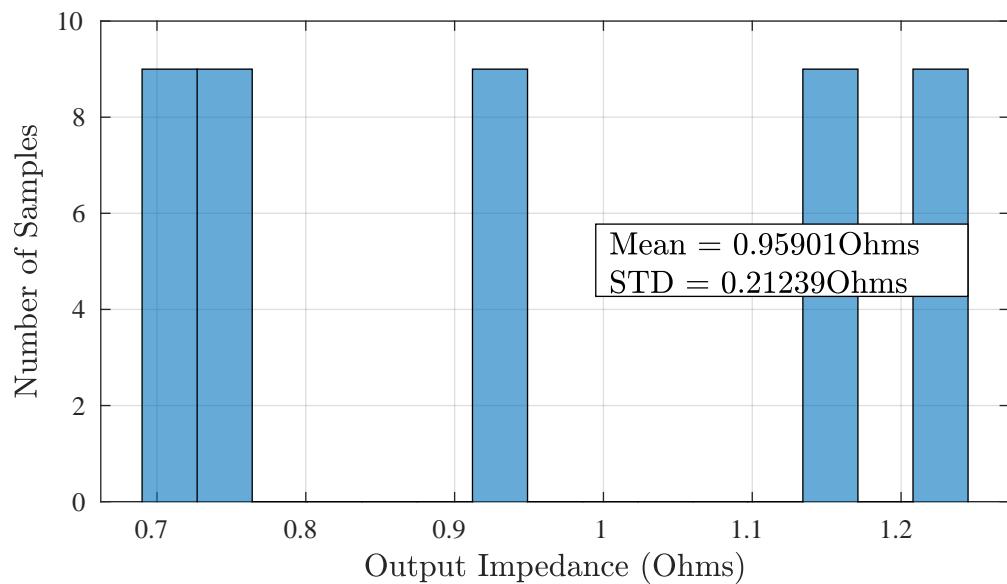


Figure A.24.: Histogram of Output Impedance due to Process Variation at $V_{bias}=700\text{mV}$

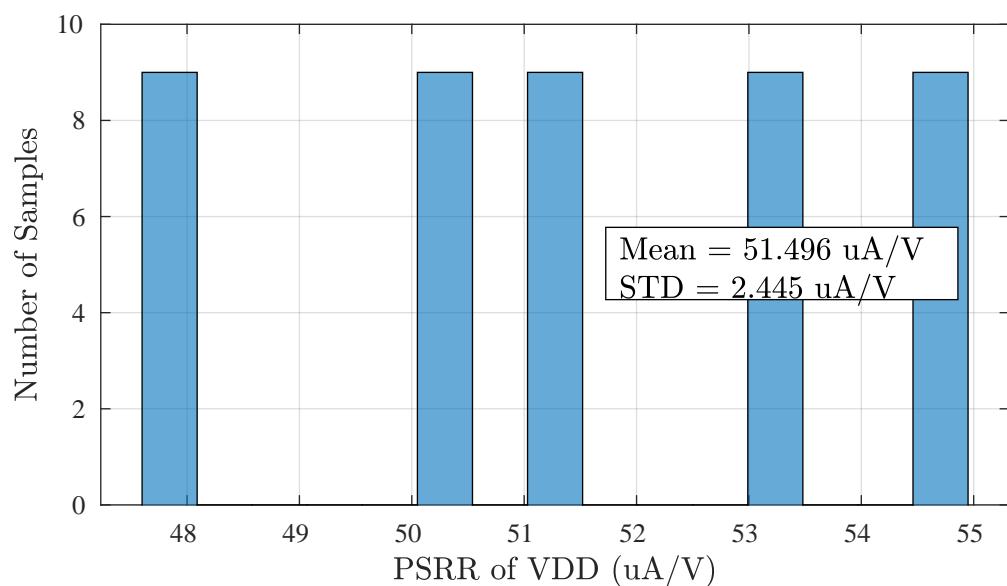


Figure A.25.: Histogram of PSRR(V_{DD}) due to Process Variation at $V_{bias}=700\text{mV}$

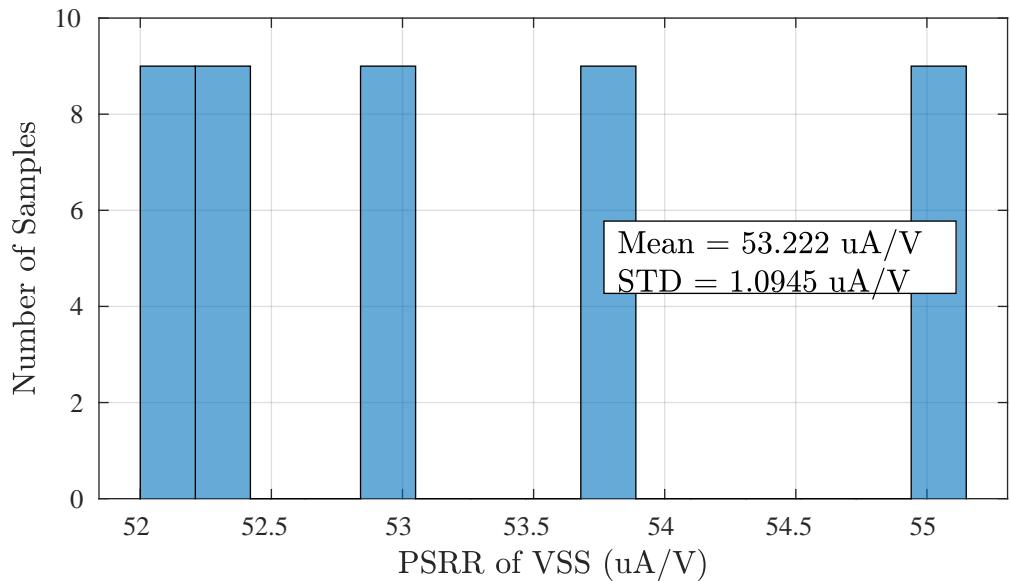


Figure A.26.: Histogram of PSRR(V_{SS}) due to Process Variation at $V_{bias}=700\text{mV}$

Process and Supply Variation - Overall System: Lowest V_{bias}

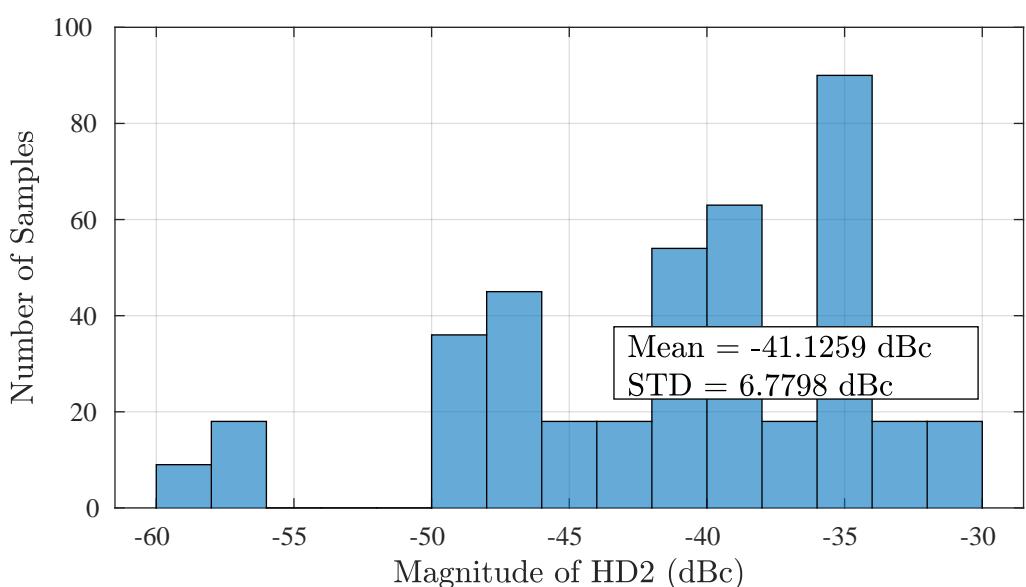


Figure A.27.: Histogram of HD2 due to Process and Supply Variation at $V_{bias}=150\text{mV}$

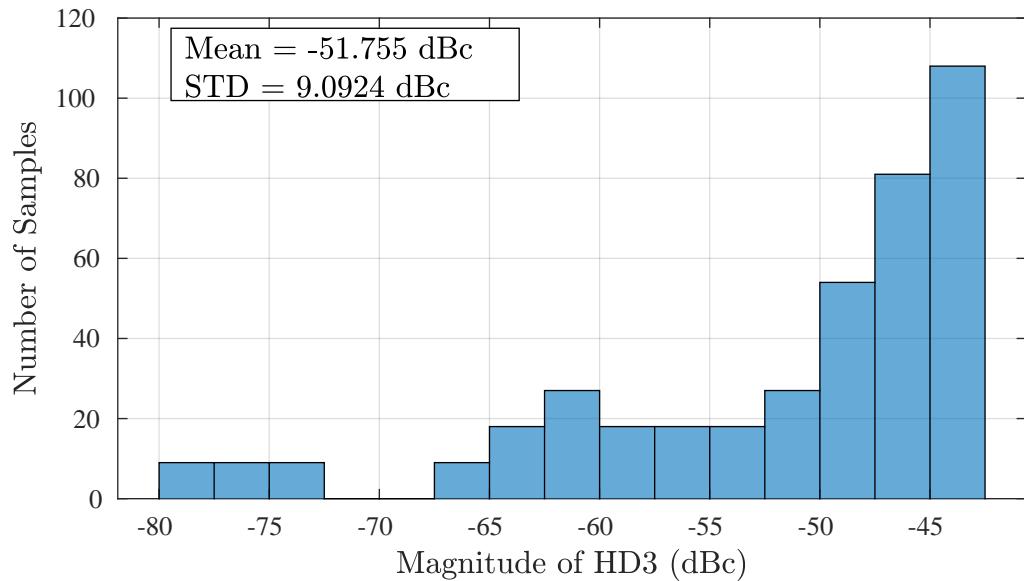


Figure A.28.: Histogram of HD3 due to Process and Supply Variation at $V_{bias}=150\text{mV}$

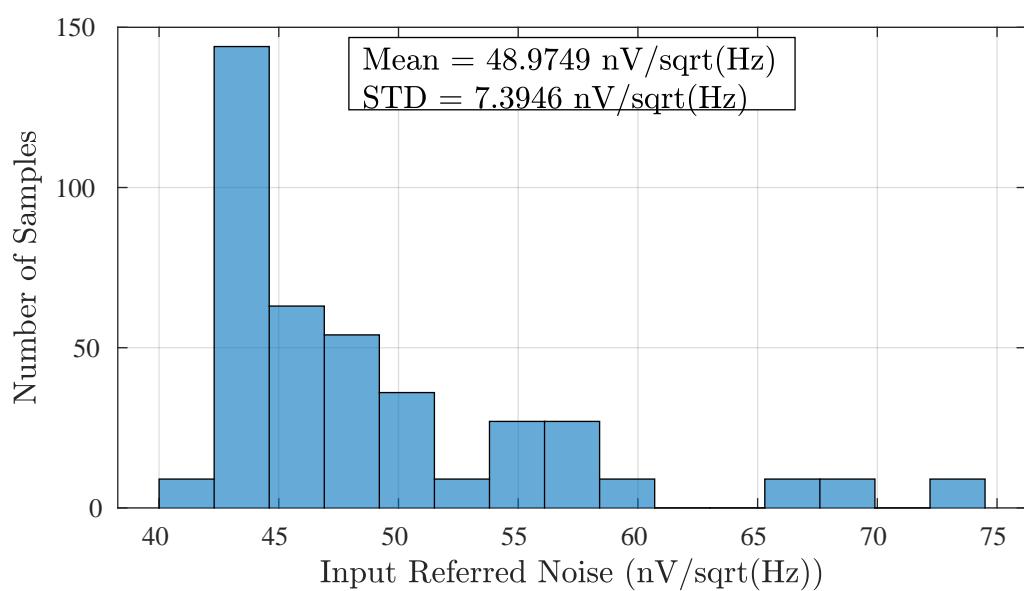


Figure A.29.: Histogram of Input Referred Noise due to Process and Supply Variation at $V_{bias}=150\text{mV}$

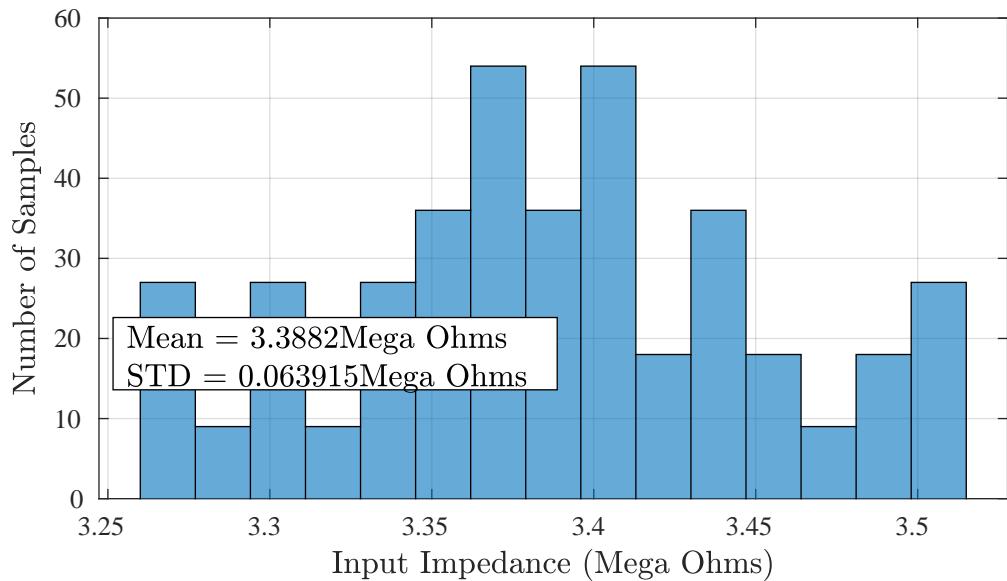


Figure A.30.: Histogram of Input Impedance due to Process and Supply Variation at $V_{bias}=150\text{mV}$

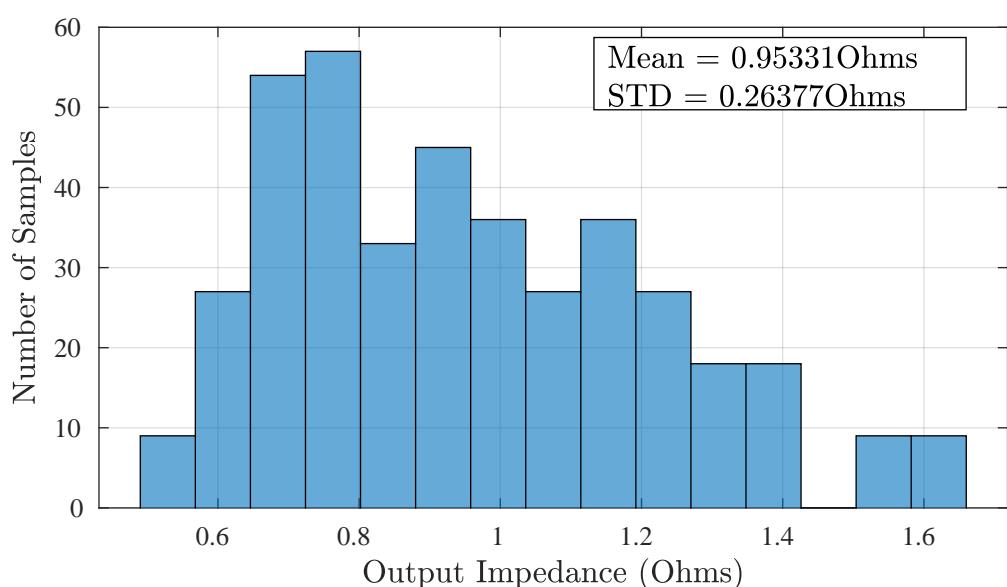


Figure A.31.: Histogram of Output Impedance due to Process and Supply Variation at $V_{bias}=150\text{mV}$

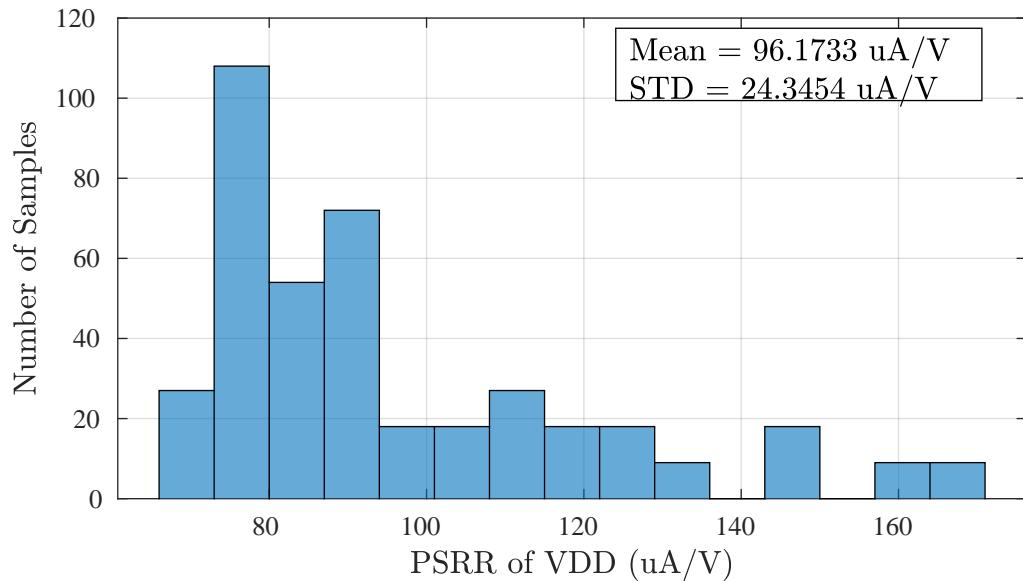


Figure A.32.: Histogram of PSRR(V_{DD}) due to Process and Supply Variation at $V_{bias}=150\text{mV}$

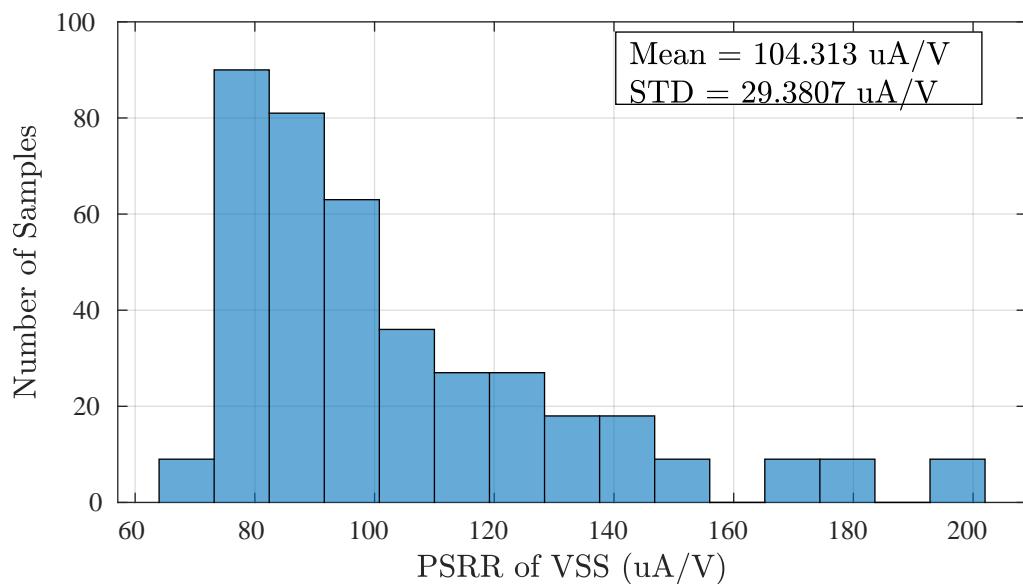


Figure A.33.: Histogram of PSRR(V_{SS}) due to Process and Supply Variation at $V_{bias}=150\text{mV}$

Process and Supply Variation - Overall System: Middle V_{bias}

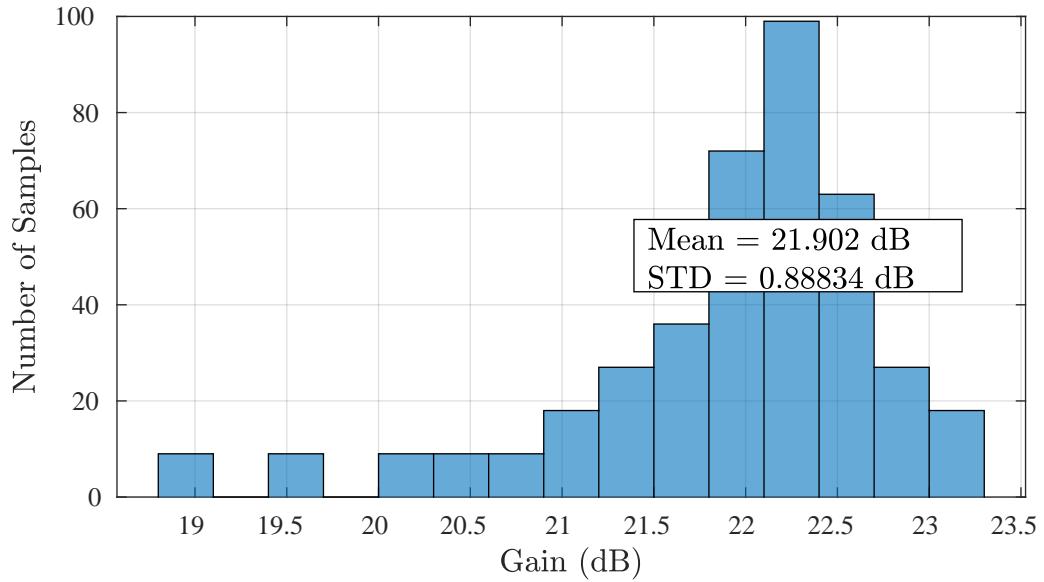


Figure A.34.: Histogram of System Gain due to Process and Supply Variation at $V_{bias}=400\text{mV}$

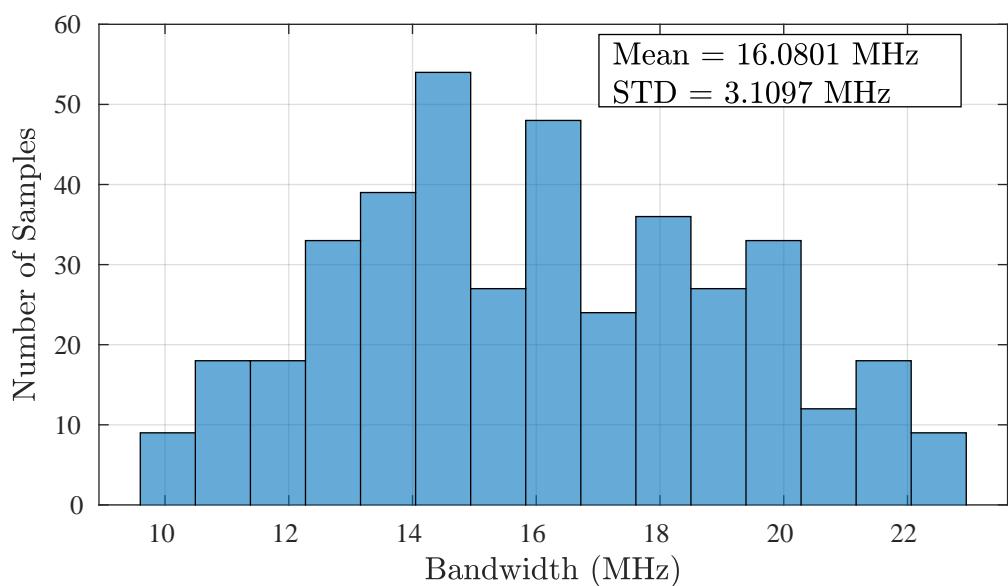


Figure A.35.: Histogram of System Bandwidth due to Process and Supply Variation at $V_{bias}=400\text{mV}$

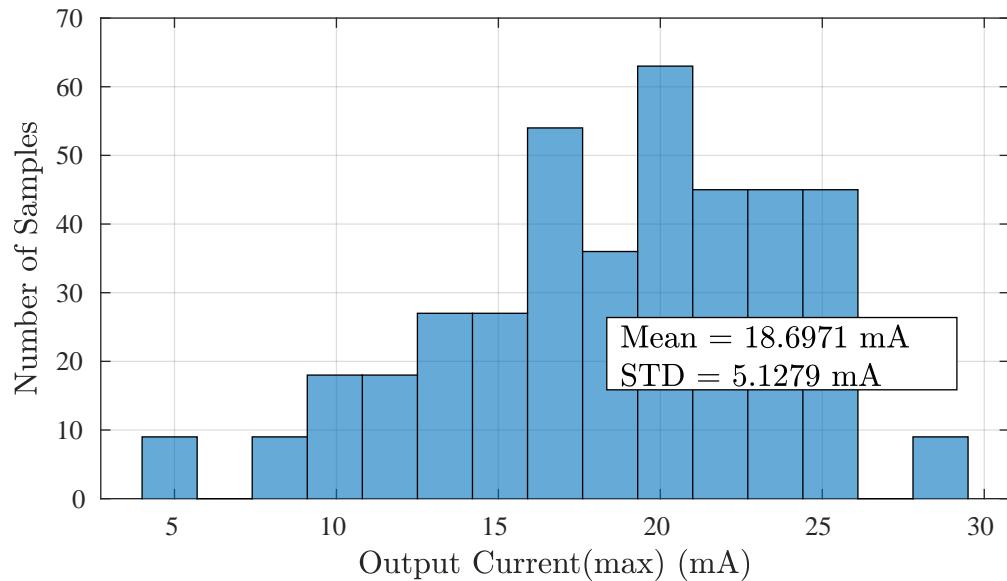


Figure A.36.: Histogram of Maximum Output Current due to Process and Supply Variation at $V_{bias}=400\text{mV}$

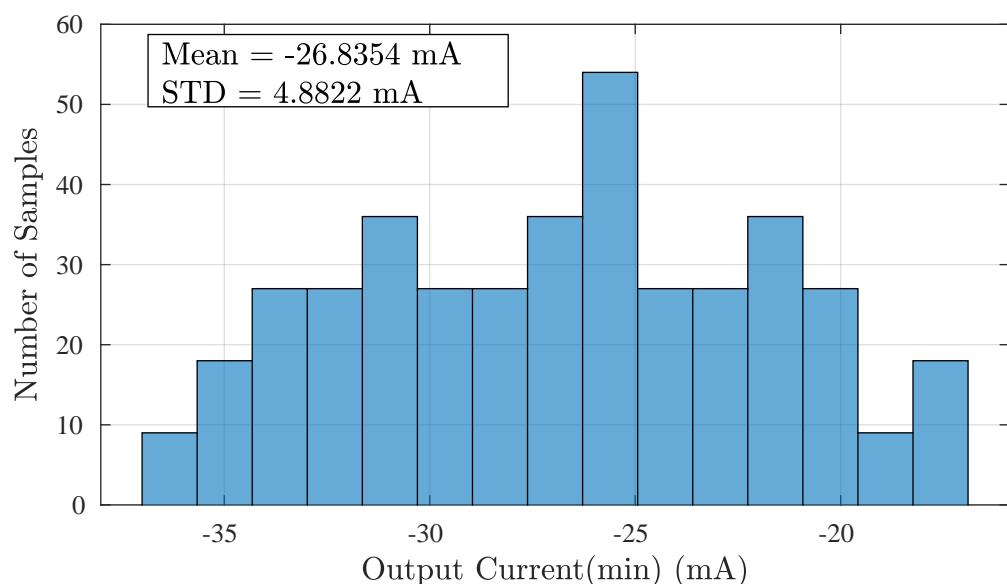


Figure A.37.: Histogram of Minimum Output Current due to Process and Supply Variation at $V_{bias}=400\text{mV}$

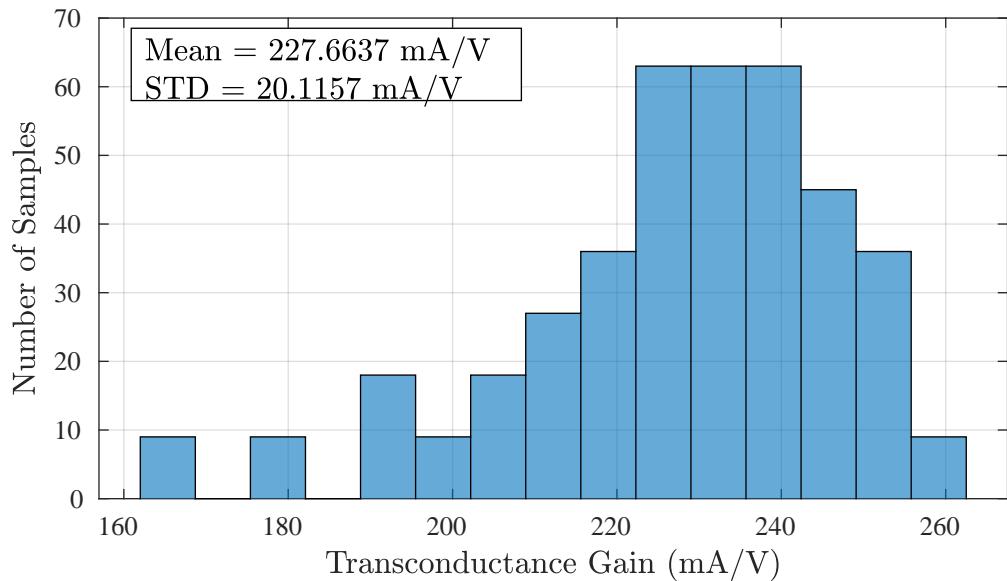


Figure A.38.: Histogram of Transconductance due to Process and Supply Variation at $V_{bias}=400mV$

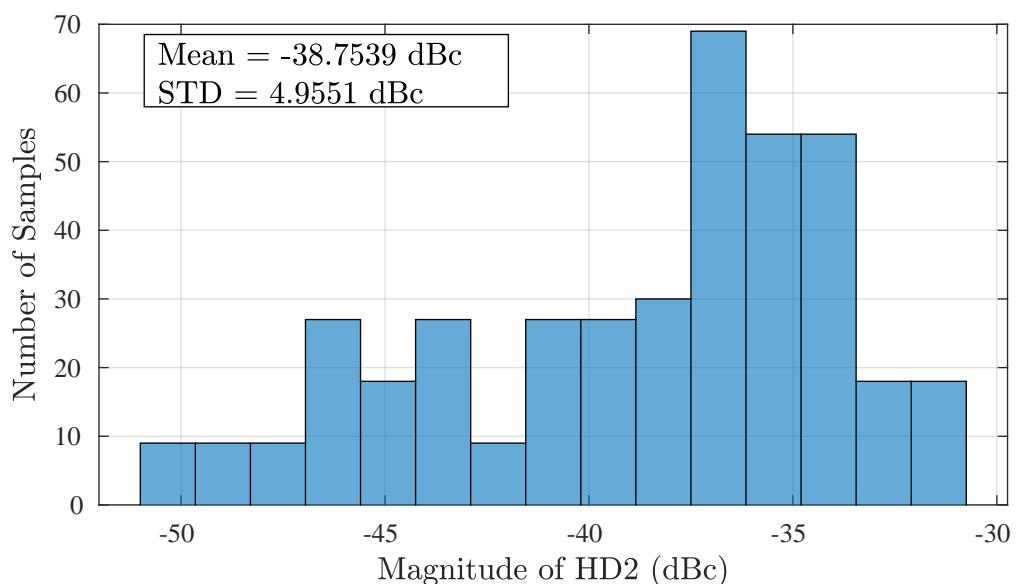


Figure A.39.: Histogram of HD2 due to Process and Supply Variation at $V_{bias}=400mV$

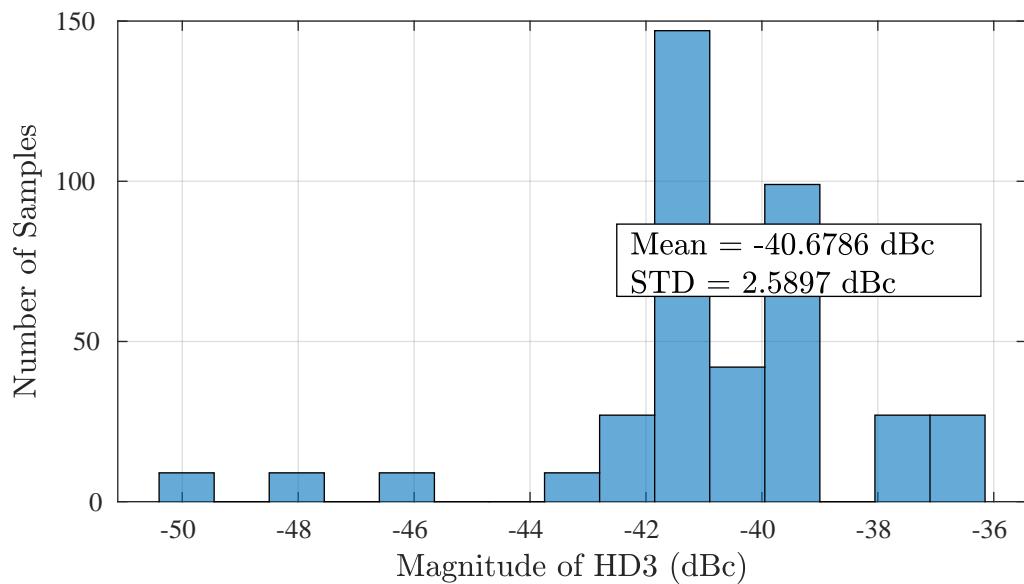


Figure A.40.: Histogram of HD3 due to Process and Supply Variation at $V_{bias}=400\text{mV}$

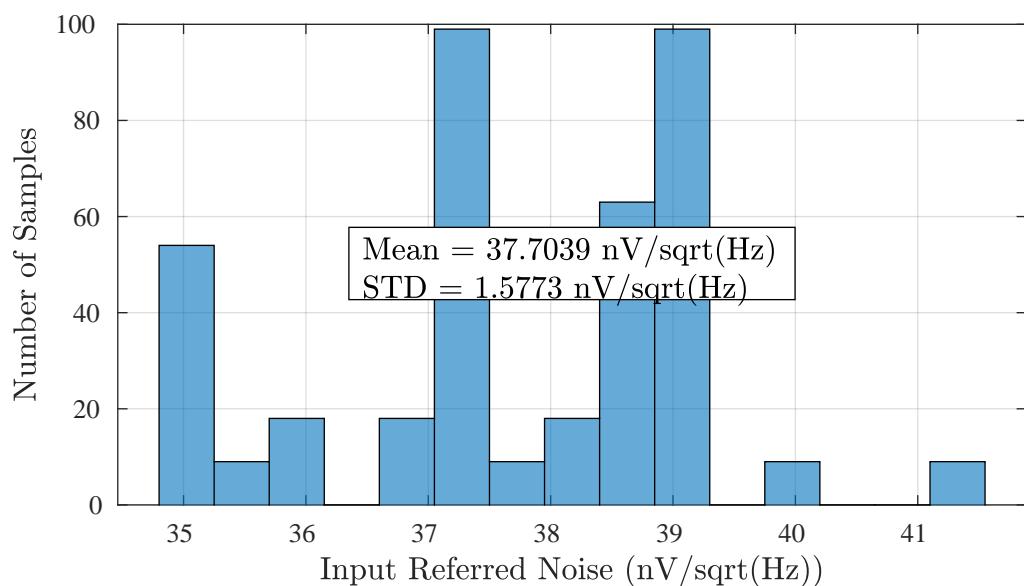


Figure A.41.: Histogram of Input Referred Noise due to Process and Supply Variation at $V_{bias}=400\text{mV}$

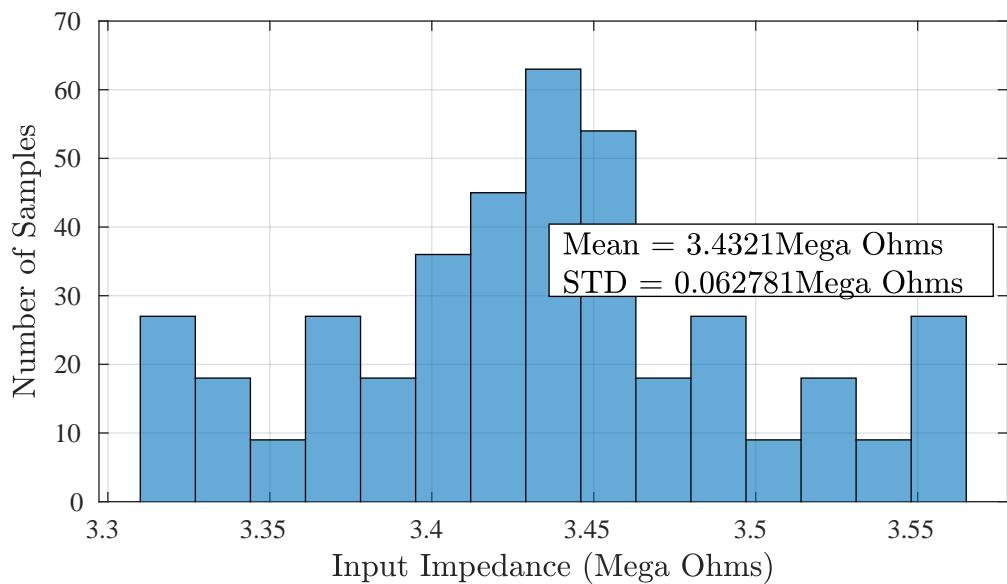


Figure A.42.: Histogram of Input Impedance due to Process and Supply Variation at $V_{bias}=400mV$

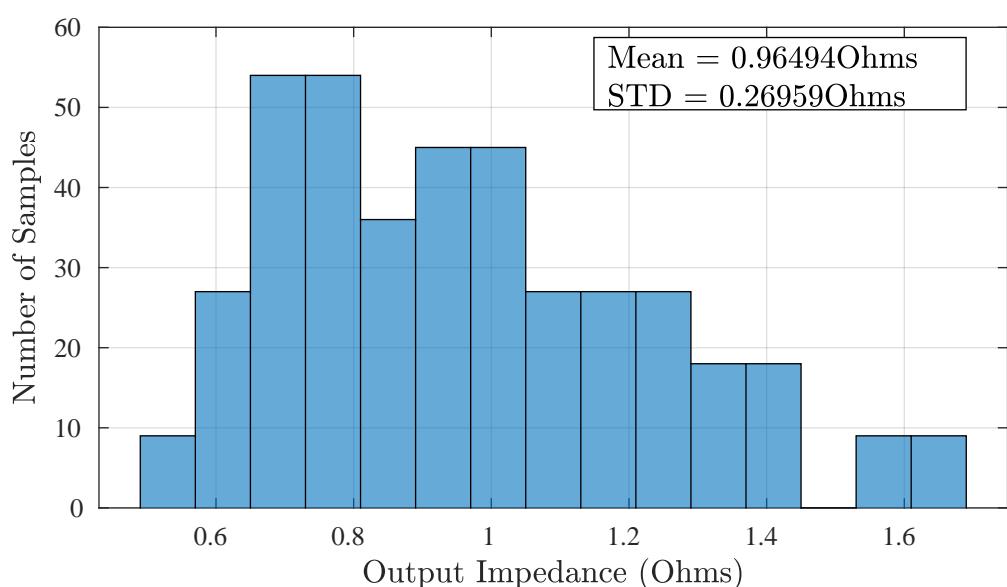


Figure A.43.: Histogram of Output Impedance due to Process and Supply Variation at $V_{bias}=400mV$

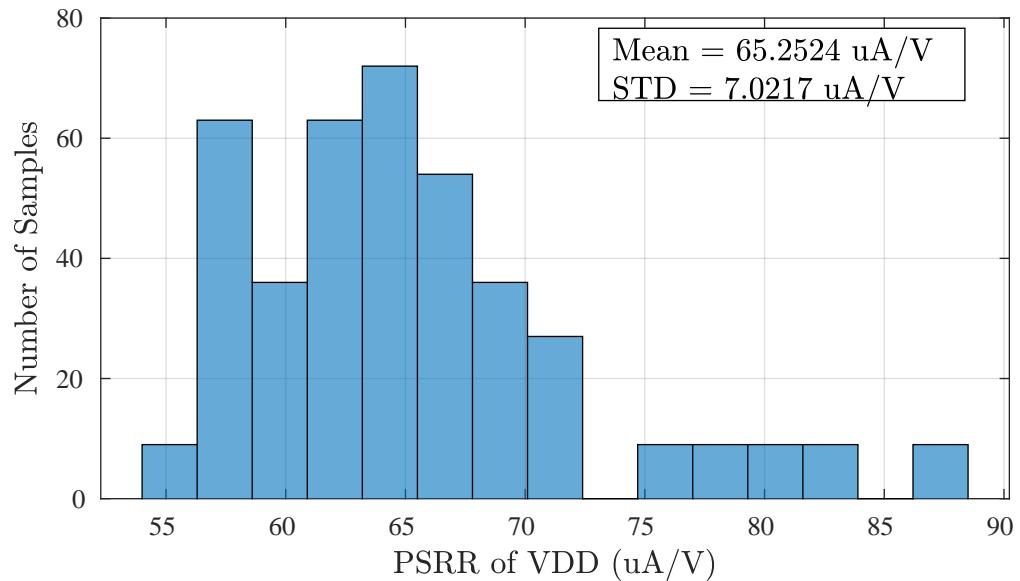


Figure A.44.: Histogram of PSRR(V_{DD}) due to Process and Supply Variation at $V_{bias}=400\text{mV}$

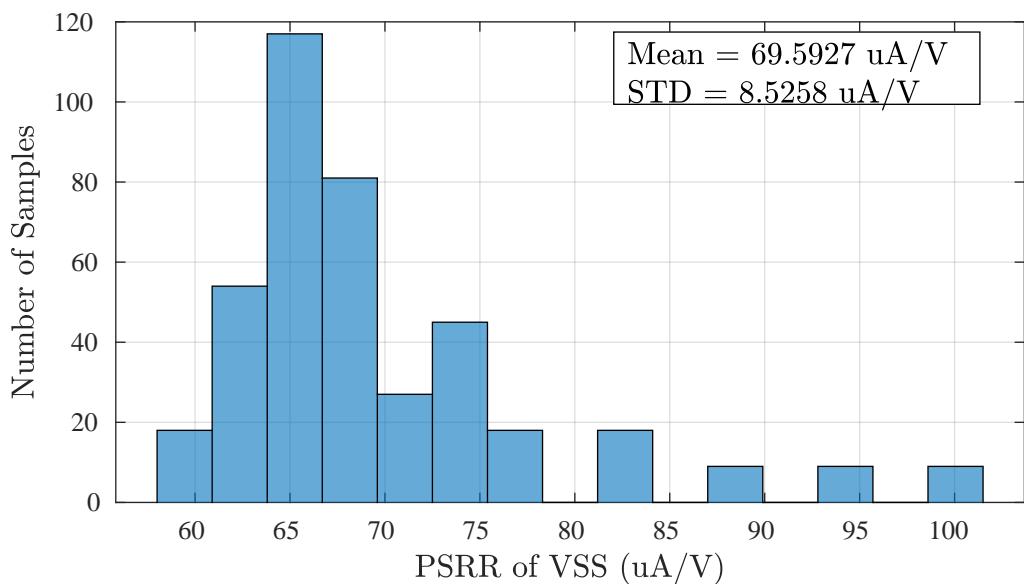


Figure A.45.: Histogram of PSRR(V_{SS}) due to Process and Supply Variation at $V_{bias}=400\text{mV}$

Process and Supply Variation - Overall System: Highest V_{bias}

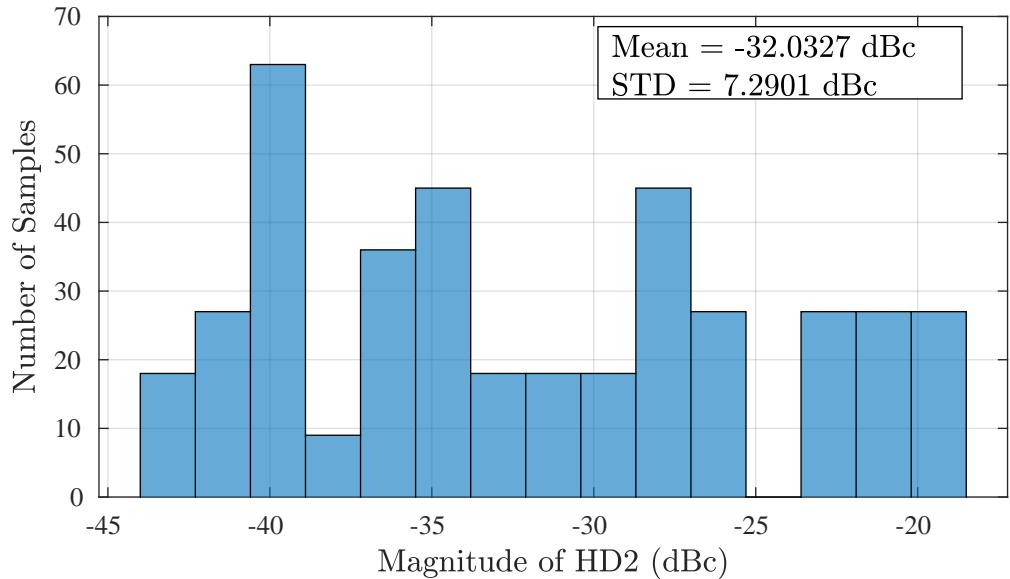
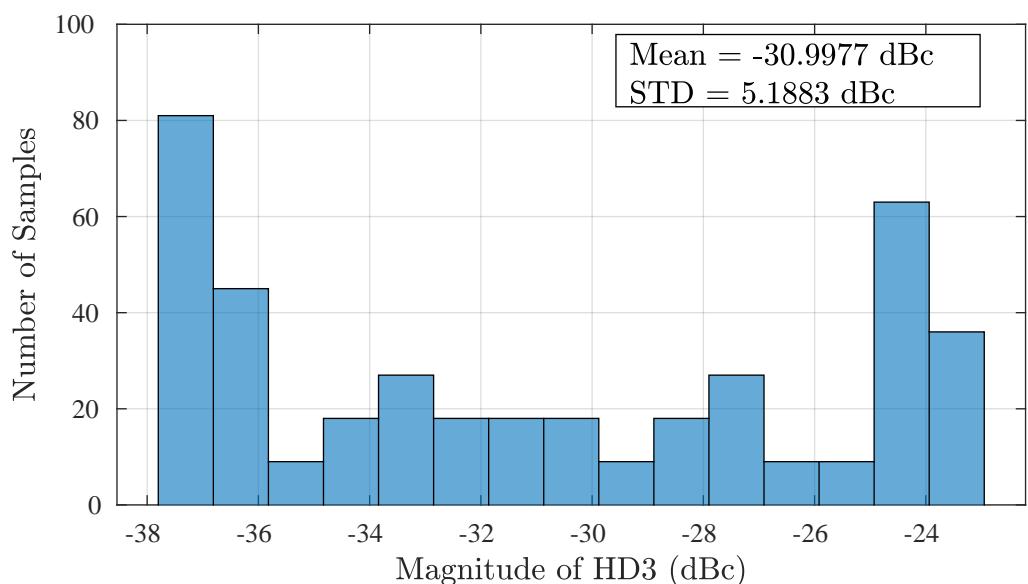


Figure A.46.: Histogram of HD2 due to Process and Supply Variation at $V_{bias}=700\text{mV}$



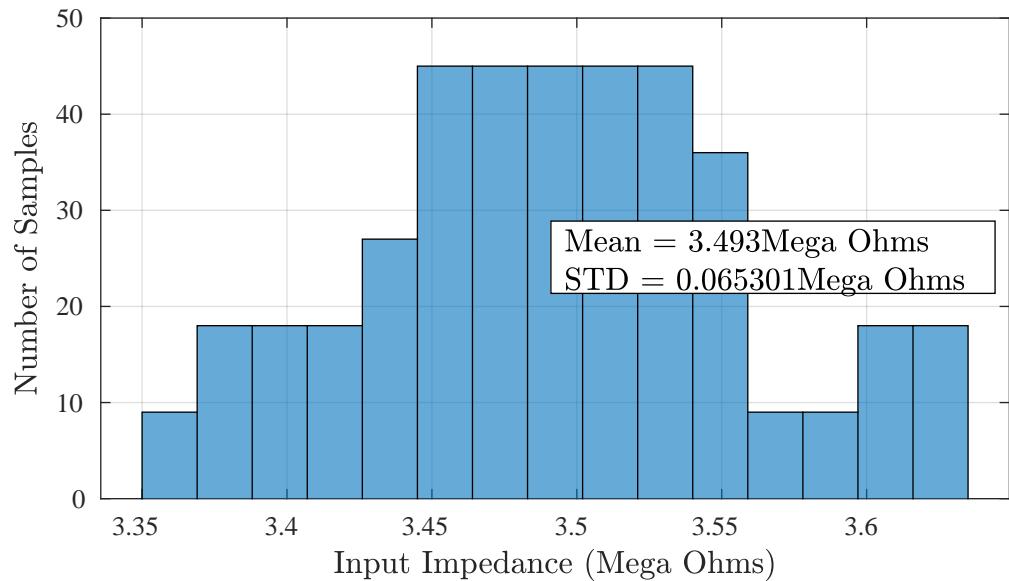


Figure A.48.: Histogram of Input Impedance due to Process and Supply Variation at $V_{bias}=700\text{mV}$

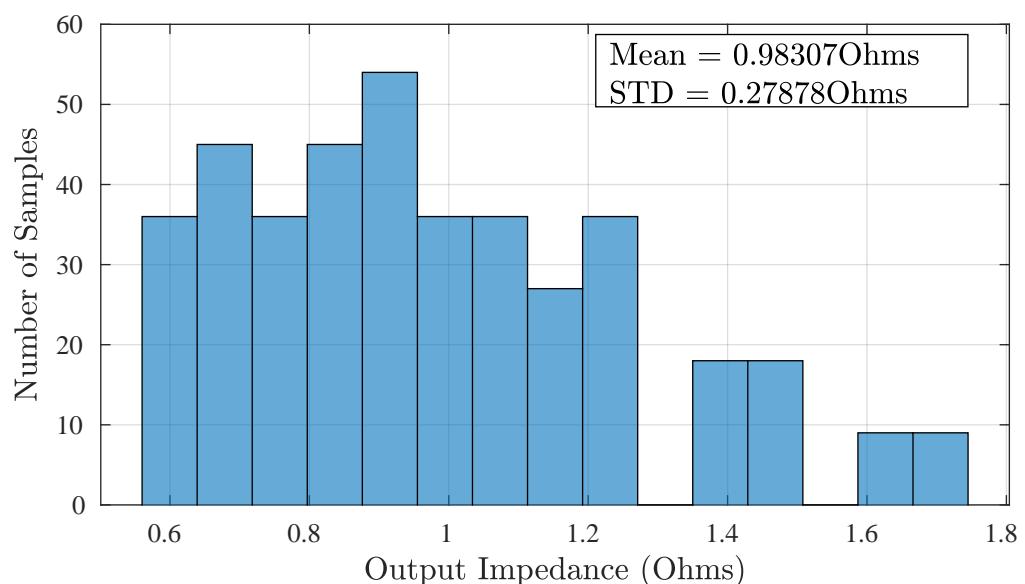


Figure A.49.: Histogram of Output Impedance due to Process and Supply Variation at $V_{bias}=700\text{mV}$

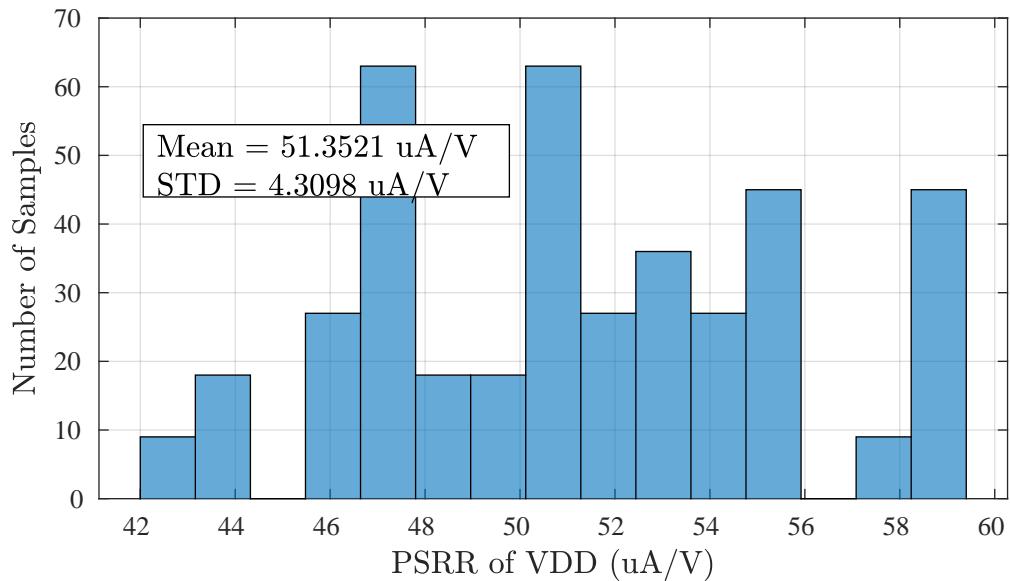


Figure A.50.: Histogram of PSRR(V_{DD}) due to Process and Supply Variation at $V_{bias}=700\text{mV}$

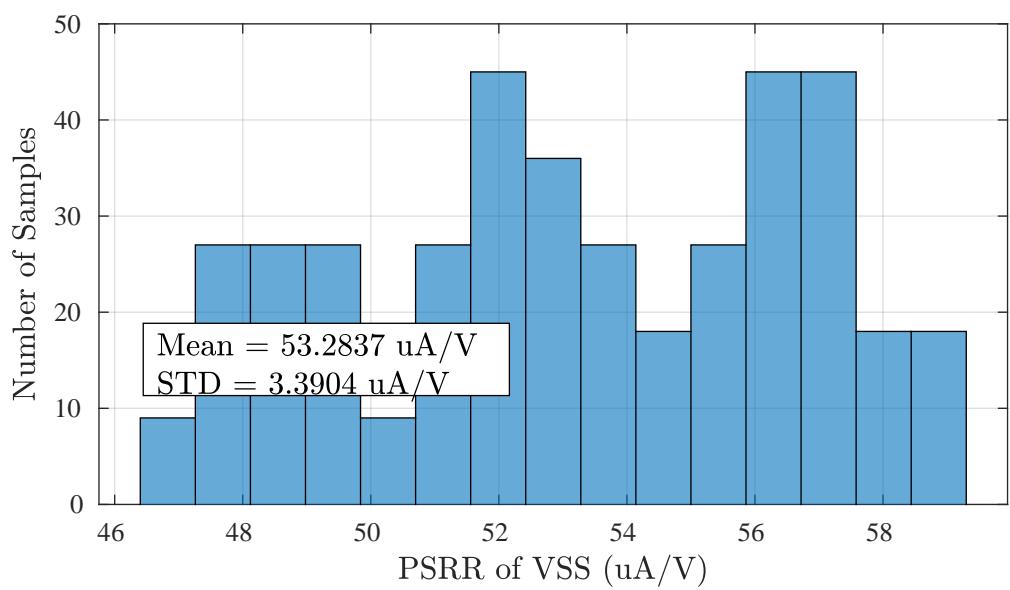


Figure A.51.: Histogram of PSRR(V_{SS}) due to Process and Supply Variation at $V_{bias}=700\text{mV}$

PVT: Overall - Middle V_{bias}

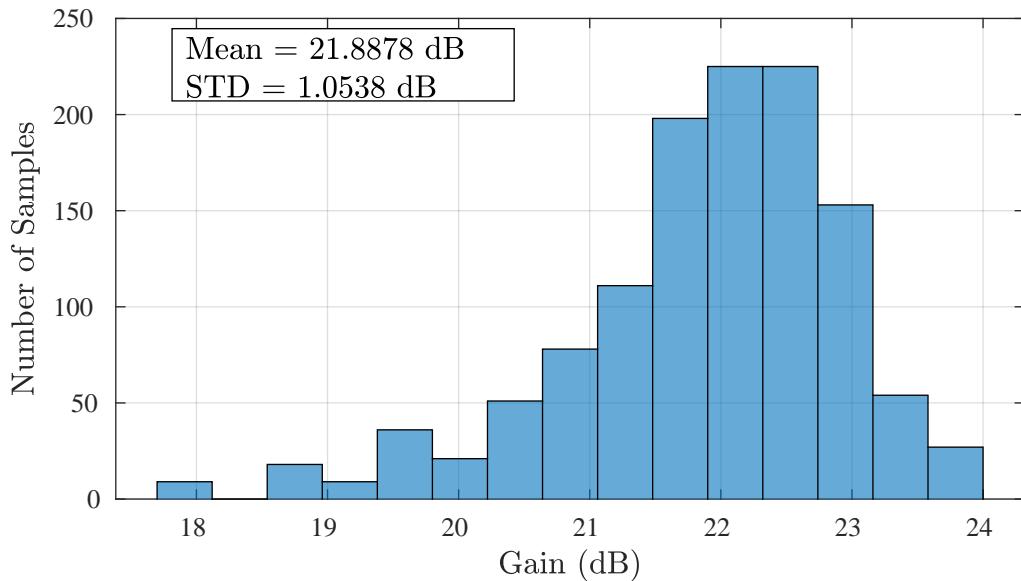


Figure A.52.: Histogram of System Gain due to PVT Variation at $V_{bias}=400\text{mV}$

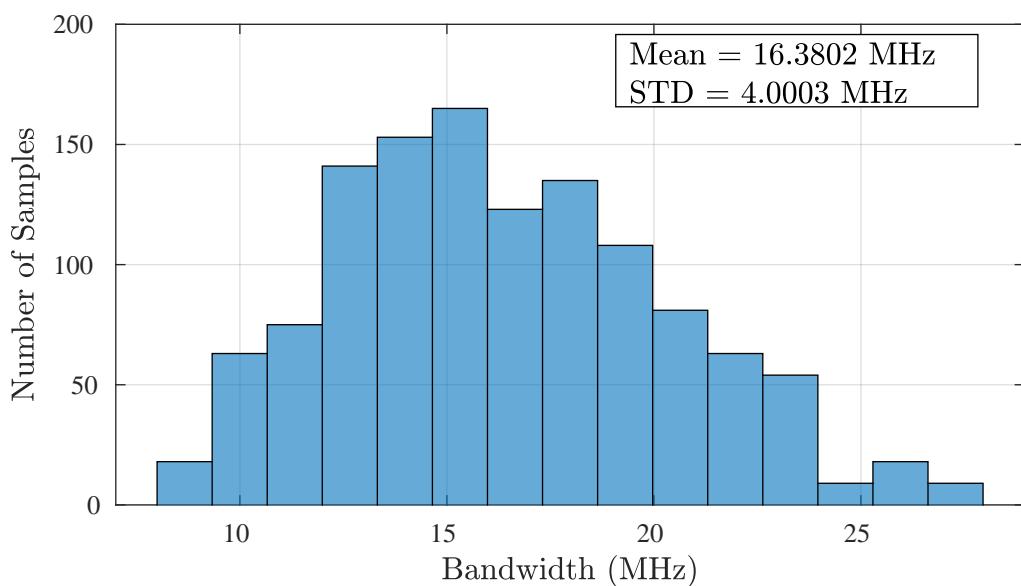


Figure A.53.: Histogram of System Bandwidth due to PVT Variation at $V_{bias}=400\text{mV}$

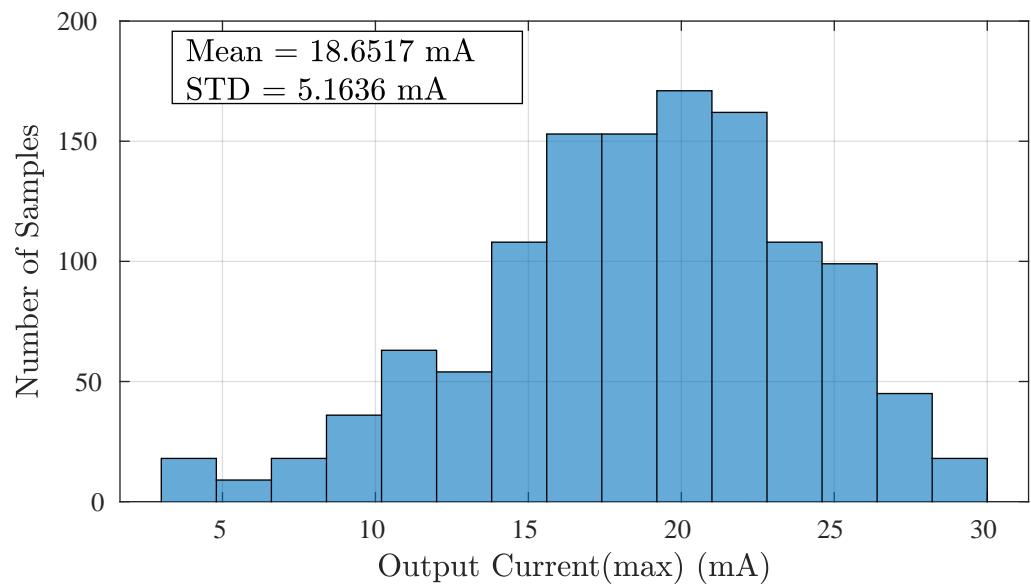


Figure A.54.: Histogram of Maximum Output Current due to PVT Variation at $V_{bias}=400\text{mV}$

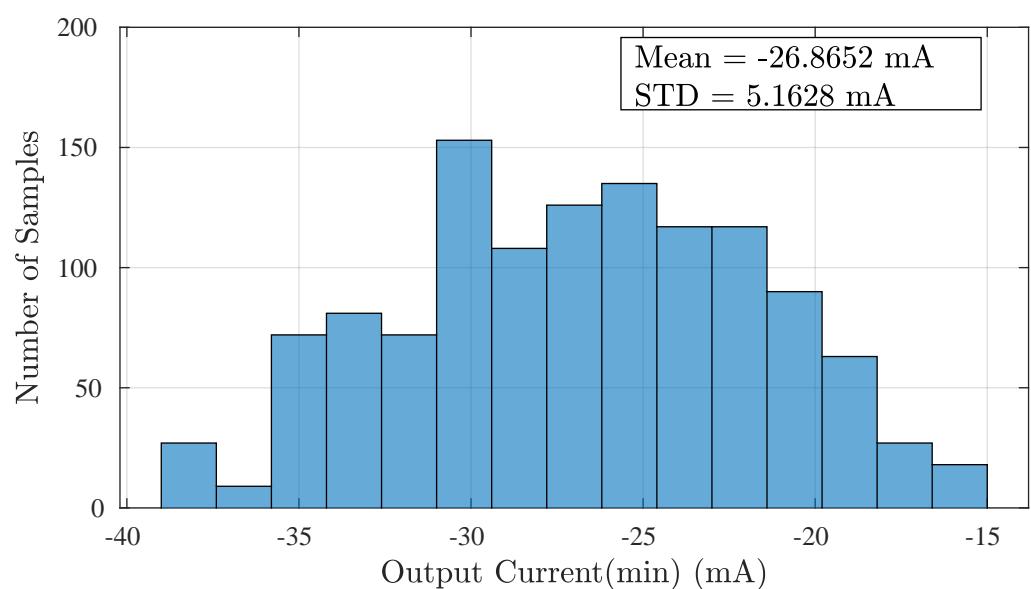


Figure A.55.: Histogram of Minimum Output Current due to PVT Variation at $V_{bias}=400\text{mV}$

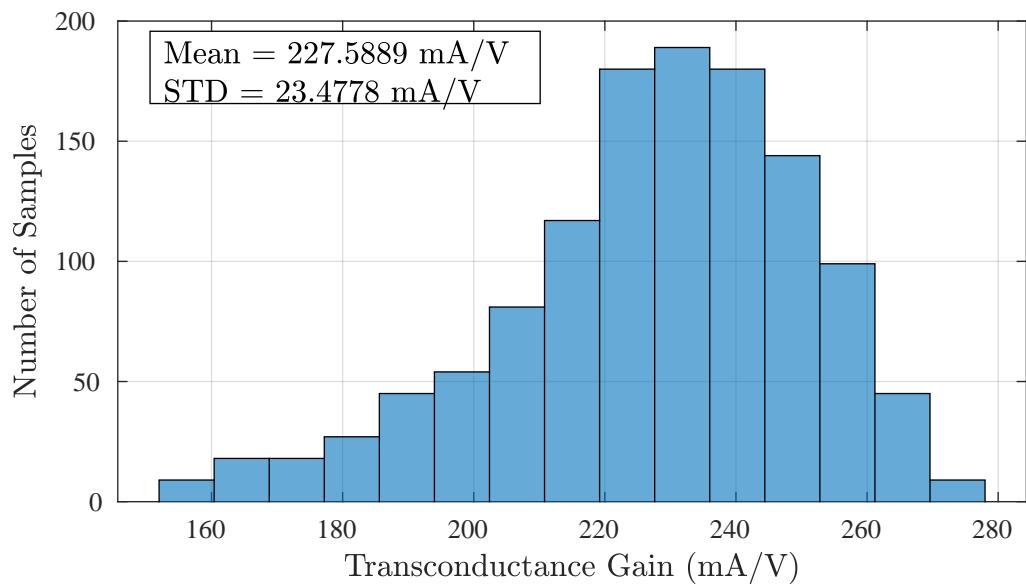


Figure A.56.: Histogram of Transconductance due to PVT Variation at $V_{bias}=400\text{mV}$

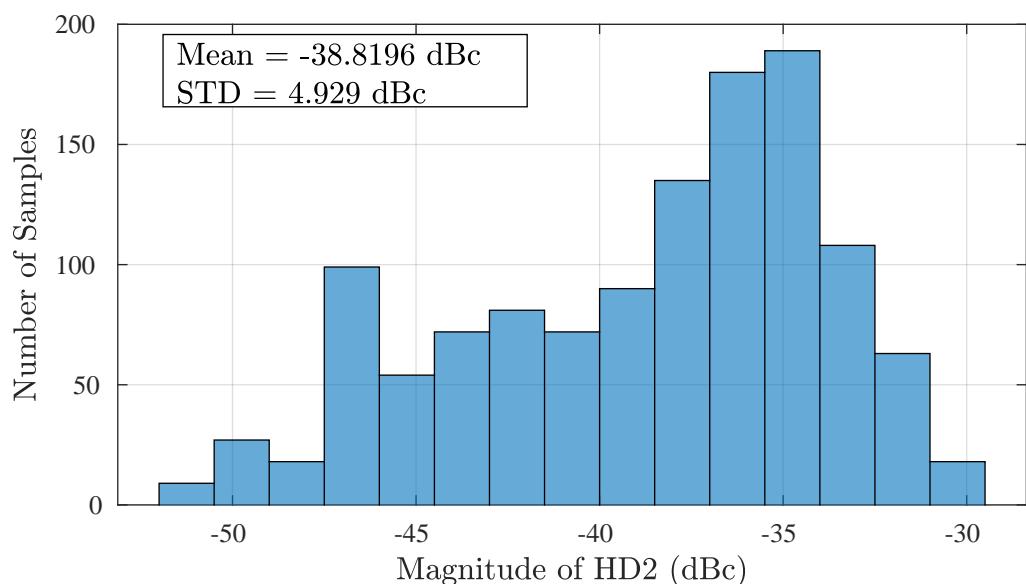


Figure A.57.: Histogram of HD2 due to PVT Variation at $V_{bias}=400\text{mV}$

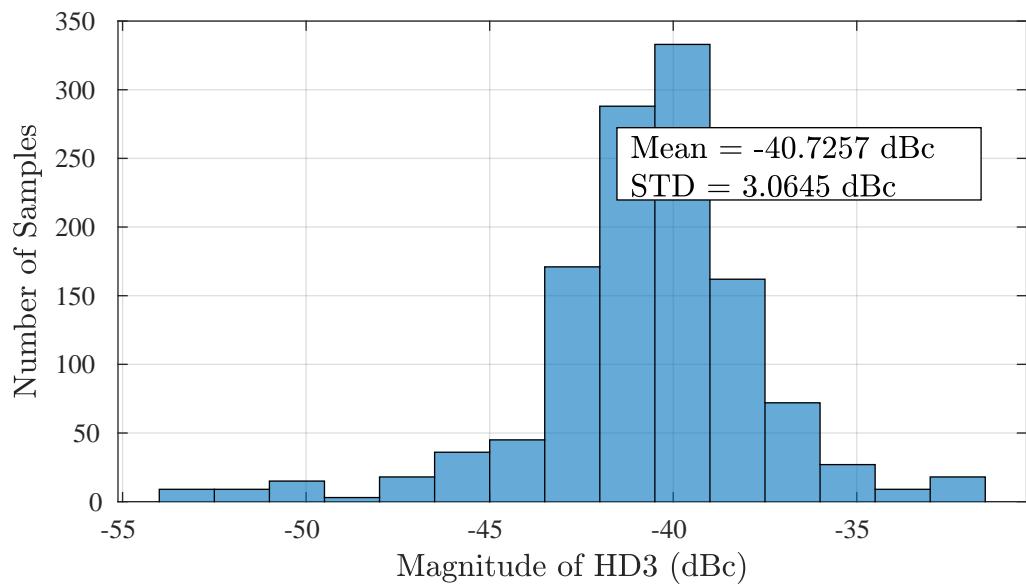


Figure A.58.: Histogram of HD3 due to PVT Variation at $V_{bias}=400\text{mV}$

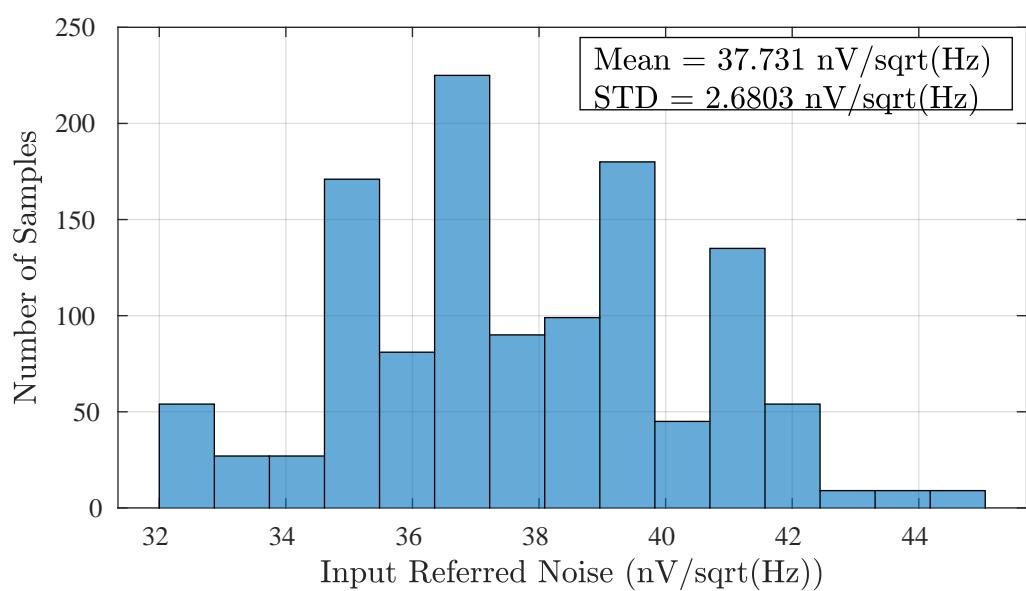


Figure A.59.: Histogram of Input Referred Noise due to PVT Variation at $V_{bias}=400\text{mV}$

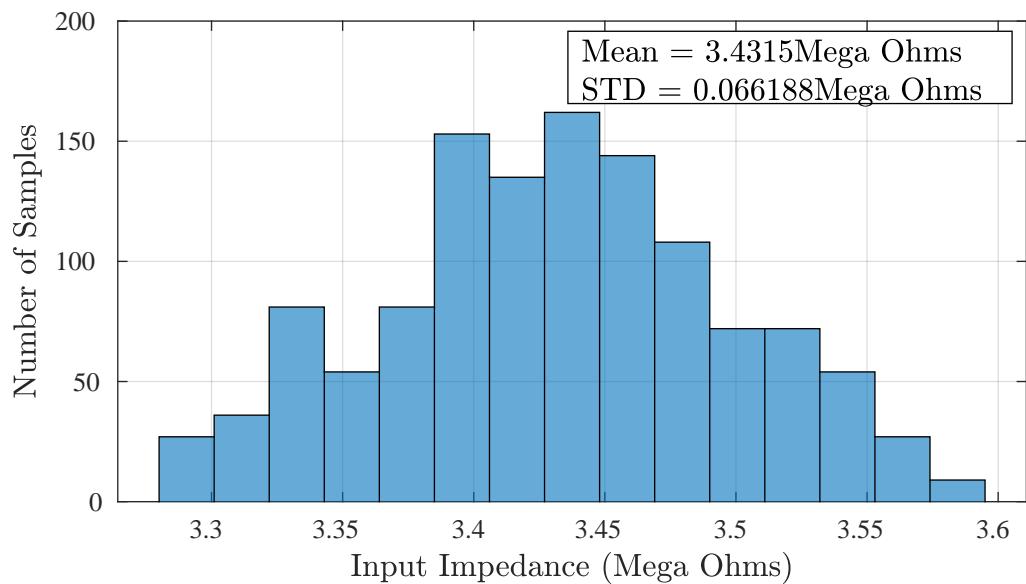


Figure A.60.: Histogram of Input Impedance due to PVT Variation at $V_{bias}=400\text{mV}$

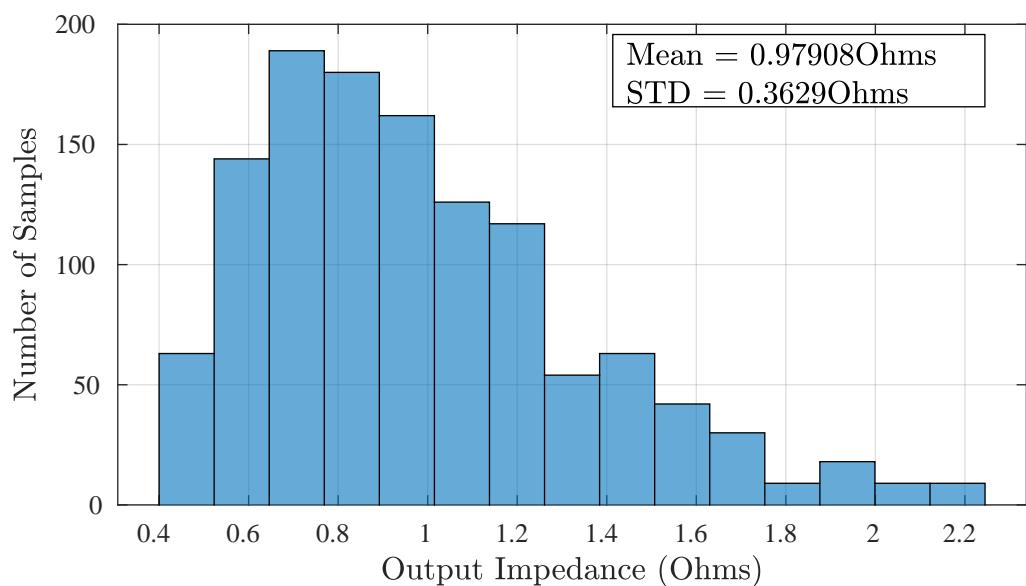


Figure A.61.: Histogram of Output Impedance due to PVT Variation at $V_{bias}=400\text{mV}$

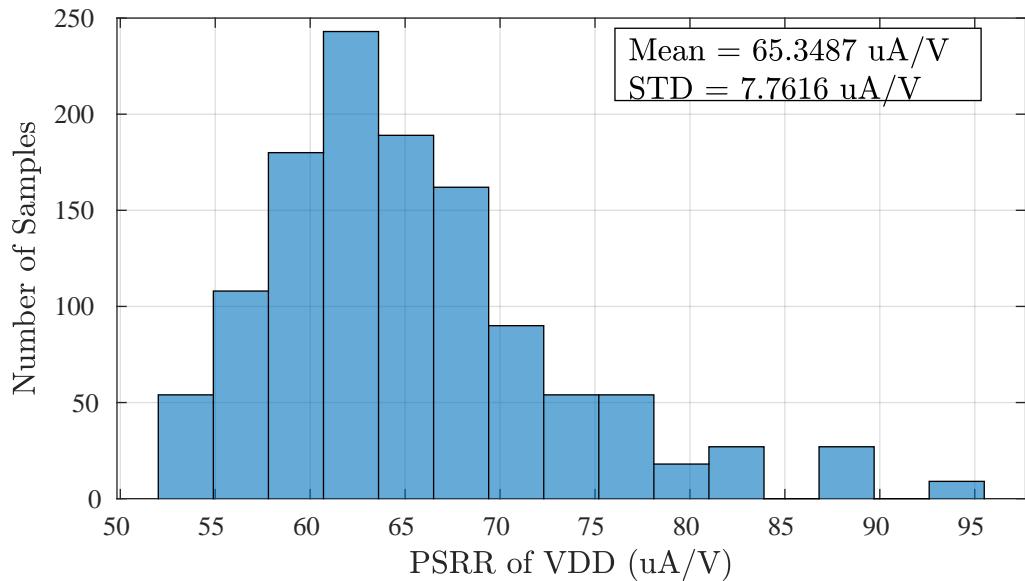


Figure A.62.: Histogram of PSRR(V_{DD}) due to PVT Variation at $V_{bias}=400\text{mV}$

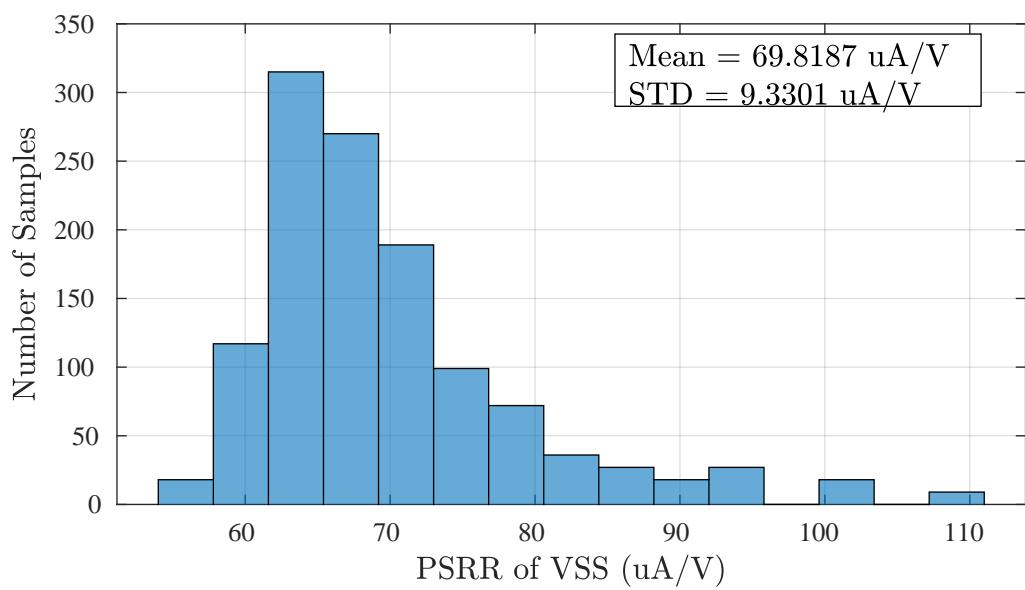


Figure A.63.: Histogram of PSRR(V_{SS}) due to PVT Variation at $V_{bias}=400\text{mV}$

A.2 Conventional OTA with PMOS Input

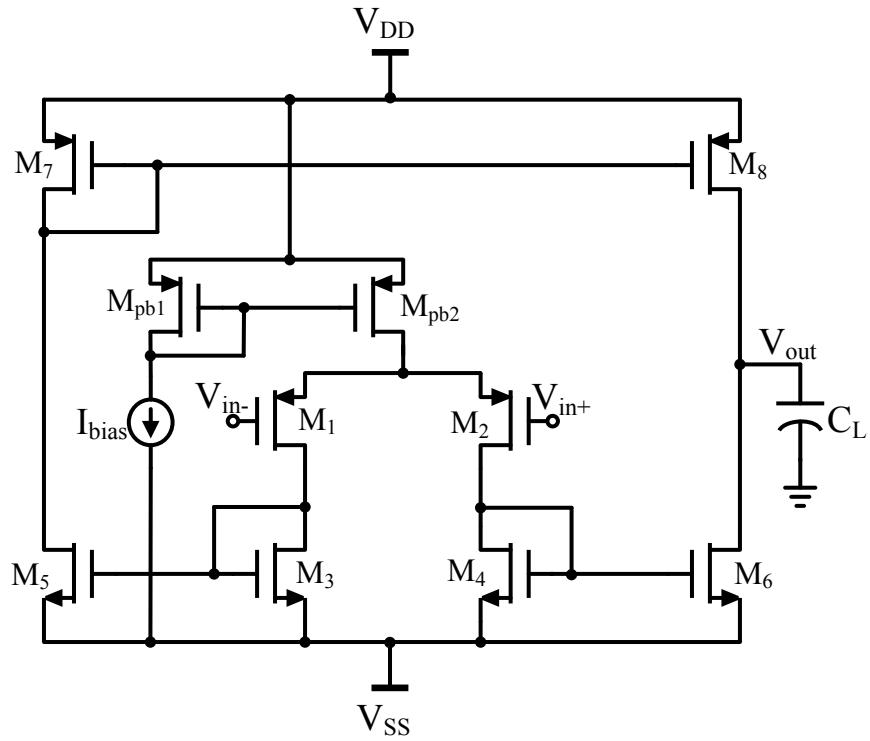


Figure A.64.: Conventional Current Mirror OTA with PMOS Input

A.3 3-stage Topology

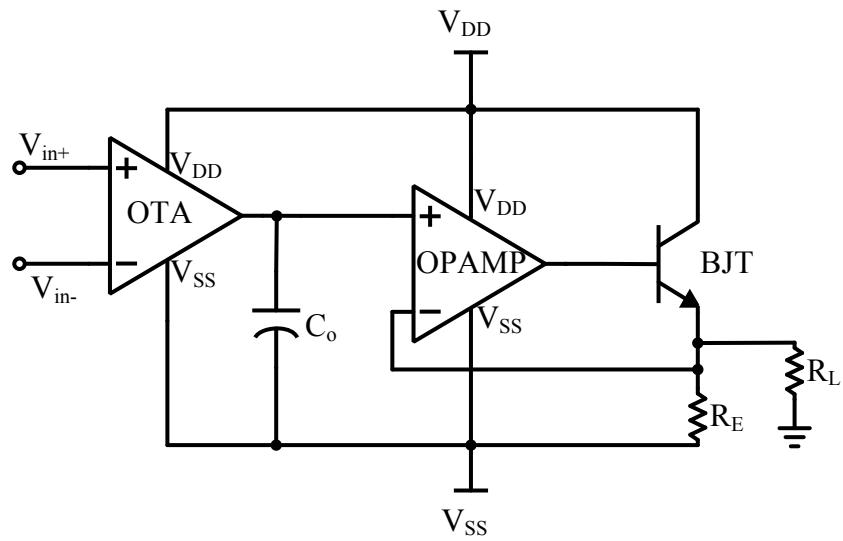


Figure A.65.: 3 stage design with an Emitter Follower

8 Bibliography

- [1] E. A. H. Azab and K. Hofmann, “R&D Accelerators: Novel-DC Beam Current Transformer.” 2015.
- [2] R. J. Baker, *CMOS: circuit design, layout, and simulation*, vol. 1. John Wiley & Sons, 2008.
- [3] A. J. Poitzsch, “A High Voltage, High Current, Low Error Operational Amplifier with Novel Features,” Master’s thesis, Massachusetts Institute of Technology, 2014.
- [4] J.-P. Colinge *et al.*, *FinFETs and other multi-gate transistors*, vol. 73. Springer, 2008.
- [5] E. Soliman, K. Hofmann, H. Reeg, and M. Schwickert, “Sensor studies for dc current transformer application,” tech. rep., GSI Helmholtz Centre for Heavy Ion Research, 2014.
- [6] E. Soliman, H. Reeg, M. Schwickert, and K. Hofmann, “A novel dc current transformer using magneto-resistance sensors for fair,” tech. rep., IES Institute, TU Darmstadt, 2014.
- [7] T. Instruments, “Wide bandwidth operational transconductance amplifier opa861 [z],” *Texas Instruments*, 2004.
- [8] “XT018 SOI Technology Specification,” tech. rep., XFB, 2017.
- [9] G. Celler and S. Cristoloveanu, “Frontiers of silicon-on-insulator,” *Journal of Applied Physics*, vol. 93, no. 9, p. 4955, 2003.
- [10] T. Romanko and B. Clegg, “Soi eases radiation-hardened asic designs,” *Military and Aerospace Designline*, 2005.
- [11] G. C. Messenger, “Radiation Hardening,” *Journal of Applied Physics*, 2014.
- [12] J. R. Schwank, V. Ferlet-Cavrois, M. R. Shaneyfelt, P. Paillet, and P. E. Dodd, “Radiation effects in soi technologies,” *IEEE Transactions on Nuclear Science*, vol. 50, pp. 522–538, June 2003.
- [13] M. J. Cabebe, C. D. Gallego, J. R. Hizon, and L. Alarcon, “Design tradeoffs in a 0.5v 65nm cmos folded cascode ota,” in *IEEE 2013 Tencon - Spring*, pp. 293–297, April 2013.
- [14] O. A. Abu-El-ela, A. A. Aldaly, Y. Abd-El-azim, and H. A. Omran, “Design automation of a fully differential switched capacitor amplifier using a telescopic cascode ota,” in *2018 35th National Radio Science Conference (NRSC)*, pp. 385–392, March 2018.
- [15] M. L. Holmes, “Application of local common mode feedback techniques to enhance slew rate and gain-bandwidth of CMOS Operational Amplifiers,” Master’s thesis, New Mexico State University, 2002.
- [16] S. Pourashraf, J. Ramirez-Angulo, A. J. Lopez-Martin, and R. Gonzalez-Carvajal, “A super class-ab ota with high output current and no open loop gain degradation,” in *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 815–818, August 2017.

- [17] S. Pourashraf, J. Ramirez-Angulo, A. Roman-Loera, A. J. Lopez-Martin, A. Diaz-Sanchez, and R. G. Carvajal, "High current efficiency class-ab ota with high open loop gain and enhanced bandwidth," *IEICE Electronics Express*, vol. 14, no. 17, pp. 20170719–20170719, 2017.
- [18] B. Razavi, *Design of analog CMOS integrated circuits*. McGraw Hill International, 2005.
- [19] D. Foty, D. Binkley, and M. Bucher, "Gm/Id-based MOSFET Modeling and Modern Analog Design," *MIXDES, Wroclaw, Poland*, 2002.
- [20] F. Silveira, D. Flandre, and P. Jespers, "A g/sub m//i/sub d/based methodology for the design of cmos analog circuits and its application to the synthesis of a silicon-on-insulator micropower ota," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 9, pp. 1314–1319, 1996.
- [21] B. Murmann, *Systematic Design of Analog Cmos Circuits-Using Pre-computed Lookup Table*. Cambridge University Press, 2017.
- [22] "A Basic Introduction to the Gm ID-Based Design," tech. rep., Scribd.
- [23] T. Instruments, "Operational transconductance amplifier (ota) and buffer. texas instruments, sbos331c-june 2005-revised august 2008."
- [24] L. T. . Datasheets, "100mhz current feedback amplifier with dc gain control. linear technology corporation, 2012."
- [25] H. Veldandi and R. A. Shaik, "A 1-v high-gain two-stage self-cascode operational transconductance amplifier," in *2017 Innovations in Power and Advanced Computing Technologies (i-PACT)*, pp. 1–4, April 2017.
- [26] S. I. Singh, "Design of low-voltage cmos two-stage operational transconductance amplifier," in *Electrical, Electronics, Communication, Computer, and Optimization Techniques (ICEECCOT), 2017 International Conference on*, pp. 248–252, IEEE, 2017.
- [27] B. K. Thandri and J. Silva-Martínez, "A robust feedforward compensation scheme for multistage operational transconductance amplifiers with no miller capacitors," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 2, pp. 237–243, 2003.
- [28] H. J. Motlak and S. N. Ahmad, "A novel design technique of one stage cmos ota for high frequency applications," *Frequenz*, vol. 61, no. 7-8, pp. 182–188, 2007.
- [29] U. of Minnesota Twin Cities, "Basic opamp design and compensation."
- [30] IES Institute, TU Darmstadt, *Miller Compensation Op Amp Design*, 2017.