

Design and Implementation of a Radiation Hardened High Output Current Transconductance Amplifier

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Abstract



Zusammenfassung



Acknowledgments



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1 Introduction

1.1 Novel DC Current Transformer

1.2 Specification

1.3 Technology

2 Theory

2.1 The Operational Transconductance Amplifier

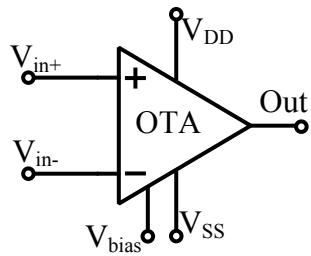


Figure 2.1.: Symbol of an OTA

2.1.1 Different Topologies

Conventional Current Mirror OTA

Super Class AB OTA

Folded Cascode OTA

2.2 The Opeartional Amplifier

2.2.1 Miller Compensation OP AMP

2.2.2 OP AMP as a Voltage Buffer

2.3 The Gm/Id Methodology



3 Design and Implementation

3.1 OTA Design

The first stage of the design is the Operational Transconductance Amplifier. This stage uses bipolar power supply of 2.5V and -2.5V. Two separate designs - OTA with PMOS Differential pair and OTA with NMOS Differential pair were designed and simulated in Cadence to get a good understanding of the circuit parameters and how the differential pair impact them.

Generally, amplifiers with PMOS transistors used as differential input offer high linearity, low flicker ($1/f$) noise. A possible reason to choose PMOS transistors as a differential pair comes from the necessity to reduce the influence of the substrate noise. The two transistors are in an N-well and the well is connected to the supply voltage that any substrate interference coupled via the parasitic capacitance to substrate is decoupled to the VDD line. P-channels typically have less flicker noise ($1/f$ noise) caused by the carriers randomly entering and leaving traps introduced by defects near the semiconductor surface. Since the majority charge carriers are holes in PMOS, there are less potential to be trapped in surface states.

Having stated all these facts, NMOS input transistors would be better in terms of transconductance gain, and hence thermal noise and the bandwidth of the amplifier. An important fact considered in the selection of the type of differential pair is that the OTA in this system is being used in an open loop. This means that the gain of the OTA has to be limited in order to avoid saturation at the crests and troughs at the output of the OTA.

PMOS transistors exhibit their low noise behaviour due to the fact that PMOS transistors are usually bigger (higher W/L ratio) than an NMOS pair. Since we need a small open loop gain, we cannot afford to have big transistors at the input that cause the output to saturate. Along with this, it was also seen that, the range of bias currents needed to obtain a similar range of voltage swing was much wider in case of PMOS than NMOS. Since this indirectly results in a high power dissipation in the 1st stage itself, it was concluded to use the NMOS based design as part of this Thesis work.

3.1.1 Schematic

Figure.3.1 shows the schematic of the OTA used as part of this Thesis. As mentioned above, the differential amplifier is formed by the NMOS pair. The bias current I_{bias} to the differential pair is provided by the current mirror formed by M_{nB1} and M_{nB2} which is in turn controlled by the PMOS transistor M_9 whose gate voltage V_{bias} is the programmable variable of the OTA and the entire system. This bias voltage is inversely proportional to the bias current flowing through each branch of the OTA.

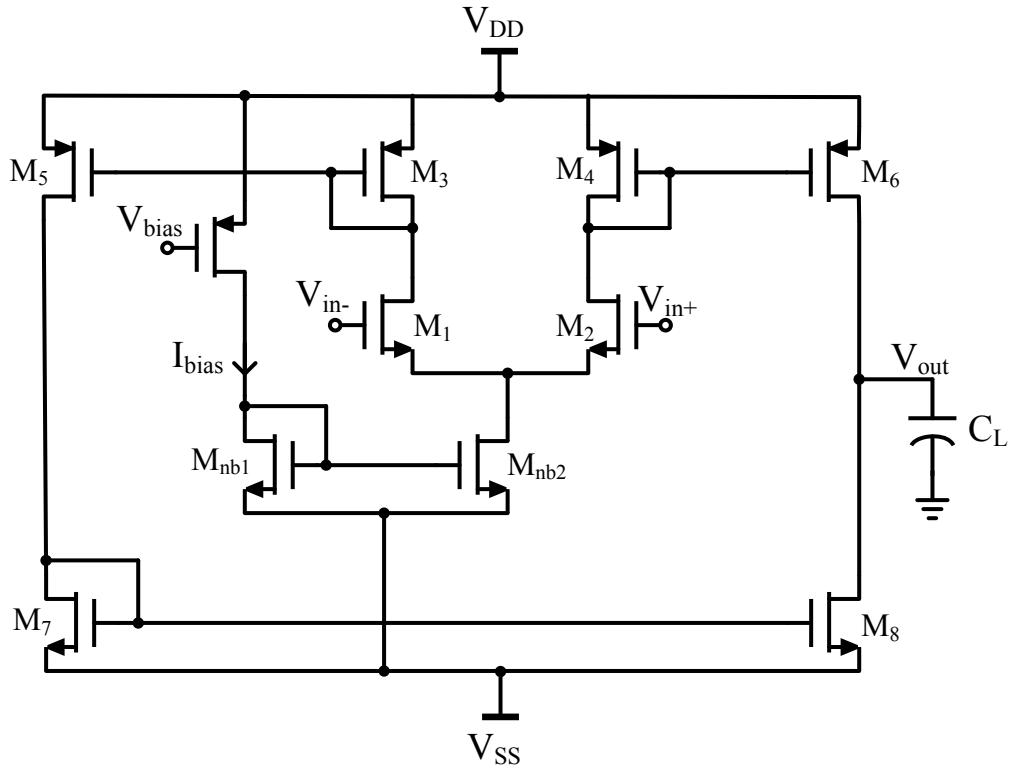


Figure 3.1.: Schematic of the OTA Designed

Transistor	Width	Length	Multiplier
M1	8u	500n	5
M2	8u	500n	5
M3	35u	500n	1
M4	35u	500n	1
M5	28u	500n	3
M6	35u	500n	3
M7	35u	500n	18
M8	33u	500n	18
M9	10u	500n	4
MnB1	20u	500n	8
MnB2	20u	500n	8

Table 3.1.: Dimensions of the Transistors of the designed OTA

From the Table.3.1, it can be seen that the current mirror gain for the current mirrors formed by M_3 , M_5 and M_4 , M_6 is 3. It can also be noted that the transistors M_5 and M_8 are not symmetric with respect to their counterparts. This is designed so to make sure the DC bias point at the output of the OTA is close to 0V, which is the mid point of V_{DD} and V_{SS} . Changing the bias current of an amplifier, will automatically change the DC bias point at its output. Since we are using the OTA as a programmable block, it is important to have an output which is symmetric over 0. Even though it is not entirely possible,

making these two transistors a little assymetric or uneven would close the gap between the bias points for highest and lowest bias currents.

3.1.2 Test Setup

In the following subsections, let us look at how this V_{bias} affects various paramters of the OTA by performing DC, AC, Transient and Noise Analyses.

DC Analysis

The circuit in Figure.3.2, is a common test bench to measure various parameters. The AC source in V_{ac} does not impact the DC analysis in any way. So for the DC analysis, the differential pair transistors will have a voltage of V_{cm} at its gates. V_{bias} is the variable supply used as a programmable parameter and a capacitive load to measure the outputs.

$$V_{DD} = 2.5V; V_{SS} = -2.5V; V_{cm} = 1.95V; V_{bias} = 150mV \text{ to } 700mV; V_{ac} = 1V; C_L = 50fF.$$

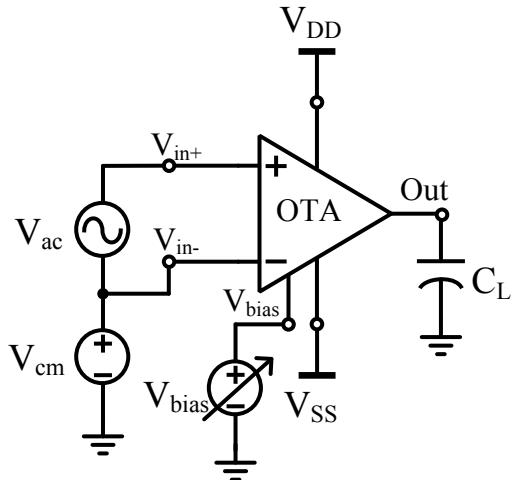


Figure 3.2.: OTA Test setup for AC, DC and Noise Analysis

Vbias (mV)	150	200	300	400	500	600	700
Output DC Bias (mV)	13.68	-16.43	-78.96	-144.6	-213.3	-285.2	-360.3

Table 3.2.: Output DC Bias Point of the OTA

The output DC bias points for various values of V_{bias} is tabulated in Table3.2. The DC voltage at the output decreses with the increase in bias voltage or decrease in bias current.

AC Analysis

Figure. 3.2 is used for AC analysis as well.

$$V_{DD} = 2.5V; V_{SS} = -2.5V; V_{cm} = 1.95V; V_{bias} = 150mV \text{ to } 700mV; V_{ac} = 1V; C_L = 50fF.$$

The same parameters hold good for AC analysis as well. Here, the value of V_{ac} becomes significant. The value of the open loop gain is given by the ratio of output voltage to input voltage.

$$\text{Gain} = \frac{V_{out}}{V_{in}}$$

$$\text{Gain in dB} = 20\log_{10} \frac{V_{out}}{V_{in}}$$

Figure 3.3 shows the semilog plot of Gain for maximum and minimum V_{bias} . The plots for the other values of V_{bias} are not shown here as that would make the plot less legible for understanding and more so because those plots would be in between the plots already shown.

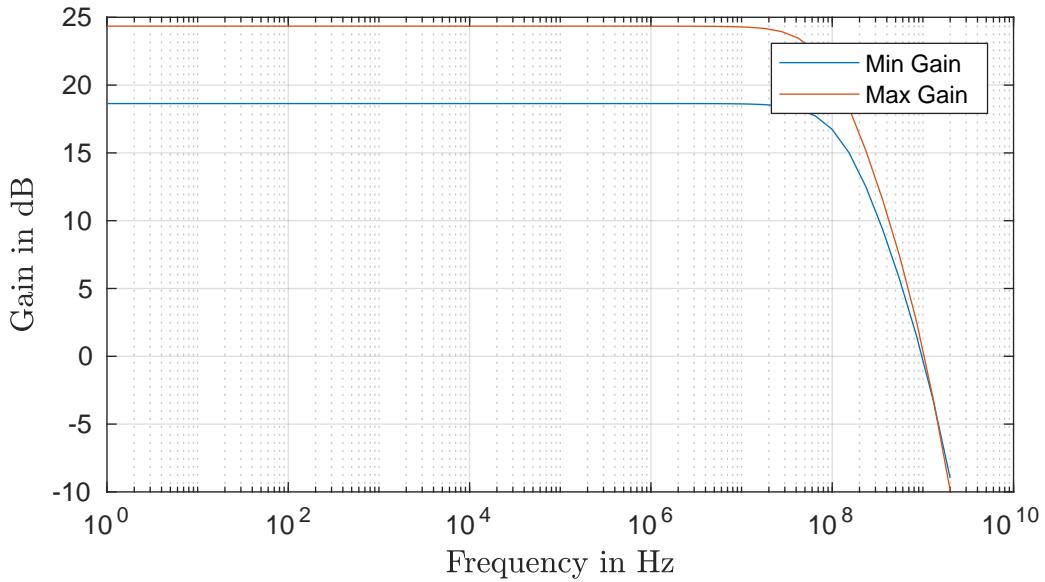


Figure 3.3.: OTA Plot of Gain vs Frequency for different V_{bias}

The variation of open loop gain of the OTA, its bandwidth and the phase margin with respect to V_{bias} is tabulated in Table.???. The bandwidth is kept at a high value in order to make sure that the dominant poles of the first and second stages are sufficiently far from each other so as to obtain a stable system for operation. The maximum open loop gain for this system is 23.7dB. Any value beyond this will cause the amplifier to saturate at the crests and troughs of the output voltage.

V_{bias} (mV)	150	200	300	400	500	600	700
Open Loop Gain (dB)	18.64	19.46	20.9	22.05	22.96	23.7	24.35
Phase Margin (degrees)	63.3	60.63	55.96	52.42	49.91	48.12	46.72
Bandwidth (MHz)	135	130.7	122.2	113.7	105	96.63	89.19

Table 3.3.: Open Loop Gain, Phase Margin and Bandwidth of the OTA

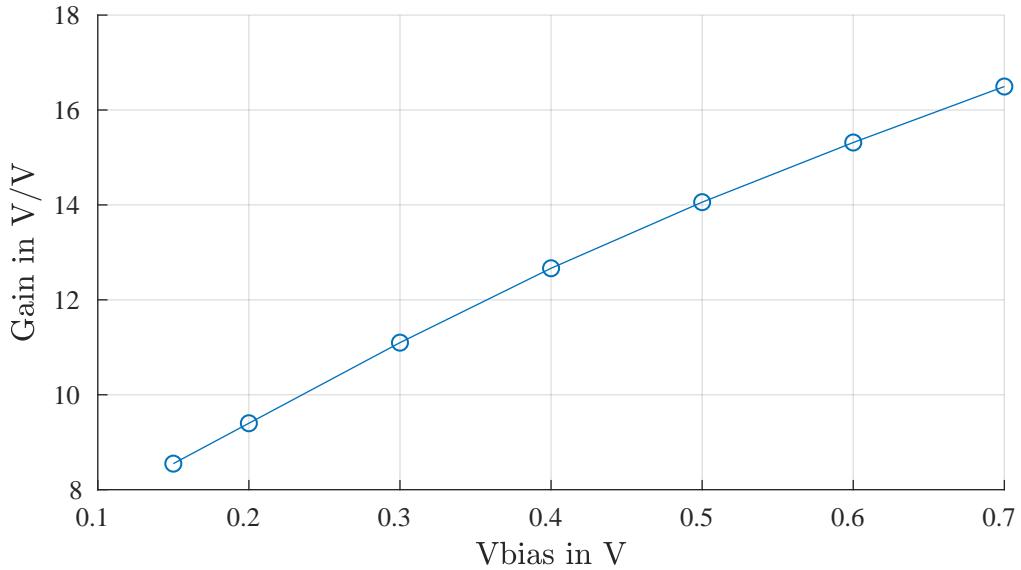


Figure 3.4.: OTA Plot of Gain vs Vbias

On the same lines, the variation of absolute value of gain with respect to different values of V_{bias} is seen in Figure 3.4 tabulated in Table 3.4. The reason to choose the values of V_{bias} are evident from this table and that is because it provides us a gain in the ratio of almost 1:2 for those values of V_{bias} . As seen from the table of specifications that we need a transconductance in the ratio of 1:1.8 or something close to that.

Vbias (mV)	150	200	300	400	500	600	700
DC Gain (V/V)	8.548	9.4	11.1	12.67	14.06	15.31	16.49

Table 3.4.: Absolute values of DC Gain of the OTA

Noise Analysis

Once again, we use the same test bench as shown in Figure 3.2. As mentioned in the previous section, the NMOS differential pair exhibits high flicker noise, also known as 1/f noise. This noise is significant at low frequencies. At moderate and high frequencies, the effect of thermal or white noise is much more dominant and hence flicker noise becomes less significant at those frequencies.

The variation of the input referred noise with respect to V_{bias} is tabulated in Table 3.5. With increase in V_{bias} , the input referred noise decreases. This is because the gain increases with increase in V_{bias} and consequently input referred noise decreases. This also converges to the fact that the input referred noise decreases with bigger dimensions of the differential pair, and thereby contributing to a higher gain.

Vbias (mV)	150	200	300	400	500	600	700
Input Referred Noise (nV/\sqrt{Hz})	46.36	43.73	39.83	37.29	35.57	34.31	33.28

Table 3.5.: Input Referred Noise of the OTA

Transient Analysis - Sine Input

The test bench in Figure.3.5 is used to measure the transient parameters for a sine wave input. An ideal balun is used at the input to provide a differential voltage to the terminals. The voltages are 180^0 out of phase with each other.

$V_{DD} = 2.5V$; $V_{SS} = -2.5V$; $V_{cm} = 1.95V$; $V_{bias} = 150mV$ to $700mV$; $V_{sin} amplitude = 100mV$; $frequency = 1MHz$ $C_L = 50fF$.

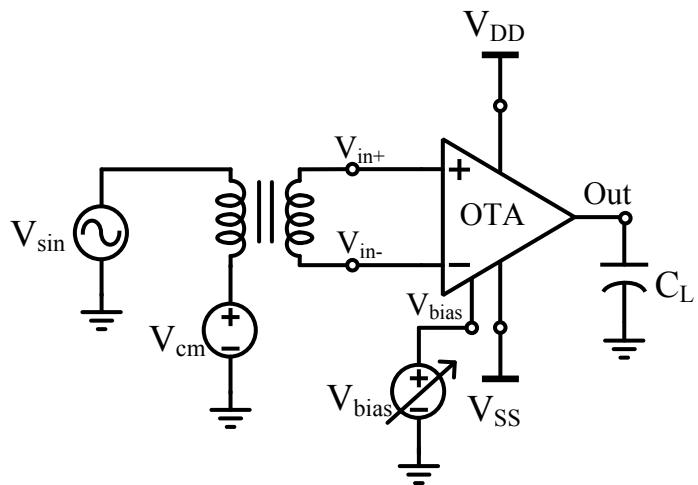


Figure 3.5.: OTA Test setup for Transient Analysis - Sine Wave Input

The transient simulation is carried out for $3\mu s$. The sinusoidal output with respect to time is shown in Figure.3.6 for different values of V_{bias} . As we know from the AC analysis, the gain varies in the ratio of 1:2 and thereby, here we have the peak-to-peak voltages varying in the same ratio. And as discussed in the DC Analysis, the DC bias points at the output are close to zero but not exactly at 0 for all the V_{bias} values.

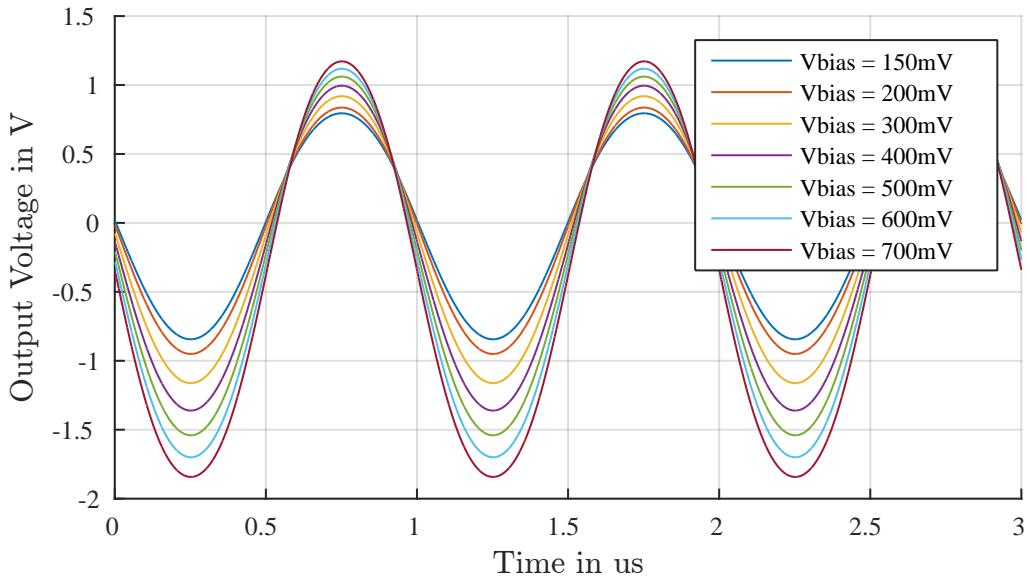


Figure 3.6.: OTA Output Voltage for vs time for different V_{bias}

Table 3.6 shows the variation of different transient parameters with respect to V_{bias} . The voltage swing varies from 1.639 to 3.014 which is almost in the ratio of 1:2. HD3 worsens with increase in V_{bias} and on the contrast, improves. Although, it is seen that the HD2 again starts to worsen beyond 600mV of V_{bias} .

V_{bias} (mV)	150	200	300	400	500	600	700
Vout Max (V)	0.7949	0.8362	0.9188	0.995	1.061	1.119	1.172
Vout Min (V)	-0.844	-0.9505	-1.162	-1.361	-1.54	-1.7	-1.842
Vout Swing (V)	1.639	1.787	2.081	2.356	2.601	2.818	3.014
HD2 (dBc)	-44.83	-44.28	-43.86	-44.74	-47.97	-60.86	-48.75
HD3 (dBc)	-52.15	-49.69	-46.13	-43.87	-42.24	-40.78	-39.32

Table 3.6.: Transient Parameters of the OTA

Transient Analysis - Square Input

The test bench in Figure 3.7 is used to measure the transient parameters for a square wave input. Slew rate is the rate of change of output voltage. It is also defined as the ratio of bias current to load capacitance.

$V_{DD} = 2.5V$; $V_{SS} = -2.5V$; $V_{cm} = 1.95V$; $V_{bias} = 150mV$ to $700mV$; $V_{pulse}V_1 = 100mV$; $V_2 = -100mV$; $PulseWidth = 49.7ns$; $Period = 100ns$; $RiseTime = 300ps$; $Falltime = 300ps$; $C_L = 50fF$.

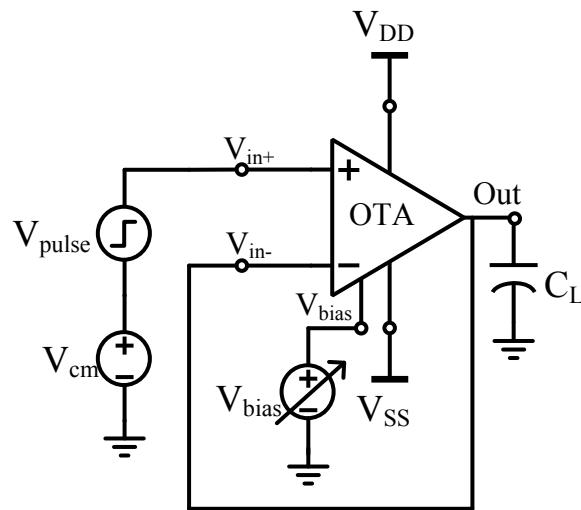


Figure 3.7.: OTA Test setup for Transient Analysis - Square Wave Input

The slew rate, both for the rising edge and the falling edge is tabulated in the Table.3.7.

Vbias (mV)	150	200	300	400	500	600	700
Slew Rate Rising Edge (V/us)	386.9	407.8	452.9	501.9	547.6	585.4	609.3
Slew Rate Falling Edge (V/us)	-389	-413.8	-469.4	-523.5	-570.5	-605.7	-626.4

Table 3.7.: Slew Rate of the OTA

AC Analysis - PSRR

PSRR or Power Supply Signal Ratio is defined as the ability of an amplifier to maintain its output as its DC power supply is varied. It is the ratio of change in the output current to change in power supply.

$$PSRR = \frac{\Delta I_{out}}{\Delta V_{DD}}$$

$V_{DD} = 2.5V$; $AC\text{Magnitude of } V_{DD} = 1V$; $V_{SS} = -2.5V$; $V_{cm} = 1.95V$; $V_{bias} = 150\text{mV to } 700\text{mV}$; $C_L = 50\text{fF}$.

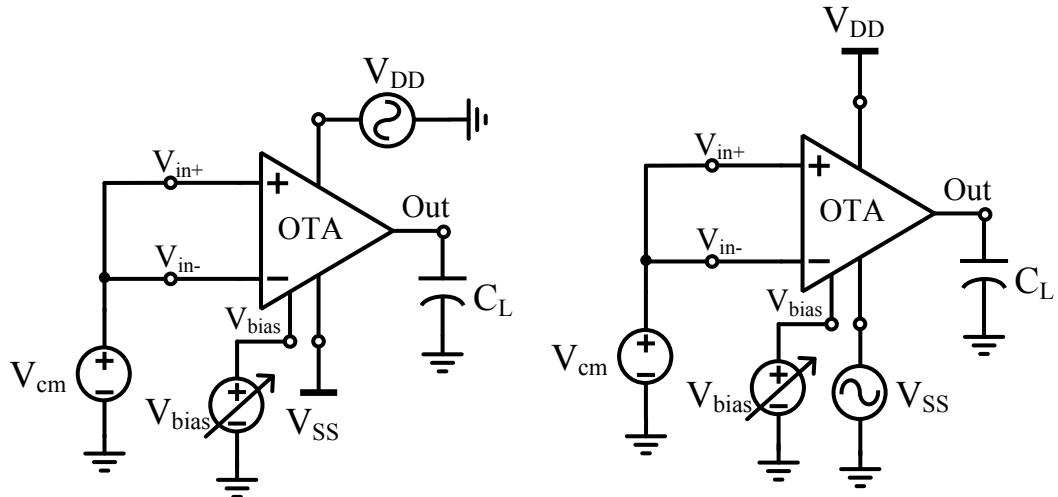


Figure 3.8.: OTA Test setup for calculating PSRR

$V_{DD} = 2.5V$; $V_{SS} = -2.5V$; $AC\text{Magnitude of } V_{SS} = 1V$; $V_{cm} = 1.95V$; $V_{bias} = 150\text{mV to } 700\text{mV}$; $C_L = 50\text{fF}$.

The test bench to measure the PSRR of the OTA is as shown in the Figure.3.8. The one on the left is used to measure PSRR for a change in V_{DD} . And similarly, the one on the right side is used to measure PSRR for a change in V_{SS} .

The variation of PSRR with respect to V_{bias} is tabulated in Table.3.8. The PSRR is fairly low in the range of nA/V and increases only slightly with increase in V_{bias} .

Vbias (mV)	150	200	300	400	500	600	700
PSRR (VDD Supply) (nA/V)	234.6	236.9	241.6	246.7	252.2	258	264.3
PSRR (VSS Supply) (nA/V)	254.5	256.5	260.4	264.2	267.9	271.5	274.9

Table 3.8.: Power Supply Rejection Ratio of the OTA

AC Analysis - Input Impedance

OTAs generally exhibit a very high input impedance. And to measure this parameter, an AC current source with a magnitude of 1A is connected to the non-inverting terminal of the OTA. And the input impedance is given by the ratio of the AC voltage to the AC current at the input of the OTA. Since the current at the input is 1A, the magnitude of the input voltage will be the value of the input impedance in Ohms at that particular frequency. Since the OTA operation is carried out at 1MHz, the voltage at 1MHz is considered to obtain the value of Input Impedance. Figure.3.9 shows the test bench to measure the input impedance.

$V_{DD} = 2.5V$; $V_{SS} = -2.5V$; $V_{bias} = 150\text{mV to } 700\text{mV}$; $C_L = 50\text{fF}$; $I_{sinmagnitude} = 1A$.

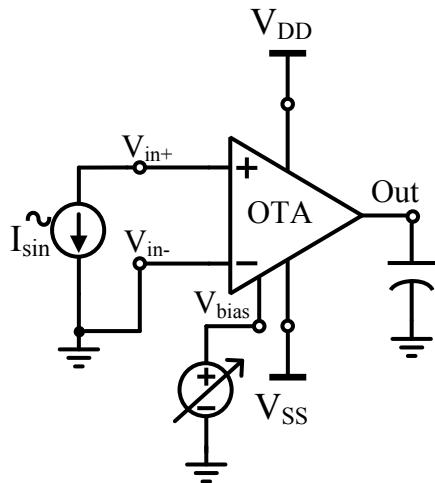


Figure 3.9.: OTA Test setup for calculating Input Impedance

The variation of input impedance with respect to V_{bias} is tabulated in Table 3.9. The variation is quite small and it increases slightly with an increase in bias voltage and is in the order of Mega Ohms.

Vbias (mV)	150	200	300	400	500	600	700
Input Impedance ($M\Omega$)	3.38	3.388	3.403	3.419	3.434	3.45	3.467

Table 3.9.: Input Impedance of the OTA

AC Analysis - Output Impedance

In a concept similar to measuring the input impedance, the output impedance too, is measured with a help of a current source with unity magnitude at the output instead of a Capacitive load. The differential inputs are connected in a common mode configuration. The test bench to measure the output impedance of the OTA is as shown in Figure 3.10.

$$V_{DD} = 2.5V; V_{SS} = -2.5V; V_{cm} = 1.95V; V_{bias} = 150mV \text{ to } 700mV; I_{sin} \text{ magnitude} = 1A.$$

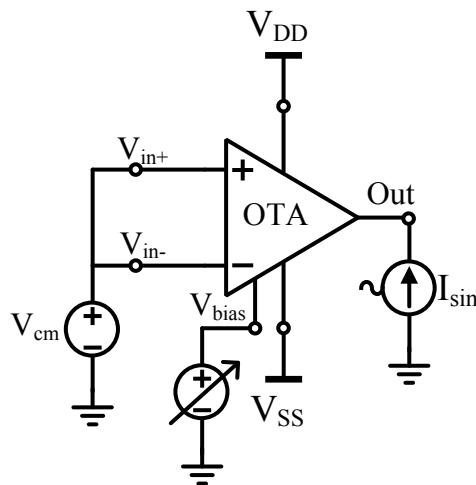


Figure 3.10.: OTA Test setup for calculating Output Impedance

As discussed in the theory chapter, OTAs generally have high output impedance. And its variation with respect to V_{bias} is tabulated in the Table.3.10

Vbias (mV)	150	200	300	400	500	600	700
Output Impedance ($k\Omega$)	1.262	1.3	1.382	1.473	1.577	1.697	1.837

Table 3.10.: Output Impedance of the OTA

3.2 OP AMP Design

The second stage of the design is the Operational Amplifier. This stage too, like the first stage uses a bipolar power supply of 2.5V and -2.5V. A two-stage Miller compensated op amp is designed and it is used as a Voltage Buffer for the OTA.

3.2.1 Schematic

The schematic of the Miller compensation op amp is as shown in the Figure.3.11. The bias current to the differential pair is provided through the current mirror pair of M_5 and M_8 . The bias current is controlled through the transistor M_9 whose gate voltage is provided by the voltage divider formed by the resistors R_{b1} and R_{b2} . C_C is the compensation capacitance between the two stages of the amplifier.

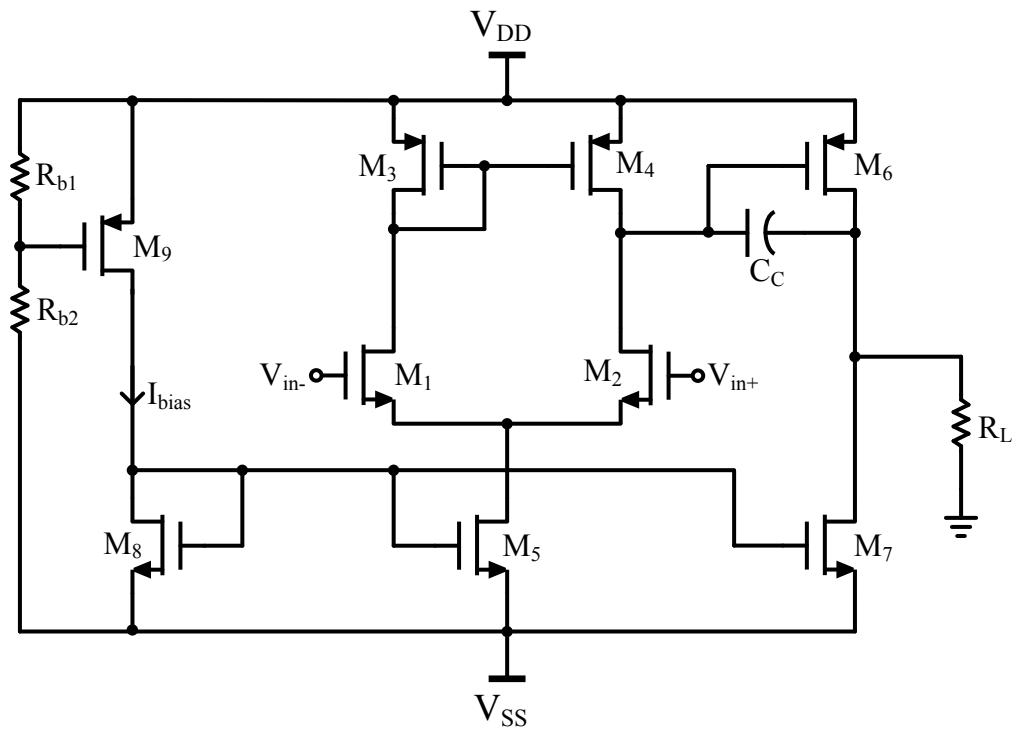


Figure 3.11.: Schematic of the OPAMP Designed

The dimensions of the transistors are tabulated in Table 3.11. One can easily recognize that the transistors at the output are large. This is designed so to make sure the op amp provides a very high current and thereby avoiding a common collector amplifier at the output of the op amp to amplify the output current. The compensation capacitance value is 50fF.

Transistor	Width	Length	Multiplier
M1	5u	500n	2
M2	5u	500n	2
M3	30u	500n	1
M4	30u	500n	1
M5	2u	500n	1
M6	85u	500n	55
M7	50u	500n	48
M8	2u	500n	1
M9	700n	500n	1

Table 3.11.: Dimensions of the Transistors of the designed OPAMP

3.2.2 Test Setup

In the following subsections, the typical parameters of an op amp are simulated and analysed.

DC Analysis

Input Common Mode Range or ICMR of an operational amplifier is the range of the common mode input voltage over which the amplifier behaves as a linear amplifier for differential input signals. In simpler words, the ICMR is defined by the input voltages at which all the transistors remain in saturation. Figure.3.12 shows the test setup to measure the ICMR of the op amp designed.

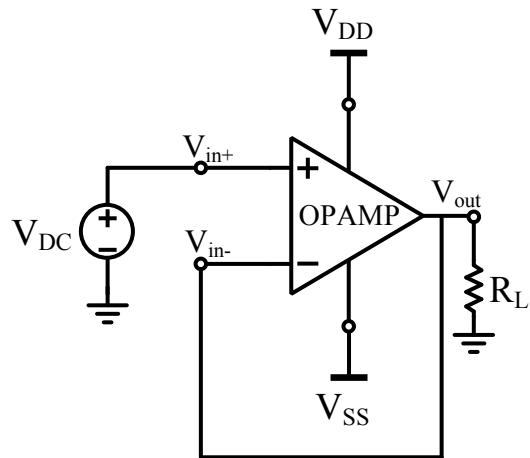


Figure 3.12.: OPAMP Test setup for calculating ICMR

The transistors which impact the ICMR are M_3 , M_4 and M_5 . These transistors were designed in such a way that the op amp ICMR lies between -2V and 2V. The DC input voltage at the non-inverting terminal is swept in the range of V_{DD} and V_{SS} , i.e., 2.5V to -2.5V. The plot of DC output voltage for a varying DC input voltage is as shown in Figure.3.13. It can be noted that the minimum value of the ICMR is -2.19V and the maximum value of the ICMR is 2.089V.

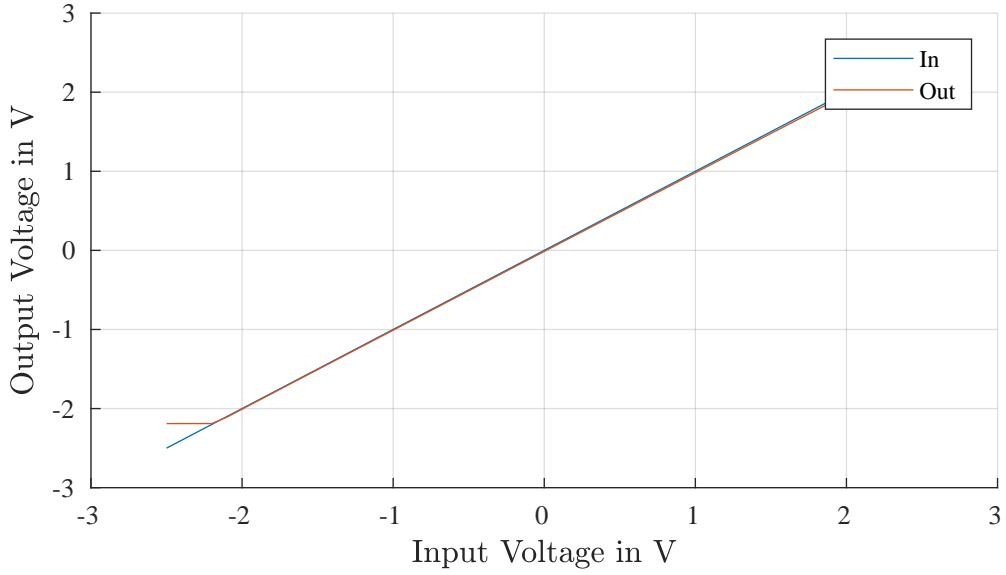


Figure 3.13.: OPAMP Plot of ICMR vs Vin

The output voltage swing is the range of voltage that an opamp can physically provide at its output. On the same lines as ICMR but without feedback, the output voltage swing is measured and plotted with respect to the input voltage. And the output voltage ranges from -2.19 to 2.323. The plot is as shown in Figure 3.14.

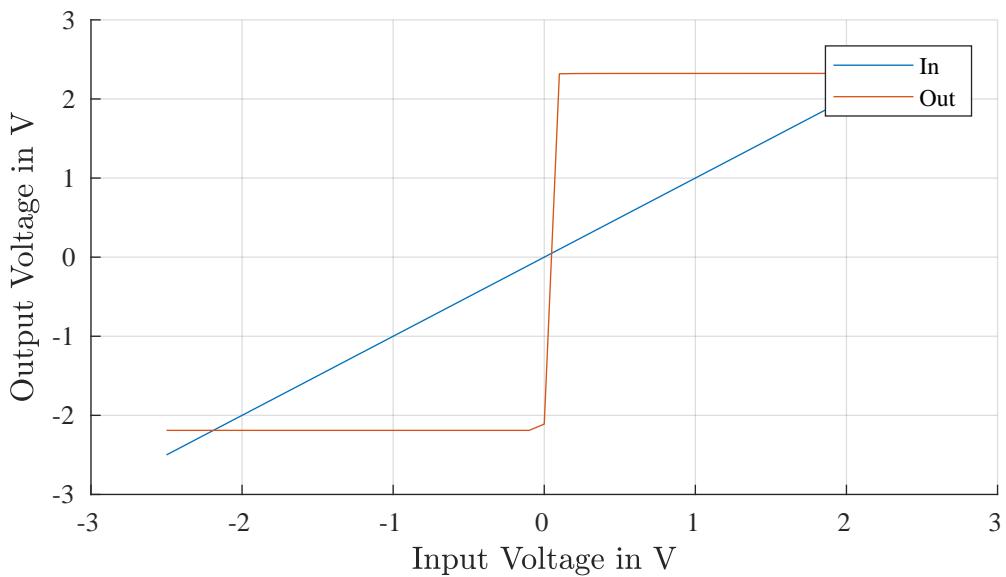


Figure 3.14.: OPAMP Plot of Output Voltage Swing vs Vin

AC Analysis

The open loop gain and the gain bandwidth product are inarguably the most important parameters of an operational amplifier. Before the op amp was actually designed, these parameters were simulated with the help of an ideal op amp from the ahdlLib in Cadence. In order to have a stable system, i.e., an OTA with an OP AMP buffer in a cascade configuration, it is necessary to have the dominant poles far from each other. So that is the reason for the OTA to have a high bandwidth and correspondingly the OP AMP bandwidth can be adjusted so as to reach the specification and also to have a stable system.

The test bench used to measure these parameters is as shown in Figure.3.15. The op amp is configured in an open loop. The DC biasing to the differential transistor pair is provided by the output of the OTA, which is centred around 0V.

$$V_{DD} = 2.5V; V_{SS} = -2.5V; V_{ac\text{magnitude}} = 1 \text{ V}; R_L = 50\Omega.$$

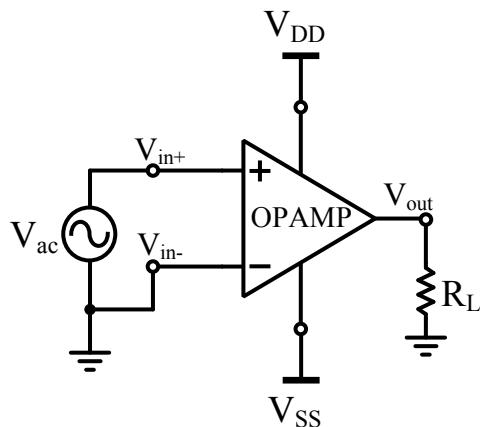


Figure 3.15.: OPAMP Test setup for AC, DC and Noise Analysis

The plot of the open loop gain and the phase of the op amp is as shown in the Figure.3.16. The open loop gain of the op amp is 30.8dB. The gain bandwidth product is 6.2MHz and correspondingly the phase margin is 76.79^0 .

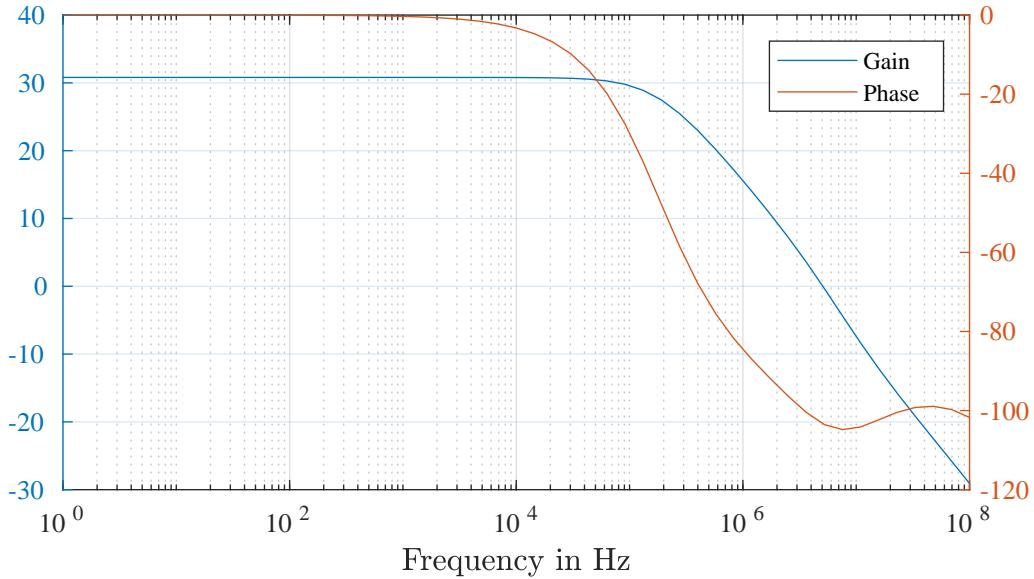


Figure 3.16.: OPAMP Plot of Gain and Phase vs Frequency

The PSRR of the OTA in the first stage was in the range of nA/V and hence negligible. However, the op amp designed exhibits a relatively high value of PSRR. This is due to the bulky transistors at the output stage. The test bench to measure the PSRR of the op amp is as shown in the Figure.3.17. The one on the left is used to measure PSRR for a change in V_{DD} . And similarly, the one on the right side is used to measure PSRR for a change in V_{SS} .

$V_{DD} = 2.5V$; $V_{SS} = -2.5V$; $V_{ac\,magnitude} = 1 V$; $R_L = 50\Omega$.

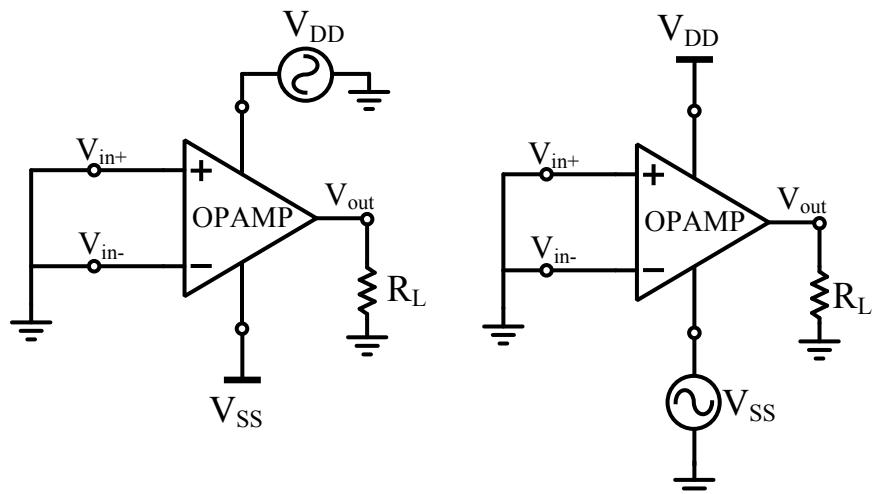


Figure 3.17.: Test setup for calculating PSRR

The PSRR (V_{DD}) of the op amp is 30.96 uA/V, and PSRR (V_{SS}) is 130.96 uA/V. In the next chapter, it is seen that the assymetry in the two PSRR values doesn't affect the PSRR of the whole system.

The test bench to calculate the input impedance follows a similar concept to that of the OTA. i.e., a unitz current source is connected to the non-inverting terminal of the op amp and the voltage at that terminal is measured which in turn is the magnitude of the input impedance of the op amp.

$$V_{DD} = 2.5V; V_{SS} = -2.5V; I_{sin}magnitude = 1A; R_L = 50\Omega.$$

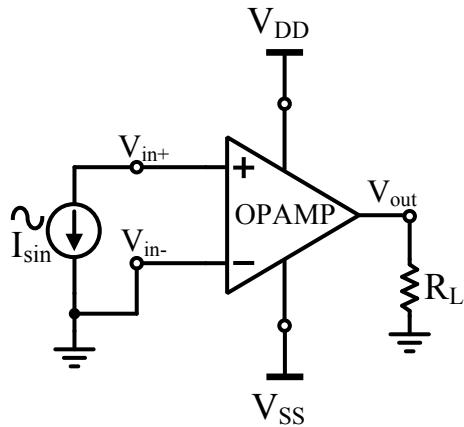


Figure 3.18.: Test setup for calculating Input Impedance

To have a stable system, it is important that input impedance of the second stage is higher than the output impedance of the first stage. Given that the output impedance of the OTA is generally high, the input impedance of the op amp becomes a very important parameter. And th input impedance is found to be 9.04MΩ.

On the same lines, the test bench to measure the output impedance of the op amp is as shown in Figure.3.19. The resistive load is replaced by a current source with unity magnitude. And hence the voltage at the output will be the magnitude of the output impedance of th op amp.

$$V_{DD} = 2.5V; V_{SS} = -2.5V; I_{sin}magnitude = 1A.$$

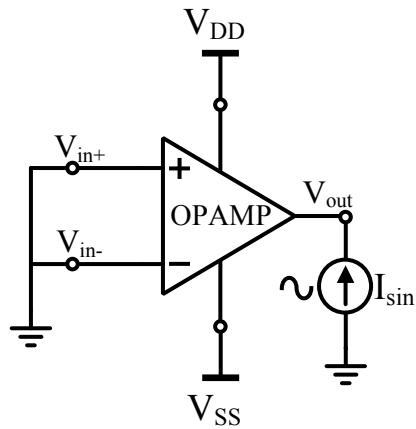


Figure 3.19.: Test setup for calculating Output Impedance

Op amps are known to have zero or very low output impedance. Along with this theoretical fact, the op amp in this work is designed to retrieve very high currents, so it is expected to have a very low output impedance. The value of the output impedance is observed to be 4.167Ω .

Transient Analysis

The test bench to perform the transient analysis is as shown in the Figure.3.20. The op amp is connected in a negative feedback configuration so as to analyse its behavior as a voltage buffer.

$V_{DD} = 2.5V$; $V_{SS} = -2.5V$; $V_{sin} amplitude = 1.5V$; frequency = 1MHz; $R_L = 50\Omega$.

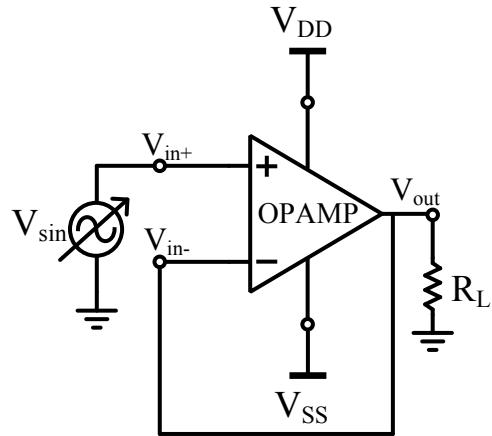


Figure 3.20.: Test setup for Transient Analysis - Sine Wave Input

The plot of input voltage and output voltage with respect to time is as shown in the Figure.3.21. The output follows the input only with a very small delay.

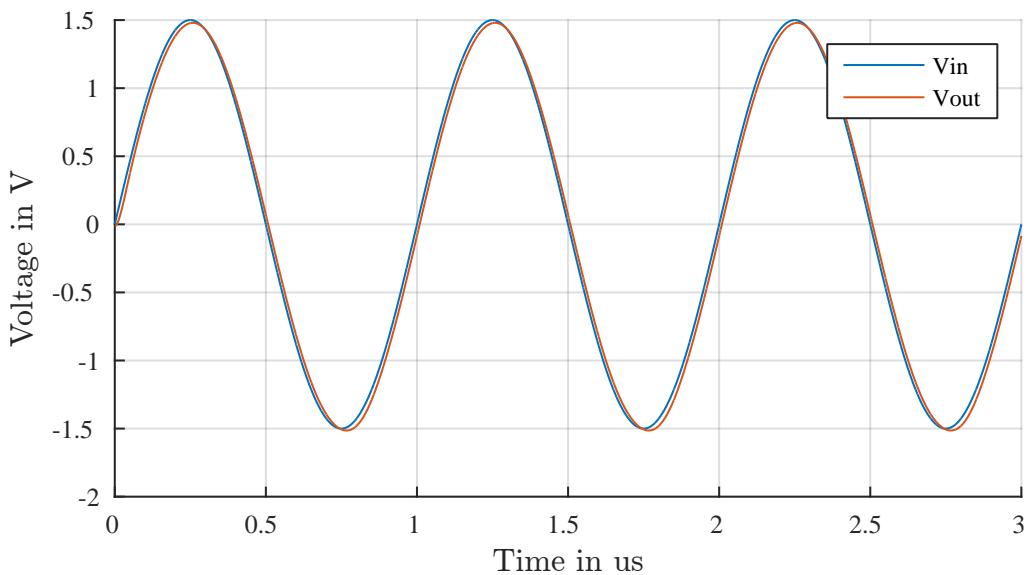


Figure 3.21.: OPAMP Plot of Output Voltage vs time

The output current of the op amp is effectively the current flowing through the load resistor R_L . The plot of current versus time is as shown in the Figure 3.22. The current is 180^0 out of phase with the voltage and it ranges from -30mA to 30mA for a 50Ω load and 3V peak to peak input voltage.

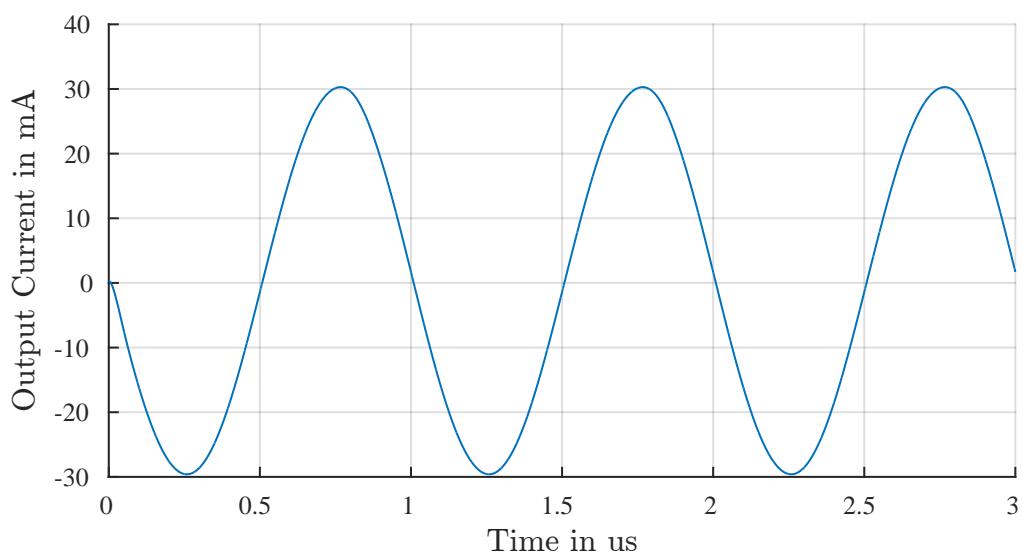


Figure 3.22.: OPAMP Plot of Ourput Current vs time

The only change from the previous test bench to this is that we need to replace the sinusoidal source by a pulse input source.

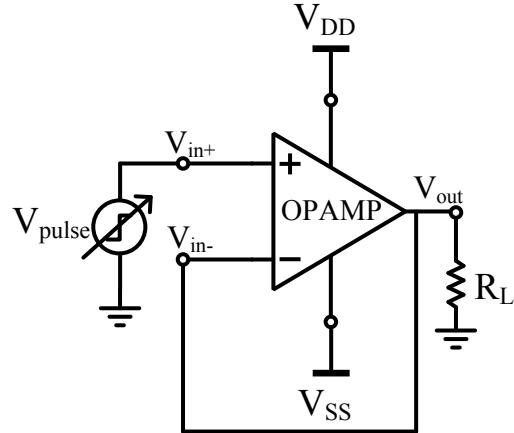


Figure 3.23.: Test setup for Transient Analysis - Square Wave Input

The values of all the parameters of the op amp discussed so far have been tabulated in Table 3.12

Parameter	Value
Open Loop Gain	30.8 dB
Gain Bandwidth Product	6.2 MHz
Phase Margin	76.79
ICMR (min)	-2.19 V
ICMR (max)	2.089 V
Output Current (max)	-29.6 mA
Output Current (min)	30.28 mA
Output Voltage Swing	-2.19 .. 2.323
Slew Rate	10 V/us
PSRR (VDD)	30.96 uA/V
PSRR (VSS)	138.8 uA/V
Input Impedance	9.04 MOhms
Output Impedance	4.167 Ohms

Table 3.12.: Simulation Results of the OPAMP

3.3 The Complete Design

The block diagram of the two stage design with an OTA and an OP AMP is as shown in Figure 3.24. The other end of the capacitor of the first stage is connected to the negative power supply instead of ground since we have only two levels in the IC (-2.5V and 2.5V). Both the stages use the same power supply. The output of the OTA is directly connected to the non-inverting terminal of the OP AMP without any DC isolation via a coupling capacitor.

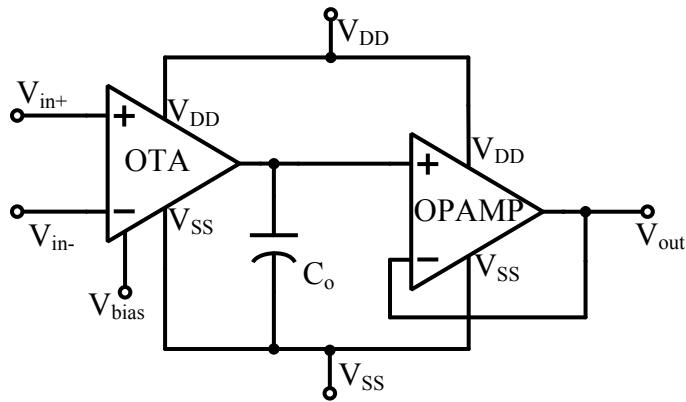


Figure 3.24.: Block Diagram of the Overall System

The schematic symbol for the overall system is as indicated in Figure 3.25. The block diagram of the system is drawn inside to get an understanding of the configuration.

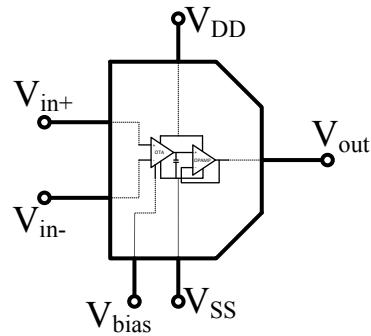


Figure 3.25.: Schematic Symbol for the Overall System

3.3.1 Schematic

The transistor level schematic of the overall system is as shown in the Figure 3.26. The upper portion of the schematic is the OTA and the bottom portion is the OP AMP. Note the feedback connection of the OP AMP and the connection between the OTA and the OP AMP. To summarize the physical aspects of the system, there are 3 input terminals, 2 power supply levels and 1 output pin.

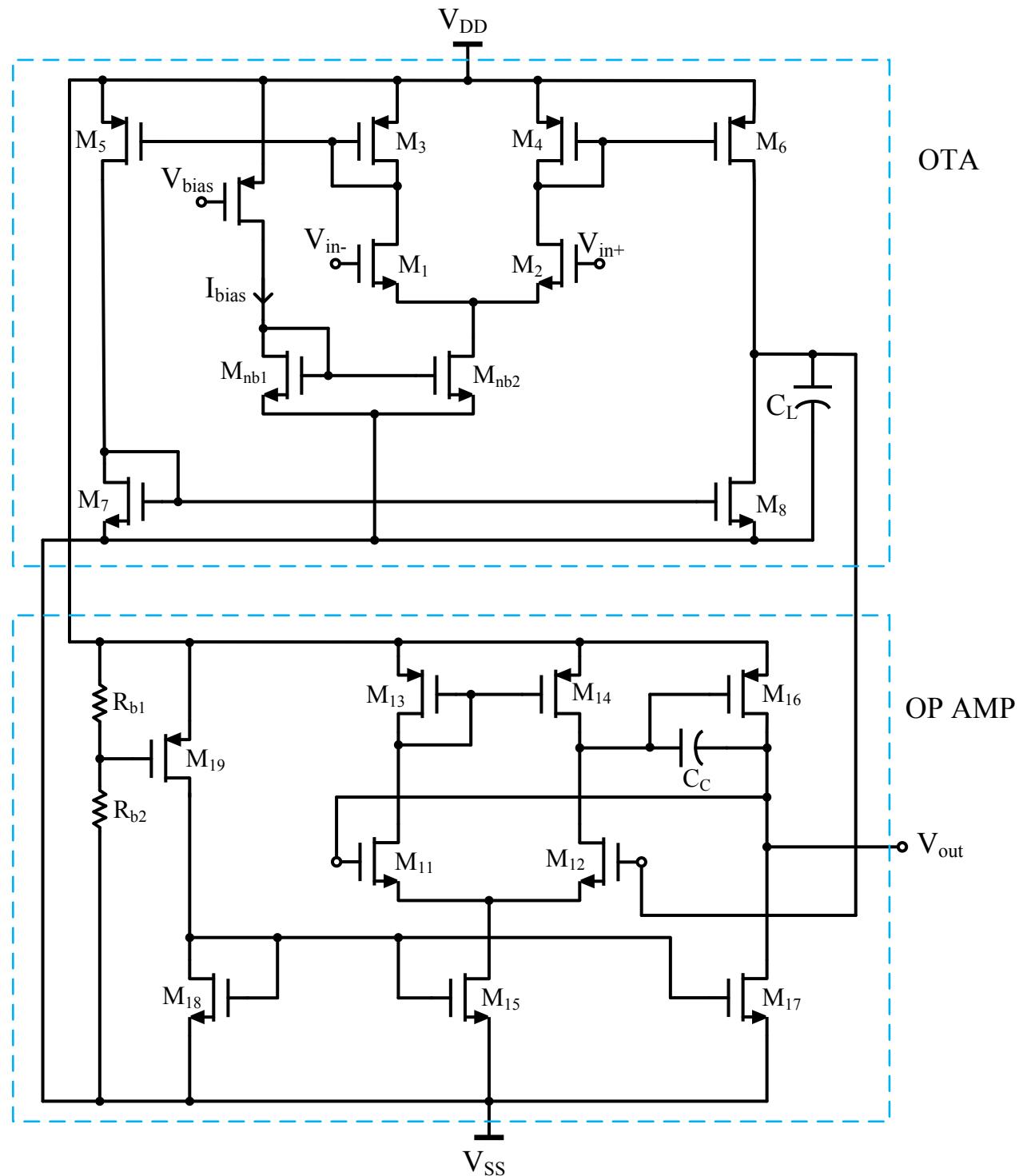


Figure 3.26.: Schematic Diagram for the Overall System

4 Simulation Results

In this chapter, the simulation results for the overall system designed are discussed. And also the behavior of the amplifier for process variation, power supply variation and temperature variation is discussed.

4.1 DC Analysis

The test bench to perform the DC analysis is as shown in the Figure.4.1.

$V_{DD} = 2.5V$; $V_{SS} = -2.5V$; $V_{cm} = 1.95V$; $V_{bias} = 150mV$ to $700mV$; $V_{ac} = 1V$; $R_L = 50\Omega$.

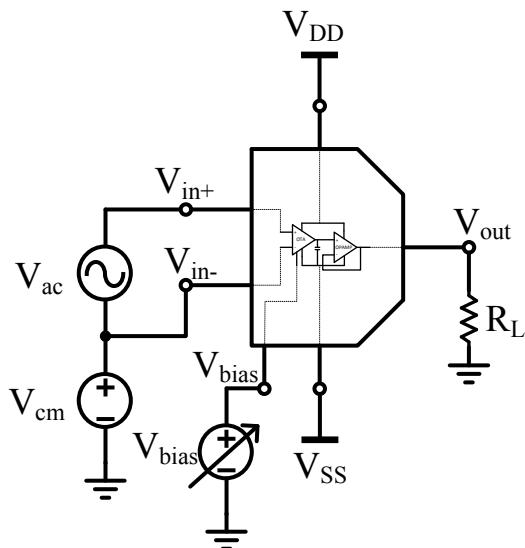


Figure 4.1.: Test setup for DC Analysis

The DC Bias point at the output of the system is tabulated in the Table.4.1. Output DC bias points are almost symmetric around 0V and vary from 180.1mV to -219.3mV.

Vbias (mV)	Output DC Bias (mV)
150	180.1
200	148.4
250	115.8
300	82.28
350	47.83
400	12.45
450	-23.86
500	-61.08
550	-99.24
600	-138.3
650	-178.4
700	-219.3

Table 4.1.: DC Bias Point at the output of the circuit

4.2 AC Analysis

The test bench is Figure.4.1 is used for the AC analysis too. The magnitude of the AC source is set to 1V and as mentioned in the previous chapter, the voltage at the output will be the gain of the overall system.

The plot of gain for different values of V_{bias} is as shown in the Figure.4.2. The value of the open loop gain is between 18dB and 25dB.

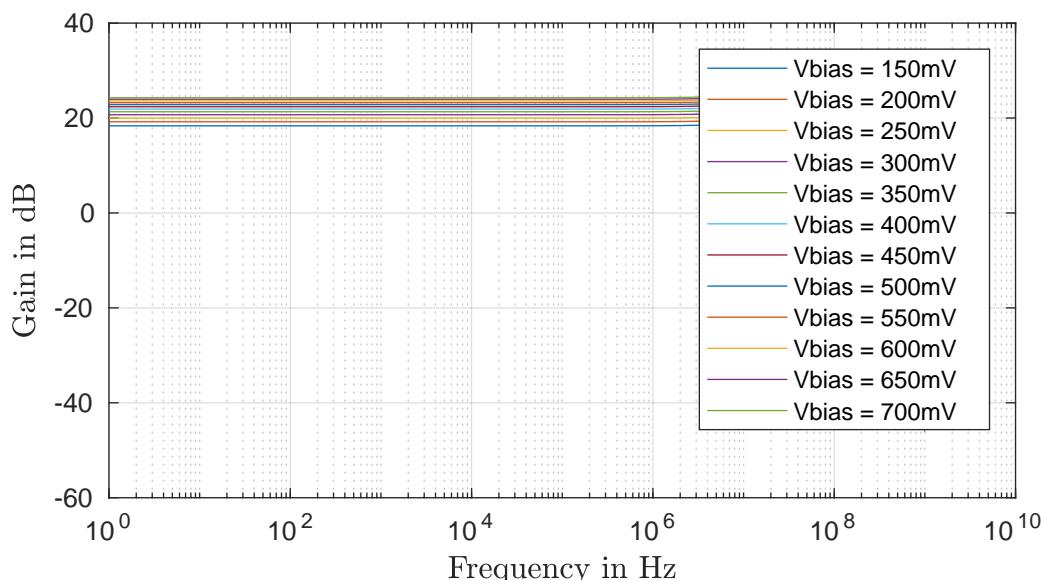


Figure 4.2.: Plot of Gain vs Frequency for different Vbias

The results of the AC analysis are tabulated below in Table.4.2. The bandwidth is fairly constant at around 14MHz. But the phase margin starting to drop just a tad below 30 with a V_{bias} of 700mV and beyond.

Vbias (mV)	DC Gain (dB)	Bandwidth (MHz)	Phase Margin
150	18.5	14.43	55.49
200	19.34	14.38	51.37
250	20.13	14.34	47.76
300	20.83	14.29	45.08
350	21.46	14.24	42.55
400	22.02	14.19	40.19
450	22.52	14.14	38
500	22.97	14.08	35.97
550	23.38	14.01	34.08
600	23.75	13.95	32.31
650	24.1	13.88	30.63
700	24.43	13.8	29.02

Table 4.2.: DC Gain, Bandwidth and Phase Margin of the Overall System

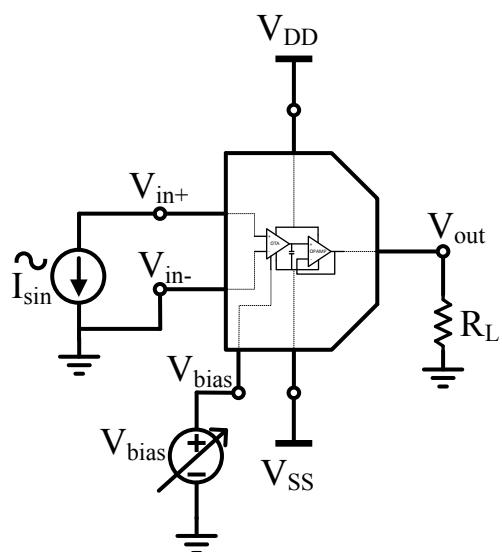


Figure 4.3.: Test setup to measure Input Impedance

Vbias (mV)	Input Impedance (Mega Ohms)
150	3.394
200	3.402
250	3.41
300	3.418
350	3.425
400	3.433
450	3.44
500	3.448
550	3.456
600	3.464
650	3.473
700	3.482

Table 4.3.: Input Impedance of the Overall System

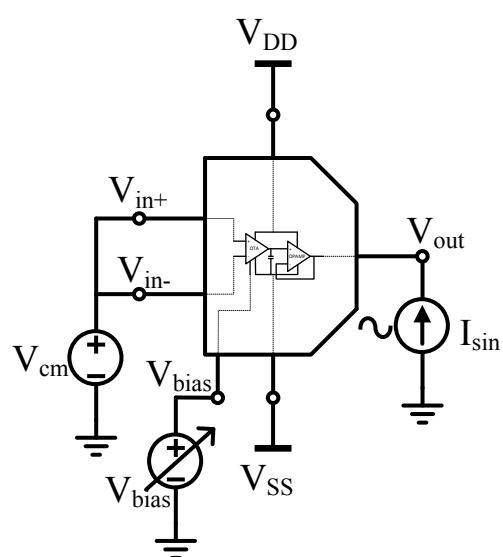


Figure 4.4.: Test setup to measure Output Impedance

Vbias (mV)	Output Impedance (Ohms)
150	0.9415
200	0.9434
250	0.9453
300	0.9474
350	0.9495
400	0.9517
450	0.9541
500	0.9565
550	0.9591
600	0.9618
650	0.9646
700	0.9675

Table 4.4.: Output Impedance of the Overall System

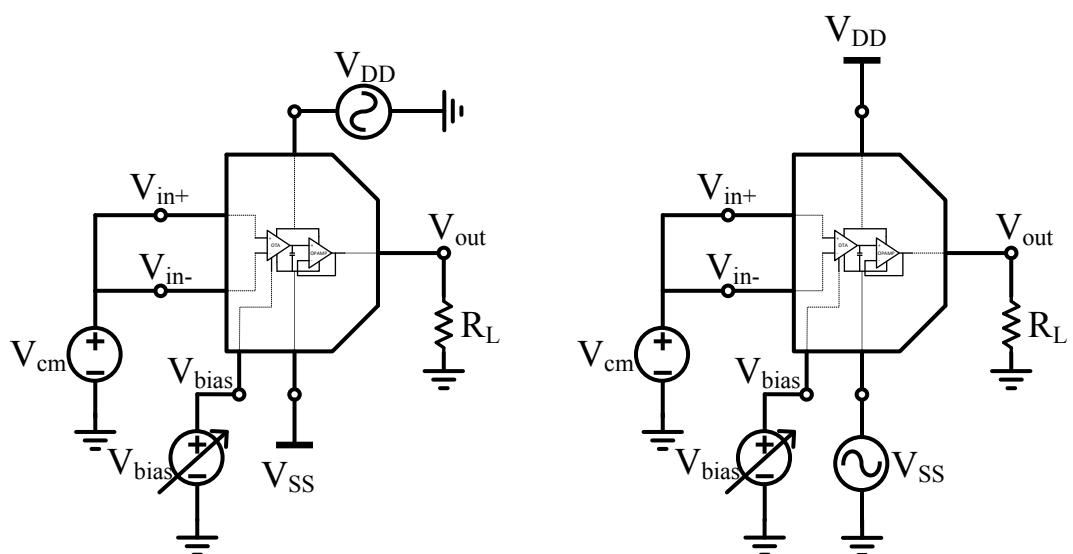


Figure 4.5.: Test setup to measure PSRR

Vbias (mV)	PSRR (VDD)(uA/V)	PSRR (VSS)(uA/V)
150	97.76	93.69
200	89.66	85.77
250	82.86	79.11
300	77.26	73.59
350	72.68	69.04
400	68.93	65.28
450	65.84	62.18
500	63.27	59.53
550	61.1	57.26
600	59.22	55.28
650	57.59	53.52
700	56.13	51.92

Table 4.5.: PSRR of the Overall System

4.3 Transient Analysis

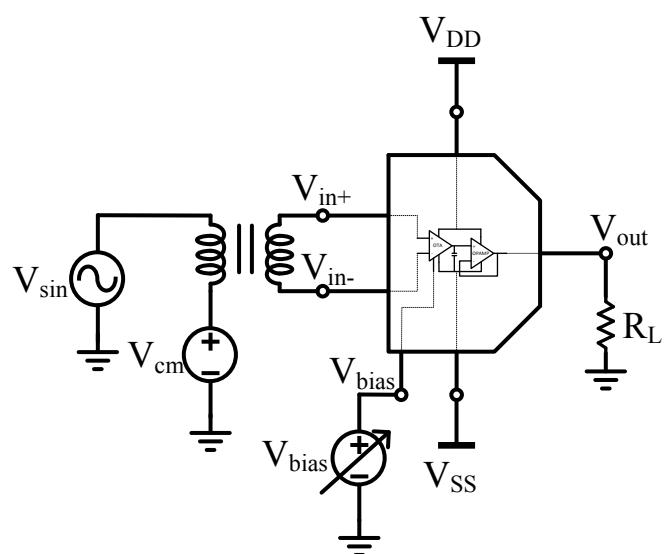


Figure 4.6.: Test setup for Transient Analysis - Sine Wave input

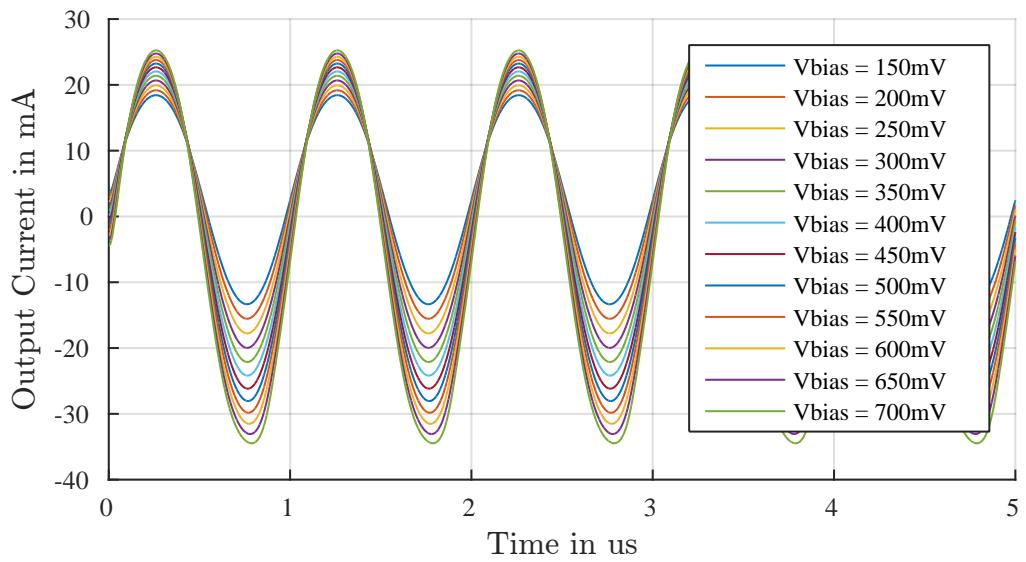


Figure 4.7.: Plot of Output Current vs time for different Vbias

Vbias (mV)	Iout Max(mA)	Iout Min(mA)	Iout p2p (mA)	HD2 (dBc)	HD3 (dBc)
150	18.43	-13.34	31.77	-37.14	-48.17
200	19.17	-15.55	34.72	-36.62	-45.67
250	19.93	-17.77	37.7	-35.65	-43.65
300	20.67	-19.97	40.64	-35.15	-42.07
350	21.38	-22.12	43.49	-34.84	-40.83
400	22.04	-24.19	46.23	-34.72	-39.85
450	22.66	-26.17	48.83	-34.8	-39.01
500	23.24	-28.05	51.29	-35.08	-38.24
550	23.77	-29.83	53.6	-35.54	-37.42
600	24.28	-31.51	55.79	-36.13	-36.47
650	24.76	-33.07	57.83	-36.61	-35.24
700	25.24	-34.47	59.71	-36.44	-33.61

Table 4.6.: Transient Parameters of the Overall System

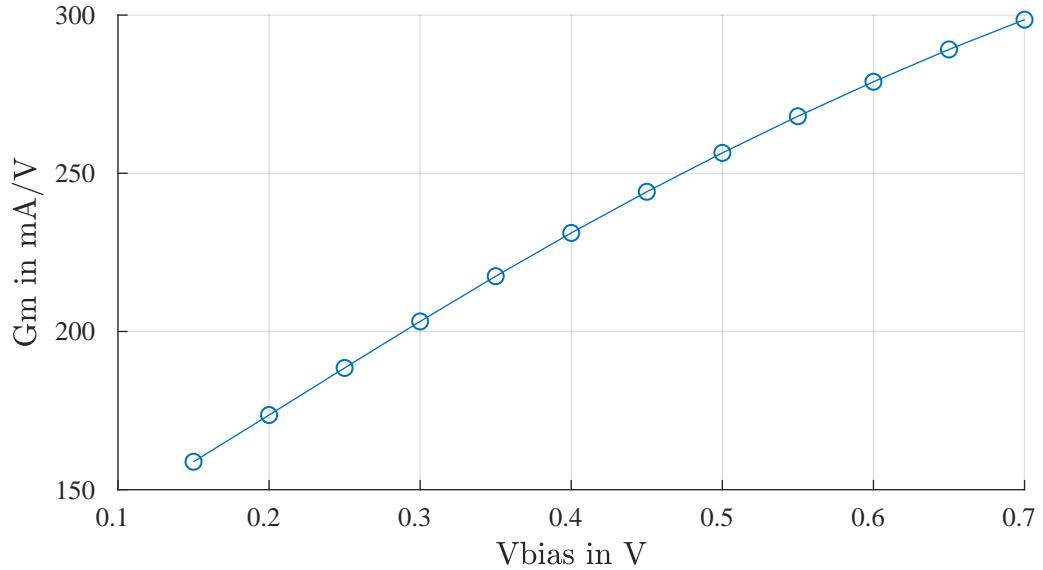


Figure 4.8.: Plot of Gm vs Vbias

Vbias (mV)	Transconductance (mA/V)
150	158.8
200	173.6
250	188.5
300	203.2
350	217.5
400	231.2
450	244.2
500	256.4
550	268
600	278.9
650	289.1
700	298.5

Table 4.7.: Transconductance Gain of the Overall System

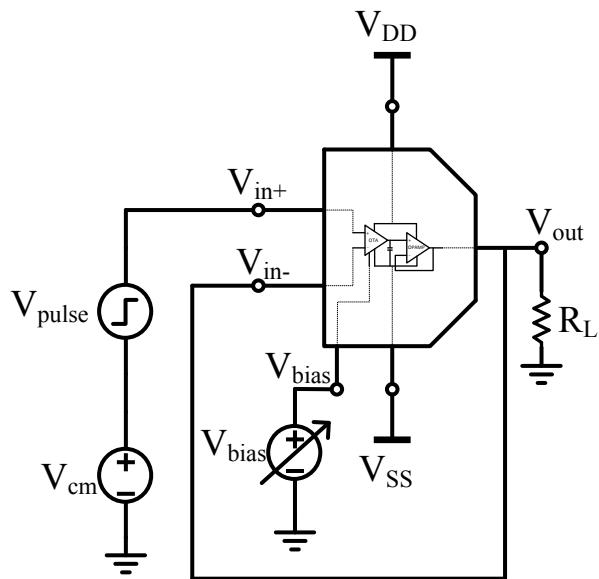


Figure 4.9.: Test setup for Transient Analysis - Square Wave input

Vbias (mV)	Slew Rate (Rising Edge)(V/us)	Slew Rate (Falling Edge)(V/us)
150	6.985	-8.73
200	7.505	-9.779
250	8.042	-10.68
300	8.581	-11.34
350	9.095	-11.66
400	9.561	-11.7
450	9.954	-11.6
500	10.27	-11.45
550	10.49	-11.3
600	10.65	-11.14
650	10.76	-10.99
700	10.82	-10.84

Table 4.8.: Slew Rate of the Overall System

4.4 Noise Analysis

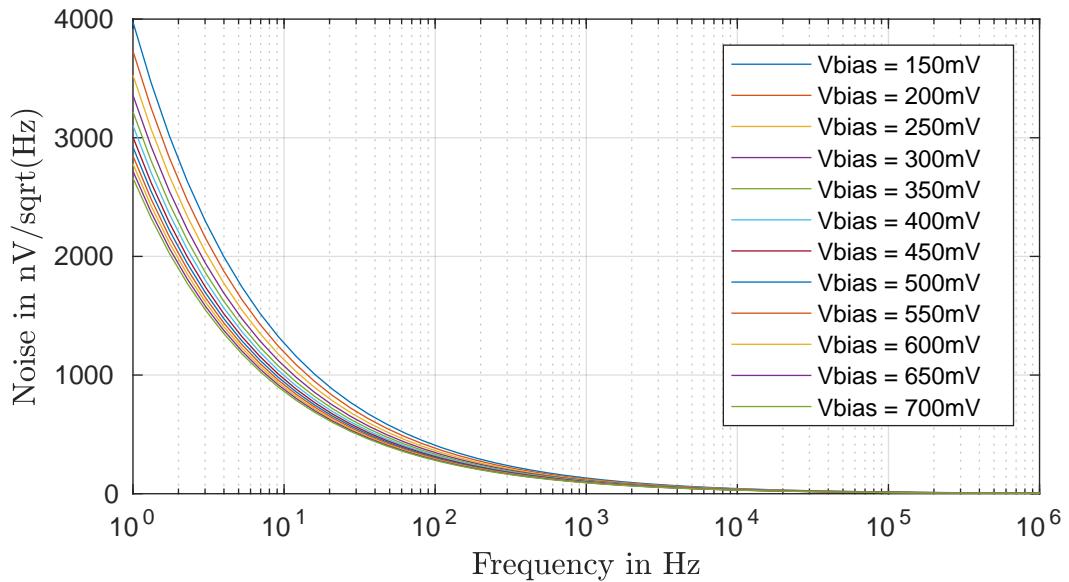


Figure 4.10.: Plot of Input Referred Noise vs Frequency for different V_{bias}

V_{bias} (mV)	Input Referred Noise (nV/sqrt(Hz))
150	46.64
200	43.93
250	41.71
300	39.91
350	38.46
400	37.29
450	36.33
500	35.52
550	34.82
600	34.21
650	33.66
700	33.16

Table 4.9.: Input Referred Noise of the Overall System

4.5 Programmable Load

RL (Ohms)	DC Gain(dB)	Bandwidth(MHz)	Phase Margin	Transconductance(mA/V)
35	22.2	13.13	40.97	338.9
40	22.22	13.55	40.22	296.8
45	22.25	13.88	39.6	264
50	22.28	14.16	39.08	237.7
55	22.3	14.4	38.63	216.2
60	22.32	14.6	38.24	198.3
65	22.34	14.77	37.9	183.1
70	22.35	14.92	37.6	170

Table 4.10.: AC Parameters of the Overall System for a programmable load - 1

Parameter	Value
Input Impedance (Mega Ohms)	3.436
Output Impedance (Ohms)	0.953
PSRR (VDD)(uA/V)	67.32
PSRR (VSS)(uA/V)	63.65
Input Referred Noise (nV/sqrt(Hz))	36.79

Table 4.11.: AC Parameters of the Overall System for a programmable load - 2

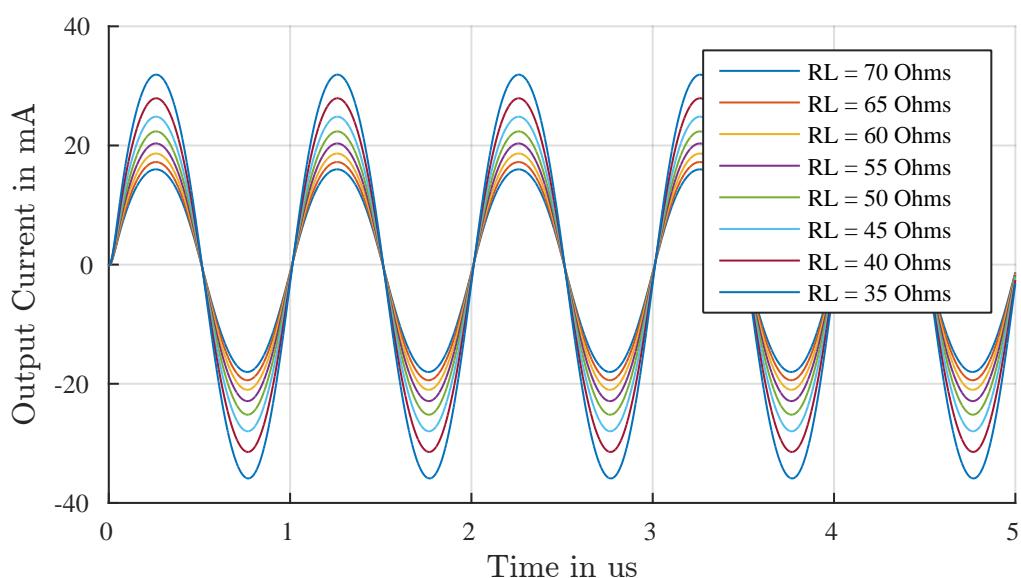


Figure 4.11.: Plot of Output Current vs Time for different RL

RL (Ohms)	Iout(max)(mA)	Iout(min)(mA)	Iout(p2p)(mA)
35	31.89	-35.89	67.77
40	27.92	-31.44	59.36
45	24.83	-27.97	52.8
50	22.36	-25.19	47.55
55	20.33	-22.91	43.24
60	18.65	-21.01	39.65
65	17.22	-19.4	36.61
70	15.99	-18.02	34.01

Table 4.12.: Maximum and Minimum Output Currents for a programmable load

Parameter	Value
HD2 (dBc)	-34.6
HD3 (dBc)	-39.4
Slew Rate (Rising Edge)(V/us)	10.28
Slew Rate (Falling Edge)(V/us)	-10.45

Table 4.13.: Transient Parameters of the Overall System for a programmable load

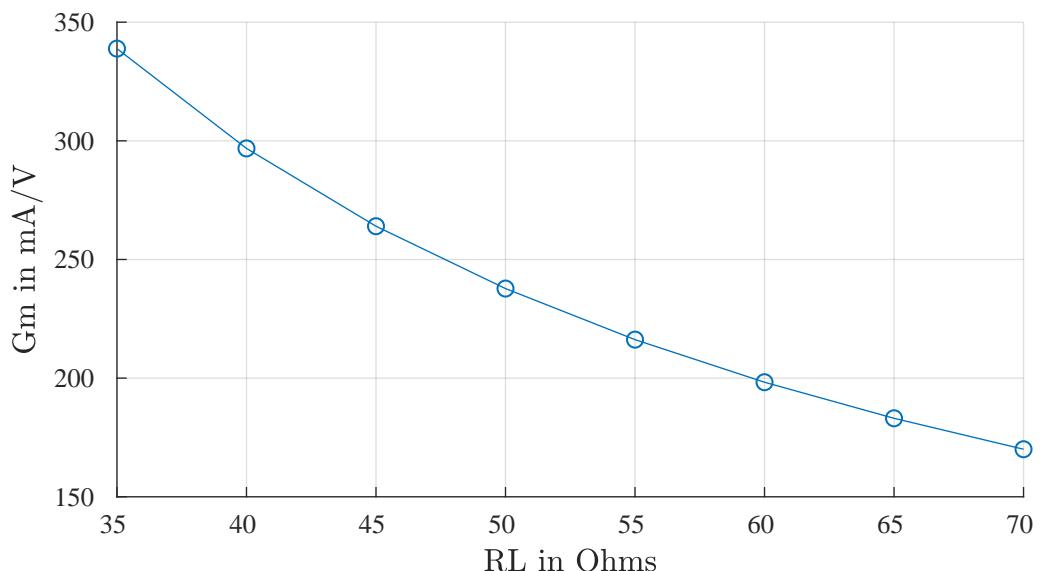


Figure 4.12.: Plot of Transconductance vs RL

4.6 Corner Simulation

4.6.1 Process Variation

4.6.2 Process and Supply Variation

4.6.3 Process, Voltage and Temperature (PVT) variation

4.6.4 Summary of PVT Corner Analysis



5 Conclusion

5.1 Summary of Results

5.2 Outlook



A Appendix

