

Design and Implementation of a Radiation Hardened High Output Current Transconductance Amplifier

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TECHNISCHE
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(Signature)



Abstract



Zusammenfassung



Acknowledgments



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1 Introduction

1.1 Novel DC Current Transformer

1.2 Specification

1.3 Technology

2 Theory

2.1 The Operational Transconductance Amplifier

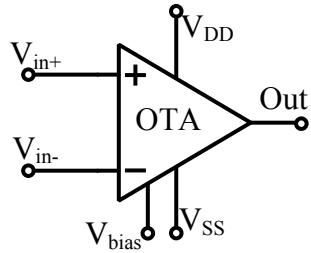


Figure 2.1.: Symbol of an OTA

2.1.1 Different Topologies

Conventional Current Mirror OTA

Super Class AB OTA

Folded Cascode OTA

2.2 The Opeartional Amplifier

2.2.1 Miller Compensation OP AMP

2.2.2 OP AMP as a Voltage Buffer



3 Design and Implementation

3.1 The Gm/Id Methodology

3.2 OTA Design

3.2.1 Schematic

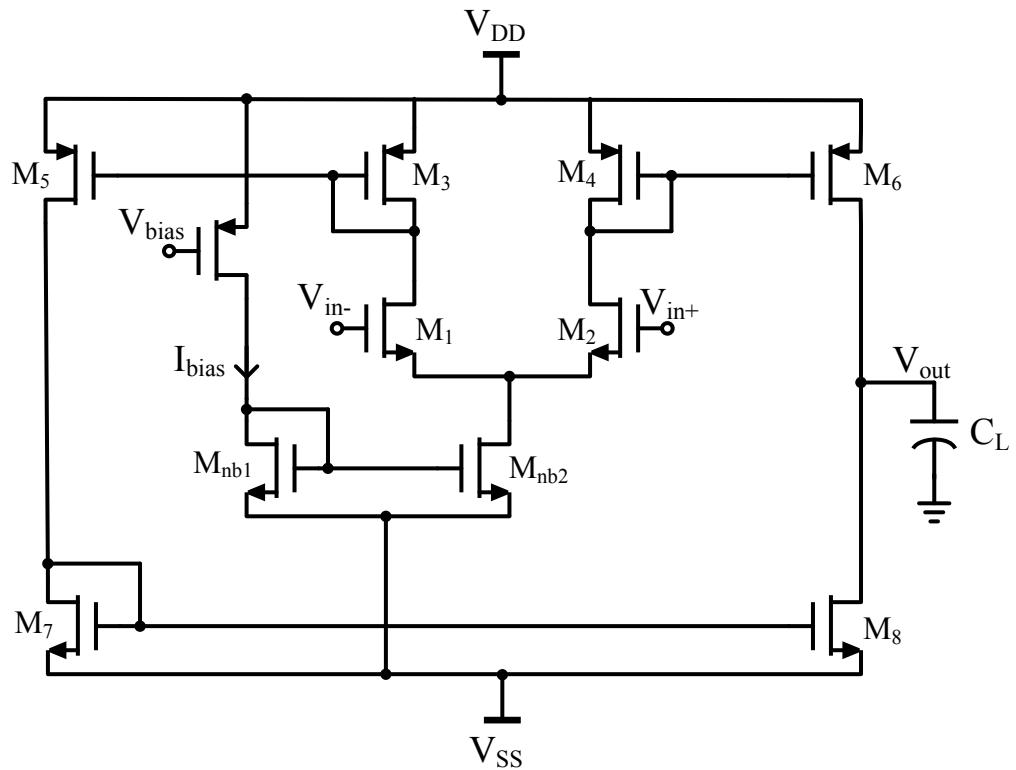


Figure 3.1.: Schematic of the OTA Designed

Transistor	Width	Length	Multiplier
M1	6u	500n	2
M2	6u	500n	2

Table 3.1.: Dimensions of the Transistors of the designed OTA

3.2.2 Test Setup

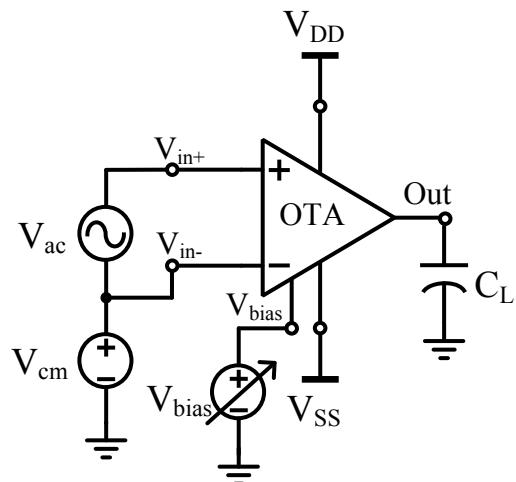


Figure 3.2.: OTA Test setup for AC, DC and Noise Analysis

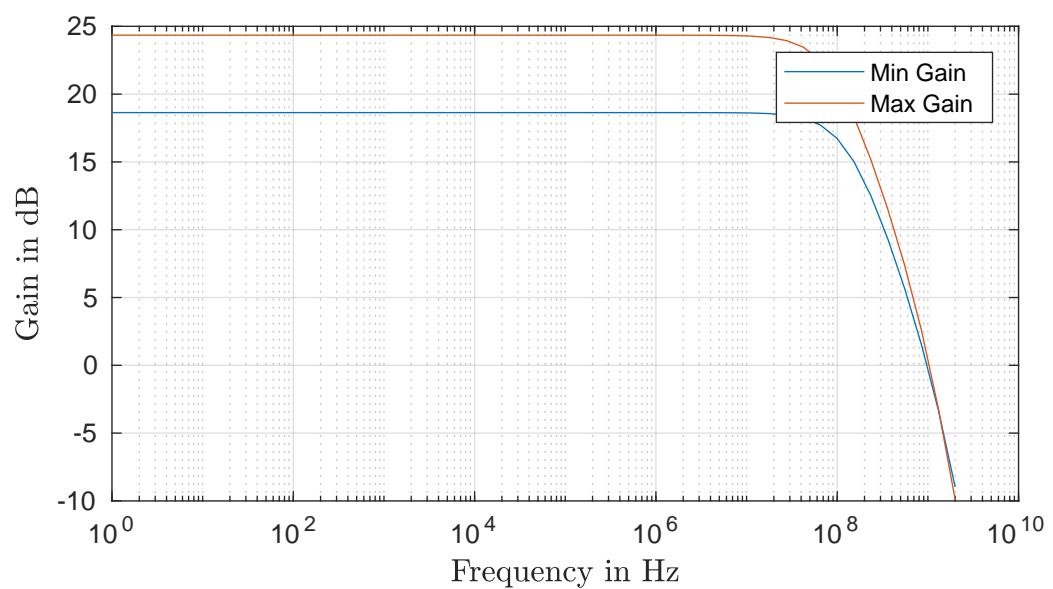


Figure 3.3.: OTA Plot of Gain vs Frequency for different V_{bias}

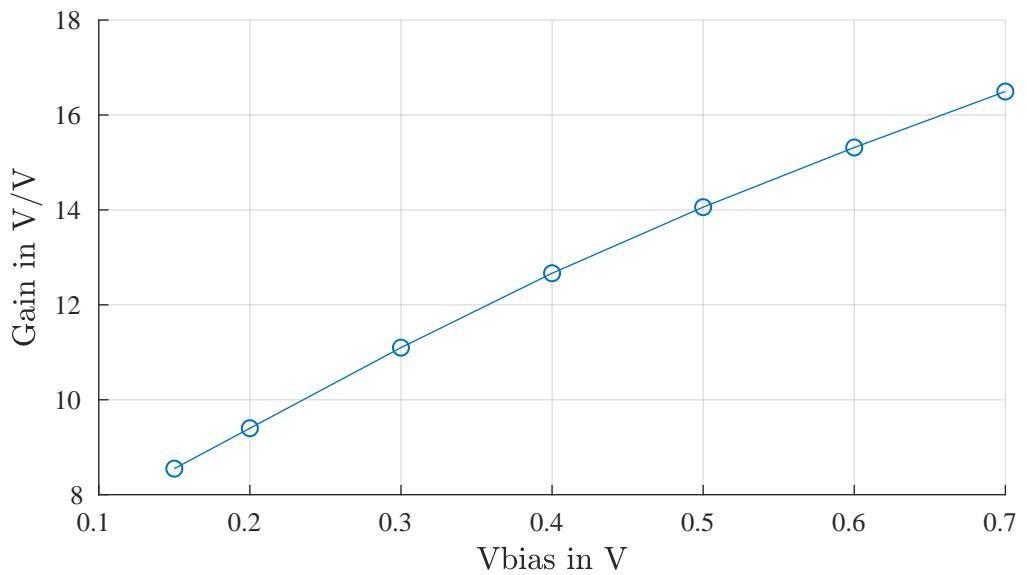


Figure 3.4.: OTA Plot of Gain vs V_{bias}

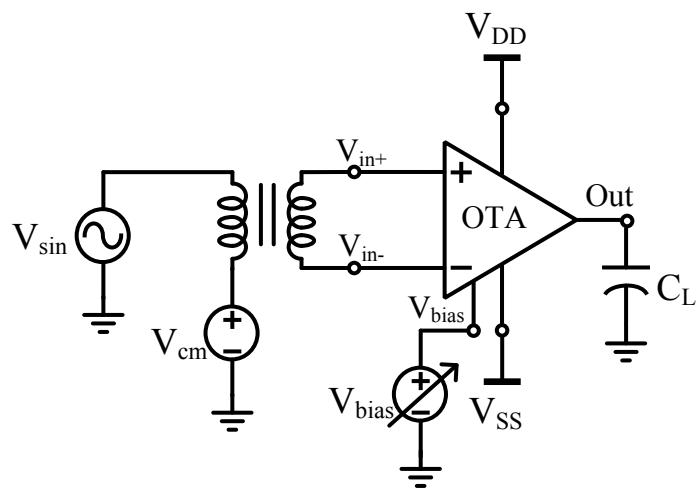


Figure 3.5.: OTA Test setup for Transient Analysis - Sine Wave Input

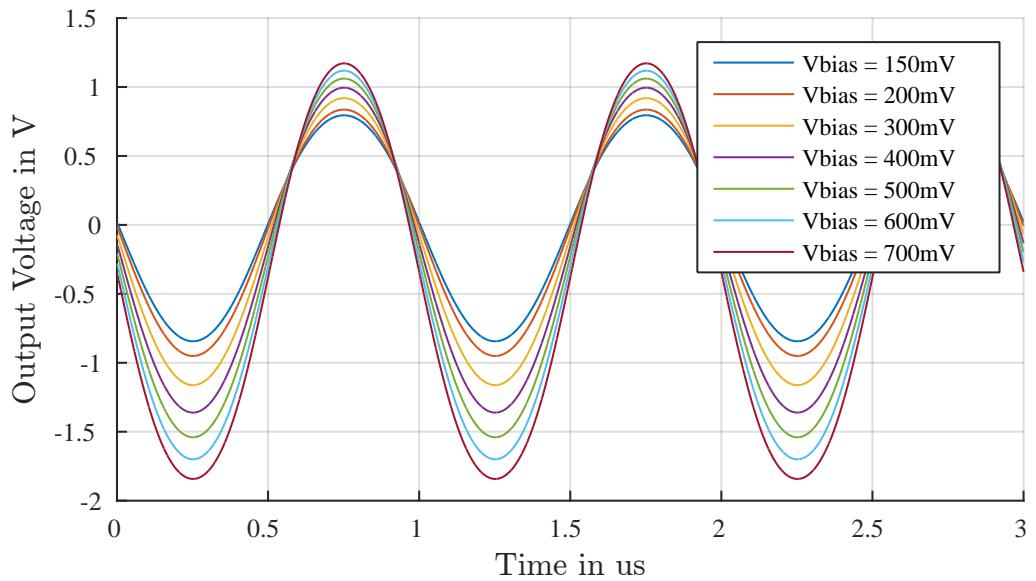


Figure 3.6.: OTA Output Voltage vs time for different V_{bias}

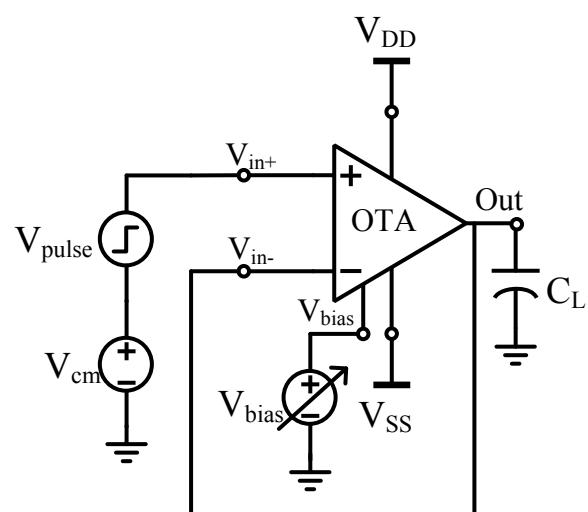


Figure 3.7.: OTA Test setup for Transient Analysis - Square Wave Input

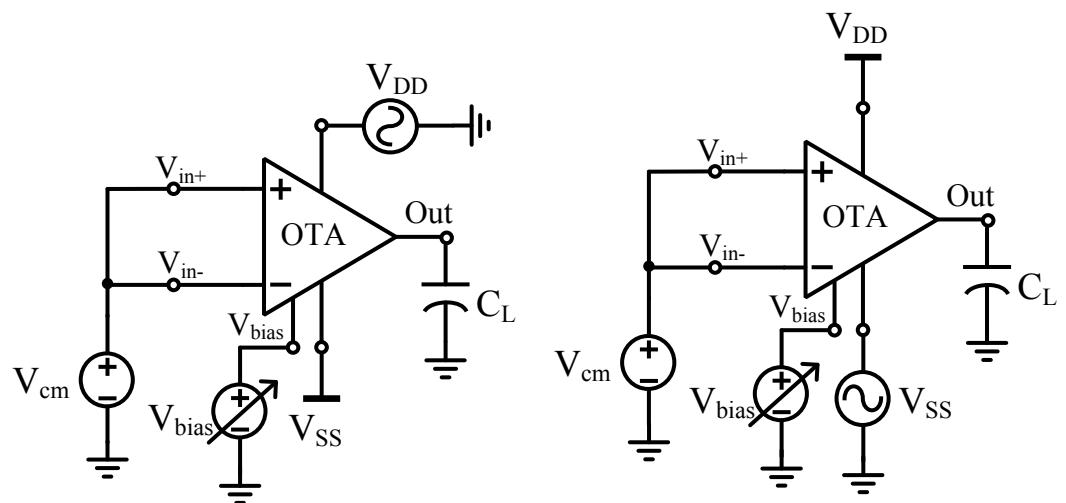


Figure 3.8.: OTA Test setup for calculating PSRR

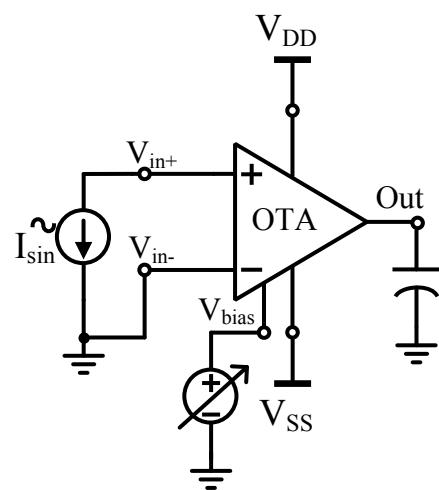


Figure 3.9.: OTA Test setup for calculating Input Impedance

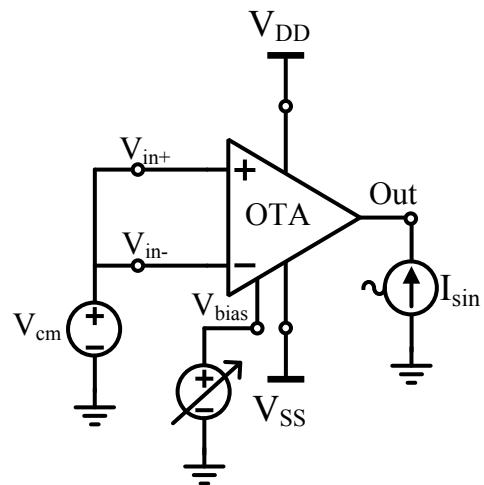


Figure 3.10.: OTA Test setup for calculating Output Impedance

3.3 OP AMP Design

3.3.1 Schematic

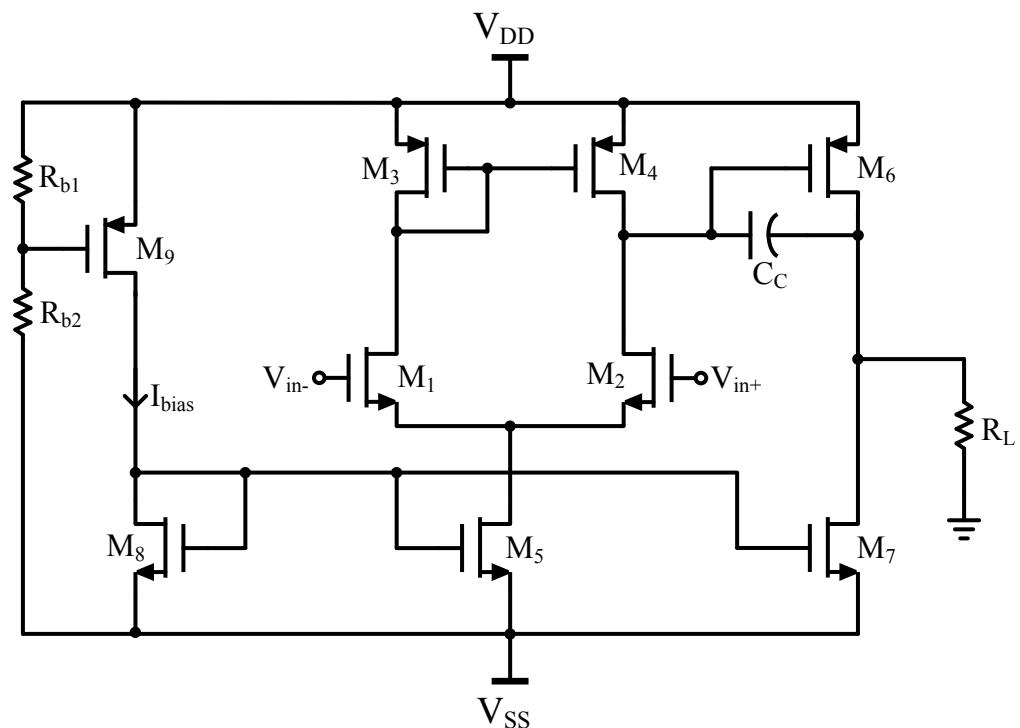


Figure 3.11.: Schematic of the OPAMP Designed

Transistor	Width	Length	Multiplier
M1	6u	500n	2
M2	6u	500n	2

Table 3.2.: Dimensions of the Transistors of the designed OPAMP

3.3.2 Test Setup

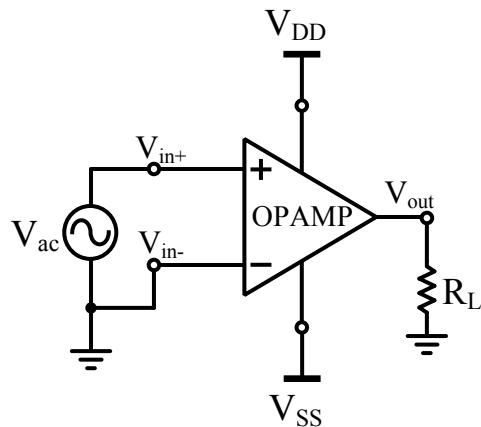


Figure 3.12.: OPAMP Test setup for AC, DC and Noise Analysis

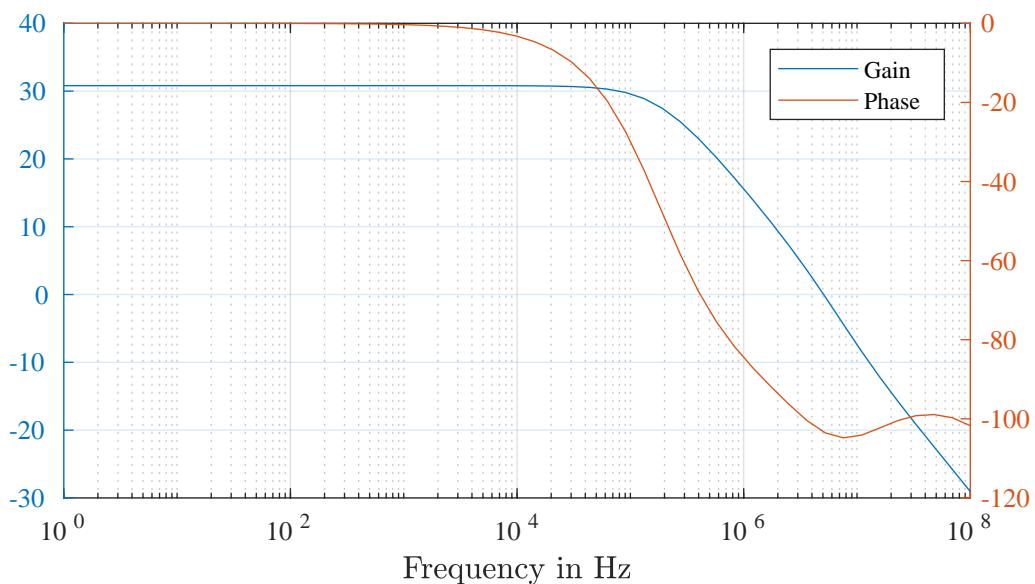


Figure 3.13.: OPAMP Plot of Gain and Phase vs Frequency

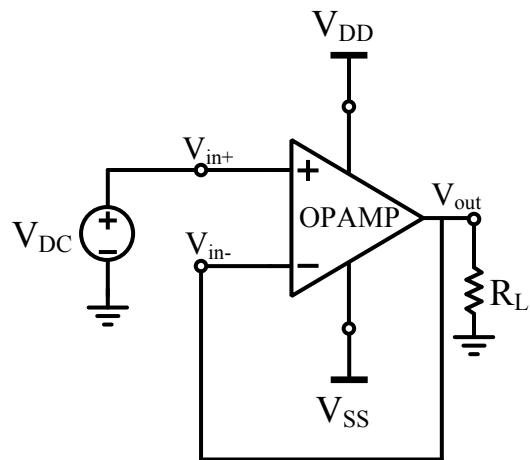


Figure 3.14.: OPAMP Test setup for calculating ICMR

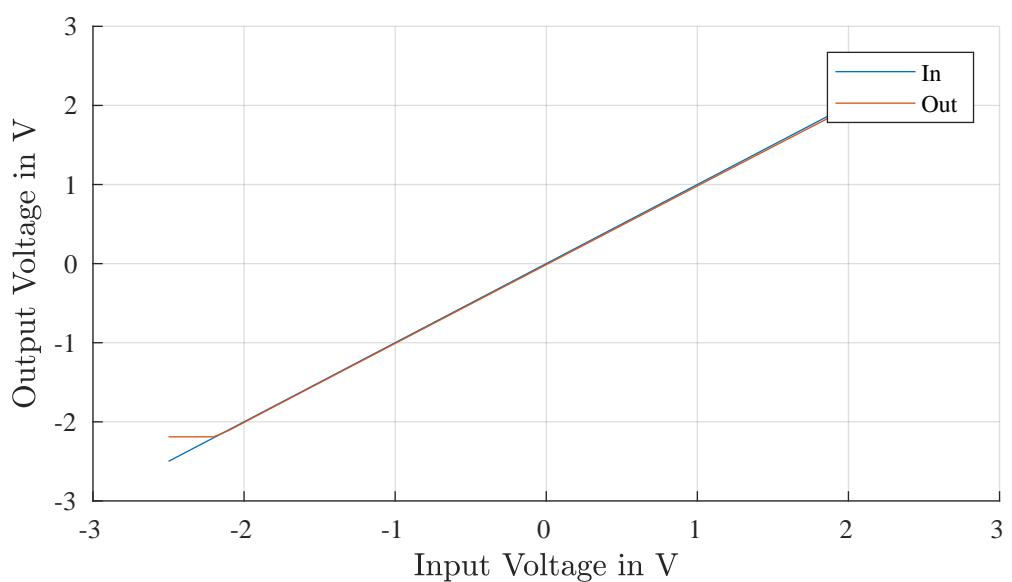


Figure 3.15.: OPAMP Plot of ICMR vs V_{in}

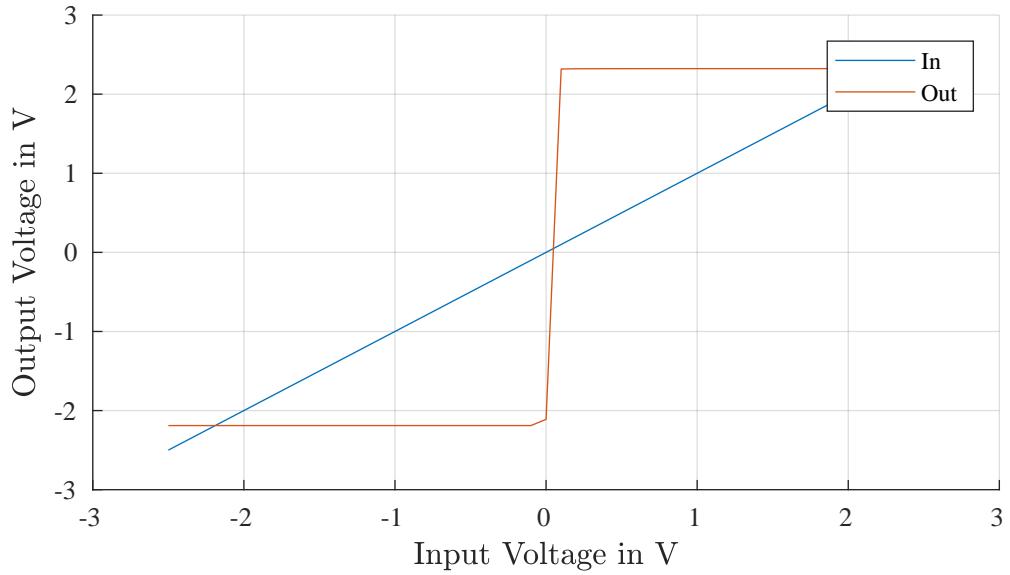


Figure 3.16.: OPAMP Plot of Output Voltage Swing vs V_{in}

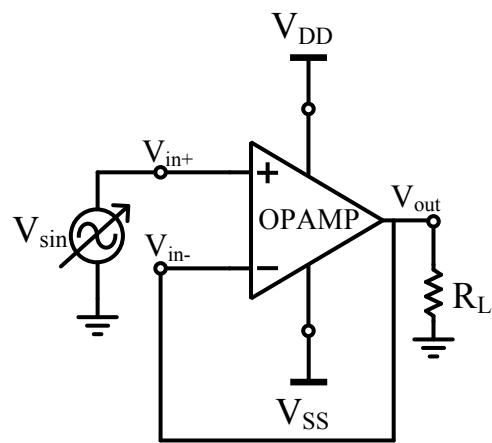


Figure 3.17.: Test setup for Transient Analysis - Sine Wave Input

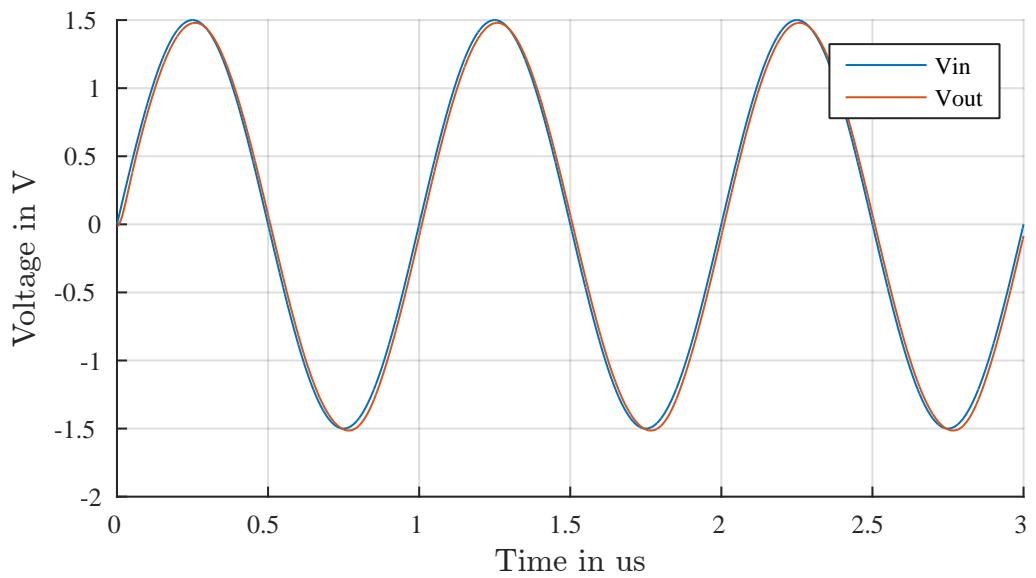


Figure 3.18.: OPAMP Plot of Output Voltage vs time

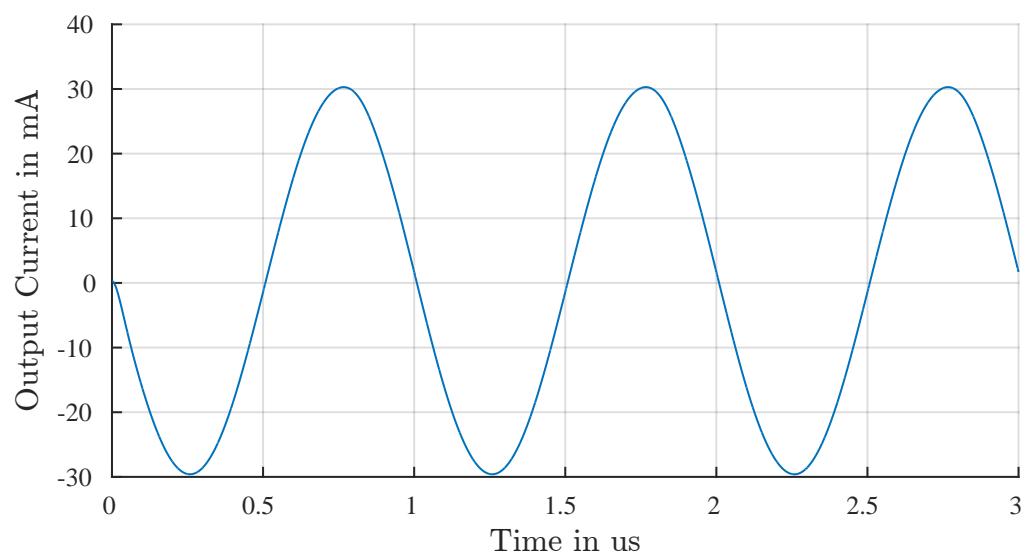


Figure 3.19.: OPAMP Plot of Ourput Current vs time

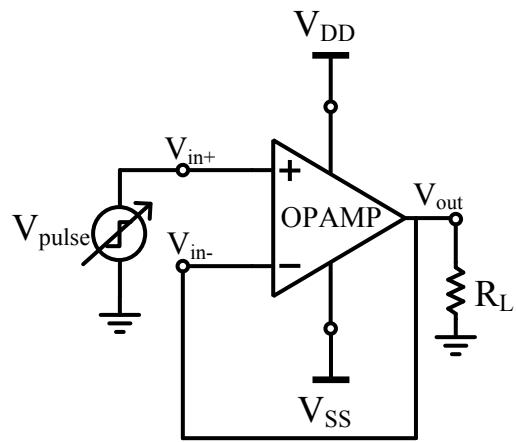


Figure 3.20.: Test setup for Transient Analysis - Square Wave Input

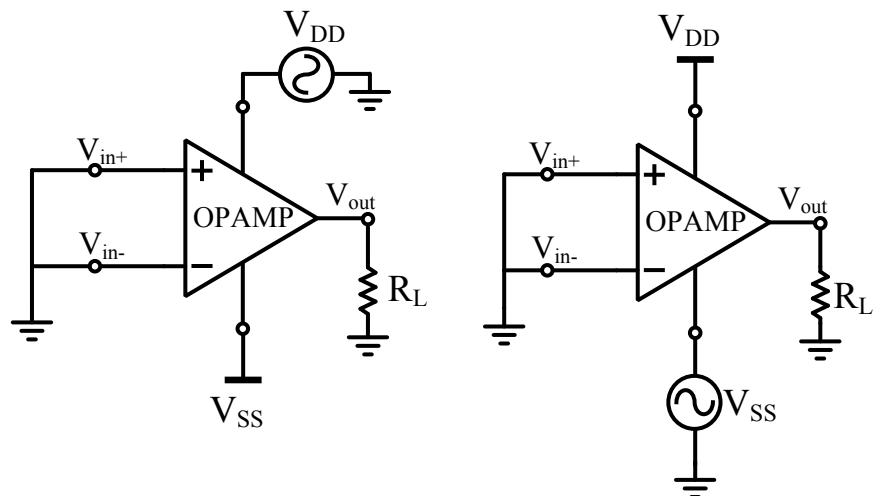


Figure 3.21.: Test setup for calculating PSRR

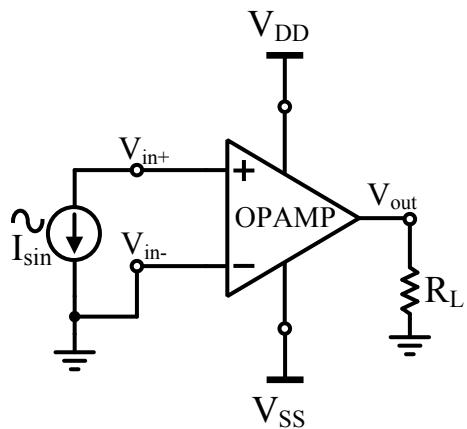


Figure 3.22.: Test setup for calculating Input Impedance

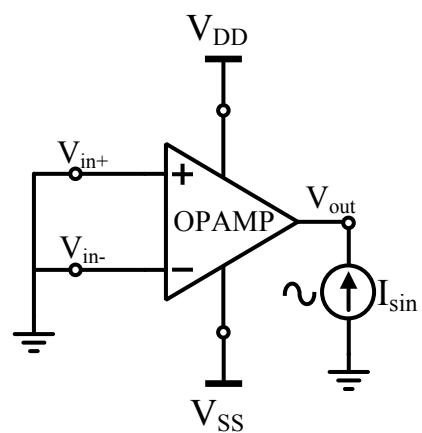


Figure 3.23.: Test setup for calculating Output Impedance

3.4 The Complete Design

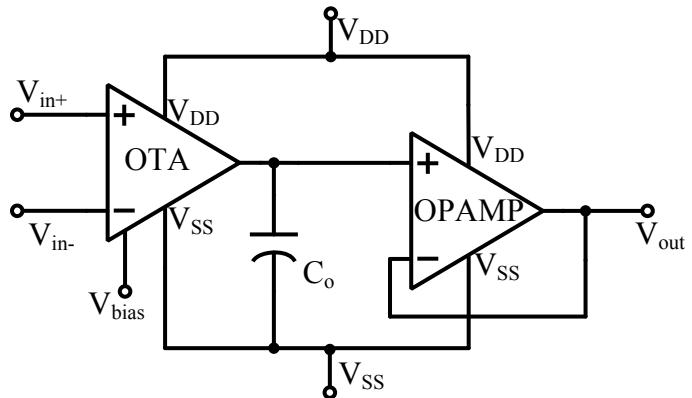


Figure 3.24.: Block Diagram of the Overall System

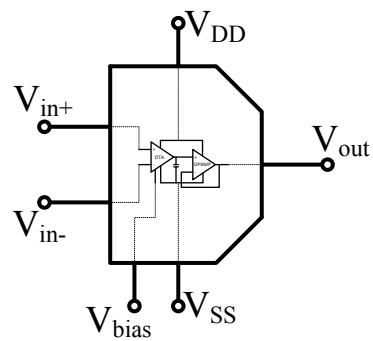


Figure 3.25.: Schematic Symbol for the Overall System

3.4.1 Schematic

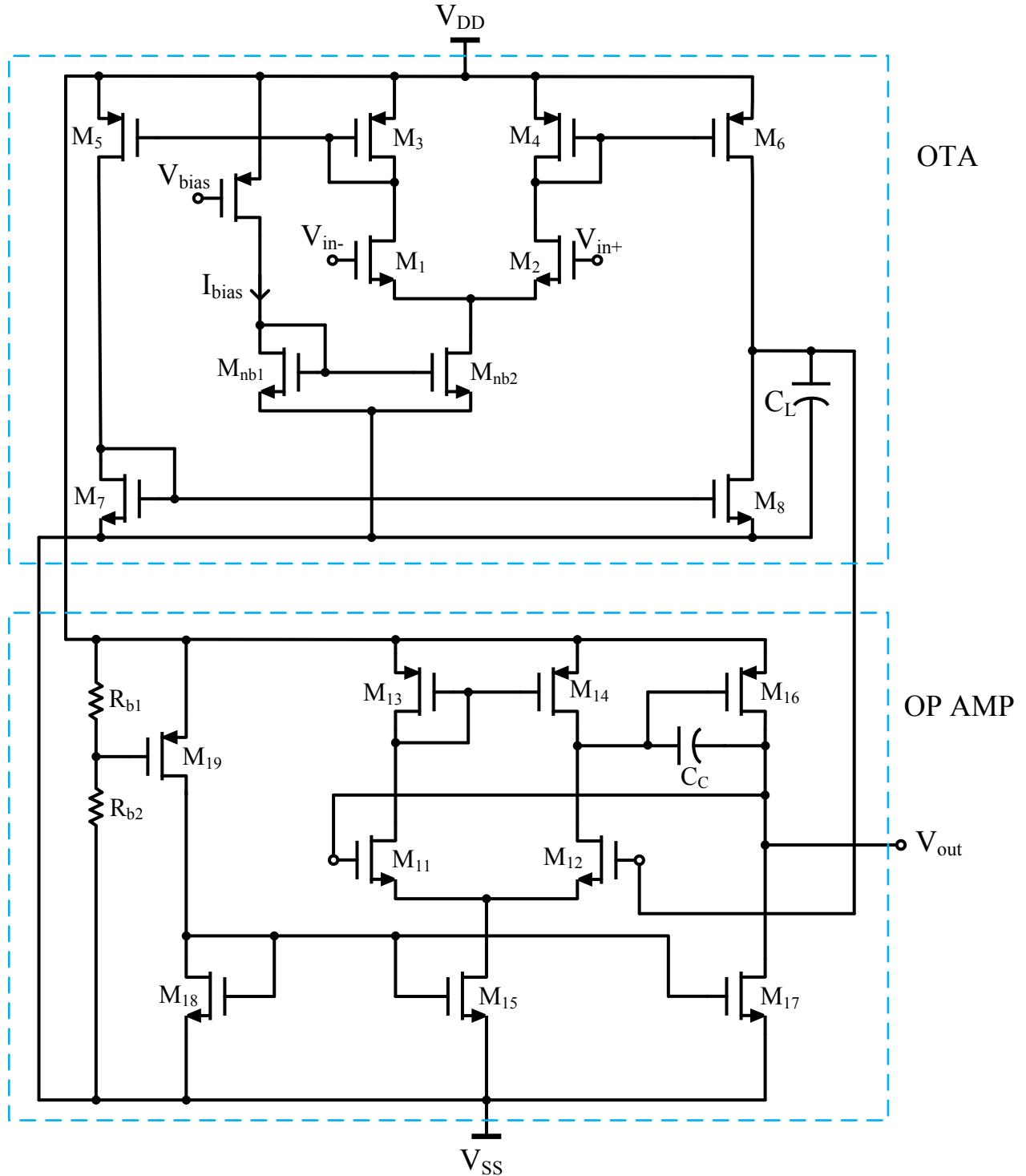


Figure 3.26.: Schematic Diagram for the Overall System

4 Simulation Results

4.1 DC Analysis

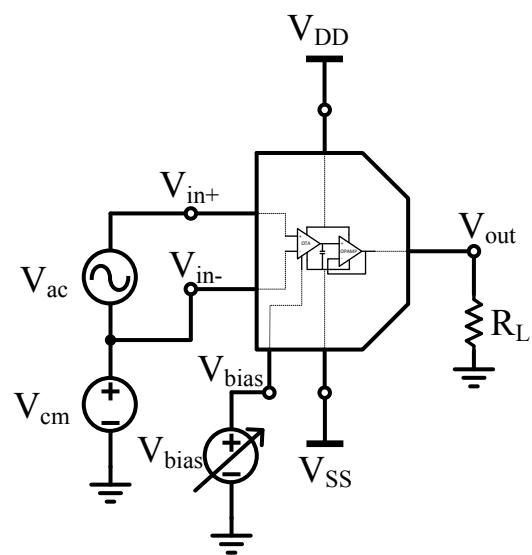


Figure 4.1.: Test setup for DC Analysis

4.2 AC Analysis

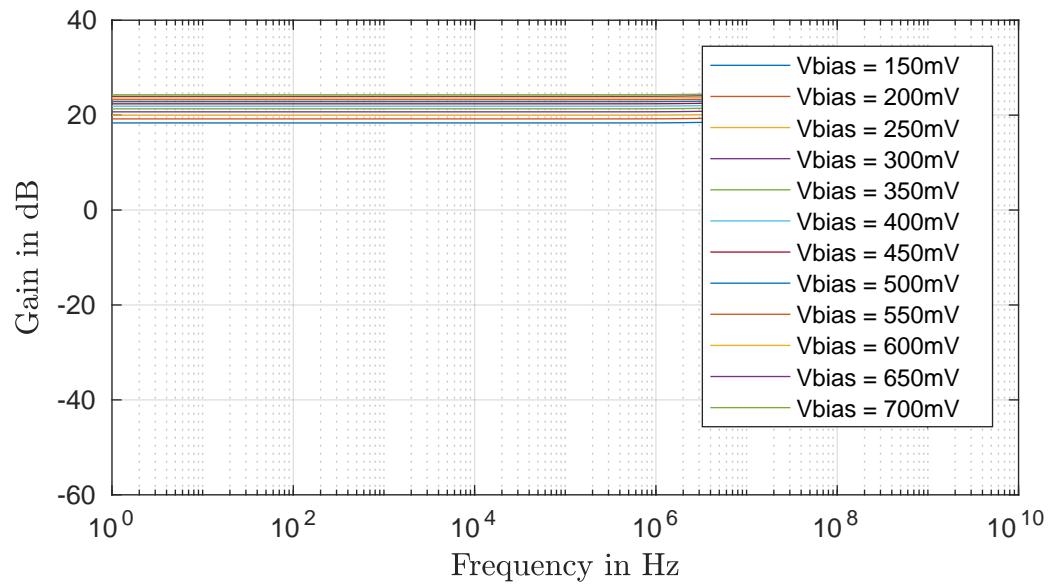


Figure 4.2.: Plot of Gain vs Frequency for different V_{bias}

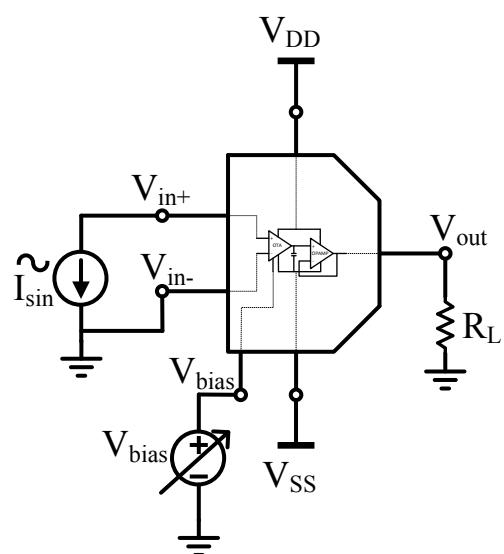


Figure 4.3.: Test setup to measure Input Impedance

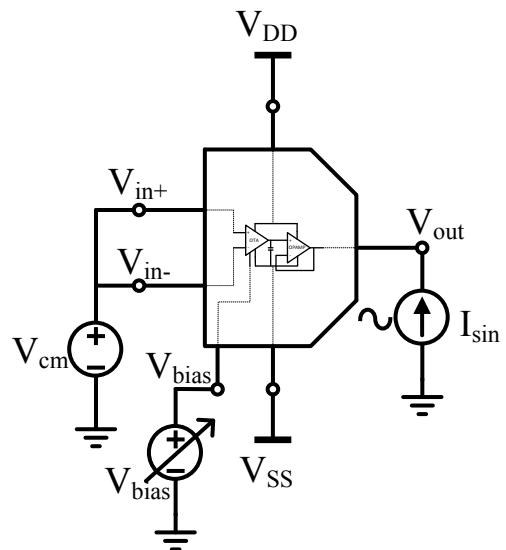


Figure 4.4.: Test setup to measure Output Impedance

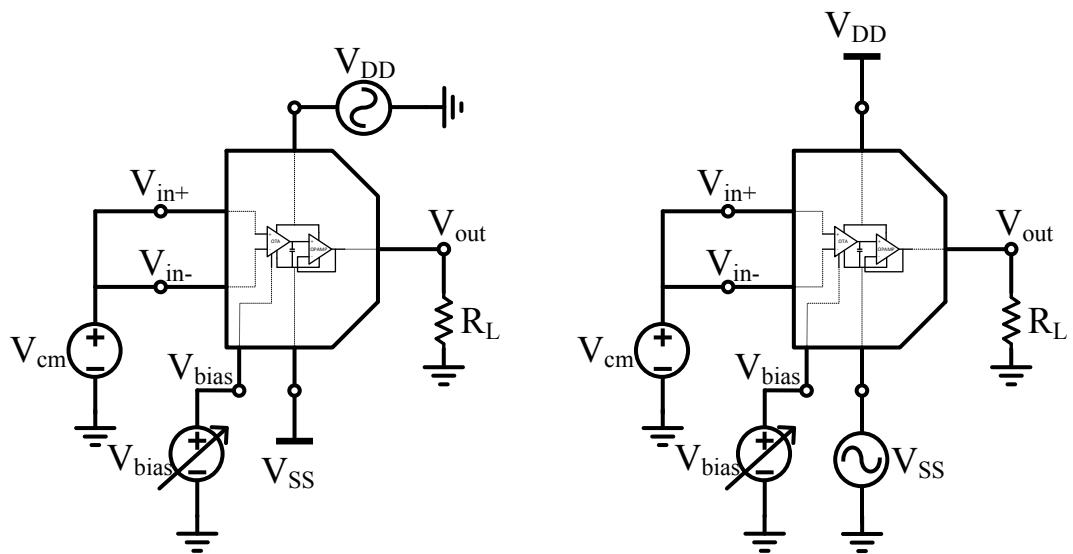


Figure 4.5.: Test setup to measure PSRR

4.3 Transient Analysis

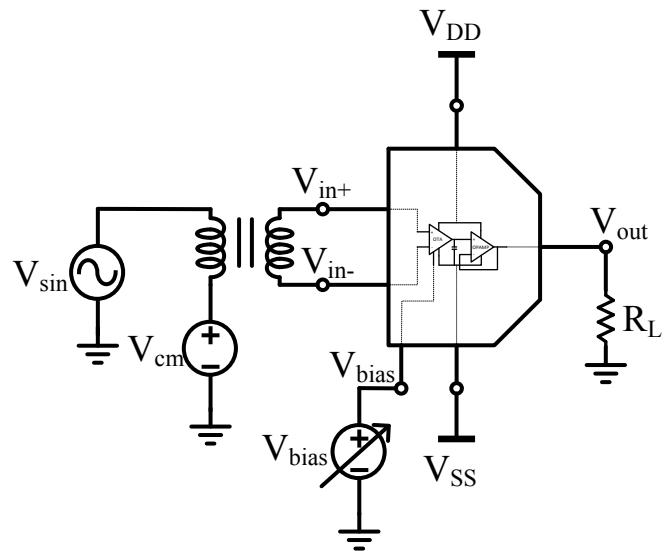


Figure 4.6.: Test setup for Transient Analysis - Sine Wave input

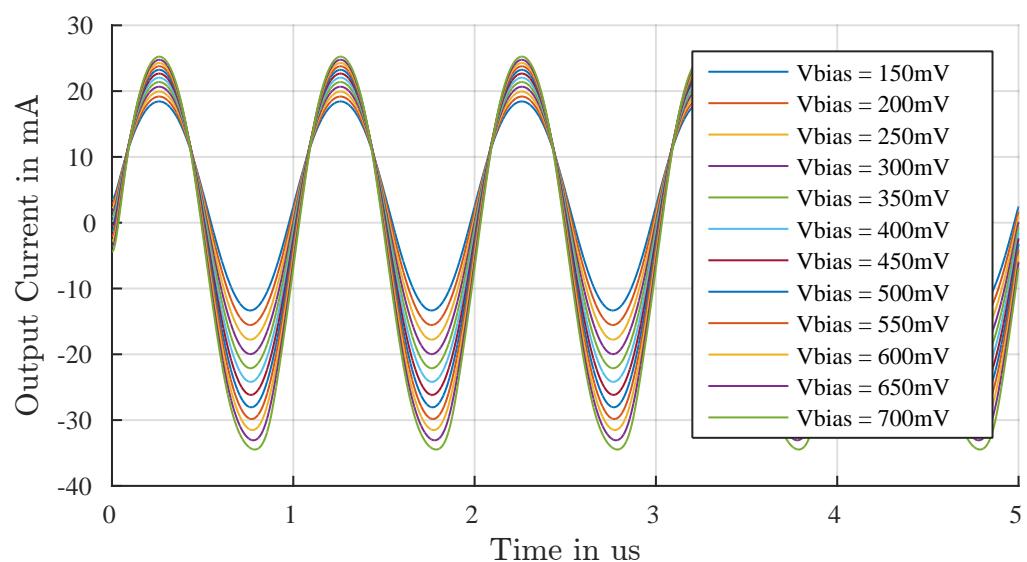


Figure 4.7.: Plot of Output Current vs time for different V_{bias}

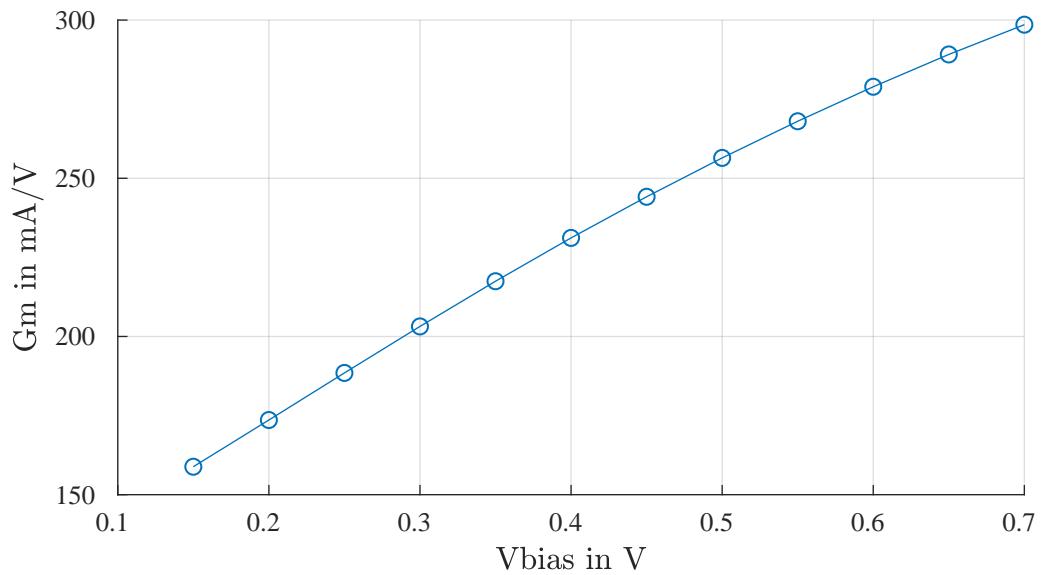


Figure 4.8.: Plot of G_m vs V_{bias}

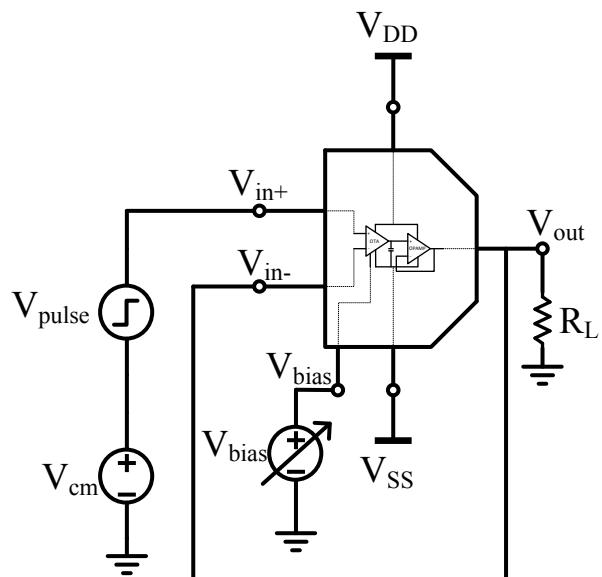


Figure 4.9.: Test setup for Transient Analysis - Square Wave input

4.4 Noise Analysis

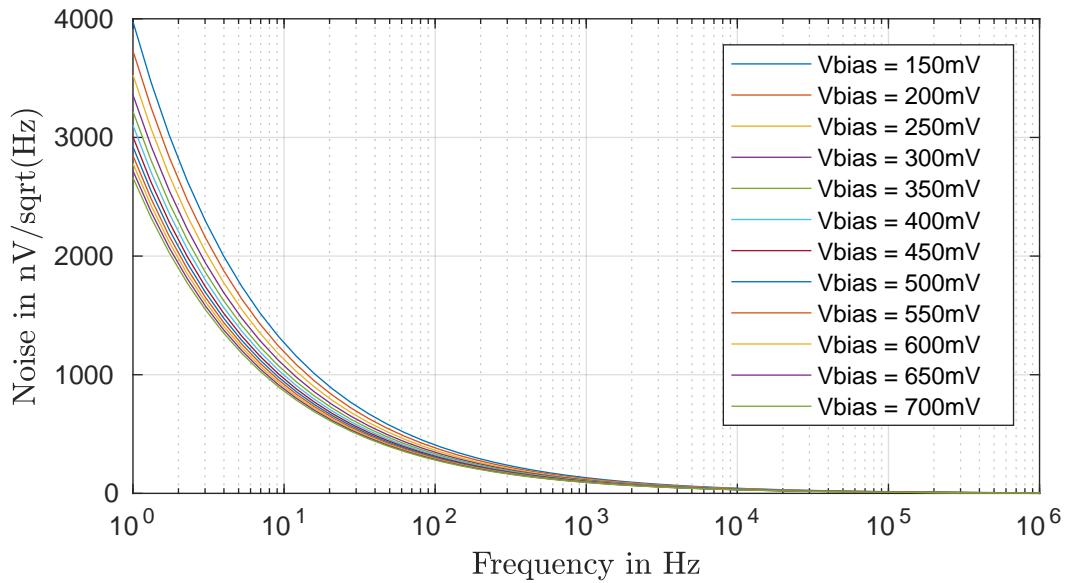


Figure 4.10.: Plot of Input Referred Noise vs Frequency for different V_{bias}

4.5 Pragammable Load

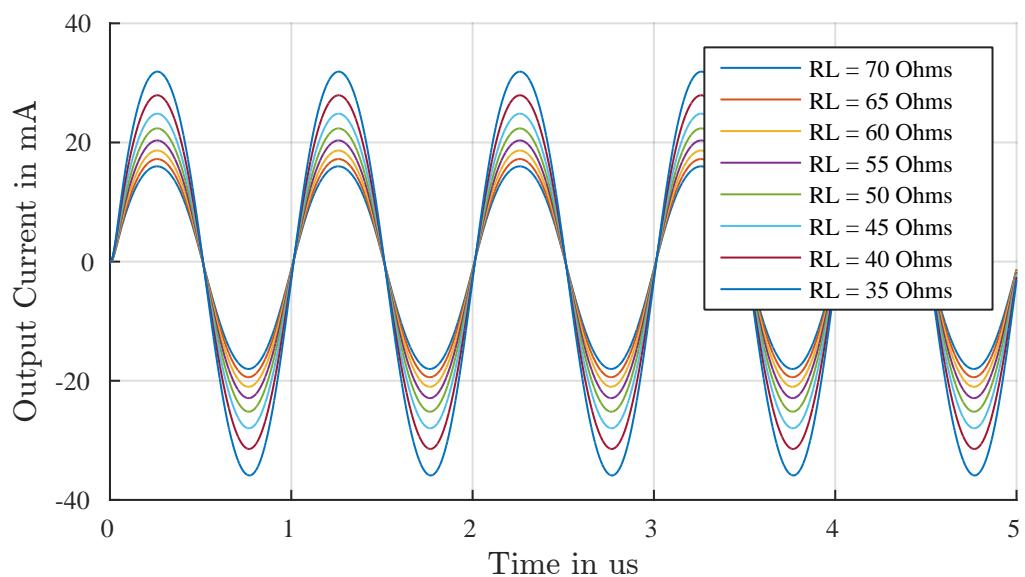


Figure 4.11.: Plot of Output Current vs Time for different R_L

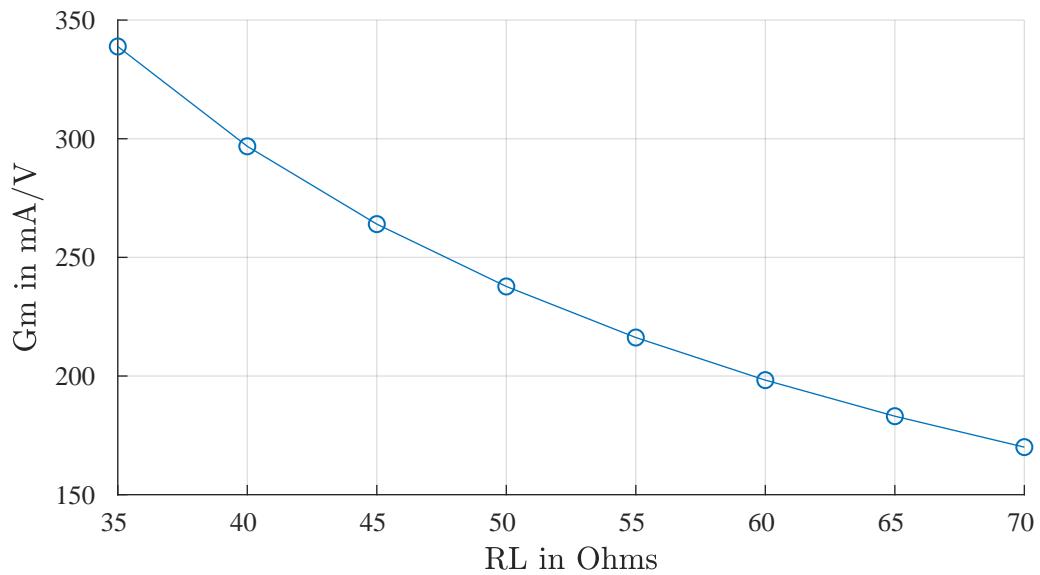


Figure 4.12.: Plot of Output Current vs time for different RL

4.6 Corner Simulation

4.6.1 Process Variation

4.6.2 Process and Supply Variation

4.6.3 Process, Voltage and Temperature (PVT) variation

4.6.4 Summary of PVT Corner Analysis



5 Conclusion

5.1 Summary of Results

5.2 Outlook



A Appendix

