



# The Road Ahead

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*RISC-V China Summit 2022*



@risc\_v

# What we will discuss today

- 2021
- How we did it?
- 2022

# 2021



*More than 2,000,000,000 RISC-V  
cores deployed for profit!*

*16 ratified ISA Specifications  
Consisting of 44 Extensions!*

10 Committees,  
17 SIGs  
19 Task Groups



# How we did it?





# Why RISC-V?

- Cost
- Flexibility
- Ecosystem
- Our position in History
- EDA Renaissance
- Pride of Ownership

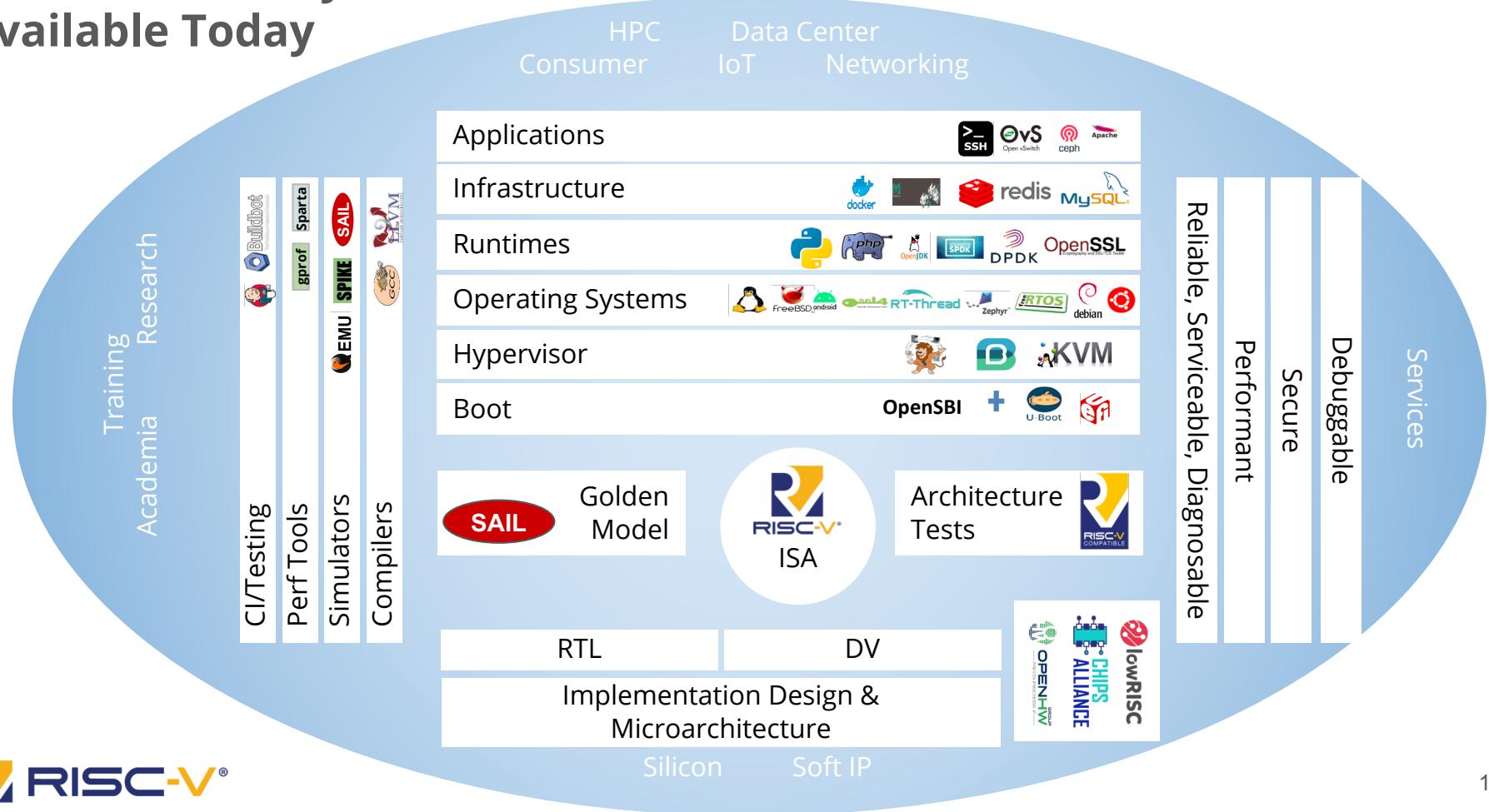
# 2022



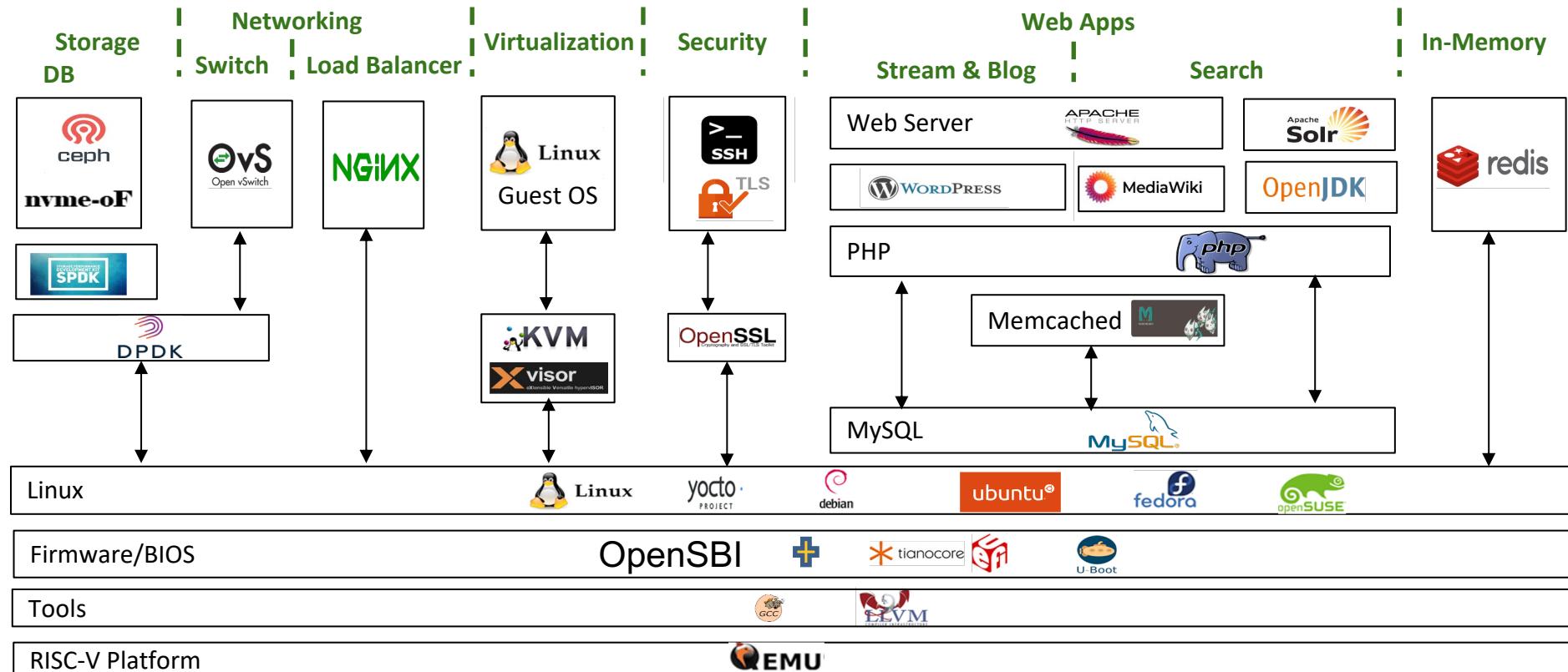
# Software Ecosystem



# Rich RISC-V Ecosystem Available Today



# Ventana Software Stack Examples Available Today



# Andes Partners: AI, Multimedia and Security Today

AI tools, SW and IP



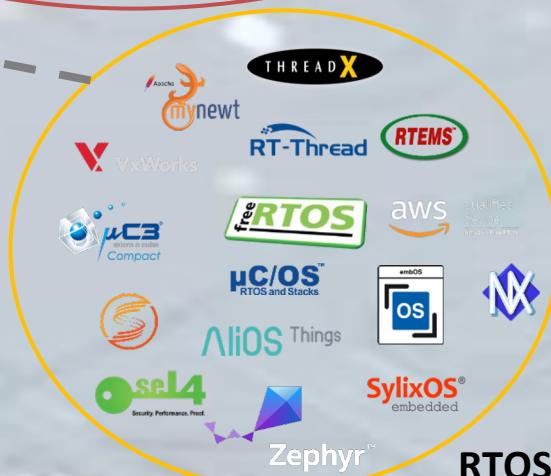
Security



DSP, Audio and Vision



Development tools  
Taking RISC-V® Mainstream



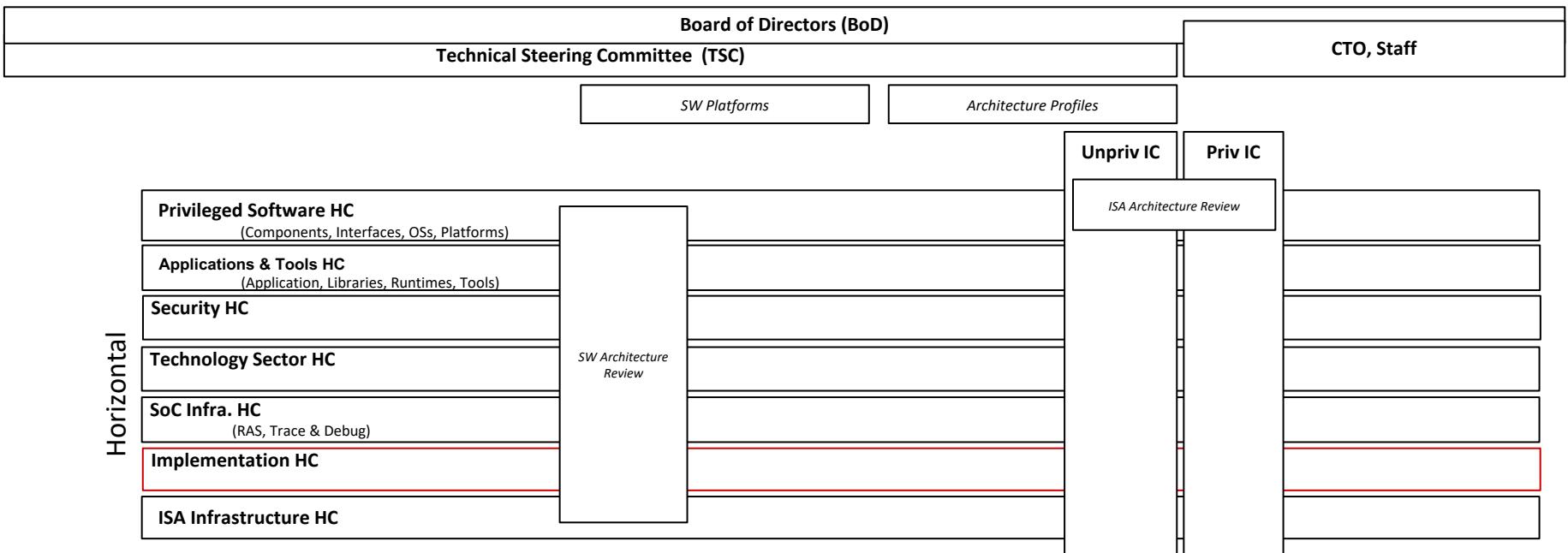
RTOS



# Organization



# Technical Organization

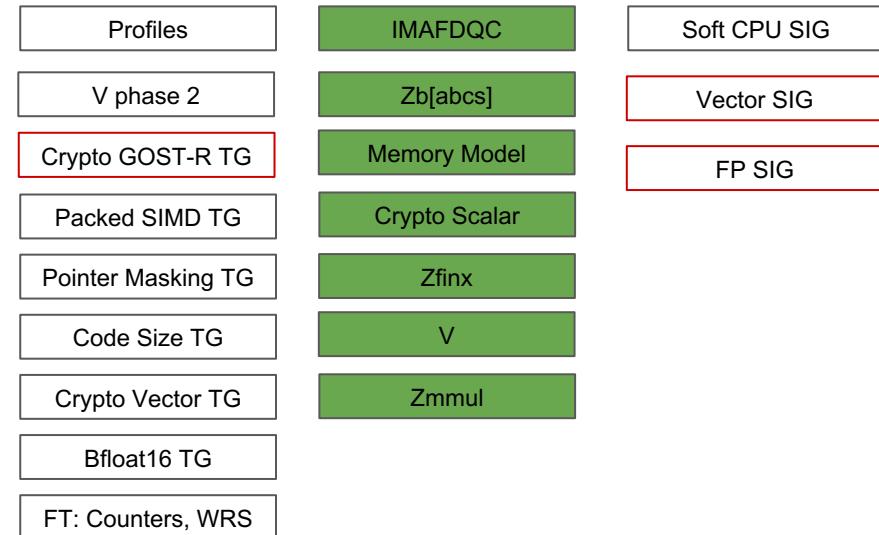


# ISA Committees

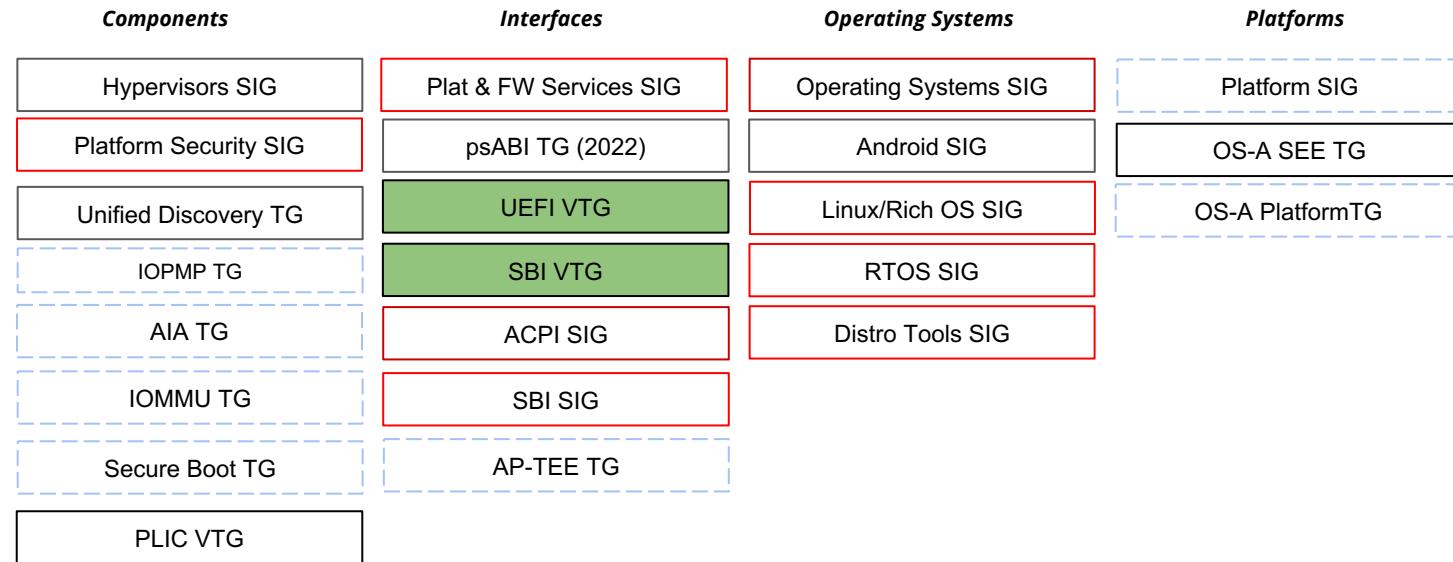
## Privileged IC



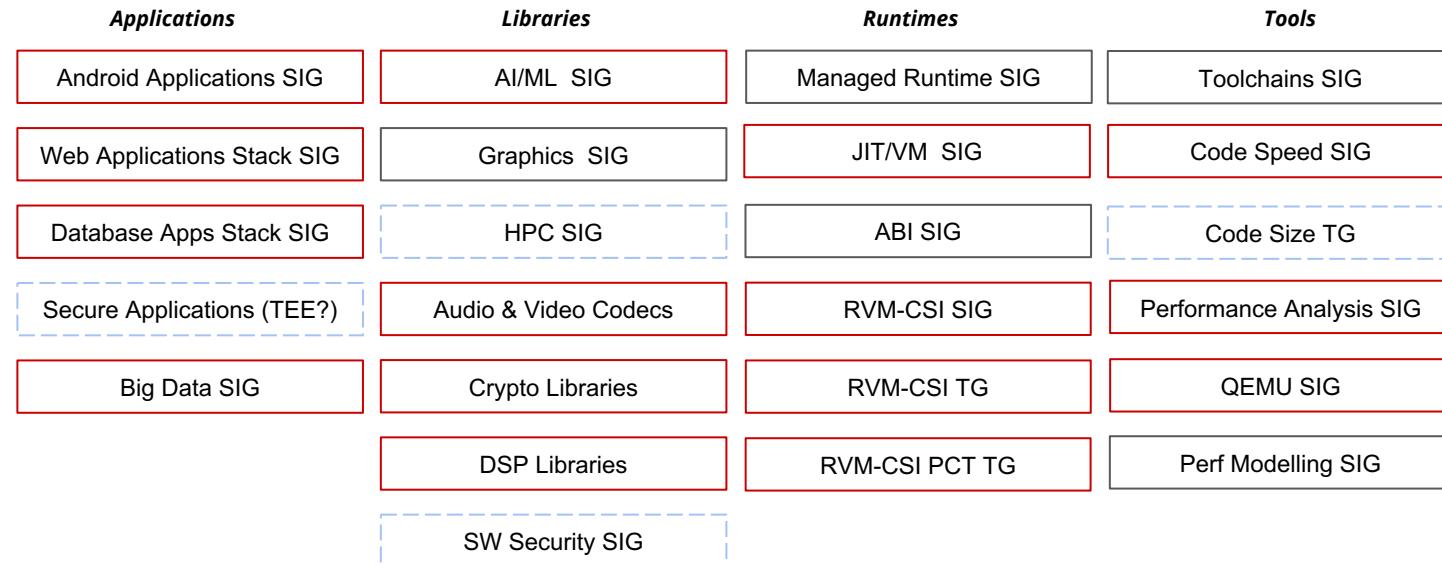
## Unprivileged IC



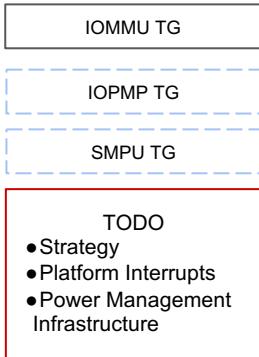
# Privileged Software HC



# Applications & Tools HC



## SOC Infrastructure HC



## Debug & Trace SIG

Debug v1.0 TG

Nexus TG

E-Trace Instruction (v1.0)

Debug 0.1X

E-Trace Instr. & Data TG (v2.0)

## RAS SIG

Functional Safety SIG

QOS SIG

RAS Error-record Register Interface (RERI) TG

RAS Terms & Definitions TG

**TODO**

- Diagnosability
- Recoverability
- Data poisoning containment
- PCIe error reporting

## Security HC

Crypto Vector TG

Crypto GOST-R TG

Security Model TG

Security Response SIG

Blockchain SIG

Control Flow Integrity SIG

Shadow Stack & Landing Pads for CFI TG

Microarchitecture Side Channel SIG

Trusted Computing SIG

AP-TEE TG

Secure Boot TG

Memory Safety SIG

IOPMP TG

SMPU TG



## ISA Infrastructure HC

Formal Specification Strategy  
Architecture Tests Strategy

Architecture Tests SIG

Simulators SIG

Documentation SIG

C/I Regression Tests SIG

Performance Modeling SIG

Golden Model SIG

## Technology Sectors HC

Embedded SIG

Data Center SIG

Fast Interrupts TG

Code Size TG

psABI TG

Packed SIMD TG

Debug TG

HPC SIG

TODO

- Networking
- Wireless
- Edge
- Automotive
- Embedded

## Implementation Virtual HC

*Final Cost/Benefit/  
Completeness Checks by  
SW & Unpriv & Priv  
Committee chairs*



# Specifications



# Types of Specifications

- ISA
  - Defines an extensions to be part of the ISA
- Non-ISA
  - Part of the HW or SW ecosystem that interacts with the RISC-V ISA
- Profiles
  - Specifies a set of ISA extensions that work together in order to minimize the targets for toolchains and operating systems.
  - Includes extensions and extension options that may be declared mandatory or optional or unsupported
- Architecture Overviews/Definitions
  - Provides the big picture about how pieces of other specifications fit together and how implementers can produce solutions from the specifications
  - May have prescriptive and best practices components
- Hybrids
  - specs including ISA and Non-ISA are considered ISA. minimal ISA impacts may be done as fastacks or part of a priv spec update

# 2022 Specifications

- Anchor Specifications
  - Profile: RVI20, RVA20, RVA22
  - ISA: Zvk
- Ratified Already
  - ISA: Zmmul
  - Non-ISA: E-Trace, SBI, UEFI
- Frozen
  - Profiles: RVI20, RVA20, RVA22
  - ISA: RV32E/64E, Zawrs, AIA
  - Non-ISA: PLIC, psABI
- Expected (not guaranteed)
  - ISA: Zc\*, Zfb\*, Zvfh, Zcfb\*, Zfa, Zjmp, Zjid, Ztso, Zfhmin, Zihintntl
  - Non-ISA: Unified Discovery, IOMMU, PRS 2022 (platform runtime services - SBI, UEFI, etc.)

# 2023 Specifications

- Anchor Specifications
  - Profiles: RVA23
- Expected or Investigating
  - ISA: P, Matrix, SPMP, Zc\* phase 2,
  - Non-ISA: SEI, Nexus, PRS 2023, IOPMP, Shadow Stack & Landing Pads, Secure Boot, AP-TEE, Security Domains
  - Architecture Overviews/Definitions: SEE, RAS, Security

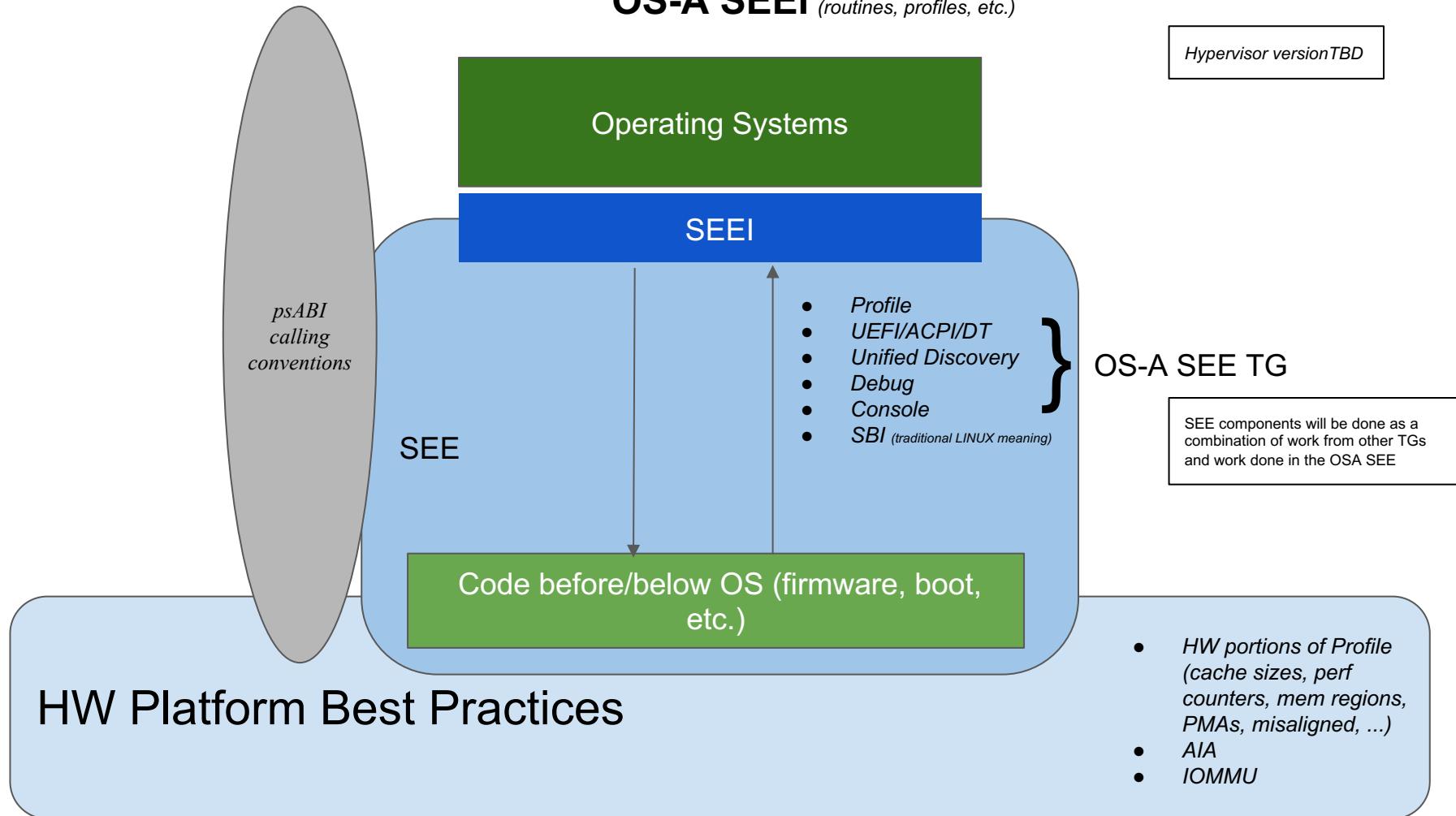
# Profiles are ...



- A mechanism to identify a group of extensions (instructions, behavior, state) that work together
- Like macros. Profiles consist of Extensions. Extensions consist of a group of rules, state, and behaviors or other extensions
- What we ask the upstream projects (gcc, binutils, llvm, ...) and Linux distros to target. Major and minor releases
- The way we reduce fragmentation in the RISC-V community

extension name - best guess	ratification package name	ratification package name	description (what this does, in English)	ratified (y/n)	ratified year (or expected) or future	RV I20	RVA20 (64 only)	RVM20	RVA22 (64 only)	RVM22	RVA23	RVM23				
					might make add a "?" after the year	m - Mandatory s - Supported Optional u - Unsupported Optional r - Unsupported Optional but part of a rollup that is in whole Supported or Mandatory i - Incompatible x - Not ratified at the date of the profile n - Not Applicable										
RVI32 is only applicable to RVM and RVI profiles																
Mode																
A	A	A	Atomics	y	2019	s m m m s s s m m m s s s	u u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m				
C	C	C	Compressed instructions	y	2019	s m m m s s s m m m s s s	u u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m				
D	D	D	floating point, double-precision (implies F)	y	2019	s m m s s s s m m m s s s	u u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m				
E	RVE32	RVE32	integer base for RVE32	y	2019	x i i i m m m i i i m m m	u u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m				
F	F	F	floating point, single-precision	y	2019	s m m s s s s m m m s s s	u u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m				
RVI32	RVI32	RVI32	integer base for RVI32	y	2019	m m m m m m m m m m m m m m	u u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m				
RVI64	RVI64	RVI64	integer base for RVI64	y	2019	m m m m m m m m m m m m m m	u u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m				
M	M	M	multiply/divide	y	2019	s m m m s s s m m m m m m	u u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m				
misaligned 32			misaligned loads and stores	y	2019	s s s s s s s s s s s s s s	u u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m				
misaligned 64			misaligned loads and stores	y	2019	?	s s s s s s s s s s s s s s	u u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m			
Q	Q	Q	floating point, quad-precision (implies F&D)	y	2019	u u u u u u u u u u u u u u	u u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m				
Sm1p11	priv 1.11	priv 1.11	m mode priv instructions and state	y	2019	s n n m n n m n n i n n i	u u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m				
Ss1p11	priv 1.11	priv 1.11	s mode priv instructions and state	y	2019	s n m m n s s n i n i i	u u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m				
Zaamo	A	A	AMOs	y	2019	r r r r r r r r r r r r r r	u u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m				
Zalrsr	A	A	LR/Store Conditional atomics	y	2019	r r r r r r r r r r r r r r	u u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m				
Zicntr	Counters	Counters	XXX priv counter in priv spec. is this just of RVI?	y	2019	s m m m s s s m m m m s s s	u u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m				
Zicsr	Zicsr	Zicsr	access CSRs	y	2019	u u s m u s m u s m u s m u s m	u u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m				
Zifencei	Zifencei	Zifencei	instruction fence	y	2019	s m m m s s s m m m m s s s	u u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m				
Zihpm	Priv 1.11	Priv 1.11	s mode priv instructions and state	y	2019	s m m m s s s m m m m s s s	u u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m	u s m u s m u s m u s m u s m u s m				

# OS-A SEEI (routines, profiles, etc.)



# Beyond the Backlog

- Automotive
  - AGL & Yocto & Realtime
  - Functional Safety (ASIL, ISO 26262)
- Datacenter
  - Databases
  - Accelerators
    - Graphics & ML/AI/NLP
      - Matrix Ops
  - Emulation Support
    - x86, Arm
  - Virtualization
  - Smart NICs
- ISA Gaps
  - RV32E, RV64E, RV128I
  - Software Ecosystem Libraries
  - Android
- Security
  - uArch
  - Robustness
  - Security Model
  - Ecosystem
- Ecosystem
  - 3rd party ISVs (e.g. VMware or OracleDB)
  - Libraries (security, graphics, etc.)
  - Distros

Join!  
Contribute!  
Make History!  
*#riscvewhere*



# Thank You!

