RISC-V Summit China 2023

Enhance UEFI on RISC-V

- MultiArchUefiPkg - Bringing RISC-V and IHV Ecosystems Together
- StandaloneMmPkg - Bringing UEFI Secure Execution to RISC-V

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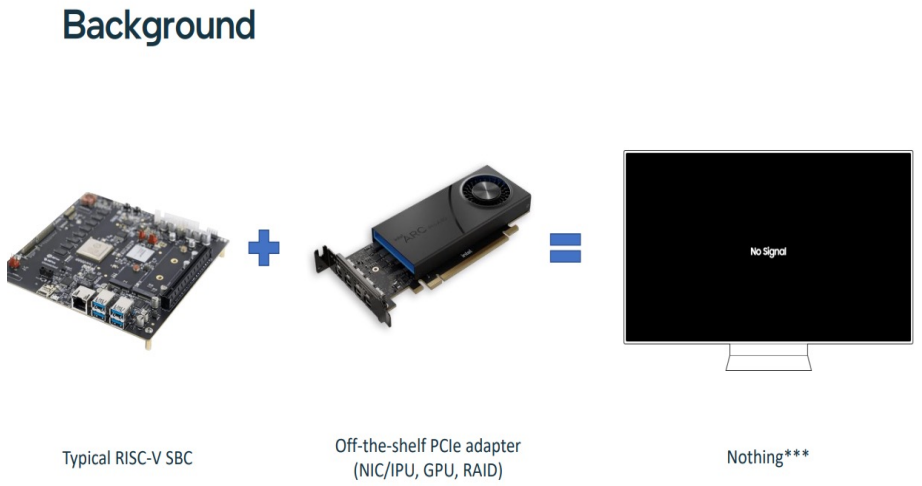
 This document contains information on products and/or processes in development.

MultiArchUefiPkg - Bringing RISC-V and IHV Ecosystems Together

- Today ➔ Non-standard RISC-V platforms, that don't lend to building to horizontal market segments where interoperability is key
- Tomorrow ➔ An interoperable RISC-V ecosystem that allows building servers and PCs

How to make existing PCIe devices work?
Will future PCIe devices ship with RISC-V firmware drivers?



MultiArchUefiPkg – Option ROM Emulation

Status:

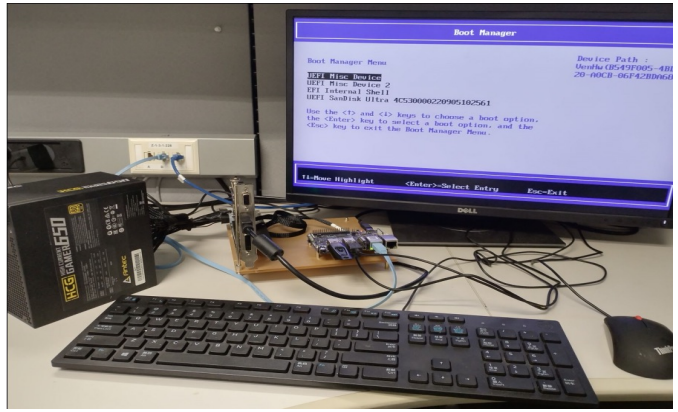
- 64-bit x64 and AArch64 instruction emulation
- Supports 64-bit RISC-V UEFI hosts
- Abstracts Qemu/TCG with Unicorn Engine API
- Verified on RiscVVirt w/ PCIE passthrough
- Verified on VisionFive2 SBC

Homepage and Source Code:

- *https://wiki.riseproject.dev/display/HOME/EDK2_00_01+-+MultiArchUefiPkg*
- *https://github.com/intel/MultiArchUefiPkg*

Next Step:

- Verify on more platforms
- Correctness, perf, code size and etc



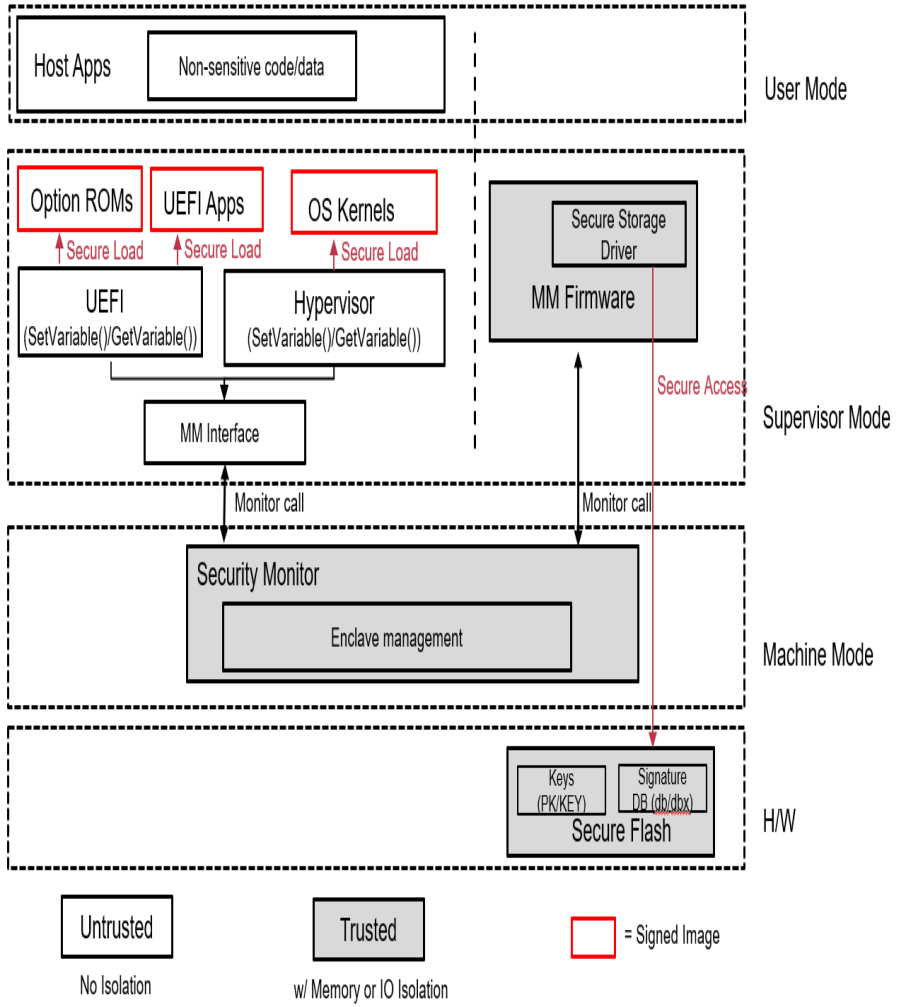

```
7A 0000000A ? - -  -  - Usb Keyboard Driver
7B 00000011 ? - -  -  - Usb Mass Storage Driver
83 13000406 ? - -  -  - Intel(R) GOP Driver [19.0.1030]
FS0:\> drivers
```

StandaloneMmPkg – Bringing UEFI Secure Execution to RISC-V

- UEFI Secure Execution Environment ➔ A software sandbox environment running in the Secure World, under the control of privileged software, to instantiate PI Standalone Management Mode, in order to execute MM (secure) services.
- Typical Use Case ➔ UEFI secure boot service do the authentication and update variables for ensuring that code launched by the UEFI firmware is trusted and that each efi payload loaded is authenticated.

How to ensure the UEFI Secure Execution on RISC-V is secure ?

How will the secure implementation be on RISC-V based servers and PCs ?



StandaloneMmPkg – UEFI Secure Service

Status:

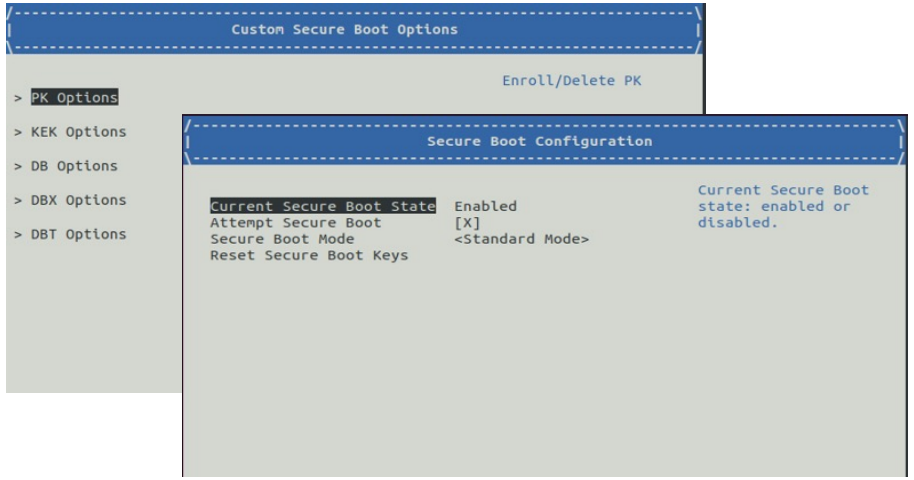
- Supports both PMP/sPMP and CoVE based TEE
- Prototyped with Penglai and Salus on QEMU
- Verified UEFI secure variables service
- Verified UEFI secure boot flow

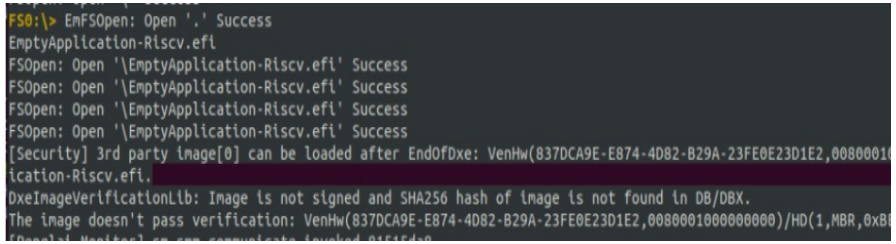
Homepage and Source Code:

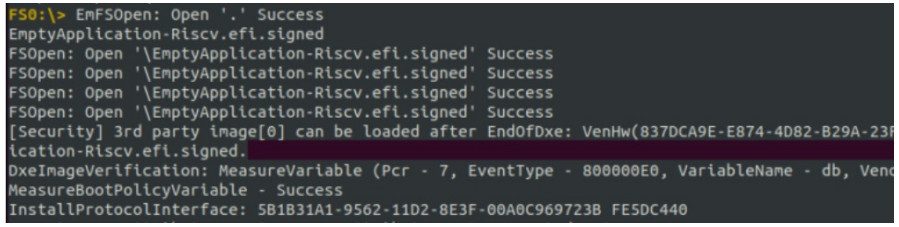
- https://wiki.riseproject.dev/display/HOME/EDK2_00_02+-+StandaloneMmPkg
- https://github.com/tianocore/edk2-staging/tree/RiscV64StandaloneMm

Next Step:

- UEFI PI and BRS-I update
- Code upstream, port to real hardware platform
- Secure firmware upgrade, management services ..







- https://riseproject.dev

RISE is focused on positive and transparent collaborations with upstream projects to deliver commercial-ready software for various use cases

https://www.intel.com/content/www/us/en/developer/articles/community/rising-to-the-challenge-risc-v-software-readiness.html

- RISE Firmware WG
  https://wiki.riseproject.dev/display/HOME/Firmware+WG
- UEFI on RISC-V Firmware Mailing List
  https://groups.google.com/a/riscv.org/g/fw-exchange
- More projects Intel China team is working on

Topic	When
RISC-V Vector Support on Valgrind	August 25 6pm
Best practice to optimize SW with vectorization on RISC-V	Poster
RISC-V firmware solution	August 24 4:30pm
Enhance UEFI on RISC-V	August 24 4:20pm
Enabling compliance test for RISC-V BRS	August 24 3pm
The ACRN/RISC-V project: embedded hypervisor design and status update	August 24 5pm

Welcome to Join RISC-V UEFI Firmware Development and Feedback Needed !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