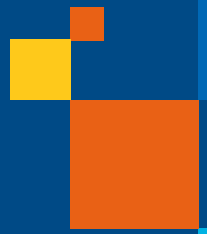
Enabling compliance test for RISC-V BRS

Haibo Xu <haibo1.xu@intel.com>
Andrei Warkentin <andrei.warkentin@intel.com>
Yin Wang <yin.wang@intel.com>



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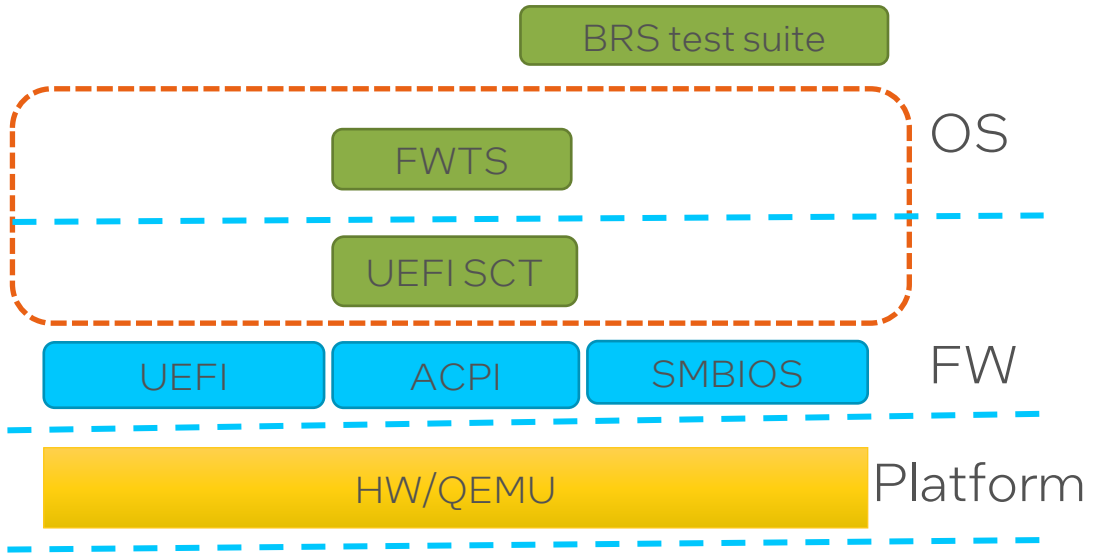
Background

- With the growing number of RISC-V implementations, there is a need for a standardized way to ensure interoperability across different RISC-V platforms
- RISC-V BRS specification defined some requirements (based on SBI/UEFI/ACPI/SMBIOS/DT etc.) for Boot and Runtime services that system software can rely on
- A compliance test suite can provide standardization and ensure that platform SW implementations adhere to the RISC-V BRS specification and maximize out of box software compatibility and interoperability

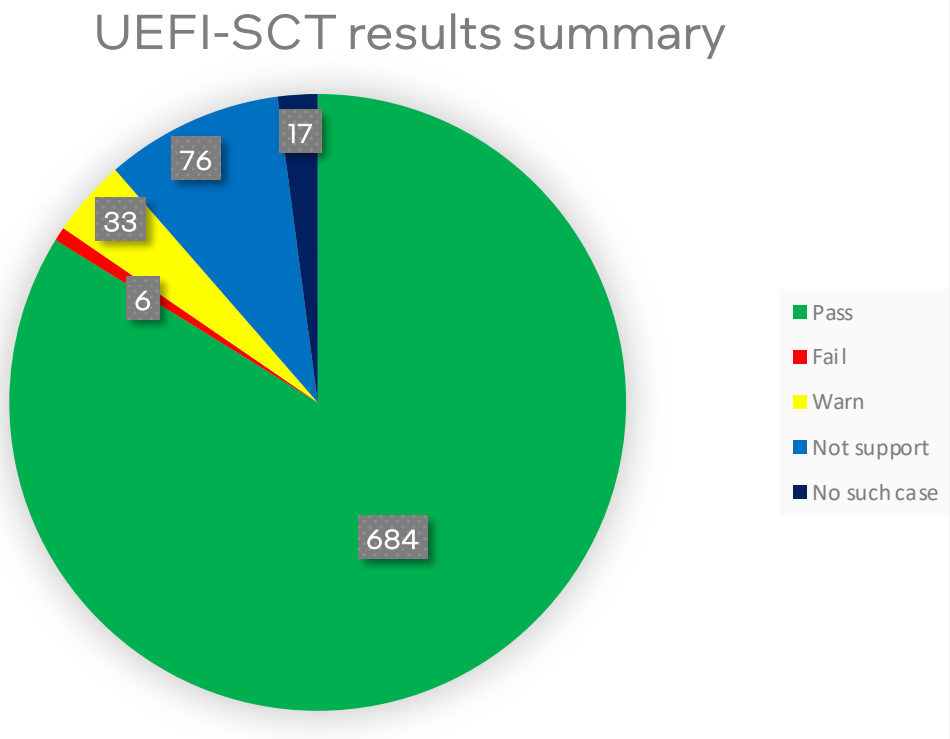
Current Status

- The RISC-V BRS Spec outlines requirements for Boot&Runtime Services based on RVI and industry standard firmware interfaces
  - https://github.com/riscv-non-isa/riscv-brs
  - Freeze Milestone – Spec development stable
  - Ratification Milestone Target Date – Q4' 23
- The RISC-V BRS test suite checks for RISC-V platform compliance against BRS Spec based on UEFI-SCT and FWTS test suite
  - https://github.com/intel/rv-brs-test-suite
  - Results on a Qemu virt platform was ready
  - More test cases are under development



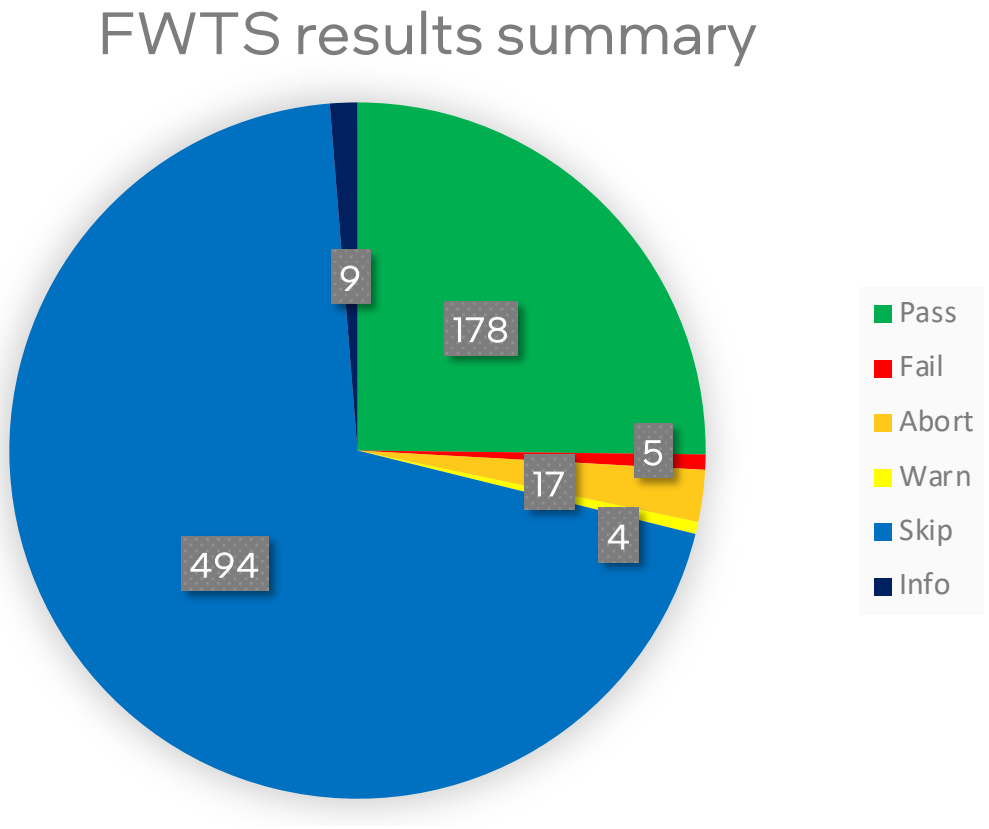
UEFI SCT Results

- UEFI-SCT: Test framework for UEFI firmware compatibility.
- 800+ test cases, 5k+ checkpoints from SCT test pool.
- Covers ~75% UEFI case of BRS spec.
- ~85% pass rate on RV64 QemuVirt platform.



FWTS Results

- Designed to validate and test different aspects of firmware
- ~700 test cases covering ACPI, SMBIOS, UEFI, Utilities
- ~70% test cases were skipped on RISC-V platform for lacking corresponding ACPI tables and UEFI features



Key Gaps & Call to Action

- ACPI tables - (Qemu/UEFI/Kernel)
  - PPTT/MCFG/SLIT/BERT/EINJ/ERST/HEST etc.
- Secure boot and variable – (UEFI)
- Join the discussion and review for BRS specification
  - https://github.com/riscv-non-isa/riscv-brs
  - https://lists.riscv.org/g/tech-brs
- Collaborate on the rv-brs-test-suite
  - https://github.com/intel/rv-brs-test-suite/issues/9
  - https://github.com/intel/rv-brs-test-suite/issues/12
  - Linux/Qemu ACPI
  - UEFI-SCT
  - FWTS

- https://riseproject.dev

RISE is focused on positive and transparent collaborations with upstream projects to deliver commercial-ready software for various use cases

How: Align on highest priorities & avoid (accidental) duplication of work
Goal: Accelerate open source SW for RISC-V architecture

https://www.intel.com/content/www/us/en/developer/articles/community/rising-to-the-challenge-risc-v-software-readiness.html

Finding more interesting topics from Intel on RISC-V summit China 2023

Topic	When
RISC-V Vector Support on Valgrind	August 25 6pm
Best practice to optimize SW with vectorization on RISC-V	Poster
RISC-V firmware solution	August 24 4:30pm
Enhance UEFI on RISC-V	August 24 4:20pm
Enabling compliance test for RISC-V BRS	August 24 3pm
The ACRN/RISC-V project: embedded hypervisor design and status update	August 24 5pm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