Syntacore™
Custom cores and tools

Is RISC-V ready for the application class workloads?

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About Syntacore

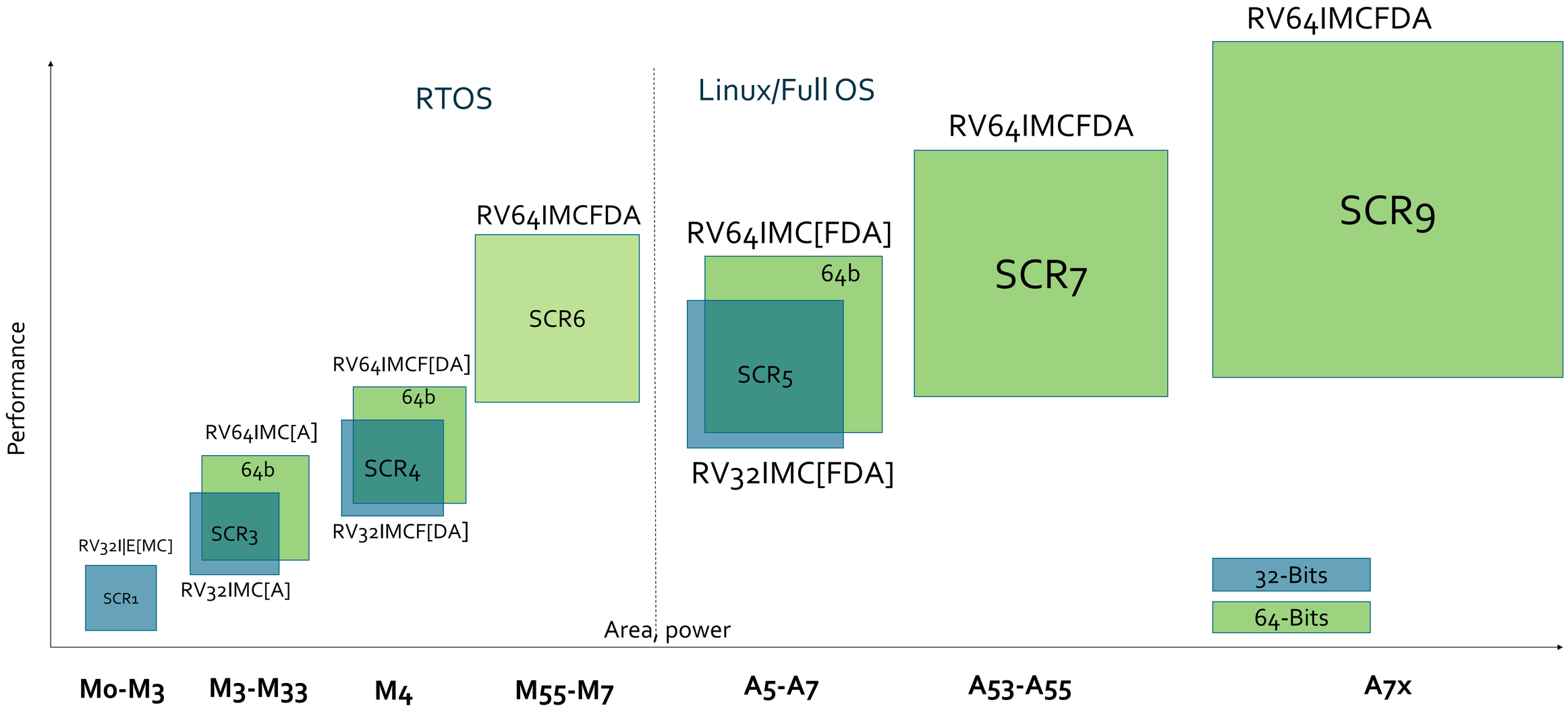
Semiconductor IP company, founding member of RISC-V foundation

Est 2015, 200+ EEs

State-of-the-art RISC-V CPU IP line with competitive features + turnkey customization

- RISC-V client silicon in 2016, RISC-V Linux-capable IP in 2016, full-wafer from 2017
- Projects on 10+ nodes at 5 foundries (230 to 5nm):
  - ✓ IoT: active battery-less SoC @22nm (extensive power optimization, ntv-ready)
  - ✓ HPC: 50+ cores heterogeneous SoC @7nm (64bit, NuMA, system arch customization)

SCRx product line



State-of-the art RISC-V CPU IP family

Features			RTOS/ Bare Metal				Linux/ "Full" OS		
			SCR1* (FREE!)	SCR3	SCR4	SCR6	SCR5	SCR7	SCR9
Width		32bit	●	●	●		●		
		64bit		●	●	●	●	●	●
ISA			RV32I|E[MC]	RV[32|64]IMC[A]	RV[32|64]IMCF[AD]	RV64IMCAFD	RV[32|64]IMC[AFD]	RV64IMCAFD[V]	RV64IMCAFDV
Pipeline type			In-order	In-order	In-order	Superscalar	In-order	Superscalar	Superscalar
Pipeline, stages			2-4	3-5	3-5	10-12	7-9	10-12	10-12
Branch prediction				Static BP, RAS	Static BP, RAS	Dynamic BP, BTB, BHT, RAS	Static BP, BTB, BHT, RAS	Dynamic BP, BTB, BHT, RAS	Dynamic BP, BTB, BHT, RAS
Execution priority levels			Machine	User, Machine	User, Machine	User, Machine	User, Machine, Supervisor	User, Machine, Supervisor	User, Machine, Supervisor, Hypervisor
Extensibility/customization			●	●	●	●	●	●	●
Execution units	MUL/DIV	area-opt	●	○	○	○			
		hi-perf	○	●	●	●	●	●	●
	FPU				●	● [hi-perf opt]	●	● [hi-perf opt]	● [hi-perf opt]
Memory subsystem	TCM [w/ECC|parity]		●	●	●	●	●	○	○
	L1$ [w/ECC|parity]			○	○	●	●	●	●
	L2$ w/ECC			○	○	○	○	●	●
	MPU/PMP			●	●	●	●	●	●
	MMU, virtual memory						●	●	●
Debug	Integrated JTAG debug		●	●	●	●	●	●	●
	HW BP		1-2	1-8 adv ctrl	1-8 adv ctrl	1-8 adv ctrl	1-8 adv ctrl	1-8 adv ctrl	1-8 adv ctrl
	Performance counters		○	●	●	●	●	●	●
Interrupt Controller	IRQs		8-32	8-1024	8-1024	8-1024	8-1024	8-1024	8-1024
	Features		basic	advanced	advanced	advanced+	advanced+	advanced+	advanced+
SMP support					up to 4 cores with coherency			up to 8-16 cores	up to 8-16 cores
I/F options	AHB		●	○	○	○	○	○	○
	AXI		○	●	●	●	●	●	●
	ACE / CHI					○		○	○

Baseline cores:

- Clean-slate designs in System Verilog
- Configurable and extensible
- 100% compatible with major EDA flows
- Silicon-proven at the customers

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RISC-V

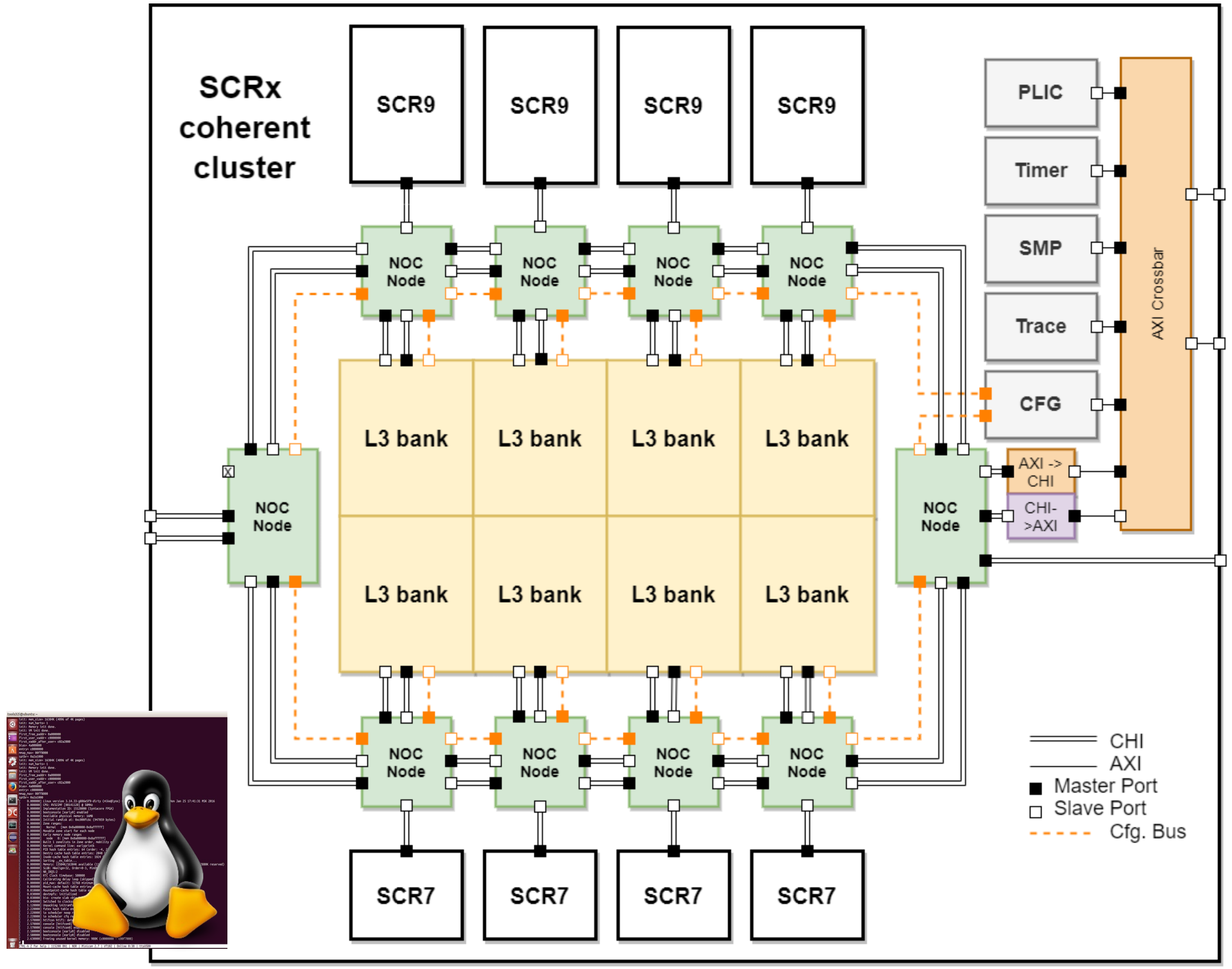
RV64 SCR9

Linux-capable application CPU with entry-level server class features:

- 8-16 cores per cluster
  - SMP and heterogeneous (~bigLittle w/SCR7)
- 12 stage OoO pipeline
- Coherent NoC-based L3
- CHI external i/f
- SV39, SV48
- RVV
- RVB
- Hypervisor
- AIA
- RVA22
- Accelerators support

- 7+ CM/MHz per core
- 2+ GHz @7nm

(*) some features may not be available in the initial release



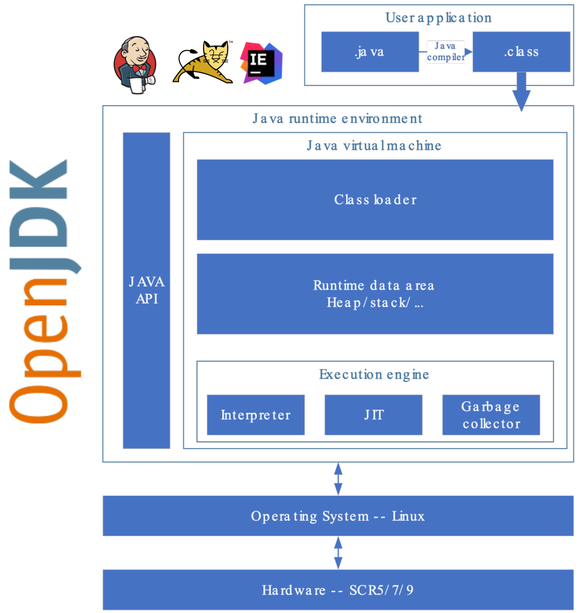
Select DC-class SW stacks running in the lab

LAPP = Linux + Apache + PostgreSQL + PHP

- Pillar enabling technology for web servers applications

OpenJDK 17u – Java execution environment

- Syntacore port based on “JEP 422: Linux/RISC-V Port”
- Additional optimizations for SCR cores (C, Zb*, V)
- Passed all OpenJDK regression tests
- Example application
- Jenkins, Apache Tomcat, Idea Community Edition



SCR9 hypervisor

Boot flow:

Virtualization tools:

- KVM 3.18.0, Qemu 7.2.0

Toolchain:

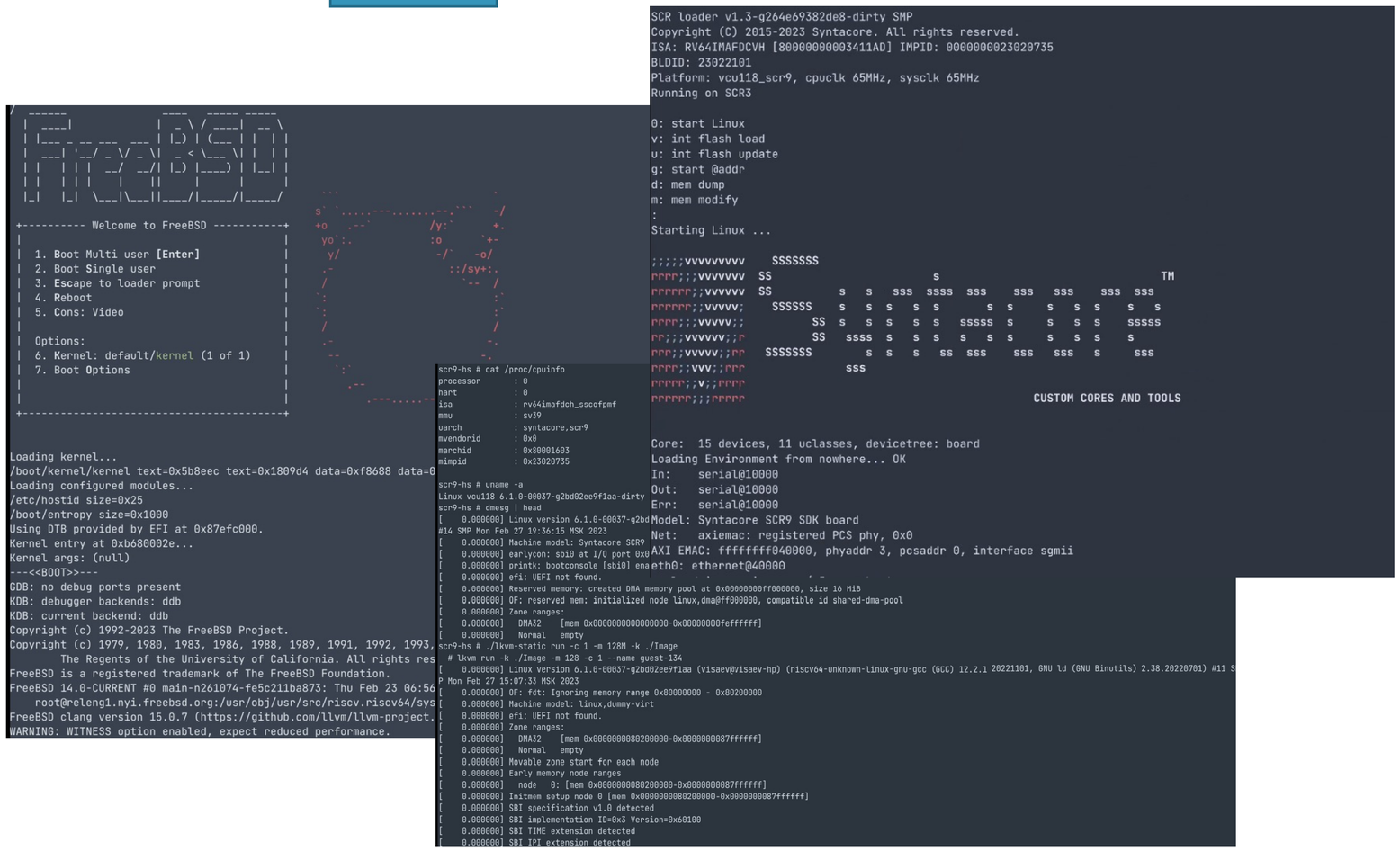
- SC - DT 2022.12, GCC 12.2.1 based

Host OS:

- Linux kernel 6.1

Guests OS:

- Linux Kernel 5.15
- Linux Kernel 6.1
- FreeBSD 14.0



Application class workload requirements

Client devices

1. 64bits, 8-16+ cores per cluster
2. Fmax 2..3+ GHz
3. Single cluster, cache hierarchy 2-3 levels
4. Memory 8-16+ GB
5. TEE/Security
6. Stable, optimized rich OS (Linux, Android)

   \+ *application layer*

Server/Datacenter

1. 32-64-128 cores per chip
   - 8-16 cores per cluster, multiple clusters
   - on-chip and die-to-die clusters coherency
2. Standard extensions:
   - Vectors/SIMD
   - High-throughput accelerators (AI, ciphers, compression, etc)
3. Memory 1+ TB w/ ECC
4. Cache hierarchy 3-4 levels
5. Advanced virtualization features
6. Server-grade Linux, hypervisor
7. Stable, optimized applications: databases, web and network services/infrastructure, middleware

Application class RISC-V HW vendors

1. Sifive

P650, 64bit, up to 16 cores per cluster, multi-cluster, 2-3 GHz, A77+ perf
https://www.sifive.com/cores/performance-p650

2. Alibaba T-Head

XuanTie E9xx family, 64bits, 4-8x cores per cluster, 2-3 GHz
https://www.t-head.cn/product/overview

3. Ventana Micro

Veyron V1, 64bit, 16 cores per cluster, up to 192 cores 3.6 GHz
https://www.ventanamicro.com

4. MIPS

I8500/P8700, 64bit, up to 8 cores per cluster, up to 64 clusters, 2-3 GHz
https://www.mips.com/products/risc-v

5. Starfive

Dubhe, 64bit, 4 cores per cluster, 2GHz, 9+ Spectint2006/GHz
https://starfivetech.com/en/site/riscv-core-ip

6. BOSC

Xiangshan open source project
https://www.bosc.ac.cn/kyxm1

7. Imagination Technology

Catapult family, 32 and 64bit
https://www.imaginationtech.com/products/cpu/img-rtxm-2200

8. Syntacore

SCR7, SCR9 - up to 8-16 cores per cluster, multi-cluster, 2+ GHz
https://syntacore.com/page/products/processor-ip

9. Tenstorrent

Alastor, Ascalone 64bit, multicore, multicluster
https://www.tenstorrent.com

10. Semidynamics

Atrevido family, 64bit, multicore, multicluster, 2+ GHz
https://semidynamics.com/products/atrevido

… + more companies in stealth

TSC application class compute focus

- Application class is in the focus since 2021

- Specifications
  - Profiles and Platforms
    SEE, SBI, ABI, Discovery, Watchdog, ACPI, UEFI
  - Security
    RISC-V Security Model, AP-TEE, IOPMP
  - Infrastructure SoC
    E-Trace, Nexus, IOMMU

- New standard extensions development
  - 30+ new in 2021

Extensive ongoing prototyping/testing to test/confirm RISC-V standards by practice

Extension Name	Description	Depends On or Implies	Ratification Year	RVI20	RVA20	RVM20	RVA22	RVM22
				m - Mandatory				
					Mode	Mode	Mode	Mode
					u s M	u s M	u s M	u s M
RVI32	ISA Base		2019	m	m m m	m m m	m m m	m m m
RVE32	ISA Base		2019	m	i i i	m m m	i i i	m m m
RVI64	ISA Base		2019	m	m m m	m m m	m m m	m m m
C	Compressed		2019	s	m m m	s s s	m m m	s s s
D	Scalar DP FP	F	2019	s	m m s	s s s	m m s	s s s
F	Scalar SP FP	not Zfinx	2019	s	m m s	s s s	m m s	s s s
H	Hypervisor		2021	x	x x x	x x x	s s s	u u u
M	Multiply/Divide		2019	s	m m m	s s s	m m m	s s s
Q	Scalar QP FP		2019	u	u u u	u u u	u u u	u u u
Sm1p11	Priv 1.11		2019	s	n n m	n n m	n n i	n n i
Ss1p11	Priv 1.11		2019	s	n m m	n s s	n i i	n i i
Sm1p12	Priv 1.12		2021	x	x x x	x x x	n n m	n n m
Ss1p12	Priv 1.12		2021	x	x x x	x x x	n m m	n s s
Smepmp	Enhanced PMP		2021	x	x x x	x x x	n n s	n n s
Smstateen	State Enable		2021	x	x x x	x x x	n s s	n s s
Sv57	Sv57	Ss1p12	2021	x	x x x	x x x	n s s	n s s
Svinval	Fast TLB Invalidation	Ss1p12	2021	x	x x x	x x x	n s s	n s s
Svnapot	64K NAPOT Pages	Ss1p12	2021	x	x x x	x x x	n s s	n s s
Svpbmt	Page-Based Memory Types	Ss1p12	2021	x	x x x	x x x	n s s	n s s
Sscofpmf	Count Overflow & Mode Filtering		2021	x	x x x	x x x	n s s	n s s
Sstc	Time Compare		2021	x	x x x	x x x	n s s	n s s
Zaamo	Atomics		2019	s	m m m	s s s	m m m	s s s
Zalrsc	Atomics		2019	s	m m m	s s s	m m m	s s s
Zba	Bitmanip		2021	x	x x x	x x x	m m m	s s s
Zbb	Bitmanip		2021	x	x x x	x x x	m m m	s s s
Zbc	Bitmanip		2021	x	x x x	x x x	s s s	s s s
Zbs	Bitmanip		2021	x	x x x	x x x	m m m	s s s
Zbkb	Crypto Scalar (Bitmanip)		2021	x	x x x	x x x	s s s	s s s
Zbkc	Crypto Scalar (Bitmanip)		2021	x	x x x	x x x	s s s	s s s
Zbkx	Crypto Scalar (Bitmanip)		2021	x	x x x	x x x	s s s	s s s
Zdinx	DP FP in Int regs	Zfinx	2021	x	x x x	x x x	i i i	s s s
Zhinx	HP FP in Int regs	Zfinx	2021	x	x x x	x x x	i i i	s s s
Zhinxmin	HP FP Conversions in Int regs	Zfinx	2021	x	x x x	x x x	i i i	s s s
Zfh	HP FP	F	2021	x	x x x	x x x	s s s	s s s
Zfhmin	HP FP Conversions	F	2021	x	x x x	x x x	s s s	s s s
Zfinx	SP FP in Int regs	not F	2021	x	x x x	x x x	i i i	s s s
Zicbom	CMO		2021	x	x x x	x x x	m m m	s s s
Zicbop	CMO		2021	x	x x x	x x x	m m m	s s s
Zicboz	CMO		2021	x	x x x	x x x	m m m	s s s
Zicsr	CSR		2019	s	m m m	m m m	m m m	m m m
Zicntr	Base Counters		2019	s	m m m	s s s	m m m	s s s
Zihpm	Hardware Performance Monitors		2019	s	m m m	s s s	m m m	s s s
Zifencei	FENCE.I		2019	s	u m m	s s s	u m m	s s s
Zihintpause	PAUSE		2021	x	x x x	x x x	m m m	m m m
Zk	Crypto Scalar		2021	x	x x x	x x x	s s s	s s s
Zkn	Crypto Scalar		2021	x	x x x	x x x	s s s	s s s
Zknd	Crypto Scalar		2021	x	x x x	x x x	s s s	s s s
Zkne	Crypto Scalar		2021	x	x x x	x x x	s s s	s s s
Zknh	Crypto Scalar		2021	x	x x x	x x x	s s s	s s s
Zkr	Crypto Scalar		2021	x	x x x	x x x	s s s	s s s
Zks	Crypto Scalar		2021	x	x x x	x x x	s s s	s s s
Zksed	Crypto Scalar		2021	x	x x x	x x x	s s s	s s s
Zksh	Crypto Scalar		2021	x	x x x	x x x	s s s	s s s
Zkt	Crypto Scalar		2021	x	x x x	x x x	s s s	s s s
Zve32f	Vector	F	2021	x	x x x	x x x	s s s	s s s
Zve32x	Vector		2021	x	x x x	x x x	s s s	s s s
Zve64d	Vector	D	2021	x	x x x	x x x	s s s	s s s
Zve64f	Vector	F	2021	x	x x x	x x x	s s s	s s s
Zve64x	Vector		2021	x	x x x	x x x	s s s	s s s
V	Vector		2021	x	x x x	x x x	s s s	s s s

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HW: good enough

SW: needs work (ongoing)

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HW: getting there

SW: ok to start

Summary

- RISC-V enters application class domain in practice
  - domain-specific and general purpose
  - HW approaches maturity for client and datacenter applications
    - SW follows, industry grade is still in early days
    - In-house open-source SW stacks pave the way
  - Sizable investments by multiple companies in all segments
- Syntacore ships application-class IP, ready to work with early adopters

Thank you!

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