

Ventana Micro Presentation at RVI China Summit 2023

**The RISC-V Revolution:
How China Can Lead the Way**



Ventana: The Leading High-Performance RISC-V & Chiplet Company



Balaji Baktha

*Ventana Founder and CEO,
RISC-V Board of Directors*



Greg Favor

*Ventana Co-Founder, CTO, and
Chief Architect
RISC-V Chair-elect of Technical
Steering Committee*

**Founded in 2019 by team of industry veterans with
a Proven Track Record of delivering Data Center
Class Processors**

- Team that brought the 1st 64-bit Arm Server Processor to Market
- Delivered several successful x86 processors with AMD starting with K6
- World's 1st High Performance Data Center Class RISC-V CPU
- 1st to Implement High Performance RISC-V CPU Chiplets

Q3'21: Launched
out of stealth

Q1'22: Announced
Partnership with IFS

Q2'23: Founding member
of **RISE** along with
Google, QCOM & Intel

Q4'21: Joined RISC-V
Board of Directors

Q4'22: Launched **Veyron**
V1: The World's First DC
Class RISC-V Processor

Ventana's Contributions to RISC-V International

| | |
|---|------------------|
| Member of Board of Directors | Balaji Baktha |
| Chair-elect of Technical Steering Committee | Greg Favor |
| Chair of Privileged Architecture Standing Committee | Greg Favor |
| Chair of Platforms Horizontal Sub-Committee | Kumar Sankaran |
| Chair of CacheOps Task Group | David Kruckemyer |
| Chair of Marketing Events Committee | Omar Hassen |
| Vice-Chair of Debug Task Group | Paul Donahue |
| Co-author of Advanced Interrupt Architecture | Greg Favor |
| Chair of Hypervisor SIG | Anup Patel |



Greg Favor

'21 RVI BoD Technical Leadership Award
'20 RVI BoD Technical Contributor Award



Anup Patel

'22 RVI BoD Technical Leadership Award



Sunil V L

'22 RVI Software Contributor Award
'22 RVI Ratification Award (UEFI)

Ventana Helped Drive RISC-V Specifications to Server Readiness

Ventana: Exceptional Industry Recognition

Media



DIGITIMES

EE Times
ASIA

The Register®

THE CHANNEL CO.
CRN
CELEBRATING 40 YEARS



Tech Insights

THE NEXT PLATFORM

Silicon



EEJ Forbes



Most Influential Founding Team

THE CHANNEL CO.
CRN
CELEBRATING 40 YEARS

10 Hot Semiconductor Companies To Watch In 2023

BY DYLAN MARTIN ▶

JANUARY 28, 2023, 10:00 AM EST

CRN breaks down 10 semiconductor companies that are driving the market with new innovations — or are on the verge of doing so — while navigating the tough economic environment.

Ventana placed among AMD, Nvidia, Intel, Qualcomm, and Arm as a Top 10 Semis To Watch for 2nd year in row



RISC-V Summit China



EU Parliament Delegation

RISC-V Day
Tokyo 2023 Summer



MEITY Panel Promoting RISC-V as National ISA



Bavarian Ministry of Economic Development

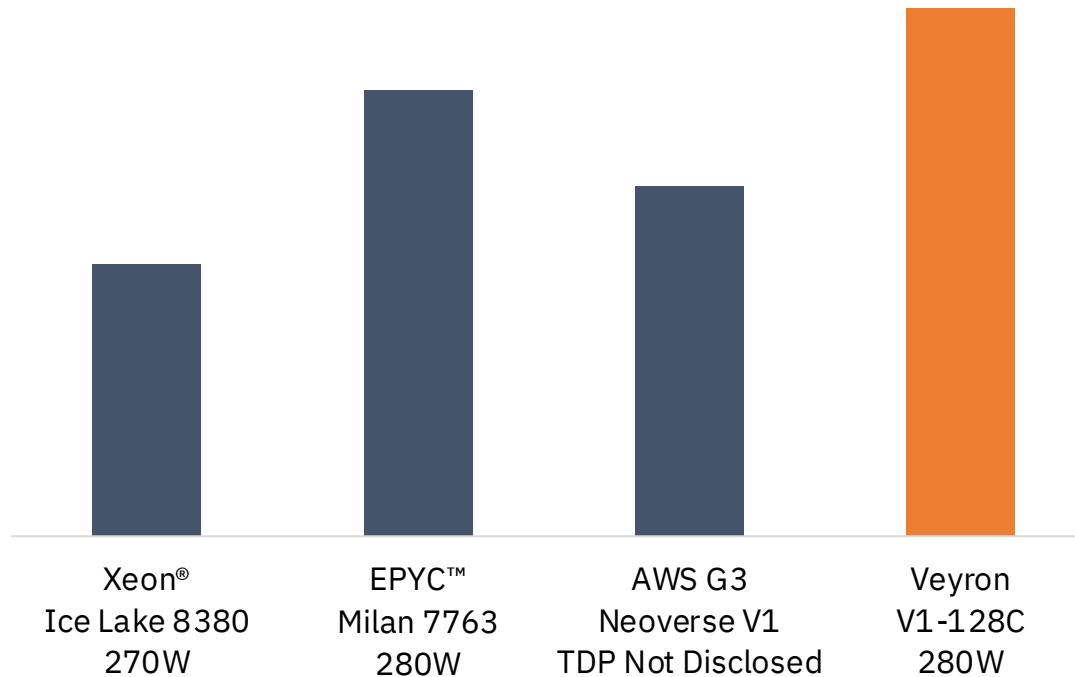
GSA
Where Leaders Meet

Invited Speaker on RISC-V and Chiplets at Global Semiconductor Alliance

Veyron V1: World's First Data Center Class RISC-V Processor

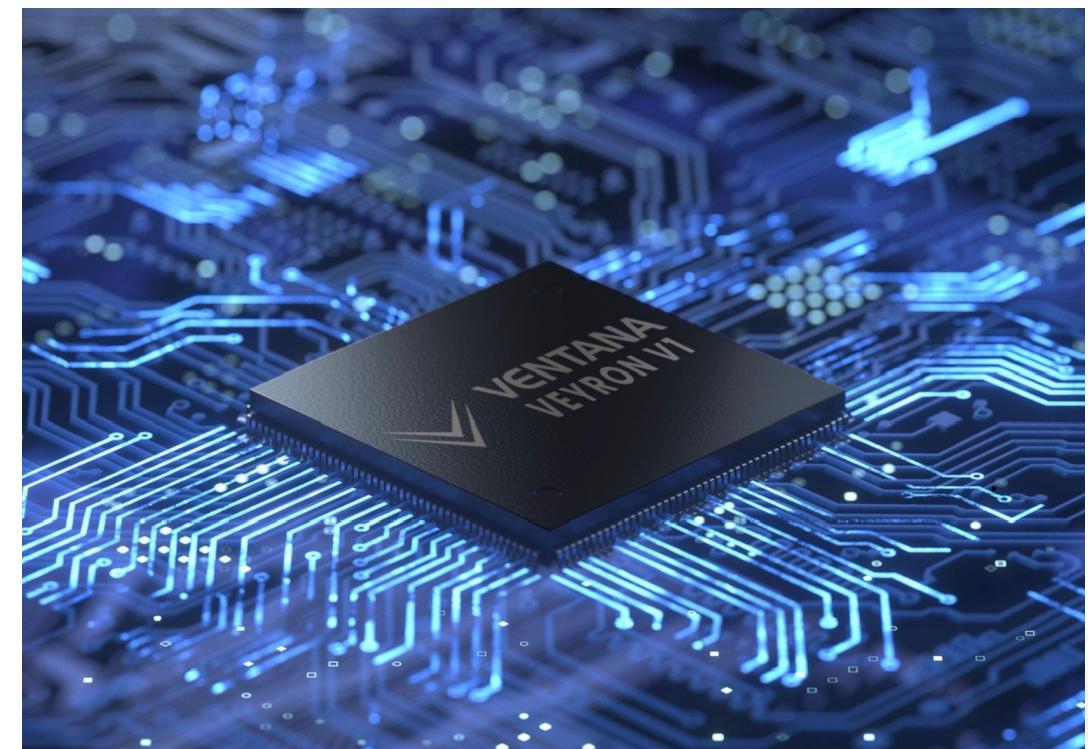
Highest Performance RISC-V CPU

3.6 GHz in 5nm process technology



ASSP Based on High Performance Chiplet Architecture

Significant reduction in development Time and Cost compared to prevailing monolithic SoC model



Disruptive ROI: Highest Single Socket Performance at Compelling Perf/Watt/\$

Ventana's Innovations for Next Gen RISC-V Platforms

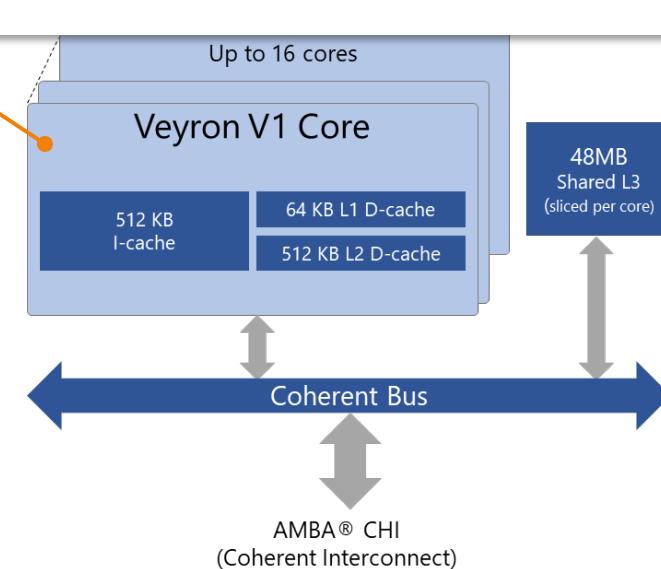
- RV64GC plus many additional User, Supervisor, and Machine level architecture extensions
- Hypervisor extension
 - Type 1 and 2 Hypervisors; nested virtualization
- Advanced Interrupt Architecture (AIA)
 - Including native MSU handling and interrupt virtualization
- 48-bit virtual addressing and 52-bit physical addressing
- External and self-host debug; trace-to-memory
- Rich set up performance events and perf counters

**Robust
Architecture
Specification**



Gen RISC-V Platforms

- Superscalar, aggressive out-of-order design
- Decoupled predict/fetch front-end with advanced branch prediction
 - Predict fetch stream ahead of just-in-time fetch to keep decode pipe fed
 - Advanced branch prediction of direction and target address
 - High capacity BTB and predictors
- Decode, dispatch, and execute up to eight instructions per cycle
 - Fusion of common instruction-pair code idioms
 - All operate in terms of “ops” (fused and unfused)
- Symmetric execution of any mix of Reg/Ld/St/Br ops per cycle



**High
Performance
CPU Core**



Robust
Architecture
Specification



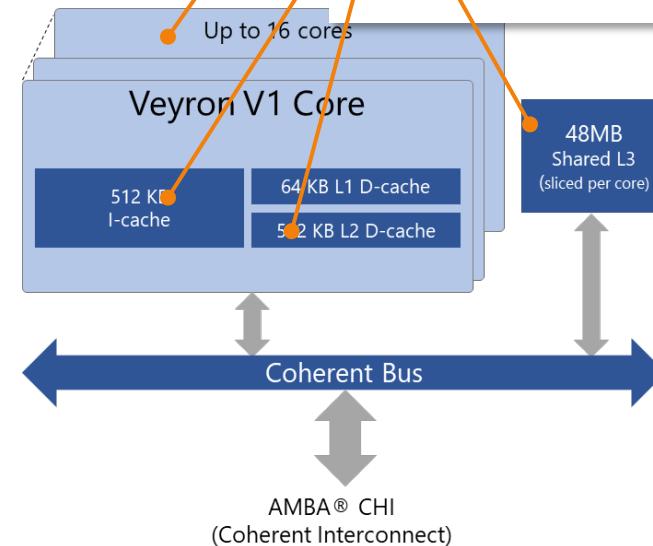
Ventana's Innovations for Next Gen RISC-V Platforms

- High core count multi-cluster scalability
 - Up to 192 cores per system
 - Up to 16 cores per cluster
- High performance cache hierarchy
 - Implemented 1M L2 per core
 - Up to 48MB of globally shared cluster-level L3 cache

High
Performance
Memory System



High
Performance
CPU Core



Robust
Architecture
Specification



Ventana's Innovations for Next Gen RISC-V Platforms

Security & RAS



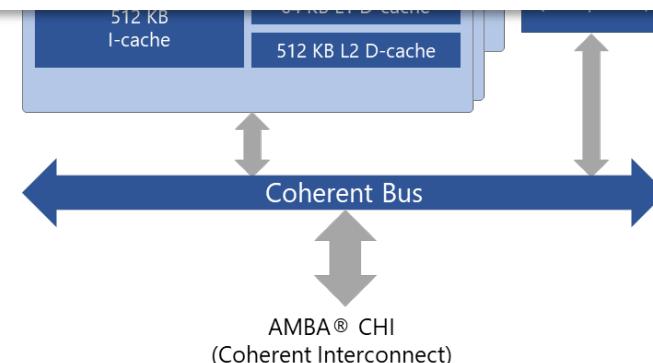
High Performance Memory System



High Performance CPU Core



- Robust resistance to side channel attack
- All necessary RAMS protected
 - All RAMs which can have dirty data protected with ECC
 - All read-only RAMs protected with parity + HW auto recovery
- Data poisoning
 - Corrupted data cache lines marked as poisoned
 - Allows killing of user application while kernel continues
- Data scrubbers
 - L2 and L2 have HW mechanism for scanning corrupted cache lines
 - Rate configurable



Robust Architecture Specification



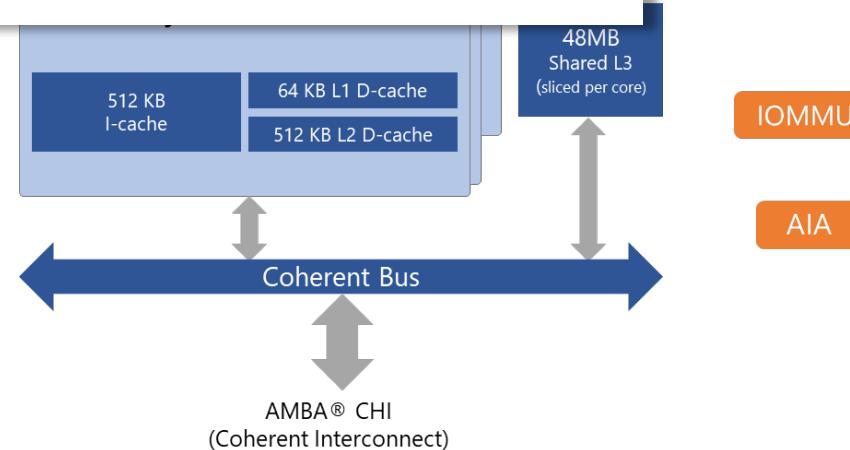
Gen RISC-V Platforms

- IOMMU
 - Equivalent of Arm SMMU
 - Enterprise-class
 - Connects direct-memory-access capable I/O devices to system memory
 - Shared virtual addressing enables sharing or process address spaces with devices
- Interrupt Controller
 - Message-Signaled Interrupts requires less complex wiring than Arm GIC
 - Traditional wired interrupts from dedicated wires are sent the Advanced Platform-Level Interrupt Controller (APLIC) where it is prioritized/routed

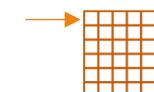
High Performance Memory System



High Performance CPU Core



Robust Architecture Specification



System IP

Ventana's Innovations for Next Gen RISC-V Platforms

Security & RAS

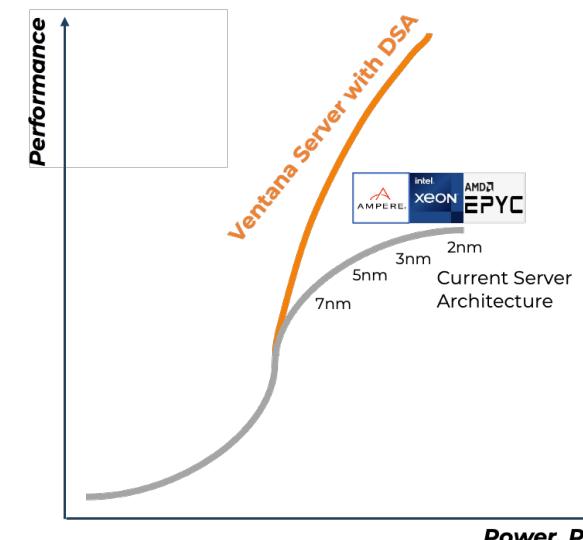


- Scalable, Flexible platform
- Customized Domain Specific Acceleration
- Optimized Performance/W/\$

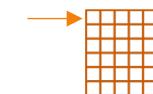
High Performance Memory System



High Performance CPU Core



Domain Specific Acceleration



System IP

Robust Architecture Specification



Ventana's Innovations for Next Gen RISC-V Platforms

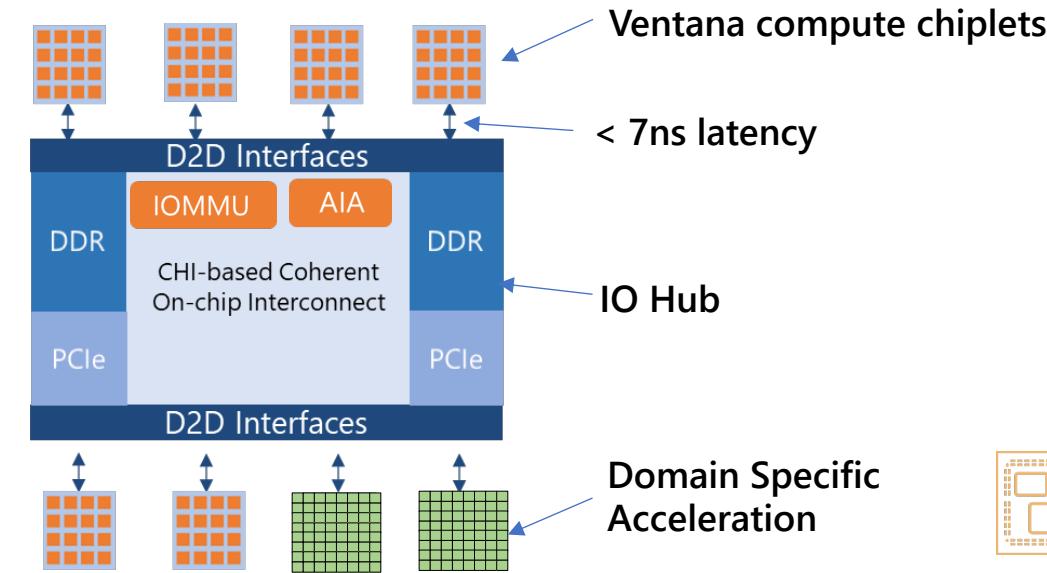
Security & RAS



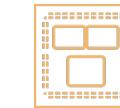
High Performance Memory System



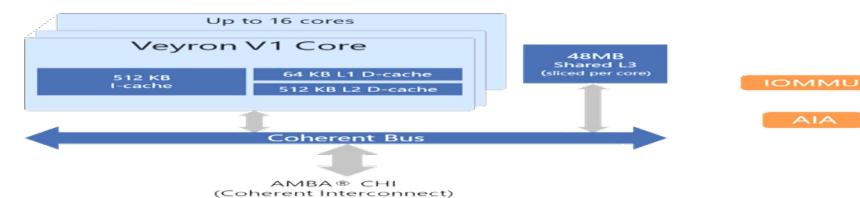
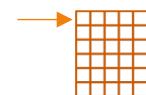
High Performance CPU Core



Chiplet Technology



System IP



Robust Architecture Specification



Ventana's Innovations for Next Gen RISC-V Platforms

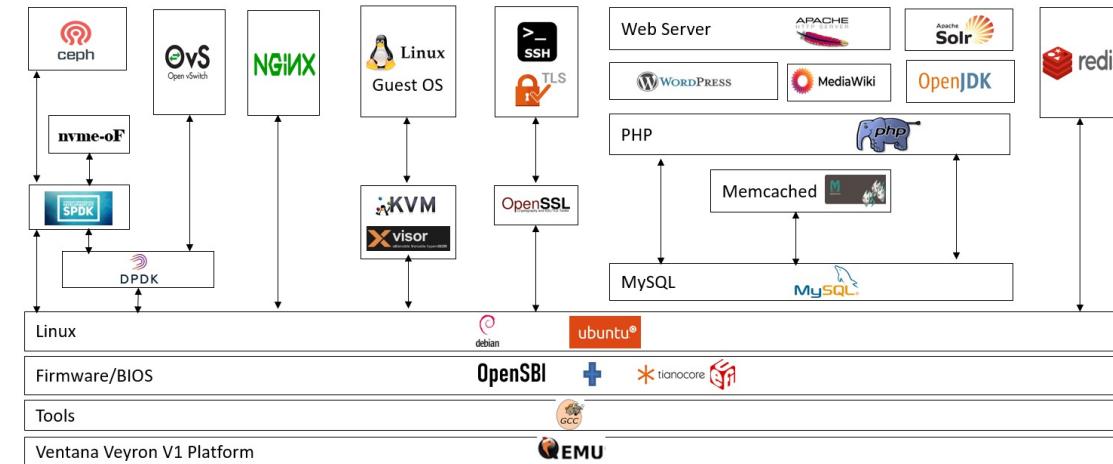
Security & RAS



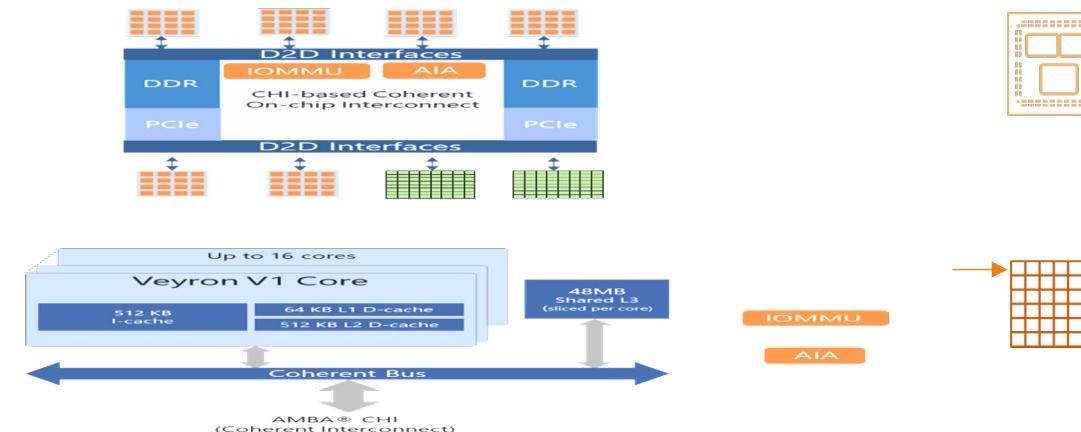
High Performance Memory System



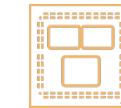
High Performance CPU Core



Software Stack



Chiplet Technology

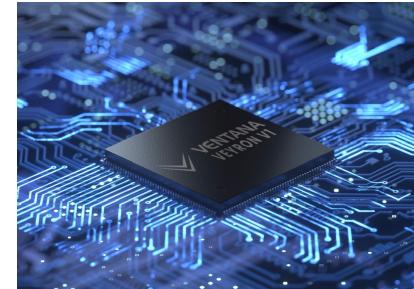


Robust Architecture Specification



Ventana's Innovations for Next Gen RISC-V Platforms

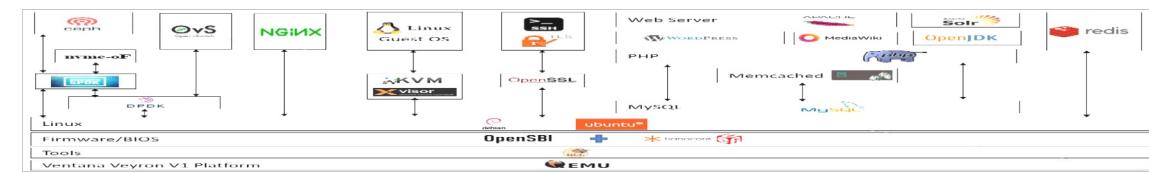
Security & RAS



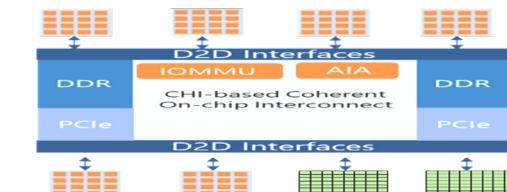
High Performance Memory System



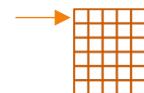
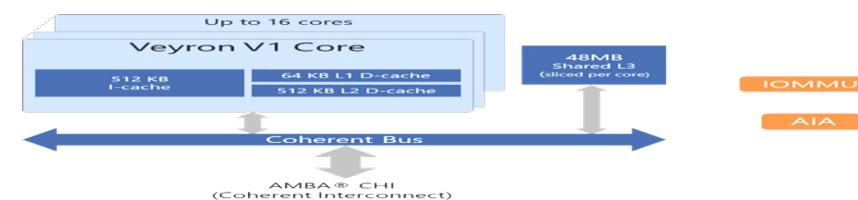
High Performance CPU Core



Software Stack



Chiplet Technology



System IP

Robust Architecture Specification

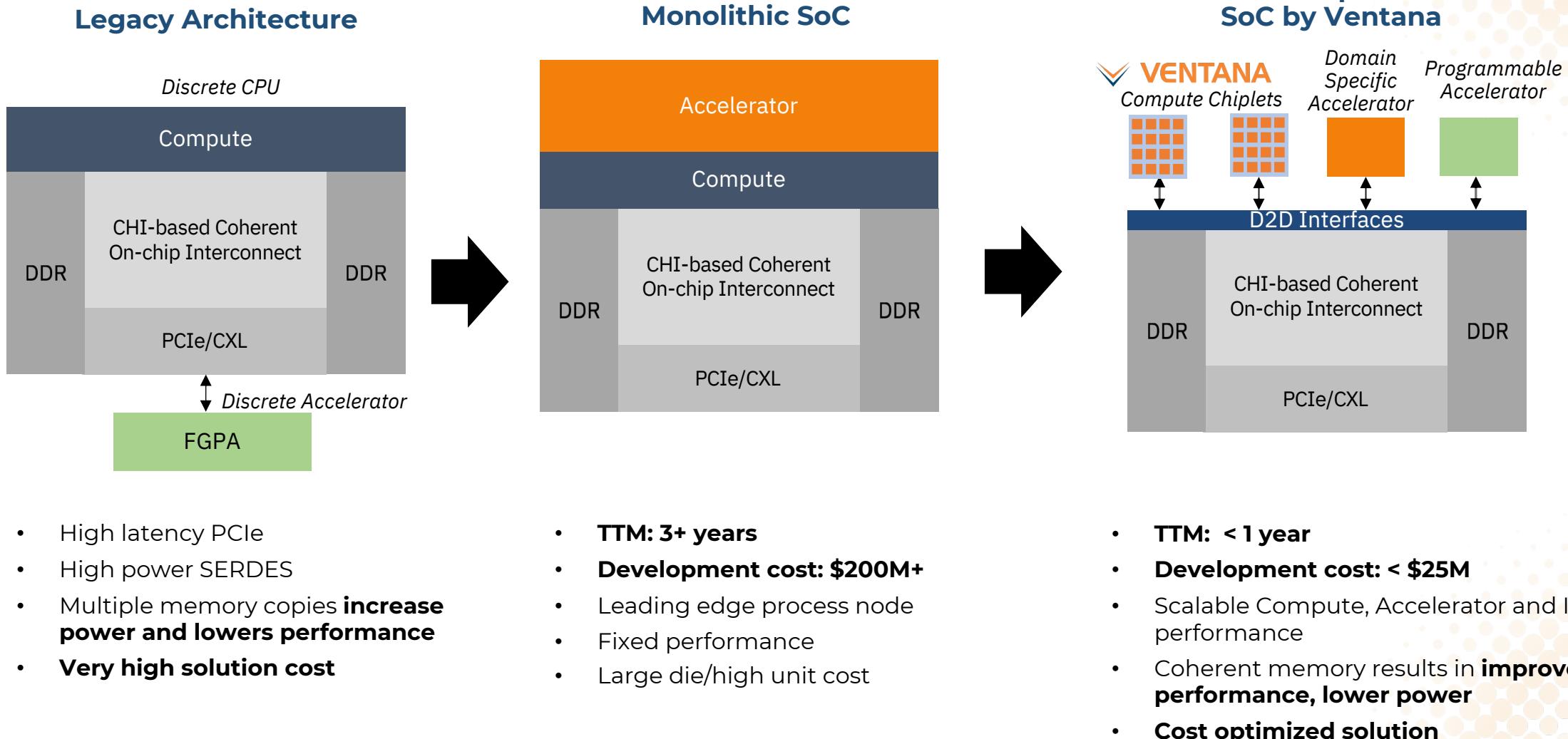


The Global Semiconductor Innovator's Dilemma...

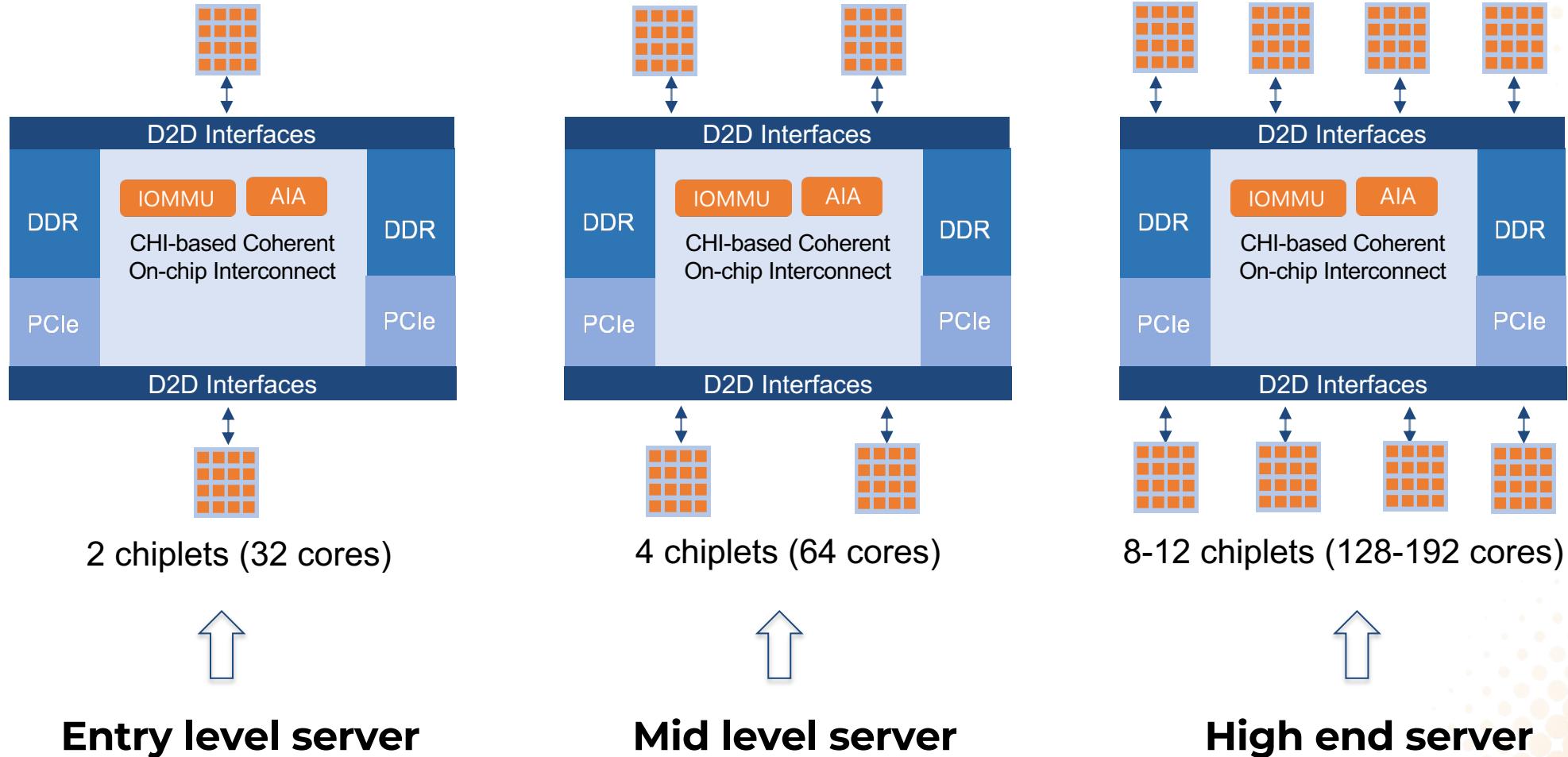


- ▶ Semiconductors Are The Foundation Of The Modern Economy and Digital Autonomy
- ▶ Unrelenting Massive Semiconductor Consolidation Since 2008
- ▶ Led To Monopolies In All Key Semiconductor Segments
- ▶ No Room For Innovation And Differentiation
- ▶ Very High Development Cost: ~\$200M Per Project
- ▶ How Do You Break The Cycle?

The Solution by Ventana



Ventana Scalable Architecture for Server-class Compute



Huge Target Markets

China Can Lead the Way



***Build World-Class, High-Performance SoCs
Based on RISC-V and Chiplet Architecture***

Target Cloud Compute Infrastructure,
Automotive, Edge, and Client

Ventana: An Ally in China's RISC-V Productization

- ▶ **Most Recognized as the RISC-V Performance Leader and as the Chiplet Leader**
- ▶ **One of the Best CPU Teams in the world**
- ▶ **One of the most influential contributors to RISC-V International at the Board of Directors, Technical, and Marketing Committees**
- ▶ **Led the way in Defining and Creating a Robust Server Class Platform and Software Ecosystem**
- ▶ **World-Class RISC-V CPU Product and Roadmap**
- ▶ **Pioneered chiplet-based Productization and Business Model: Customized, Rapid, Cost-Optimized Processors**

Thank You!



Ventana's Contributions to RISC-V Architecture

Greg Favor, CTO for Ventana Systems, has made huge contributions to RISC-V while serving as the vice chair of our Technical Steering Committee, and the chair of our Privileged ISA Committee. Greg is a recipient of multiple RISC-V Leadership and Technical awards. RISC-V and I are grateful for his presence among our technical leaders.. - *Mark Himmelstein, CTO RISC-V International*



Balaji Baktha

Member, Board of Directors



Greg Favor

Chair, Technical Steering Committee
Chair, Privileged Architecture Committee
Co-author, Advanced Interrupt Architecture
'21 RVI BoD Technical Leadership Award
'20 RVI BoD Technical Contributor Award



Kumar Sankaran

Vice-Chair, RISE Technical Steering Committee



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Chair, Hypervisor SIG
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Vice-Chair, Platform and Runtime Services TG



Omar Hassen

Chair, Marketing Events Committee



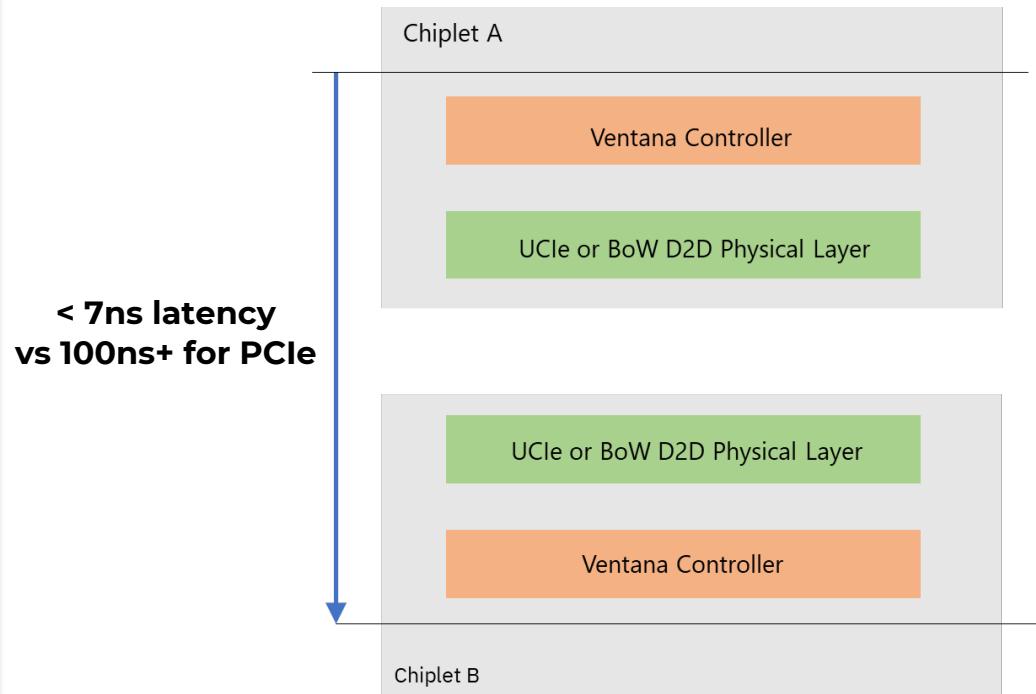
Paul Donahue

Vice-Chair, Debug Task Group
Vice-Chair, Debug, Trace, and Performance Monitoring SIG

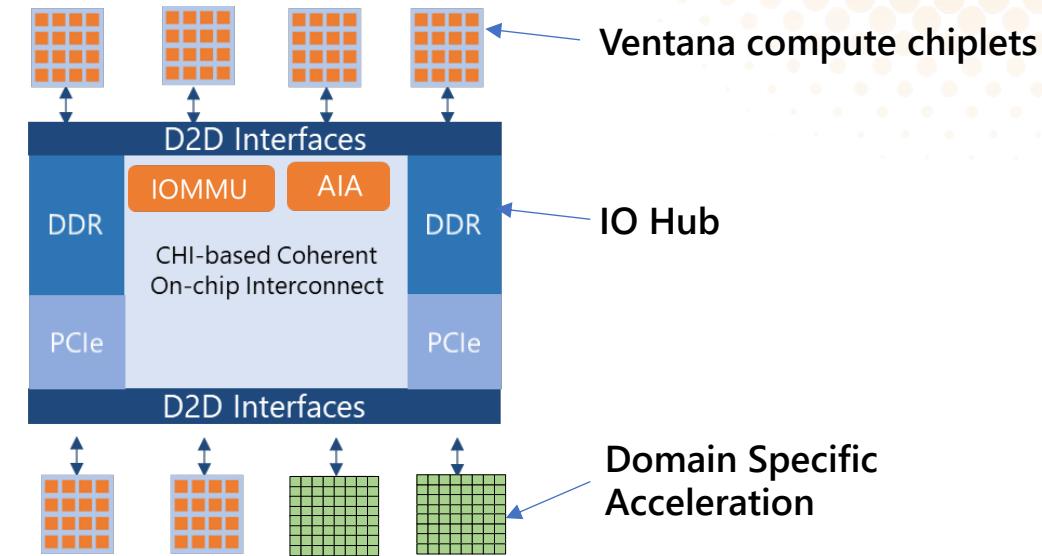
Veyron: Putting It Together With Chiplets

Solving the D2D Latency Problem

- Ventana has developed low-latency controller IP which maps standard, coherent SoC buses such as CHI & AXI to D2D PHY



Veyron Chiplet Solution



- Veyron compute chiplets
 - In latest process node technology
 - Scalable CPU performance/count
- IO Hub
 - Implemented in process node of choice
 - Customized for application requirements
- Custom Domain Specific Acceleration
 - Low-cost process node

Ventana Veyron Software Stack



**Please attend Kumar Sankaran's keynote for an in-depth review of Ventana's software solution:
“Full Stack Acceleration for the Datacenter with RISC-V”**

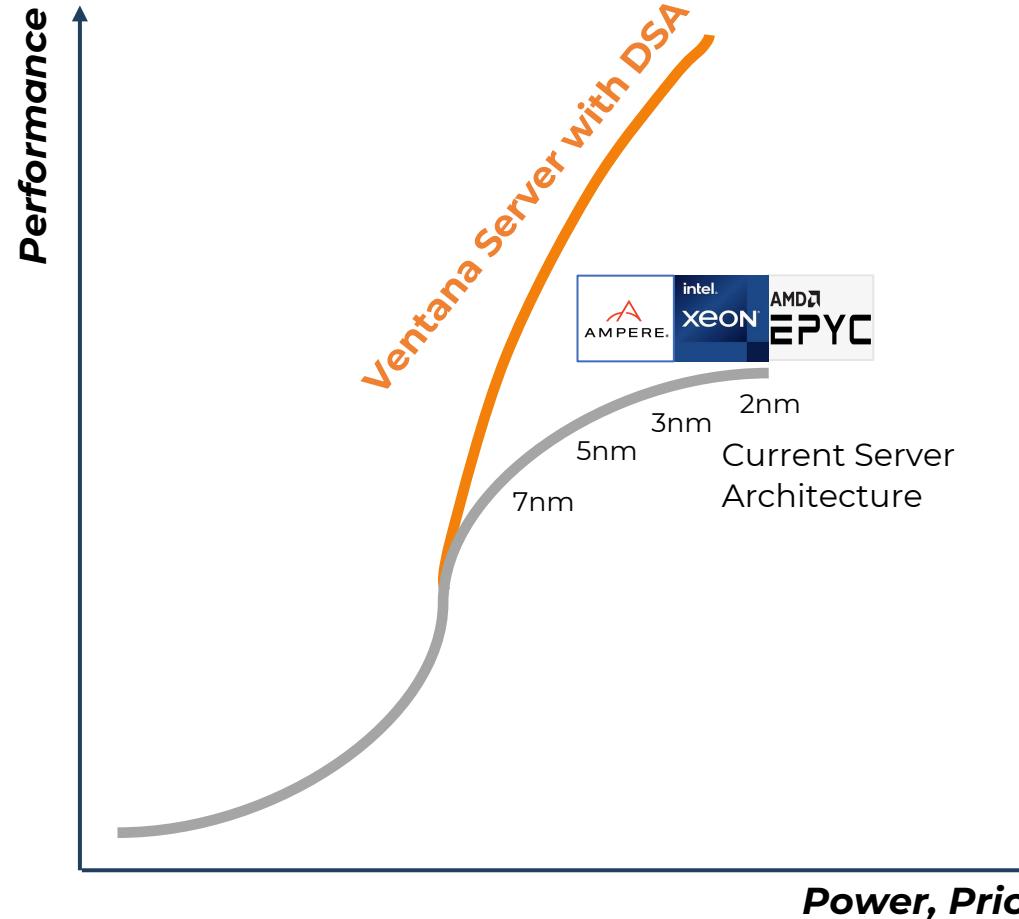
China is at the Forefront of the RISC-V Revolution

Significant Contributions to RISC-V by China:
1st Android Port, OpenJDK, RISC-V Processor Cores

***World-Class, High-Performance SoCs Powered by
RISC-V and Chiplets Can Be Built in China Today***



Ventana DSA Accelerators Drive Workload Efficiency



- **X86/ARM Server Architecture**

- Fixed Configuration
- No Hardware acceleration
- High Performance/W/\$

- **Ventana Server with DSA**

- Scalable, Flexible platform
- Customized Domain Specific Acceleration
- Optimized Performance/W/\$

50% Fewer Servers to Achieve the Same Workload
Performance at Scale

RISC-V Driving Unprecedented Opportunities

Powered by

Ventana Processors and Chiplets



Ventana Micro Introduction



**World's First High
Performance
RISC-V Server
*Powered by Ventana***

