

BRIDGING THE DIVIDE

Unifying RISC-V through Binary Translation



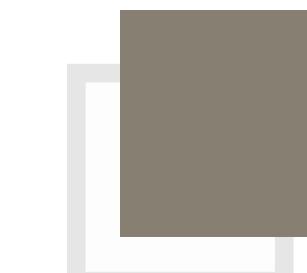
Dr. Philipp Tomsich
Chief Technologist & Founder, VRULL GmbH

RISC-V BUILDS MOMENTUM



RAPIDLY EVOLVING CAPABILITIES

The Technical Groups at RISC-V are continuously evolving the capabilities of the instruction set through new standards development.



SCALES TO EVERY APPLICATION

RISC-V offers the freedom for every implementer to add to, remove from, or customise the ISA as needed for their specific application or use-case.



INNOVATION ON A GLOBAL SCALE

The RISC-V ecosystem shares a common software foundation, and support the continuous innovation through custom, vendor-defined extension.

RISC-V evolves rapidly driven by market and application requirements.

CONTINUOUS EVOLUTION

2021

RISC-V Vector extension

State-of-the-art scalable vector extension supporting applications including ADAS, AI/ML and video processing

RISC-V bitmanipulation extensions

Instructions that improve code-density and optimise a wide variety of workloads in general purpose computing and signal processing

RISC-V scalar cryptography extension

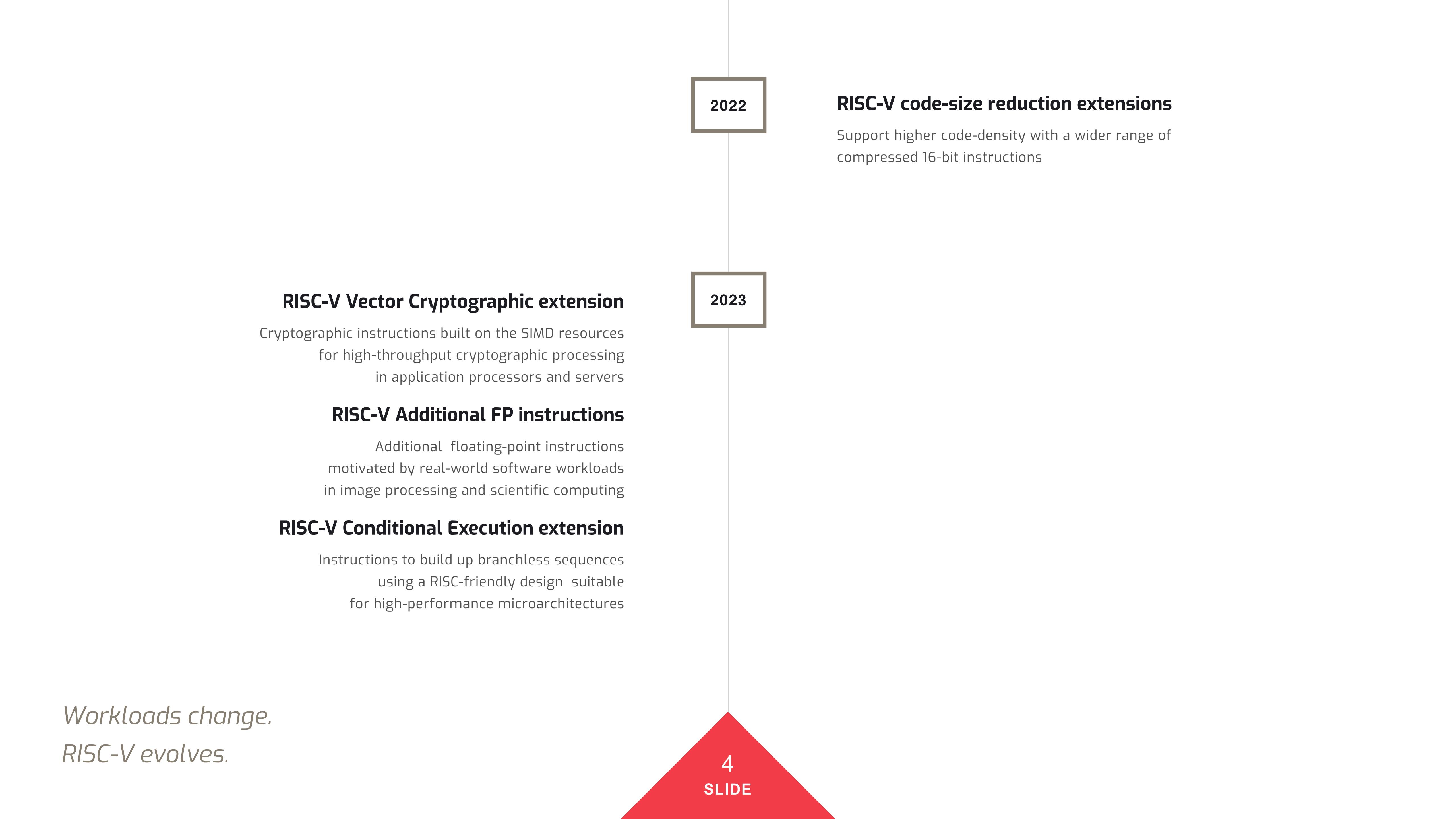
Cryptographic instructions targeting embedded workloads and microcontrollers

RISC-V Hypervisor extension

Architectural prerequisites for virtualisation

Workloads change.

RISC-V evolves.



2022

RISC-V code-size reduction extensions

Support higher code-density with a wider range of compressed 16-bit instructions

2023

RISC-V Vector Cryptographic extension

Cryptographic instructions built on the SIMD resources for high-throughput cryptographic processing in application processors and servers

RISC-V Additional FP instructions

Additional floating-point instructions motivated by real-world software workloads in image processing and scientific computing

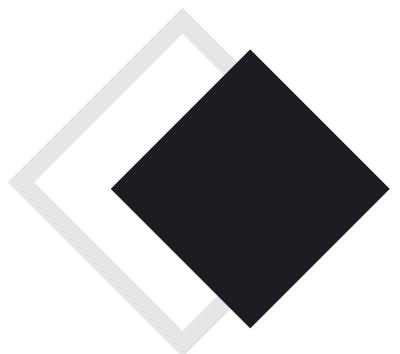
RISC-V Conditional Execution extension

Instructions to build up branchless sequences using a RISC-friendly design suitable for high-performance microarchitectures

*Workloads change.
RISC-V evolves.*

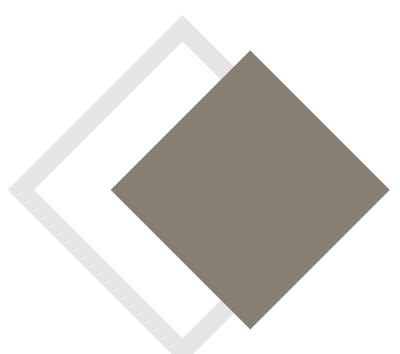
Addressing the adoption challenge

ENGINEERING UBIQUITY FOR RISC-V



SOFTWARE MIGRATION

Run binaries from legacy architectures on RISC-V unmodified and avoid porting overheads.



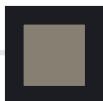
ARCHITECTURAL EVOLUTION

Embrace differentiation and avoid fragmentation through transparent retranslation.





SMART CAMERAS



DATACENTER



INDUSTRIAL



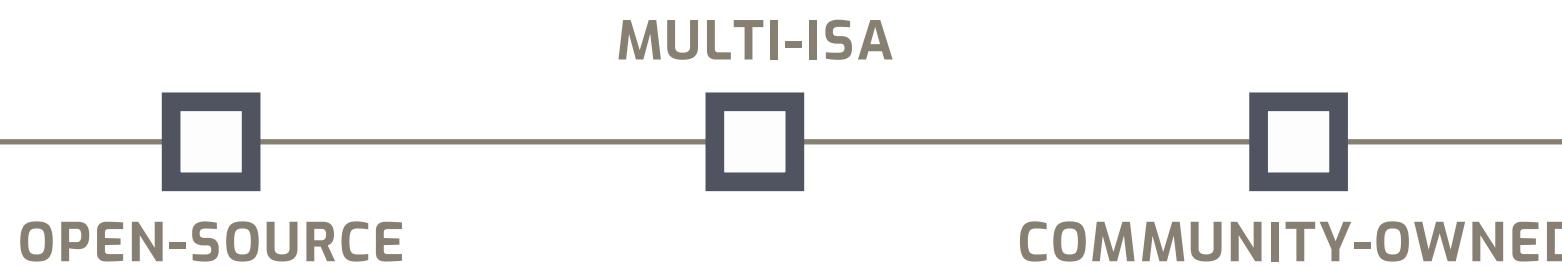
CLIENT COMPUTING



Announcing the

Open Binary Translation Alliance

www.binary-translation-alliance.org



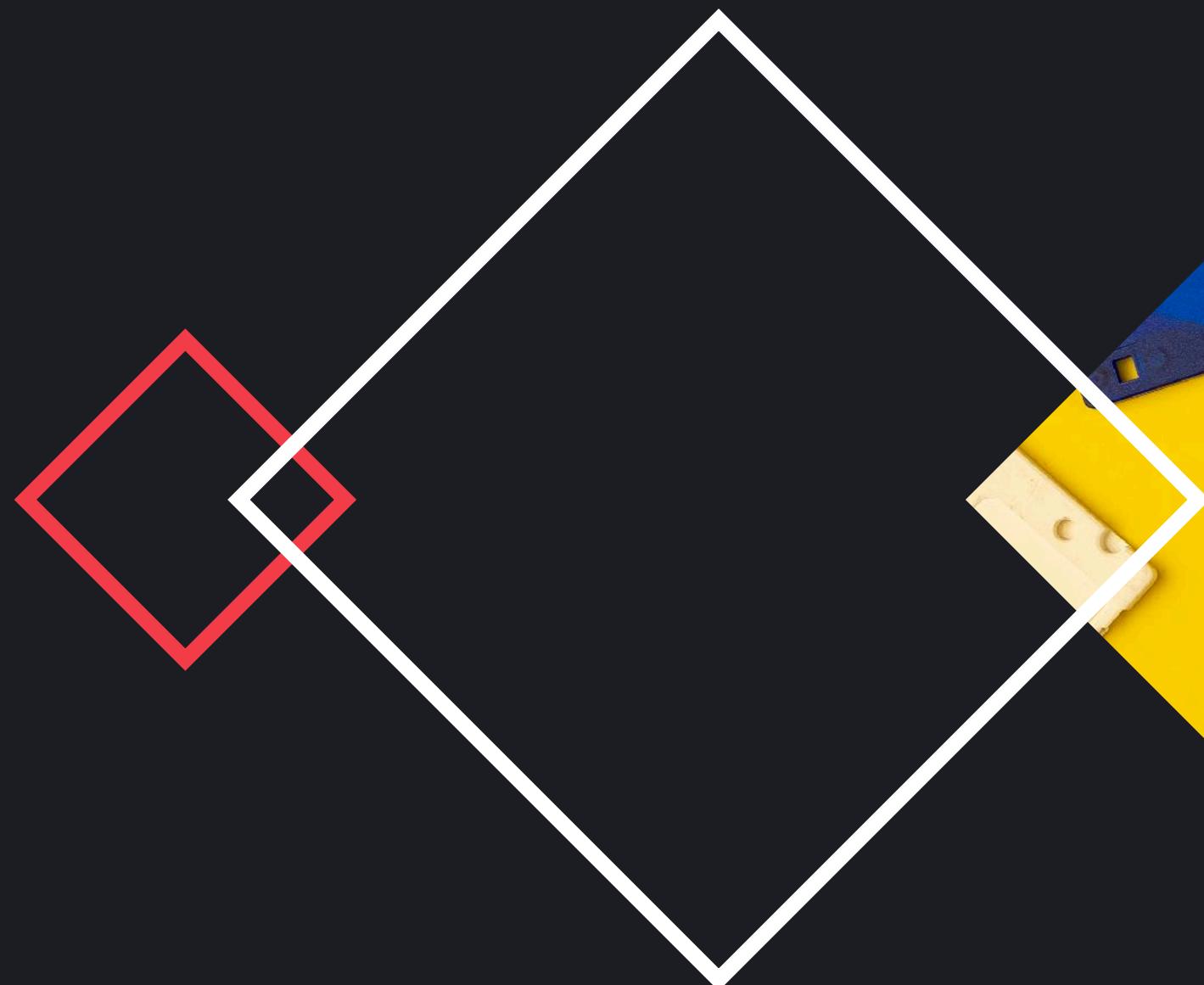
"An open and multi-ISA Binary Translation framework will be an unprecedented gamechanger for the rapidly evolving RISC-V landscape: it accelerates adoption, solves the question of legacy software, and empowers rapid innovation of the ISA without sacrificing compatibility."

OPEN COLLABORATION POOLED RESOURCES

LEARN FROM THE MISTAKES OF THE PAST

Binary translation has a prosperous and long future in RISC-V: we need to **pool resources** and build a single, maintained and well-optimised solution.

Vendor lock-in and “temporary solutions” would be a disadvantage for the entire RISC-V ecosystem while **competing against legacy architectures**.



ADVANCING BINARY TRANSLATION



EDUCATE



We engage with the research community.
Our academic outreach helps to educate the next generation of researchers and engineers.



DEVELOP



Develop and maintain the key components for integrating production-ready binary-translation into a wide range of products



EMPOWER



Encourage the development of a downstream ecosystem of service providers, consultants and integrators that assist in the commercial adoption



AMPLIFY YOUR IMPACT

Be a driving force in the community shaping decisions in line with your product strategy.



EARLY ACCESS TO INNOVATION

Gain a head start by being a part of the community's open-source development.



FLEXIBILITY & TRANSPARENCY

Embrace open-source freedom.
Avoid vendor lock-in.



SHARED RISK

Maximize efficiency & share risk through collaboration.



BUILDING TRUST AND RELIABILITY

Be at the forefront of building a trusted and reliable standard solution



ACCELERATE COMMERCIALIZATION

Establish Binary Translation as an Open-Source Technology and speed up RISC-V adoption.

Ensure readiness before the first Android devices ship.

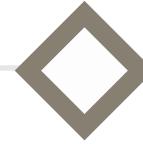
PROPOSED DEVELOPMENT TIMELINE

Open Binary Translation Alliance
launched and proof-of-concept
implementation available.

LATE 2023



TODAY



Membership drive to secure all
funding agreements necessary
for the development.

First developer preview

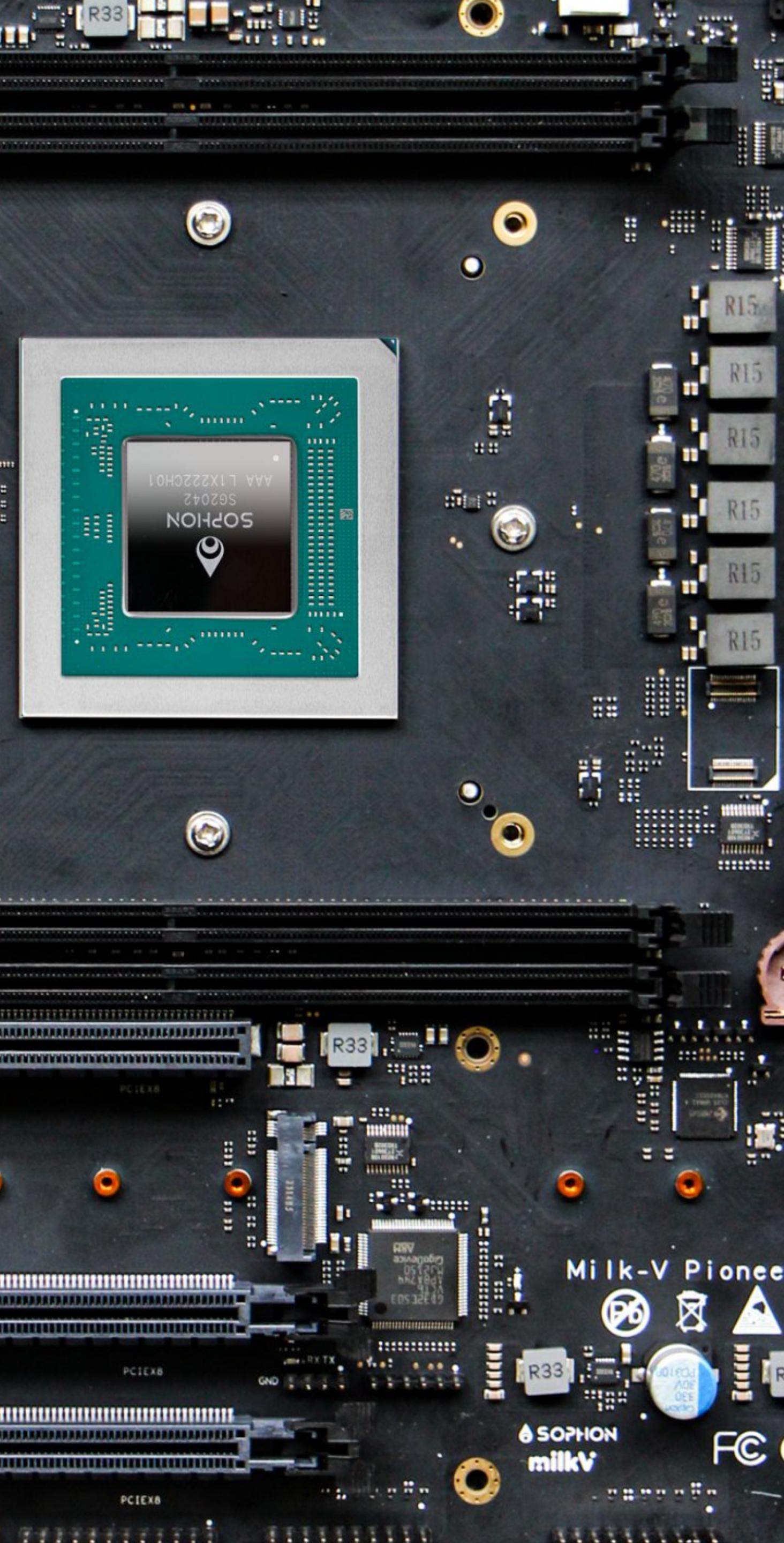
MID 2025



LATE 2024



First customer ship



```
[ptomsich@fedora-riscv ~]$ uname -a
Linux fedora-riscv 6.1.22 #2 SMP Thu May 4 19:24:40 CST 2023 riscv64 GNU/Linux

[ptomsich@fedora-riscv ~]$ file ~/coremark.exe
/home/ptomsich/coremark.exe: ELF 64-bit LSB executable, ARM aarch64, version 1 (GNU/Linux), statically linked, BuildID[sha1]=23bd08adbe542b95ce0c227ccb315660cccd9e83b, for GNU/Linux 3.7.0, not stripped, too many notes (256)

[ptomsich@fedora-riscv ~]$ ~/coremark.exe
-bash: /home/ptomsich/coremark.exe: cannot execute binary file: Exec format error

[ptomsich@fedora-riscv dbt-xlate]$ ./build/xlate ~/coremark.exe 0x0 0x0 0x66 100000
2K performance run parameters for coremark.
CoreMark Size      : 666
Total ticks        : 17744
Total time (secs) : 17.744000
Iterations/Sec     : 5635.707845
Iterations         : 100000
Compiler version   : GCC12.2.1 20221121 (Red Hat 12.2.1-4)
Compiler flags     : -O2 -O3 -static -DPERFORMANCE RUN=1 -lrt
Memory location    : Please put data memory location here
                     (e.g. code in flash, data on heap etc)
seedcrc            : 0xe9f5
[0]crclist          : 0xe714
[0]crcmatrix        : 0x1fd7
[0]crcstate          : 0x8e3a
[0]crcfinal          : 0xd340
Correct operation validated. See README.md for run and reporting rules.
CoreMark 1.0 : 5635.707845 / GCC12.2.1 20221121 (Red Hat 12.2.1-4) -O2 -O3 -static
-DPERFORMANCE_RUN=1 -lrt / Heap
```

ARM Neoverse-N1 binary executing on a Sophia Milk-V



Join the Alliance!

BRING THE SPIRIT OF
OPEN COLLABORATION
TO BINARY TRANSLATION

www.binary-translation-alliance.org