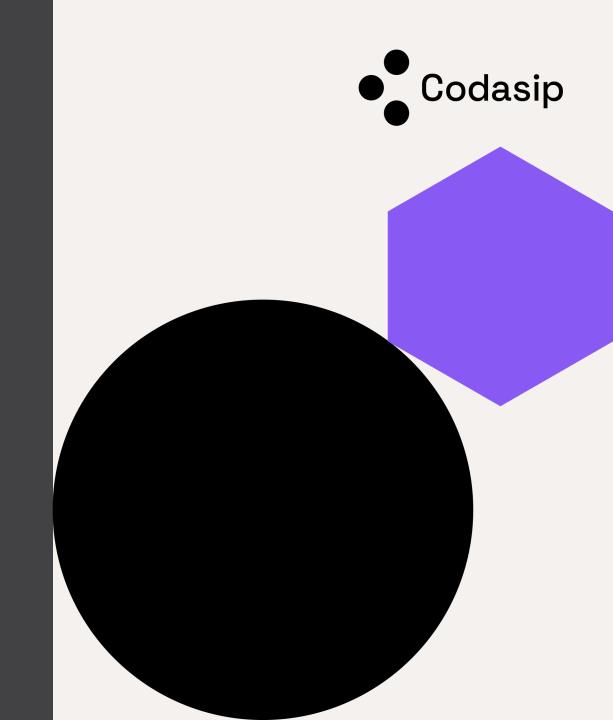


# RISC-V with HW/SW co-design and Custom Compute

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#### → Challenge in the market





No more "free improvements" with end of Moore's law



Need to optimize processing to the application

→ Custom Compute



Difficult and risky to do by hand

- Usually takes too long
- Usually is not optimal
- Requires large teams

#### → Benefits of Custom Compute



#### Improve performance

- Use older nodes
- Push boundaries

#### Improve efficiency

- Reduce power
- Reduce area
  - For example, remove companion DSP, compress code

#### Differentiate

- Beat the competition
- Protect against copy
  - Your custom processor is unique

#### → Leaders use Custom Compute



#### If you do it by hand

- Very long and difficult
  - Understand the application needs
  - Design a processor
  - Verify the processor
- Expensive
  - Need to iterate
  - Custom ISA
  - Custom SDK (compiler, debugger, ...)
  - Custom model
- Need large dedicated teams

#### At Codasip we make it with:

- → Automation
- → Ready-to-modify IP

#### → Custom compute enabled by two components



#### Design automation tools

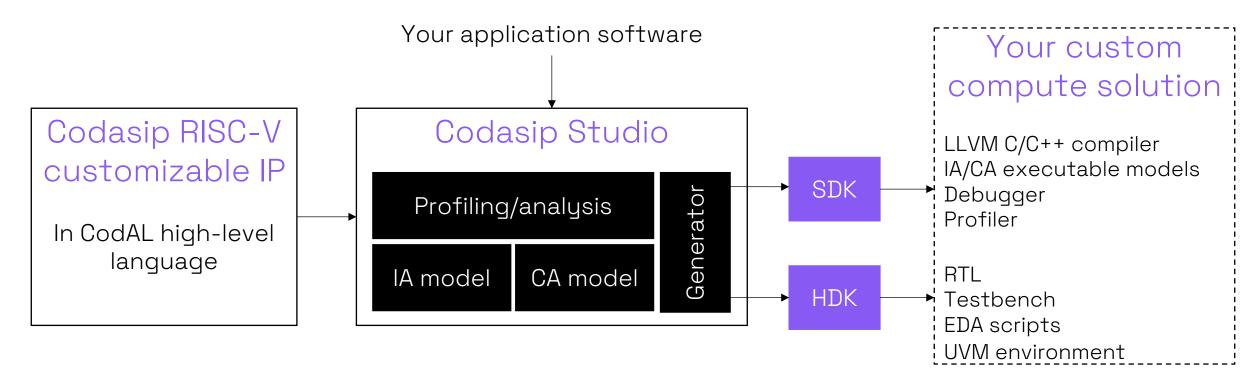
- Design automation tool
- Fast architectural iteration loop
  - Profiling & optimization
  - Co-simulation
  - Results analysis
- Using CodAL high-level language
- Generating custom RTL and SDK

#### RISC-V Processor IPs

- Production-ready processors
- Written in CodAL
- Designed for customization
- Fully RISC-V compliant
- Best-in-class verification
- Also available as ready-to-use RTL

#### → IP & tools combination



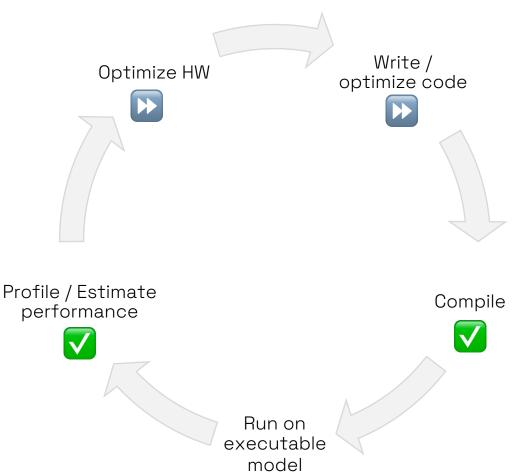


- Start with a standard core
  - Embedded and application cores
  - High quality, production-ready
  - Fully RISC-V compliant

- Differentiate with Codasip Studio
  - Configure / Modify
  - Using CodAL architecture description language



#### → Hardware and software co-optimization accelerated through automation



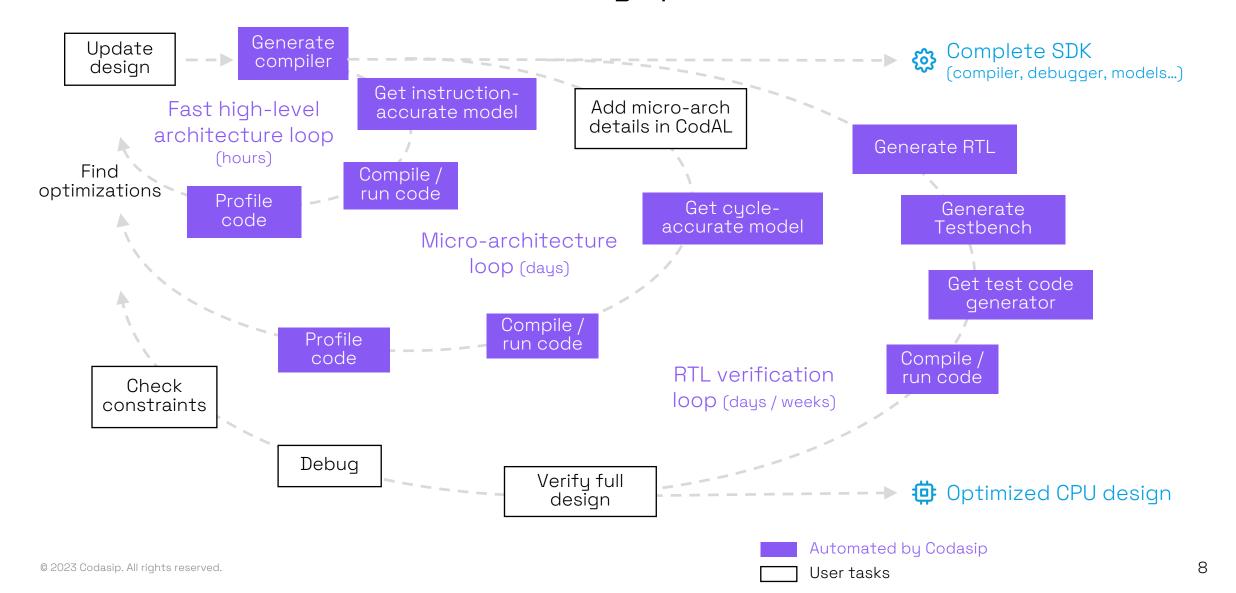
- Iterate to find optimal hardware
- Very long loop by hand
- Codasip provides automation
  - Very fast HW description
  - No need to change code
  - Automatic compiler generation
  - Automatic model generation
  - SW Profiling

Accelerate process with Codasip automation
Operation done with Codasip tools

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### → Get optimal results, fast. With an automated, iterative design process







- Silicon process technology progress (Moore's Law) has slowed down
- Differentiation is vital

Custom compute brings

10x ... 100x

efficiency improvement from HW / SW co-optimization



## 

Architect
your
ambition

