



# Bet on the **Ecosystem of the Future**

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# Timeline of RISC-V in China (partial)

- 2015, Chinese version position paper was published on CCCF
- 2015, organizations became the founding members of RISC-V Foundation
- 2016, scholars present research work at the 4<sup>th</sup> RISC-V Workshop
- 2017, the 6<sup>th</sup> RISC-V Workshop was held in Shanghai
- 2018, CRVA and CRVIC were founded
- 2018, Alibaba/T-Head (BoD) and many RISC-V startups were founded
- 2019, CAS launched a project to promote RISC-V in China
- 2019, RIOS Lab was established (BoD)
- 2020, the 1<sup>st</sup> “One Student One Chip” Initiative was announced
- 2021, the 1<sup>st</sup> RISC-V Summit China was held
- 2021, Allwinner D1, XiangShan v1 and other ten RISC-V chips released
- 2021, BOSC (BoD) was founded
- 2022, more and more companies chose RISC-V, such as Tencent
- 2022, eleven RISC-V chips released
- 2023, Sophon announced 64-core RISC-V processor SG2042

# Contributions from China to the RISC-V Ecosystem

- **AOSP RISC-V** (upstreaming): main contributors (Alibaba T-Head, PLCT Lab@ISCAS, ESWIN, ...)
- **OpenJDK RISC-V** (upstreamed): main contributors & port maintainers (Huawei, Alibaba, PLCT Lab@ISCAS, ...)
- **V8 RISC-V** (upstreamed): main contributors & port maintainers (PLCT Lab@ISCAS), FutureWei, ...)
- **Firefox Spidermonkey RISC-V backend** (upstreamed): key contributors & port maintainers (PLCT Lab@ISCAS)
- **GNU Toolchain, Clang/LLVM, MLIR, QEMU, Spike, Gem5**: active contributors (RiVAI, Alibaba, PLCT Lab@ISCAS, Huawei, WindRiver, Tsinghua, ...)
- **Chisel**: active contributors & maintainers (PLCT Lab@ISCAS)
- **OpenCV RISC-V Vector Optimization**: key contributors (PLCT Lab@ISCAS)
- **OpenBLAS RISC-V Arch**: key contributors & maintainers (PerfXLab, ...)
- **Box64**: key contributors (PLCT Lab@ISCAS)
- **LuaJIT**: contributors (PLCT Lab@ISCAS)
- **Debian** (RISC-V port): many active contributors (PLCT Lab@ISCAS, ...)
- **Fedora** (RISC-V port): many active contributors (RedHat, PLCT Lab@ISCAS, ...)
- **Arch Linux** (RISC-V port): main contributors & maintainers (PLCT Lab@ISCAS, ...)
- **Gentoo Linux** (RISC-V port): main contributors & core developers (PLCT Lab@ISCAS, ...)
- **openEuler** (RISC-V): key contributors & maintainers (PLCT Lab@ISCAS, ...)
- .....

Source: Wei Wu@PLCT Lab

# > 4000 students participated in the OSOC Initiative

No.	Start	End of Enrollment	#Enrollment	#School	#Stu. Learning > 10%	#Stu. Finish
1 <sup>st</sup>	Aug, 2019	-	5	1	5	5
2 <sup>nd</sup>	Aug, 2020	-	11	5	11	11
3 <sup>rd</sup>	Jul, 2021	Sep, 2021	760	168	215	51
4 <sup>th</sup>	Feb, 2022	Aug, 2022	1753	328	215	16
5 <sup>th</sup>	Aug, 2022	In progress	1689	335	148	6
6 <sup>th</sup>	<b>Will start in July, 2023</b>					

Updated: Jun 6<sup>th</sup>, 2023



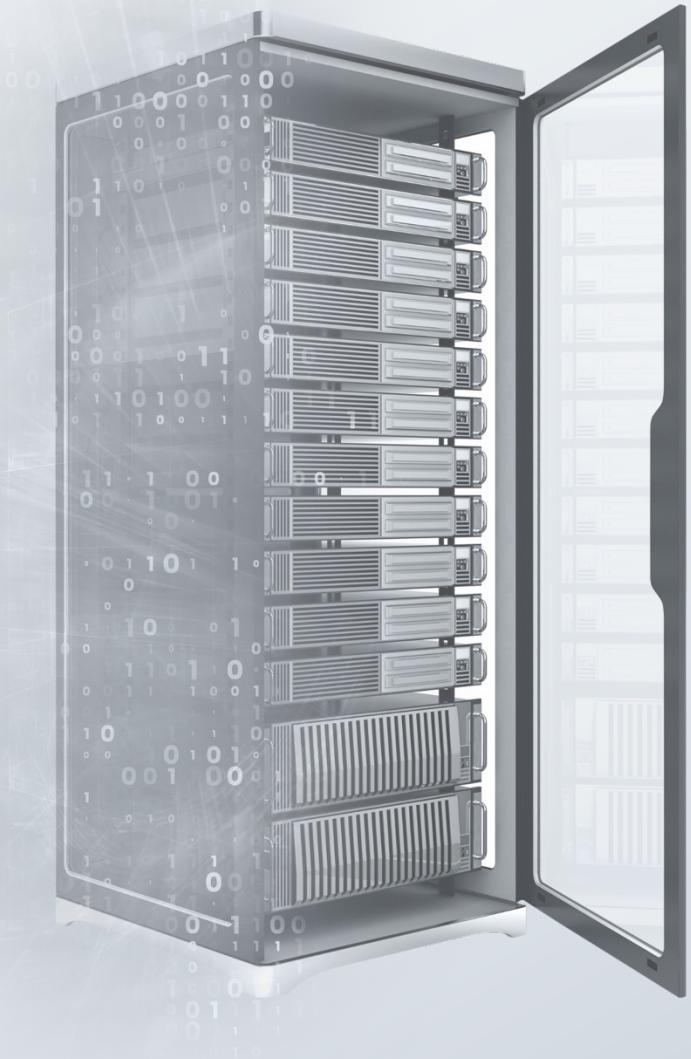
# China is taking a lead in RISC-V adoption, by doing it right

- Taught in major universities
- Building the ecosystem
- Partnering with global ecosystem to take it to the world



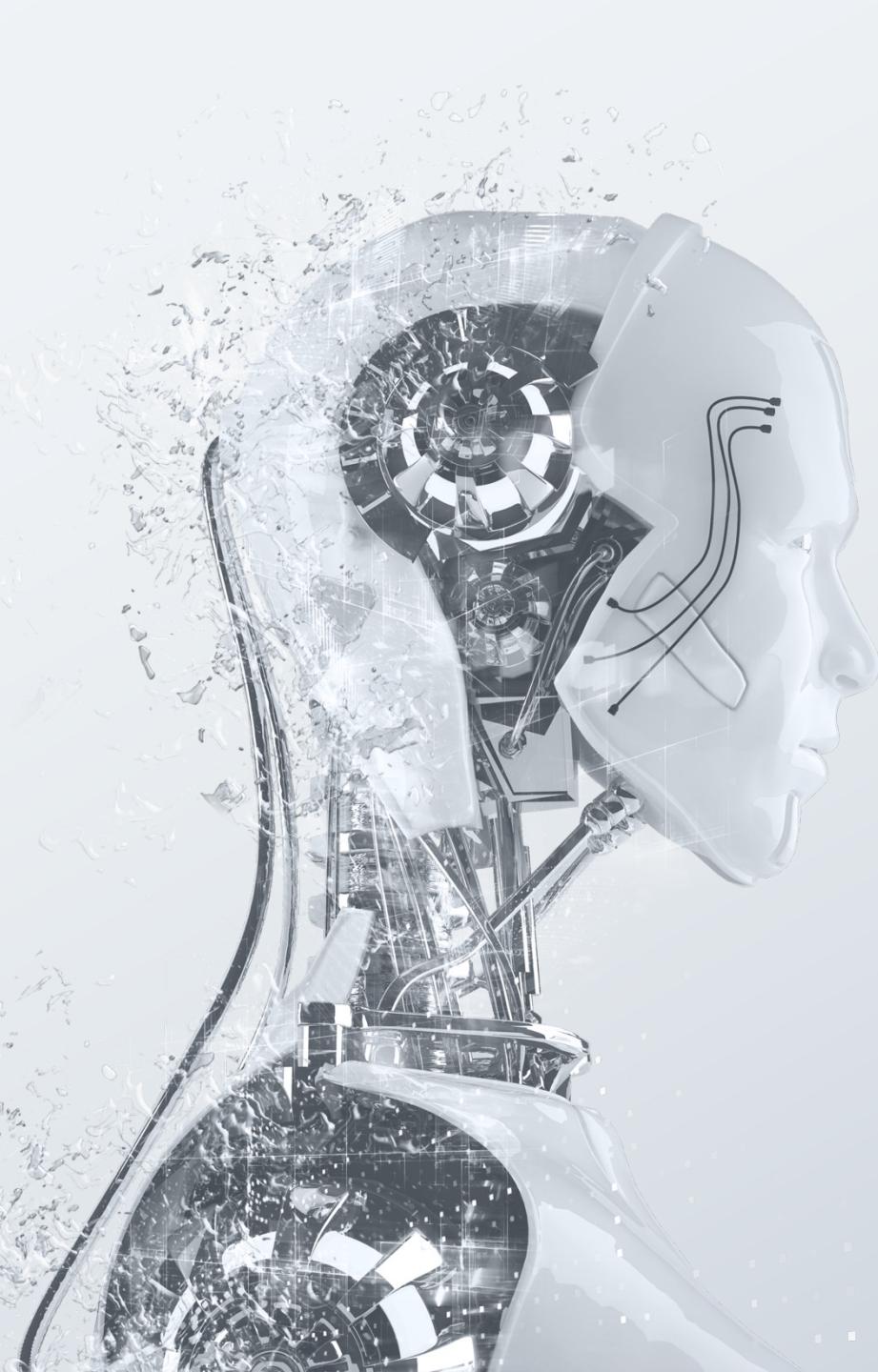
# Enabling next-generation Automotive

- Electric vehicles & Autonomous driving is disrupting the Automotive industry
- RISC-V enables best-in-class ADAS/AD solutions that are programmable and future proof
- Single common ISA for all compute (AI/ML, high-performance, micros) simplifies software complexity



## Highest performance RISC-V for Infrastructure

- Customize best-in-class solutions for applications and workloads of your interest
- Reduce single-point supply chain risks



## AI from the edge to the cloud

- Generative AI and LLM workloads prove need for programmability
- Optimize your AI/ML solution with RISC-V vectors, and leverage the ecosystem built on an open standard



## Power efficiency matters in Consumer and Mobile

- RISC-V provides 30-40% better power efficiency than Arm
- Google porting Android, as leading mobile suppliers adopt RISC-V



# Bet on RISC-V

RISC-V is *the* modern, global, open ISA, which allows **flexibility** and **freedom** of design, eliminates proprietary handcuffs, **delivers** performance and **power** others can't, and **benefits** the common good



# RISC-V is the ecosystem of the future

- Open & Collaborative
  - Not controlled by a single entity
- Single ISA that scales from microcontrollers to datacenters
  - Leverage stable & rigid base ISA and extend
- Every \$ you spend on software will benefit you
  - You are not spending money to lock yourself into a SW ecosystem built around a proprietary ISA
- Large developer ecosystem

# Diversity != Fragmentation

- Fragmentation = Same thing done different ways
- Diversity = Solving different problems
  - Each domain has a different set of requirements that have to be met
- Open standards are the antidote to fragmentation
  - Leverage stable & rigid base ISA and extend
  - Filling ISA gaps reduces motivation for fragmentation
  - ISA profiles: ISA extension packages for different domains
  - HW/SW platform standards for portability

# RISC-V Results in Best Perf/W & Perf/mm<sup>2</sup>

- Pick the right ISA
- Pick the right RISC-V vendor
- Think about every W you will save
- Think about every mm<sup>2</sup> you will save
- Calculate your TCO
  - RISC-V is the obvious choice
  - SW ecosystem development cost is easily covered

RISC-V is here, time is now  
**一万年太久，只争朝夕**



Enabling **innovators**

[www.sifive.com](http://www.sifive.com)