



# Waveform Terminator

## 填补底层波形与高层语义鸿沟的调试栈

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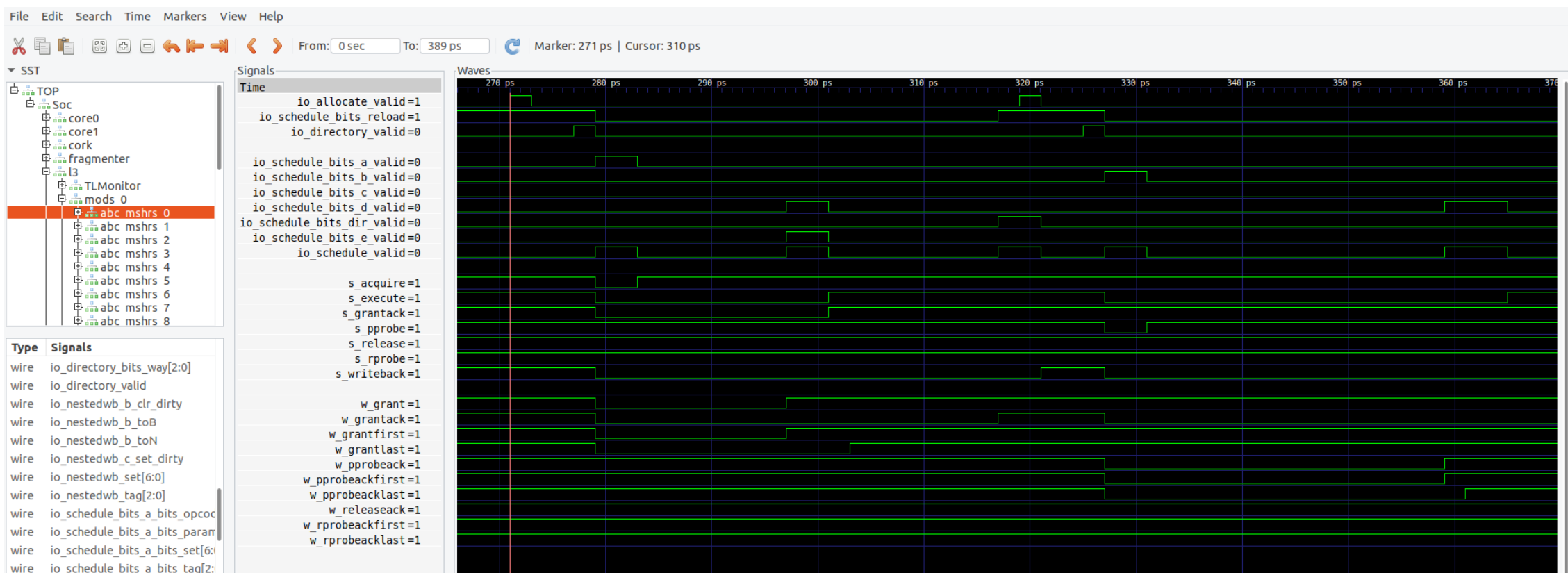
中科院计算所

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# 传统硬件仿真调试方法: 波形分析

- 分析波形的过程实际上是从波形中提取信息的过程
- 波形本身不包含语义信息，人工分析效率低、任务重



# Waveform Terminator: 新型硬件调试栈

- 我们设计了一套工具，能够将高层语义信息从波形中提取出来

日志分析

对事件日志进行高层次的语义分析和检查

Firrtl Transform

用于将Chisel中开发者关心的事件自动转换成“Xiang”语言描述的转换规则

Xiang语言

自定义的DSL “Xiang” 语言，用于描述波形信息到事件日志的转换规则

波形文件Parser

解析波形文件

# Waveform Terminator: 香语言

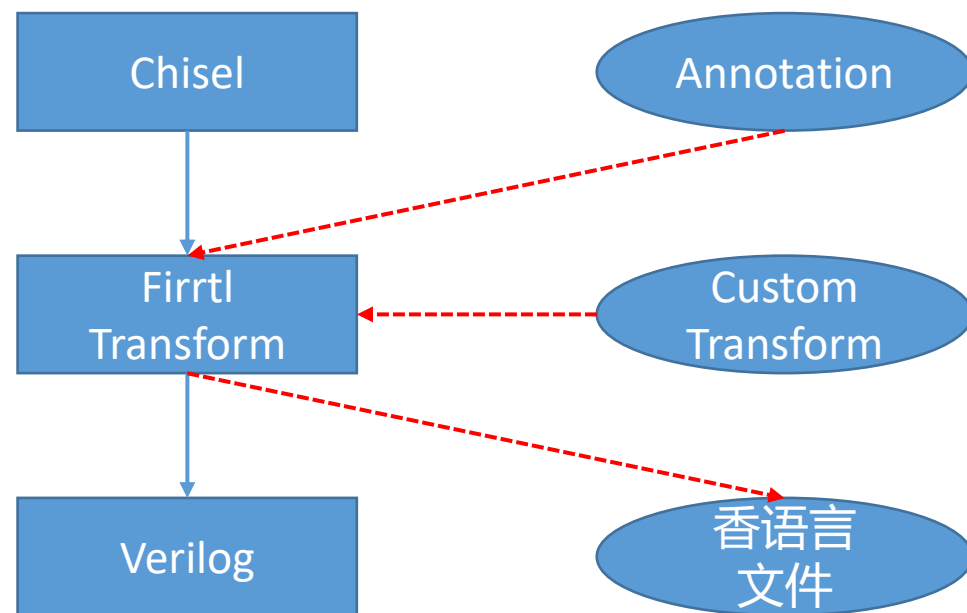
- 一种DSL，用于描述底层波形到高层语义的转换规则
- 将基于波形的调试转换成基于事件的调试
- Waveform Terminator解析香语言并根据对应规则从波形中提取信息
- 语法简单易用
  - “name”: {expression}
  - 示例: “adder output fire” : { adder.io.out.valid && adder.io.out.ready }

# 🏔️ Waveform Terminator: 香语言

- 大型设计中，模块层次结构复杂
  - Chisel中的匿名信号生成Verilog后人工追踪困难
  - 手写香语言工作量太大
- 因此我们设计了两种辅助工具
  - Custom Firrtl Transform
  - Xiang Editor - 可视化编写界面
    - 提供信号、模块路径补全功能

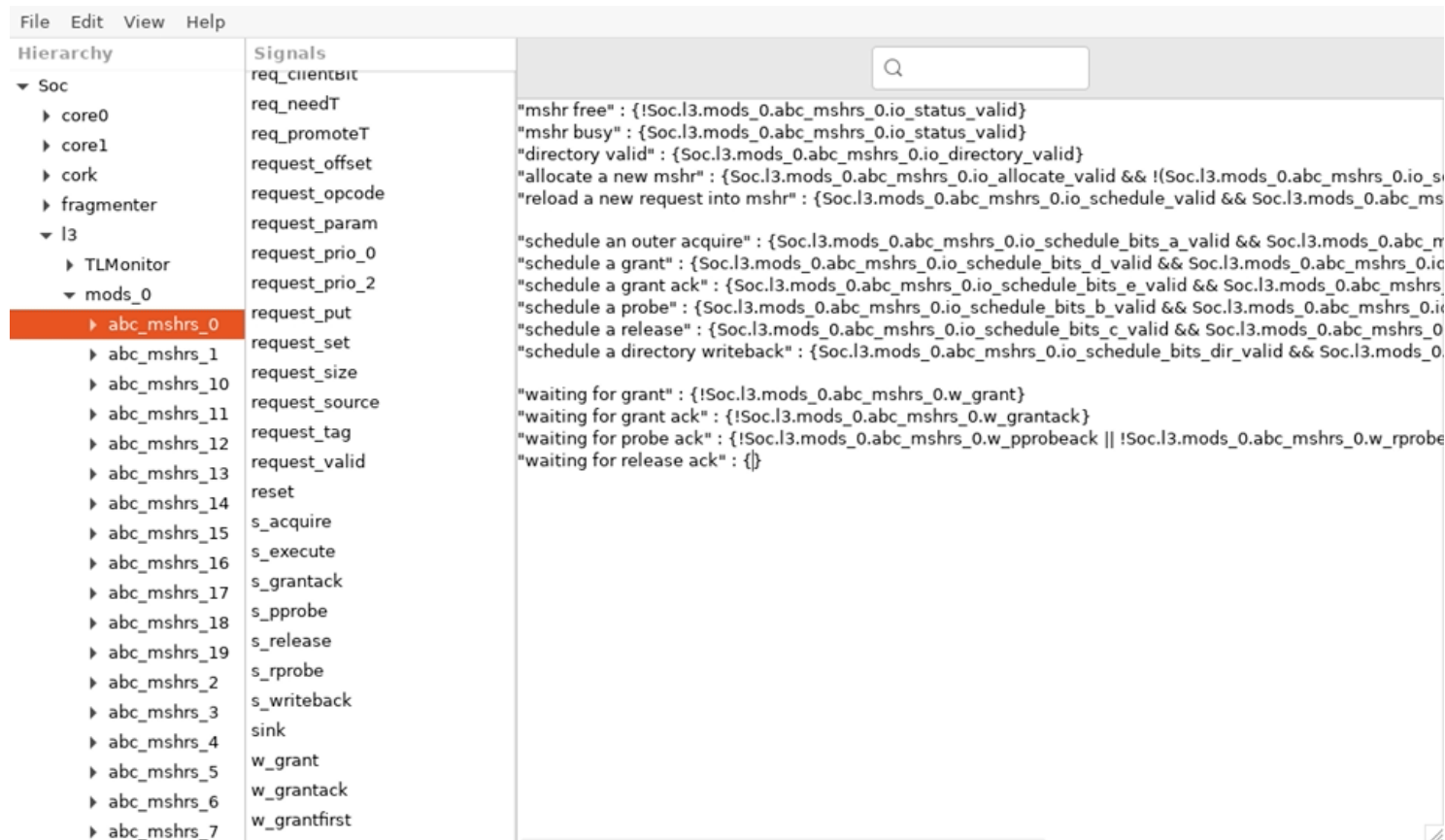
```
Log.add("adder output fire", io.out.fire())
```

“adder output fire” : {xxx.adder.adder\_output\_fire}



Custom Firrtl Transform workflow

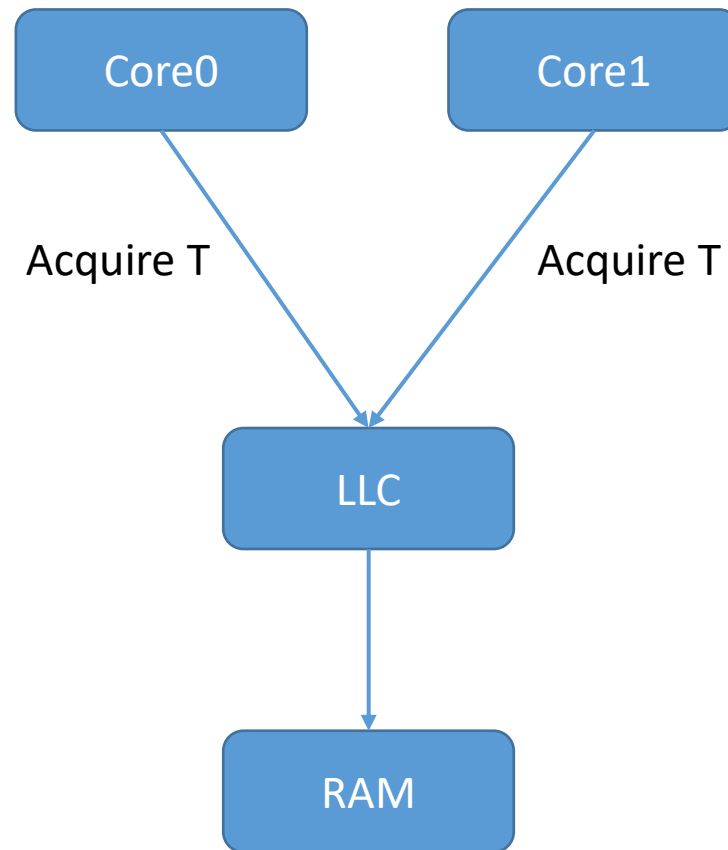
- 解析波形文件
- 提供设计的层次结构及每个子模块中的信号
- 提供自动信号补全功能
- 使修改、编辑香语言更加方便



使用Xiang Editor为Cache的工作过程编写事件转换规则

## Waveform Terminator: 应用示例

- 以分析基于Tilelink协议的LLC中一个MSHR对两个请求的处理流程为例
- 系统连接简化模型如右图所示
- Core0、Core1向LLC Acquire同一个Block，均要求T权限(写权限)
- 初始状态时Core0、Core1、LLC中均无该Block





# Waveform Terminator: 应用示例—编写转换规则

File Edit View Help

Hierarchy	Signals	
▼ Soc	req_clientBit	
▶ core0	req_needT	
▶ core1	req_promoteT	
▶ cork	request_offset	
▶ fragmenter	request_opcode	
▼ l3	request_param	
▶ TLMonitor	request_prio_0	
▼ mods_0	request_prio_2	
▶ abc_mshrs_0	request_put	"mshr free" : {!Soc.l3.mods_0.abc_mshrs_0.io_status_valid}
▶ abc_mshrs_1	request_set	"mshr busy" : {Soc.l3.mods_0.abc_mshrs_0.io_status_valid}
▶ abc_mshrs_10	request_size	"directory valid" : {Soc.l3.mods_0.abc_mshrs_0.io_directory_valid}
▶ abc_mshrs_11	request_source	"allocate a new mshr" : {Soc.l3.mods_0.abc_mshrs_0.io_allocate_valid && !Soc.l3.mods_0.abc_mshrs_0.io_schedule_valid}
▶ abc_mshrs_12	request_tag	"reload a new request into mshr" : {Soc.l3.mods_0.abc_mshrs_0.io_schedule_valid && Soc.l3.mods_0.abc_mshrs_0.io_status_valid}
▶ abc_mshrs_13	request_valid	"schedule an outer acquire" : {Soc.l3.mods_0.abc_mshrs_0.io_schedule_bits_a_valid && Soc.l3.mods_0.abc_mshrs_0.io_status_valid}
▶ abc_mshrs_14	reset	"schedule a grant" : {Soc.l3.mods_0.abc_mshrs_0.io_schedule_bits_d_valid && Soc.l3.mods_0.abc_mshrs_0.io_status_valid}
▶ abc_mshrs_15	s_acquire	"schedule a grant ack" : {Soc.l3.mods_0.abc_mshrs_0.io_schedule_bits_e_valid && Soc.l3.mods_0.abc_mshrs_0.io_status_valid}
▶ abc_mshrs_16	s_execute	"schedule a probe" : {Soc.l3.mods_0.abc_mshrs_0.io_schedule_bits_b_valid && Soc.l3.mods_0.abc_mshrs_0.io_status_valid}
▶ abc_mshrs_17	s_grantack	"schedule a release" : {Soc.l3.mods_0.abc_mshrs_0.io_schedule_bits_c_valid && Soc.l3.mods_0.abc_mshrs_0.io_status_valid}
▶ abc_mshrs_18	s_pprobe	"schedule a directory writeback" : {Soc.l3.mods_0.abc_mshrs_0.io_schedule_bits_dir_valid && Soc.l3.mods_0.abc_mshrs_0.io_status_valid}
▶ abc_mshrs_19	s_release	
▶ abc_mshrs_2	s_rprobe	
▶ abc_mshrs_3	s_writeback	
▶ abc_mshrs_4	sink	
▶ abc_mshrs_5	w_grant	"waiting for grant" : {!Soc.l3.mods_0.abc_mshrs_0.w_grant}
▶ abc_mshrs_6	w_grantack	"waiting for grant ack" : {!Soc.l3.mods_0.abc_mshrs_0.w_grantack}
▶ abc_mshrs_7	w_grantfirst	"waiting for probe ack" : {!Soc.l3.mods_0.abc_mshrs_0.w_pprobeack    !Soc.l3.mods_0.abc_mshrs_0.w_rprobeack}
		"waiting for release ack" : {!}





# Waveform Terminator: 应用示例—提取Log

- 输入：一个波形文件，一个香语言转换规则描述文件
- 输出：从波形中提取的Log

```
→ waveform-terminator ./wt --trace L3CacheExample.vcd --config L3CacheExample.xiang
[cycle = 0] "mshr free"
[cycle = 1] "mshr free"
[cycle = 2] "mshr free"
[cycle = 3] "mshr free"
[cycle = 4] "mshr free"
[cycle = 5] "mshr free"
[cycle = 6] "mshr free"
[cycle = 7] "mshr free"
[cycle = 8] "mshr free"
[cycle = 9] "mshr free"
[cycle = 10] "mshr free"
[cycle = 11] "mshr free"
[cycle = 12] "mshr free"
[cycle = 13] "mshr free"
[cycle = 14] "mshr free"
[cycle = 15] "mshr free"
[cycle = 16] "mshr free"
```

```
[cycle = 181] "schedule a grant"
[cycle = 181] "waiting for grant ack"
[cycle = 182] "mshr busy"
[cycle = 182] "waiting for grant ack"
[cycle = 183] "mshr busy"
[cycle = 183] "waiting for grant ack"
[cycle = 184] "mshr busy"
[cycle = 184] "waiting for grant ack"
[cycle = 185] "mshr busy"
[cycle = 185] "waiting for grant ack"
[cycle = 186] "mshr busy"
[cycle = 186] "waiting for grant ack"
[cycle = 187] "mshr busy"
[cycle = 187] "waiting for grant ack"
[cycle = 188] "mshr busy"
[cycle = 188] "waiting for grant ack"
[cycle = 189] "mshr busy"
[cycle = 189] "waiting for grant ack"
[cycle = 190] "mshr busy"
[cycle = 191] "mshr busy"
[cycle = 191] "schedule a directory writeback"
[cycle = 192] "mshr free"
[cycle = 193] "mshr free"
[cycle = 194] "mshr free"
→ waveform-terminator
```



# Waveform Terminator: 应用示例—Log分析

确认前进一步(n)倒退一步(N)

## Log

[cycle = 0] "mshr free"

[cycle = 1] "mshr free"

[cycle = 2] "mshr free"

[cycle = 3] "mshr free"

[cycle = 4] "mshr free"

[cycle = 5] "mshr free"

[cycle = 6] "mshr free"

[cycle = 7] "mshr free"

[cycle = 8] "mshr free"

[cycle = 9] "mshr free"

[cycle = 10] "mshr free"

[cycle = 11] "mshr free"

[cycle = 12] "mshr free"

[cycle = 13] "mshr free"

[cycle = 14] "mshr free"

[cycle = 15] "mshr free"

[cycle = 16] "mshr free"



# Waveform Terminator: 应用示例—Log分析





# Waveform Terminator: 应用示例—Log分析

## Log

[cycle = 145] "mshr busy"

[cycle = 145] "waiting for grant"

[cycle = 145] "waiting for grant ack"

[cycle = 146] "mshr busy"

[cycle = 146] "waiting for grant"

[cycle = 146] "waiting for grant ack"

[cycle = 147] "mshr busy"

[cycle = 147] "waiting for grant"

[cycle = 147] "waiting for grant ack"

[cycle = 148] "mshr busy"

[cycle = 148] "waiting for grant ack"

[cycle = 149] "mshr busy"

[cycle = 149] "schedule a grant"

[cycle = 149] "schedule a grant ack"

[cycle = 149] "waiting for grant ack"

[cycle = 150] "mshr busy"

[cycle = 150] "waiting for grant ack"

①

收到了RAM返回的数据

②

向Core0 返回数据

继续等待Core0的grant ack

Core0

Core1

② Grant data

LLC

① Grant data

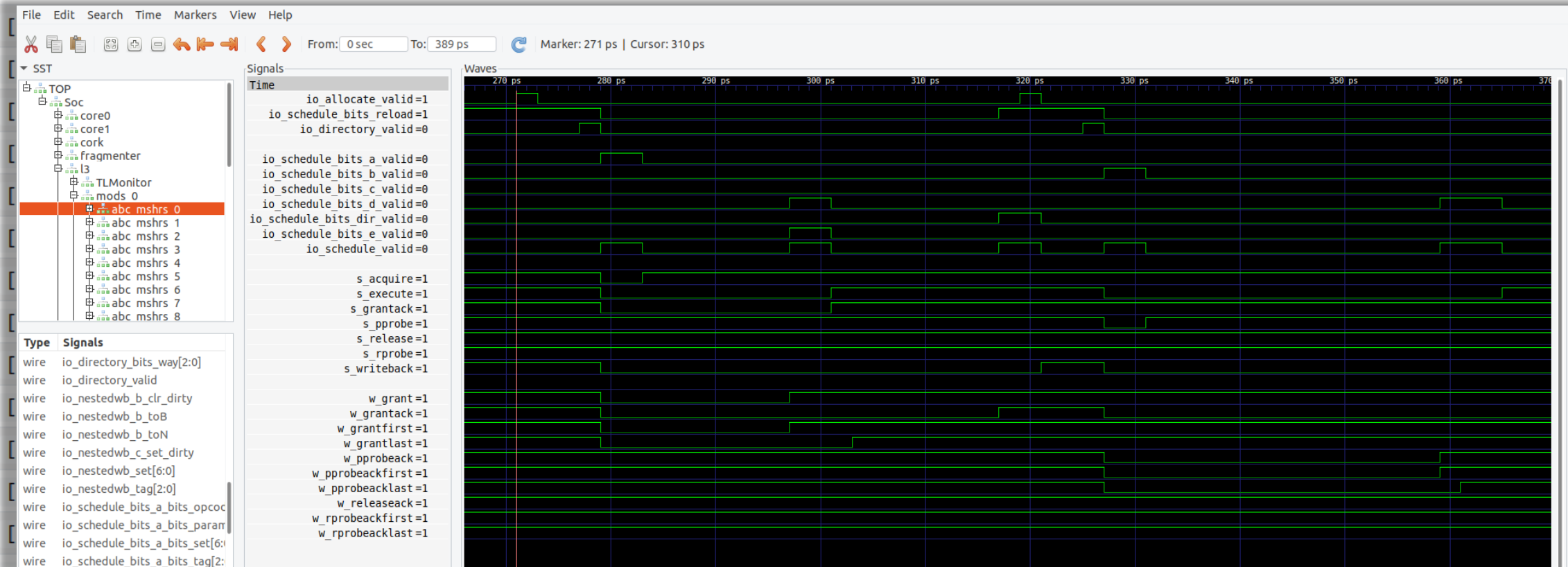
RAM



# Waveform Terminator: 与波形调试的对比

Log

[cycle = 145] "mshr busy"



[cycle = 149] "waiting for grant ack"

[cycle = 150] "mshr busy"

[cycle = 150] "waiting for grant ack"

RAM

# Waveform Terminator: 问题讨论

- 为何不使用fwrite/display/printf?
  - 每次修改事务转换规则后需要重新仿真
  - 对于使用Chisel开发的电路，修改/添加printf后还需要重新生成Verilog

**敬请批评指正！**



# Waveform Terminator: 应用示例—Log分析







# Waveform Terminator: 应用示例—Log分析

## Log

[cycle = 145] "mshr busy"

[cycle = 145] "waiting for grant"

[cycle = 145] "waiting for grant ack"

[cycle = 146] "mshr busy"

[cycle = 146] "waiting for grant"

[cycle = 146] "waiting for grant ack"

[cycle = 147] "mshr busy"

[cycle = 147] "waiting for grant"

[cycle = 147] "waiting for grant ack"

[cycle = 148] "mshr busy"

[cycle = 148] "waiting for grant ack"

[cycle = 149] "mshr busy"

[cycle = 149] "schedule a grant"

[cycle = 149] "schedule a grant ack"

[cycle = 149] "waiting for grant ack"

[cycle = 150] "mshr busy"

[cycle = 150] "waiting for grant ack"

①

收到了RAM返回的grant

②

向Core0 grant数据

继续等待Core0的grant ack

Core0

Core1

② Grant data

LLC

① Grant data

RAM



# Waveform Terminator: 应用示例—Log分析





# Waveform Terminator: 应用示例—Log分析

确认前进一步(n)倒退一步(N)

## Log

[cycle = 160] "mshr busy"

[cycle = 161] "mshr busy"

[cycle = 162] "mshr busy"

[cycle = 162] "directory valid"

[cycle = 163] "mshr busy"

[cycle = 163] "waiting for grant ack"

[cycle = 163] "waiting for probe ack"

[cycle = 164] "mshr busy"

[cycle = 164] "schedule a probe"

[cycle = 164] "waiting for grant ack"

[cycle = 164] "waiting for probe ack"

[cycle = 165] "mshr busy"

[cycle = 165] "waiting for grant ack"

[cycle = 165] "waiting for probe ack"

查directory, 发现Core0占有该Block

Probe Core0

Core0

Core1

Probe

LLC

RAM

# Waveform Terminator: 应用示例—Log分析

## Log

[cycle = 175] "mshr busy"

[cycle = 175] "waiting for grant ack"

[cycle = 175] "waiting for probe ack"

[cycle = 176] "mshr busy"

[cycle = 176] "waiting for grant ack"

[cycle = 176] "waiting for probe ack"

[cycle = 177] "mshr busy"

[cycle = 177] "waiting for grant ack"

[cycle = 177] "waiting for probe ack"

[cycle = 178] "mshr busy"

[cycle = 178] "waiting for grant ack"

[cycle = 178] "waiting for probe ack"

[cycle = 179] "mshr busy"

[cycle = 179] "waiting for grant ack"

收到probe ack

[cycle = 180] "mshr busy"

[cycle = 180] "waiting for grant ack"

Core0

Core1

Probe ack

LLC

RAM

# Waveform Terminator: 应用示例—Log分析

## Log

[cycle = 180] "mshr busy"

[cycle = 180] "waiting for grant ack"

[cycle = 181] "mshr busy"

[cycle = 181] "schedule a grant" 向Core1 grant数据

[cycle = 181] "waiting for grant ack"

[cycle = 182] "mshr busy"

[cycle = 182] "waiting for grant ack"

[cycle = 183] "mshr busy"

[cycle = 183] "waiting for grant ack"

[cycle = 184] "mshr busy"

[cycle = 184] "waiting for grant ack"

[cycle = 185] "mshr busy"

[cycle = 185] "waiting for grant ack"

Core0

Core1

Grant data

LLC

RAM



# Waveform Terminator: 应用示例—Log分析

