KD32F328CBT6

Arm® Cortex® -M0 based 32-bit MCU

Flash: up to 128 Kbytes, SRAM: up to 24 Kbytes

48 pins

1Msps 12-bit high accuracy ADC

5-channel DMA controller

32/16-bit Divider

CRC calculation unit

10 timers

Low power modes : Sleep, Stop, Standby

Two I2C interfaces

Two USART interfaces

Two SPIs with 4 to 16 programmable bit frames

Rev 1.00

1. Features

Core

- 32-bit Arm® Cortex® -M0 Core
- Up to 96 MHz working frequency
- 32-bit single-cycle multiplier
- Serial wire debug (SWD) with 2 watchpoints and 4 break points

Memories

- 128 KB Flash
- 24 KB SRAM

Reset and power management

- Digital and I/O supply : V_{DD}= 2.0 V – 5.5 V
- Analog supply : $V_{DDA} = V_{DD}$
- Power-on/Power down reset (POR/PDR)
- Programmable voltage detector (PVD)
- Low power modes : Sleep, Stop, Standby
- Low power current @ 3.3 V :
  - Standby : 1.4 μA

Clock management

- 4 to 32 MHz crystal oscillator
- 32 kHz oscillator for RTC with calibration
- Internal 40 kHz RC oscillator
- Internal 14 MHz RC oscillator
- Internal 48 MHz oscillator with calibration
- PLL supports 2~16 frequency doubling

Peripheral features

- Up to 37 fast I/Os
  - All mappable on external interrupt vectors
- 5-channel DMA controller
- CRC calculation unit
- 32/16-bit Divider
  - 32/16 signed division
  - Divide by zero interrupt
  - 10 Bus cycle to calculate
- 1Msps 12-bit ADC
  - Up to 16 channels
  - Internal channels
    - Temperature sensor (V_{TS})
    - Reference voltage (V_{REFINT})
    - Operational amplifier (V_{OP})
    - I/O Sample and hold circuit (V_{IOSH})
  - Conversion range : 0 – V_{REF+}
  - 3 V_{REFINT} : 0.625V, 1.5V, 2.5 V
- 3 fast analog comparators
  - programmable input and output
- Calendar RTC
  - Alarm and periodic wakeup from Stop/Standby
- 10 timers
  - TIM1, 16-bit, 4-channel PWM, 3-channel with complementary
  - TIM3, 16-bit, 4-channel PWM
  - TIM14, 16-bit, 1-channel PWM
  - TIM15, 16-bit, 2-channel PWM, 1-channel PWM complementary
  - TIM16/TIM17, 16-bit, 1-channel PWM, 1-channel with complementary
  - TIM6, 16-bit, basic timer
  - Independent and system watchdog timers
  - 24-bit System tick timer
- Communication Interfaces
  - 2 I2C interfaces, I2C1 support FM+ and SMBus
  - 2 USART interfaces supporting master synchronous SPI and modem control
  - 2 SPIs with 4 to 16 programmable bit frames
- 96-bit unique ID
- Packages : LQFP48

Contents

2. Description

The KD32F328CBT6 microcontrollers incorporate the high-performance ARM® Cortex®-M0 32-bit RISC core operating at up to 96 MHz frequency, high-speed embedded memories (up to 128 kbytes of Flash memory and 24 kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (two I2Cs, two SPI, two USARTs), one 12-bit ADC, seven 16-bit timers and an advanced-control PWM timer.

KD32F328CBT6 microcontrollers operate in the -40 to +105 °C temperature ranges, from a 2.0 to 5.5 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Table 2.1 KD32F328CBT6 family device festures and peripheral counts

Peripheral		KD32F328CBT6
Flash	kbytes	128
SRAM	kbytes	24
Timers	Advanced control	1 (16bit)
	General purpose	5 (16bit)
	Basic	1 (16bit)
Comm. Interfaces	SPI	2
	I2C	2
	USART	2
32/16 Divider		√
12-bit ADC (number of channels)		10 ext + 6 int
Analog comparator		3
Operational amplifier		2
GPIOs		39
Max. CPU frequency		96 MHz
Operating voltage		2.0 – 5.5 V
Operating temperature		-40 – 105 °C
Package		LQFP48

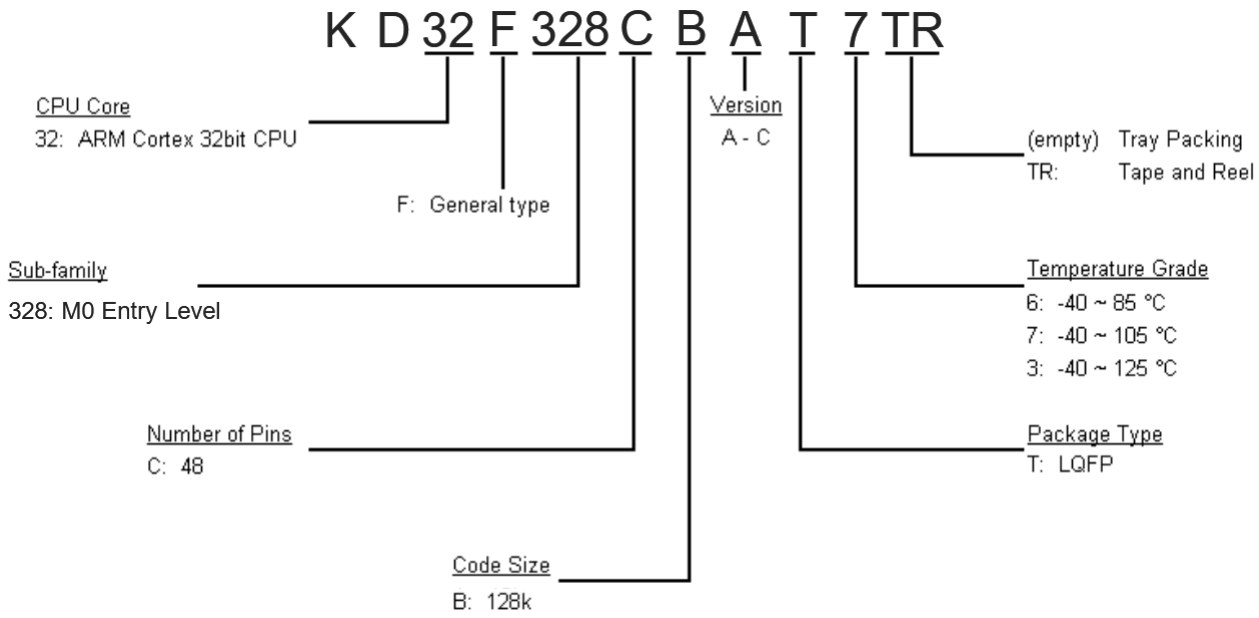


Figure 2.1 MCU Product Ordering Information

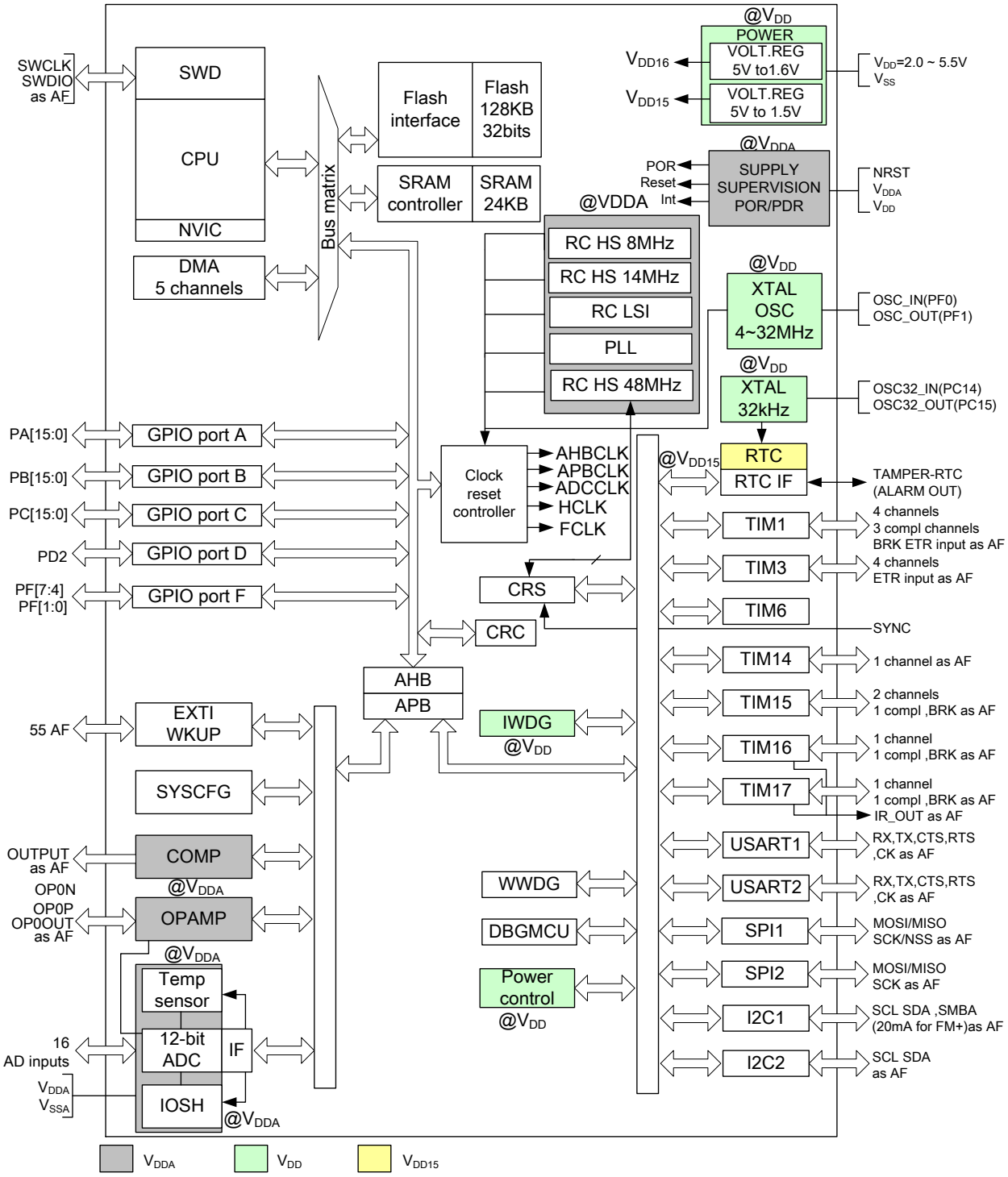


Figure 2.2 Block Diagam

3. Function overview

3.1. Arm® Cortex® -M0 Core

The Arm® Cortex® -M0 is a generation of ARM 32-bit RISC processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The Arm® Cortex® -M0 processors feature exceptional code-efficiency, delivering the high performance expected from an ARM core, with memory sizes usually associated with 8- and 16-bit devices.

The KD32F328CBT6 devices embed ARM core and are compatible with all ARM tools and software.

3.2. Memories

The device has the following features:

- 24 kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.
- The non-volatile memory is divided into two arrays:

— 128kbytes of embedded Flash memory for programs and data
— Option bytes

The option bytes are used to write-protect the memory (with 0.5 KB granularity) and/or readout-protect the whole memory with the following options:

—Level 0: no readout protection
—Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
—Level 2: chip readout protection, debug features (Cortex®-M0 serial wire) and boot in RAM selection disabled

3.3. Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- boot from User Flash memory
- boot from System Memory
- boot from embedded SRAM

Table 3.1 Boot modes configuration

configuration		Mode
nBOOT1	BOOT0 pin	
x	0	Flash memory
1	1	System Memory
0	1	embedded SRAM

3.4. Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.5. Power management

3.5.1. Power supply schemes

- V_{DD}=2.0 to 5.5 V: external power supply for I/Os and the internal regulator. It is provided externally through VDD pins.
- V_{DDA}=V_{DD} : external analog power supply for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4V when the ADC_VREF is V_{DDA}, minimum voltage to be applied to V_{DDA} is 2.7V when the ADC_VREF is internal reference voltage 2.5V). It is provided externally through V_{DDA} pin. The V_{DDA} voltage level must be equal to the VDD voltage level.

3.5.2. Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$.

- The POR monitors only the V_{DD} supply voltage. During the startup phase V_{DDA} and V_{DD} power-on together, and V_{DDA} should be equal to $V_{DD.}$
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state.The PVD is enabled by software

3.5.3. Voltage regulator

The KD32F328CBT6 microcontrollers have a 1.6V regulator and a 1.5V regulator.

The 1.6V regulator has two operating modes and it is always enabled after reset.

- Normal: Normal is used in normal operating mode or Stop mode
- LP: Low power (LP) can be used in Stop mode where the power demand is reduced.

In Standby mode, it is put in power down mode. In this mode, the 1.6V regulator output is in high impedance and the kernel circuitry is powered down, including zero consumption (but the contents of the register and SRAM are lost)

The 1.5V regulator can be enabled/disabled by Software.

3.5.4. Low-power modes

The KD32F328CBT6 microcontrollers support three low-power modes to achieve the best balance between low power consumption, short startup time and available wakeup sources.
Note: To ensure that the chip can enter the lowest power consumption state, all I/Os must have a fixed state (output 0 or 1, input pull-down or pull-up), or configured in analog mode. They can't be left floating, so as to avoid unnecessary power leakage.

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.6V domain are stopped, the PLL, the HSI RC, HSI14 RC, HSI48 RC and the HSE crystal oscillators are disabled. The 1.6V voltage regulator can also be put either in normal or in low power mode.

The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines or RTC.

The IWDG can work in STOP mode.

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal 1.6V voltage regulator is switched off so that the entire 1.6V domain is powered off. The PLL, the HSI RC, HSI14 RC, HSI48 RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

IWDG and RTC and corresponding clocks still work normally in standby mode.

3.6. GPIO

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.7. Clocks and startup

System clock selection is performed on startup, however the HSI RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the HSI RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 72 MHz.

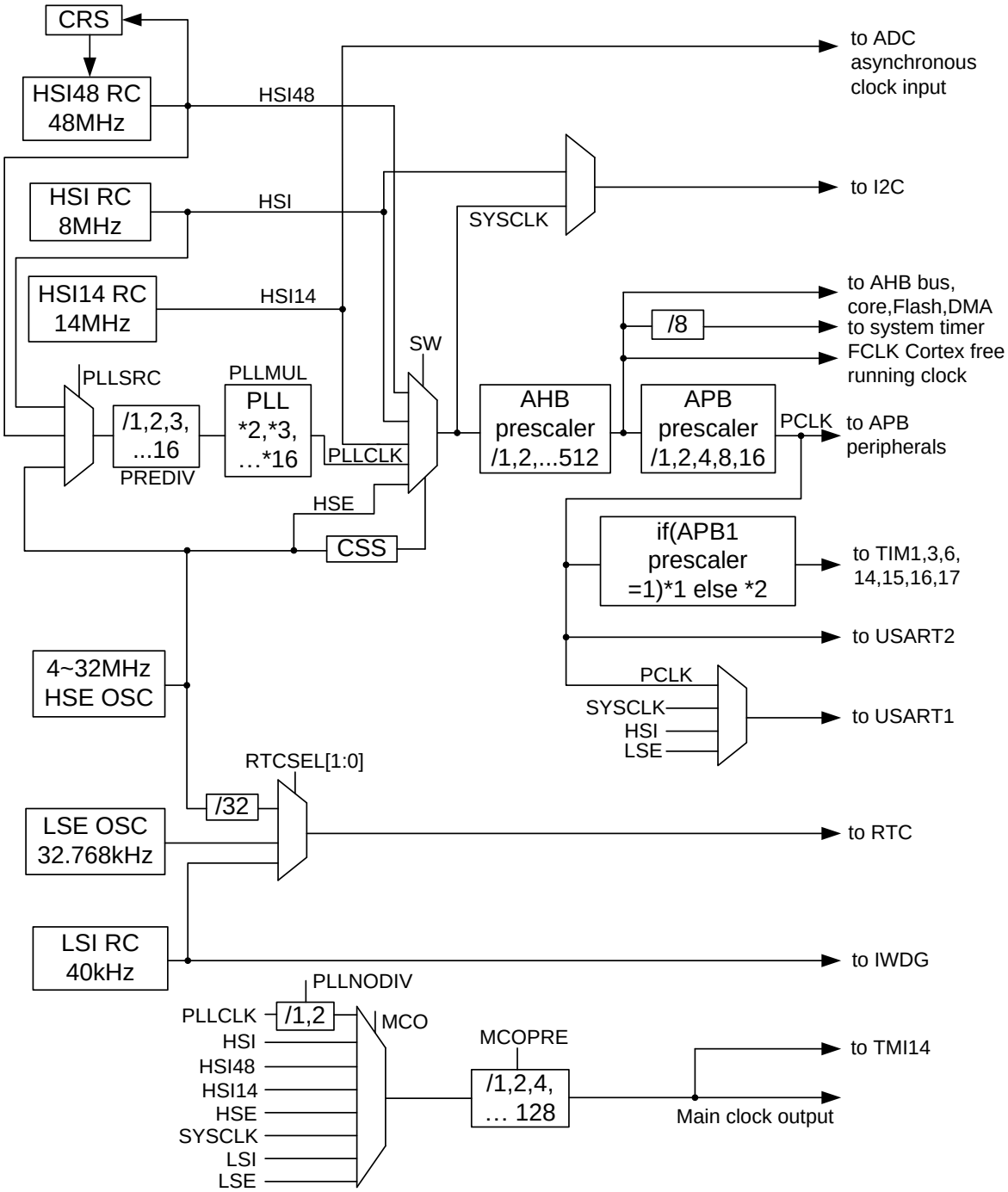


Figure 3.1 Clock tree

3.8. 32/16-bit Divider

The device embeds a 32/16-bit divider for user data division. The dividend is 32 bits and the divisor is 16 bits. It needs 10 Bus cycles to calculate. The divider supports divide by zero interrupt.

3.9. Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPIx , I2Cx, USARTx, all TIMx timers (except TIM14) and ADC.

3.10. Interrupts and events

3.10.1. Nested vectored interrupt controller (NVIC)

The KD32F328CBT6 family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.10.2. Extended interrupt/event controller (EXTI)

The EXTI consists of 32 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period.

3.11. Analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter has up to 16 external and 6 internal (temperature sensor, voltage reference, 2 I/O sample and hold circuits, 2 operational amplifiers) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all

selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.11.1. Temperature sensor (V_{TS})

The temperature sensor(TS) is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage V_{TS} into a digital value.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated. The temperature sensor factory calibration data are stored in the system memory area, accessible in read-only mode.

Table 3.2 Temperature sensor calibration values

Name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 25 °C (±5 °C), V_{DDA}=3.3 V(±10 mV)	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at a temperature of 110 °C (±5 °C), V_{DDA}=3.3 V(±10 mV)	0x1FFF F7C2 - 0x1FFF F7C3

3.11.2. Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part during production test and stored in the system memory area. It is accessible in read-only mode.

Table 3.3 Internal voltage reference calibration values

Name	Description	Memory address
V_{REFINT_CAL}	Raw data acquired at a temperature of 25 °C (±5 °C), V_{DDA} = 3.3 V(±10 mV)	0x1FFF F7BA - 0x1FFF F7BB

3.11.3. I/O sample and hold circuit (V_{IOSH})

The I/O sample and hold circuit is used to hold the input voltage (V_{IOSH}) for ADC conversion. The V_{IOSH} is internally connected to the ADC_IN18 input channel. And the ADC should convert V_{IOSH} as soon as possible to avoid error because the hold time is limited.

3.11.4. Operational amplifier (V_{OP})

The output of OPAMP1 is internally connected to the ADC_IN18 input channel or IOSH1. The output of OPAMP2 is internally connected to the ADC_IN19 input channel or IOSH2.The offset voltage of OPAMP is individually factory-calibrated and stored in the system memory area (read only), which will be auto reloaded to the register of OPAMP after power on and can be accessed by users.

3.12. Timers and watchdogs

The KD32F328CBT6 devices include five general-purpose timers, a basic timer and an advanced control timer.

Table 3.4 Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture /Compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, Up/down	integer from 1 to 65536	√	4	3
General purpose	TIM3	16-bit	Up, down, Up/down	integer from 1 to 65536	√	4	—
	TIM14	16-bit	Up	integer from 1 to 65536	√	1	—
	TIM15	16-bit	Up	integer from	√	2	1

				1 to 65536			
	TIM16, TIM17	16-bit	Up	integer from 1 to 65536	√	1	1
Basic	TIM6	16-bit	Up	integer from 1 to 65536	√	0	—

3.12.1. Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- input capture
- output compare
- PWM generation (edge or center-aligned modes)
- one-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

3.12.2. General-purpose timers (TIM3/TIM14/TIM15/TIM16/TIM17)

There are five synchronizable general-purpose timers embedded in the KD32F328CBT6 devices. Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM3

KD32F328CBT6 devices feature a synchronizable 4-channel general-purpose timer. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output.

The TIM3 general-purpose timer can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

TIM15/TIM16/TIM17

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

TIM15, TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

3.12.3. Basic timers (TIM6)

TIM6 can be used as generic 16-bit time bases.

3.12.4. Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.12.5. ystem window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.12.6. SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- a 24-bit down counter
- autoreload capability
- maskable system interrupt generation when the counter reaches 0
- programmable clock source

3.13. Leading Edge Blanking(LEB) and Filter(FLT)

The device embeds 3 LEB counters, 1 I/O FLT and 3 comparator FLTs. In high speed switching application, the transition of switch may produce break source noises and the comparator output noises. The LEB&FLT can used for blanking or filtering those noises.

The TIM1 break input, TIM15 break input and PVD output break are only support LEB. The output of comparator and comparator output break both support LEB and FLT.

- S

3.14. Real-time clock (RTC)

The RTC is an independent BCD timer/counter. Its main features are the following:

- calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- automatic correction for 28, 29 (leap year), 30 and 31 day of the month
- programmable alarm with wake up from Stop and Standby mode capability
- RTC on-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock
- digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- Two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection
- timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection
- reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision

The RTC clock sources can be:

- a 32.768 kHz external crystal
- the internal low-power RC oscillator (typical frequency of 40 kHz)
- the high-speed external clock divided by 32

3.15. Inter-integrated circuit interface (I2C)

Up to two I2C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (up to 100 kbit/s), Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive on most of the associated I/Os.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). They also include programmable analog and digital noise filters.

Table 3.5 Comparison of I2C1 and I2C2

I2C features	I2C1	I2C2
7-bit addressing mode	√	√
10-bit addressing mode	√	√
Standard mode	√	√
Fast mode	√	√
Independent clock	√	—
SMBus	√	—
Fast Mode Plus with 20 mA output drive I/Os	√	—
Wakeup from STOP	—	—

3.16. Universal synchronous/asynchronous receiver/transmitter (USART)

The device embeds two universal synchronous/asynchronous receivers/transmitters (USART1, USART2) which communicate at speeds of up to 9 Mbit/s.They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1 have a clock domain independent of the CPU clock.

Table 3.6 Comparison of USART1 and USART2

USART features	USART1	USART2
Hardware flow control for modem	√	√
Continuous communication using DMA	√	√
Multiprocessor communication	√	√
Synchronous mode	√	√
Single-wire half-duplex communication	√	√
Receiver timeout interrupt	√	—
Auto baud rate detection	√	—
RS485 Driver enable	√	√

3.17. Serial peripheral interface (SPI)

Two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits. The SPI interfaces can be served by the DMA controller.

Table 3.7 SPI features

SPI features	SPI1	SPI2
Hardware CRC calculation	√	√
FIFO Rx/Tx FIFO	√	√
NSS pulse mode	√	√
TI mode	√	√

3.18. Clock recovery system

The KD32F328CBT6 embeds a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be derived from from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.19. Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

4. Pinouts and pin description

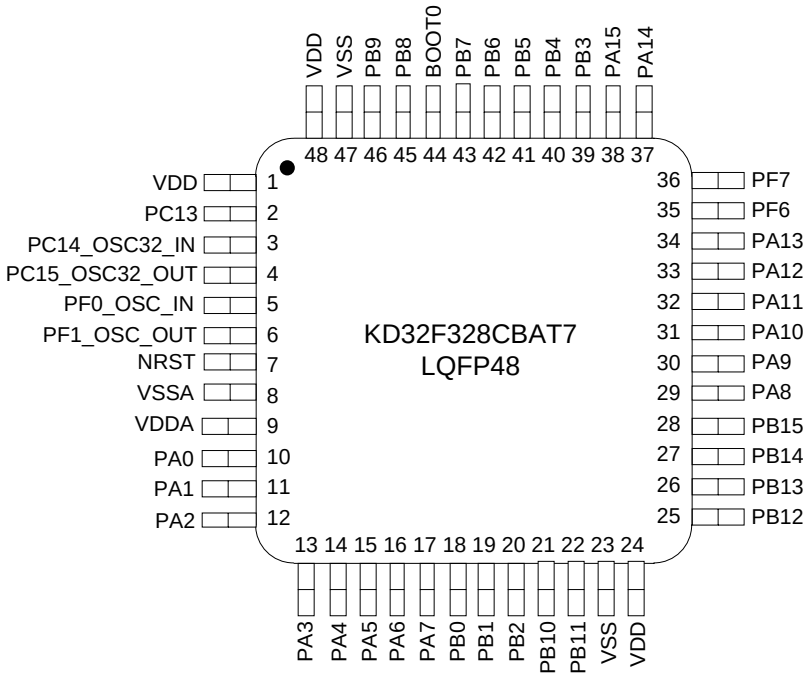


Figure 4.2 LQFP48 package pinout

Table 4.1 KD32F328CBT6 pin definitions

KD32F328CBT6					
LQFP48	Pin name	Pin type	Structure	AF	Add. Func
1	VDD	S		Complementary power supply	
2	PC13	I/O	FC	—	RTC_TAMP1
					RTC_TS
					RTC_OUT
					WKUP2
3	PC14-OSC32_IN (PC14)	I/O	FC	—	OSC32_IN
					RTC_OUT
4	PC15-OSC32_OUT (PC15)	I/O	FC	—	OSC32_OUT
					RTC_OUT
5	PF0-OSC_IN (PF0)	I/O	FC	—	OSC_IN
6	PF1-OSC_OUT (PF1)	I/O	FC	—	OSC_OUT
7	NRST	I/O	RST	Device reset input / internal reset output(active low)	
8	VSSA	S		Analog ground	
9	VDDA	S		Analog power supply	
10	PA0	I/O	FC	USART2_CTS	ADC_IN0
				COMP1_OUT	RTC_TAMP2
				—	WKUP1
					[COMP1_VIN]
					OP1OUT
11	PA1	I/O	FC	EVENTOUT	ADC_IN1
				USART2_RTS	[COMP1_VIP]
				—	OP1+
					[COMP2_VIP]
12	PA2	I/O	FC	USART2_TX	ADC_IN2
				TIM15_CH1	[COMP2_VIN]
				COMP2_OUT	OP1-
13	PA3	I/O	FC	USART2_RX	ADC_IN3
				TIM15_CH2	[COMP2_VIP]
				—	OP2+

KD32F328CBT6					
LQFP48	Pin name	Pin type	Structure	AF	Add. Func
14	PA4	I/O	FC	SPI1_NSS	ADC_IN4
				USART2_CK	—
				TIM14_CH1	—
				—	—
					—
					—
					—
					—
					—
					—
15	PA5	I/O	FC	SPI1_SCK	—
				MCO	—
				—	—
					ADC_IN5
					—
16	PA6	I/O	FC	SPI1_MISO	ADC_IN6
				TIM3_CH1	
				TIM1_BKIN	
				TIM16_CH1	
				EVENTOUT	
				COMP1_OUT	
17	PA7	I/O	FC	SPI1_MOSI	ADC_IN7
				TIM3_CH2	
				TIM14_CH1	
				TIM1_CH1N	
				TIM17_CH1	
				EVENTOUT	
				COMP2_OUT	
18	PB0	I/O	FC	TIM3_CH3	ADC_IN8 (IOSH2)
				TIM1_CH2N	—
				EVENTOUT	
19	PB1	I/O	FC	TIM3_CH4	ADC_IN9（IOSH1）
				TIM14_CH1	
				TIM1_CH3N	—
20	PB2	I/O	FC	—	—

KD32F328CBT6					
LQFP48	Pin name	Pin type	Structure	AF	Add. Func
21	PB10	I/O	FC	I2C2_SCL	—
22	PB11	I/O	FC	I2C2_SDA	—
				EVENTOUT	
23	VSS	S		Ground	
24	VDD	S		Digital power supply	
25	PB12	I/O	FC	SPI2_NSS	—
				TIM1_BKIN	
				EVENTOUT	
26	PB13	I/O	FC	SPI2_SCK	—
				TIM1_CH1N	
27	PB14	I/O	FC	SPI2_MISO	—
				TIM1_CH2N	
				TIM15_CH1	
				TIM1_CH1	
28	PB15	I/O	FC	SPI2_MOSI	RTC_REFIN
				TIM1_CH3N	
				TIM15_CH1N	
				TIM15_CH2	
29	PA8	I/O	FC	USART1_CK	—
				TIM1_CH1	
				EVENTOUT	
				CRS_SYNC	
				MCO	
				TIM1_CH2	
30	PA9	I/O	FC	USART1_TX	—
				TIM1_CH2	
				TIM15_BKIN	
				MCO	
				TIM1_CH3N	
31	PA10	I/O	FC	USART1_RX	—
				TIM1_CH3	
				TIM17_BKIN	
32	PA11	I/O	FC	USART1_CTS	—
				TIM1_CH4	
				EVENTOUT	

KD32F328CBT6					
LQFP48	Pin name	Pin type	Structure	AF	Add. Func
33	PA12	I/O	FC	USART1_RTS TIM1_ETR EVENTOUT	—
34	PA13 (SWDIO)	I/O	FC	IR_OUT SWDIO	—
35	PF6	I/O	FC	I2C2_SCL	—
36	PF7	I/O	FC	I2C2_SDA	—
37	PA14	I/O	FC	USART2_TX SWCLK	—
38	PA15	I/O	FC	SPI1_NSS USART2_RX EVENTOUT	— — —
39	PB3	I/O	FC	SPI1_SCK EVENTOUT	—
40	PB4	I/O	FC	SPI1_MISO TIM3_CH1 EVENTOUT	—
41	PB5	I/O	FC	SPI1_MOSI I2C1_SMBA TIM16_BKIN TIM3_CH2	—
42	PB6	I/O	FCf	I2C1_SCL USART1_TX TIM16_CH1N	—
43	PB7	I/O	FCf	I2C1_SDA USART1_RX TIM17_CH1N	—
44	BOOT0	I	B	Boot memory selection	
45	PB8	I/O	FCf	I2C1_SCL TIM16_CH1	
46	PB9	I/O	FCf	I2C1_SDA IR_OUT TIM17_CH1 EVENTOUT	
47	VSS	S		Ground	
48	VDD	S		Digital power supply	

Table 4.2 abbreviations used in the pin definition table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input-only pin
	I/O	Input/output pin
I/O structure	FC	Standard 5V I/O
	FCf	Standard 5V I/O, I2C FM+ capable
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	AF	Functions selected through GPIOx_AFR registers
	Add. func	Functions directly selected/enabled through peripheral registers

Table 4.3 PA alternate functions

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0		USART2_CTS						COMP1OUT
PA1	EVENTOUT	USART2_RTS						
PA2	TIM15_CH1	USART2_TX						COMP2OUT
PA3	TIM15_CH2	USART2_RX						
PA4	SPI1_NSS	USART2_CK			TIM14_CH1			
PA5	SPI1_SCK	MCO						
PA6	SPI1_MISO	TIM3_CH1	TIM1_BKIN			TIM16_CH1	EVENTOUT	COMP1OUT
PA7	SPI1_MOSI	TIM3_CH2	TIM1_CH1N		TIM14_CH1	TIM17_CH1	EVENTOUT	COMP2OUT
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	CRS_SYNC		TIM1_CH2	
PA9	TIM15_BKIN	USART1_TX	TIM1_CH2			MCO	TIM1_CH3N	
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3					COMP3OUT
PA11	EVENTOUT	USART1_CTS	TIM1_CH4					COMP1OUT
PA12	EVENTOUT	USART1_RTS	TIM1_ETR					COMP2OUT
PA13	SWDIO	IR_OUT						
PA14	SWCLK	USART2_TX						
PA15	SPI1_NSS	USART2_RX		EVENTOUT				

Table 4.4 PB alternate functions

Pin name	AF0	AF1	AF2	AF3	AF4
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N		
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N		
PB2					
PB3	SPI1_SCK	EVENTOUT			
PB4	SPI1_MISO	TIM3_CH1	EVENTOUT		
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N		
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N		
PB8		I2C1_SCL	TIM16_CH1		
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT	
PB10		I2C2_SCL			
PB11	EVENTOUT	I2C2_SDA			
PB12	SPI2_NSS	EVENTOUT	TIM1_BKIN		
PB13	SPI2_SCK		TIM1_CH1N		
PB14	SPI2_MISO	TIM15_CH1	TIM1_CH2N		TIM1_CH1
PB15	SPI2_MOSI	TIM15_CH2	TIM1_CH3N	TIM15_CH1N	

Table 4.5 PF alternate functions

Pin name	AF0	AF1
PF4	EVENTOUT	COMP3OUT
PF5	EVENTOUT	
PF6	I2C2_SCL	
PF7	I2C2_SDA	

5. Memory mapping

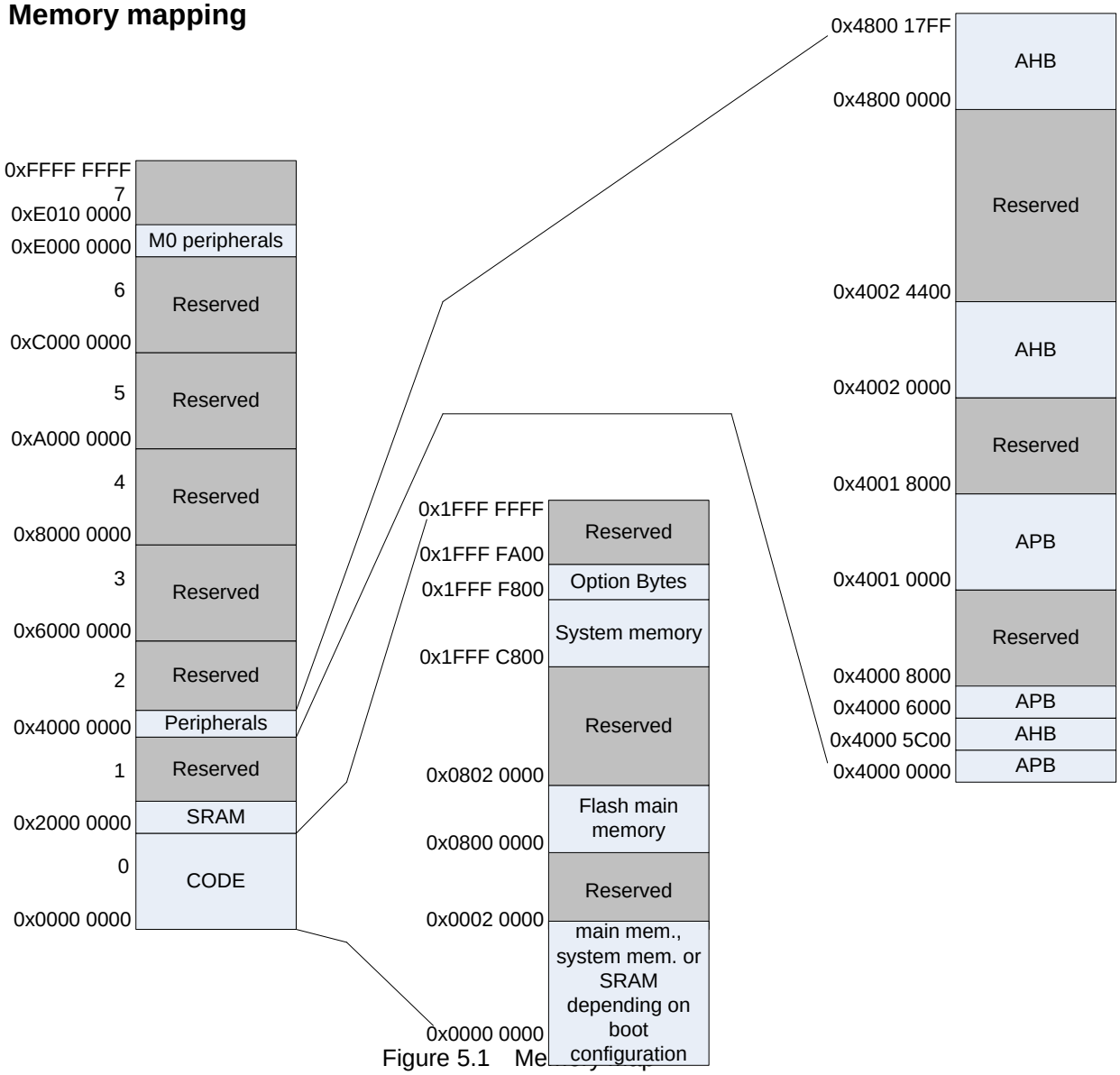


Figure 5.1 Me

1 Row = 2048 bits = 256 Bytes = 64 Words

1 Page = 2 Row = 128 Words

1Sector = 4 Pages = 8 Rows = 2 kbytes

Table 5.1 peripheral register boundary addresses

BUS	Boundary addresses	Size	Peripheral
AHB	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	Reserved

BUS	Boundary addresses	Size	Peripheral
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
	0x4002 3400 - 0x4002 43FF	4 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH Interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
APB	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved
	0x4001 5C00 - 0x4001 7FFF	9 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG+DIV
	0x4000 FC00 - 0x4000 FFFF	1 KB	LEB&FLT
	0x4000 7400 - 0x4000 FBFF	34 KB	Reserved
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6C00 - 0x4000 6FFF	1 KB	CRS
	0x4000 5C00 - 0x4000 6BFF	4 KB	Reserved
APB	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 4800 - 0x4000 53FF	3 KB	Reserved
	0x4000 4400 - 0x4000 47FF	1 KB	USART2

BUS	Boundary addresses	Size	Peripheral
	0x4000 3C00 - 0x4000 43FF	2 KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1400 - 0x4000 1FFF	3 KB	Reserved
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0800 - 0x4000 0FFF	2 KB	Reserved
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	Reserved

6. Electrical characteristics

6.1. Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1. Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are tested at T_A = 25 °C, V_{DD} = 3.3 V. Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production

6.1.2. Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested

6.1.3. Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4. Loading capacitor

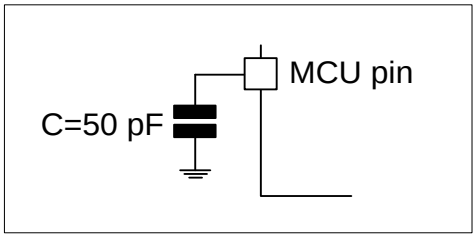


Figure 6.1 Pin loading conditions

6.1.5. Pin input voltage

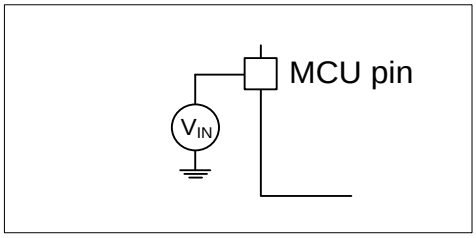


Figure 6.2 Pin input voltage

6.1.6. Power supply scheme

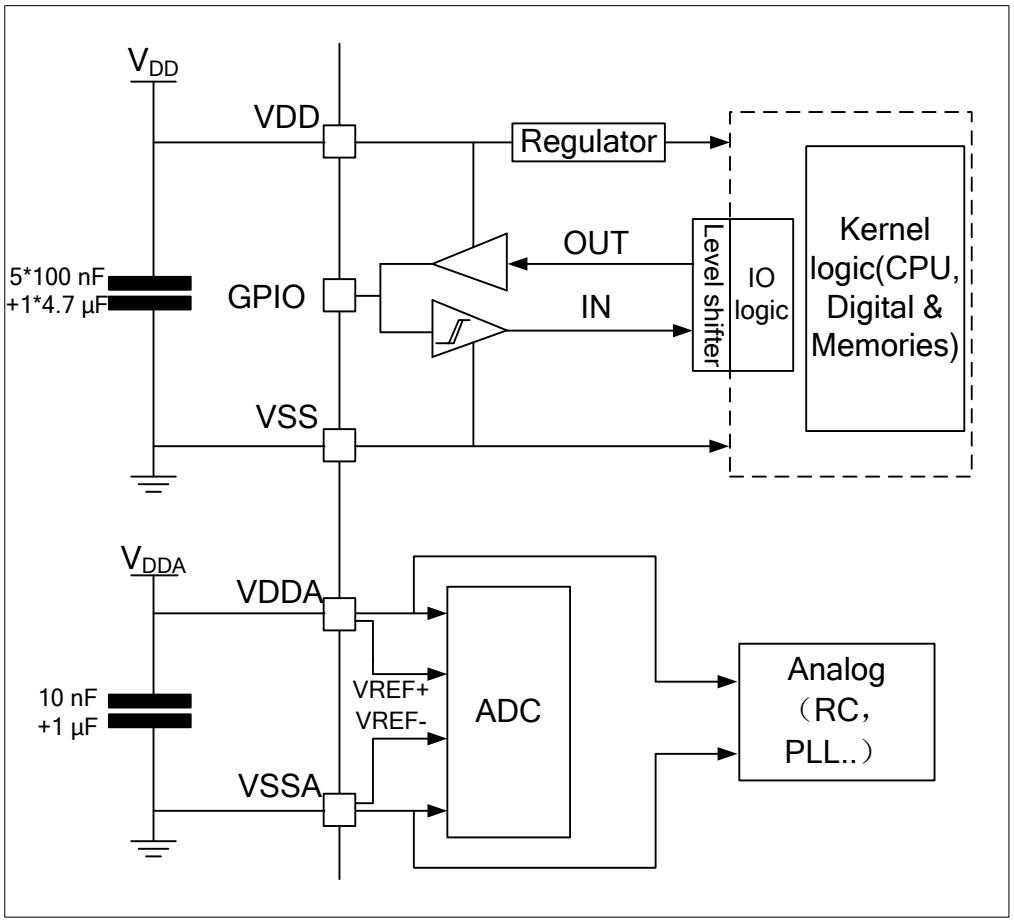


Figure 6.3 Power supply scheme

Note: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA}) must be decoupled with filtering ceramic capacitors as shown above

6.1.7. Current consumption measurement

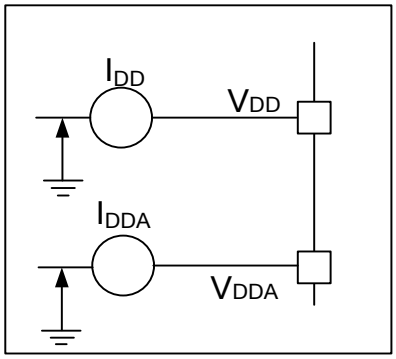


Figure 6.4 Current consumption measurement scheme

6.2. Absolute maximum ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6.1 Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage (1)	-0.3	6.0	V
V_{DDA}-V_{SSA}	External analog supply voltage (1)	-0.3	6.0	V
V_{DD}-V_{DDA}	Allowed voltage difference for V_{DD}-V_{DDA}	0	0	V
V_{IN} (2)	Input voltage on pin	V_{SS} – 0.3	V_{DD} + 0.3	V
$\|\Delta V_{DDx}\|$	Voltage difference between different power supply pins	—	0	mV
$\|V_{SSX}$-$V_{SS}\|$	Voltage difference between different grounding pins	—	0	mV

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to **Table 6.2**: Current characteristics for the maximum allowed injected current values $I_{INJ(PIN)}$.

Table 6.2 Current characteristics

Symbol	Description	Max	Unit
ΣI_{VDD}	Total current into sum of all VDD power lines (source) (1)	120	mA
ΣI_{VSS}	Total current out of sum of all VSS ground lines (sink) (1)	-120	
I_{VDD}	Maximum current into each VDD power pin (source) (1)	100	
I_{VSS}	Maximum current out of each VSS ground pin (sink) (1)	-100	
I_{IO}	Output current sink by any I/O and control pin	26	
	Output current source by any I/O and control pin	-18	
$I_{INJ(PIN)}$ (2) (3)	Injected current on FC and FCf pin	-1/+0	
	Injected current on RST pin	0/+5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) (4)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

2. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded.

3. Negative injection disturbs the analog performance of the device.

4. When several inputs are submitted to a current injection, the maximum$\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents.

Table 6.3 Thermal characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-40 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3. Operating conditions

6.3.1. General operating conditions

Table 6.4 General operating conditions

Symbol	Parameter		Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		—	0	96	MHz
f_{PCLK}	Internal APB clock frequency		—	0	96	MHz
V_{DD}	Standard operating voltage		—	2.0	5.5	V
V_{DDA}	Analog operating voltage	ADC_VREF = VDDA, ADCCLK ≤ 500 kHz	$V_{DDA} = V_{DD}$	2.0	5.5	V
		ADC_VREF = VDDA, ADCCLK ≤ 16 MHz		2.4	5.5	V
		ADC_VREF = Int.2.5V, ADCCLK ≤ 250 kHz		2.7	5.5	V
P_D	Power dissipation at T_A = 85 °C (1)		LQFP64	—	333	mW
			LQFP48	—	370	

Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Ambient temperature	Maximum power dissipation	-40	105	°C
		Low power dissipation (2)	-40	125	
T_J	Junction temperature range	—	-40	125	°C

1. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
2. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}

6.3.2. Operating conditions at power-up / power-down

Table 6.5 Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
T_{VDD}	V_{DD} rise time rate	T_A = 25 °C	0	∞	μs/V
	V_{DD} fall time rate		20	∞	

6.3.3. Embedded reset and power control block characteristics

Table 6.6 Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$ (1)	Power on/power down reset threshold	Falling edge	1.61	1.68	1.75	V
		Rising edge	1.65	1.72	1.79	V
$V_{PDRHYST}$ (2)	PDR hysteresis	—	—	40	—	mV
$t_{RSTTEMPO}$ (2)	Reset temporization	—	—	2.5	—	ms

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.
2. Data based on characterization results, not tested in production.

Table 6.7 Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD0}	PVD threshold 0	PLS[3:0]=0000 (Rising edge)	1.71	1.78	1.85	V
		PLS[3:0]=0000 (Falling edge)	1.61	1.68	1.75	V
V_{PVD1}	PVD threshold 1	PLS[3:0]=0001(Rising edge)	1.81	1.88	1.95	V
		PLS[3:0]=0001 (Falling edge)	1.71	1.78	1.85	V
V_{PVD2}	PVD threshold 2	PLS[3:0]=0010 (Rising edge)	1.90	1.98	2.05	V
		PLS[3:0]=0010 (Falling edge)	1.80	1.88	1.95	V
V_{PVD3}	PVD threshold 3	PLS[3:0]=0011(Rising edge)	2.00	2.08	2.16	V
		PLS[3:0]=0011 (Falling edge)	1.90	1.98	2.06	V
V_{PVD4}	PVD threshold 4	PLS[3:0]=0100 (Rising edge)	2.10	2.18	2.26	V
		PLS[3:0]=0100 (Falling edge)	2.00	2.08	2.16	V
V_{PVD5}	PVD threshold 5	PLS[3:0]=0101(Rising edge)	2.19	2.28	2.37	V
		PLS[3:0]=0101(Falling edge)	2.09	2.18	2.27	V
V_{PVD6}	PVD threshold 6	PLS[3:0]=0110 (Rising edge)	2.29	2.38	2.47	V
		PLS[3:0]=0110 (Falling edge)	2.19	2.28	2.37	V
V_{PVD7}	PVD threshold 7	PLS[3:0]=0111 (Rising edge)	2.38	2.48	2.58	V
		PLS[3:0]=0111(Falling edge)	2.28	2.38	2.48	V
V_{PVD8}	PVD threshold 8	PLS[3:0]=1000(Rising edge)	2.48	2.58	2.68	V
		PLS[3:0]=1000 (Falling edge)	2.38	2.48	2.58	V
V_{PVD9}	PVD threshold 9	PLS[3:0]=1001 (Rising edge)	2.58	2.68	2.78	V
		PLS[3:0]=1001 (Falling edge)	2.48	2.58	2.68	V
V_{PVD10}	PVD threshold 10	PLS[3:0]=1010(Rising edge)	2.67	2.78	2.89	V
		PLS[3:0]=1010 (Falling edge)	2.57	2.68	2.79	V
V_{PVD11}	PVD threshold 11	PLS[3:0]=1011 (Rising edge)	2.77	2.88	2.99	V
		PLS[3:0]=1011 (Falling edge)	2.67	2.78	2.89	V
V_{PVD12}	PVD threshold 12	PLS[3:0]=1100 (Rising edge)	3.49	3.64	3.78	V
		PLS[3:0]=1100 (Falling edge)				
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD13}	PVD threshold 13	PLS[3:0]=1101 (Rising edge)	2.96	3.08	3.20	V
		PLS[3:0]=1101 (Falling edge)	2.86	2.98	3.10	V
V_{PVD14}	PVD threshold 14	PLS[3:0]=1110(Rising edge)	3.80	3.97	4.13	V
		PLS[3:0]=1110 (Falling edge)				
V_{PVD15}	PVD threshold 15	PLS[3:0]=1111 (Rising edge)	3.15	3.28	3.41	V
		PLS[3:0]=1111 (Falling edge)	3.05	3.18	3.31	V
$V_{PVDhyst}$	PVD hysteresis	—	—	100	—	mV

6.3.4. Embedded reference voltage

The parameters given in **Table 6.8** are derived from tests performed under the ambient temperature and supply voltage conditions summarized in **Table 6.4**.

Table 6.8 Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40 – 105 °C	1.205	1.217	1.229	V
t_{START}	ADC_IN17 buffer startup time	—	—	400(1)	—	μs
$t_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	—	4(1)	—	—	μs
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DDA} = 3.0V	—	11(1)	—	mV
T_{Coeff}	Temperature coefficient	-40 – 105 °C	—	±100(1)	—	ppm/°C

1. Guaranteed by design, not tested in production

Table 6.9 ADC reference voltage

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{ADCREF}	ADC internal reference voltage (0.625V)	V_{DDA}≥2.4V (-40 – 105 °C)	0.616	0.625	0.634	V
	ADC internal reference voltage (1.5V)	V_{DDA}≥2.4V (-40 – 105 °C)	1.476	1.5	1.524	
	ADC internal reference voltage (2.5V)	V_{DDA}≥2.7V (-40 – 105 °C)	2.458	2.5	2.543	

1. Guaranteed by design, not tested in production

6.3.5. Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in **Figure 6.4**.

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency:

  0 wait state and Prefetch OFF from 0 to 24 MHz;

  1 wait state and Prefetch ON from 24 MHz to 48 MHz;

  2 wait state and Prefetch ON above 48 MHz.
- When the peripherals are enabled $f_{PCLK} = f_{HCL}$

Table 6.10 Typical current consumption at V_{DD} = 5V

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled			All peripherals disabled			Unit
				Typ@T_A(1)			Typ@T_A(1)			
				25 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, code executing from Flash	HSI48	48 MHz	11.45	11.57	11.62	5.92	6.24	6.18	mA
		HSE bypass PLL ON	96 MHz	20.00	20.17	20.16	9.97	10.07	10.14	
			72 MHz	15.18	15.36	15.32	7.59	7.67	7.76	
			48 MHz	11.25	11.40	11.29	5.63	5.66	5.78	
			36 MHz	8.50	8.69	8.68	4.33	4.39	4.40	
			24 MHz	6.14	6.18	6.25	3.43	3.51	3.57	
			16 MHz	3.88	3.97	4.07	2.66	2.45	2.49	
		HSE bypass PLL OFF	8 MHz	2.24	2.33	2.42	1.41	1.54	1.56	
			1 MHz	0.42	0.45	0.50	0.31	0.35	0.39	
		HSI PLL ON	96 MHz	20.27	20.82	20.94	9.98	10.33	10.44	
			72 MHz	15.46	15.88	15.86	7.69	7.98	8.01	
			48 MHz	10.77	11.10	11.13	6.00	6.30	6.37	
			36 MHz	8.77	9.11	9.15	4.52	4.72	4.73	
			24 MHz	6.02	6.30	6.37	3.64	3.85	3.95	
			16 MHz	4.22	4.45	4.49	2.58	2.78	2.86	
		HSI14	14 MHz	3.55	3.67	3.77	2.26	2.43	2.49	
		HSI	8 MHz	2.43	2.64	2.68	1.43	1.58	1.60	

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled			All peripherals disabled			Unit
				Typ@T_A(1)			Typ@T_A(1)			
				25 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, code executing from SRAM	HSI48	48 MHz	13.32	13.57	13.47	7.41	7.57	7.47	mA
		HSE bypass PLL ON	96 MHz	24.17	24.28	24.12	14.53	14.44	14.47	
			72 MHz	18.38	18.33	18.19	10.96	10.95	10.87	
			48 MHz	12.39	12.31	12.47	7.39	7.34	7.30	
			36 MHz	9.36	9.31	9.34	5.52	5.52	5.53	
			24 MHz	6.26	6.29	6.32	3.68	3.64	3.70	
			16 MHz	4.19	4.20	4.23	2.60	2.40	2.44	
		HSE bypass PLL OFF	8 MHz	2.23	2.33	2.36	1.33	1.44	1.49	
			1 MHz	0.42	0.45	0.49	0.30	0.34	0.38	
		HSI PLL ON	96 MHz	24.61	24.81	24.88	14.70	14.78	14.93	
			72 MHz	18.76	19.02	19.08	11.15	11.35	11.21	
			48 MHz	12.77	13.05	13.10	7.46	7.64	7.68	
			36 MHz	9.65	9.85	9.87	5.74	5.85	5.86	
			24 MHz	6.59	6.74	6.76	3.86	3.96	4.03	
			16 MHz	4.55	4.71	4.79	2.60	2.73	2.76	
		HSI14	14 MHz	3.81	3.95	3.96	2.26	2.33	2.36	
		HSI	8 MHz	2.35	2.47	2.50	1.39	1.50	1.52	
I_{DD}	Supply current in Sleep mode	HSI48	48 MHz	7.55	8.89	8.84	2.59	2.71	2.76	mA
		HSE bypass PLL ON	96 MHz	15.24	15.42	15.44	4.93	4.97	5.01	
			72 MHz	11.47	11.62	11.70	3.69	3.68	3.76	
			48 MHz	7.69	7.77	7.77	2.46	2.46	2.49	
			36 MHz	5.77	5.82	5.94	1.83	1.83	1.88	
			24 MHz	3.88	3.88	3.95	1.22	1.33	1.36	
			16 MHz	2.57	2.58	2.61				
		HSE bypass PLL OFF	8 MHz	1.38	1.48	1.54	0.54	0.57	0.62	
			1 MHz	0.31	0.34	0.39	0.19	0.22	0.27	
		HSI PLL ON	96 MHz	15.49	15.72	15.90	5.09	5.26	5.33	
			72 MHz	11.72	12.03	12.29	3.84	4.01	4.04	
			48 MHz	7.98	8.32	8.37	2.63	2.76	2.82	
			36 MHz	6.06	6.31	6.35	1.99	2.12	2.16	
			24 MHz	4.16	4.32	4.33	1.38	1.50	1.53	
			16 MHz	2.84	3.04	3.04	0.96	1.06	1.11	
		HSI14	14 MHz	2.36	2.46	2.51	0.81	0.90	0.93	
		HSI	8 MHz	1.51	1.66	1.70	0.57	0.66	0.70	

1. Data based on characterization results, not tested in production.

Table 6.11 Typical current consumption from the VDDA supply (1)

Symbol	Parameter	Conditions	f_{HCLK}	V_{DDA}=2.0 V			V_{DDA}=5.5 V			Unit
				Typ@T_A (2)			Typ@T_A (2)			
				25 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run or Sleep mode, code executing from Flash memory or SRAM	HSI48	48 MHz	343	360	367	350	367	373	μA
		HSE bypass PLL ON	96 MHz	549	573	583	558	583	592	
			72 MHz	467	487	494	476	496	501	
			48 MHz	377	392	398	385	400	405	
			36 MHz	331	340	345	339	350	353	
			24 MHz	285	295	301	293	305	308	
			16 MHz	251	265	272	259	274	278	
		HSE bypass PLL OFF	8 MHz	49	59	60	55	65	67	
			1 MHz	49	58	60	54	64	66	
		HSI PLL ON	96 MHz	624	656	669	639	671	683	
			72 MHz	542	569	578	556	583	592	
			48 MHz	451	473	482	466	487	496	
			36 MHz	405	421	428	420	435	443	
			24 MHz	359	375	383	374	389	397	
			16 MHz	325	345	353	339	359	368	
		HSI14	14 MHz	111	122	126	117	128	132	
		HSI	8 MHz	123	136	141	135	149	154	

1. Current consumption from the V_{DDA} supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash memory or SRAM. I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production.

Table 6.12 Typical RTC current consumption

Symbol	Parameter	Conditions		Typ@ (V_{DD} = V_{DDA}) (1)			Unit
				2.0 V	3.3 V	5.5 V	
I_{DD}	RTC current	RTC & LSE ON	LSEDRV[1:0]=00	0.7	0.9	1.7	μA
			LSEDRV[1:0]=01	0.9	1.1	1.9	
			LSEDRV[1:0]=10	0.8	1.0	1.8	
			LSEDRV[1:0]=11	1.0	1.2	2.0	
I_{DD}+ I_{DDA}		RTC & LSI ON		1.1	1.5	2.0	

1. Data based on characterization results, not tested in production.

Table 6.13 Typical current consumption in Stop and Standby modes

Symbol	Parame-ter	Conditions		Typ@ (V_{DD} = V_{DDA})(1)									Unit
				T_A = 25 °C			T_A = 85 °C			T_A = 105 °C			
				2.0 V	3.3 V	5.5 V	2.0 V	3.3 V	5.5 V	2.0 V	3.3 V	5.5 V	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF		11.03	11.69	12.40	18.82	19.37	20.33	27.82	28.06	30.29	μA
		Regulator in low-power mode, all oscillators OFF		2.85	3.12	3.64	8.56	8.82	9.86	16.71	16.40	18.66	
	Supply current in Standby mode	LSI ON and IWDG ON		0.57	1.02	1.81	0.84	1.32	2.42	1.18	1.81	3.09	
		LSI OFF and IWDG OFF		0.28	0.55	1.00	0.55	0.84	1.56	0.90	1.30	2.23	
I_{DDA}	Supply current in Stop mode	VDDA monitoring ON	Regulator in run mode, all oscillators OFF	1.36	1.65	2.20	1.69	2.03	2.73	1.85	2.25	3.07	
			Regulator in low-power mode, all oscillators OFF	1.38	1.64	2.19	1.70	2.03	2.74	1.86	2.23	3.04	
	Supply current in Standby mode		LSI ON and IWDG ON	1.97	2.27	2.85	2.30	2.64	3.40	2.42	2.88	3.71	
			LSI OFF and IWDG OFF	1.27	1.57	2.09	1.56	1.95	2.64	1.77	2.13	2.95	
I_{DDA}	Supply current in Stop mode	VDDA monitoring OFF	Regulator in run mode, all oscillators OFF	0.88	0.91	1.03	1.06	1.13	1.32	1.17	1.28	1.49	
			Regulator in low-power mode, all oscillators OFF	0.88	0.90	1.03	1.07	1.11	1.31	1.17	1.28	1.50	
	Supply current in Standby mode		LSI ON and IWDG ON	1.46	1.53	1.68	1.66	1.73	1.95	1.76	1.90	2.15	
			LSI OFF and IWDG OFF	0.78	0.81	0.92	0.98	1.01	1.20	1.10	1.13	1.40	

1. Data based on characterization results, not tested in production

Typical current consumption

The MCU is placed under the following conditions

- V_{DD}=V_{DDA}=3.3 V
- All I/O pins are in analog input configuration
- The Flash memory access time is adjusted to the f_{HCLK} frequency:

  0 wait state and Prefetch OFF from 0 to 24 MHz;

  1 wait state and Prefetch ON from 24 MHz to 48 MHz;

  2 wait state and Prefetch ON above 48 MHz.
- When the peripherals are enabled f_{PCLK} = f_{HCLK}
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8, 16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz, 125kHz respectively

Table 6.14 Typical current consumption, code executing from Flash memory, running from HSE 8 MHz

Symbol	Parameter	f_{HCLK}	Run mode (Typ@ 25 °C)		Sleep mode (Typ@ 25 °C)		Unit
			Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	
I_{DD}	Current consumption from VDD supply	96 MHz	18.57	9.04	14.35	4.35	mA
		72 MHz	14.16	6.83	10.90	3.39	
		48 MHz	9.98	5.28	7.42	2.42	
		36 MHz	8.18	3.85	5.69	1.87	
		32 MHz	7.10	4.04	5.11	1.78	
		24 MHz	5.75	3.56	3.99	1.40	
		16 MHz	4.19	2.26	2.89	1.18	
		8 MHz	2.18	1.40	1.41	0.55	
		4 MHz	1.17	0.82	0.78	0.40	
		2 MHz	0.71	0.53	0.54	0.33	
		1 MHz	0.48	0.39	0.39	0.29	
		500 kHz	0.38	0.32	0.32	0.27	
		125 kHz	0.28	0.27	0.27	0.25	
I_{DDA}	Current consumption from VDDA supply	96 MHz	554				μA
		72 MHz	471				
		48 MHz	380				
		36 MHz	334				
		32 MHz	323				
		24 MHz	290				
		16 MHz	256				
		8 MHz	50				
		4 MHz	50				
		2 MHz	50				

		1 MHz	50	
		500 kHz	50	
		125 kHz	50	

On-chip peripheral current consumption

The MCU is placed under the following conditions：

- All I/O pins are in analog input configuration
- All peripherals are disabled except when explicitly mentioned
- The given value is calculated by measuring the current consumption : 1.with all peripherals clocked off 2. with only one peripheral clocked on
- the ambient temperature and supply voltage conditions summarized in Table 6.4 General operating conditions

Table 6.15 Peripheral current consumption

Peripheral		Typ @25 °C	Unit
AHB	Busmatrix(1)	2.2	μA/MHz
	CRC	1.4	
	DMA	25.5	
	FLASH interface	6.6	
	GPIOA	9.0	
	GPIOB	8.9	
	GPIOC	8.8	
	GPIOD	8.1	
	GPIOF	8.3	
	SRAM	0.8	
APB	APB-Bridge(2)	2.8	
	ADC	3.0	
	CRS	2.8	
	DBG	7.7	
	I2C1	11.4	
	I2C2	19.4	
	SPI1	3.4	
	SPI2	10.7	
	PWR	2.5	
	USART1	22.3	
	USART2	12.8	
	SYSCFG	2.8	
	TIM1	10.6	
	TIM3	8.5	
	TIM6	3.9	
	TIM14	3.7	
	TIM15	13.1	

Peripheral		Typ @25 °C	Unit
	TIM16	11.6	
	TIM17	11.5	
	WWDG	2.7	
	IWDG	14.8	
APB	LEB	8.9	μA/MHz

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. The APB Bridge is automatically active when at least one peripheral is ON on the Bus.

6.3.6. Wakeup time from low-power mode

Table 6.16 Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ@ (V_{DD}=V_{DDA})	Unit
			3.3 V	
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	10	μs
		Regulator in low power mode	10	
$t_{WUSTANDBY}$	Wakeup from Standby mode	—	40	
$t_{WUSLEEP}$	Wakeup from Sleep mode	—	4 SYSCLK cycles	

1. Data based on design values, not tested in production

6.3.7. External clock source characteristics

High-speed external user clock generated from an external source

The given value is tested by High-speed external clock, the ambient temperature and supply voltage conditions summarized in **Table 6.4**.

Table 6.17 High-speed external user clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	4	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	0.7 V_{DD}	—	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage	V_{SS}	—	0.3 V_{DD}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	—	15	—	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time	—	20	—	

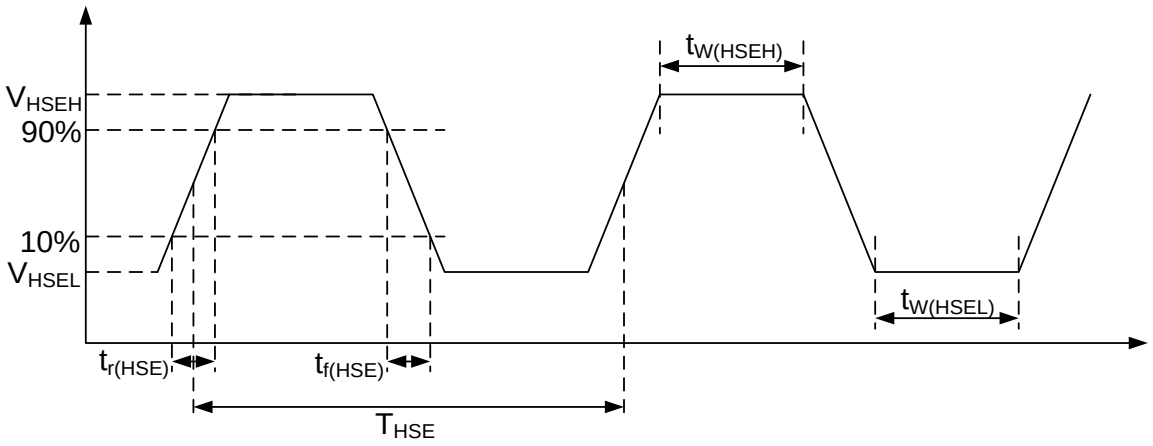


Figure 6.5 High-speed external clock source AC timing diagram

Low-speed external user clock generated from an external source

Table 6.18 Low-speed external user clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	—	32.768	1000	kHz
V_{LSEH}	OSC_IN input pin high level voltage	0.7 V_{DD}	—	V_{DD}	V
V_{LSEL}	OSC_IN input pin low level voltage	V_{SS}	—	0.3 V_{DD}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC_IN high or low time	—	450	—	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC_IN rise or fall time	—	50	—	

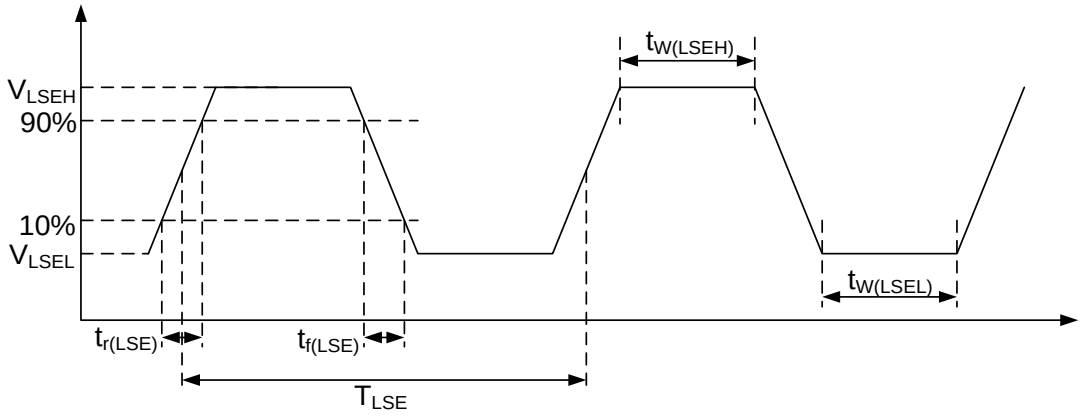


Figure 6.6 Low-speed external clock source AC timing diagram

High-speed external clock generated from a crystal/ceramic resonator

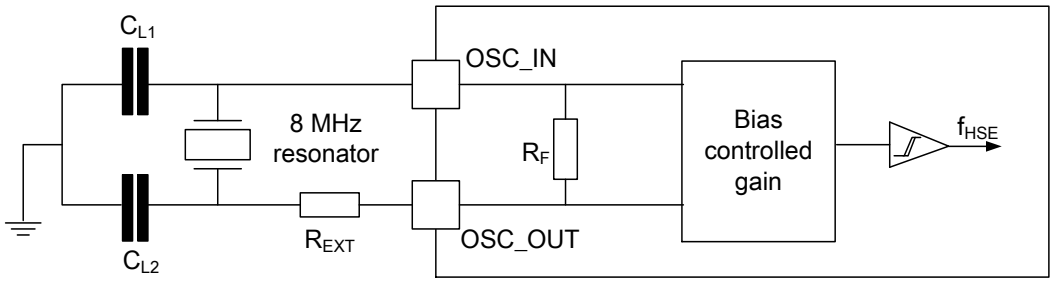
The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 6.19 HSE oscillator characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
f_{OSC_IN}	Oscillator frequency	—	4	8	32	MHz
R_F	Feedback resistor	—	—	3.6	—	MΩ
I_{DD}	HSE current consumption	V_{DD}=3.3 V, R_M=30 Ω CL=10pF@8 MHz	—	0.2	—	mA
		V_{DD}=3.3 V, R_M=45 Ω CL=10pF@8 MHz	—	0.2	—	
		V_{DD}=3.3 V, R_M=30 Ω CL=5pF@32 MHz	—	0.3	—	
		V_{DD}=3.3 V, R_M=30 Ω CL=10pF@32 MHz	—	0.3	—	
		V_{DD}=3.3 V, R_M=30 Ω CL=20pF@32 MHz	—	0.5	—	
g_m	Oscillator transconductance	Startup	10	—	—	mA/V
$t_{SU(HSE)}$(2)	Startup time	VDD is stabilized	—	2	—	ms

1. Data based on characterization results, not tested in production

2. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer



R_{EXT} value depends on the crystal characteristics

Figure 6.7 Typical application with an 8 MHz crystal

For CL1 and CL2, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. CL1 and CL2 are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing CL1 and CL2.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 6.20 LSE oscillator characteristics (f_{LSE}=32.768 kHz)

Symbol	Parameter	Conditions	Typ@ (V_{DD} = V_{DDA}) (1)		Unit
			3.3V	5.5V	
I_{DD}	LSE current consumption	LSEDRV[1:0]=00	0.8	1.5	μA
		LSEDRV[1:0]=01	1.0	1.7	
		LSEDRV[1:0]=10	0.9	1.6	
		LSEDRV[1:0]=11	1.2	1.9	
g_m	Oscillator transconductance	LSEDRV[1:0]=00	5		μA/V
		LSEDRV[1:0]=01	11		
		LSEDRV[1:0]=10	8		
		LSEDRV[1:0]=11	15		
$t_{SU(LSE)}$ (2)	Startup time	V_{DD} is stabilized	2		s

1. Data based on characterization results, not tested in production

2. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768kHz LSE is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

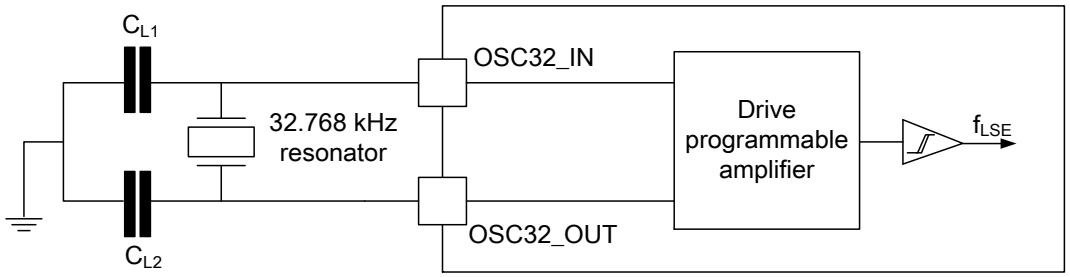


Figure 6.8 Typical application with a 32.768 kHz crystal

For CL1 and CL2, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (Typ.), designed for low-frequency applications, and selected to match the requirements of the crystal or resonator. CL1 and CL2 are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing CL1 and CL2.

6.3.8. Internal clock source characteristics

High-speed internal (HSI) RC oscillator

The given value is at the ambient temperature and supply voltage conditions summarized in **Table 6.4**.

Table 6.21 HSI oscillator characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
f_{HSI}	Frequency	—	—	8	—	MHz
TRIM	HSI user trimming step	—	—	0.5	—	%
Duty	Duty cycle	—	45	—	55	%
ACC	Accuracy of the HSI oscillator	-40 – 105 °C	—	±3.5	—	%
		25 °C	—	±1.0	—	
$t_{SU(HSI)}$	HSI oscillator startup time	—	—	5	—	μs
$I_{DDA(HSI)}$	HSI oscillator power consumption	—	—	100	—	μA

1. Data based on characterization results, not tested in production

High-speed internal 14 MHz (HSI14) RC oscillator

Table 6.22 HSI14 oscillator characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
f_{HSI14}	Frequency	—	—	14	—	MHz
TRIM	HSI14 user trimming step	—	—	0.39	—	%
Duty	Duty cycle	—	45	—	55	%
ACC	Accuracy of the HSI14 oscillator	-40 – 105 °C	-4.2	—	5.1	%
		25 °C	—	±1.0	—	
$t_{SU(HSI14)}$	HSI14 oscillator startup time	—	—	2	—	μs
$I_{DDA(HSI14)}$	HSI14 oscillator power consumption	—	—	65	—	μA

1. Data based on characterization results, not tested in production

High-speed internal 48 MHz (HSI48) RC oscillator

Table 6.23 HSI48 oscillator characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
f_{HSI48}	Frequency	—	—	48	—	MHz
TRIM	HSI48 user trimming step	—	—	0.14	—	%
Duty	Duty cycle	—	45	—	55	%
ACC	Accuracy of the HSI48 oscillator	-40 – 105 °C	—	±4.8	—	%
		25 °C	—	±1.0	—	
$t_{SU(HSI48)}$	HSI48 oscillator startup time	—	—	16	—	μs
$I_{DDA(HSI48)}$	HSI48 oscillator power consumption	—	—	330	—	μA

1. Data based on characterization results, not tested in production

Low-speed internal (LSI) RC oscillator

Table 6.24 LSI oscillator characteristics

Symbol	Parameter	Min(1)	Typ(1)	Max(1)	Unit
f_{LSI}	Frequency	36.4	40	43.6	kHz
$t_{SU(LSI)}$(1)	LSI oscillator startup time	—	19	48	μs
$I_{DDA(LSI)}$(1)	LSI oscillator power consumption	—	0.6	1.1	μA

1. Data based on characterization results, not tested in production

6.3.9. PLL characteristics

The given value is at the ambient temperature and supply voltage conditions summarized in **Table 6.4**.

Tabel 6.25 PLL characteristics

Symbol	Parameter	Min(1)	Typ(1)	Max(1)	Unit
f_{PLL_IN}	PLL input clock	0.8	8	24	MHz
	PLL input clock duty cycle	40	—	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	—	96	MHz
t_{LOCK}	PLL lock time	—	—	200	μs
$Jitter_{PLL}$	Cycle-to-cycle jitter	—	—	300	ps

1. Data based on characterization results, not tested in production

6.3.10. Memory characteristics

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 6.26 Flash memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
tprog	32bit programming time	T_A = -40 – 105 °C	—	25	—	μs
t_{ERASE}	Page(0.5 KB) erase time	T_A = -40 – 105 °C	—	2	—	ms
t_{ME}	Mass erase time	T_A = -40 – 105 °C	—	8	—	ms
I_{DD}	Supply current	Write mode	—	—	10	mA
		Erase mode	—	—	12	mA

1. Data based on characterization results, not tested in production

Table 6.27 Flash endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = -40 – 105 °C	100	kcycle
t_{RET}	Data retention	T_A = 85 °C (2), 1 kcycle	20	year
		T_A = 105 °C (2), 1 kcycle	10	

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.11. EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} as well as V_{DDA} and V_{SSA} through a 1μF capacitor (a total of 1μF*4), until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

Table 6.28 EMS characteristic

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD}=5.0 V, T_A=25 °C, f_{HCLK}=96MHz, conforming to IEC 61000-4-2	—
V_{EFTB}	Fast transient voltage burst limits to be applied through 1μF on V_{DD} and V_{SS} as well as V_{DDA} and V_{SSA} pins (a total of 1μF*4) to induce a functional disturbance	V_{DD}=5.0 V, T_A=25 °C, f_{HCLK}=96MHz, conforming to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.
Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with SAE-J1752/3 standard which specifies the test board and the pin loading.

Table 6.29 EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max(f_{HSE}/f_{HCLK}) 8/48 MHz	Unit
SEMI	Peak level	VDD=3.6 V T_A=25 °C compliant with SAE-J1752/3	0.1~30 MHz	-8	dBμV
			30~130 MHz	—	
			130 MHz~1 GHz	-6	
			EMILevel	Class B	—

6.3.12. Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device. This test conforms to the MIL-STD-883 / JESD22-C101 standard.

Table 6.30 ESD characteristics

Symbol	Parameter	Conditions	Packages	Class	Min(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C, conforming to MIL-STD-883	All	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to JESD22-C101	All	C3	1000	V

1. Data based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required to assess the latch-up performance：

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78 IC latch-up standard.

Table 6.31 Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = 25 °C, conforming to JESD78	I level A

6.3.13. I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below VSS or above VDD (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

- **Functional susceptibility to I/O current injection**

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins or other functional failure (for example reset occurrence or oscillator frequency deviation).

Table 6.32 I/Ocurrent injection susceptibility

Symbol	Description	Function		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0 pins	0	NA	mA
	Injected current on PA11, PA12 pin	-5	NA	
	Injected current on NRST pin	0	+5	
	Injected current on all other pins	-1	NA	

6.3.14. I/O port characteristics

- **General input/output characteristics**

Unless otherwise specified, the parameters given in **Table 6.33** are derived from tests performed under the conditions summarized in **Table 6.4**. All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Table 6.33 I/O static characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
V_{IL}	Low level input voltage	FC and FCf I/O	—	—	0.3 V_{DD}	V
		BOOT0	—	—	0.3 V_{DD} -0.3	
V_{IH}	High level input voltage	FC and FCf I/O	0.7V_{DD}	—	—	V
		BOOT0	0.2V_{DD} +0.95	—	—	
V_{hys}	I/O Schmitt trigger hysteresis	FC and FCf I/O	—	100	—	mV
		BOOT0	—	300	—	
I_{IKg}	Input leakage current (2)	FC and FCf I/O in digital mode $V_{SS}\leq V_{IN}\leq V_{DD}$	—	—	±0.1	μA
R_{PU}	Weak pull-up equivalent resistor (3)	$V_{IN}= V_{SS}$	—	40	—	kΩ
R_{PD}	Weak pull-down equivalent resistor (3)	$V_{IN}=V_{DD}$	—	40	—	kΩ
C_{IO}	I/O pin capacitance	—	—	5	—	pF

1. Data based on design simulation only. Not tested in production
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins.
3. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

- **Output driving current**

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed VOL/VOH).In the user application, the number of I/O pins which can drive current must

be limited to respect the absolute maximum rating specified in **Section 6.2**:

- The sum of the currents sourced by all the I/Os on VDDIOx, plus the maximum consumption of the MCU sourced on VDD, cannot exceed the absolute maximum rating I_{VDD} (see **Table 6.2**)
- The sum of the currents sunk by all the I/Os on VSS, plus the maximum consumption of the MCU sunk on VSS, cannot exceed the absolute maximum rating I_{VDD} (see **Table 6.2**)

- **Output voltage levels**

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in **Table 6.4**. All I/Os are CMOS- and TTL-compliant.

Table 6.34 Output voltage characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O	$\|I_{IO}\|$ = 8 mA, V_{DD} ≥ 2.7 V	—	0.2	V
V_{OH}	Output high level voltage for an I/O		V_{DD} – 0.4	—	
V_{OL} (2)	Output low level voltage for an I/O	$\|I_{IO}\|$ = 20 mA, V_{DD} ≥ 2.7 V	—	0.8	V
V_{OH} (2)	Output high level voltage for an I/O		V_{DD} – 1.1	—	
V_{OL} (2)	Output low level voltage for an I/O	$\|I_{IO}\|$ = 6 mA	—	0.2	V
V_{OH} (2)	Output high level voltage for an I/O		V_{DD} – 0.2	—	
V_{OLFm+} (2)	Output low level voltage for an FCf I/O pin in FM mode	$\|I_{IO}\|$ = 20 mA, V_{DD} ≥ 2.7 V	—	0.7	V
		$\|I_{IO}\|$ = 10 mA	—	0.3	V

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings.
2. Data based on characterization results. Not tested in production.

- **Input/output AC characteristics**

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in **Table 6.4**.

Table 6.35 I/O AC characteristics [1] [2]

OSPEEDy[1:0]	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency [3]	CL = 50 pF, V_{DD} ≥ 2.0 V	—	2	MHz
	$t_{f(IO)out}$	Output fall time		—	125	ns
	$t_{r(IO)out}$	Output rise time		—	125	
01	$f_{max(IO)out}$	Maximum frequency [3]	CL = 50 pF, V_{DD} ≥ 2.0 V	—	10	MHz
	$t_{f(IO)out}$	Output fall time		—	25	ns
	$t_{r(IO)out}$	Output rise time		—	25	
11	$f_{max(IO)out}$	Maximum frequency [3] Output fall time	CL = 30 pF, V_{DD} ≥ 2.7 V	—	50	MHz
			CL = 50 pF, V_{DD} ≥ 2.7 V	—	30	
			CL = 50 pF, 2.0 V ≤V_{DD} < 2.7 V	—	20	
	$t_{f(IO)out}$	Maximum frequency [3] Output fall time	CL = 30 pF, V_{DD} ≥ 2.7 V	—	5	ns
			CL = 50 pF, V_{DD} ≥ 2.7 V	—	8	
			CL = 50 pF, 2.0 V ≤V_{DD} < 2.7 V	—	12	
	$t_{r(IO)out}$	Maximum frequency [3]	CL = 30 pF, V_{DD} ≥ 2.7 V	—	5	ns
			CL = 50 pF, V_{DD} ≥ 2.7 V	—	8	
			CL = 50 pF, 2.0 V ≤V_{DD} < 2.7 V	—	12	
Fm+ configuration[4]	$f_{max(IO)out}$	Maximum frequency [3]	CL = 50 pF, V_{DD} ≥ 2.0 V	—	2	MHz
	$t_{f(IO)out}$	Output fall time		—	12	ns
	$t_{r(IO)out}$	Output rise time		—	34	
—	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	—	20	—	ns

1. The I/O speed is configured using the SPEEDy [1:0], Refer to the reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design, not tested in production
3. The maximum frequency is defined in **Figure 6.9**.
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the reference manual for a detailed description of Fm+ I/O configuration.

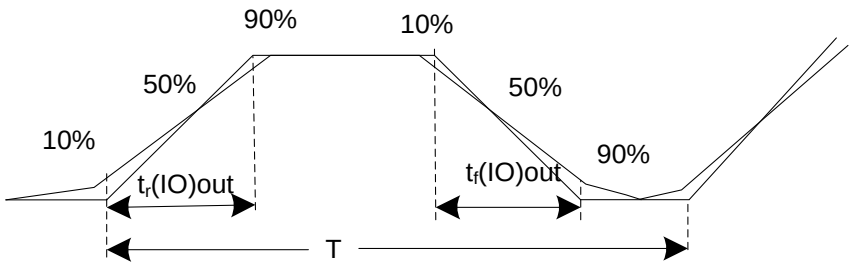


Figure 6.9 I/O AC characteristics definition

Maximum frequency is achieved if $(t_r + t_f) \leq \frac{2}{3}T$ and if the duty cycle is (45 ~ 55%) when loaded by 50 pF

6.3.15. NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, RPU. Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in **Table 6.4**.

Table 6.36 NRST pin characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
$V_{IL(NRST)}$	NRST input low level voltage	—	—	—	0.3 V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage	—	0.7 V_{DD}	—	—	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	—	—	200	—	mV
R_{PU}	Weak pull-up equivalent resistor	—	—	4.3	—	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	—	—	160	—	ns
$V_{NF(NRST)}$	NRS Tinput not filtered pulse	—	500	—	—	

1. Data based on design simulation only. Not tested in production.

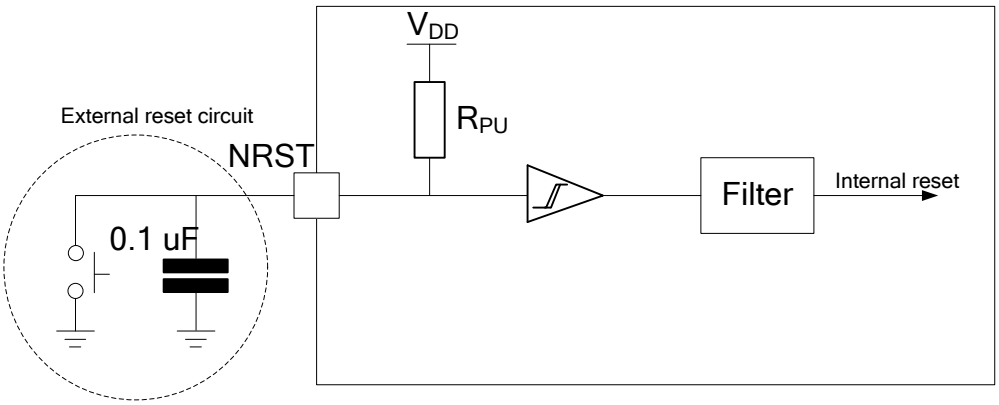


Figure 6.10 Recommended NRST pin protection

1. The external capacitor protects the device against parasitic resets.

2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in **Table 6.36**. Otherwise the reset will not be taken into account by the device.

6.3.16. 12-bit ADC characteristics

Unless otherwise specified, the parameters given in **Table 6.37** are derived from tests performed under the conditions summarized in **Table 6.4**.

Note: It is recommended to perform a calibration after each power-up.

Table 6.37 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON	ADC_VREF = VDDA, ADCCLK ≤ 500 kHz	2.0	—	5.5	V
		ADC_VREF = VDDA, ADCCLK ≤ 16 MHz	2.4	—	5.5	V
		ADC_VREF = Int.2.5 V, ADCCLK ≤ 250 kHz	2.7	—	5.5	V
$I_{DDA(ADC)}$	Current consumption of the ADC (1)	V_{DD} = V_{DDA} = 3.3 V	—	0.8	—	mA
f_{ADC}	ADC clock frequency	ADC_VREF = Internal reference voltage	—	—	250	kHz
		—	—	14	—	MHz
f_S (2)	Sampling rate	—	—	1	—	MHz
f_{TRIG} (2)	External trigger frequency	f_{ADC} = 14 MHz	—	—	823	kHz
		—	—	—	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	—	0	—	V_{REF+}	V
R_{AIN} (2)	External input impedance	—	—	—	50	kΩ
R_{ADC} (2)	Sampling switch resistance	—	—	1	—	kΩ
C_{ADC} (2)	Internal sample and hold capacitor	—	—	3	—	pF
t_{CAL} (2)(3)	Calibration time	f_{ADC} = 14 MHz	8.4			μs
		—	117			$1/f_{ADC}$
$W_{LATENCY}$ (2)(4)	ADC_DR register ready latency	—	2	—	3	$1/f_{PCLK}$
t_{latr} (2)	Trigger conversion latency	—	2	—	3	$1/f_{ADC}$
$Jitter_{ADC}$	ADC jitter on trigger conversion	—	—	1	—	$1/f_{ADC}$
t_S (2)	Sampling time	f_{ADC} = 14 MHz	0.107	—	17.1	μs
		—	1.5	—	239.5	$1/f_{ADC}$
t_{STAB} (2)	Stabilization time	—	20			$1/f_{ADC}$
t_{CONV} (2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz 12-bit resolution	1	—	18	μs
		12-bit resolution	14 to 252 (t_S+12.5)			$1/f_{ADC}$

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 μA on IDDA and 60 μA on IDD should be taken into account
2. Guaranteed by design, not tested in production
3. Specified value includes only ADC timing. It does not include the latency of the register access
4. This parameter specify latency for transfer of the conversion result to the ADC_DR register. EOC flag is set at this time.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 6.38 R_{AIN} max for f_{ADC} = 14 MHz

T_S (cycles)	t_S (μs)	R_{AIN} max (kΩ)(1)
1.5	0.11	2.7
7.5	0.54	17.4
13.5	0.96	32.1
28.5	2.04	NA
41.5	2.96	NA
55.5	3.96	NA
71.5	5.11	NA
239.5	17.1	NA

1. Guaranteed by design, not tested in production

Table 6.39 ADC accuracy (1)(2)(3)

Symbol	Parameter	Test conditions		Typ	Max(4)	Unit
ET	Total unadjusted error			±4	—	LSB
EO	Offset error	F_{HCLK} = 8 MHz V_{DD} = V_{DDA} = 5 V, ADC_VREF=V_{DDA} R_{AIN} < 10 kΩ T_A = 25 °C		±1.5	—	
EG	Gain error			±1.5	—	
ED	Differential linearity error	F_{HCLK} = 8 MHz, V_{DD} = V_{DDA} = 5 V R_{AIN} < 10 kΩ T_A = 25 °C	ADCVref = V_{DDA} f_{ADC} = 14 MHz	±1	—	
EL	Integral linearity error			±1	—	
ED	Differential linearity error		ADCVref = Int 2.5V f_{ADC} = 250 kHz	±1	—	
EL	Integral linearity error			±2	—	
ED	Differential linearity error		ADCVref = Int 1.5V f_{ADC} = 250 kHz	±1	—	

Symbol	Parameter	Test conditions		Typ	Max(4)	Unit
EL	Integral linearity error			±2	—	
ED	Differential linearity error		ADCVref = Int 0.625V f_{ADC} = 250 kHz	±2	—	
EL	Integral linearity error			±3	—	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and$\Sigma I_{INJ(PIN)}$ in **Section 6.3.14** does not affect the ADC accuracy.
3. Better performance may be achieved in restricted VDDA, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.

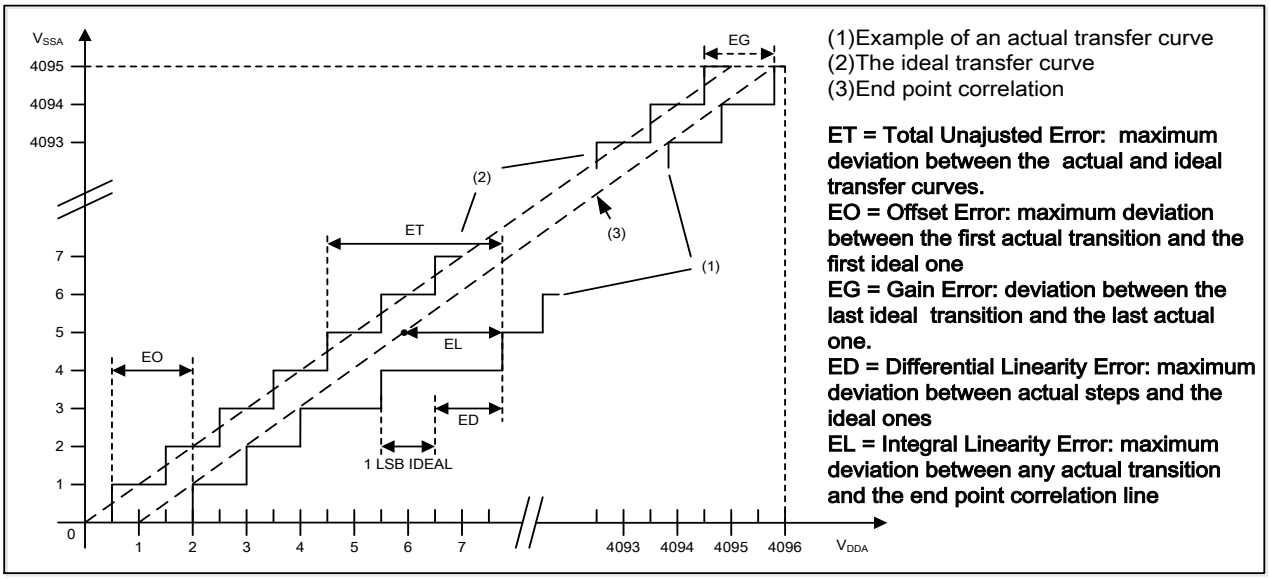


Figure 6.11 ADC accuracy characteristics

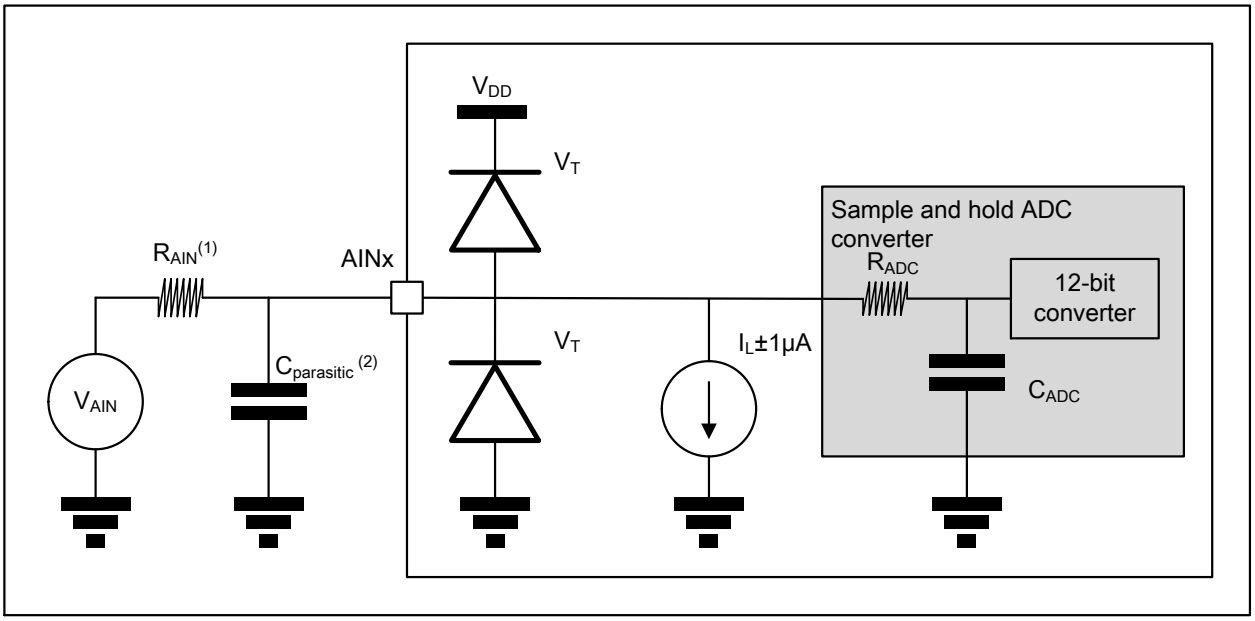


Figure 6.12 Typical connection diagram using the ADC

1. Refer to **Table 6.37**: ADC characteristics for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. Cparasitic represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high Cparasitic value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in **Figure 6.3**: Power supply scheme. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.17. Temperature sensor(V_{TS}) characteristics

Table 6.40 TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L (1)	V_{TS} linearity with temperature	—	±1.4	±2	°C
Avg_Slope(1)	Average slope	—	4.3	—	mV/°C
V_{25}	Voltage at 25 °C (± 5 °C) (2)	—	1.50	—	V
t_{START} (1)	ADC_IN16 buffer startup time	—	—	10	μs
t_{S_temp} (1)	ADC sampling time when reading the temperature	4	—	—	μs

1. Guaranteed by design, not tested in production.
2. Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{25} ADC conversion result is stored in the TS_CAL1 byte. Refer to **Table 3.2**: Temperature sensor calibration values.

6.3.18. I/O Sample and hold circuit characteristics

Table 6.41 IOSH characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{S_iosh}(1)	ADC sampling time when reading the V_{IOSH}	—	4	—	μs
t_{IOSH_SAMP}	I/O input sampling time (refer to formula 1 and **Table 6.42**)	—	3.32	—	μs
t_{IOSH_HOLD}(1)	I/O voltage output hold time (after disabling sample)	—	1	—	ms
V_{IOSH_AIN}(1)	I/O input voltage range	0.5V	—	V_{DDA}-1.5V	V
V_{IOSH_OFFSET}(1)	IOSH Offset voltage	-5	—	5	mV

1. Guaranteed by design, not tested in production.

Formula1 :

$$t_{IOSH\_SAMP} > [\ 0.04 \times R + 2.84\ ]\ (\mu s)$$

Table 6.42 Minimum value of t_{IOSH_SAMP} at different external series resistor

Res(kΩ)	t_{IOSH_SAMP} (μs)(1)
> 50	(Not recommended)
50	4.84
25	3.84
12	3.32
< 12	3.32

1. Guaranteed by design, not tested in production.

6.3.19. Operational amplifier characteristics

Table 6.43 Operational amplifier characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{S_op}(1)	ADC sampling time when reading the output of OPAMP	—	4	—	μs
t_{OP_SAMP}(1)	Internal time between I/O sample and output stable	—	300	—	μs
V_{OP_AIN}(1)	IO input voltage range, V_{DD} =5V	V_{SS}	—	V_{DDA} – 1.5	V
V_{OP_OFFSET}(1)	Offset voltage	—	±0.75	—	mV
GBW(1)	Gain bandwidth	—	2.49	—	MHz
PSRR(1)	Power supply rejection ratio, V_{DD} =5V	—	100	—	dB
CMRR(1)	common mode rejection ratio, VCM=V_{DD}/2, V_{DD} =5V	—	100	—	dB
GAIN(1)	Voltage gain	—	135	—	dB

1. Guaranteed by design, not tested in production.

6.3.20. Comparator

Table 6.44 Comparator Characteristics

Symbol	Parameter		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage		2.0	—	5.5	V
V_{IN}	Comparator input voltage range(1)	COMP1	1.0	—	V_{DDA}-0.5	V
		COMP2	0.5	—	V_{DDA}-1.5	
		COMP3	0.5	—	V_{DDA}-1.5	
V_{offset}	Offset error(2)	COMP1	—	±6	—	mV
		COMP2	—	±4	—	
		COMP3	—	±5	—	
$I_{DD(comp)}$	power dissipation		—	60	—	μA

1. -40 – 85 °C, V_{DD} = 2.0 – 5.5 V;
2. -40 – 85 °C, Vin = V_{DD}/2, V_{DD} = 2.0 – 5.5 V.

6.3.21. Timer characteristics

Refer to **Section 6.3.14**: I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 6.45 TIMx characteristics

Symbol	Parameter	Conditions	Min(1)	Max(1)	Unit
t_{res}(TIM)	Timer resolution time	—	—	—	$t_{TIMXCLK}$
		$f_{TIMXCLK}$ = 96 MHz	10.4	—	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	—	—	$f_{TIMXCLK}$/2	MHz
		$f_{TIMXCLK}$ = 96 MHz	0	48 MHz	MHz
$t_{COUNTER}$	16-bit timer period	—	—	65536	$t_{TIMXCLK}$
		$f_{TIMXCLK}$ = 96 MHz	0.0104	683	μs
$t_{MAX\ COUNT}$	maximum count	—	—	65536*65536	$t_{TIMXCLK}$
		$f_{TIMXCLK}$ = 96 MHz	—	44.74	s

1. Guaranteed by design, not tested in production.

Table 6.46 IWDG min/max timeout period at 40 kHz (LSI) (1)

Prescaler	PR[2:0]	Min timeout RL[1:0]=0x000	Max timeout RL[1:0]=0xFFF	Unit
/4	0	0.1	409.6	ms
/8	1	0.2	819.2	
/16	2	0.4	1638.4	
/32	3	0.8	3276.8	
/64	4	1.6	6553.6	
/128	5	3.2	13107.2	
/256	6/7	6.4	26214.4	

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 6.47 WWDG min/max timeout value at 96 MHz

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0427	2.7307	ms
2	1	0.1138	7.2818	
4	2	0.1707	10.9227	
8	3	0.3413	21.8453	

6.3.22. Communication interfaces

SPI characteristics

Unless otherwise specified, the parameters given in **Table 6.48** are derived from tests performed under the conditions summarized in **Table 6.4**.

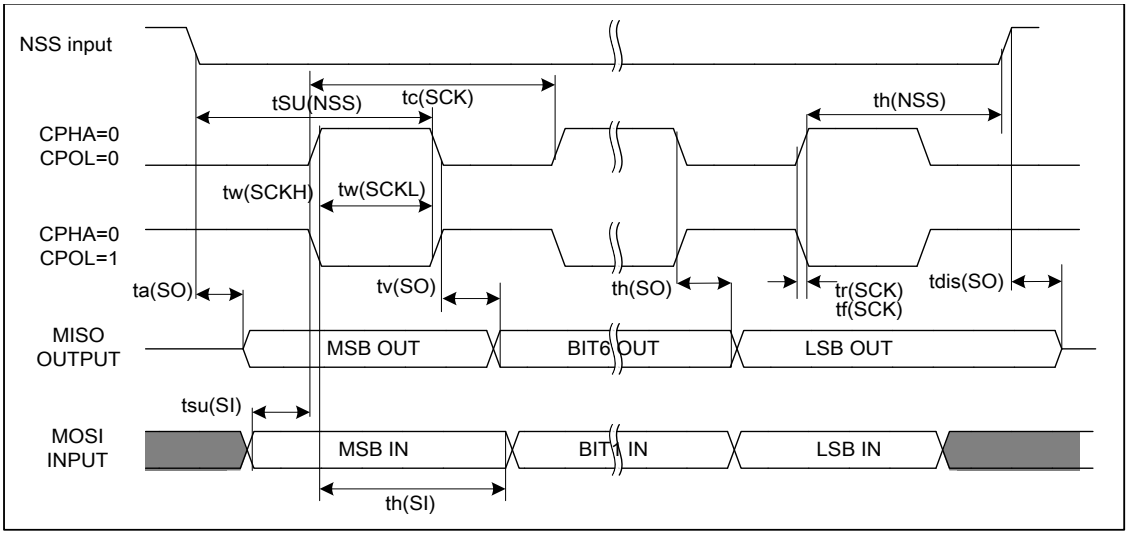
Refer to **Section 6.3.14**: I/O port characteristics for details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 6.48 SPI characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{C(SCK)}$	SPI clock frequency	Master mode	—	36	MHz
		Slave mode	—	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	—	6	ns
$t_{su(NSS)}$ (2)	NSS setup time	Slave mode	$4T_{PCLK}$	—	ns
$t_{su(NSS)}$ (2)	NSSB hold time	Slave mode	$2T_{PCLK}$ + 10	—	
$t_{W(SCKH)}$ $t_{W(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz prescaler = 4	T_{PCLK} /2-2	T_{PCLK}/2+1	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	4	—	
		Slave mode	5	—	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	4	—	
		Slave mode	5	—	
$t_{a(SO)}$ (2)(3)	Data output access time	Slave mode, f_{PCLK} = 24 MHz	0	4 T_{PCLK}	
$t_{dis(SO)}$ (3)	Data output disable time	Slave mode	0	18	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	—	22.5	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	—	6	
$t_{h(SO)}$	Data output hold time	Slave mode	11.5	—	

		(after enable edge)			
$t_{h(MO)}$		Master mode (after enable edge)	2	—	
Duty(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%

1. Data based on characterization results, not tested in production
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z



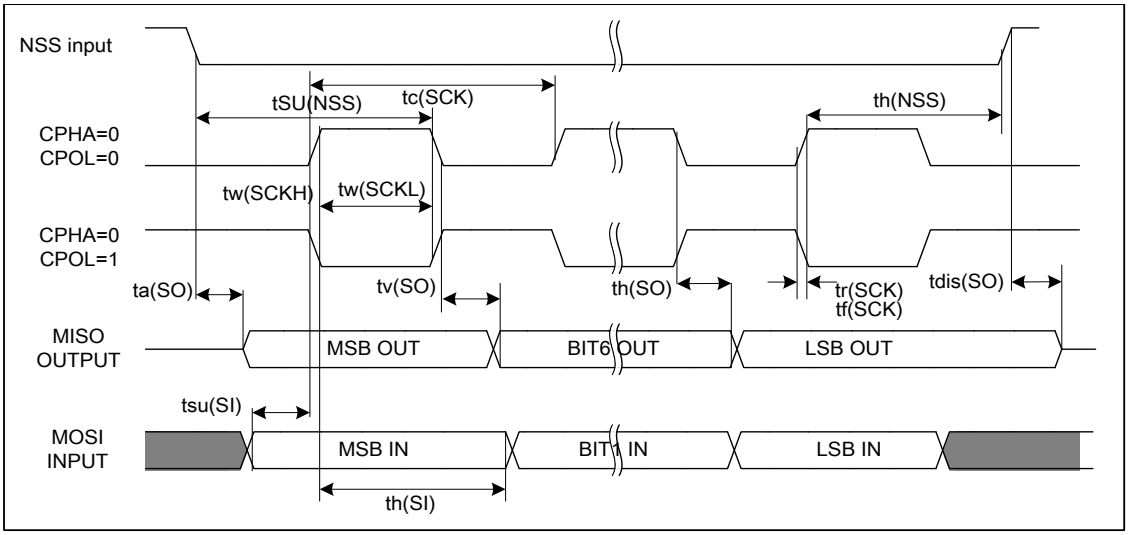


Figure 6.13 SPI timing diagram – slave mode and CPHA=0

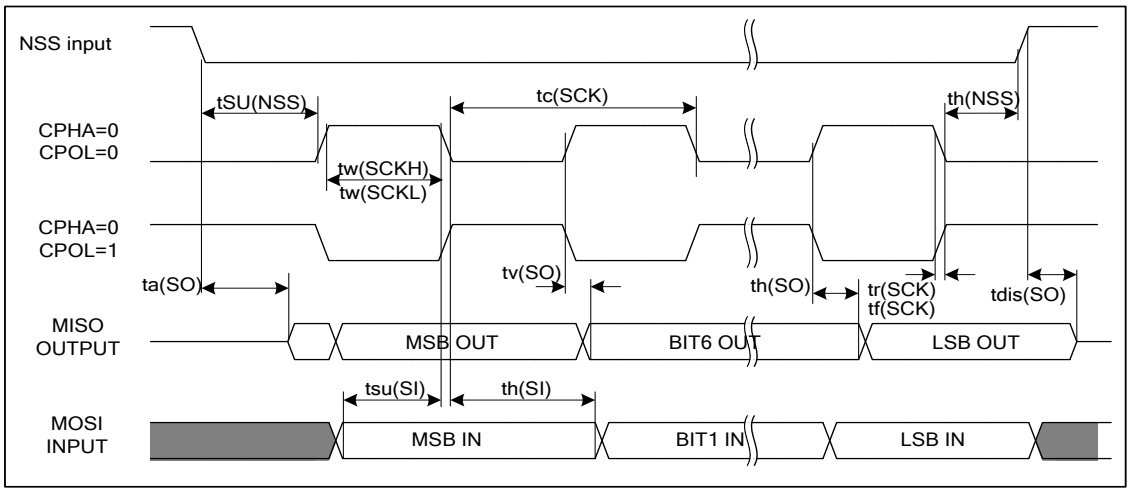


Figure 6.14 SPI timing diagram – slave mode and CPHA=1

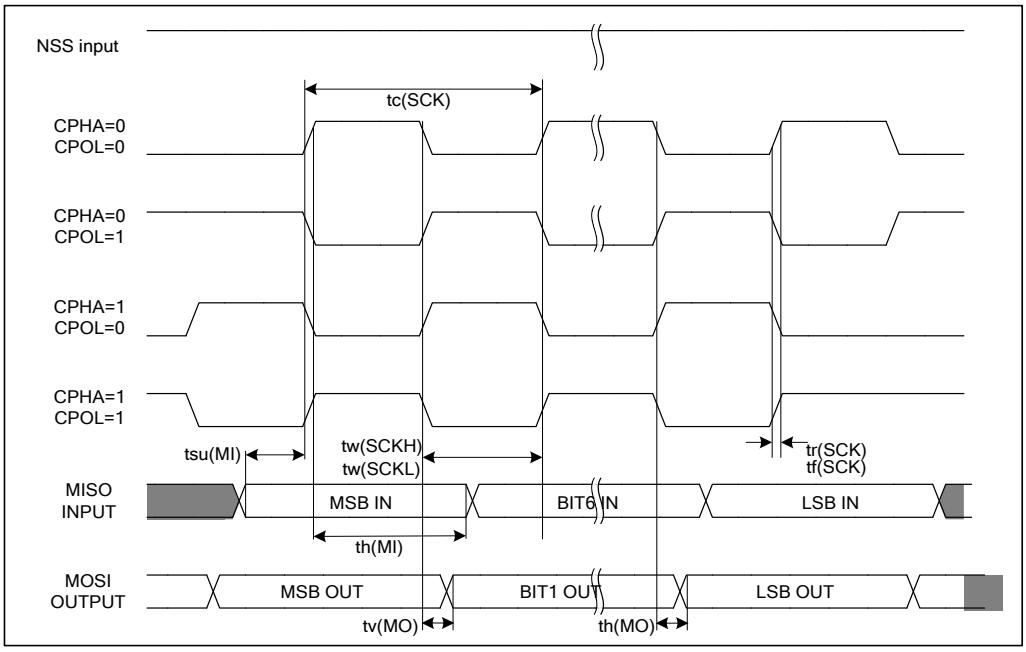
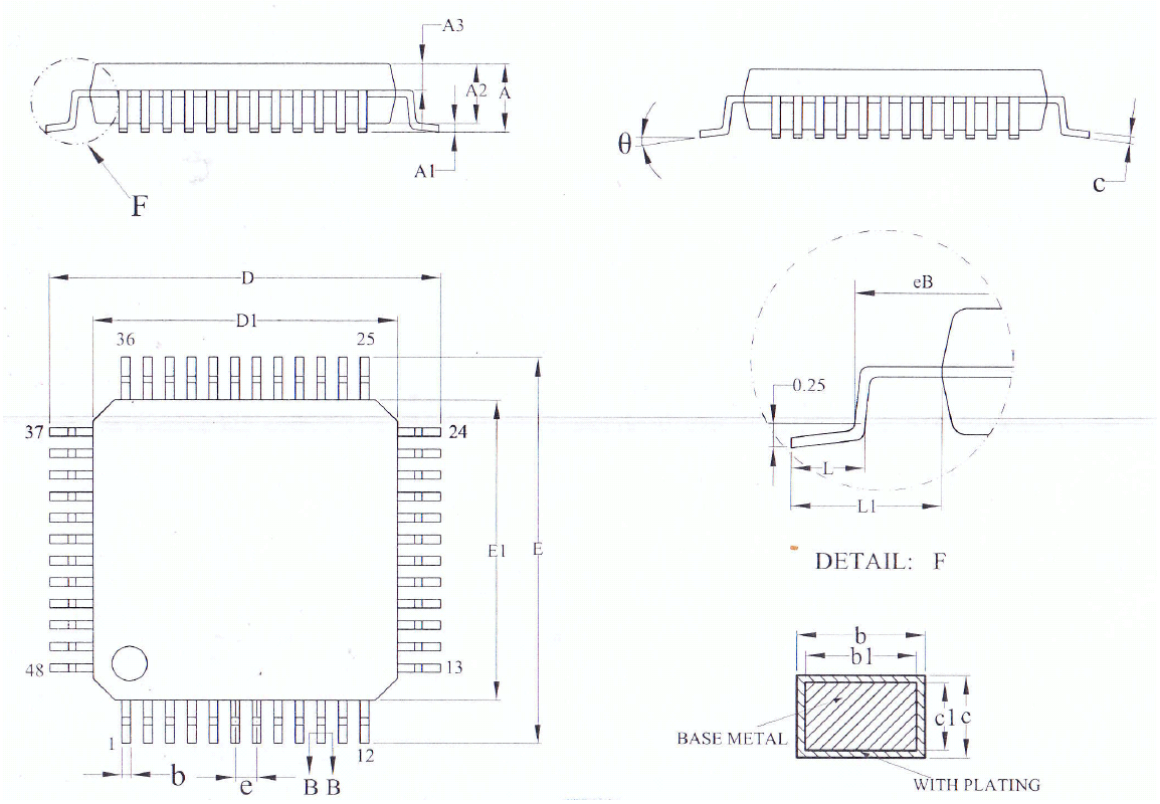


Figure 6.15 SPI timing diagram – master mode

7. Package information

The device is available in LQFP48 packages. The specific package size information is shown below:



Symbol	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.063
A1	0.050	—	0.150	0.002	—	0.006
A2	1.350	1.400	1.450	0.053	0.055	0.057
A3	0.590	0.640	0.690	0.023	0.025	0.027
b	0.180	—	0.260	0.007	—	0.010
b1	0.170	0.200	0.230	0.007	0.008	0.009
c	0.130	—	0.170	0.005	—	0.007
c1	0.120	0.130	0.140	0.005	0.005	0.006
D	8.800	9.000	9.200	0.346	0.354	0.362
D1	6.900	7.000	7.100	0.272	0.276	0.280
E	8.800	9.000	9.200	0.346	0.354	0.362
E1	6.900	7.000	7.100	0.272	0.276	0.280
eB	8.100	—	8.250	0.319	—	0.325
e	0.500BSC			0.020BSC		
L	0.450	—	0.750	0.018	—	0.030
L1	1.000REF			0.039REF		
θ	0°	—	7°	0°	—	7°