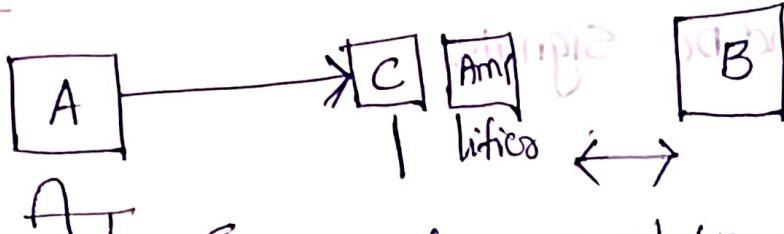


UNIT - 4

Operational Amplifiers

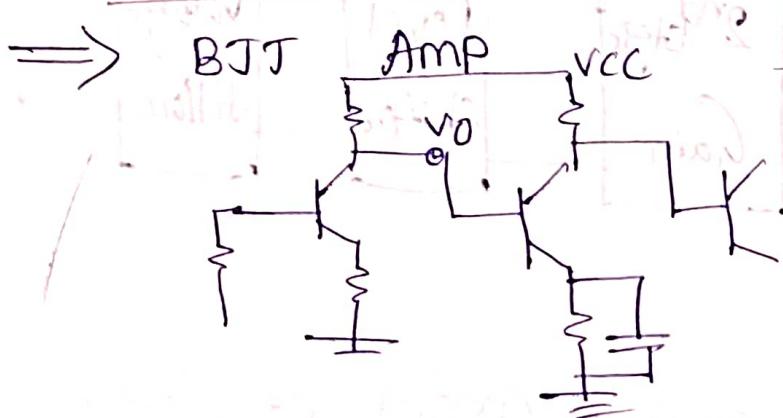
Introduction



* It is a Direct coupled Amplifier having high voltage gain

⇒ In the previous stages

we use BJT



In this circ. capacitor, Resistor, BJT are the discrete components.

⇒ The discrete components increase the size of circ complexity n. are increased, then the

⇒ The more number of stages amplification factor is increases.

⇒ so we are overcome circ complexity disadvantage of OP-AMP by using IC. [Integrated Circuits].

The chip size is 100. nm

⇒ for first IC, the operation Amplifier was designed was MA 741

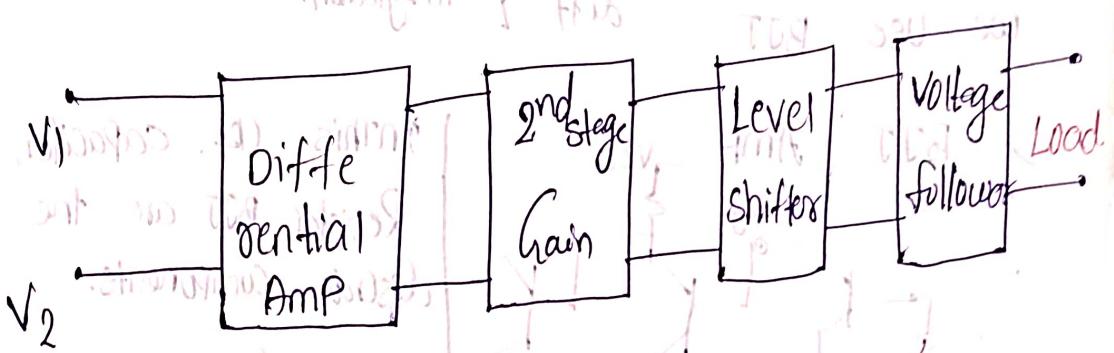
This IC consist of 7 pins. 1 OIP

⇒ IC 741 →

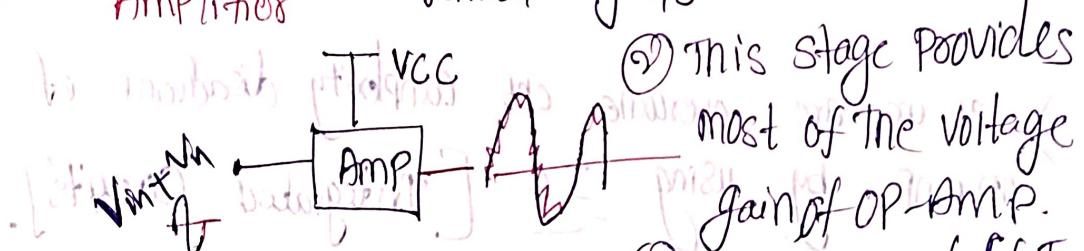
Internal block diagram of OP-AMP:

- * An operational amplifier can be used to amplify both AC and DC signals.

The internal block diagram of operational amplifier is shown in figure.



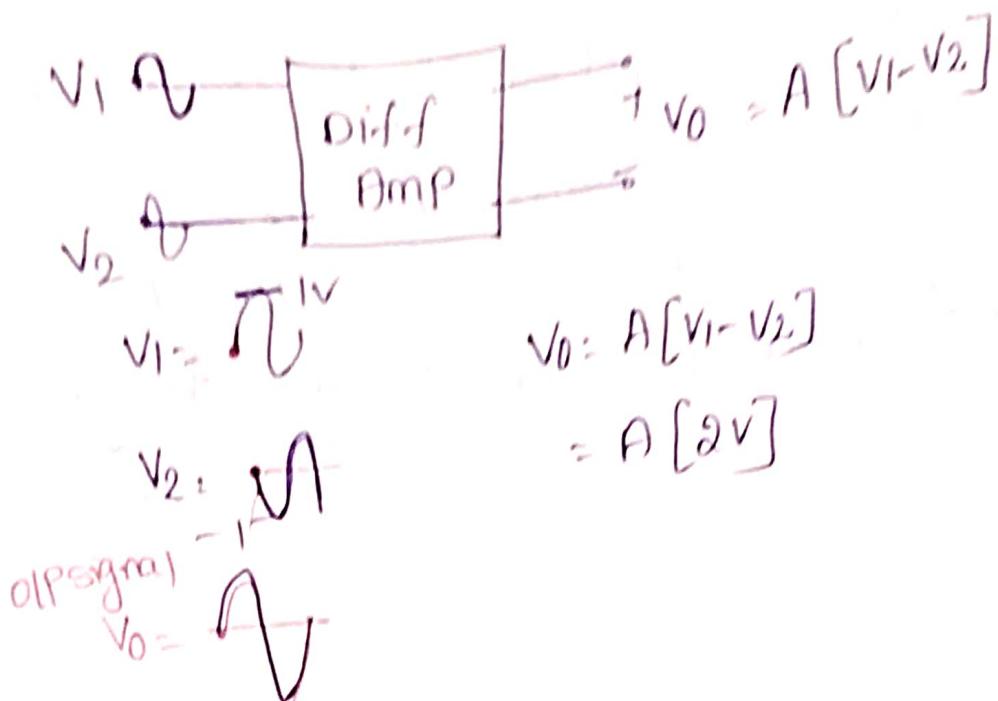
- * The input stage of OP-AMP consists of dual input balanced output diff amp differential :- It will amplify only the differential signals.



- * This stage provides most of the voltage gain of OP-AMP.
- * It consists of FET
- To overcome this single stage Amp problem

we are using Differential Amp.

with matched Charach. & sig in order to have high input Impedance



② 2nd stage Gain:- The OIP of first is connected at input of second stage. Second stage of OP-Amp is dual input unbalanced output differential amplifier. This stage is used to further increase the voltage gain and to get single output from dual input. There is direct coupling between input stage and second stage due to which the DC level of signal at output of second stage is well above the ground level.

In second stage, the output of first stage is fed back through a negative feedback path. The feedback factor is determined by the ratio of the resistors Rf and R2. The output of the second stage is given by the equation:

$$V_{out} = A_{v2} V_{in} + A_{fb} V_{fb}$$

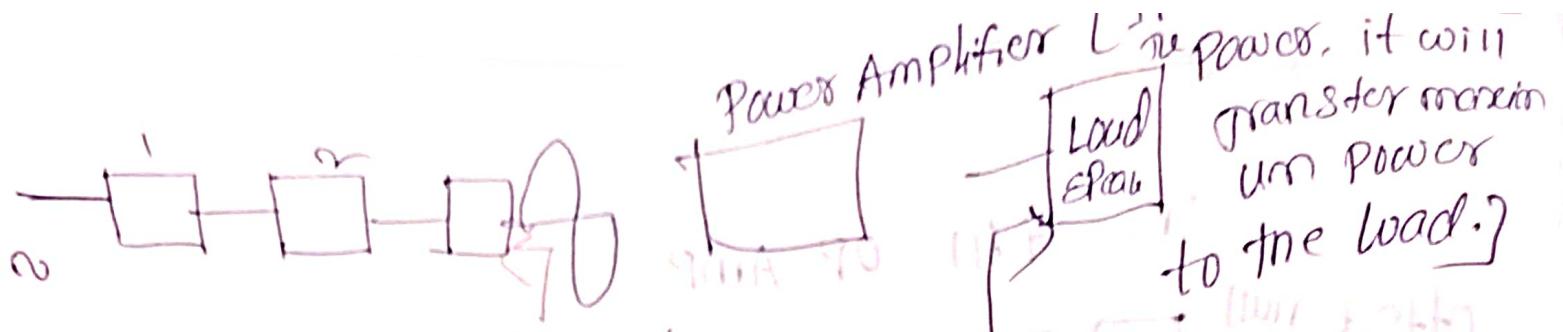
(iii) Third stage:- [Level shifter] [champer]

This stage of operational Amplifiers consist of an emitter follower or level shifter. This stage is used to bring DC level of signal to ground level.

(iv) voltage followers

The other name of voltage follower is Power - Amplifiers or voltage Buffer.

- * Last or output stage of an operation Amplifiers is a Push-Pull Complementary Amplifier. This stage increases the output voltage swing and raise current supplying capability of OP-Amp. Therefore, output stage is used to enhance the Power level at the output of OP-Amplifiers. This output stage also provide the low output Resistance.



OIP Impedance
will be very low
large

Power Amplifier L'ie power, it will
transfer maximum
power to the load.]

OIP Impedance
low

Low

load

→ It may not deliver maximum power to the load. There should be some device match the impedance.

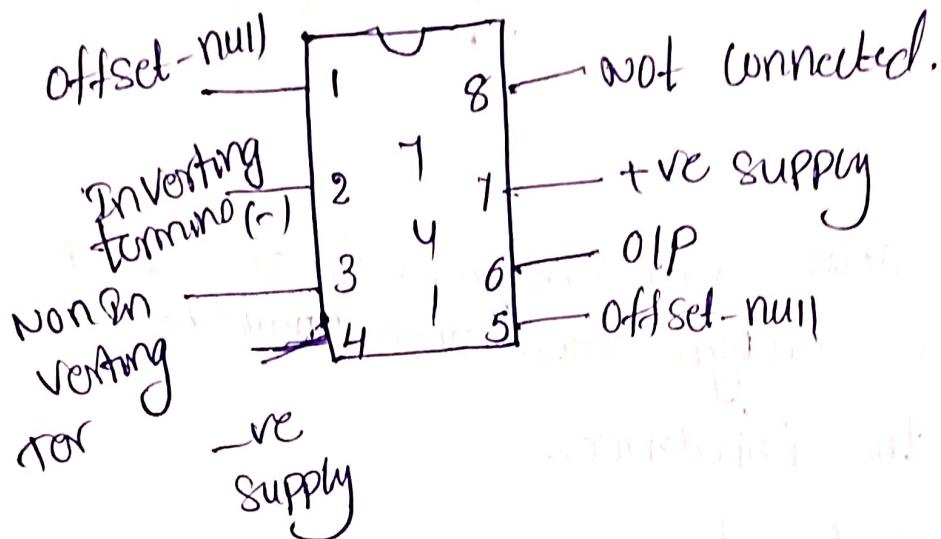
→ why we are match the impedance. we recall the

$$R_L = R_s = R_i$$

→ The Power Amplifier have very large OIP Impedance.
Low output impedance.

Pin Diagram of OP-AMP

IC 741 OP-AMP



- ⇒ The schematic symbol of an OP-AMP is shown in figure. OP-amp has two input terminals with Plus (+) and minus (-) notations and one output terminal.
- ⇒ Two additional terminals shown in fig. are used for Power supplies of OP-AMP. The input terminal with (+) notation is called non-inverting terminal and input terminal with (-) notation is called inverting terminal.
- ⇒ When OIP is connected at non-inverted terminal with inverting terminal grounded, The OIP of OP-AMP in phase with OIP signal and when OIP is applied at inverting terminal with non-inverting terminal connected to

Ground; the OIP signal is 180° out of phase with respect to IIP signal.

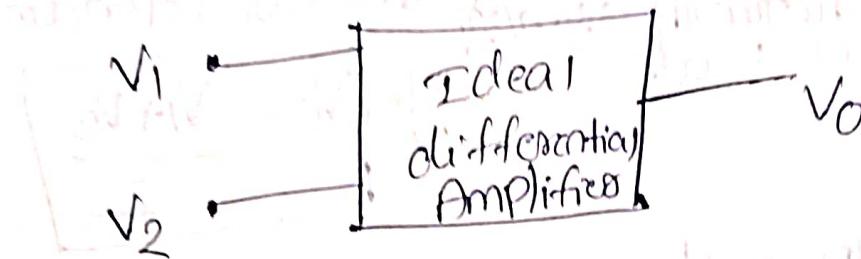
- * The Pin diagram of an 8 Pin IC operational Amp As shown in figure. The labellings along with number of each Pin indicates the function of Pin. The Pin number 2 is inverting input, Pin 3 is non-inverting input, Pin 6 is output terminal of OP-AMP. Pin 7 & 4 are Power supply terminal labeled as $+V_{CC}$ & $-V_{EE}$ respectively, Pin 1 and 5 are used for DC offset null. Pin 8 is labeled as NC which indicates "no connection".



Differential Amplifier

⇒ A differential Amplifier can Amplify the difference between two input voltages:

$$[V_d = V_1 - V_2]$$



- $V_0 \propto V_1 - V_2$

- $V_0 = Ad(V_1 - V_2)$ where Ad = differential gain

we know that

$V_0 = Ad V_d$

hence
$$Ad = \frac{V_0}{V_d}$$

⇒ now Inorder to express differential gain in terms of decibels;

$Ad \text{ in dB} = 20 \log Ad (\text{dB})$

* Ex:-

$V_1 = 5V \quad V_2 = 2V$

$V_d = 3V$

Ex:-2 If $V_1 = V_2$, then diff Amplifier out Put voltage $V_0 = 0$ (Practical this not happen.)

* Common mode gain:-

- If two i/p voltages are equl, it is common mode: [The diff Amp O/P not only dependent upon diff i/p and also dependent on average of the two i/p signals]
• The common mode voltage $V_C = \frac{V_1 + V_2}{2}$
- Now the O/P voltage $V_O = A_C V_C$

$$A_C = \frac{V_O}{V_C}$$

- ⇒ ∵ The total voltage for any differential amplifier is

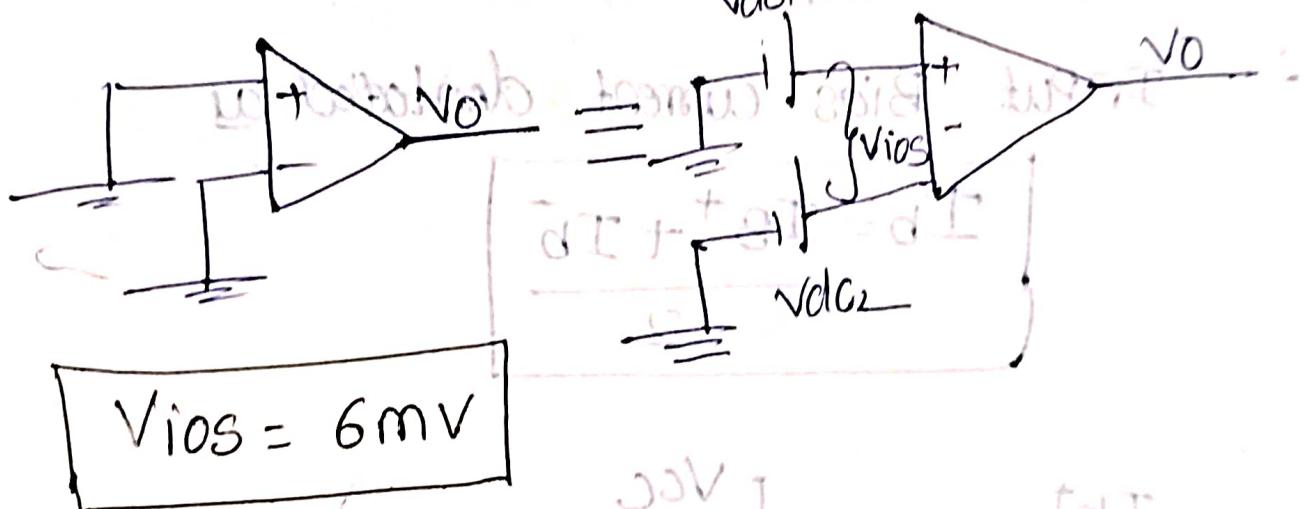
$$V_O = A_D V_d + A_C V_C$$

* characteristics of OP-Amp:-

① Input Offset Voltage:-

The differential voltage that must be applied between the two input terminals of an OP-Amp to make the output voltage zero is called input offset voltage.

$$\Rightarrow \text{It is denoted as } V_{ios} = |V_{dc1} - V_{dc2}|$$

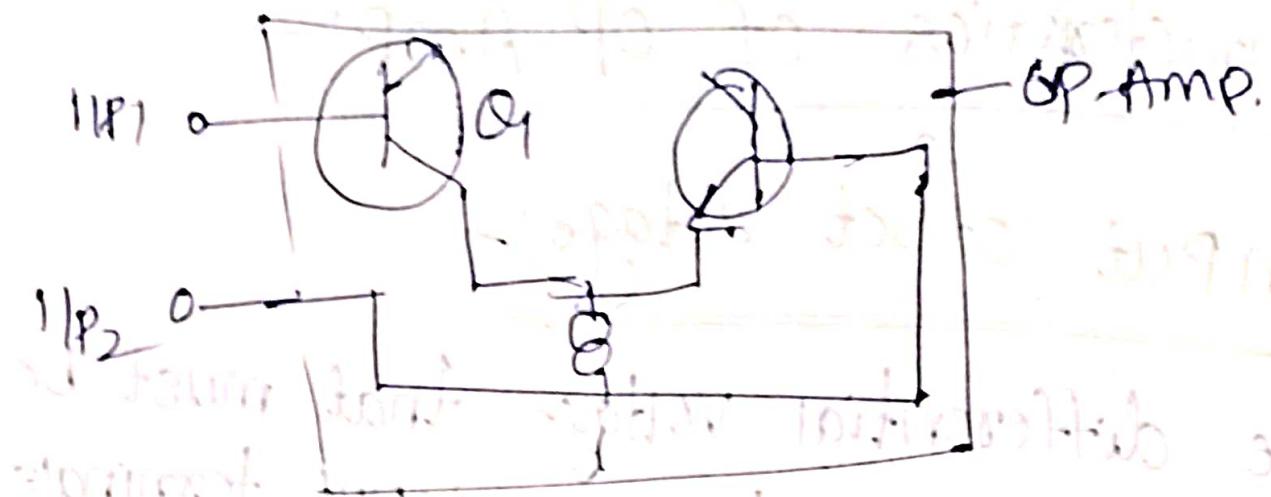


② Input Offset Current:-

The algebraic difference between the current flowing into the two input terminals of the OP-Amp is called input offset current.

$$\Rightarrow \text{Input offset current denoted as}$$

$$I_{ios} = |I_{b1} - I_{b2}|$$

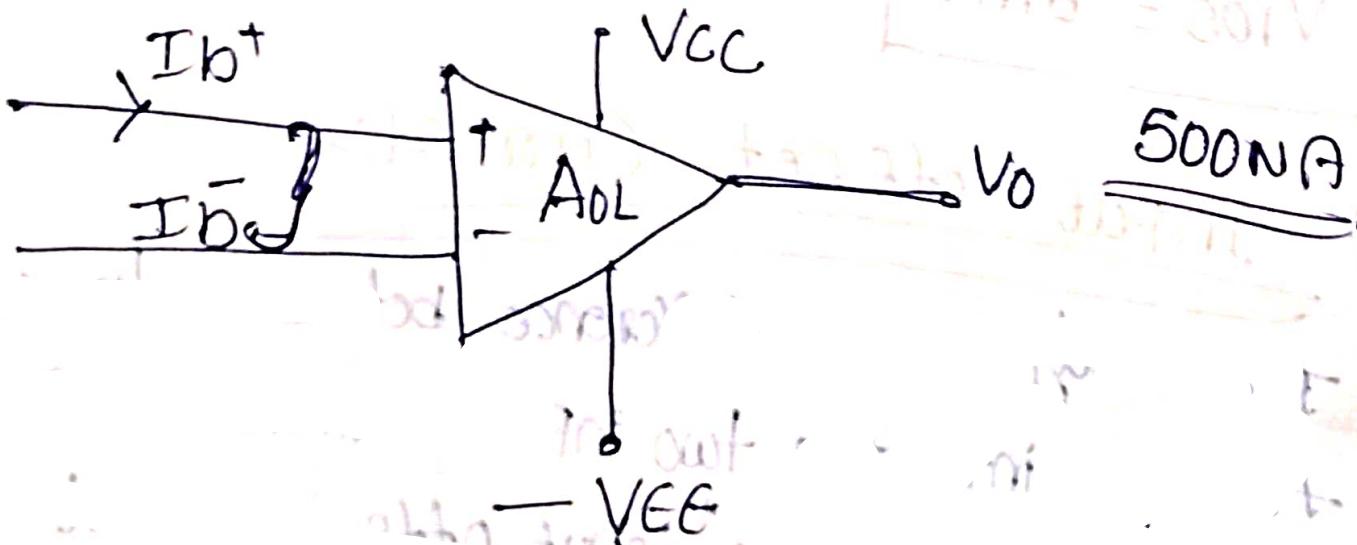


- ③ Ideally zero, but IC741 OP-Amp maximum value of I_{ios} is 20nA

The Average value of the two currents flowing into the OP-Amp input terminals is called input bias current.

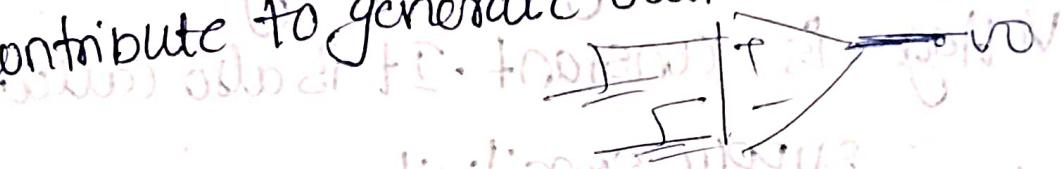
Input Bias Current denoted by

$$I_b = \frac{I_{B^+} + I_{B^-}}{2}$$



* Output offset voltage:-

The output offset voltage is the D.C voltage present at the output terminals when both the input terminals are grounded. Both input offset voltage V_{ios} and input bias current contribute to generate output offset voltage.



* Output voltage swing:-

→ The O.P. voltage swing is limited.

It gets decided by the supply voltages.

If it never exceeds the limits $+V_{CC}$ and $-V_{EE}$. If it gets above these values, OP-Amp output gets saturated.

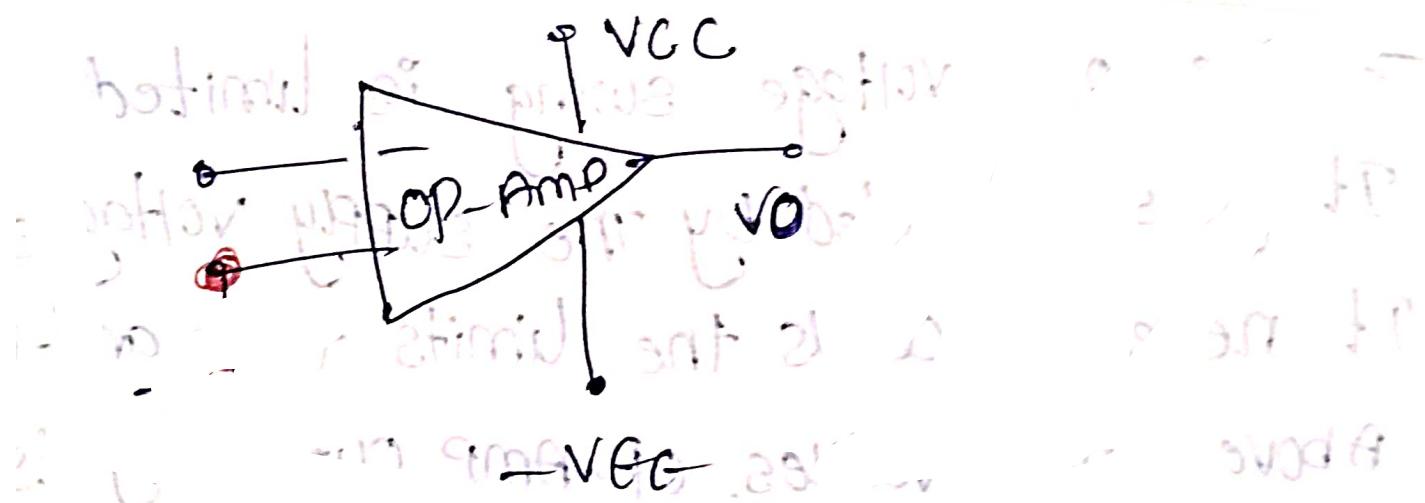
⇒ Thus note that the OP-Amp output voltage gets saturated at $+V_{CC}$ and $-V_{EE}$ & it can produce output voltage more than $+V_{CC}$ and $-V_{EE}$. Practically saturation voltages $+V_{sat}$ and $-V_{sat}$ are slightly less than $+V_{CC}$ and $-V_{EE}$.

for

OP-Amp saturation voltages are I.B SUPPLY $\pm 1\text{V}$.

Power Supply Rejection ratio (PSRR)

- Power supply Rejection ratio (PSRR) is defined as the ratio of the change in input offset voltage due to the change in supply voltage. Producing it, keeping other supply voltage is constant. It is also called power supply sensitivity.



- * Now V_{EE} is constant and due to certain change in V_{CC} , there is change in input offset voltage. Then PSRR is defined as

$$PSRR = \frac{\Delta V_{ios}}{\Delta V_{CC}}$$

$V_{EE} = \text{constant}$

* Thermal drift:-

the OP-Amp parameters input offset voltage, input bias current I_b and input offset current I_{ios} are not constant but vary with factors.

- ① Temperature
- ② supply voltage changes
- ③ Time.

* Thermal voltage drift:- The Thermal voltage drift is defined as average rate of change of input offset voltage per unit change in temperature.

$$\therefore \text{Input offset voltage drift} = \frac{\Delta V_{ios}}{\Delta T}$$

* Thermal drift input bias current:-

$$\therefore \text{Thermal drift input bias current} = \frac{\Delta I_b}{\Delta T}$$

$$\therefore \text{Thermal drift input offset current} = \frac{\Delta I_{ios}}{\Delta T}$$

* CMRR:- It is the ratio of differential gain and to the common mode voltage gain AC.

$$\boxed{\text{CMRR} = \frac{A_d}{A_c}}$$

For IC 741-OP-Amp QdB

* Slew rate:

⇒ The slew rate is defined as the maximum rate of change of output voltage with time.

$$\text{slew rate } s = \frac{dv_o}{dt} \Big|_{\text{max}} \quad (\text{V/}\mu\text{s})$$

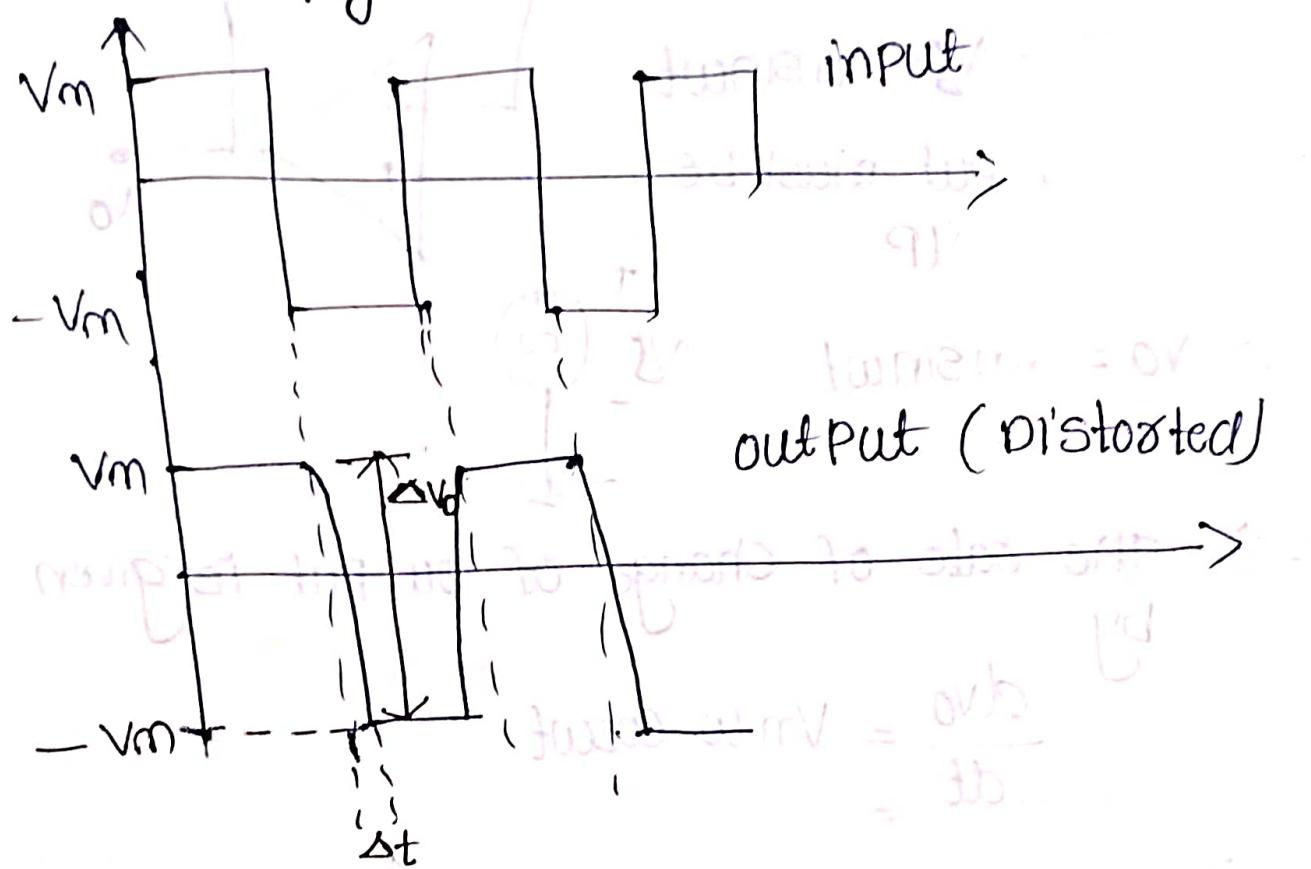
⇒ The slew rate indicates how fast output changes if input is also changing.

⇒ It is specified by operating OP-Amp in unity gain condition.

* Effect of slew rate

⇒ Consider a circuit using OP-Amp having unity gain. The output is same as input.

⇒ If the input is square wave, output has to be square wave. But this is observed for certain frequency of input. Due to slew rate of an OP-AMP, for a particular input frequency output gets distorted as shown in the fig.



* Reason for Slew Rate

- There is usually a capacitor within or outside of OP-AMP to prevent oscillation.
- This capacitor which prevents the o/p volt from fast changing input.
- ⇒ The rate at which the voltage across the capacitor changes is given by

$$\text{3rd order} \quad \frac{dv_o}{dt} = \frac{V_m \sin \omega t}{C} \quad i = C \frac{dv}{dt}$$

or becomes

and at first it will be ~~form~~ ~~prop~~ ~~ratio~~

\Rightarrow For a sine wave input, the effect of slope can be calculated as consider voltage follower.

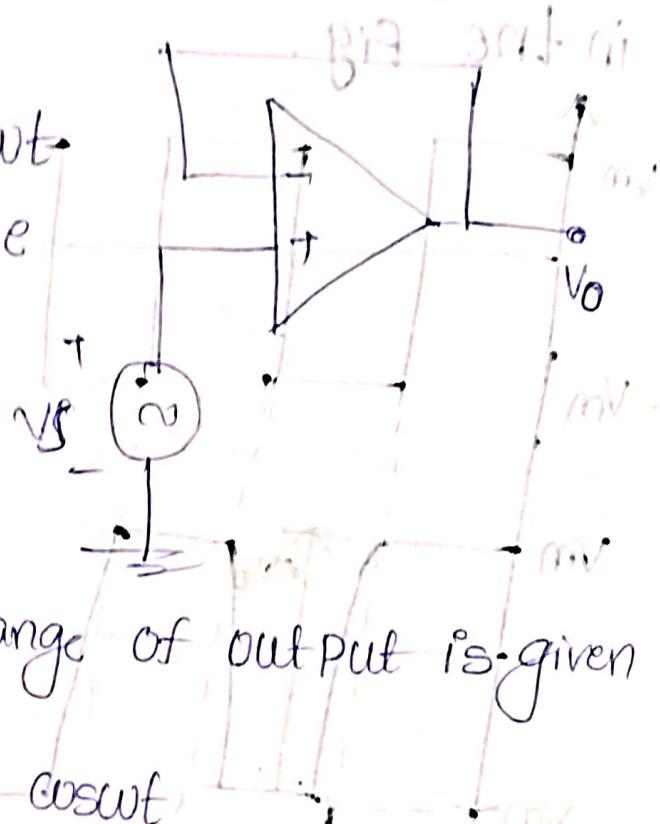
~~more~~ ~~more~~ ~~more~~ ~~more~~

\Rightarrow If i_P V_S = V_m sin ωt

Then output must be same as i_P

$$\therefore V_o = V_m \sin \omega t$$

(because i_P & V_S) ~~are two~~



\Rightarrow The rate of change of output is given by

$$\frac{dv_o}{dt} = V_m \omega \cos \omega t$$

\Rightarrow The maximum rate of change of output (when $\cos \omega t = 1$)

$$\text{so SR} = \frac{dv_o}{dt} \max = \omega V_m \text{ or } \omega = \frac{\omega V_m}{V_m} = \omega$$

$$\therefore SR = 2\pi f V_m \text{ V/sec}$$

\Rightarrow For distortion free output, the maximum allowable input frequency f_{in} can be obtained as

$$f_{\text{on}} = \frac{S_{\text{in}}}{2 \pi V_m} \text{ Hz}$$

where f_{on} is the full power bandwidth of OP-AMP.