* BJT Biasing :-

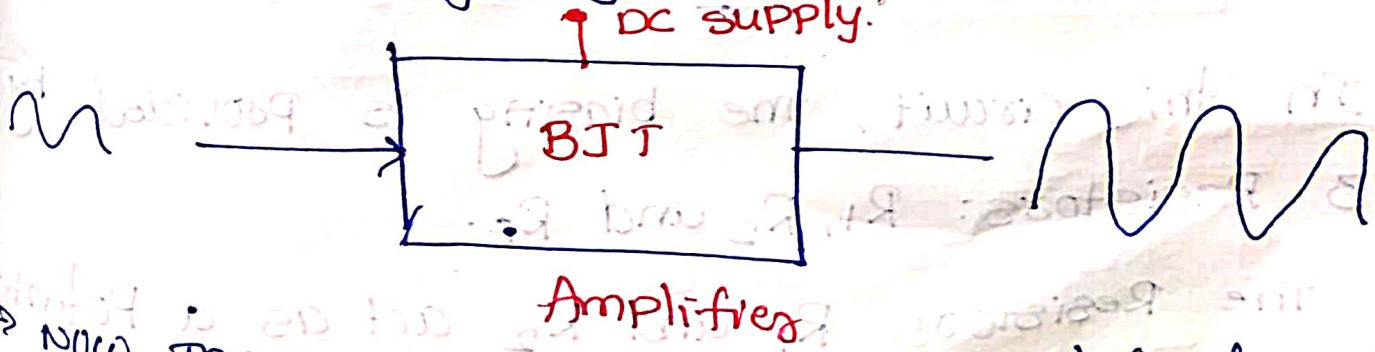
→ The Transistor can be operated in 3 regions. Cut-off, Active and saturation by applying proper biasing conditions as shown in the table.

Region of operation	J_E	J_C
Cut-off	R-B	R-B
Active	F-B	R-B
saturation	F-B	F-B

→ In order to operate Transistor in the desired region we have to apply external d-c voltages of correct Polarity and magnitude to the two Junctions of the Transistor. Because d-c voltages are used to bias the transistor, biasing is known as d-c biasing of the Transistor.

* Need for Biasing :-

→ In Transistor Amplifier Circuits, output signal Power is always greater than input signal Power.



→ Now the question is how this Amplification of Power is achieved. The d-c sources (d-c biasing) supplies the Power to the transistor circuit to get

→ ∴ Therefore the biasing is needed

1. To operate transistor in the desired Region
2. To get the output signal power greater than input signal power.

⇒ Commonly used BJT Biasing ckts are

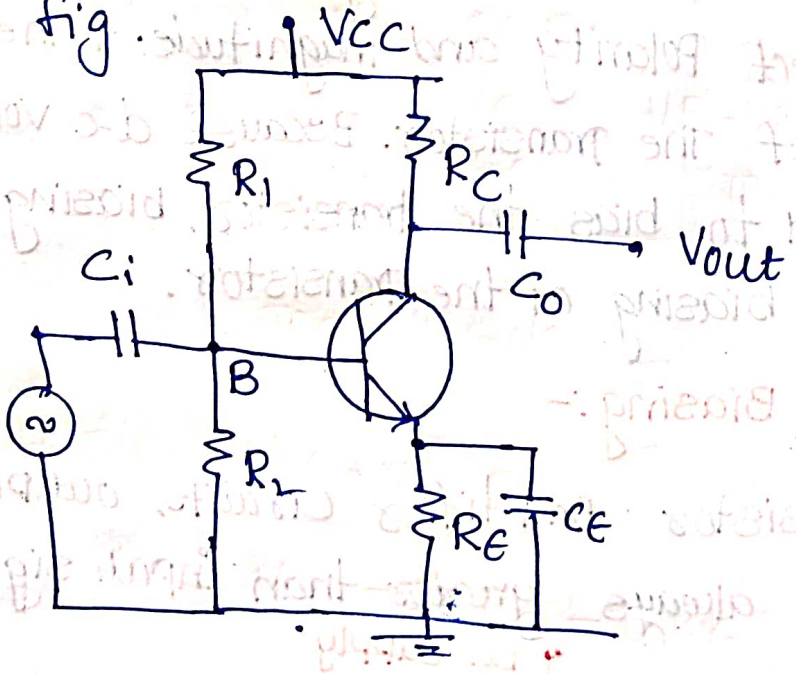
① fixed bias ckt

② collector to Base bias ckt

③ self bias ckt [Voltage divider bias ckt]

* Self bias Circuit:-

→ The voltage divider bias circuit As shown in fig.



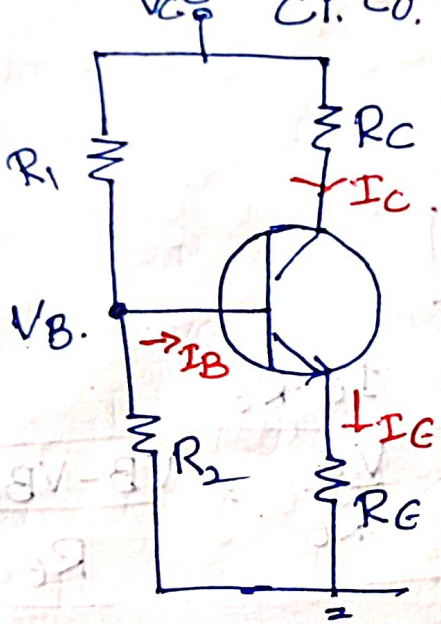
⇒ In this circuit, the biasing is provided by 3 Resistors: R_1, R_2 and R_E.

→ The Resistors R_1 and R_2 act as a Potential divider ~~biasing~~ giving a fixed voltage to

→ If collector current increases due to change in temparature or change in β, the emitter current I_E also increases and the voltage drop across R_E increases, Reducing the voltage difference blw base and emitter (V_{BE}).

→ Due to Reduction in V_{BE}, base current I_B and hence collector current, I_C also reduces.

DC Analysis:- [i/p voltages shorted. The capacitor C_i. C_o. C_E are open circuited]

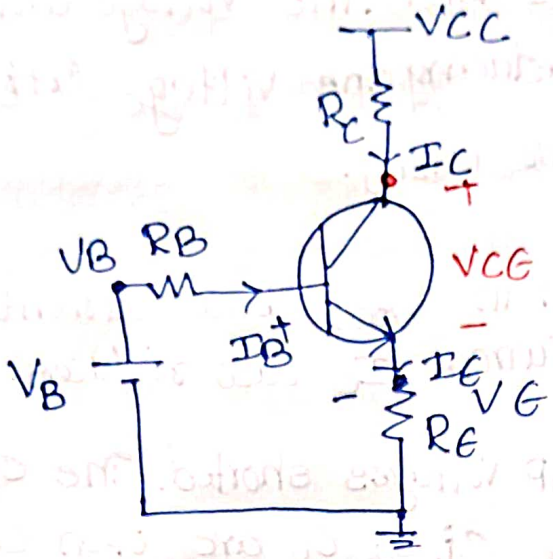


→ Let us consider the base circuit as shown in fig voltage across R_2 is the base voltage V_B.

$$V_B = \left[\frac{R_2}{R_1+R_2}\right] \cdot V_{CC}$$

$$R_{Th} = R_1 \,||\, R_2 = R_B.$$

→ The simplified circuit as shown in figure



From i/p

$$-V_B + V_{BE} + V_E = 0$$

$$\therefore \boxed{V_E = V_B - V_{BE}}$$

∴ we know that $V_E = I_E \cdot R_E$

$$\checkmark \quad \boxed{I_E = \frac{V_E}{R_E} = \frac{V_B - V_{BE}}{R_E}}$$

⇒ Apply KVL to the o/p side

$$-V_{CC} + I_C R_C + V_{CE} + V_E = 0$$

$$\checkmark \quad \boxed{V_{CE} = V_{CC} - I_C R_C - I_E R_E} \quad \checkmark$$

* Calculation I_B

Apply KVL to the i/p side

$$-V_B + I_B R_B + V_{BE} + V_E = 0$$

$$I_B \cdot R_B + I_E R_E = V_B - V_{BE}$$

We know that $I_C = (1+\beta) I_B$.

$I_B \cdot R_M + (1+\beta) I_B \cdot R_E = V_B - V_{BE}$

$$\therefore \boxed{I_B = \frac{V_B - V_{BE}}{R_M + (1+\beta) R_E}}$$

∴ we know that $I_C = \beta \cdot I_B$.

$$\boxed{I_C = \beta \cdot \frac{V_B - V_{BE}}{R_M + (1+\beta) R_E}}$$

* DC Load Line and Quiescent Point

→ we know that, at cut off both the junctions of the transistor are reverse biased and at saturation both are forward biased and in Active Region Emitter Junction is forward biased and collector Junction is reverse biased.

⇒ DC Load Line is the straight line drawn on the output characterstics of the transistor.

⇒ Extreme Points on the DC Load line are called as ~~cut~~ cut off point and saturation point which are obtained by putting two conditions.

① $I_C = 0$, $V_{CE} = V_{CC}$ (cut-off)

② ~~$V_{CC} = 0$~~, $I_C = \frac{V_{CC}}{R_E}$, $V_{CE} = 0$ (saturation

Example:-

Consider the voltage divider biasing ckt

The output voltage eq

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

($I_C \approx I_E$)

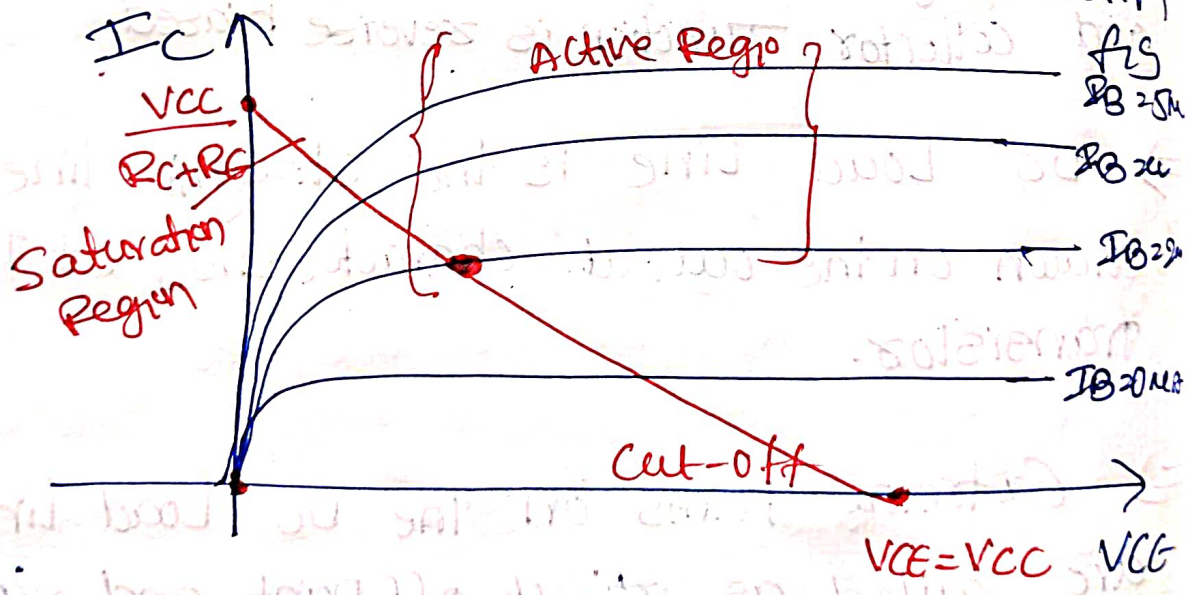
$$V_{CE} = V_{CC} - I_C [R_C + R_E]$$

DC Load Line:-

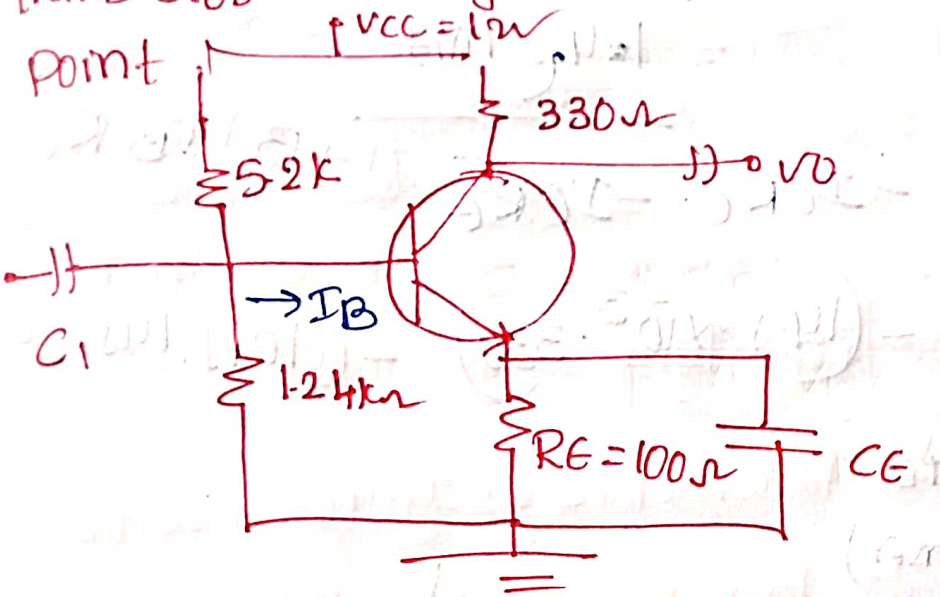
① $I_C = 0$, $V_{CE} = V_{CC}$ (Cut-off)

② $I_C = \frac{V_{CC}}{R_C + R_E}$, $V_{CE} = 0$ (Saturation)

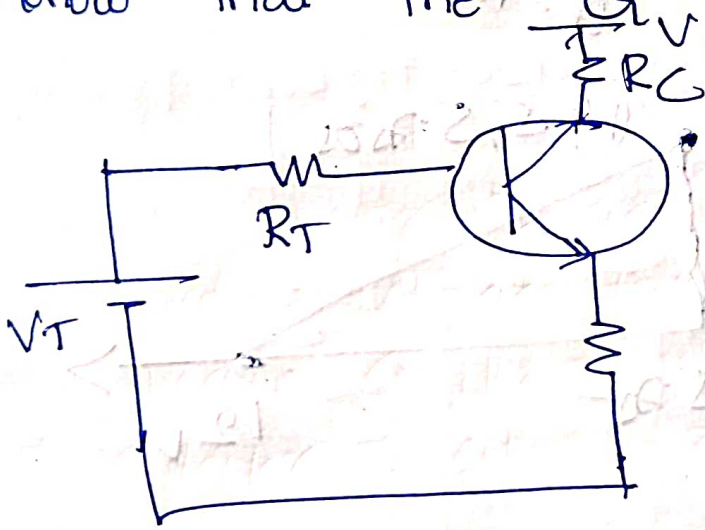
The O/P characteristic curve as shown in fig



(P1) Draw the d.c Load Line for the following transistor configuration. obtain the quiescent point



we know that the Q ckt is.



$$\therefore V_T = \left(\frac{R_2}{R_1+R_2}\right) \cdot V_{CC} = \left(\frac{1.24}{1.24+5.2}\right) \cdot 12 = 2.31\,V.$$

$$R_B = R_T = R_1 \| R_2 = \frac{5.2 \times 1.24}{5.2+1.24} = 1K.$$

Apply KVL to the base ckt.

$$-V_T + I_B R_B + V_{BE} + I_E R_E = 0$$

$$I_B = \frac{V_T - V_{BE}}{R_B + (1+\beta)R_E} = \frac{2.31 - 0.7}{1K + (1+100)100} = 145\,MA$$

$I_C = \beta I_B = 100 \cdot 145\,\mu A$

$= 14.5\ mA$

$V_{CE} = V_{CC} - I_C R_C - I_E R_E \quad (I_E = (1+\beta) I_B)$

$= 12 - (14.5 \times 10^{-3} \cdot 330) - ((101) \cdot 145 \cdot 10^{-6} \cdot 100)$

$= 5.20$