第一届全国大学生计算机系统能力培养大赛（龙芯杯）

西北工业大学计算机学院一队

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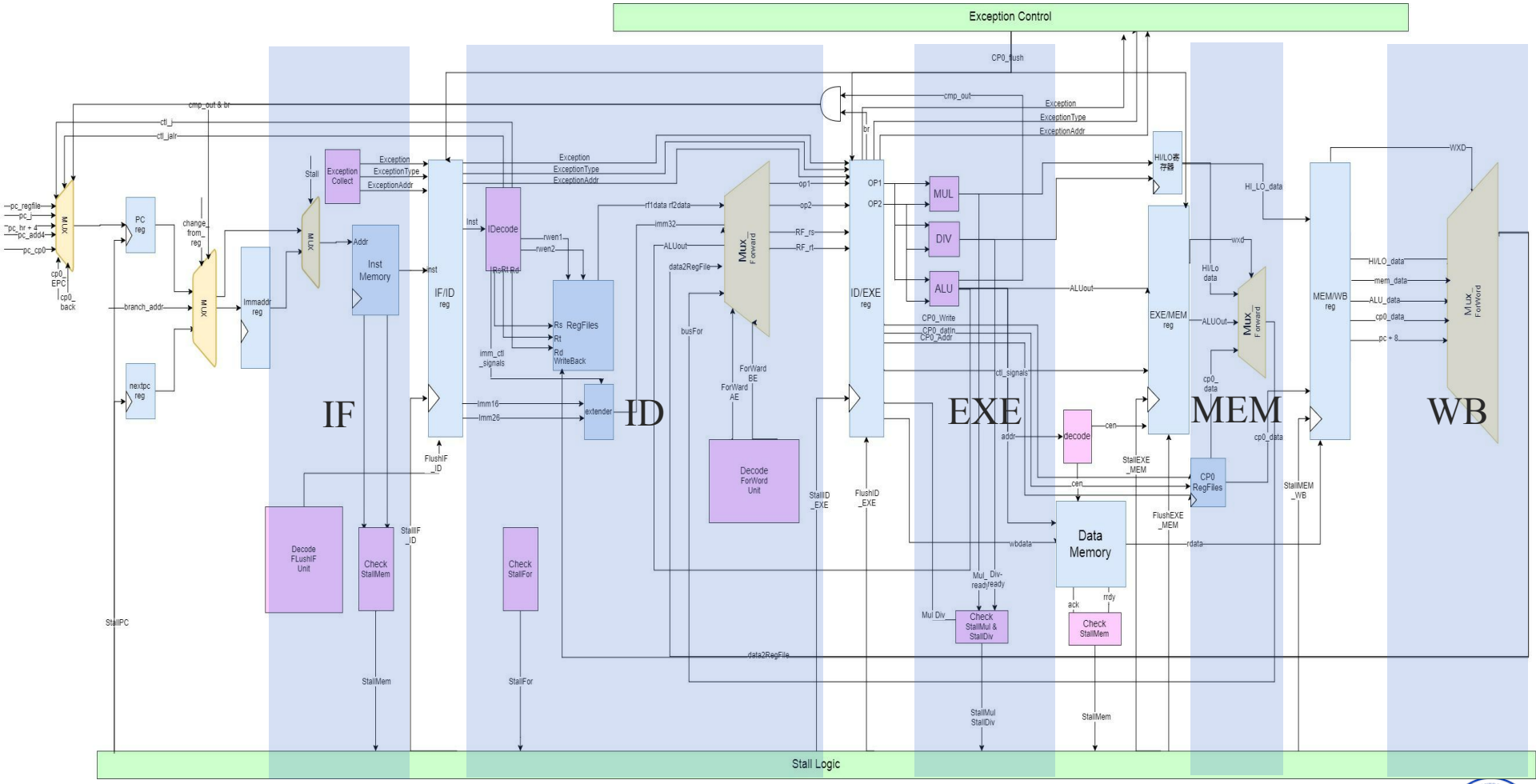
Outline

1. Single-issue CPU design and optimization
2. Dual-issue CPU design
3. SoC design and verification
4. Conclusion

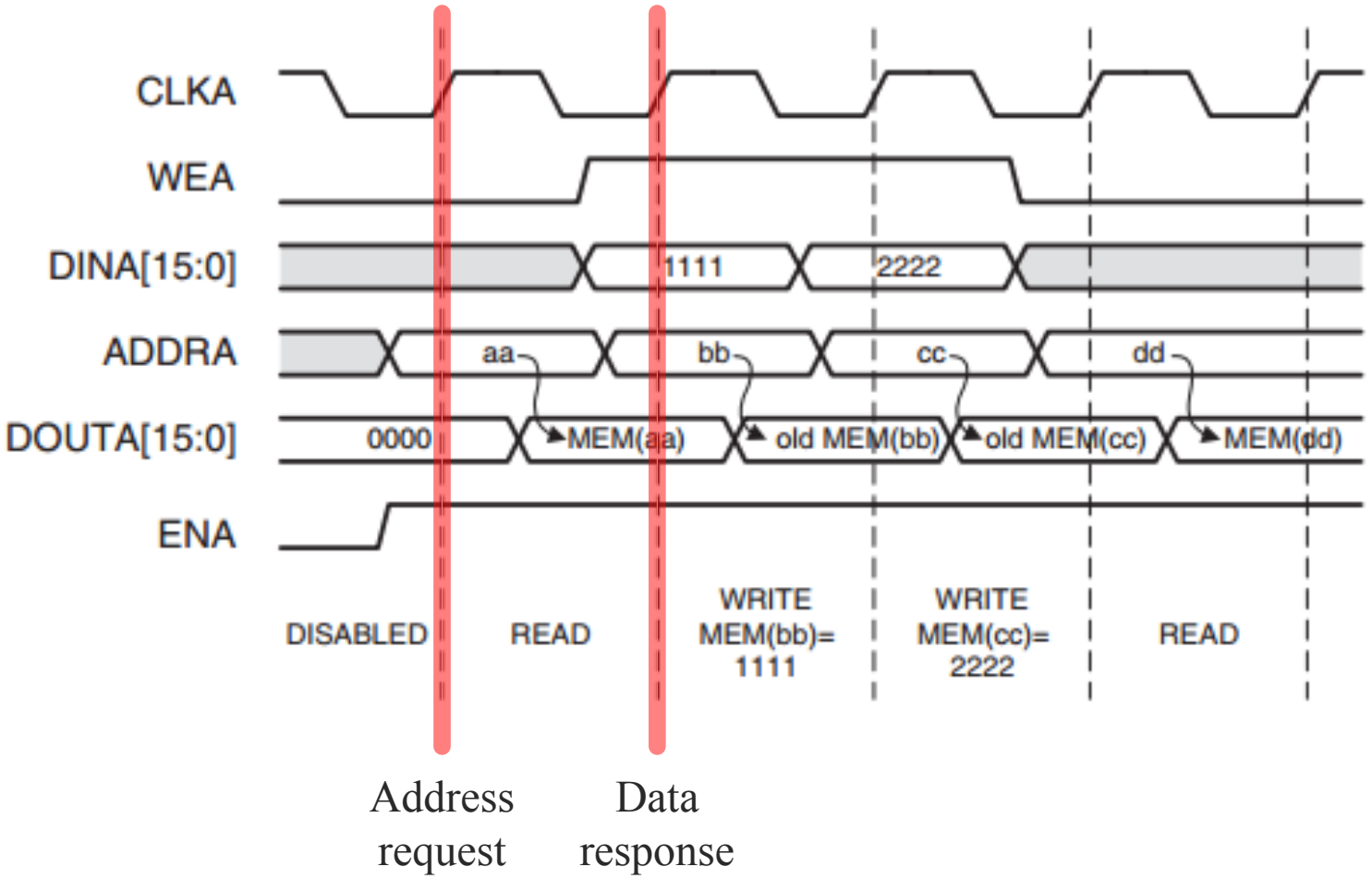
1. Single-issue CPU design and optimization

- Based on the 5-stage pipeline from the PH&HP book.

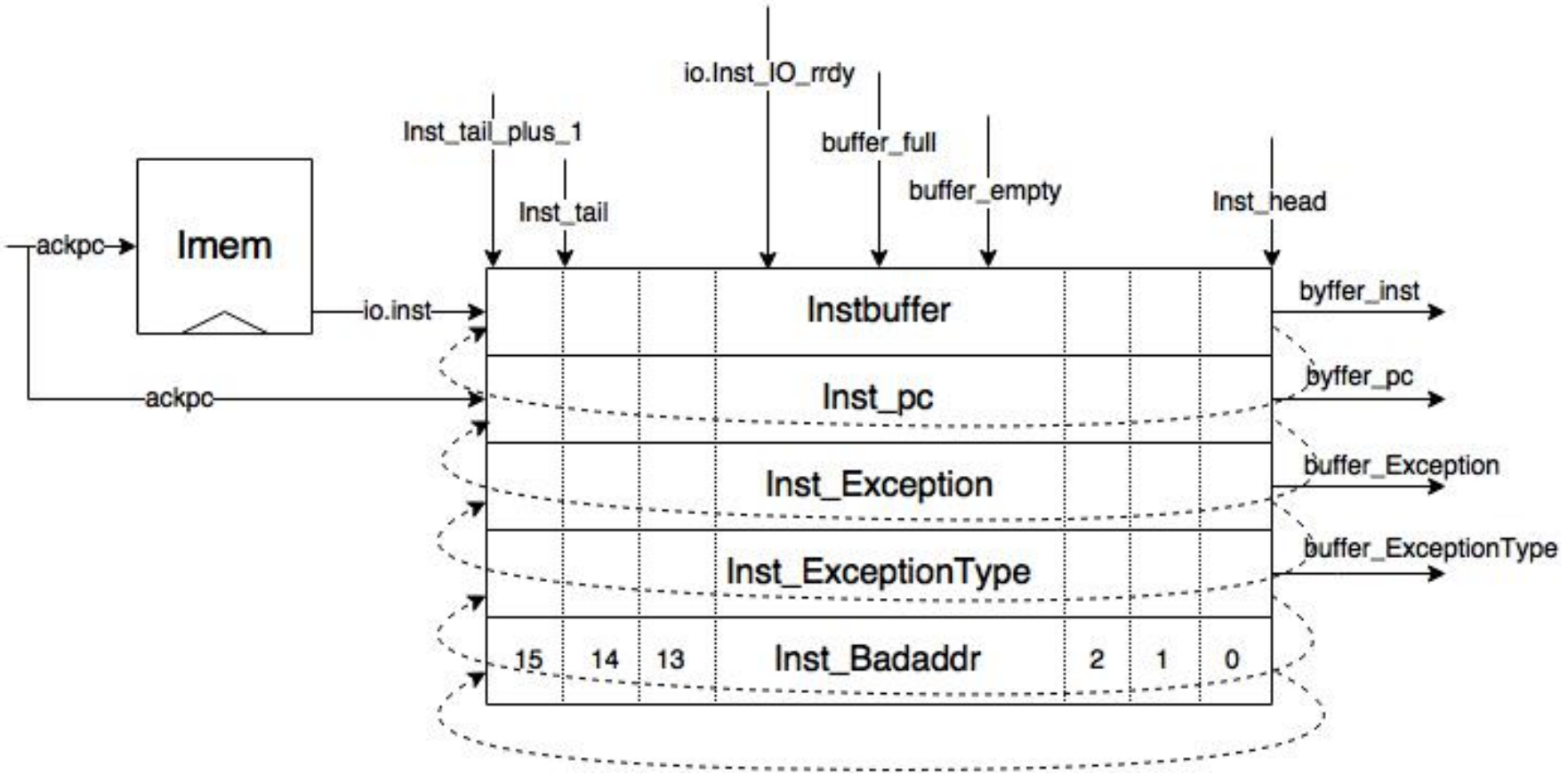


1.1 Instruction Prefetch Buffer

BRAM access timing



Single Instruction Register→Instruction Buffer



1.2 Hazard Detection and Solution

- Data Hazard

  ——Forward and Stall

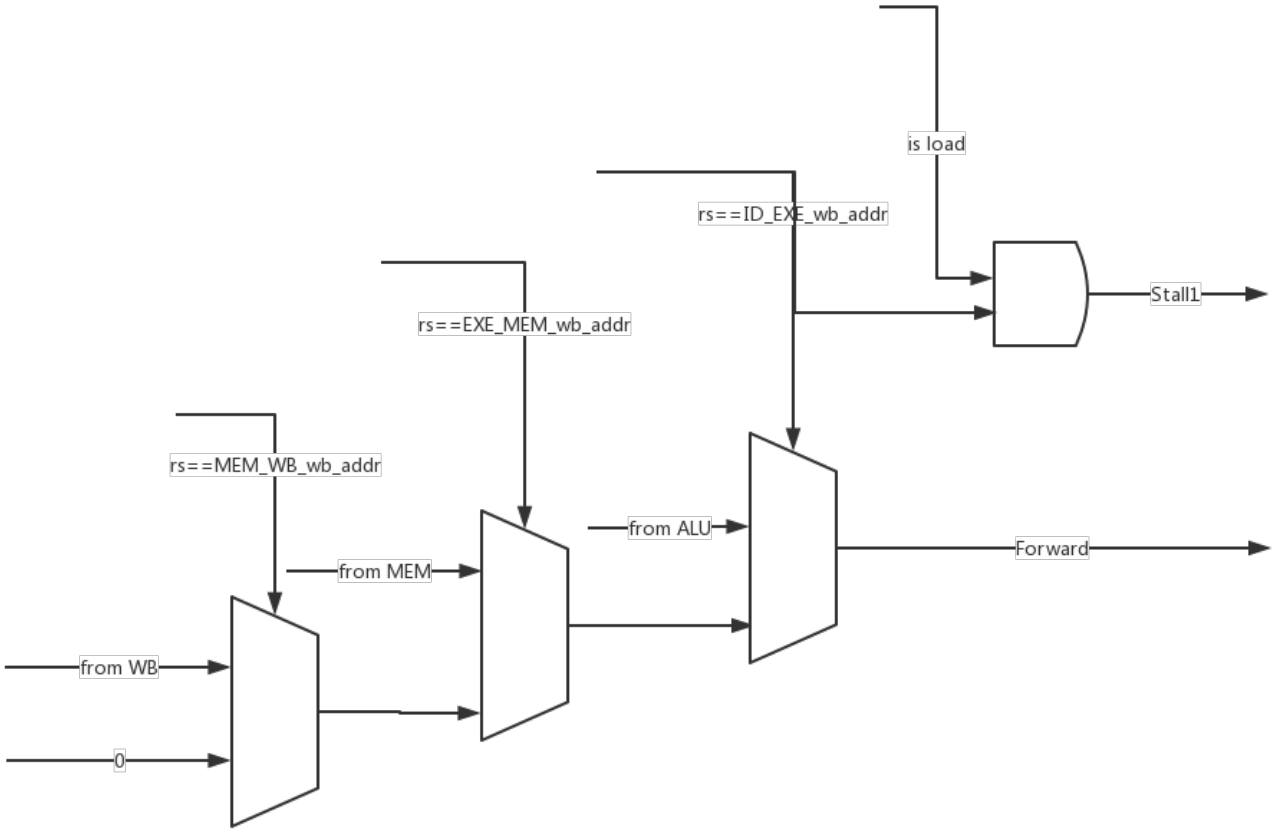
- Control Hazard

  ——Delay Slot and Flush

- (No Structure Hazard)

Data Hazard: Read After Write

- Full Forwarding and Stalling

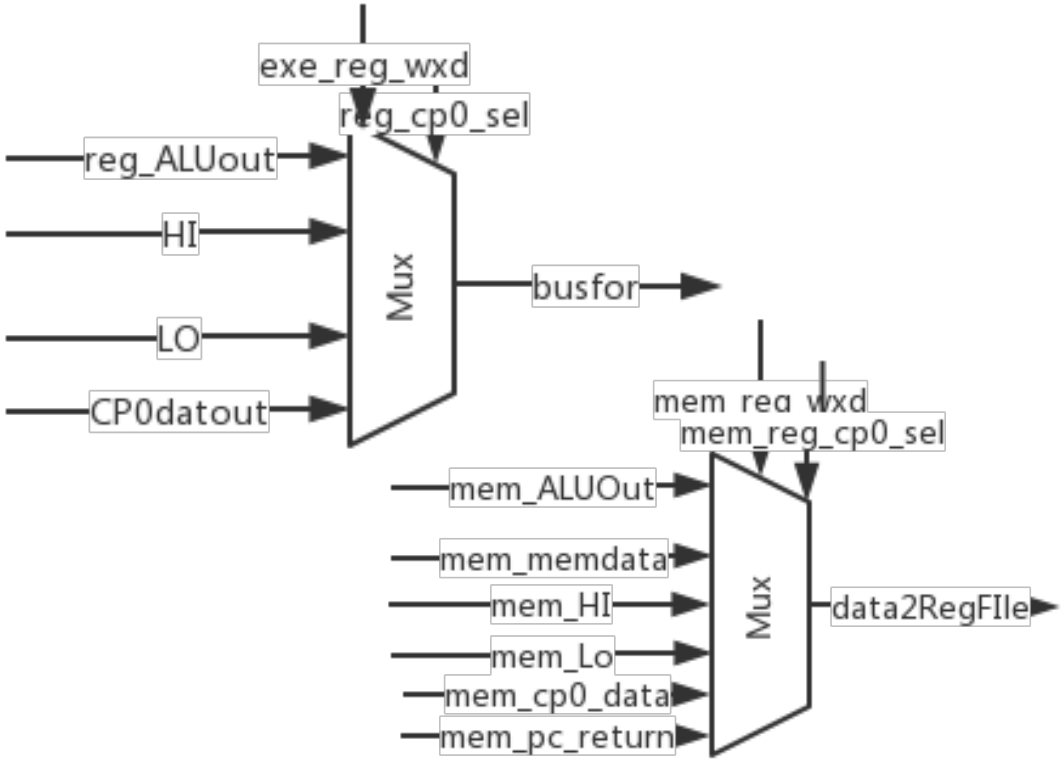


Data Hazard Analysis

From ALU_out

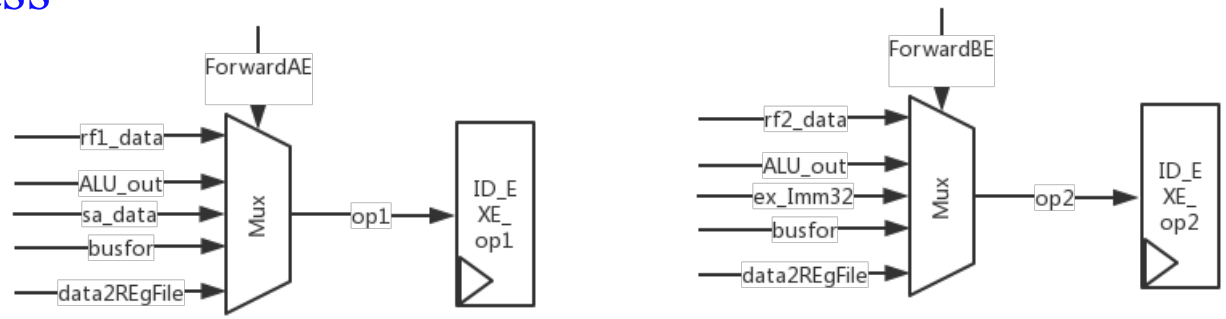
From busFor

From data2RegFile

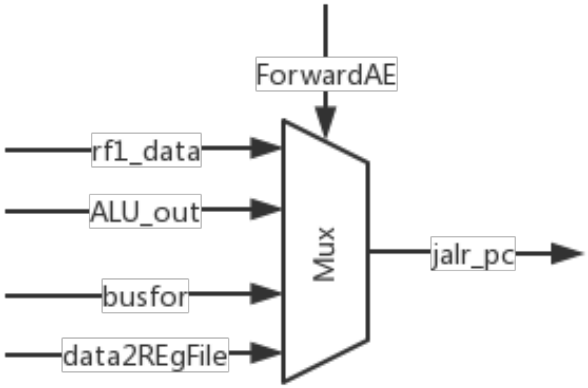


Data Hazard Bypass

ID bypass

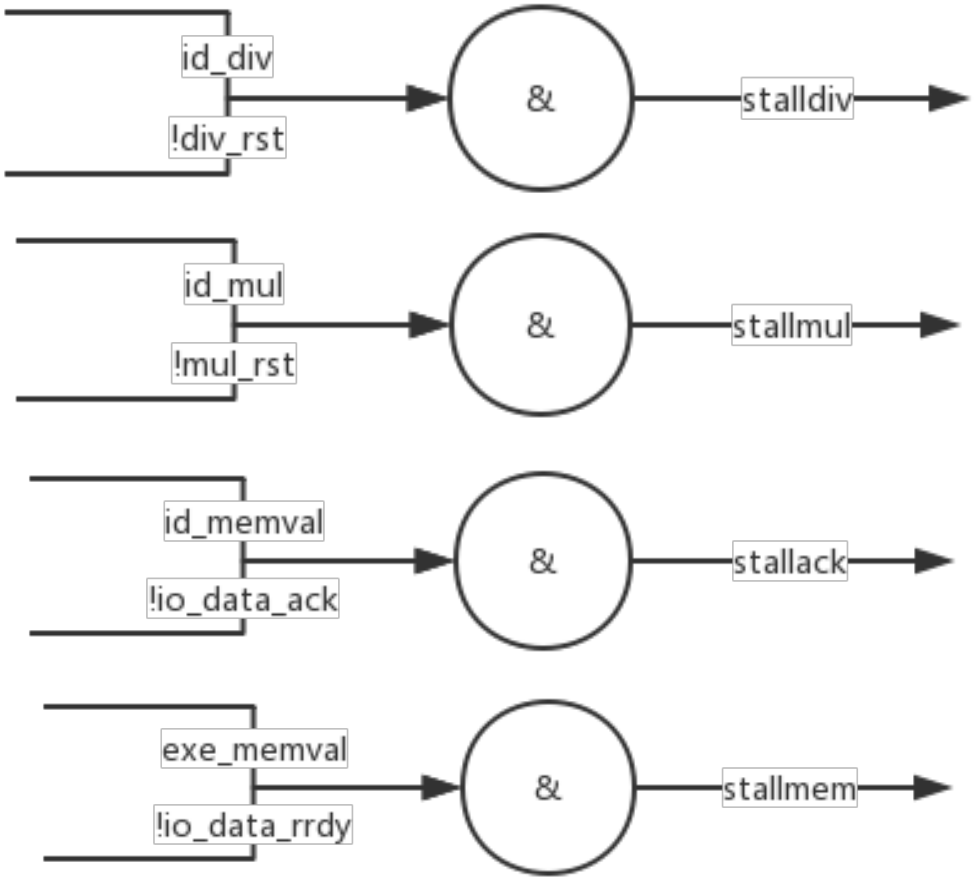


PC bypass



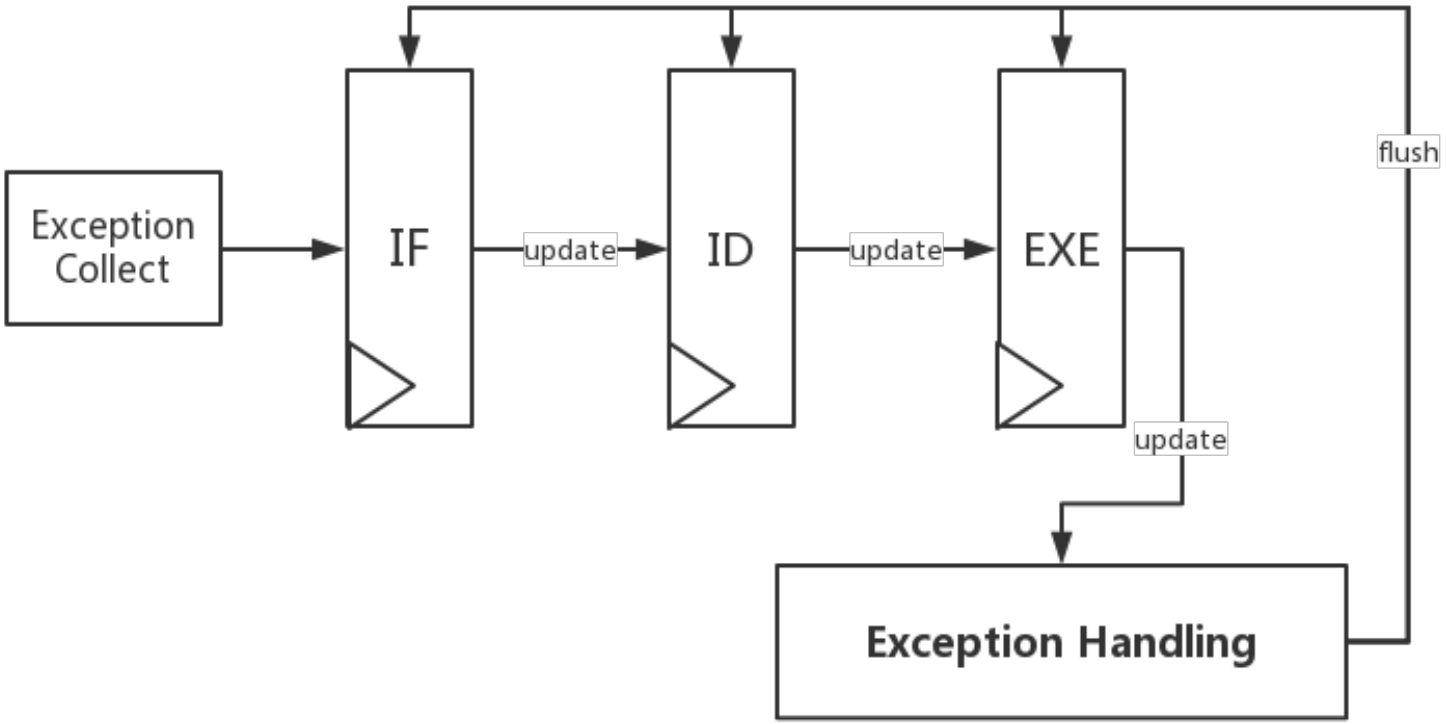
Stall Generation

Stalldiv、Stallmul、Stallack (EXE) and Stallmem (MEM)



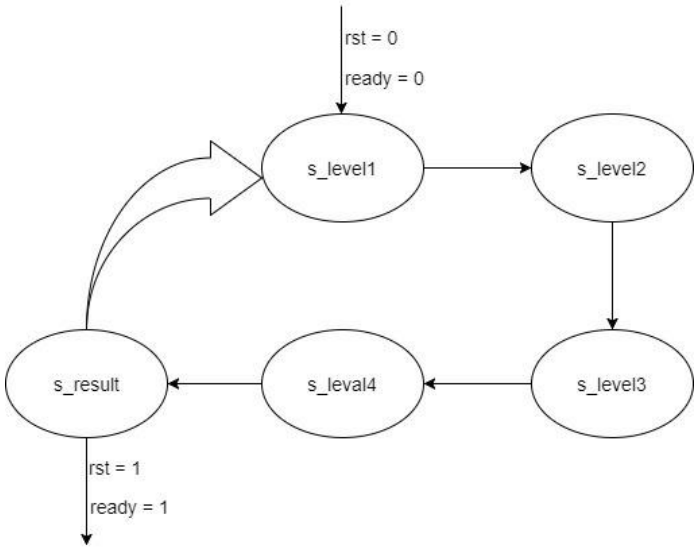
1.3 Exception Checking and Handling

- Design of **Accurate** Exception



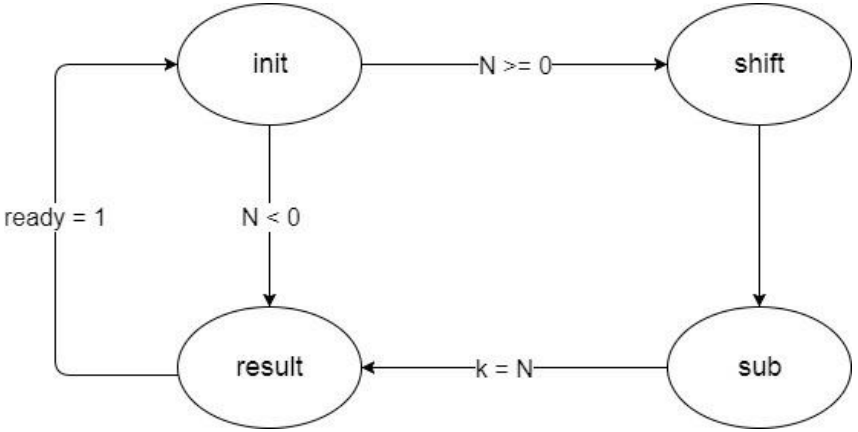
1.4 MUL and DIV Implementation

Booth MUL



5 cycles

Fast Signed Integer Division[*]

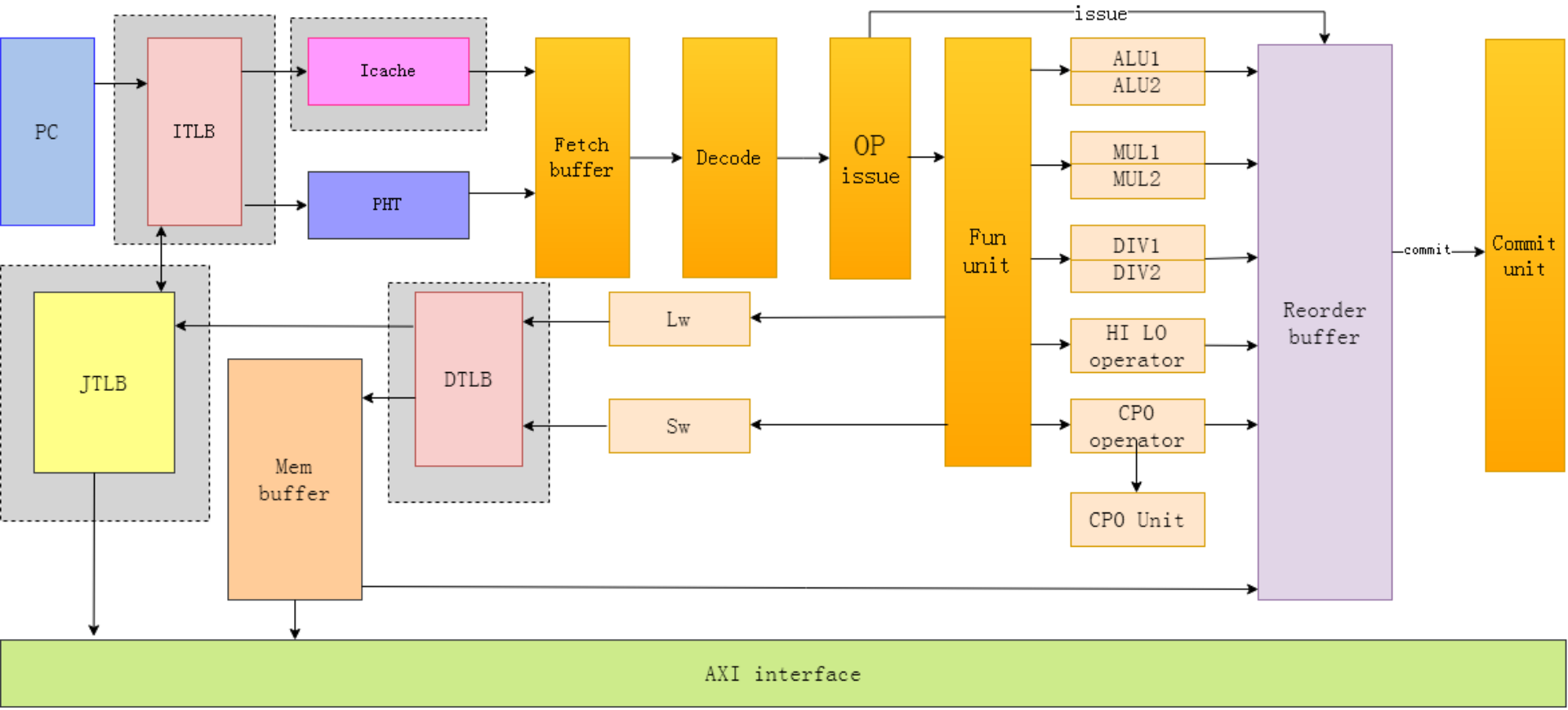


3.94 cycles on average

[*]快速有符号除法算法及其低成本实现（2015.04)

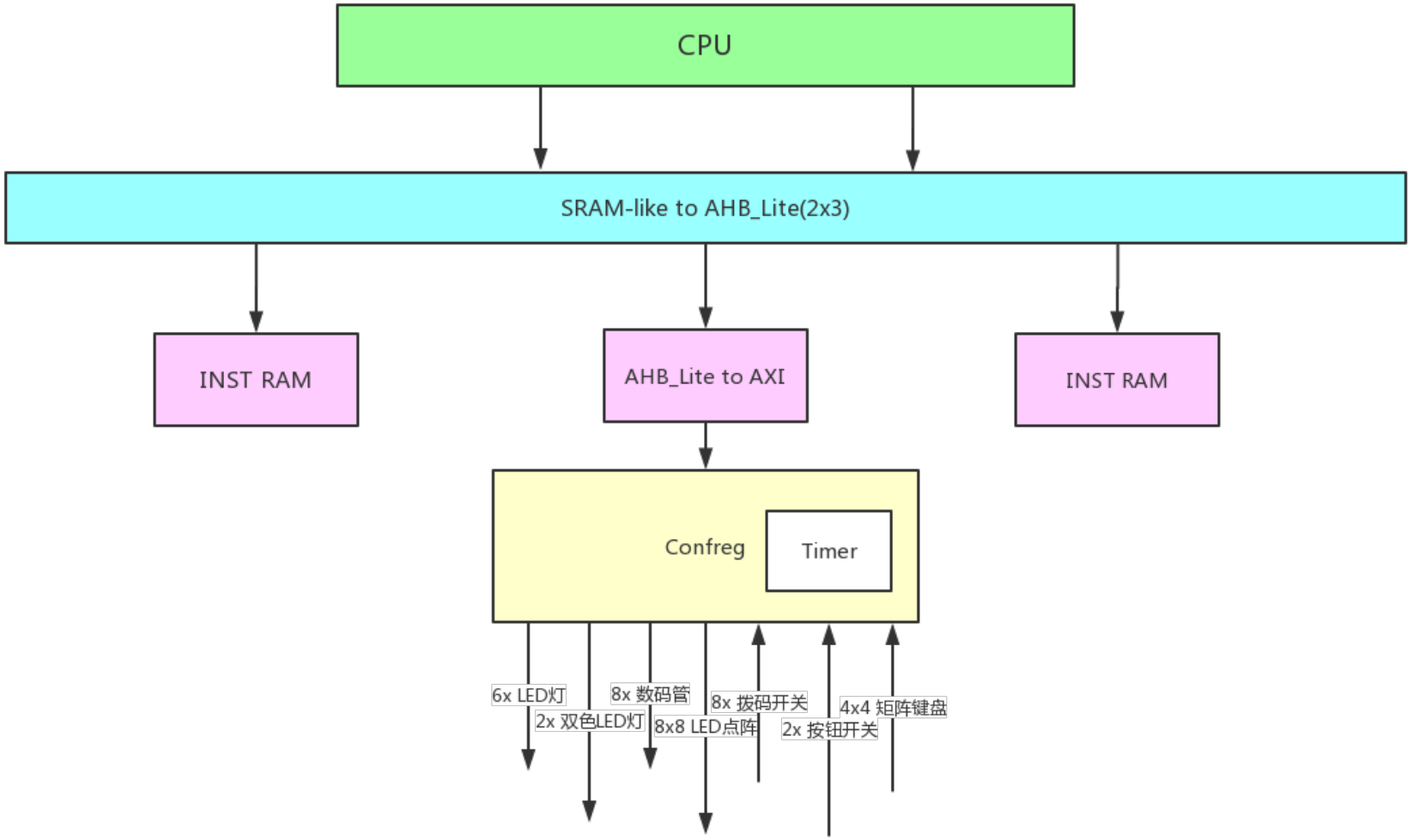
2. Dual-issue CPU Design

- Scoreboard with multi execution unit.



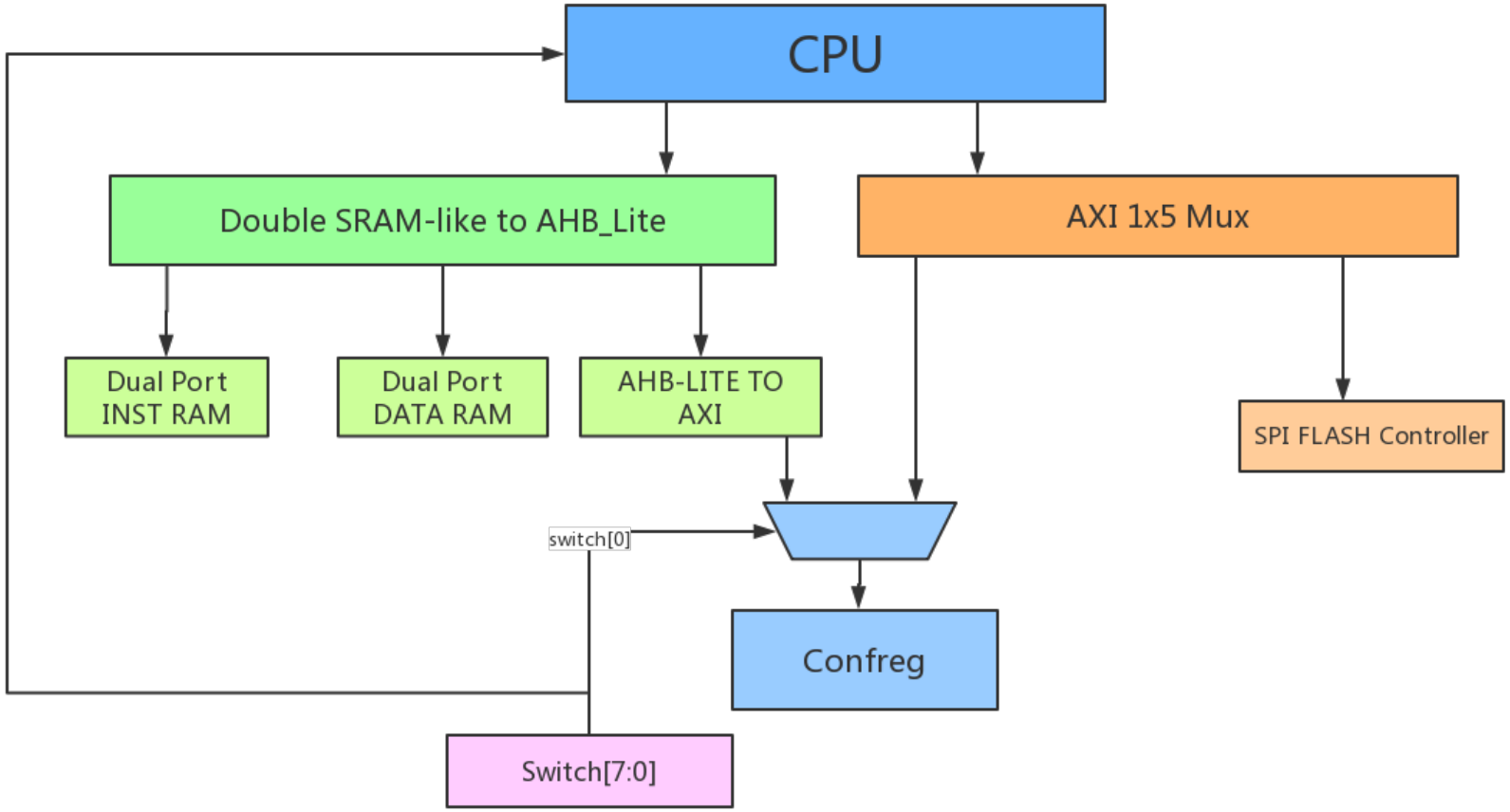
3. SoC Design and Verification

- Base on the SoC Lite architecture.



Switch between SoC Lite and SoC Up

- Support performance test and SoC test with single FPGA configuration.



Conclusion

Design	Period	IPC	Func. Test	Perf. Test
Single-issue	23.0ns	1.205	pass	pass
Dual-issue	14.7 ns	-	pass	-

Thanks and Question?