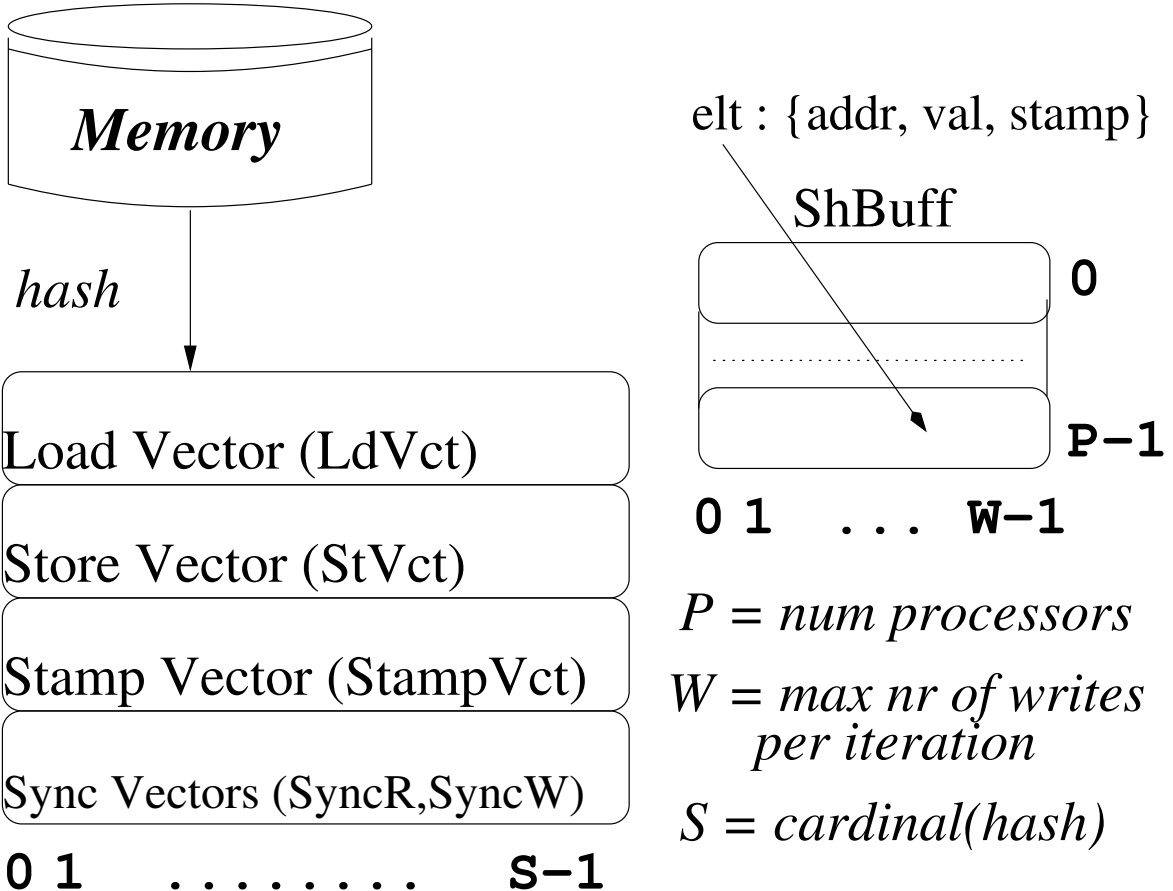
Memory
hash
Load Vector (LdVct)
Store Vector (StVct)
Stamp Vector (StampVct)
Sync Vectors (SyncR,SyncW)
0 1 ..... S-1
elt : {addr, val, stamp}
ShBuff
0
P-1
0 1 ... W-1
P = num processors
W = max nr of writes per iteration
S = cardinal(hash)