	T1	T2	T3	CACHE STATES C1 C2 C3	Comments
t0			$L^3(A)a_0$	NIC NIC SHA	Miss in C3; APT1
t1	$S^1(A)a_1$			NIC NIC SHA	
t2			$S^3(A)a_2$	NIC NIC SHA	
t3	$L^1(A)a_1$			NIC NIC SHA	
t4		$S^2(A)a_3$		NIC NIC SHA	
t5			$L^3(A)a_2$	NIC NIC SHA	
t6	$S^1(A)a_4$			NIC NIC SHA	
t7		$L^2(A)a_3$		NIC NIC SHA	
t8	$L^1(A)a_4$			NIC NIC SHA	
t9		$L^2(A)a_3$		NIC NIC SHA	
t10	$WB^1(A)a_4$			MOD NIC INV	Miss in C1; APT2
t11	$L^1(A)a_4$			MOD NIC INV	Hit in C1
t12		$S^2(A)a_5$		DTY NIC INV	
t13		$WB^2(A)a_5$		INV DTY INV	Miss in C2; APT3
t14	$L^1(A)a_5$			SHA SHA INV	Miss in C1; APT4
t15			$L^3(A)a_2$	SHA SHA INV	
t16			$WB^3(A)a_2$	INV INV MOD	Miss in C3; APT5
t17	$L^1(A)a_2$			SHA INV SHA	Miss in C1; APT6
t18			$L^3(A)a_2$	SHA INV SHA	Hit in C3
t19		$L^2(A)a_2$		SHA SHA SHA	Miss in C2; APT7
t20		$S^2(A)a_6$		SHA SHA SHA	
t21		$L^2(A)a_6$		SHA SHA SHA	
t22		$WB^2(A)a_6$		INV MOD INV	Upgrade in C2; APT8