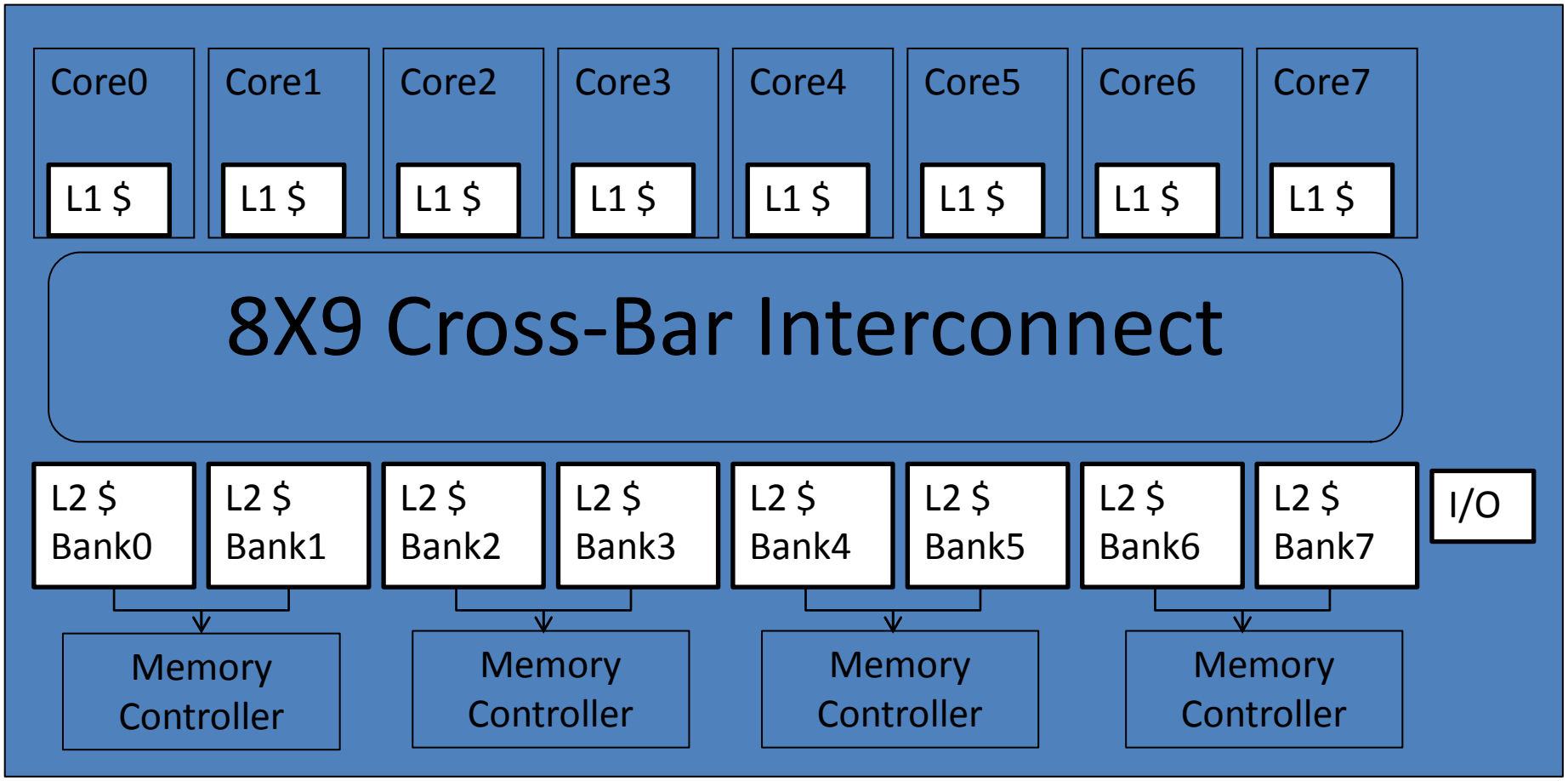
Core0
Core1
Core2
Core3
Core4
Core5
Core6
Core7
L1 $
L1 $
L1 $
L1 $
L1 $
L1 $
L1 $
L1 $
8X9 Cross-Bar Interconnect
L2 $ Bank0
L2 $ Bank1
L2 $ Bank2
L2 $ Bank3
L2 $ Bank4
L2 $ Bank5
L2 $ Bank6
L2 $ Bank7
I/O
Memory Controller
Memory Controller
Memory Controller
Memory Controller