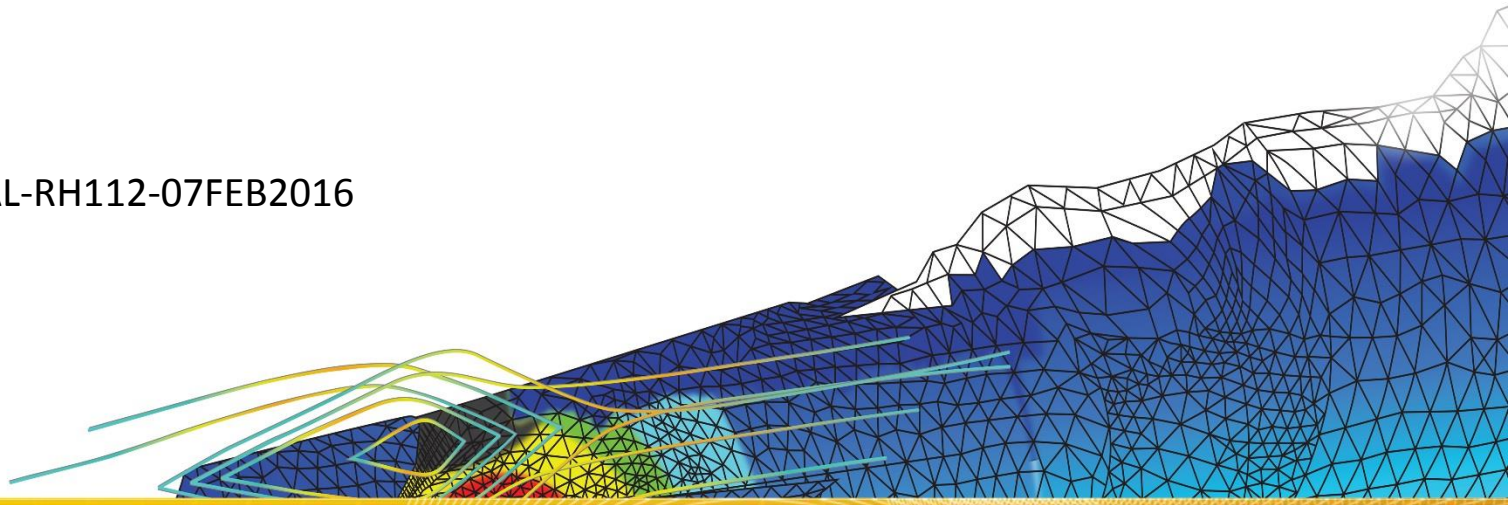
Average Power Calculation & Static Analysis

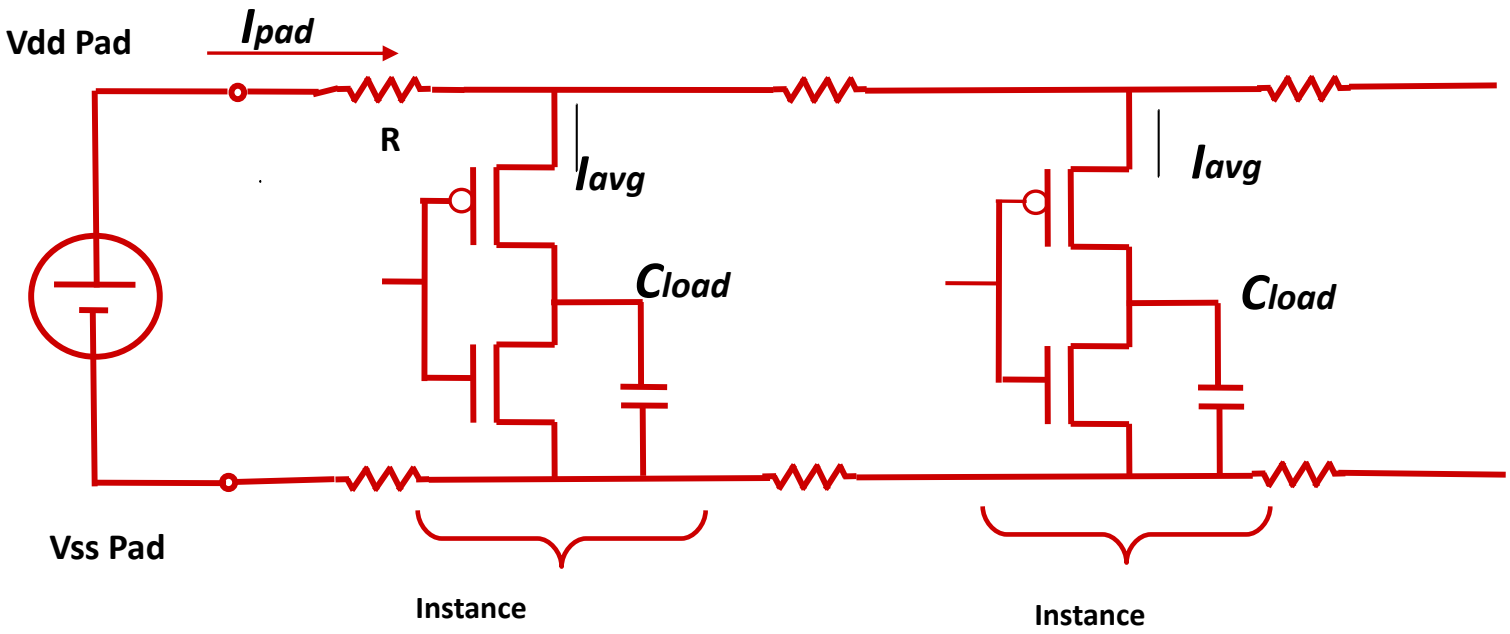
VERSION: V5.2-AL-RH112-07FEB2016



Agenda

- Static Analysis Theory
- RedHawk Static IR/EM Analysis Flow
- Analysis of Results
- Conclusions

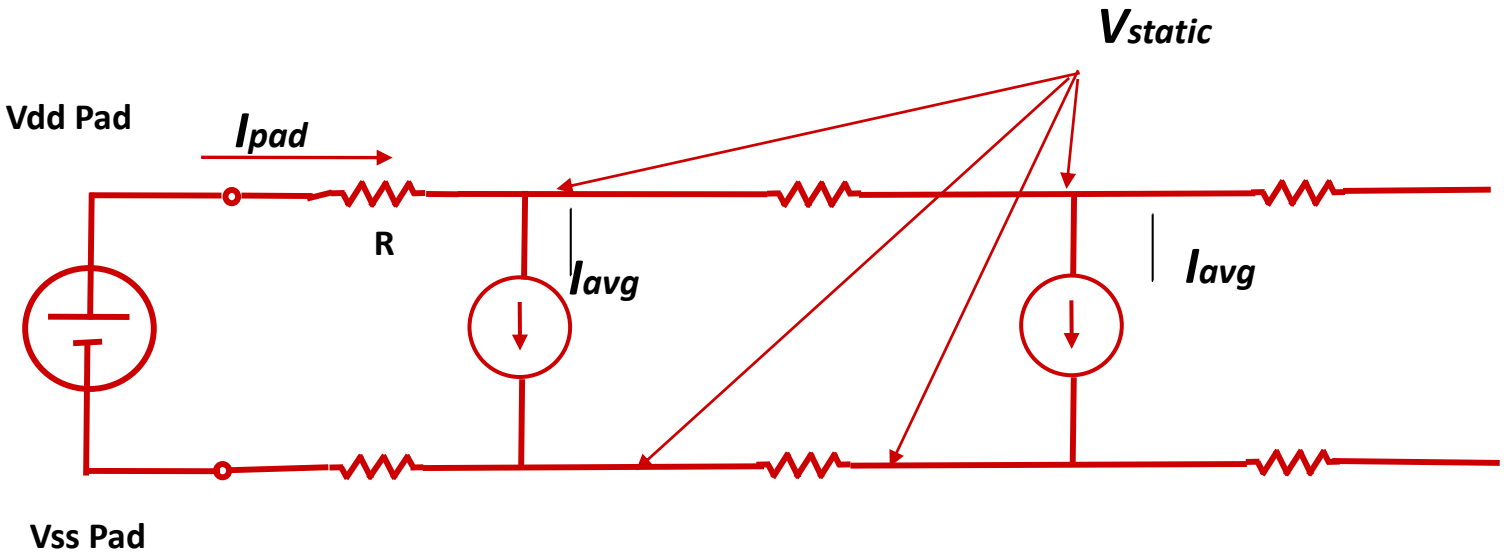
Static Voltage Drop Background



- On-chip power/ground network → mesh of resistors
- Instances →DC current sources

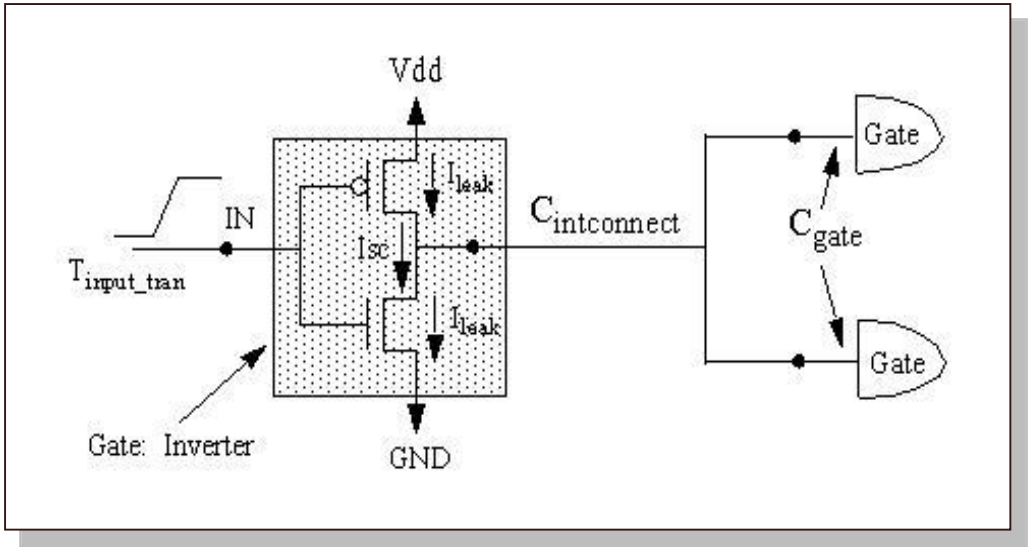
Static Voltage Drop on P/G Network

- Average current is calculated for each instance
- V_{static} is computed at every node (Ohm's law ...)
- Wire / via electromigration (*EM*) is post-processed from static current density



Gate-level Static Power and DC Current

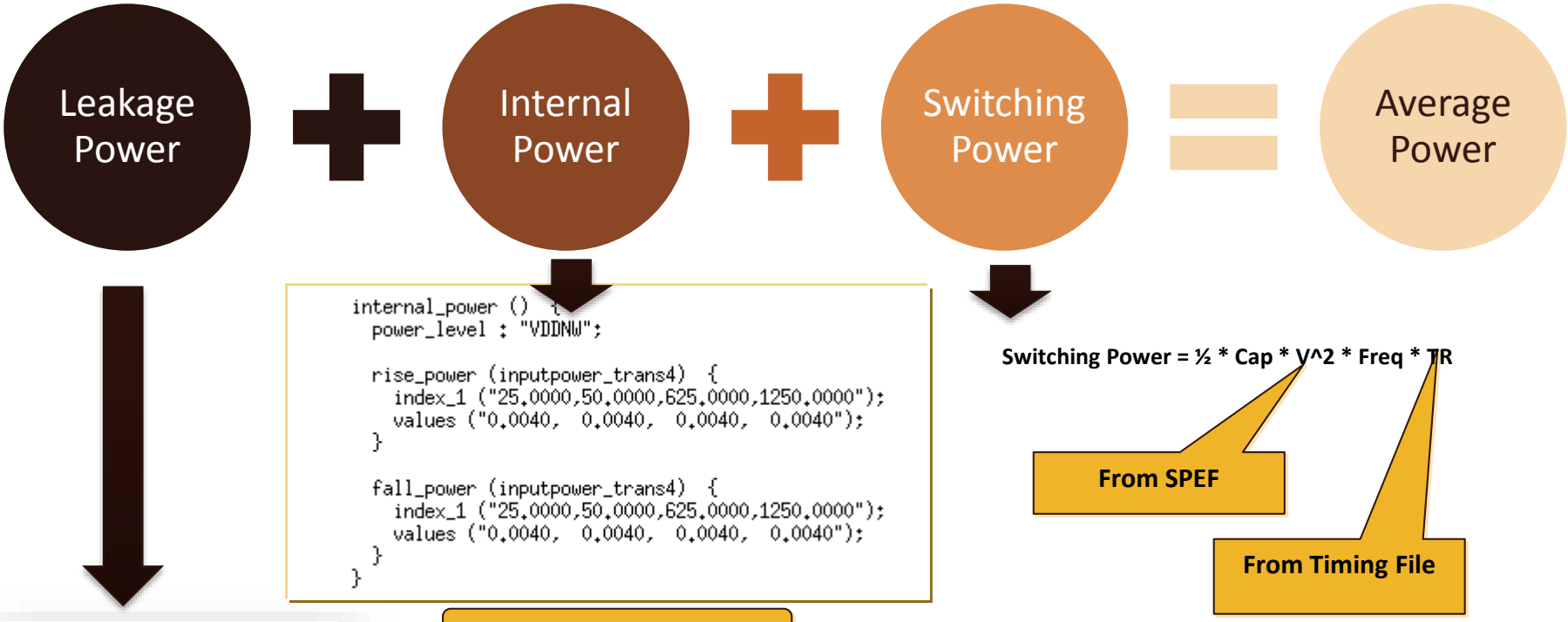
$$P_{avg} = P_{leakage} + P_{internal} + P_{switching}$$



Gate Active Average Power is

- **function of input slew, output load (.lib power tables)**
- **linearly proportional to frequency and toggle rate**

Gate-level Average Power Calculation

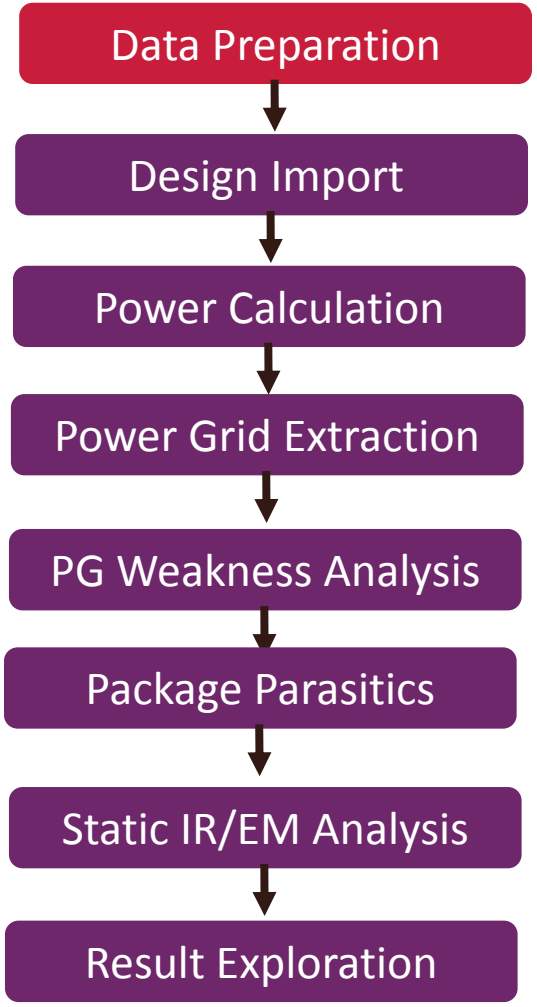


Internal Power = Internal Energy(in .lib) * Freq * TR

P(total) = P(Leakage) + ½ * (Internal-energy * Freq * TR) + ½ * C * V^2 * Freq * TR

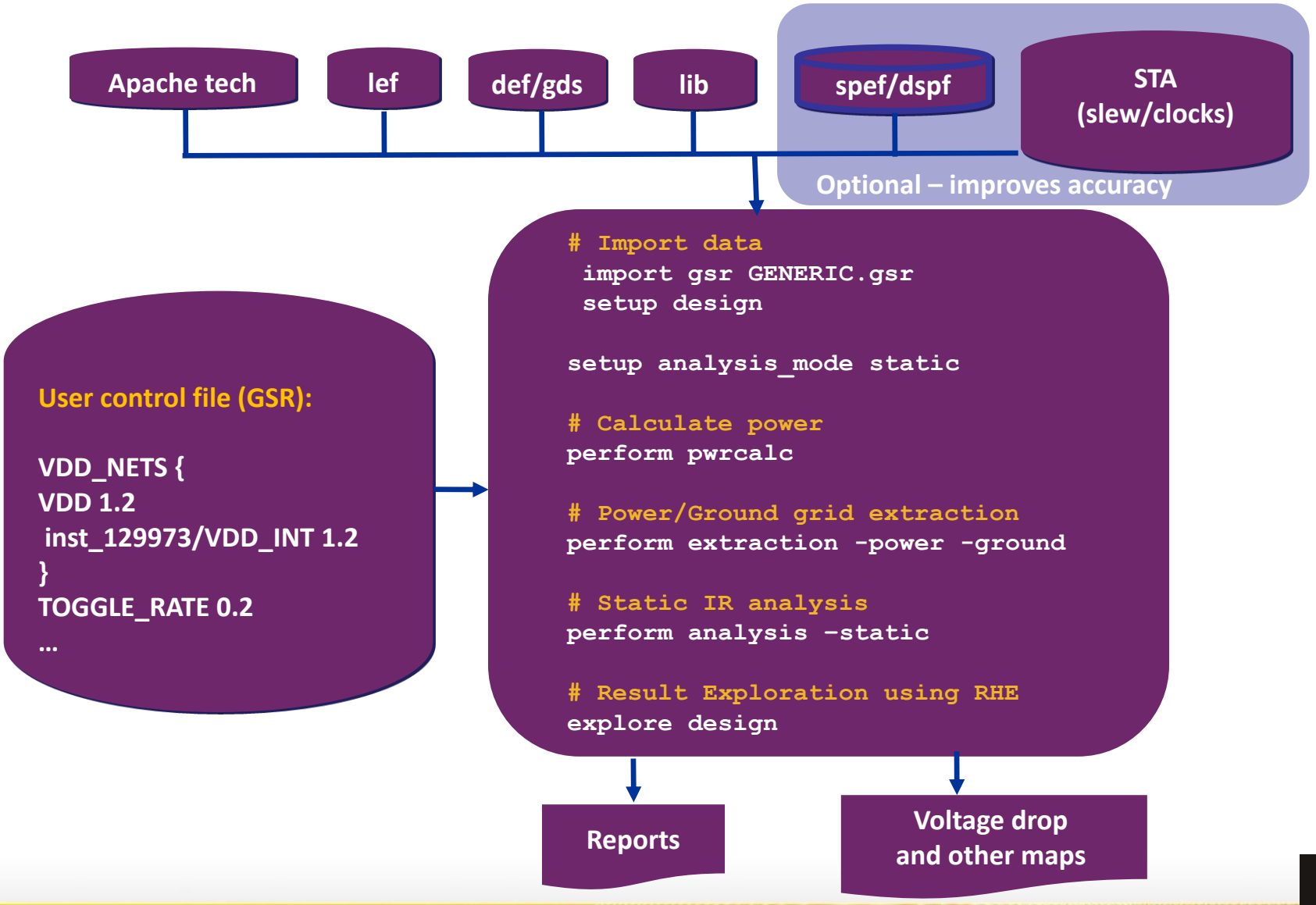
REDHAWK STATIC IR/EM ANALYSIS FLOW

Data Preparation

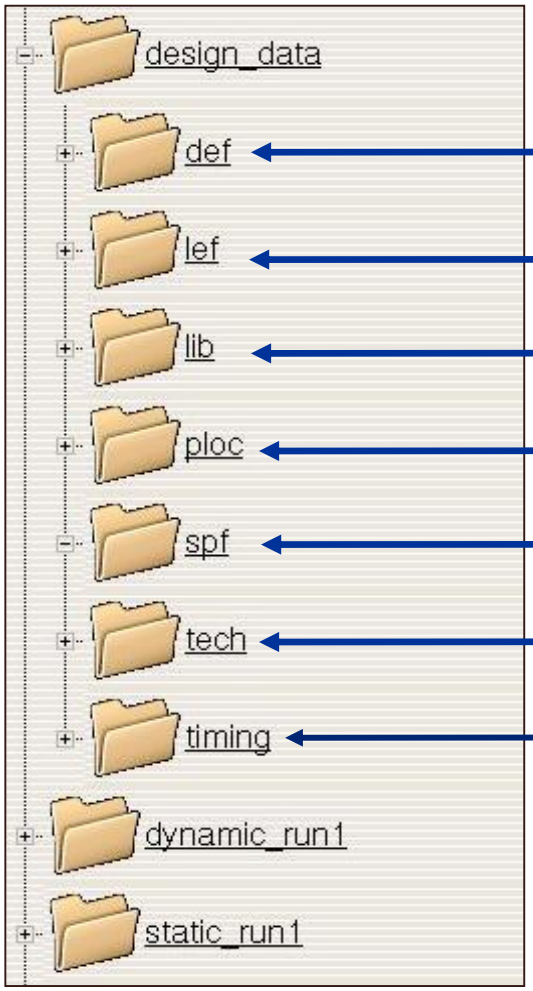


- **Copying the training tarball**
- **Creating GSR and run command file**
- **Setting up the environment**
- **Reviewing the user inputs**

Static Analysis Flow and Required Data



Recommended Directory Structure



- def: Cell placement + power grid
- lef: Tech section and all macros used in design
- lib: For power calculation
- ploc: Location of ideal pwr/gnd sources
- spf: Signal nets parasitics (optional)
- tech: Apache technology file
- timing: Instance Slew/Frequency + Clocks (optional for static)
- dynamic_run1, static_run1: Run directories

Setting Up The Training Testcase

- cp –R <original_path>/GENERIC_tutorial.tar.gz
- tar –xvzf GENERIC_tutorial.tar.gz
- Follow the instructions in README to run static analysis

Step 1: Data Preparation

- cd GENERIC_tutorial/static_run
- Review the GSR and Command File
- source setup.csh : This will set APACHEROOT, PATH and LM_LICENSE_FILE.

GSR File Overview

```
TECH_FILE ads.tech

LIB_FILES {
<path to lib file>
<path to lib directory> (all *.lib files in dir)
<path to custom lib file> custom
}

LEF_FILES {
<lef file path>/name1.lef << tech definition
<lef file path>/name2.lef
}

DEF_FILES {
<def file path>/name1.def
<def file path>/name2.def TOP < last one to be TOP DEF
}
```

OR

```
LIB_FILES {
<design>.libs
}
```

OR

```
LEF_FILES {
<design>.lefs
}
```

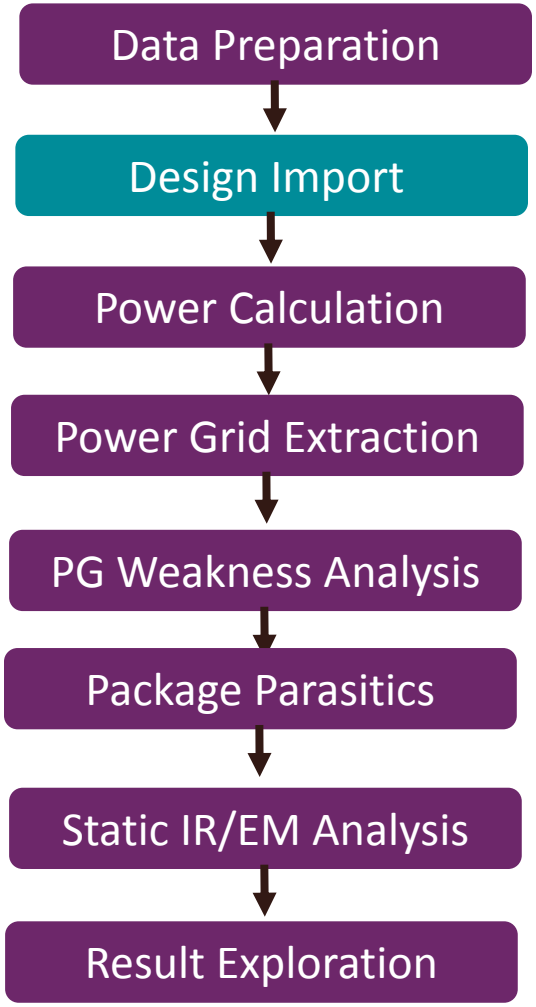
OR

```
DEF_FILES {
<design>.defs
}
```

Static Run Command File

```
# Import data
import gsr GENERIC.gsr
setup design
setup analysis_mode static

# Calculate power
perform pwrcalc

# Power/Ground grid extraction
perform extraction -power -ground

# Lumped resistance (in Ohms)
# for package, wirebond and pads
setup package -power -r 0.005 -l 2.5 -c 5
setup package -ground -r 0.005 -l 2.5 -c 5
setup wirebond -power -r 0.01 -l 2.2 -c 1.42
setup wirebond -ground -r 0.05 -l 1.7 -c 0.2
setup pad -power -r 0.001
setup pad -ground -r 0.001

# Static IR analysis
perform analysis -static

# Result Exploration using RHE
explore design
```

Step 2: Importing the Design

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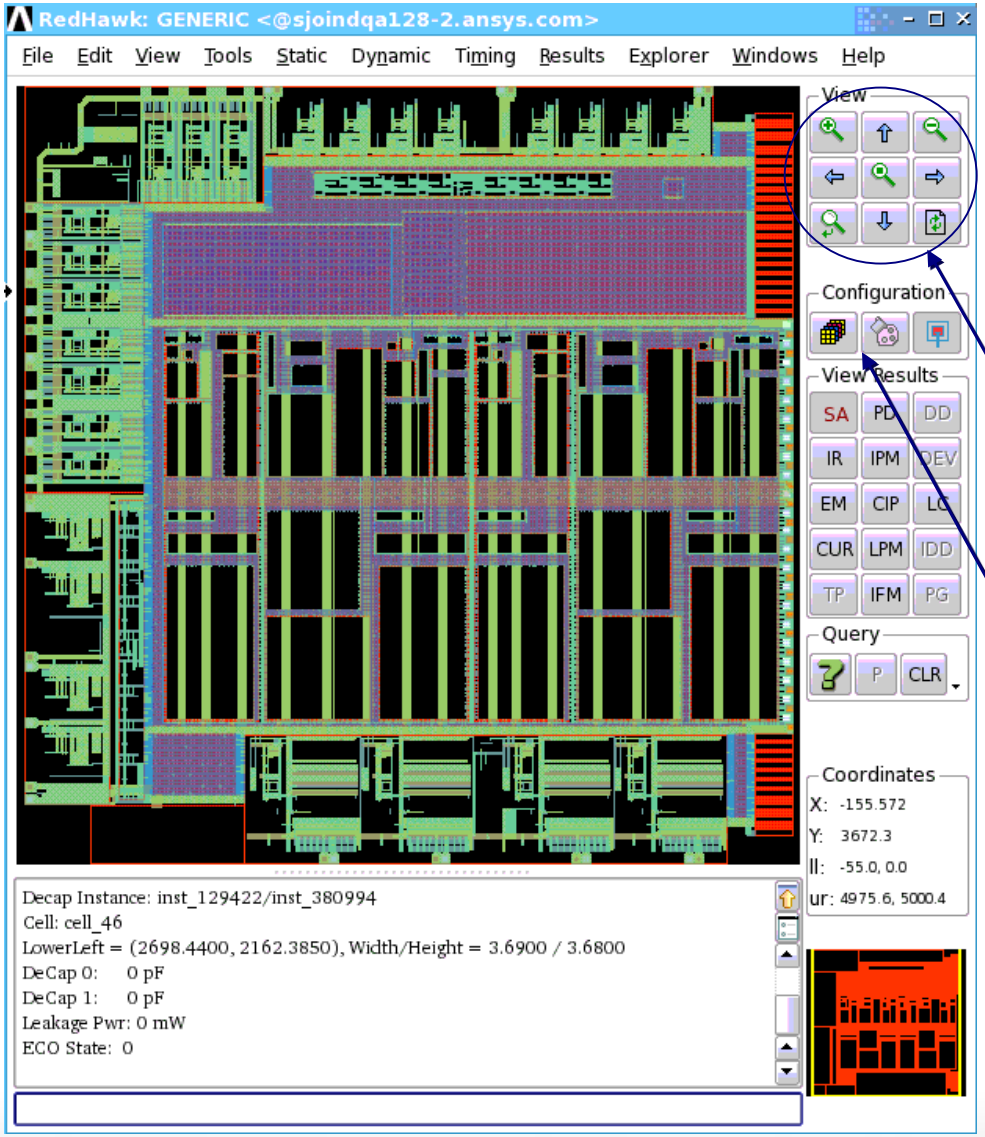
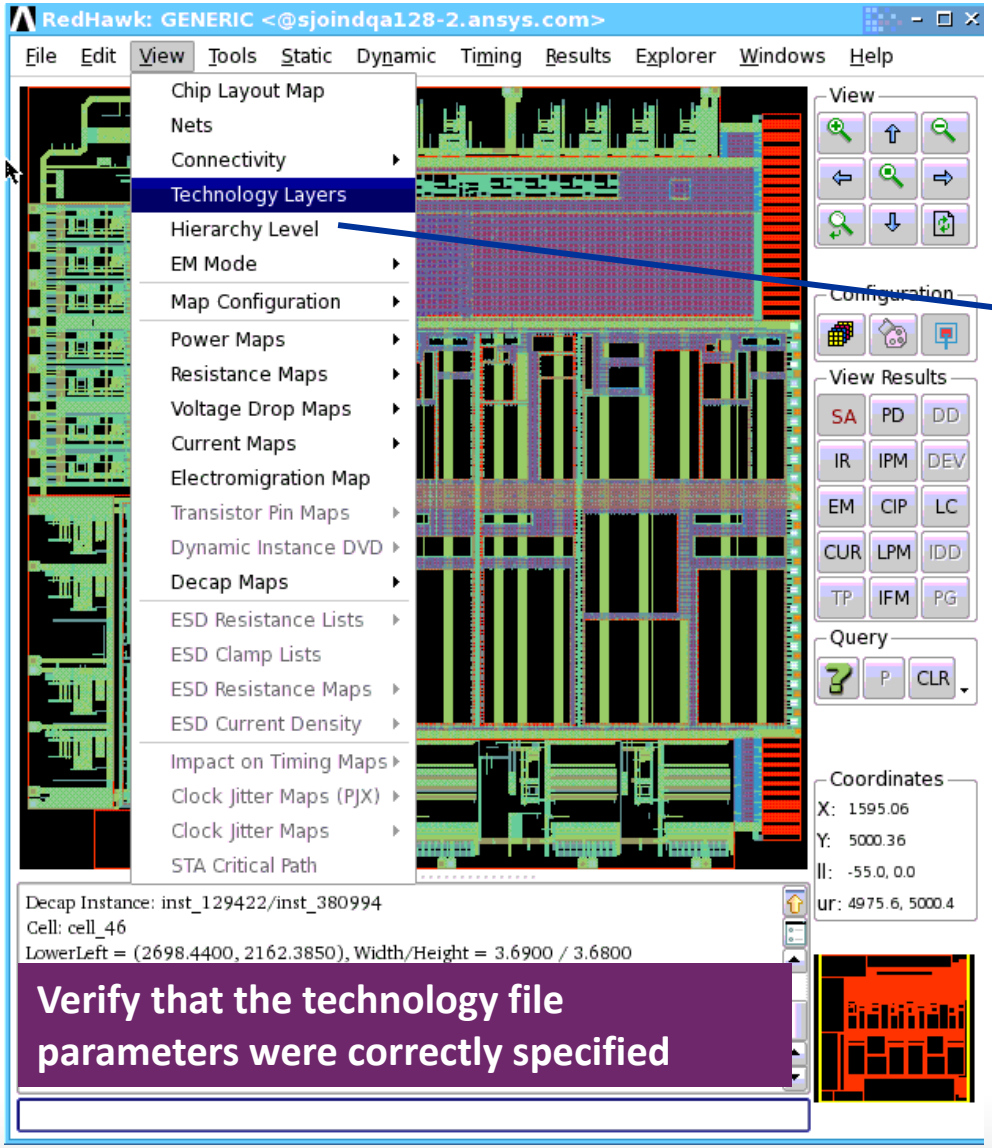
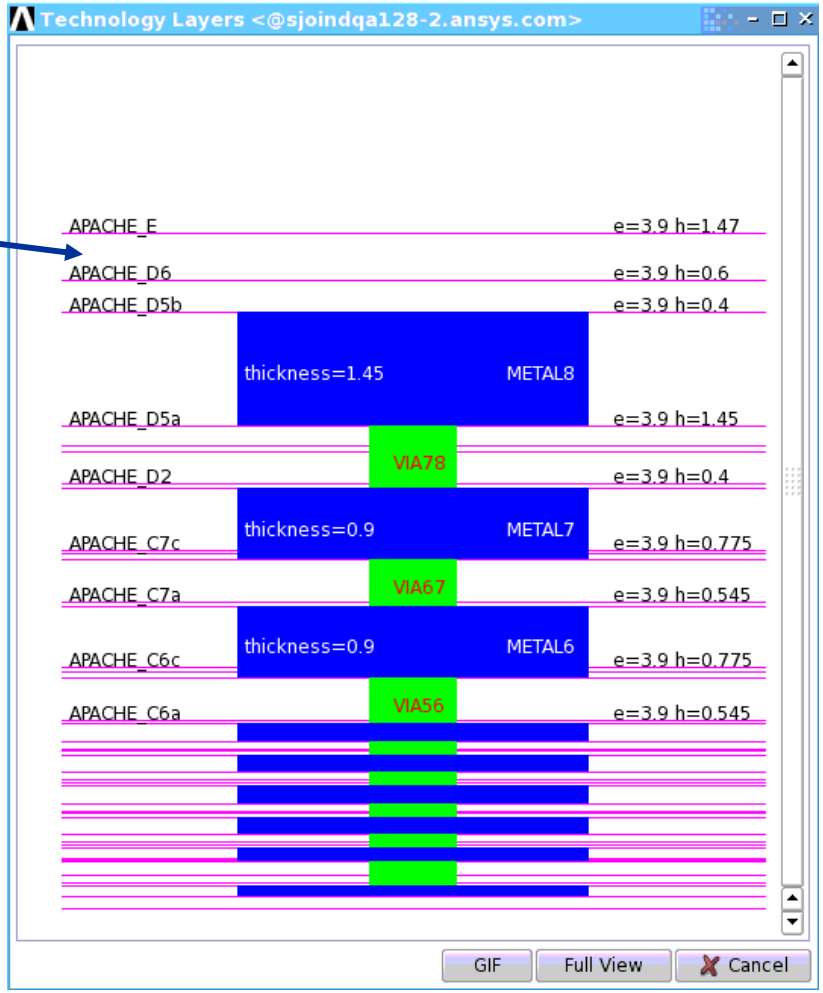
Starting RedHawk and Setting Up the Design



- **Start RedHawk**
- **Execute commands:**
  import gsr GENERIC.gsr
  setup design
- **Zoom in/out/scroll**
  - Drag Right mouse button (Zoom in)
- **Layer dialog box**
  - Turn on/off Layer/Instance
  - Fill/Outline

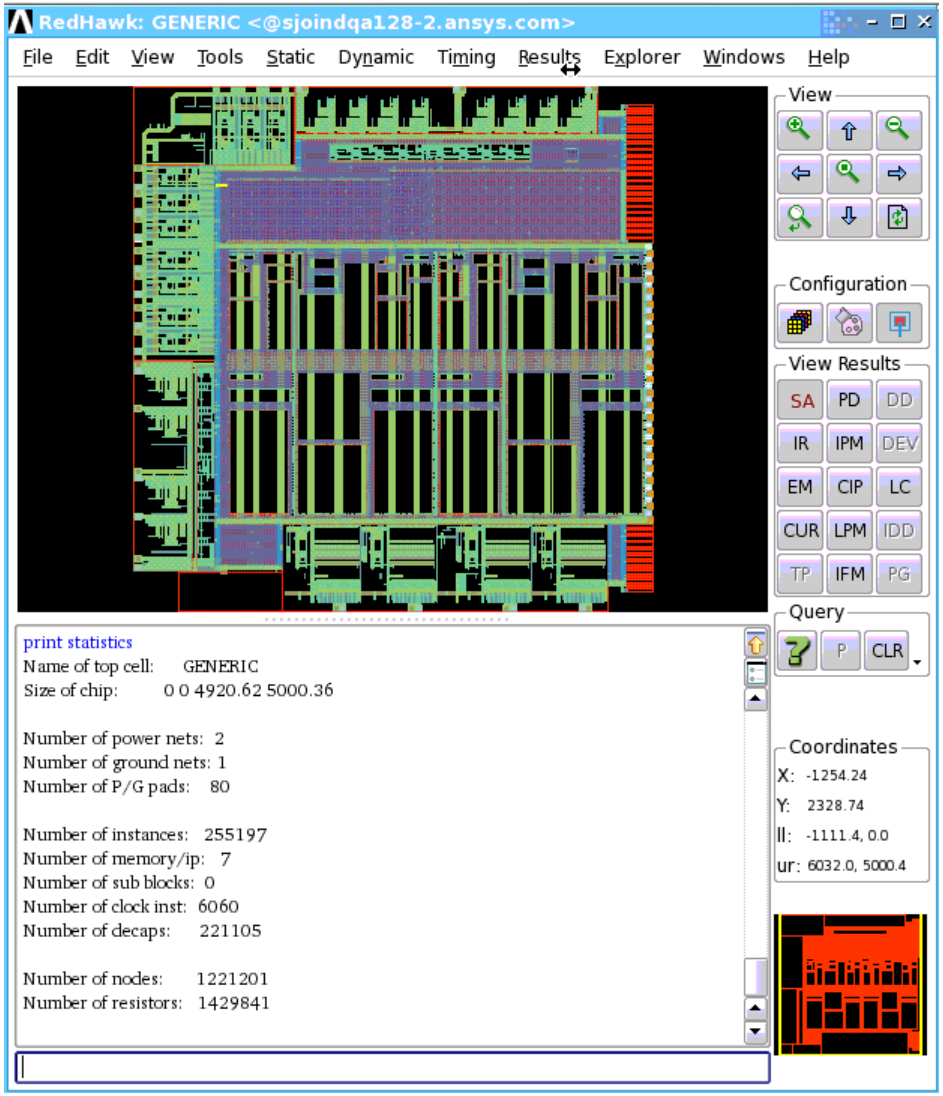
Tech File Viewer





Verify that the technology file parameters were correctly specified

Design Information



TCL query: *print statistics*

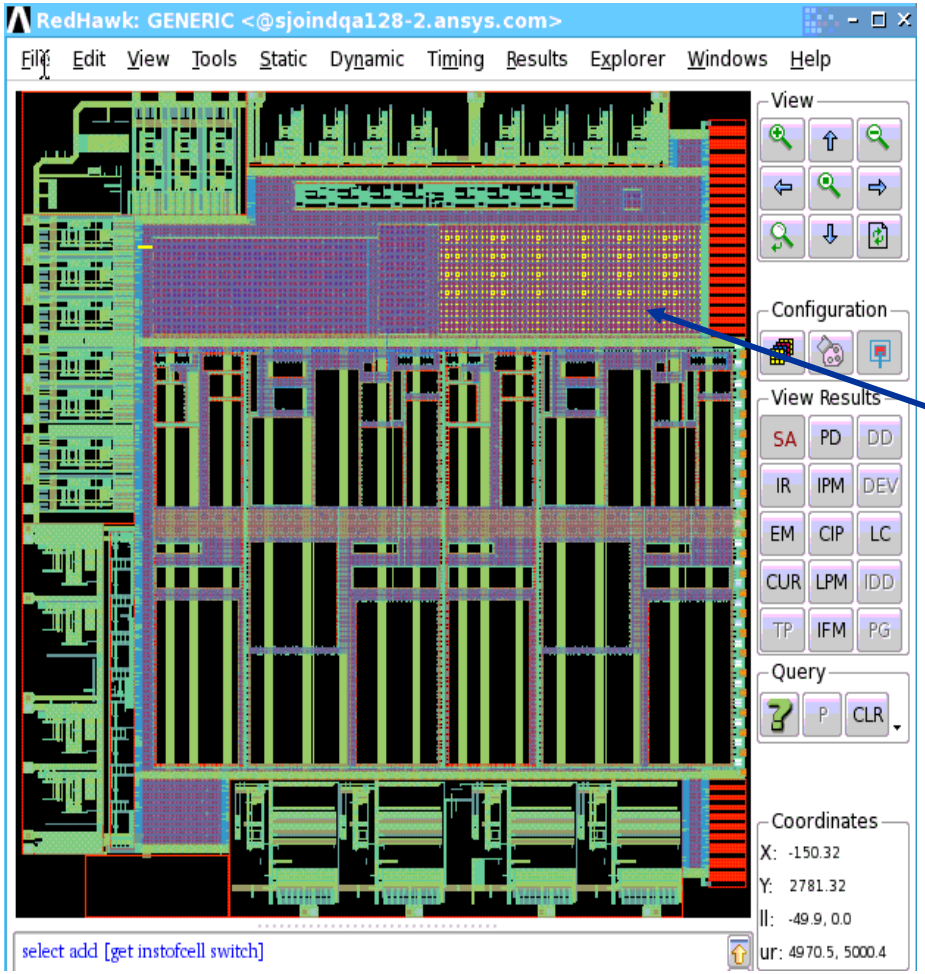
```
Name of top cell:        GENERIC
Size of chip:            0 0 4920.62
5000.36

Number of power nets:    2
Number of ground nets:   1
Number of P/G pads:      80

Number of instances:     255197
Number of memory/ip:     7
Number of sub blocks:    0
Number of clock inst:    6060
Number of decaps:        221105

Number of nodes:         1234696
Number of resistors:     1447700
```

Some GUI Features

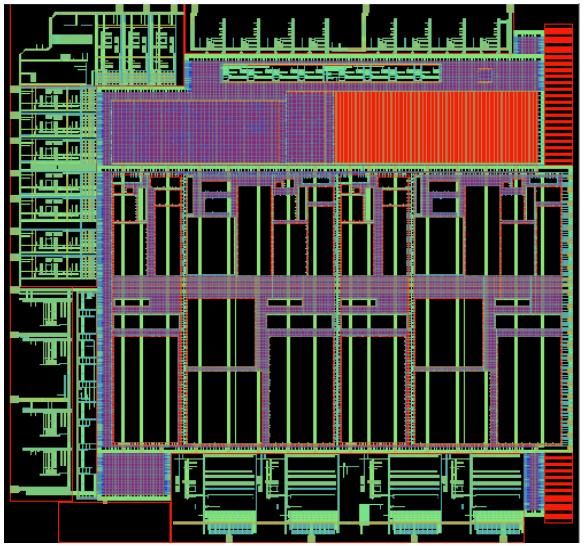


- **TCL query**

```
select add [get instofcell switch]
```

Some GUI Features
Net Selection Options

Constant VDD Domain

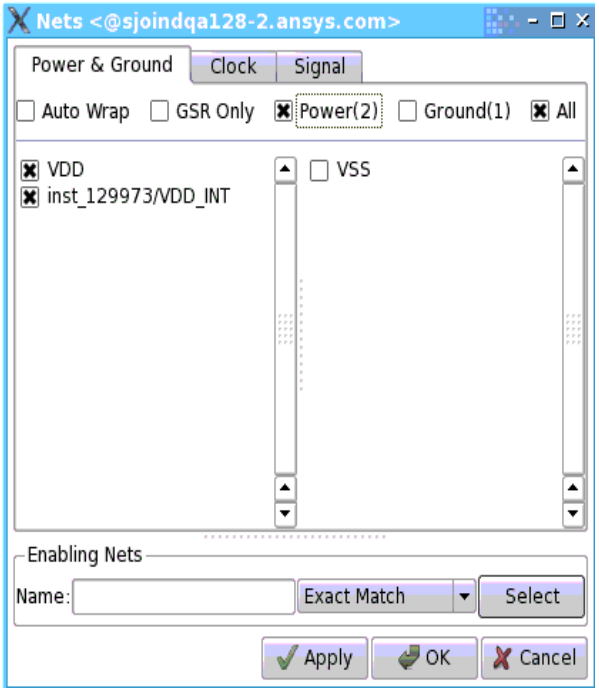


```
config viewnet -name all -mode
off
config viewnet -name VDD -mode on
```

Virtual VDD_INT Domain

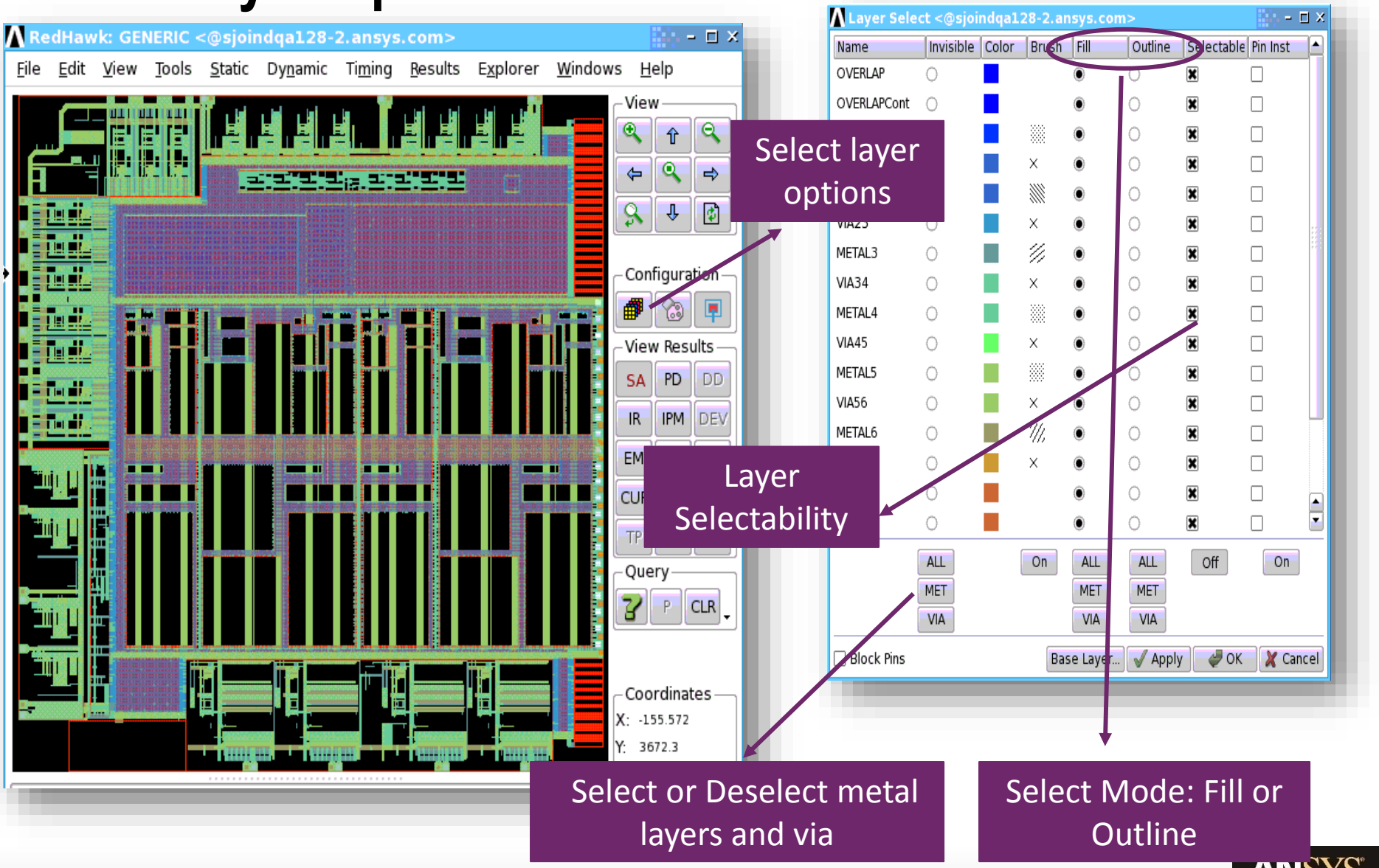
```
config viewnet -name all -mode off

config viewnet -name inst_129973/VDD_INT
-mode on
```



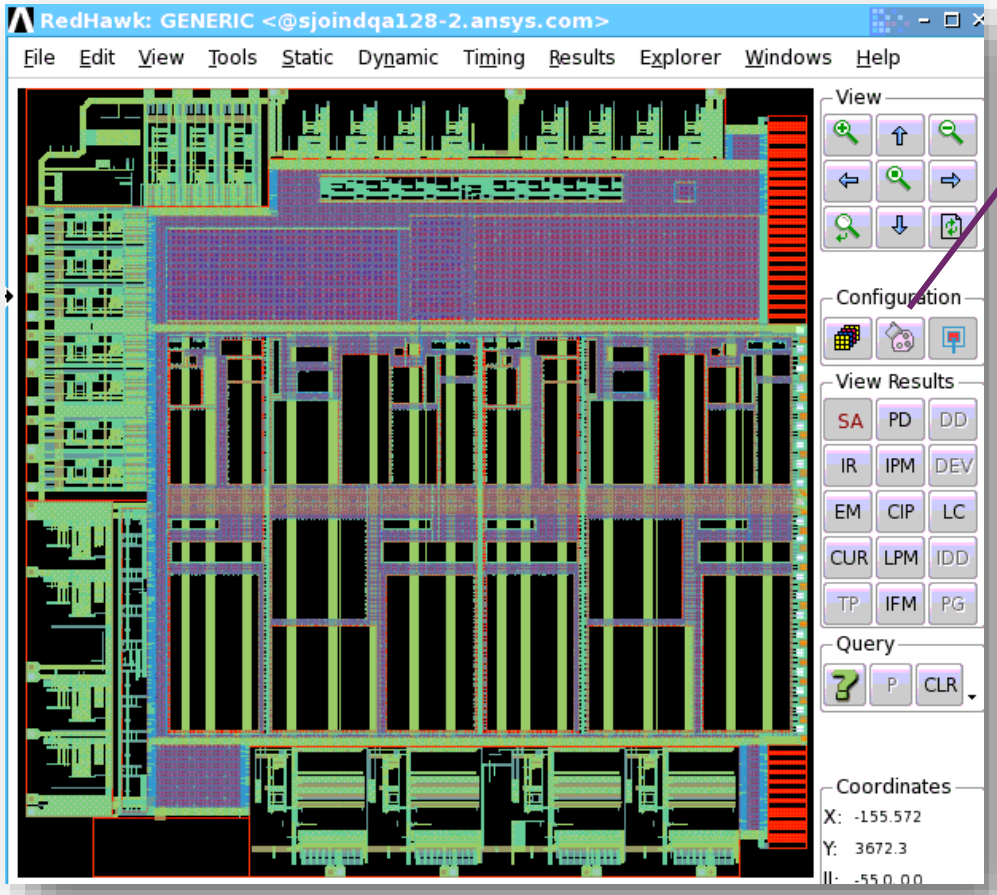
Same can be done with View -> Nets Menu

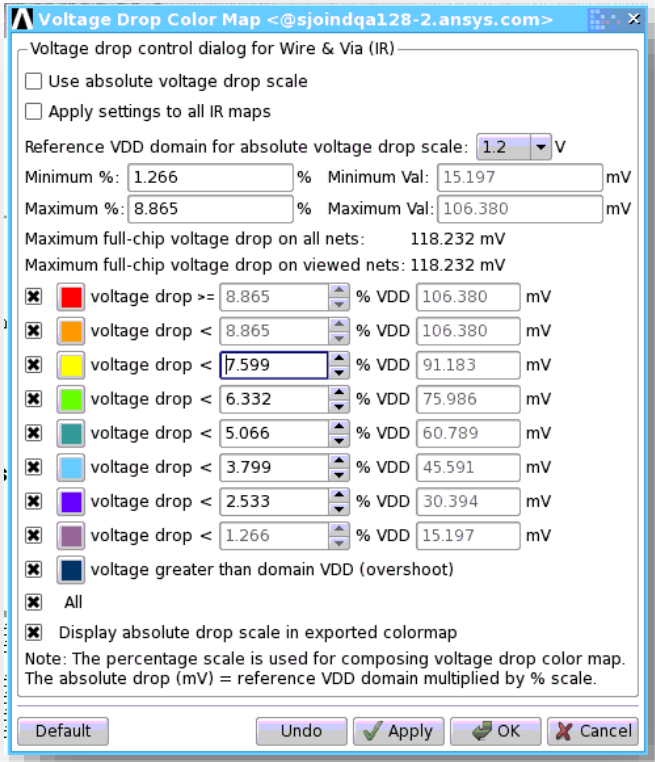
Layer Options



Set Color Range

Select color range options for different Maps



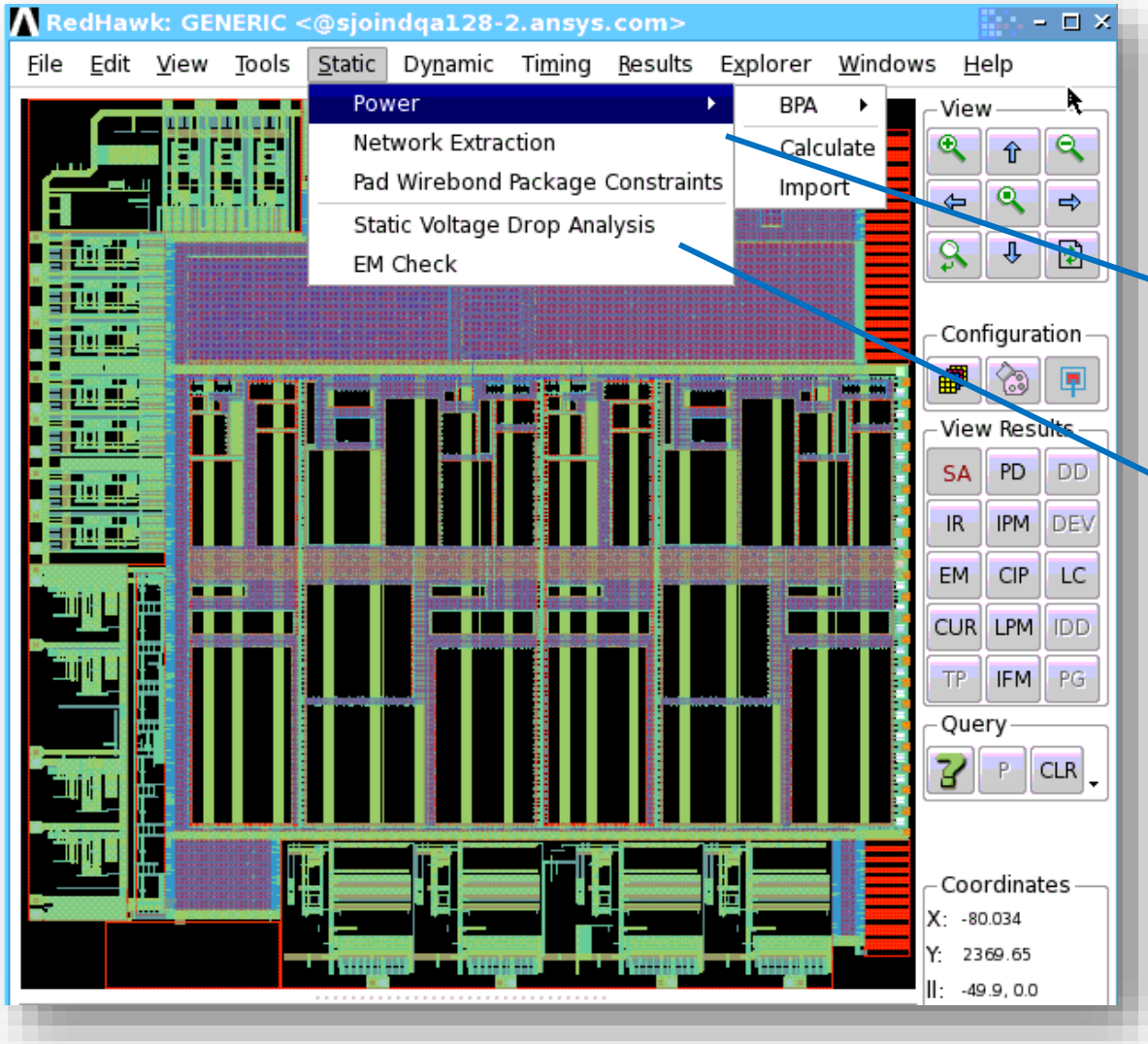


This window appearance will change based on the option you are currently viewing

You can export the color configuration using “export guiconf <outputFileName>” command.

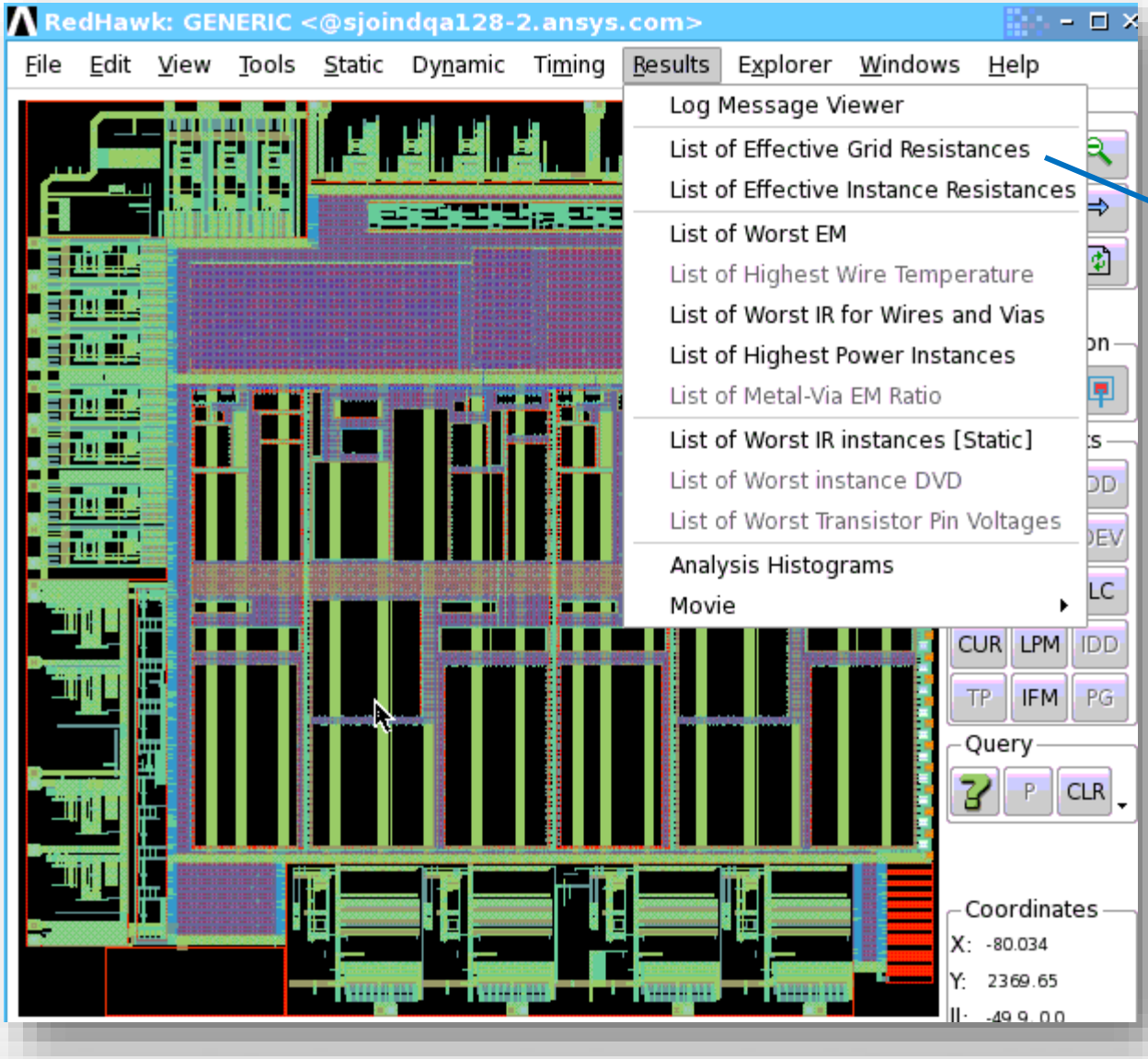
This file can be imported later in other RedHawk sessions using “import guiconf”

GUI Menu Overview



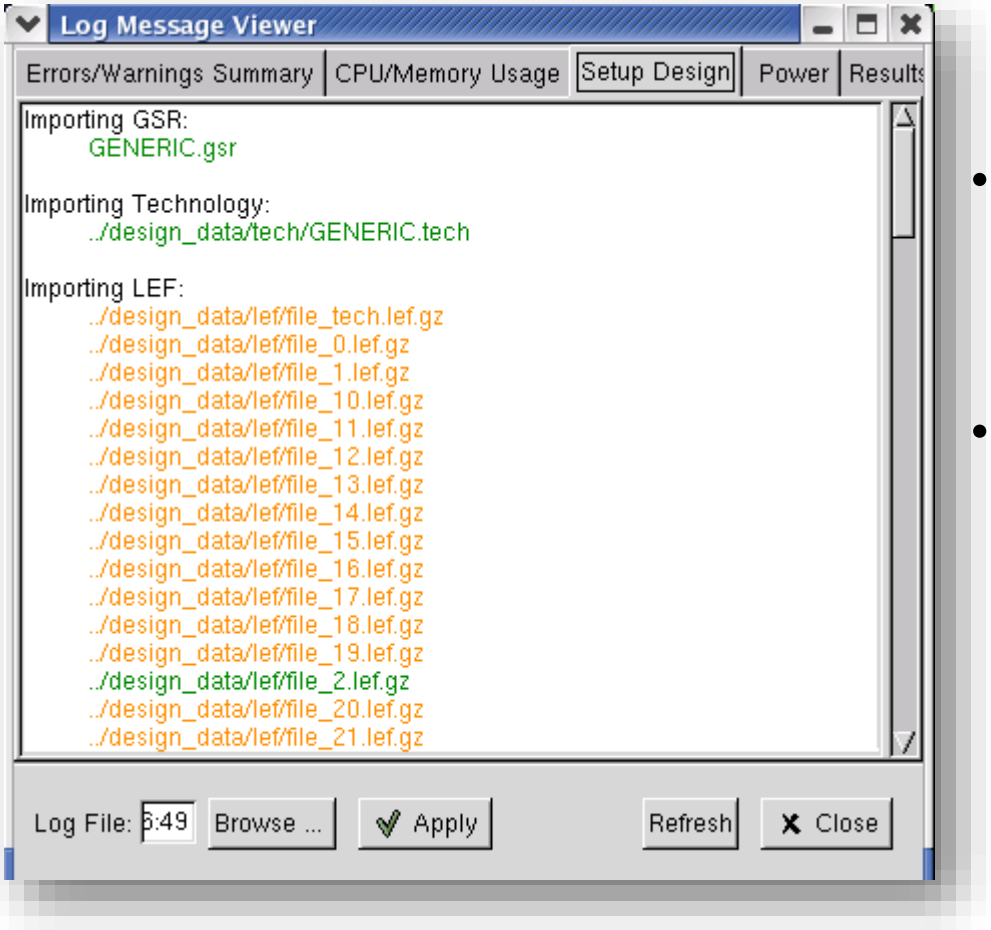
- **Static Analysis Steps**
  - Power calculation and Extraction options
- **Static IR/EM analysis options**

GUI Menu Overview (Cont'd)



- **Result viewing options**

Log Message Viewer



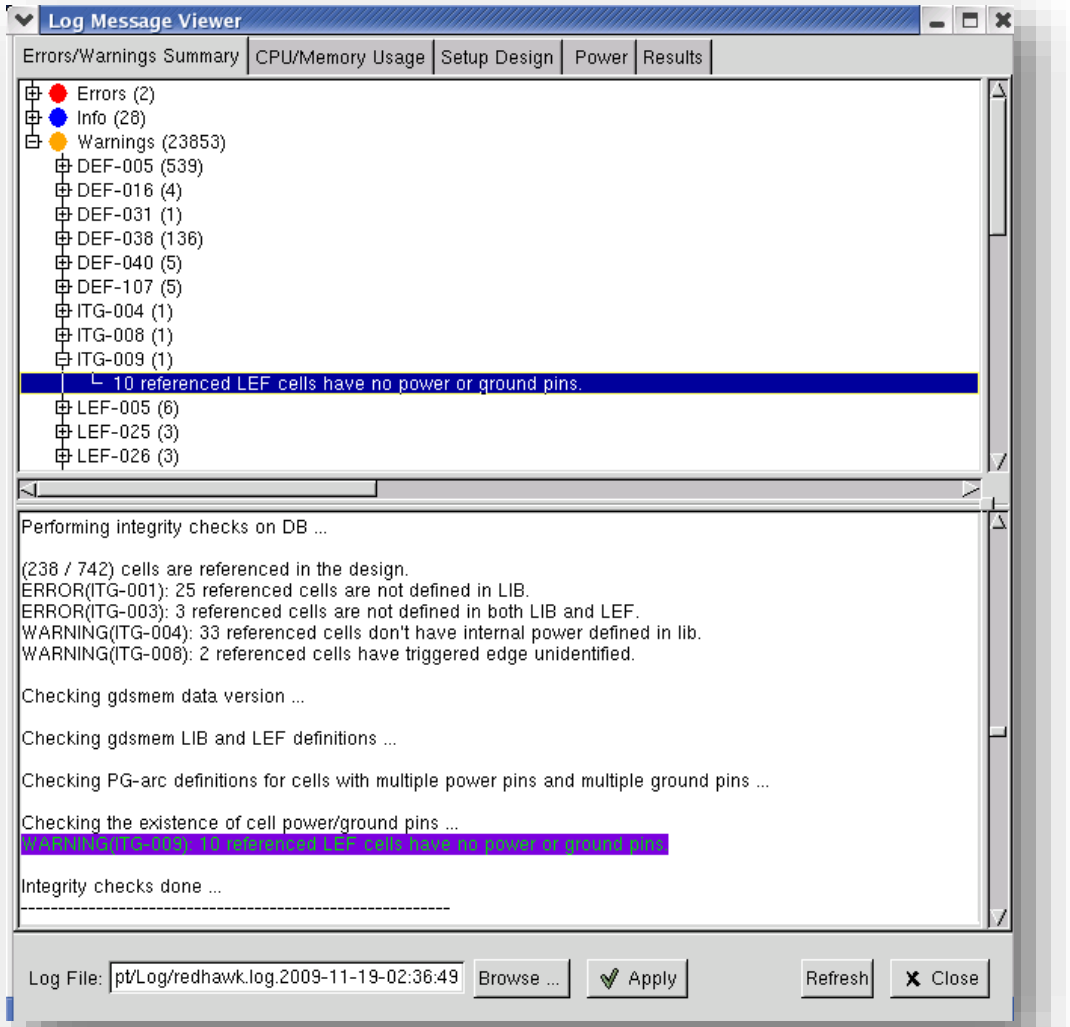
- **Select**

  Results → Log Message Viewer

  Click on Setup Design Tab

- **Error tagging on files read-in**
  - Red → Error during import
  - Orange → Warnings
  - Green → No issues seen

Log Message Viewer (Cont'd)



Common LEF/DEF Issues

- **Power pins in LEF**
  - Both power and ground pins must be defined
  - Must contain geometries
  - USE POWER and USE GROUND specified?
- **Power pins in DEF**
  - Block level DEF must have logical definition
  - Top level DEF need not have pins defined, unless 'ADD_PLOC_FROM_TOP_DEF 1' is set in GSR
  - Example

    - VDD + NET VDD + USE POWER + DIRECTION INOUT

    + LAYER MET6 + RECT (0 0) (100 100) + PLACED N (12340 23450)

Common LEF/DEF Issues (Cont'd)

- **Power/Ground nets in DEF**
  - Power and ground nets in SPECIAL NETS and/or NETS section must have USE POWER and USE GROUND attributes

- **P/G nets must establish logical connectivity**
  - - VDD (I1 VDD) (I1/MUX1 VDD) (RAM1 VDD) + MET1 ….
  - - VDD (* VDD) + MET1 ….

PG-arc Issues

- **ERROR(ITG-016): Missing PG-arc definitions for cell**
  - To support cells with multiple Vdd and multiple Vss pins, you need to specify the P/G arcs to define the current path between each VDD node to the associated GND node pair.

  - Example of pgarc defined in custom lib file for a cell

```
cell ram_mvdd {
pgarc {
VDD VSS
VDD2 VSS2
VDDL VSS
}
}
```

PG-arc Issues *(Cont'd)*

- **Specify the custom.lib under the LIB_FILES section of the GSR**

  LIB_FILES {

  <lib_filename> CUSTOM

  ...

  }

- **If you are unsure as to which cells need to be specified in a custom library, then run the design through 'setup design' and look at the data in the file adsRpt/apache.refCell.noPGArc**

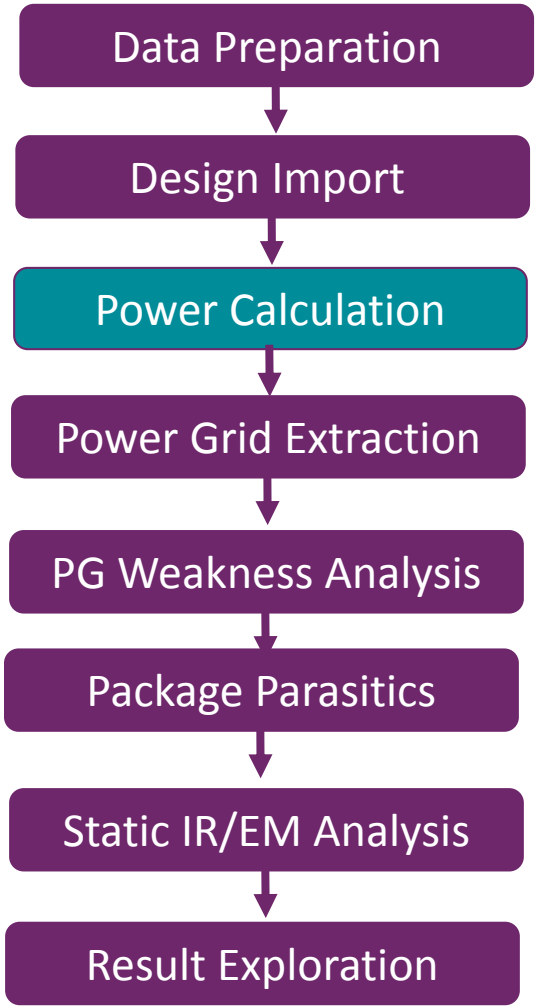
- **RedHawk detects cells with multiple ground pins that have no custom LIB file and reports them in the report adsRpt/apache.refCell.noPGArc, along with all power and ground pins for each cell.**

  Example:

  #<cell_name> <vdd_pin_names> <gnd_pin_names>

  <SC_ANALOG> <VDD1A VDD2A> <VSS1A VSS2A>

Step 3: Power Calculation

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# Import data
import gsr GENERIC.gsr
setup design
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# Calculate power
perform pwrcalc

# Power/Ground grid extraction
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# Lumped resistance (in Ohms)
# for package, wirebond and pads
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setup pad -power -r 0.001
setup pad -ground -r 0.001

# Static IR analysis
perform analysis -static

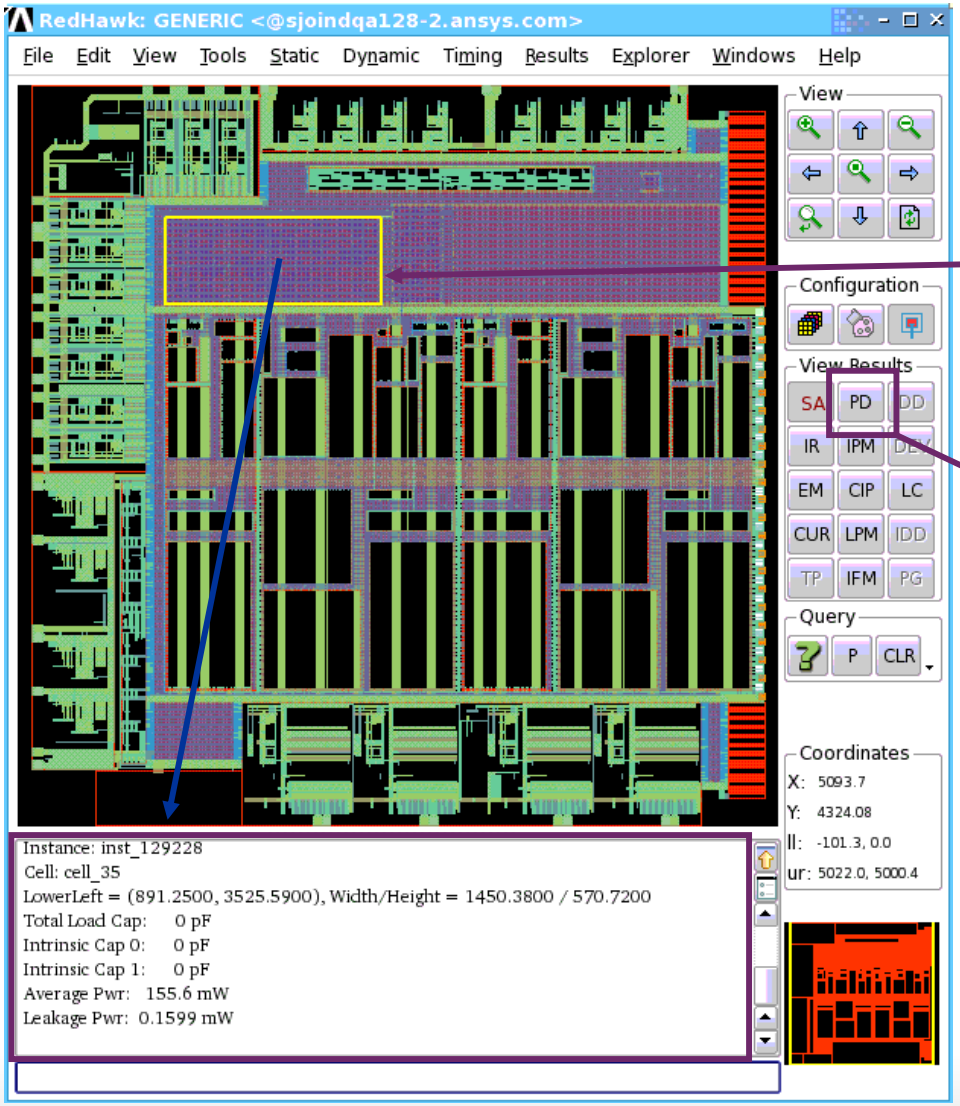
# Result Exploration using RHE
explore design
```

*** In GUI : *Static -> Power -> Calculate Power***

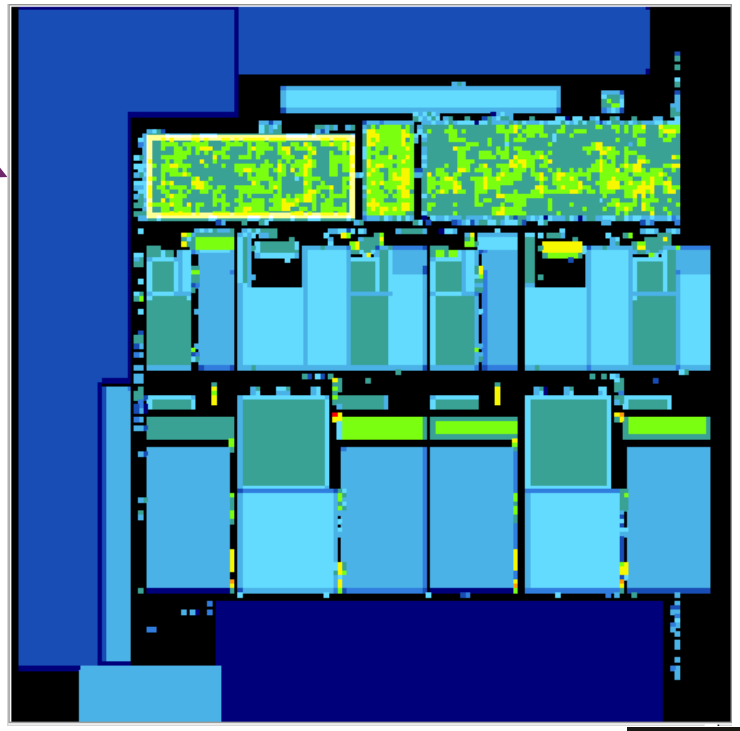
Power Calculation

- **Calculates power of cells and blocks in the design and total power of the design**
- **Can also import power from 3rd party tools**
- **Power DB created has the name: adsPower**
- **Can be imported for subsequent static and dynamic analysis if the design netlist and parameters do not change**
- **Important: Check for cell with missing .lib or power models during run or in RedHawk™ log file**
  - adsRpt/apache.refCell.noLib
  - adsRpt/apache.refCell.noPwr

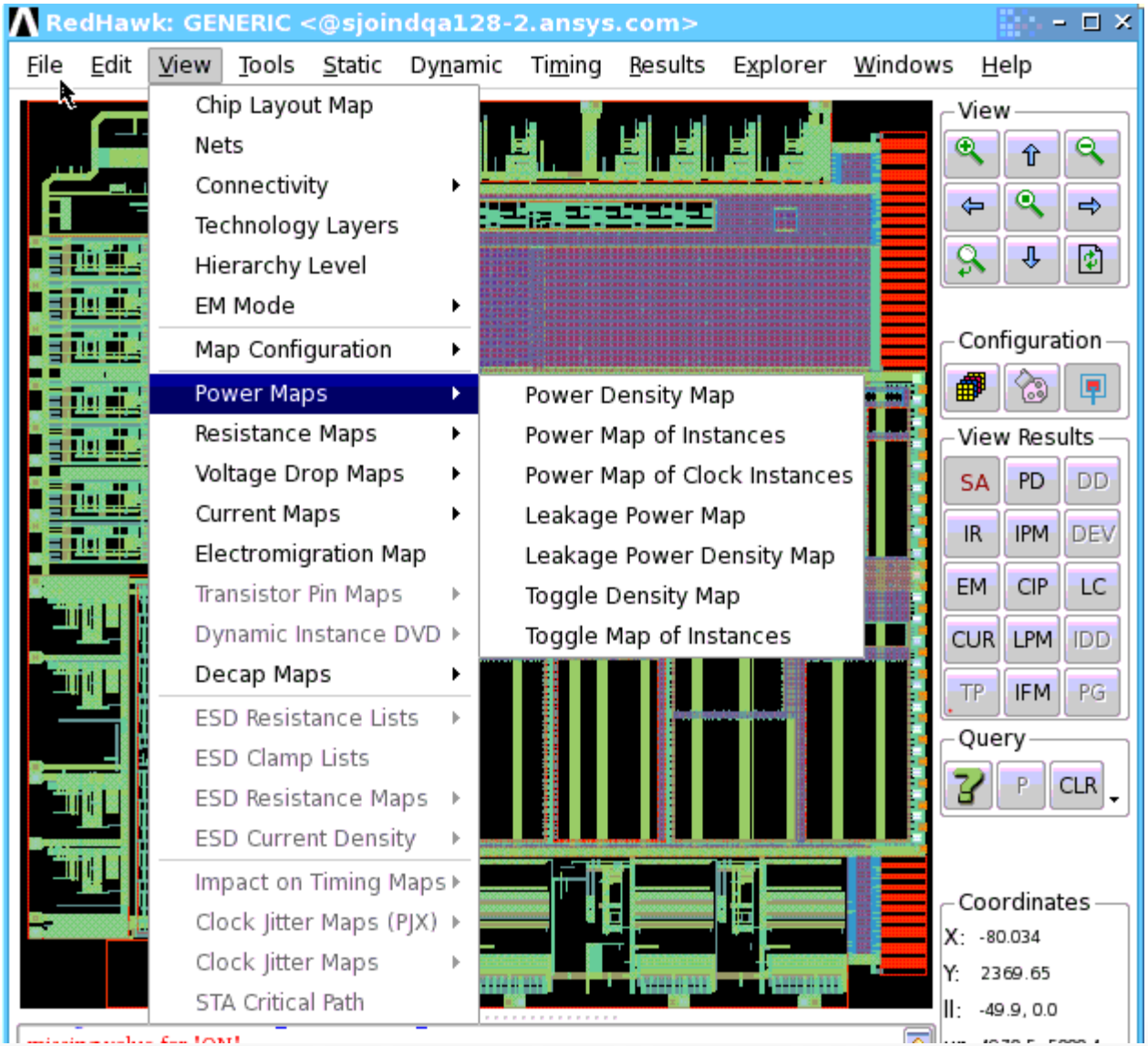
Power Calculation *(Cont'd)*



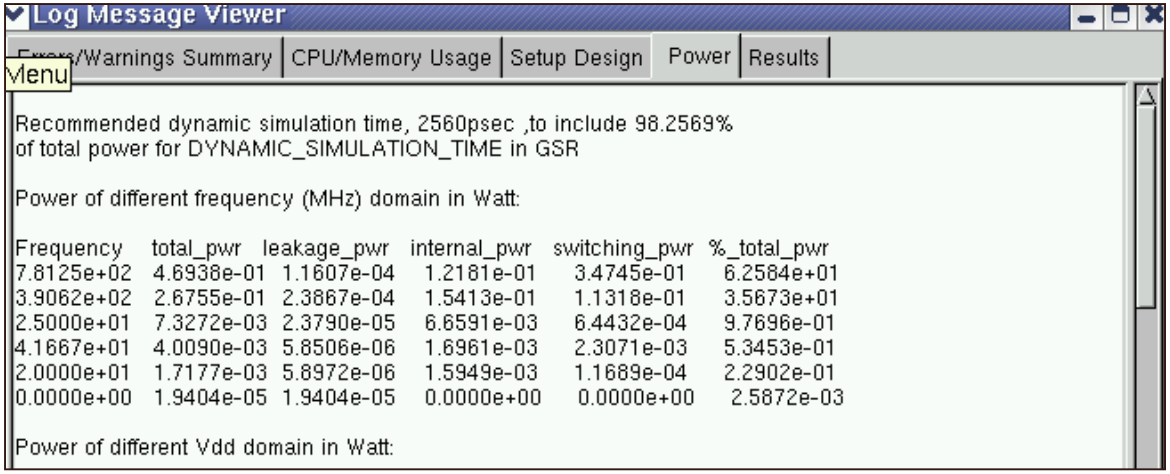
- **Examine Power Density (PD) map and Instance Power (IPM) map**
- **Click on instance to query the power**



Viewing Power Maps



Power Analysis Reports



Select
Results ➔ ***Log Message Viewer***
Then select *Power* tab
Examine power summary

adsRpt/power_summary.rpt - Summary of power consumption
Domain
Frequency
Clock, non-clock
tcl command: report power –o power.rpt
gives instance level power, frequency, toggle, location, cell name

*** Same report as in Log Message Viewer**

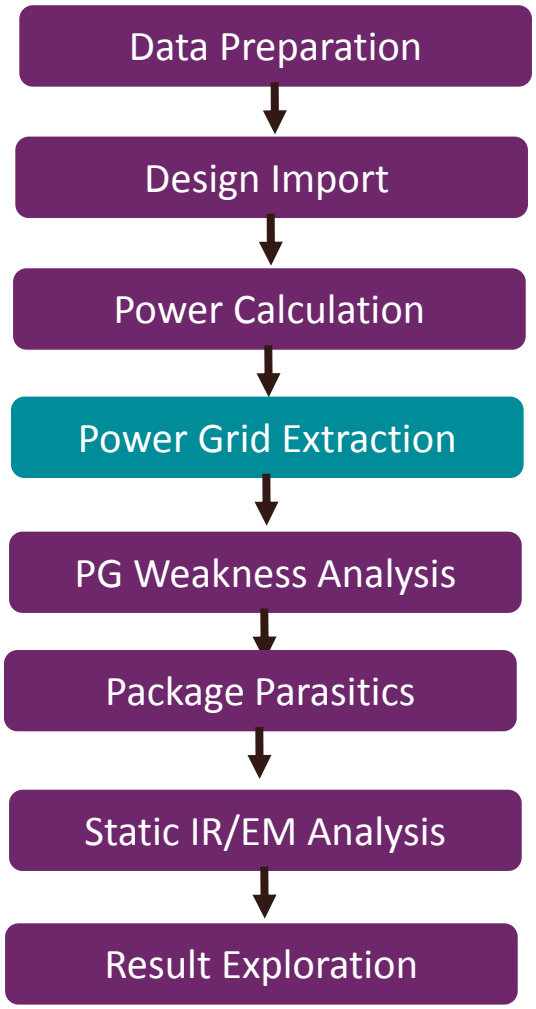
Power Calculation Issues/Checks

- **Does the Total Power number make sense?**

- **Clock network power and Clock power reasonable?**
  - Clock network power is power of clock tree/mesh, typically ~ 20-30% of total
  - Clock power is network power + clock pin power, typically ~ 30-40% of total

- **Power per clock frequency domain reasonable?**
  - Determined by clock roots or Primetime STA file
  - Incorrect clock roots or PT case analysis?

Step 4: Network Extraction

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# Static IR analysis
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# Result Exploration using RHE
explore design
```
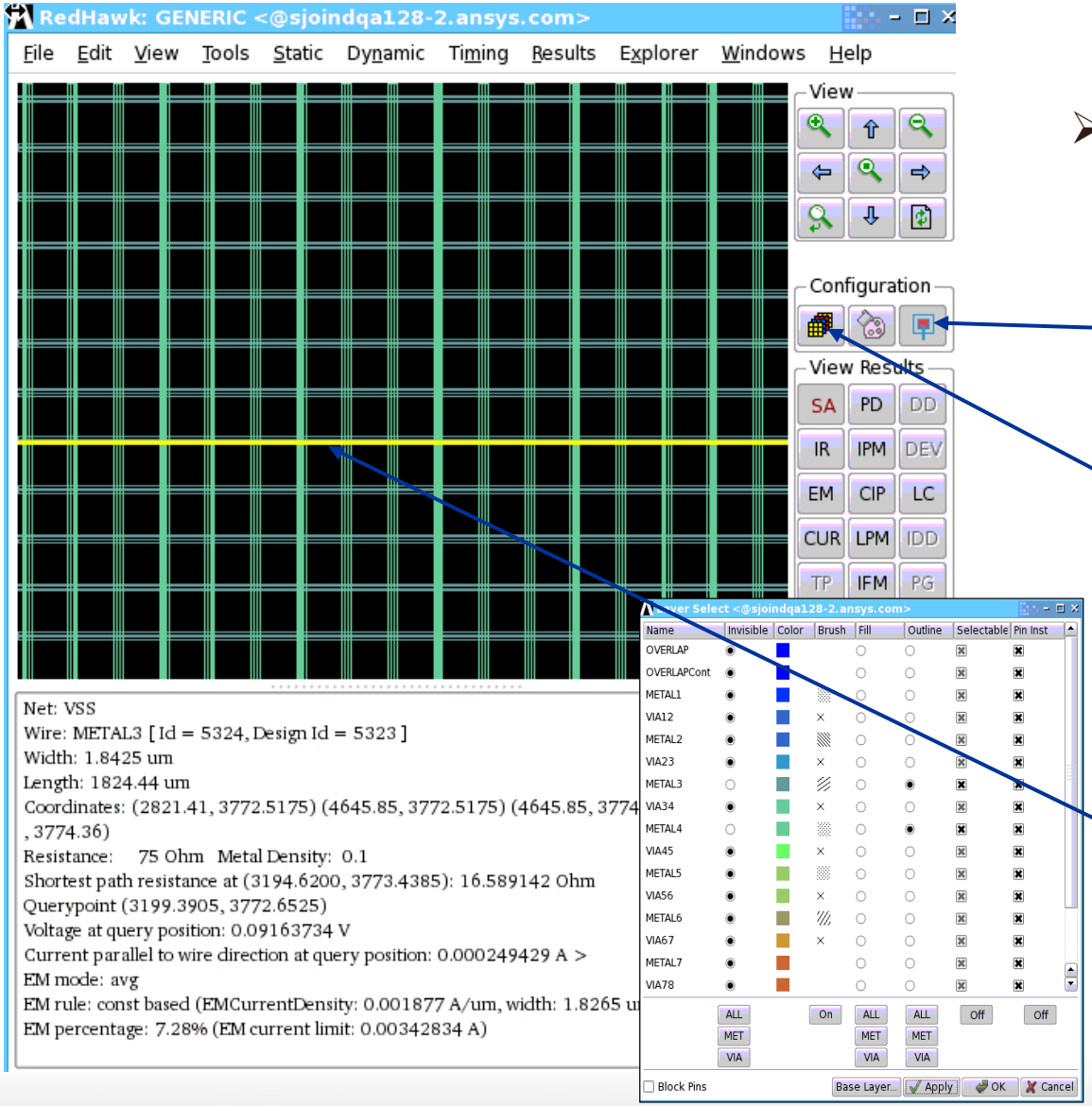

*** In GUI: *Static -> Network Extraction***

Extraction



- **Execute:**
  `perform extraction -power -ground`

Click on Show Power Pad button to see location of voltage sources

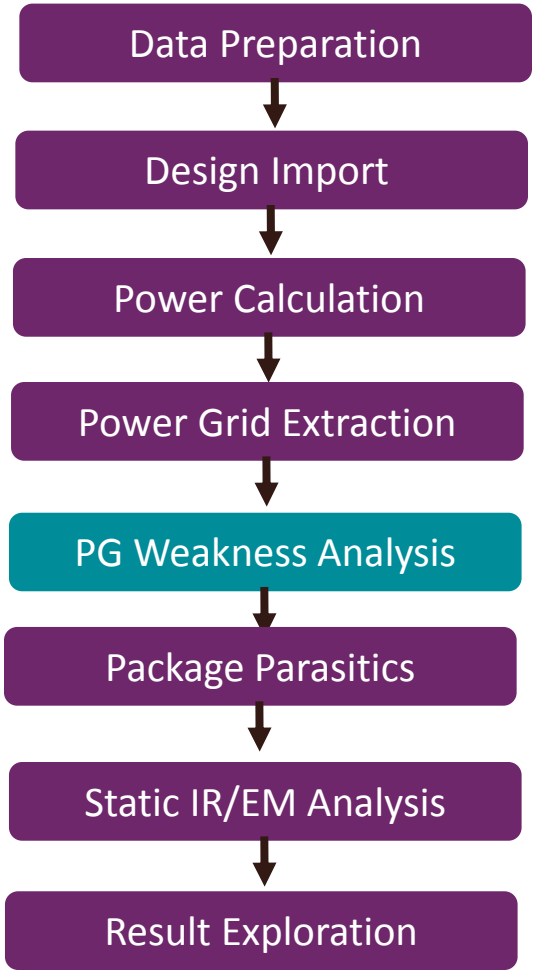
Bring up *View Layers* Dialog box. Choose some metals/via layers

Click on wires/vias to query resistance

PG Network Extraction Issues

- **Is Power or Ground net connected to ideal source?**
  - "Net VDD not driven by any pad, pcell or ploc"
- **Any disconnected PinInst, wire or vias?**
  - Check adsRpt/<design>_VDD.*.unconnect
  - Check adsRpt/<design>_VSS.*.unconnect
  - Check adsRpt/<design>.*.unconnect
- **Any shorts between nets?**
  - Watch out for CON-109, CON-110 and CON-111 errors
  - These can result from either physical shorts or from lack of logical connectivity between DEFs and LEFs
- **Look for power and/or ground pins that are incorrectly placed – either wrong polarity or not placed on a wire**

Step 5: PG Weakness Analysis

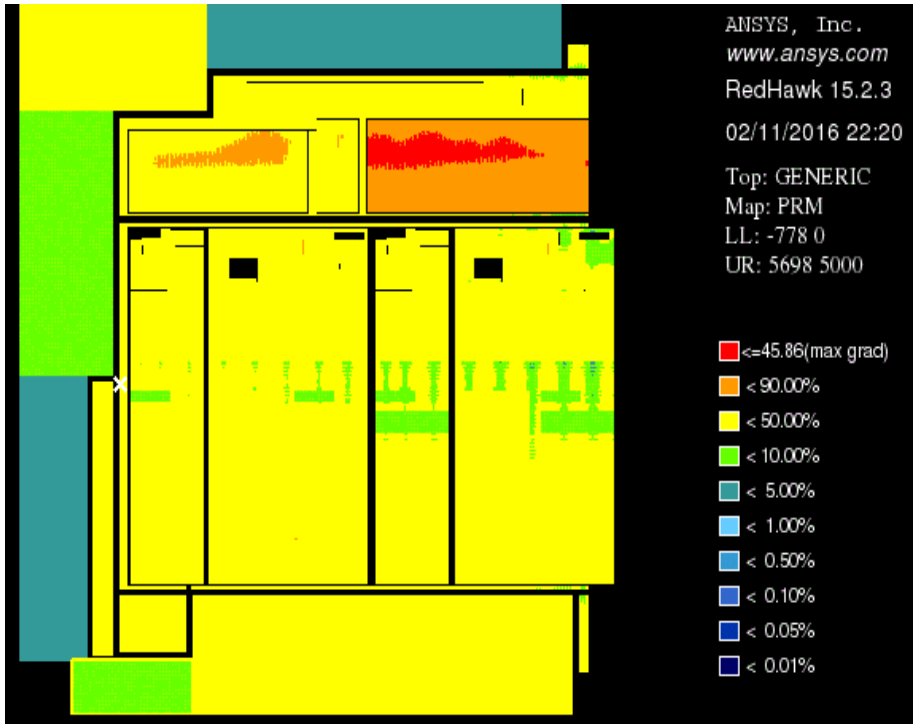


- **Early analysis capability for power grid robustness**
  - **PG Resistance Analysis**
  - **Missing Vias**
  - **Analyzing Shorts**
  - **Disconnected wires / Vias**
  - **Disconnected instances**
  - **Perform Resistance Calculation**
- **Can be performed as early as in the floor-plan stage**

Resistance Maps

GUI: View→ Resistance Maps

VDD Resistance

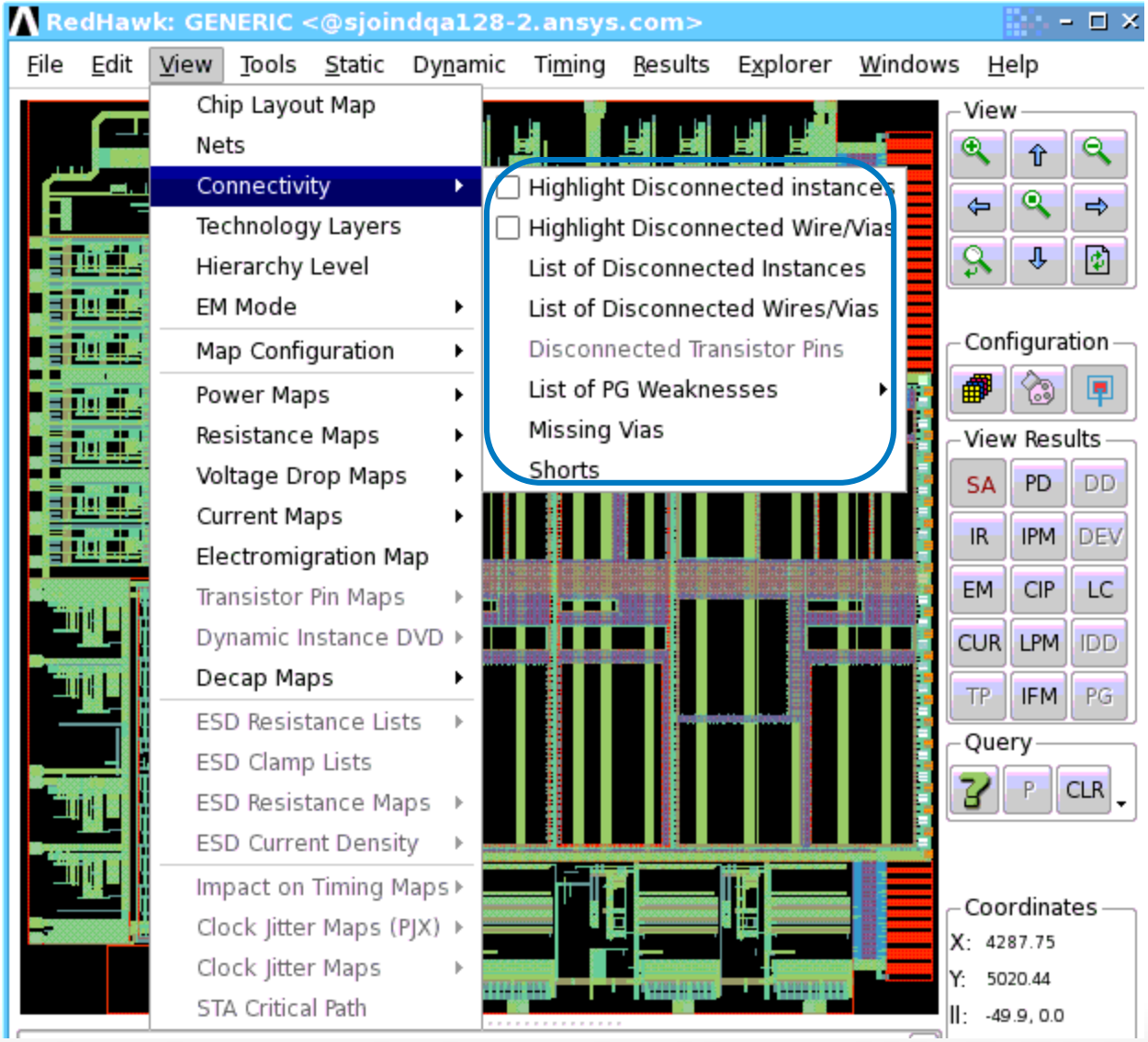


VSS Resistance

Asymmetry between power and ground resistance

Helps identifying weak regions

Connectivity Checks



Explore 'perform res_calc' Command

- **`'perform res_calc'` command calculates effective PG grid resistance from all pads to selected instances or locations.**
- **It gives the absolute resistance value whereas `'perform gridcheck'` gives the normalized resistance.**
- **Syntax**

```
perform res_calc ?[-instance <name>]? ?[-inst_file <file>]?
? -incremental? ?[-cell <name>]? ?-all_point? ?-worst_point?
?-box <llx lly urx ury>? ?-gnd <name>? ?-pwr <name>?
?-layer <name>? ?-limit <num>? ?-o <file>? ?-append? ?-verbose?
?-thread <num>? ?-xtor <name_list>? ? -loopmode ?
?-pin <name_list>? ?-all_pin? ? -cell_file <CellFile>?
```

  - Please refer to the RedHawk Manual for details about each option.

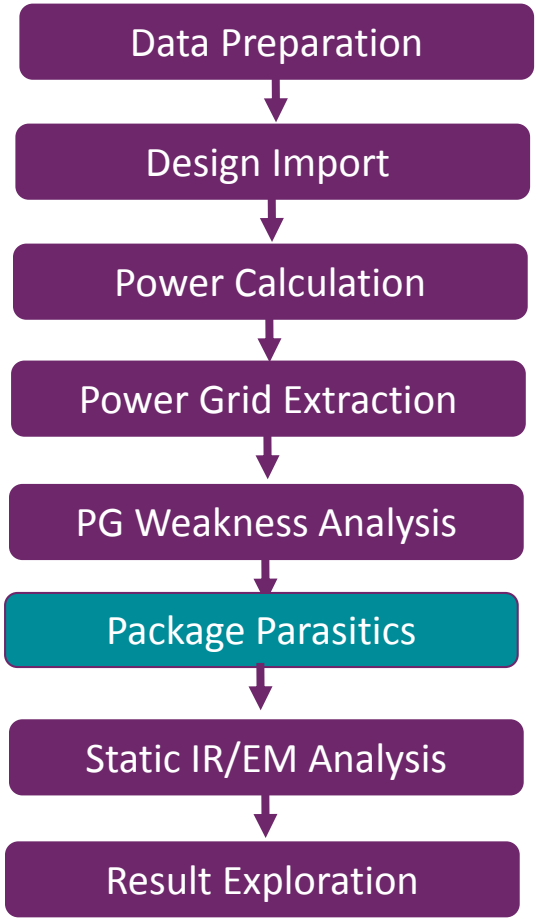
- **The default, without any option 'perform res_calc' gives the resistance report for worst instances as indicated by quick estimation**
- **The default output file is *adsRpt/<design_name>.res_calc***

'perform res_calc' - Output

```
# Grid Resistance Calculation Report
#
# Resistances from all pads to the listed points
# Ohm   Location(x y)   Layer   Net     Instance
67.3972 4459.77 443.855 METAL3  VDD     inst_129747/adsU1
4.42445 2839.61 3959.78 METAL1  inst_129973/VDD_INT     inst_129973/inst_375304
4.30808 2840.44 3952.4  METAL1  inst_129973/VDD_INT     inst_129973/inst_367447
4.12397 2841.42 3952.4  METAL1  inst_129973/VDD_INT     inst_129973/inst_431199
4.03733 2841.88 3952.4  METAL1  inst_129973/VDD_INT     inst_129973/inst_431200
3.9507  2842.34 3952.4  METAL1  inst_129973/VDD_INT     inst_129973/inst_431201
3.86406 2842.8  3952.4  METAL1  inst_129973/VDD_INT     inst_129973/inst_431203
3.77742 2843.26 3952.4  METAL1  inst_129973/VDD_INT     inst_129973/inst_368305
3.69078 2843.72 3952.4  METAL1  inst_129973/VDD_INT     inst_129973/inst_431205
2.92883 2871.29 3981.92 METAL1  inst_129973/VDD_INT     inst_129973/inst_304473
2.92823 2870.86 3981.92 METAL1  inst_129973/VDD_INT     inst_129973/inst_304472
2.92575 2870.4  3981.92 METAL1  inst_129973/VDD_INT     inst_129973/inst_304471
```

- **The first column shows the absolute resistance of P/G pads from the selected points, the second and third column give the (x,y) co-ordinates of the instance ,the fourth ,fifth and sixth columns give the Layer name, Net name and instance name respectively.**

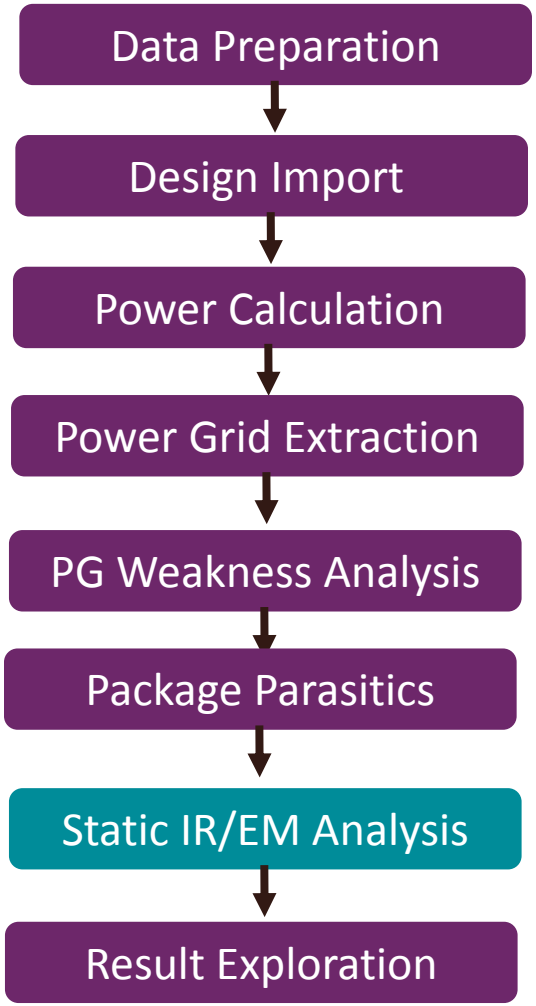
Step 6: Package and Pad Constraints




```
# Import data
import gsr GENERIC.gsr
setup design
setup analysis_mode static
# Calculate power
perform pwrcalc
# Power/Ground grid extraction
perform extraction -power -ground

# Lumped resistance (in Ohms)
# for package, wirebond and pads
setup package -power -r 0.005 -l 2.5 -c 5
setup package -ground -r 0.005 -l 2.5 -c 5
setup wirebond -power -r 0.01 -l 2.2 -c 1.42
setup wirebond -ground -r 0.05 -l 1.7 -c 0.2
setup pad -power -r 0.001
setup pad -ground -r 0.001

# Static IR analysis
perform analysis -static
# Result Exploration using RHE
explore design
```

- **GUI: *Static -> Pad, Wirebond / Bump and Package Constraint***
- **Distributed Package model in spice / S-parameter format also supported**

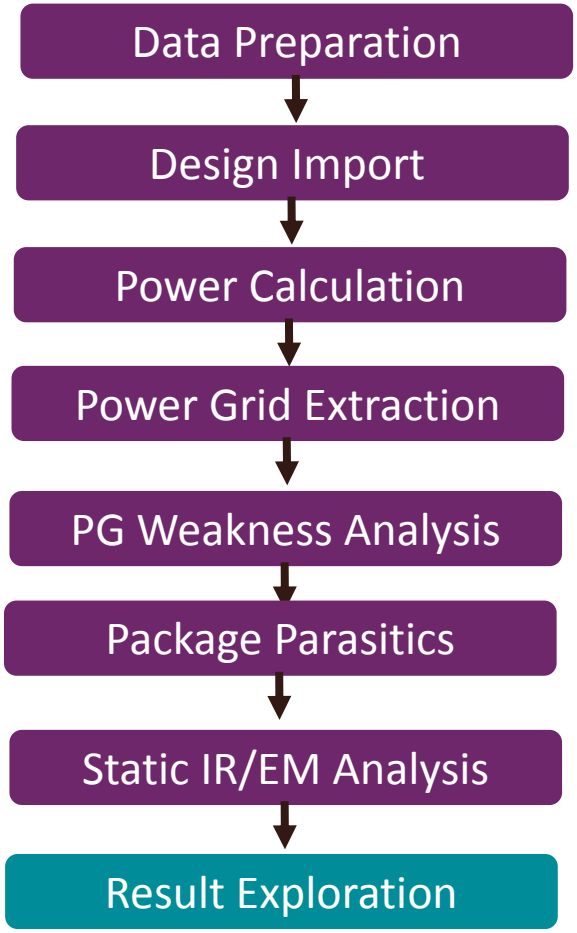
Step 7: Static Analysis




```
# Import data
import gsr GENERIC.gsr
setup design
setup analysis_mode static
# Calculate power
perform pwrcalc
# Power/Ground grid extraction
perform extraction -power -ground
# Lumped resistance (in Ohms)
# for package, wirebond and pads
setup package -power -r 0.005 -l 2.5 -c 5
setup package -ground -r 0.005 -l 2.5 -c 5
setup wirebond -power -r 0.01 -l 2.2 -c 1.42
setup wirebond -ground -r 0.05 -l 1.7 -c 0.2
setup pad -power -r 0.001
setup pad -ground -r 0.001

# Static IR analysis
perform analysis -static

# Result Exploration using RHE
explore design
```

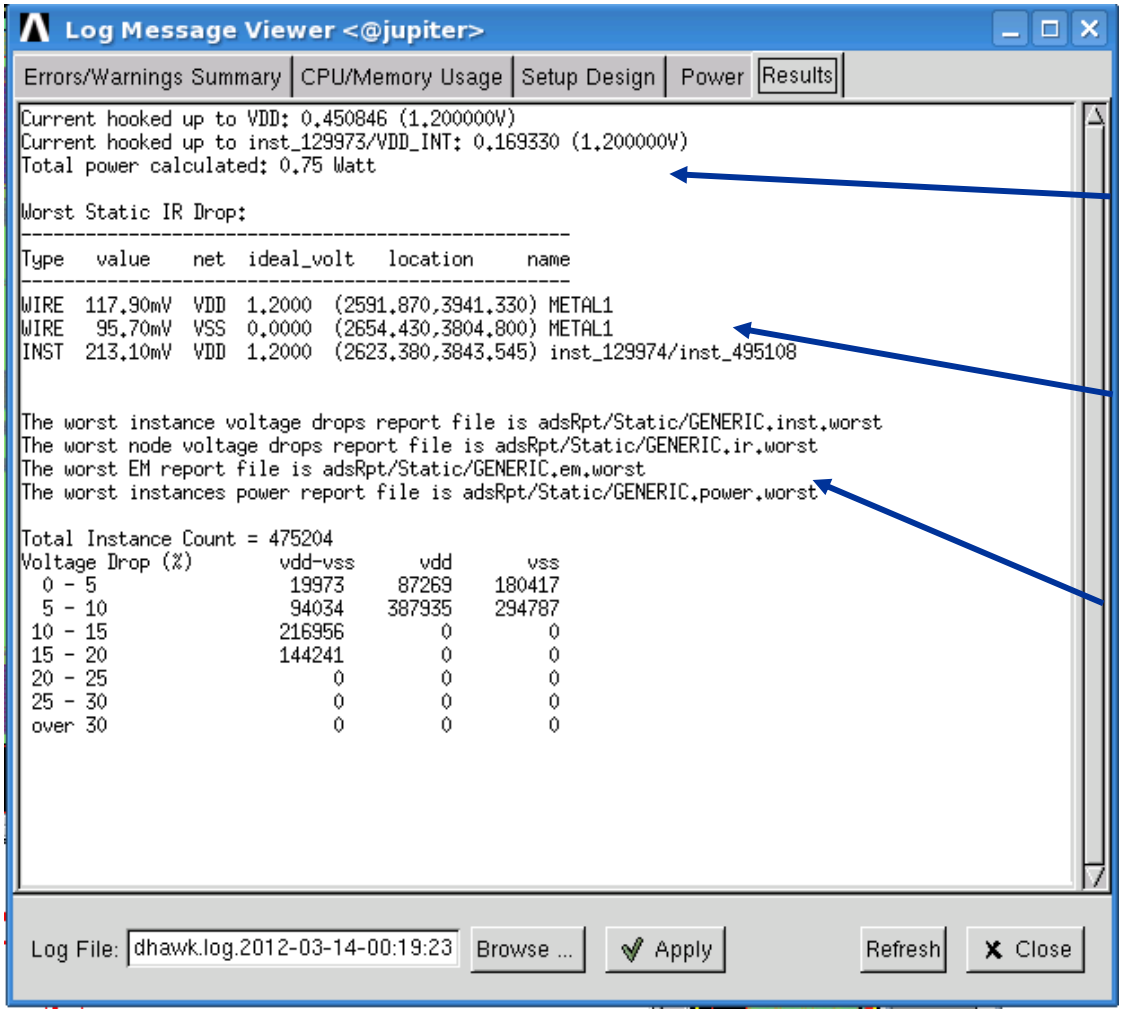
**GUI: Static -> Static IR-drop & EM Analysis*

Step 8: Result Exploration and Debugging



- **Result summary**
- **Log message viewer**
- **Result Maps**
- **EM violations**
- **Text Results**
- **RedHawk Explorer**

Examine Summary of Results



Total power of cells hooked to the network

IR drop summary

Text report pointers

*** Log/error/warnings/command history stored under adsRpt**

Examine Summary of Results *(Cont'd)*

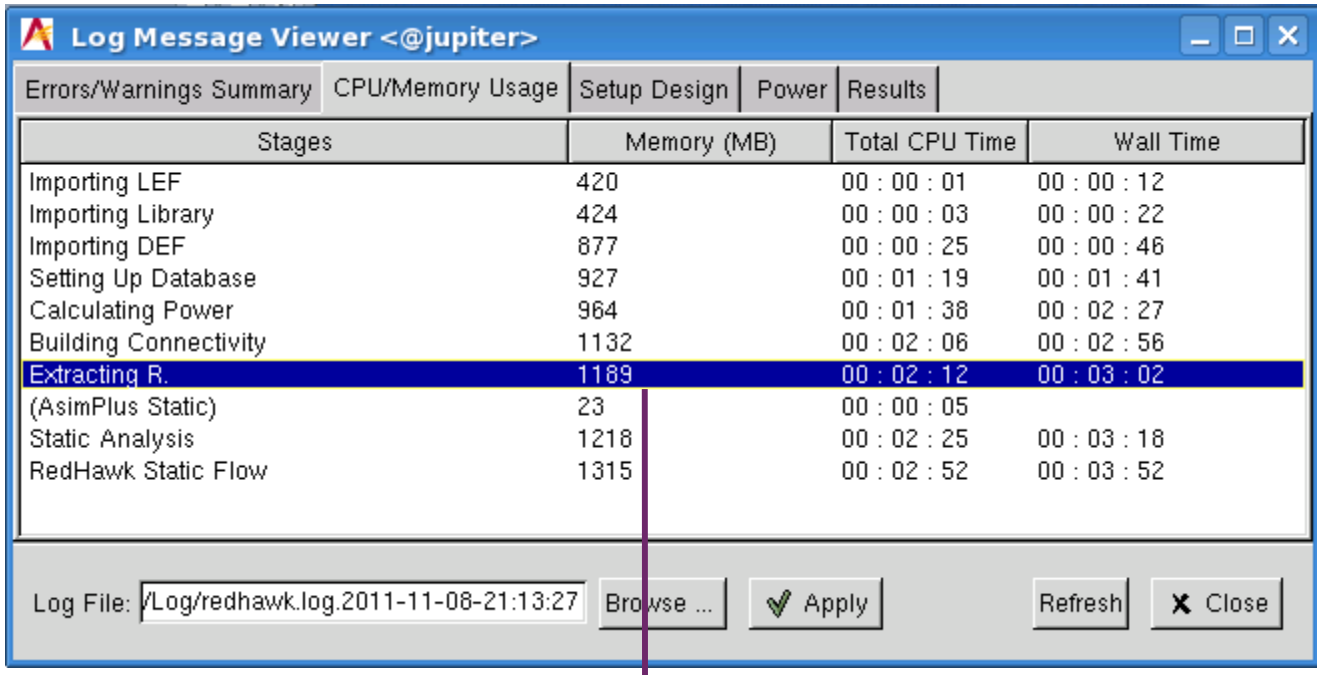
- **Summarizes variation in current load for all switches**
- **Can identify the in-effective switches from this report**
- **Switches supplying high current also cause high voltage drop**

```
#Report static results of switch voltage and current (milli-amperes)
#instance_name  type  internal_node_volt  volt_across_switch  avg_current
inst_129973/switch_inst_R1_C37  header  1.120460e+00  7.119894e-03  3.559953e-01
inst_129973/switch_inst_R2_C37  header  1.120161e+00  5.535722e-03  2.767889e-01
inst_129973/switch_inst_R3_C37  header  1.119729e+00  4.471302e-03  2.235622e-01
inst_129973/switch_inst_R4_C37  header  1.119197e+00  3.818512e-03  1.909233e-01
inst_129973/switch_inst_R5_C37  header  1.118597e+00  3.499985e-03  1.750022e-01
inst_129973/switch_inst_R6_C37  header  1.118092e+00  3.330708e-03  1.665321e-01
inst_129973/switch_inst_R7_C37  header  1.117795e+00  3.185511e-03  1.592779e-01
inst_129973/switch_inst_R8_C37  header  1.117690e+00  3.070951e-03  1.535502e-01
inst_129973/switch_inst_R9_C37  header  1.117705e+00  3.050566e-03  1.525241e-01
inst_129973/switch_inst_R10_C37 header  1.117875e+00  3.087044e-03  1.543536e-01
inst_129973/switch_inst_R11_C37 header  1.118198e+00  3.185987e-03  1.593002e-01
inst_129973/switch_inst_R12_C37 header  1.118591e+00  3.437638e-03  1.718832e-01
inst_129973/switch_inst_R13_C37 header  1.119055e+00  3.858209e-03  1.929125e-01
inst_129973/switch_inst_R14_C37 header  1.119729e+00  4.336834e-03  2.168394e-01
inst_129973/switch_inst_R15_C37 header  1.120405e+00  5.117297e-03  2.558678e-01
inst_129973/switch_inst_R16_C37 header  1.120906e+00  6.428599e-03  3.214287e-01
inst_129973/switch_inst_R17_C37 header  1.121169e+00  8.426189e-03  4.213073e-01
inst_129973/switch_inst_R1_C5   header  1.093288e+00  4.444599e-03  2.222256e-01
inst_129973/switch_inst_R2_C5   header  1.093037e+00  3.346086e-03  1.673064e-01
inst_129973/switch_inst_R3_C5   header  1.092635e+00  2.631903e-03  1.315955e-01
"adsRpt/Static/switch_static.rpt" 887L, 71176C                1,1           Top
```

/adsRpt/Static/switch_static.rpt

CPU/Memory Usage

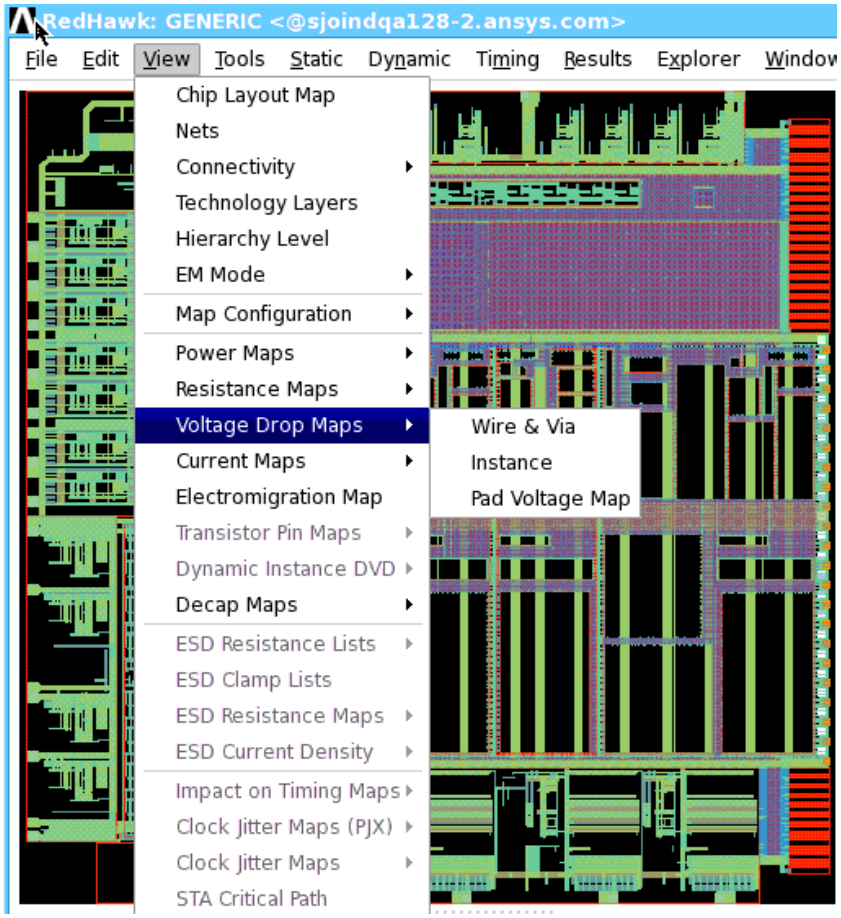
Select *Results* ➔ *Log Message Viewer*
Then select *CPU/Memory usage* tab



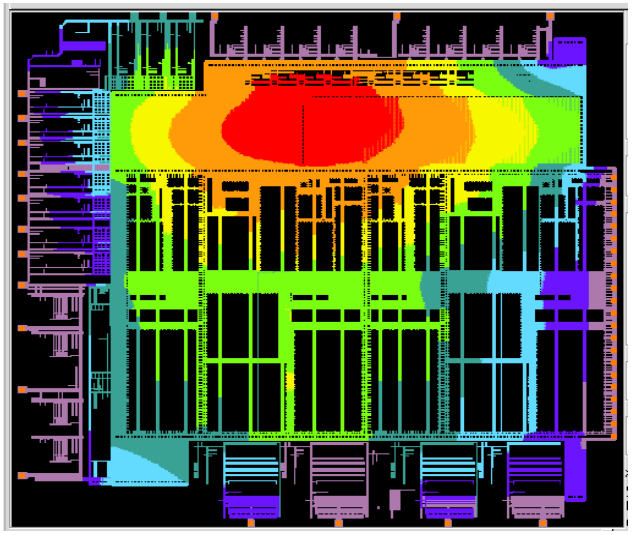
Both Power and Ground Nets solved simultaneously

Viewing Voltage Drop Map for Wires

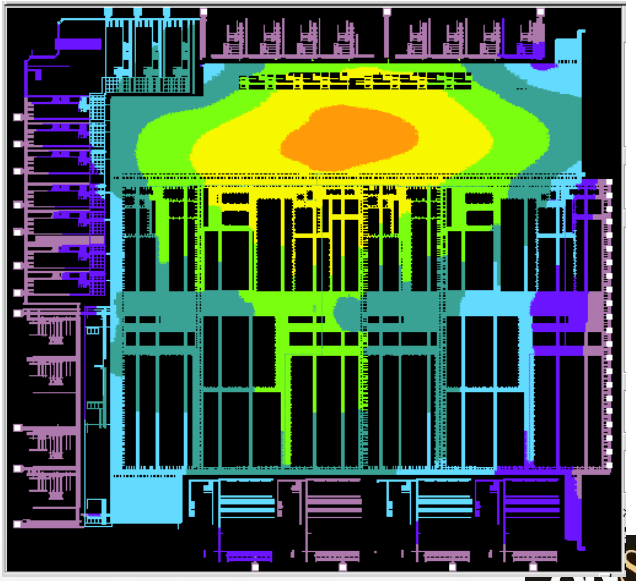
View > Voltage Drop Maps > Wire&Via



VDD + VDD_INT

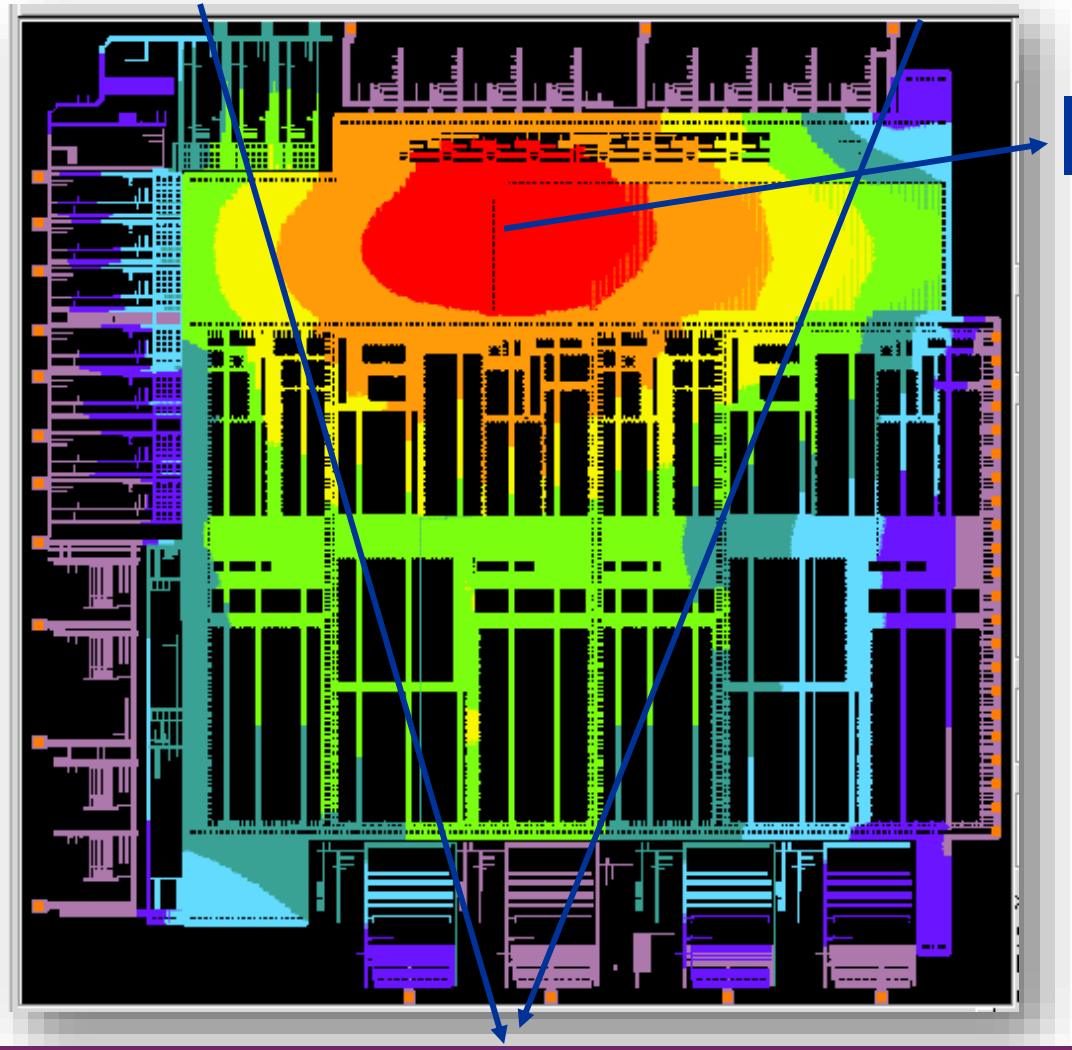


VSS



Use View -> Nets Menu for selecting individual nets

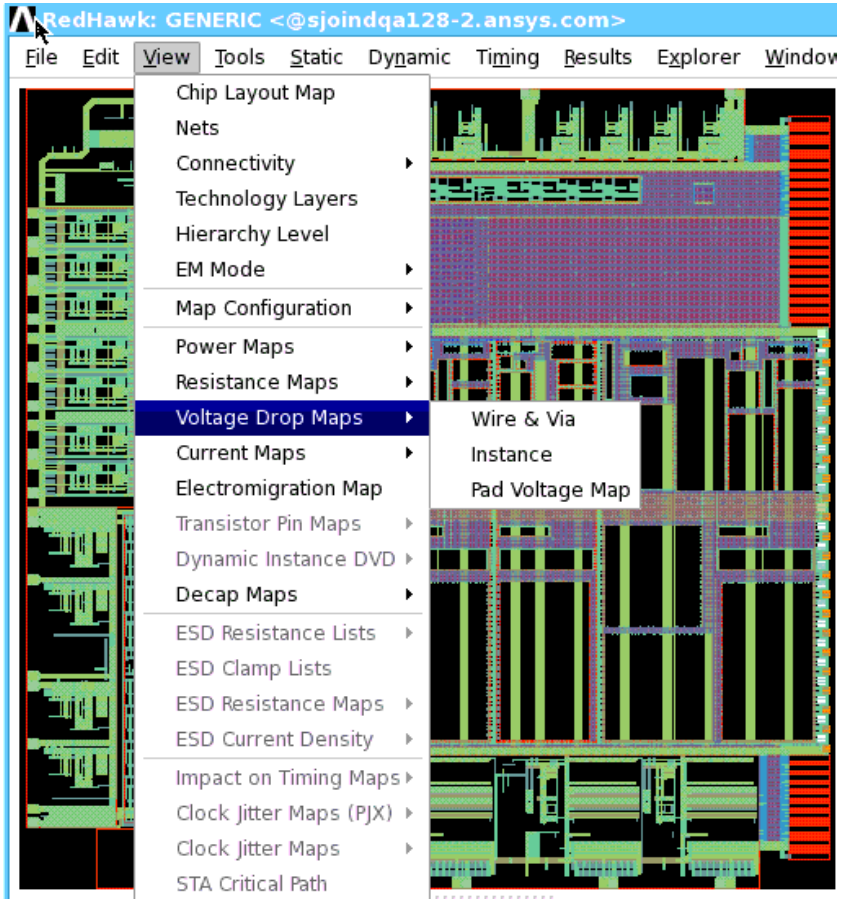
Debugging Voltage Drop

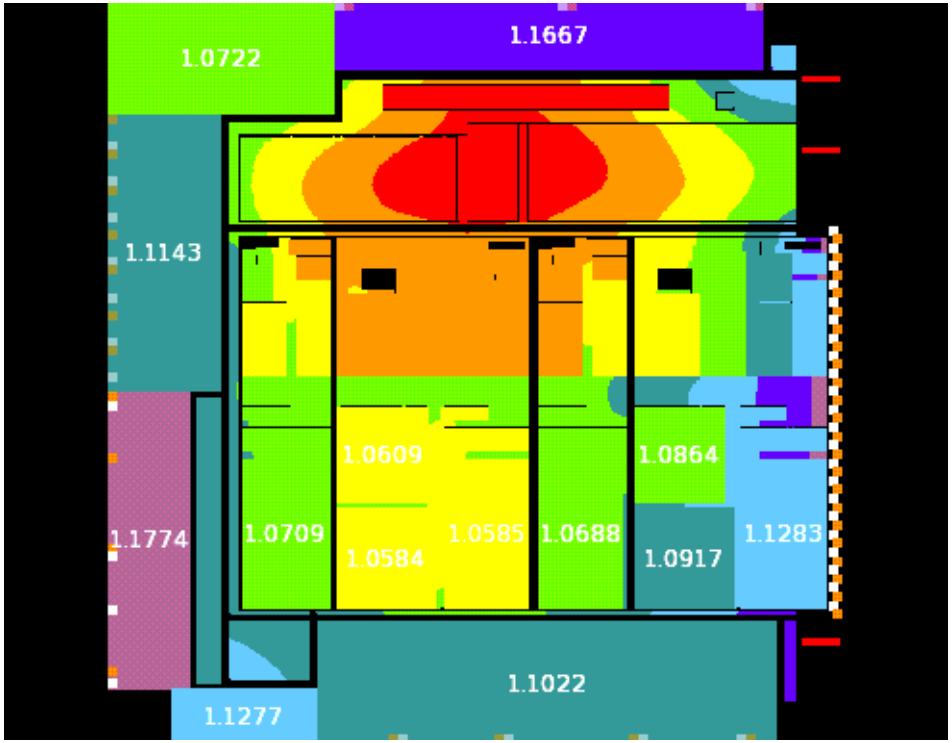


Drop is due to inadequate number of pads at the corner and at the top

Viewing Voltage Drop Map for Instances

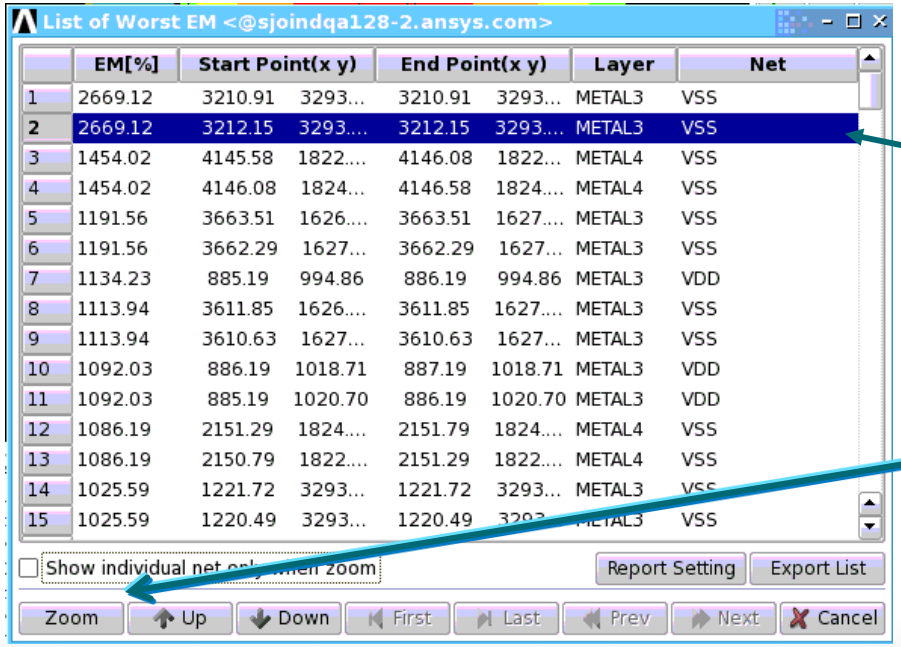
View > Voltage Drop Maps > Instance





Violations Browsing

- **Purpose: Enables browsing of IR,EM violations**
- **View report**
  - Results → List of Worst IR Instances for Static Simulation
  - Results → List of Worst EM for Static Simulation
  - Results → List of Worst IR for Wire & Via for Static Simulation
  - Results → List of Highest Power Instances for Static Simulation



Select violation interest

Zoom to selected instance

Example – EM Issues

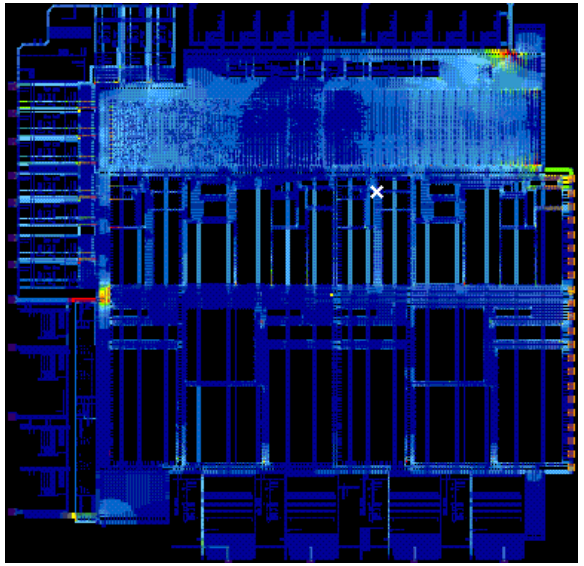
List of Worst EM <@sjoindqa128-2.ansys.com>

	EM[%]	Start Point(x y)		End Point(x y)		Layer	Net
1	2669.12	3210.91	3293...	3210.91	3293...	METAL3	VSS
2	2669.12	3212.15	3293....	3212.15	3293....	METAL3	VSS
3	1454.02	4145.58	1822....	4146.08	1822...	METAL4	VSS
4	1454.02	4146.08	1824...	4146.58	1824....	METAL4	VSS
5	1191.56	3663.51	1626....	3663.51	1627....	METAL3	VSS
6	1191.56	3662.29	1627...	3662.29	1627...	METAL3	VSS
7	1134.23	885.19	994.86	886.19	994.86	METAL3	VDD
8	1113.94	3611.85	1626....	3611.85	1627....	METAL3	VSS
9	1113.94	3610.63	1627...	3610.63	1627...	METAL3	VSS
10	1092.03	886.19	1018.71	887.19	1018.71	METAL3	VDD
11	1092.03	885.19	1020.70	886.19	1020.70	METAL3	VDD
12	1086.19	2151.29	1824....	2151.79	1824....	METAL4	VSS
13	1086.19	2150.79	1822....	2151.29	1822....	METAL4	VSS
14	1025.59	1221.72	3293...	1221.72	3293...	METAL3	VSS
15	1025.59	1220.49	3293...	1220.49	3293...	METAL3	VSS

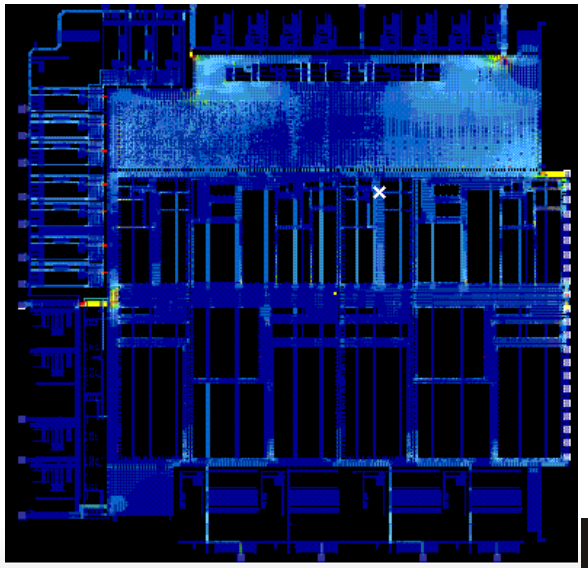
Show individual net only when zoom | Report Setting | Export List

Zoom | Up | Down | First | Last | Prev | Next | Cancel

VDD



VSS

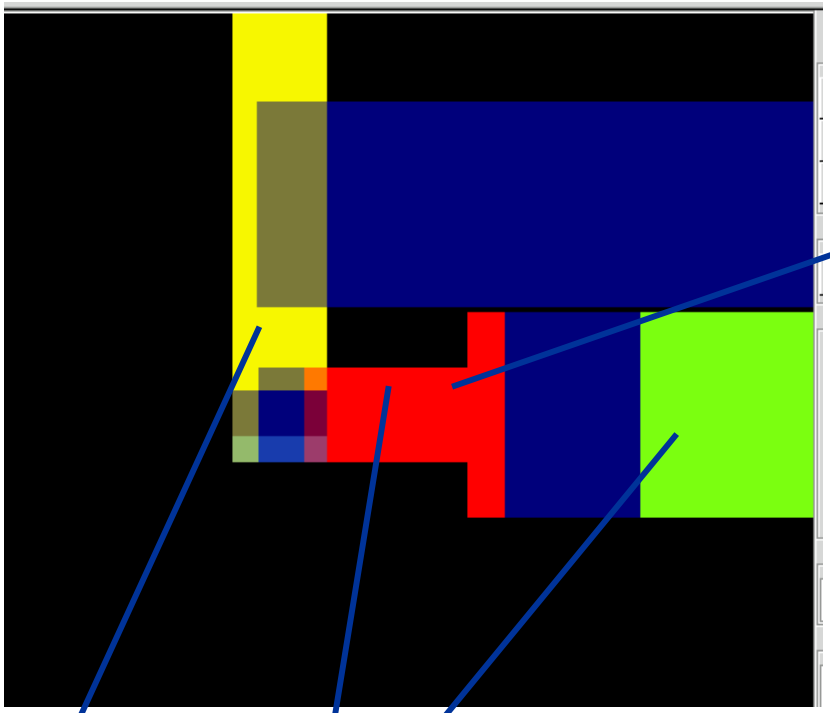


Less false EM violations due to accurate prediction of current direction

Debugging EM Violations

GUI> zoom rect 1500 4480 1600 4500

Highlight only METAL5 and METAL6, then click on the EM map button



METAL6

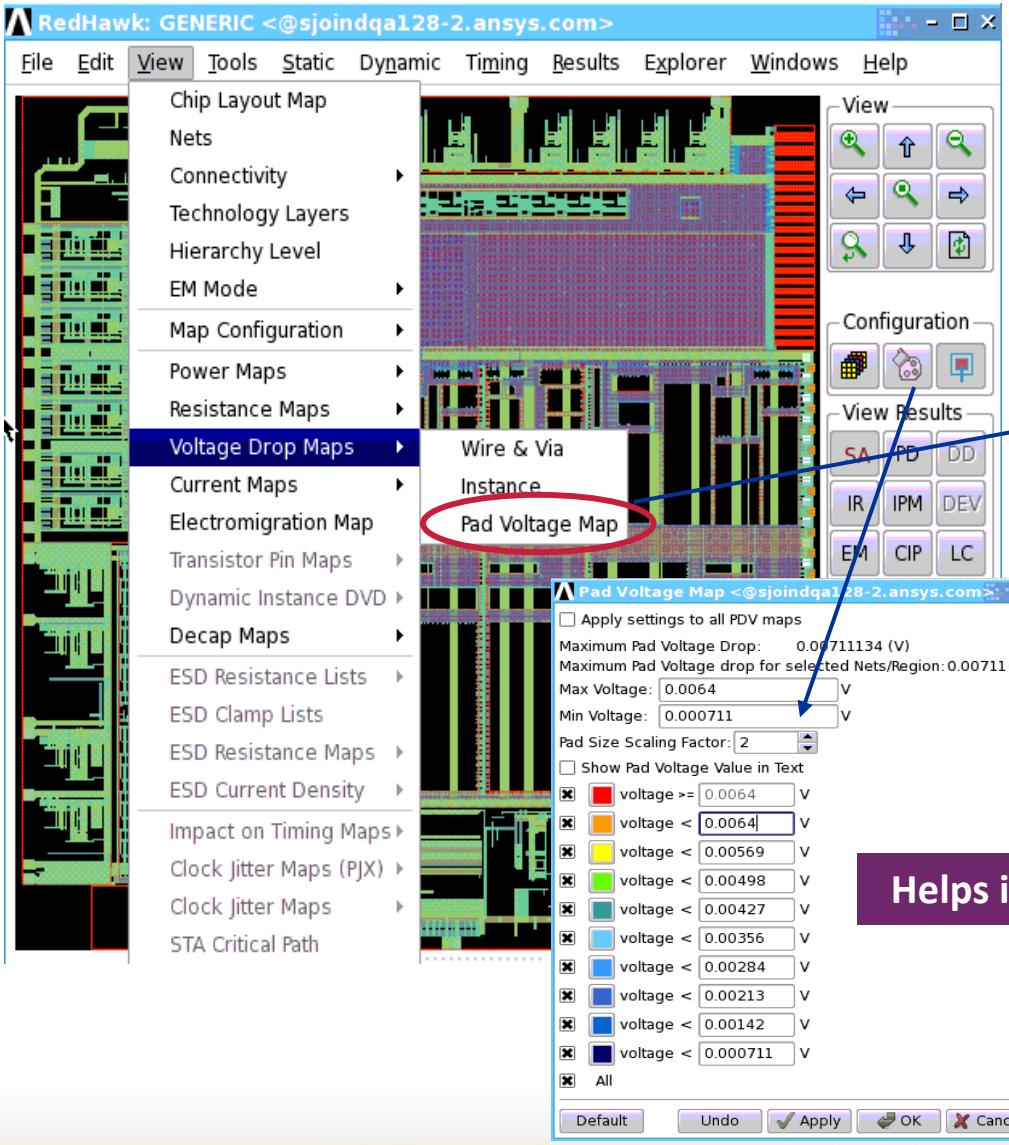
METAL5

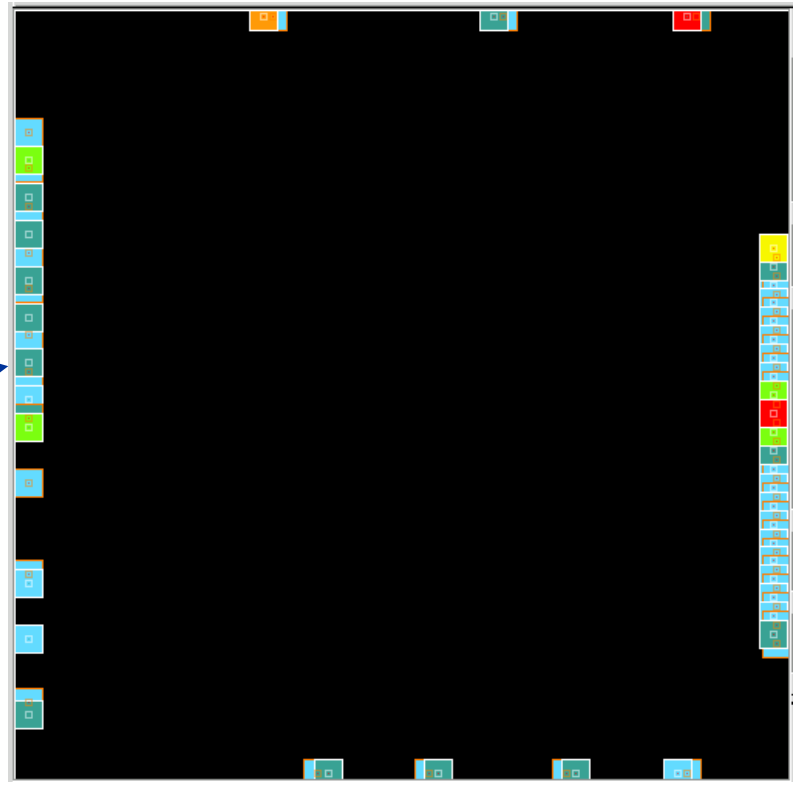
EM violation is caused due to narrowing of METAL5

The EM limit for METAL6 is very high compared to METAL5, hence there is no violation

Pad Voltage Map

View > Voltage Drop Maps > Pad Voltage Map





Helps in analyzing distribution and number of pads !

Static Analysis Reports

In adsRpt/Static/

GENERIC.inst.worst GENERIC.inst GENERIC.inst.arc	Instance voltage drop
GENERIC.ir.worst *GENERIC.ir(Use tcl command: report ir -routing -o adsRpt/Static/GENERIC.ir*)	Wire voltage drop
GENERIC.em.worst	List of EM violations
pad.current	DC current through each voltage source

Result Exploration using RedHawk Explorer

Summary Section

RedHawk™-Explorer

ANSYS

Summary | Data Integrity | Design Weakness | Hotspots | Performance

Back Forward 3D-IC FAQ

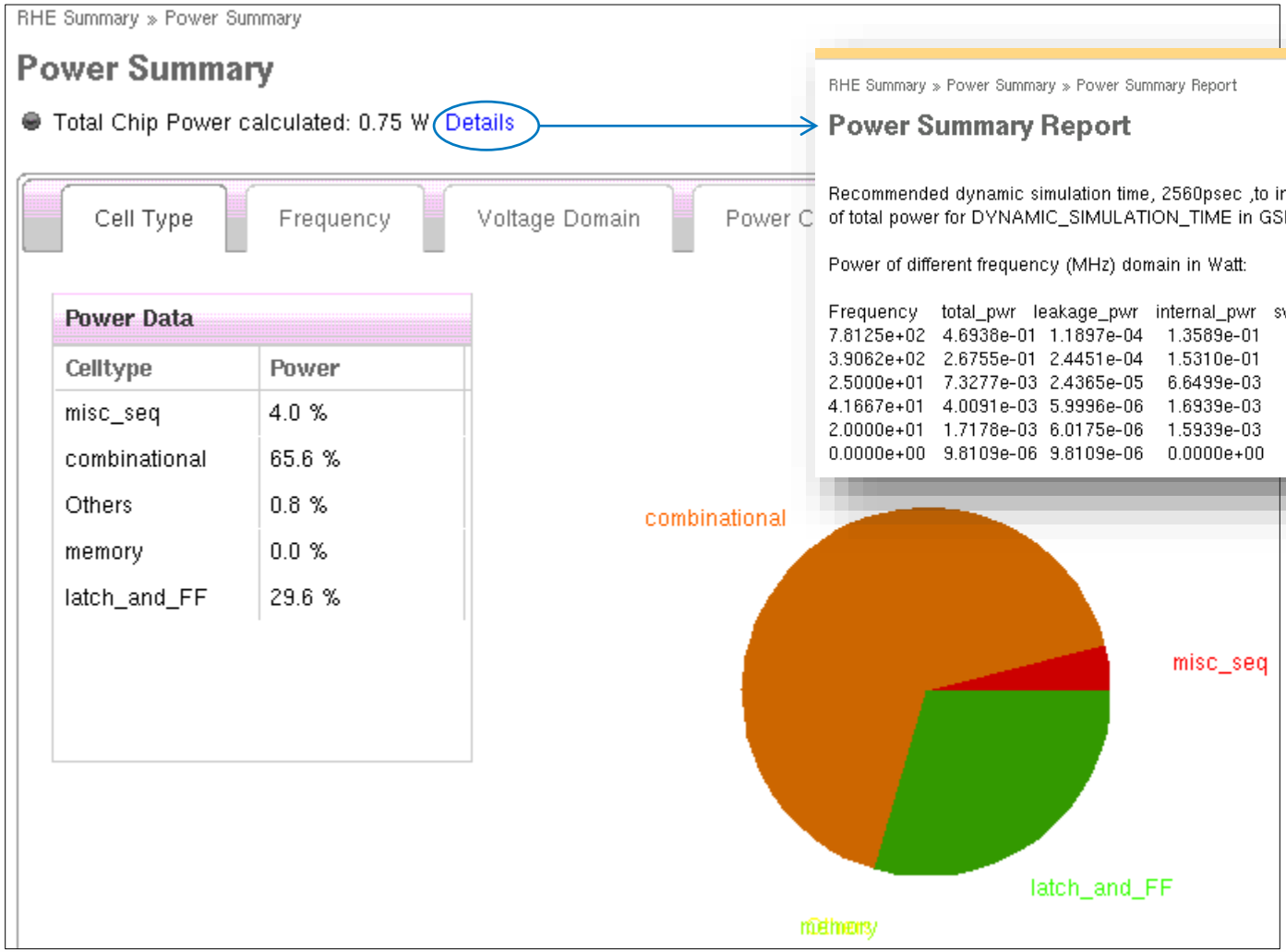
- Design Summary
- Results Summary
  - Power Summary
  - Static Voltage Drop Summary
  - Dynamic Voltage Drop Summary
  - Current w/f Summary
  - Power EM Summary
  - Signal EM Summary
  - PathFinder Summary
  - Low Power Analysis Summary
  - CPM Summary
- Run Details

Design Statistics

Key Parameters	
Design Name	GENERIC
Design Size	4920.62u x 5000.36u
Instance Count	476302
No of Voltage domains	2(Power) & 1(Ground)
Total Power	0.75 W
Dominant Frequency	390.62 MHz
Temperature	Details
Min Supply Voltage	1.2 V

Chip Layout

Power Summary



RHE Summary » Power Summary » Power Summary Report

Power Summary Report

Recommended dynamic simulation time, 2560psec ,to include 98.2581% of total power for DYNAMIC_SIMULATION_TIME in GSR

Power of different frequency (MHz) domain in Watt:

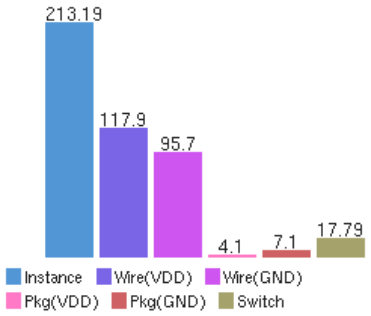
Frequency	total_pwr	leakage_pwr	internal_pwr	switching_pwr	%_total_pwr
7.8125e+02	4.6938e-01	1.1897e-04	1.3589e-01	3.3338e-01	6.2584e+01
3.9062e+02	2.6755e-01	2.4451e-04	1.5310e-01	1.1421e-01	3.5674e+01
2.5000e+01	7.3277e-03	2.4365e-05	6.6499e-03	6.5344e-04	9.7703e-01
4.1667e+01	4.0091e-03	5.9996e-06	1.6939e-03	2.3092e-03	5.3455e-01
2.0000e+01	1.7178e-03	6.0175e-06	1.5939e-03	1.1782e-04	2.2904e-01
0.0000e+00	9.8109e-06	9.8109e-06	0.0000e+00	0.0000e+00	1.3081e-03

Static Analysis Summary

Worst Voltage Drop | Activity Summary | Instance Based StaticIR Histogram

Worst Voltage Drop Data

Type	Drop (mV)
Instance	213.19 mV (17.77 %)
Wire(VDD)	117.9 mV (9.82 %)
Wire(GND)	95.7 mV (7.97 %)
Pkg(VDD)	4.1 mV (0.3 %)
Pkg(GND)	7.1 mV (0.6 %)
Switch	17.79 mV (1.48 %)

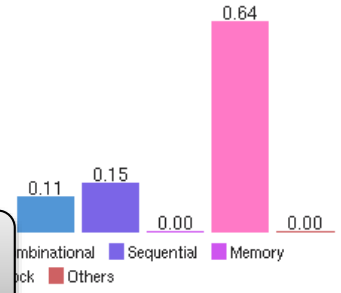


Voltage Drop Break up

Worst Voltage Drop | Activity Summary | Instance Based StaticIR Histogram

Instance Toggle Data

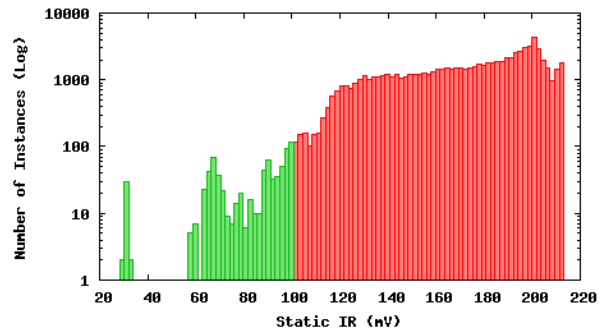
Type	Average Toggle Rate
Combinational	0.11
Sequential	0.15
Memory	0.00
Clock	0.64
Others	0.00



Tells what % of instances are switching in dynamic simulation

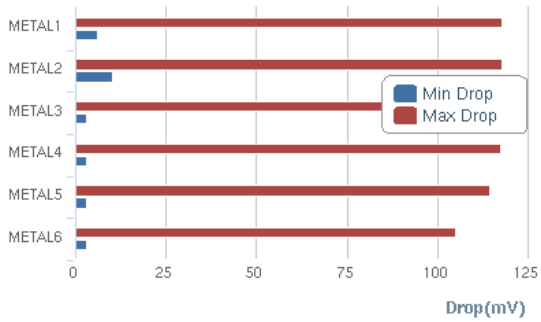
Worst Voltage Drop | Activity Summary | Instance Based StaticIR Histogram

Instance Based Static IR Histogram



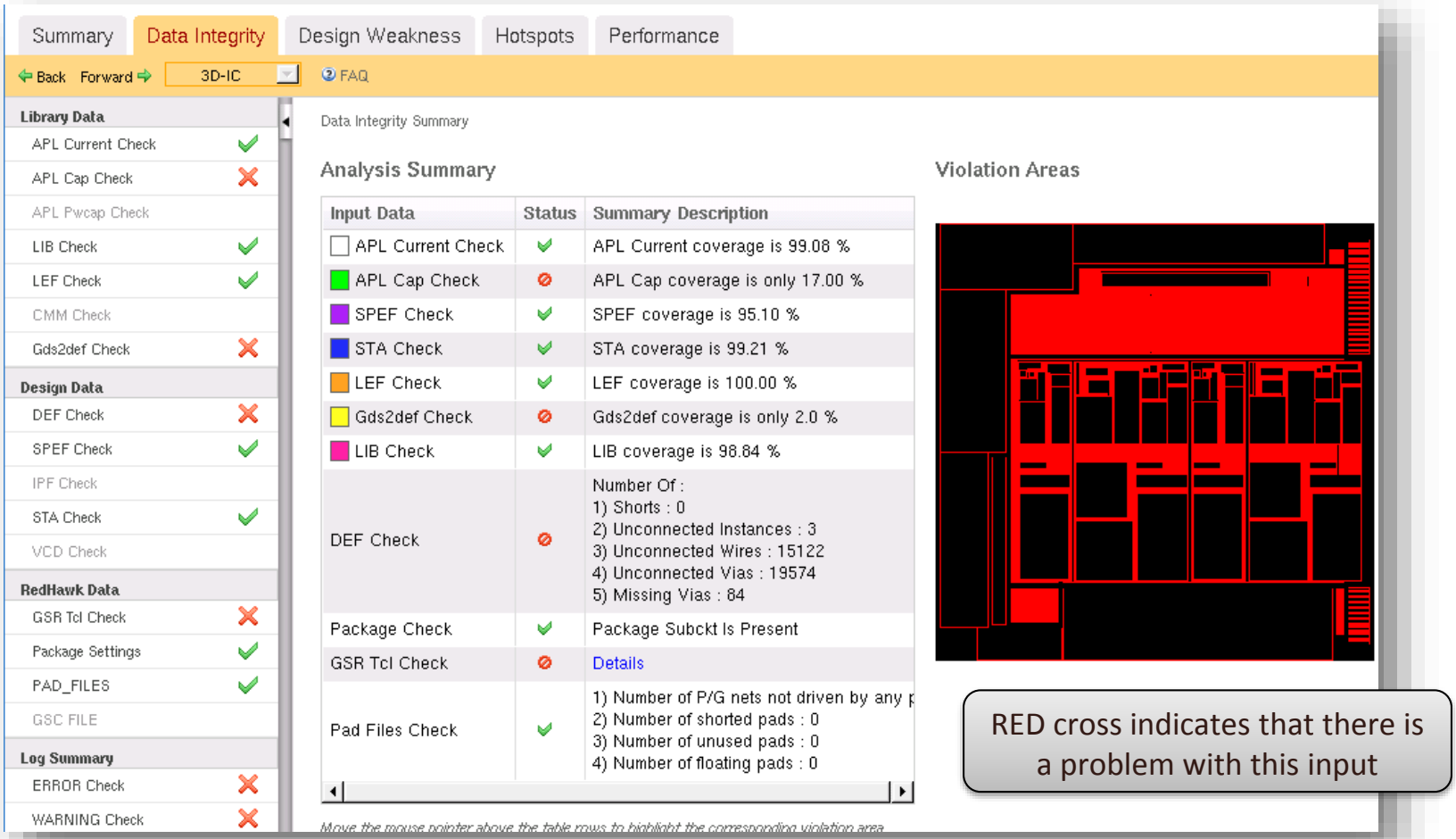
Worst Voltage Drop | Activity Summary | Instance Based StaticIR Histogram | Layer Wise Drop

Layer	Min Drop (mV)	Max Drop (mV)
METAL1	6.09	117.94
METAL2	10.22	117.88
METAL3	3.11	117.81
METAL4	3.10	117.83
METAL5	3.12	114.78
METAL6	3.12	105.35



ANSYS

Data Integrity Check Summary



- Design specific data integrity check
- Helps to identify and understand impact of missing data
- Breaks design into regions and presents missing data for each region

Data Integrity Check : DEF Check
Missing Via Debug

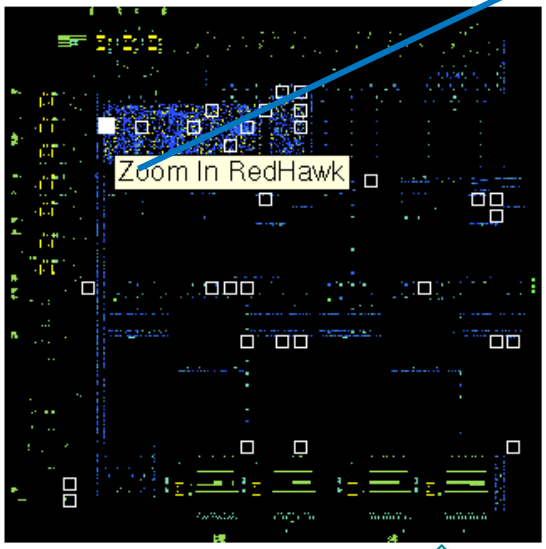
Shorts Check | Instance Unconnect | Wire Unconnect | Via Unconnect | Missing Via

MISSING VIAS CHECK

Check the number of missing vias in a design is not more than 10000

Number of missing vias Reported : 84

Highlighting Regions with Missing Via in GUI



Direct zoom into RH GUI by clicking on the image

RH Crossprobing Options

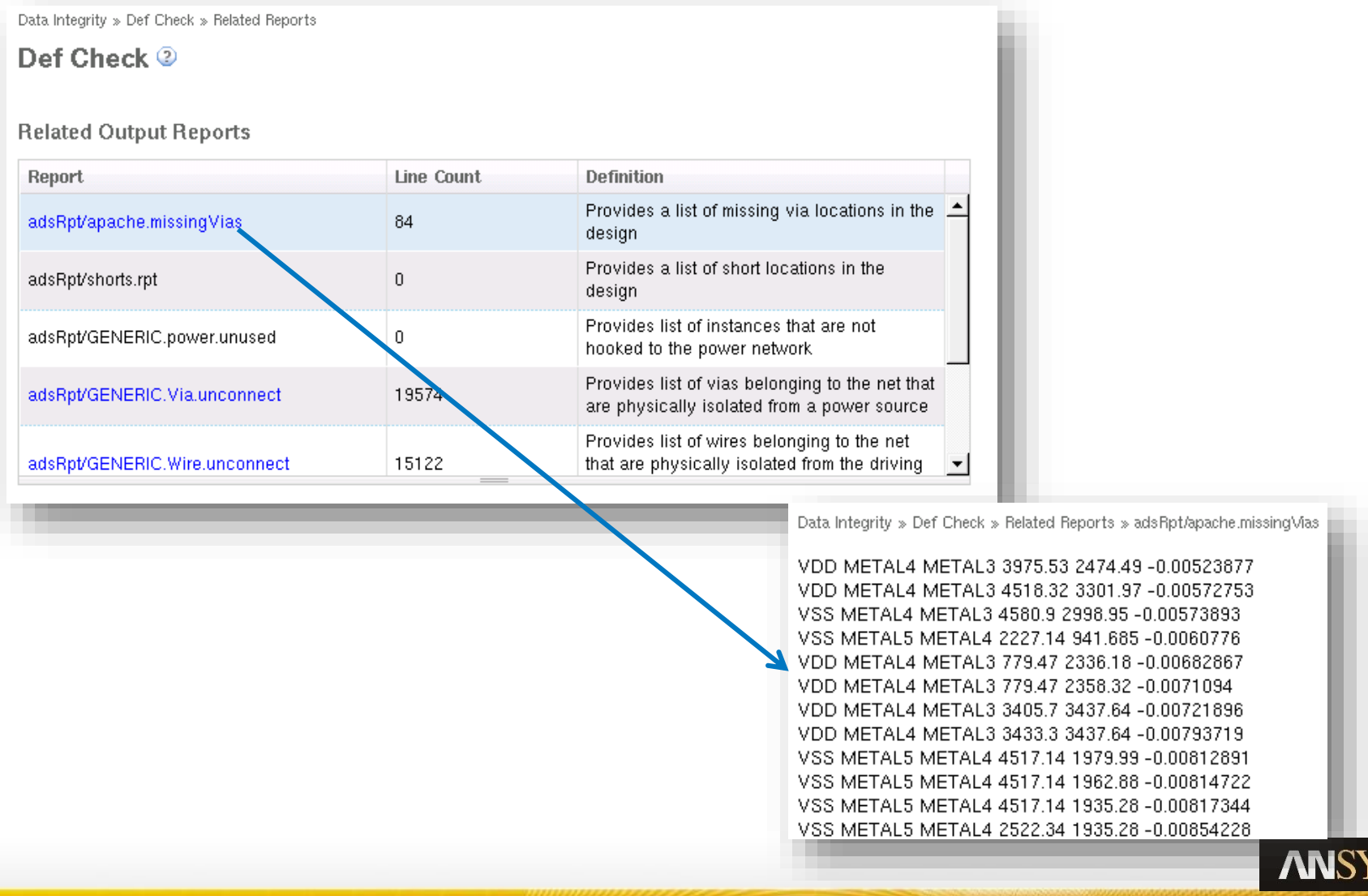
Highlight Color

Show in RedHawk

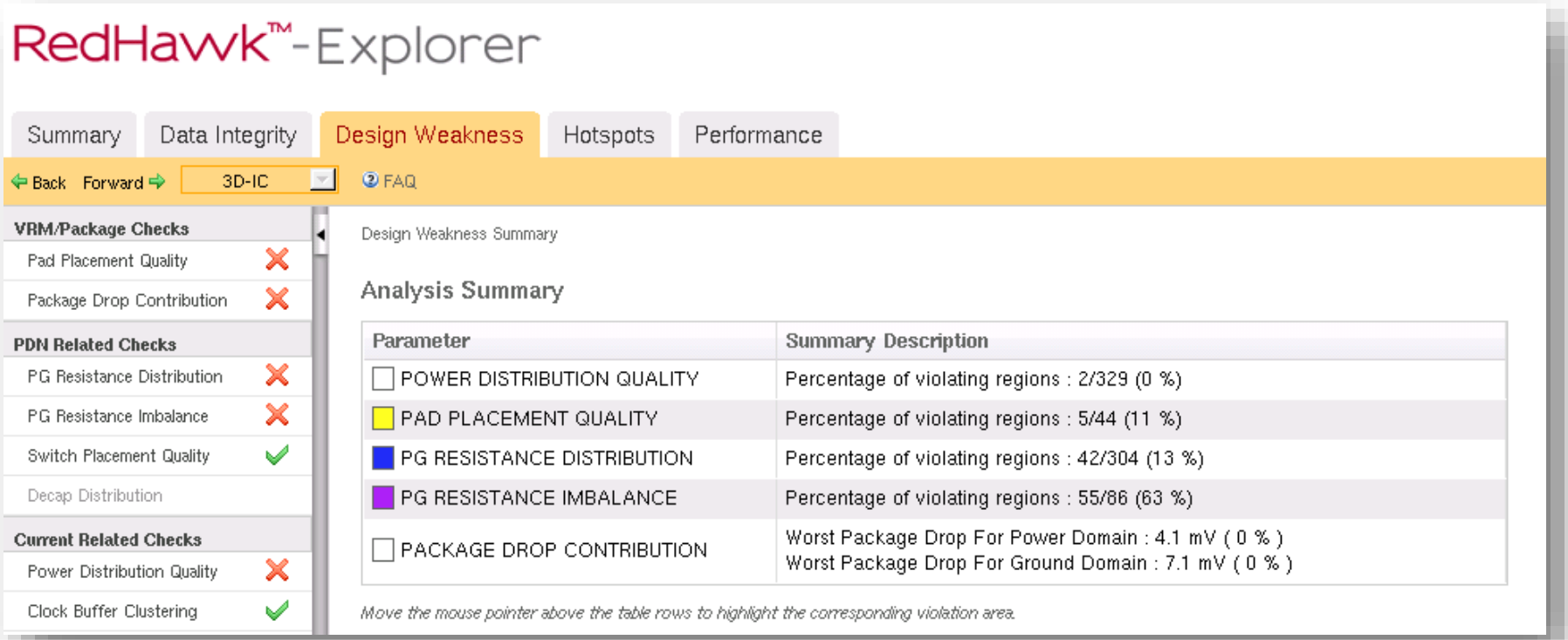
Highlights Regions with missing vias
(User can click and zoom into RH)

Exact locations highlighted with marker

DEF Check: Related Reports



Design Weakness Checks Summary



- Ranks Different Regions in the design for Various Design Weakness Parameters
- Identifies Regions Affected with Design Quality Issues

Design Weakness Analysis Example

PG Resistance Distribution Check

PG Resistance Distribution Check

Checks whether the PG Resistance in any region is greater than 2 times Average PG Resistance(24.3

Number of Regions with Violations : 42/304 (13.81 %)

Top Violations

Region	PG Resistance Ra	Zoom	Details
1	2.94		Details
2	2.91		Details
3	2.86		Details
4	2.85		Details
5	2.84		Details

Histogram | Voltage Drop | Cross Probing

RH Crossprobing Options

Highlight Color

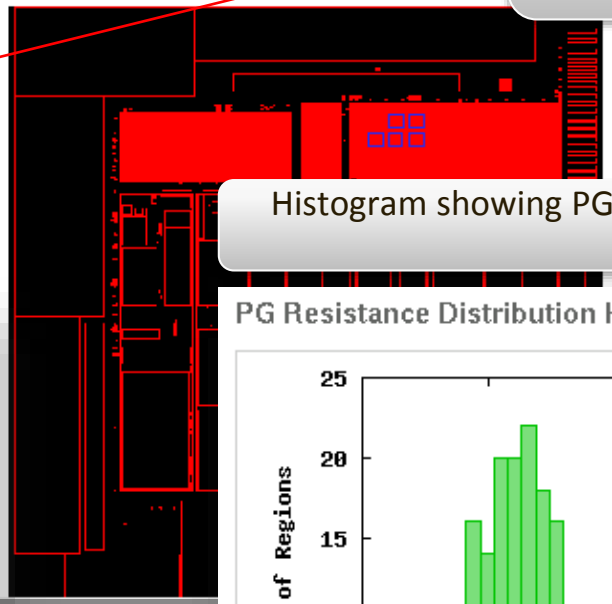
Threshold Range: 2

Number of Violations: 5

Show in RedHawk | Reload Reports

Changing the constraints on-the-fly through cross-probing menu

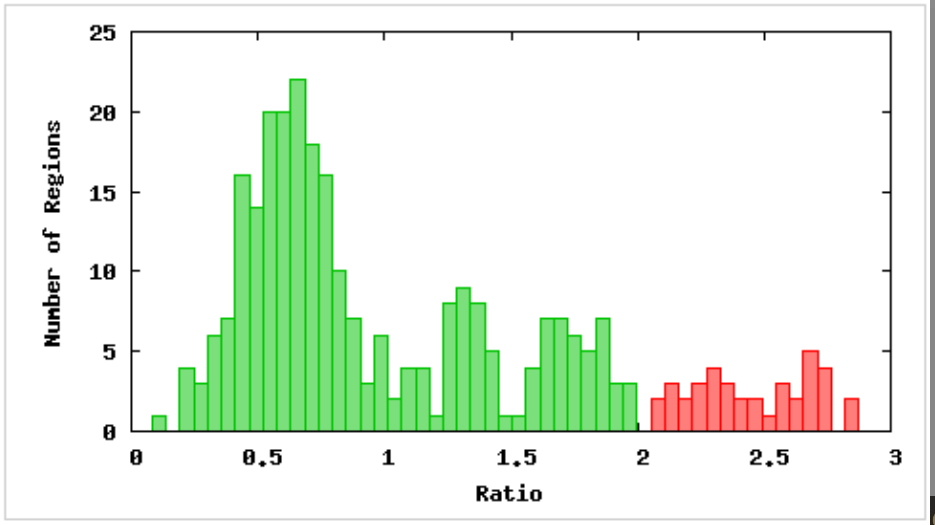
Issues Highlighted in GUI



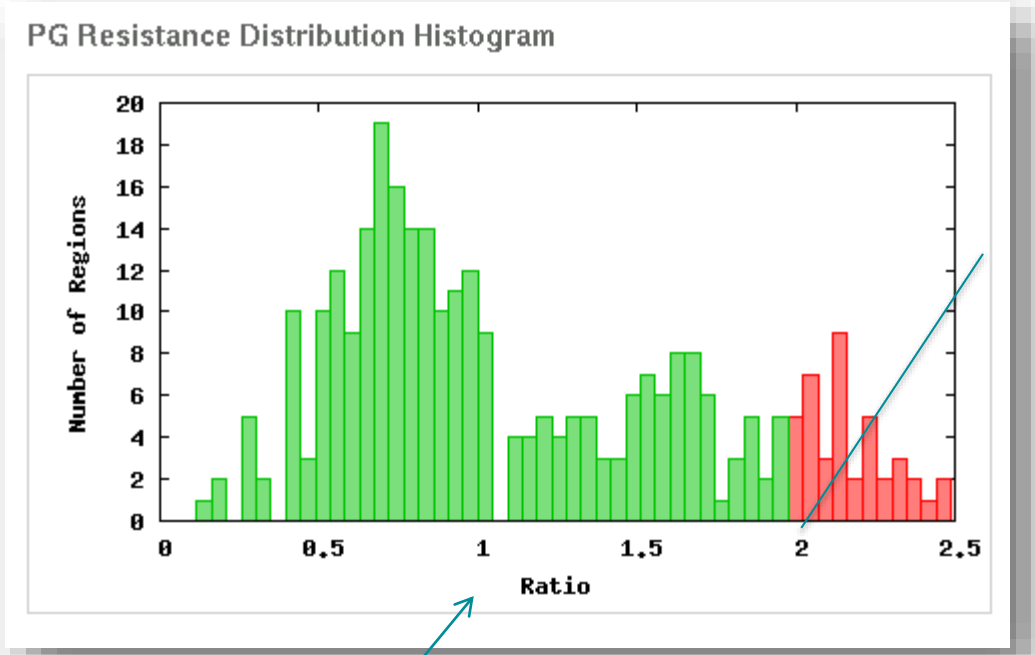
Indicates that PG Resistance in this region is 2.94 X higher than the average PG Resistance obtained from all regions

Histogram showing PG Resistance distribution in different regions

PG Resistance Distribution Histogram



Interpreting Histograms in RHE



Simple interpretation:
Ratio 2 means this region is 2X weaker than other part of the design

How is this ratio computed in this example ?

- STEP-1 : RHE computes the peak resistance for each region (REGION-R)
- STEP-2 : Average resistance across all the regions is computed (AVG-R)
- STEP-3 : PGR Design Weakness Ratio for each region is computed as REGION-R/AVG-R

Cross-probing violations in RedHawk GUI

PG Resistance Distribution Check

Checks whether the PG Resistance in any region is greater than 2 times Average PG Resistance(24.350 ohm)

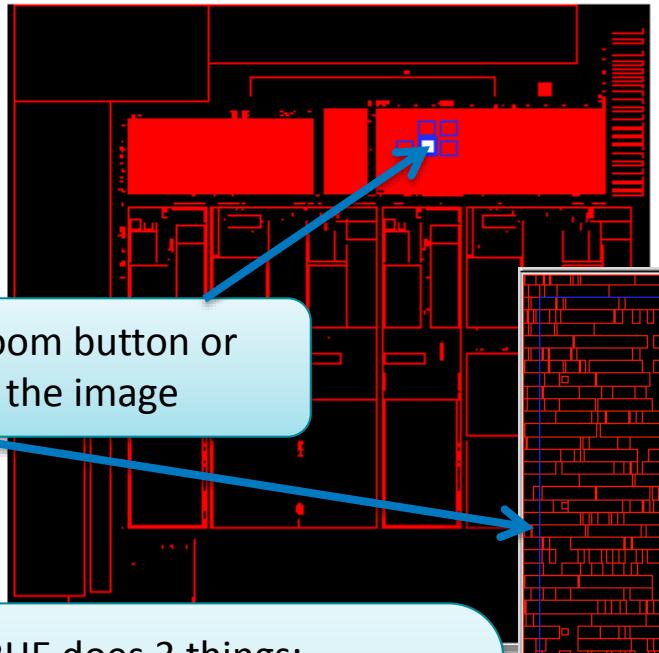
Number of Regions with Violations : 42/304 (13.81 %)

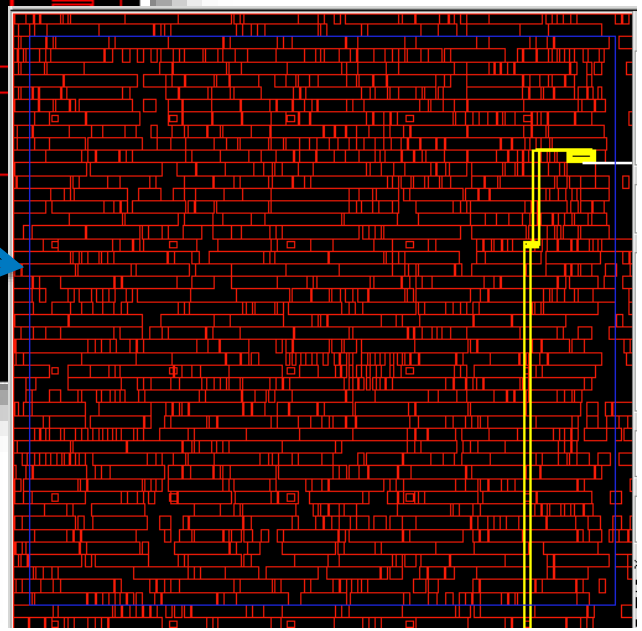
Top Violations

Region	PG Resistance Ra	Zoom	Details
1	2.94		Details
2	2.91		Details
3	2.86		Details
4	2.85		Details
5	2.84		

Move the mouse pointer
to highlight the correspo

Issues Highlighted in GUI





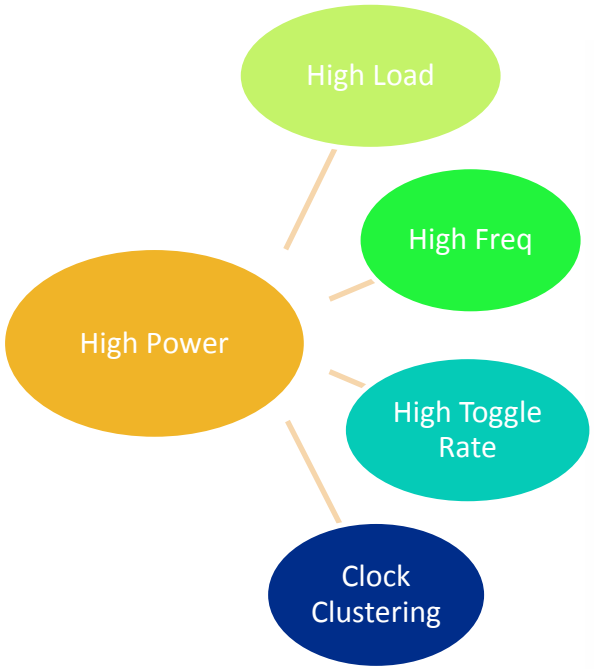
User can click on zoom button or directly click on the image

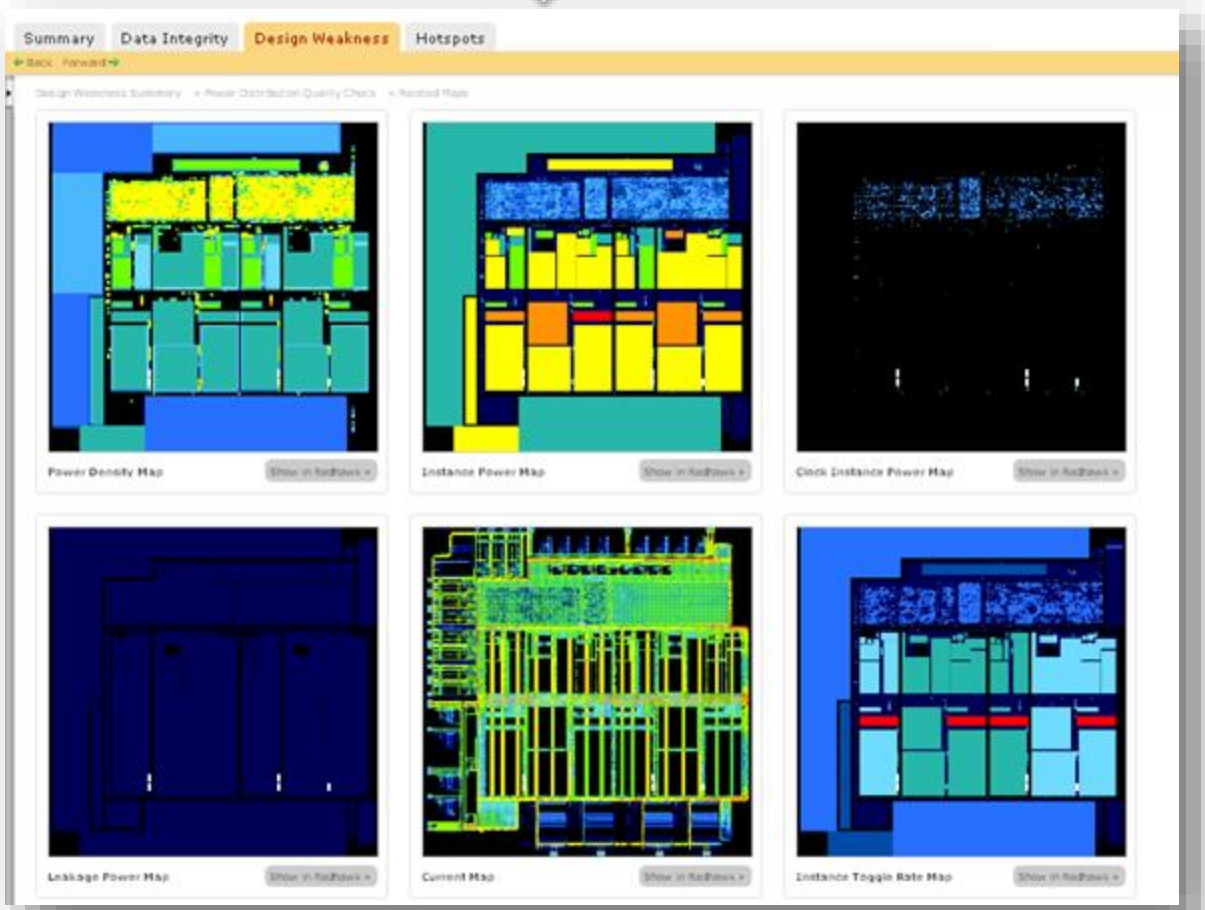
When you click on the image, RH/RHE does 3 things:

- Zooms into the violating regions
- Highlights the worst instance within the regions
- Update the map with some relevant views
  - Example, PG resistance map will display SPT for the worst instance

Design Weakness Analysis
Related Maps Section

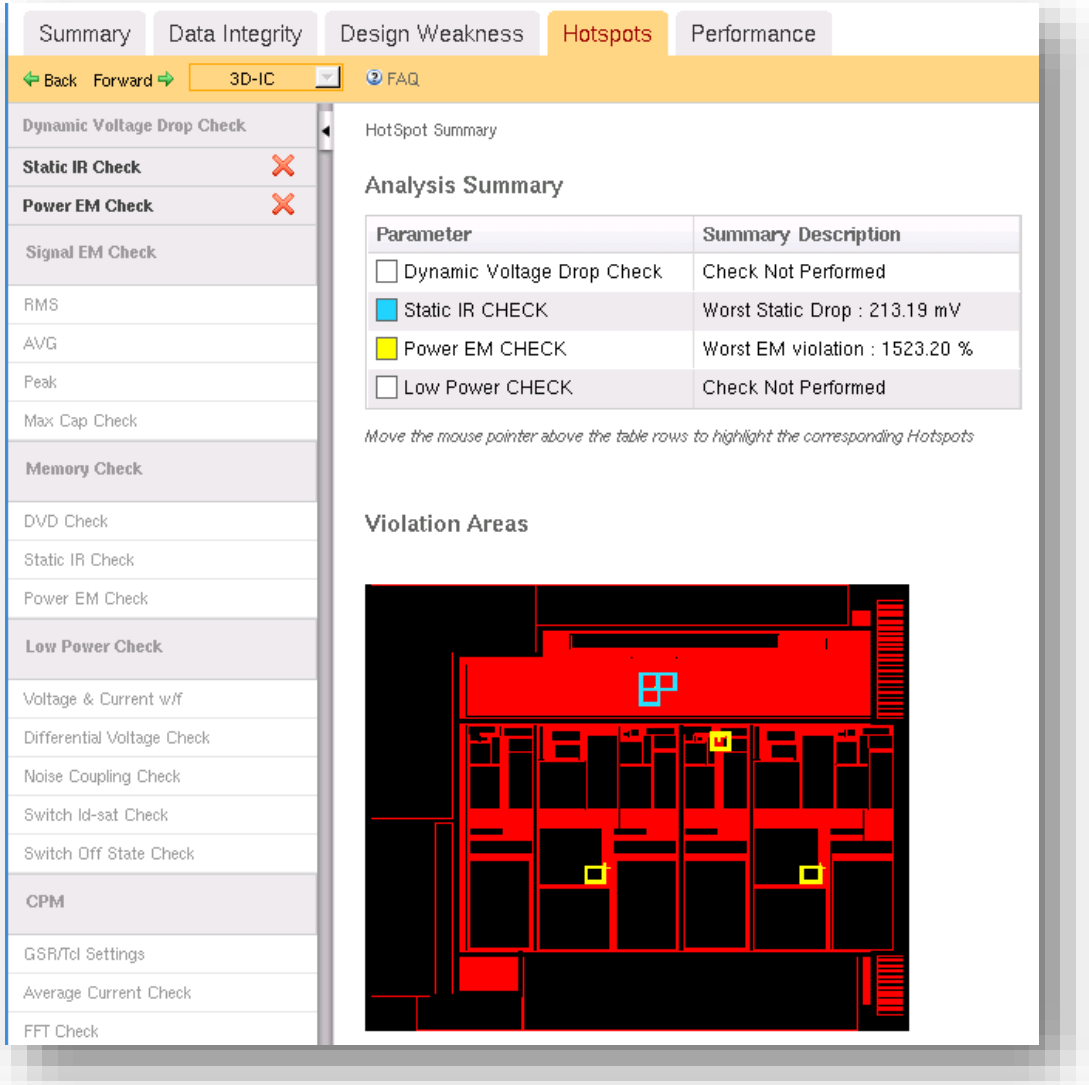
Design Weakness -> Power Distribution Quality -> Related Maps



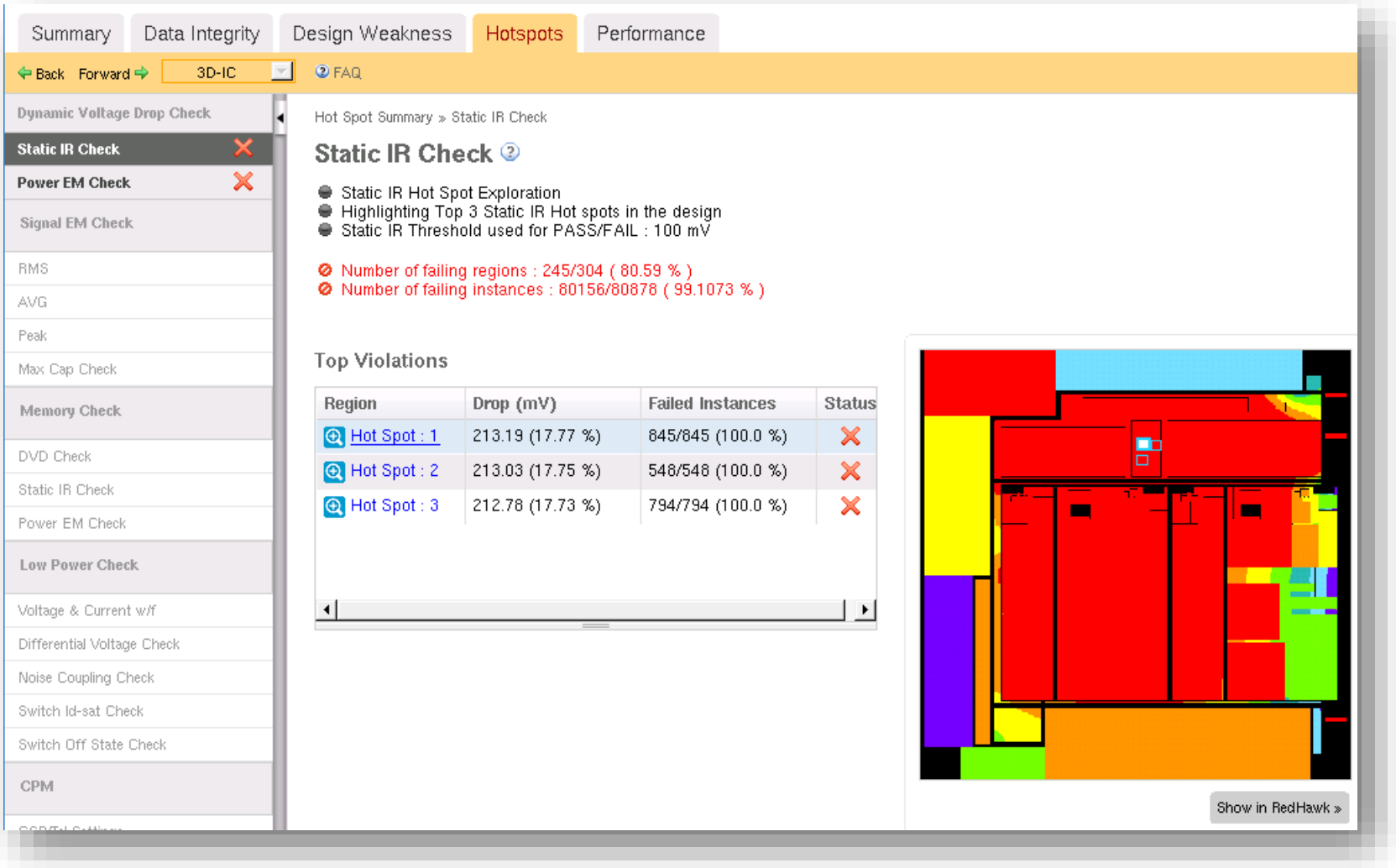


Related maps section helps identifying the exact cause for a weakness

Hotspot Analysis Summary



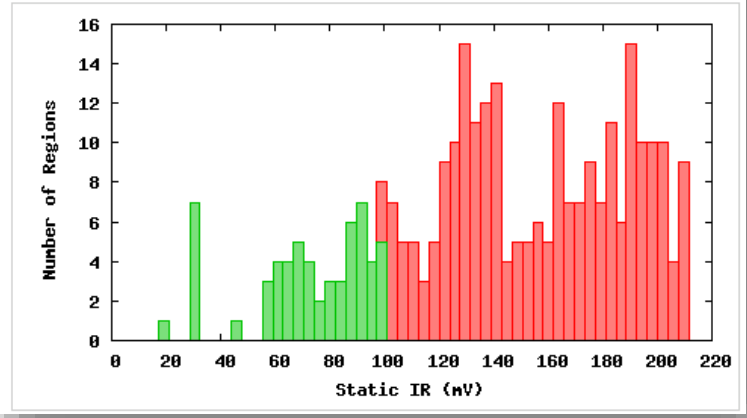
Static IR Check : Summary



Static IR Check : Summary

Histogram | Domain Based : Instance Drop | Domain Based : Wire Drop

Static IR Distribution Histogram



Histogram | Domain Based : Instance Drop | Domain Based : Wire Drop | CrossProbing

RH Crossprobing Options

Highlight Color

Static Voltage Drop Limit (mV) 100

Number of Violations 3

Show in RedHawk

Histogram | Domain Based : Instance Drop | Domain Based :

Voltage Domain Based Hot spot Exploration

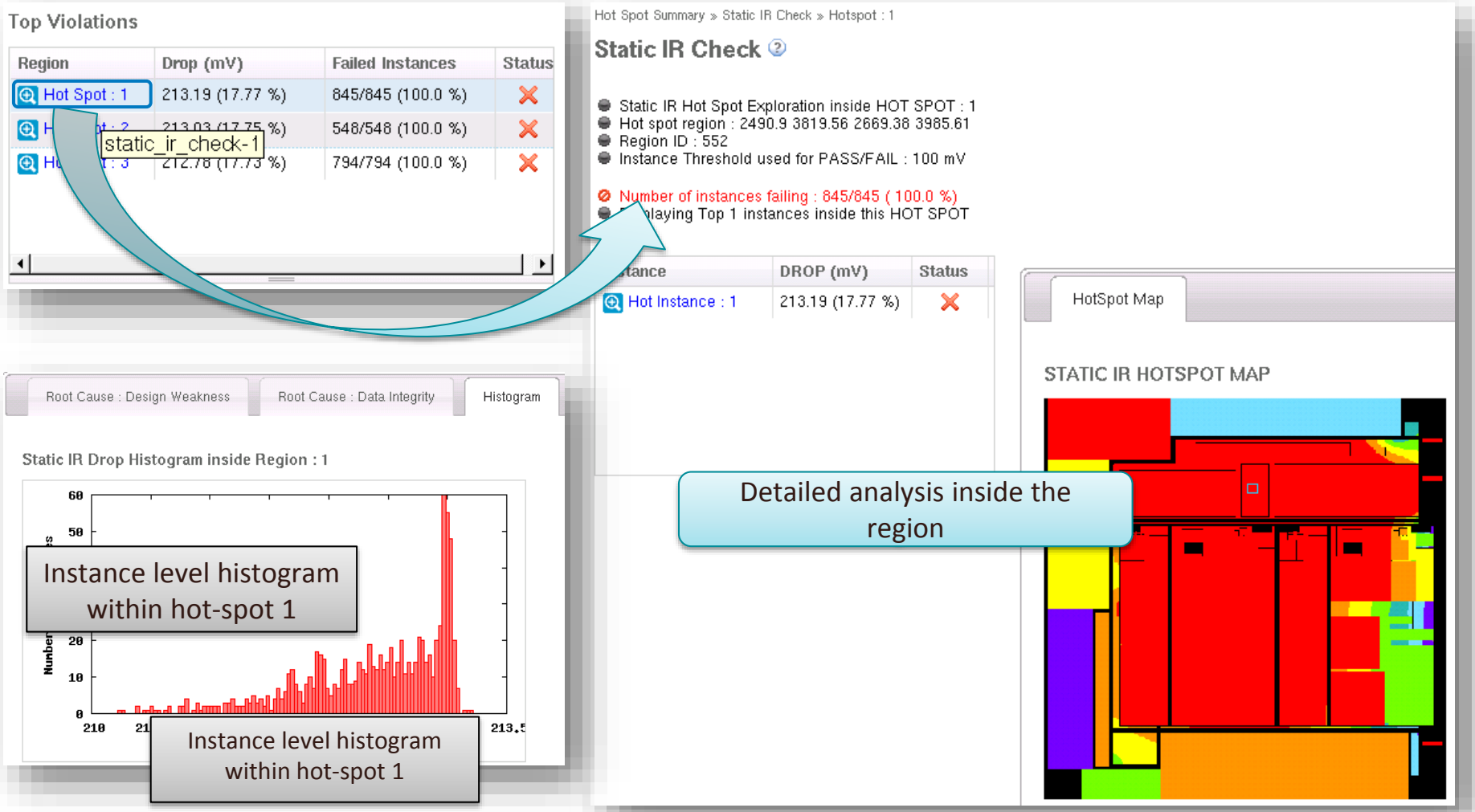
Domain	Failed Instances	Max Drop in mV(%)	Status
inst_129973/VDD_	40971/40971	202.73 (16.89 %)	✗
VDD	39185/39907	213.19 (17.77 %)	✗

Histogram | Domain Based : Instance Drop | Domain Based : Wire Drop

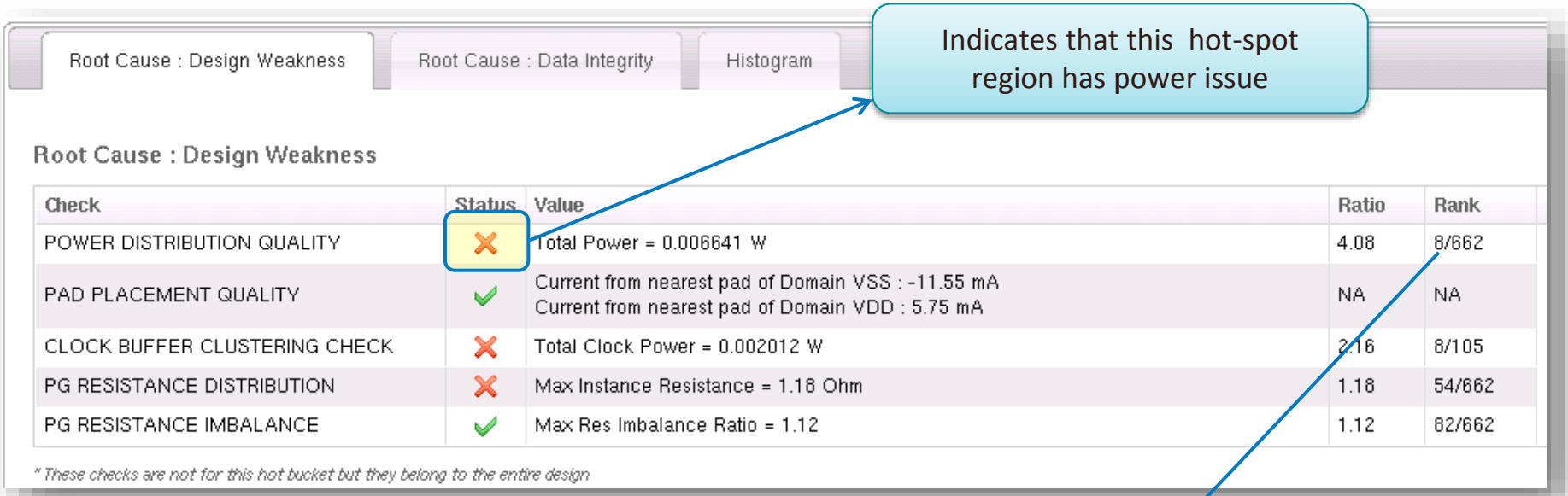
Voltage Domain Based Hot spot Exploration

Domain	Max Drop
VDD	117.943 mV
inst_129973/VDD_	108.496 mV

Static IR Check
Checking Hot-spot #1



Root Cause Identification
Design Weakness Analysis

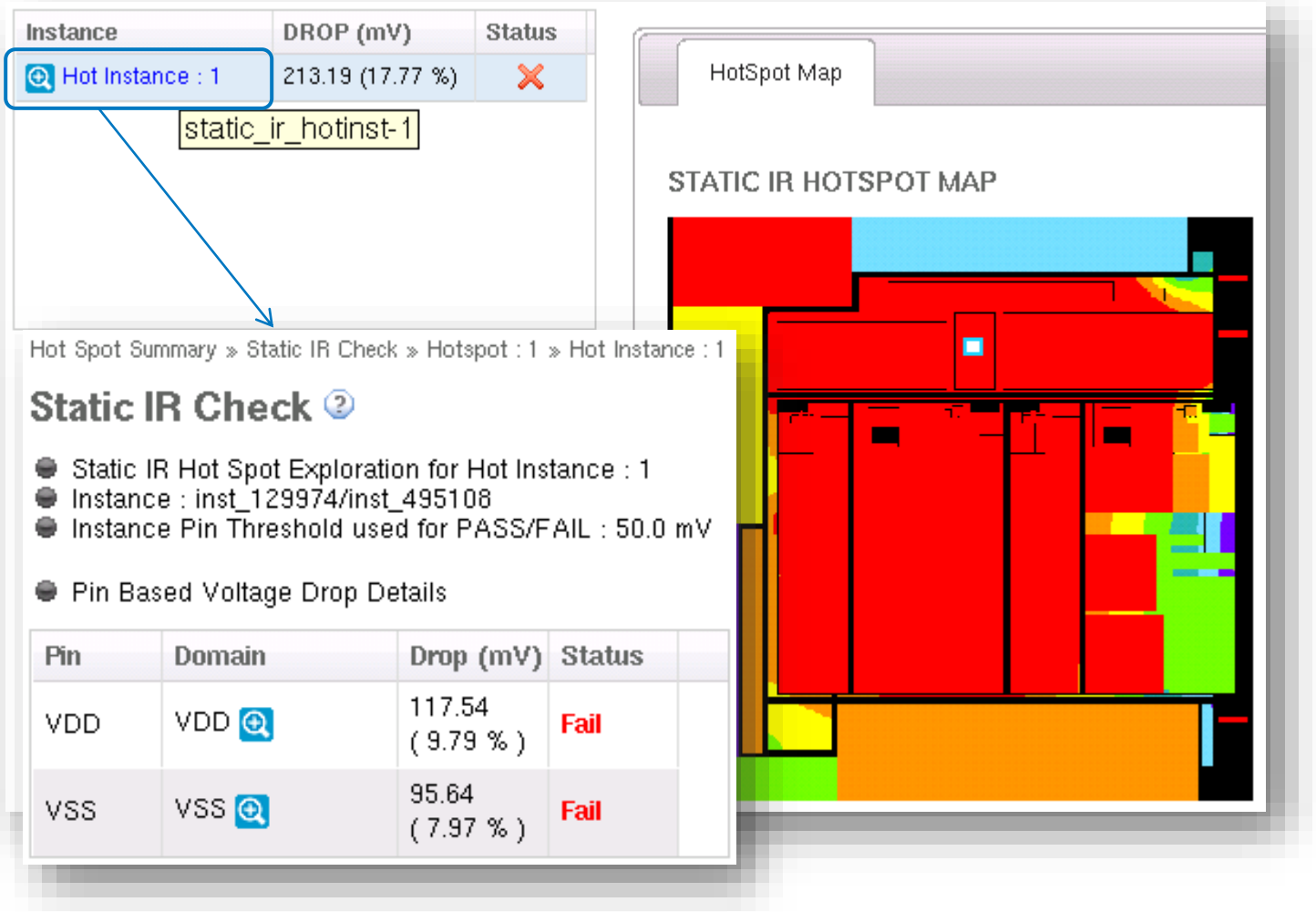


Indicates that this hot-spot region has power issue

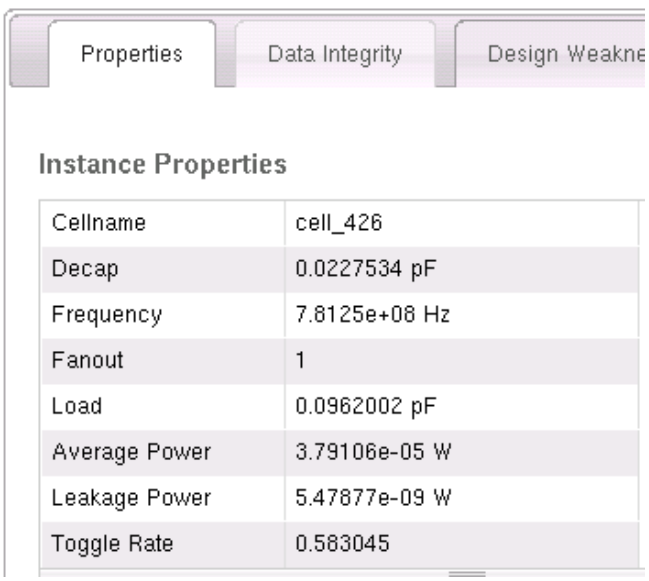
Design Weakness Ranking

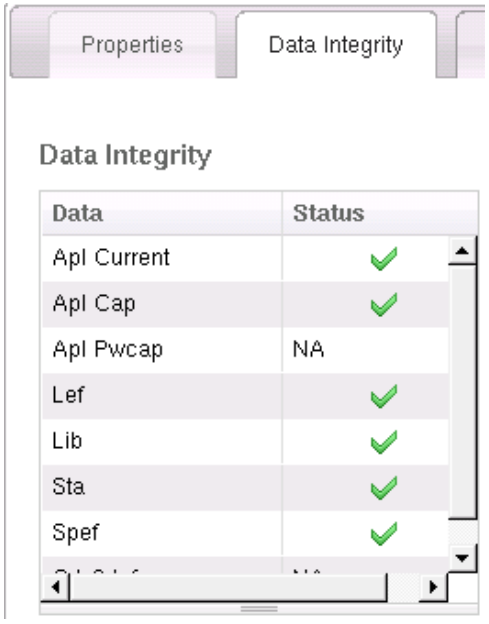
This hot-spot region ranks 8th among all regions in the design based on Power Distribution Quality Ranking
(Rank-1 indicates the weakest region)

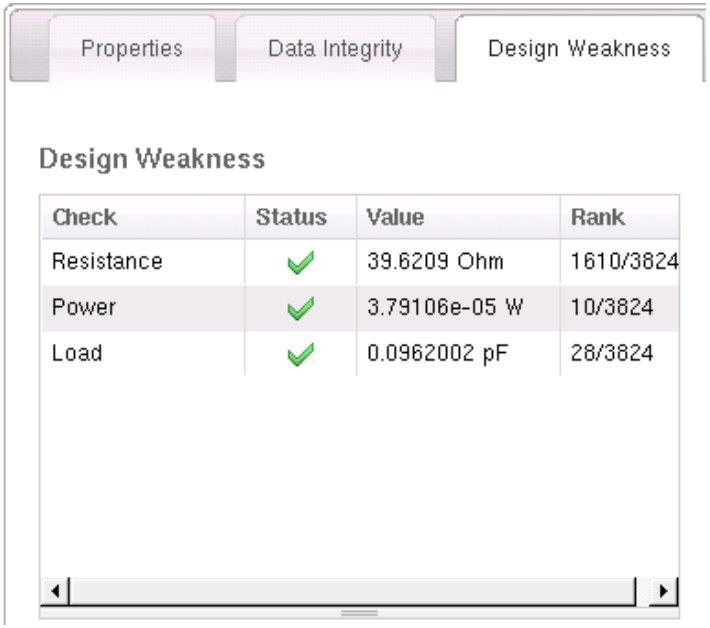
Static IR Check
Instance Level Debug



Static IR Check
Instance Level Debug







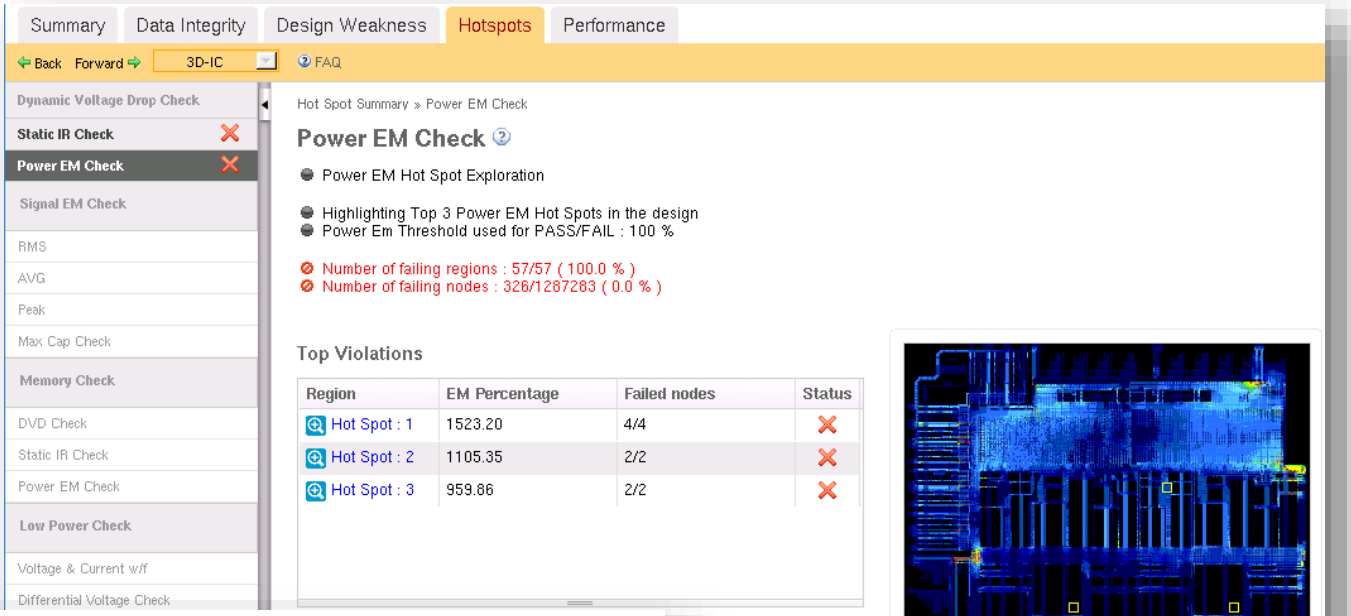
Static IR Check

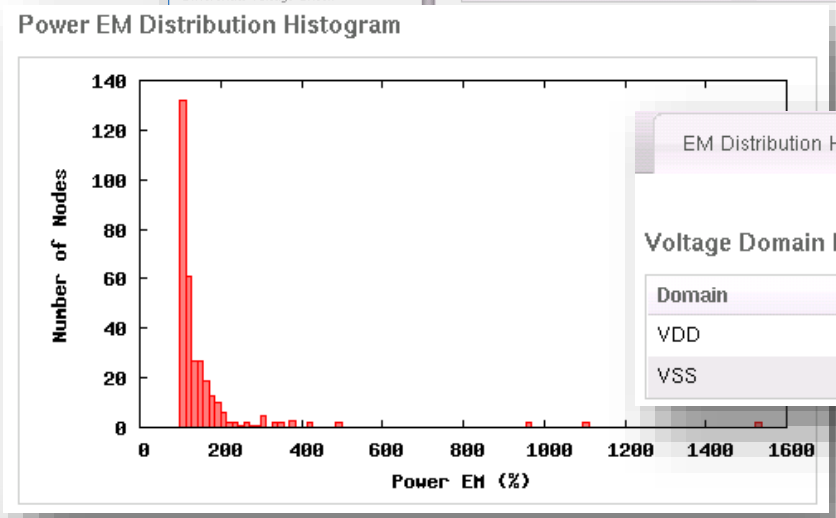
Instance Level Debug: SPT and Resistance Report

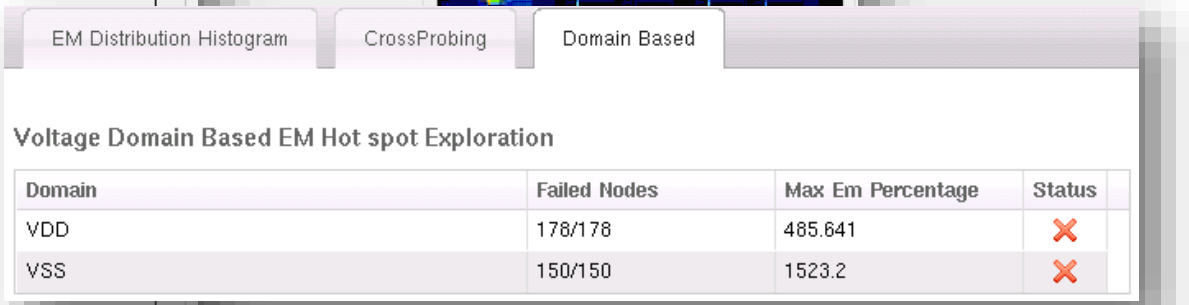
Equivalent Tcl Command:

perform min_res_path –o res_path.rpt

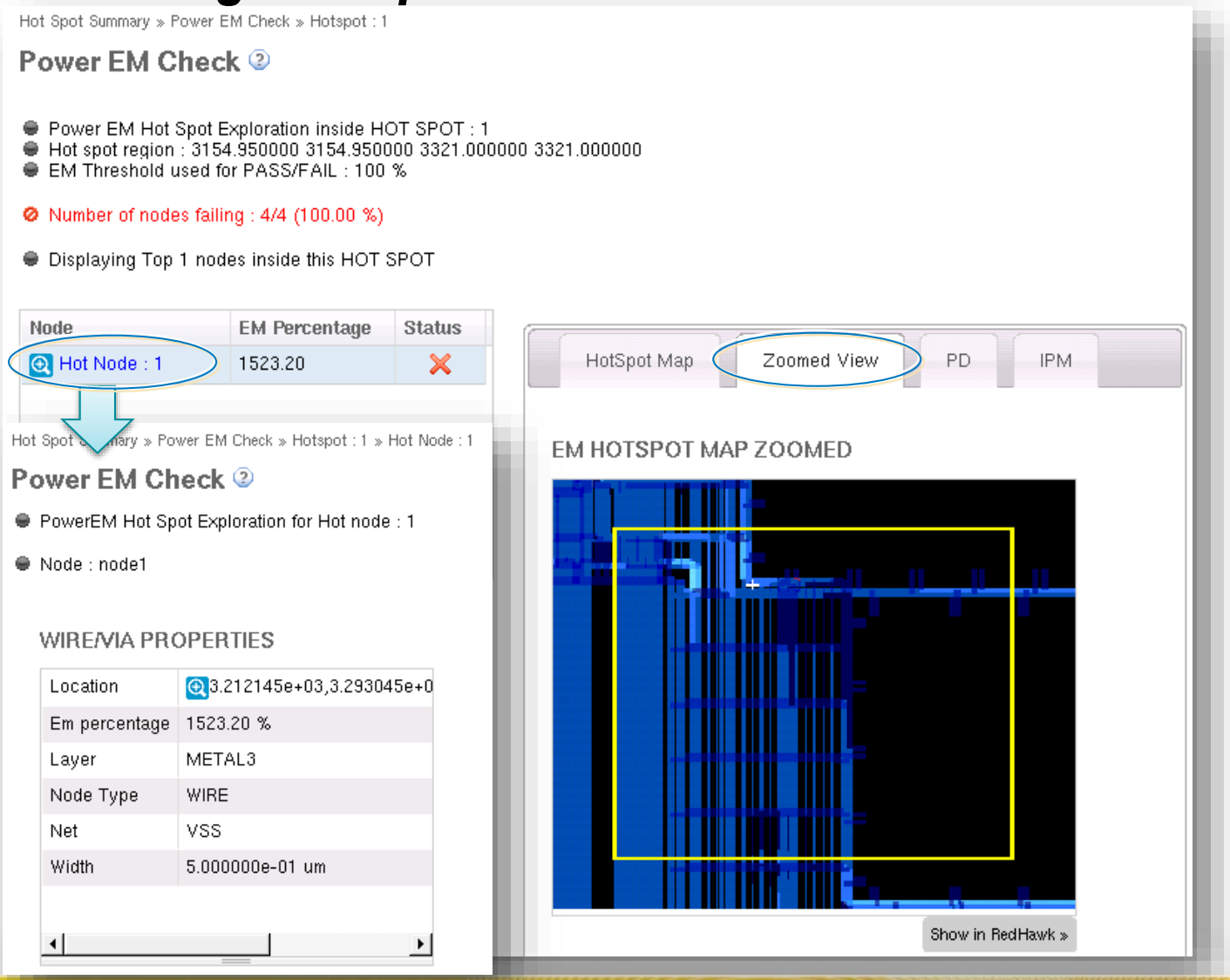
Power EM Check : Summary





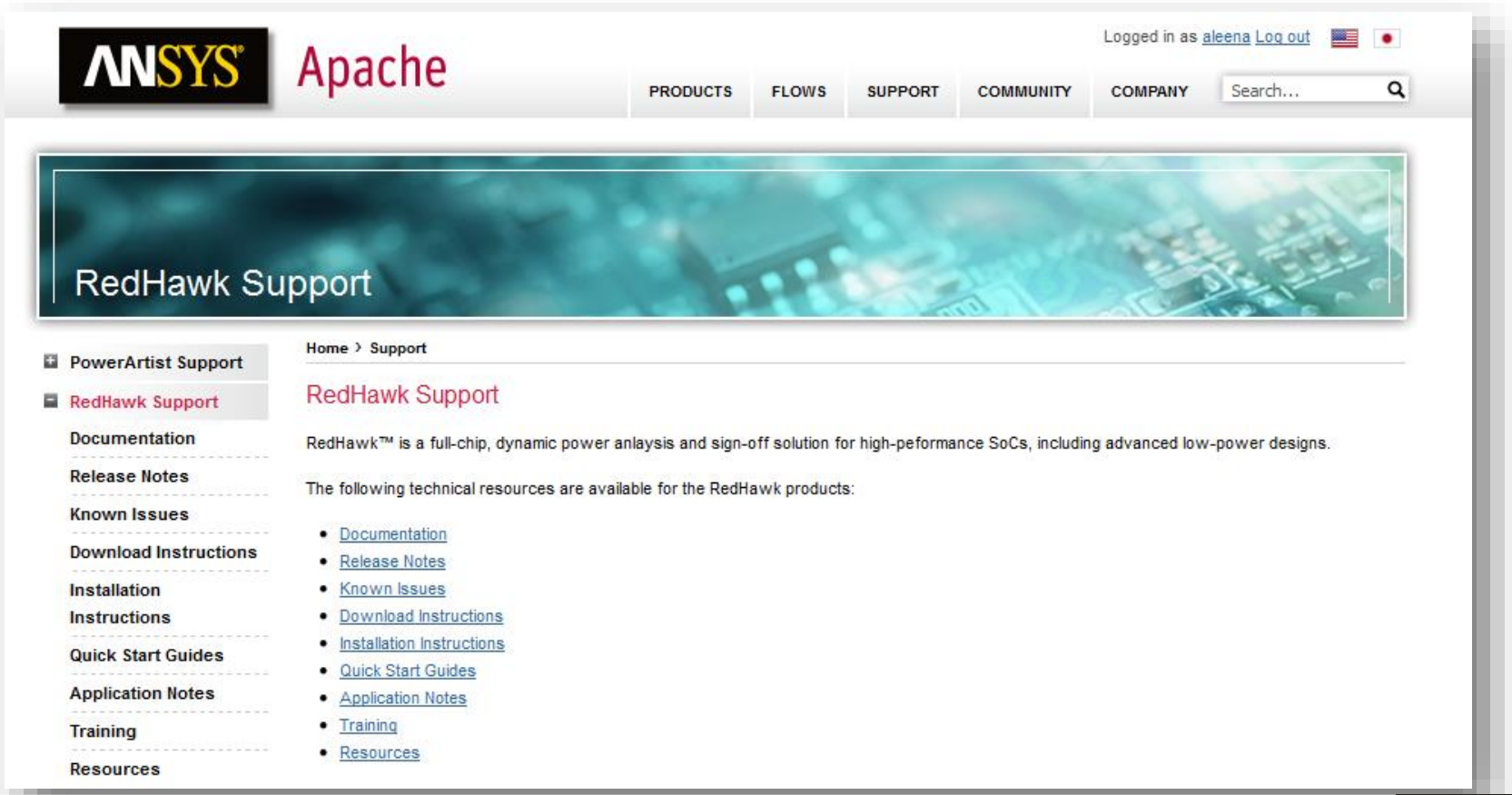


Power EM Check
Checking Hot-spot #1



How to get Help!!

- **Apache Online Customer Support Center**
  - http://support.apache-da.com
  - **Email:** support@apache-da.com



Thank You!!!