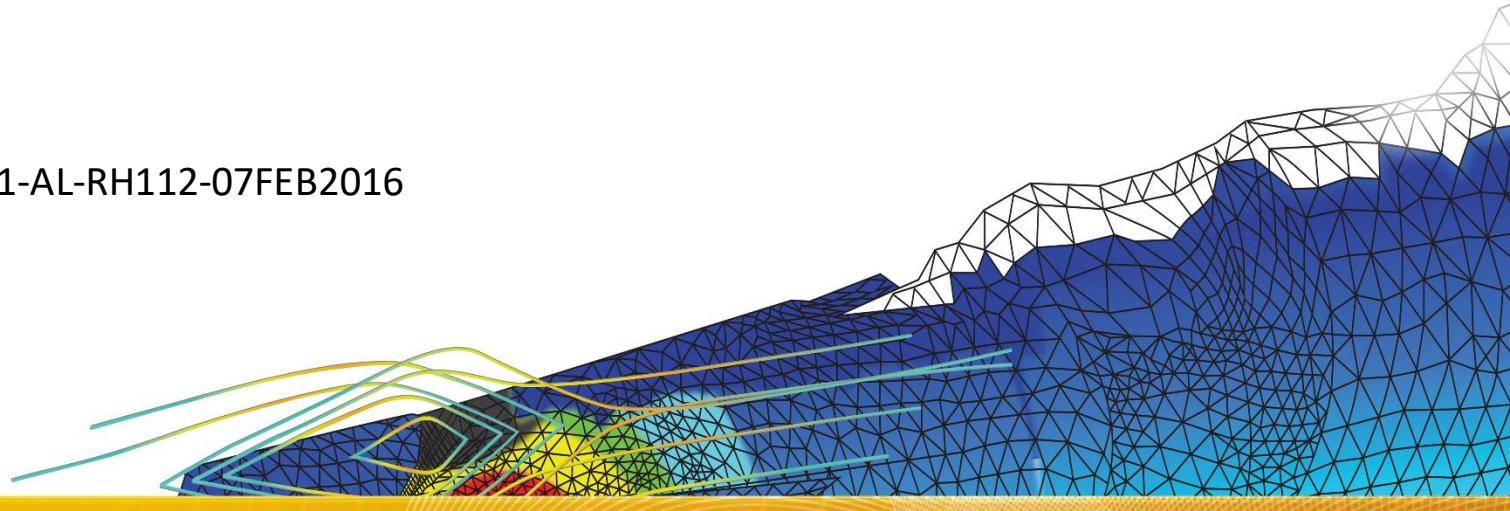


Realize Your Product Promise®



RedHawk™ Dynamic Analysis

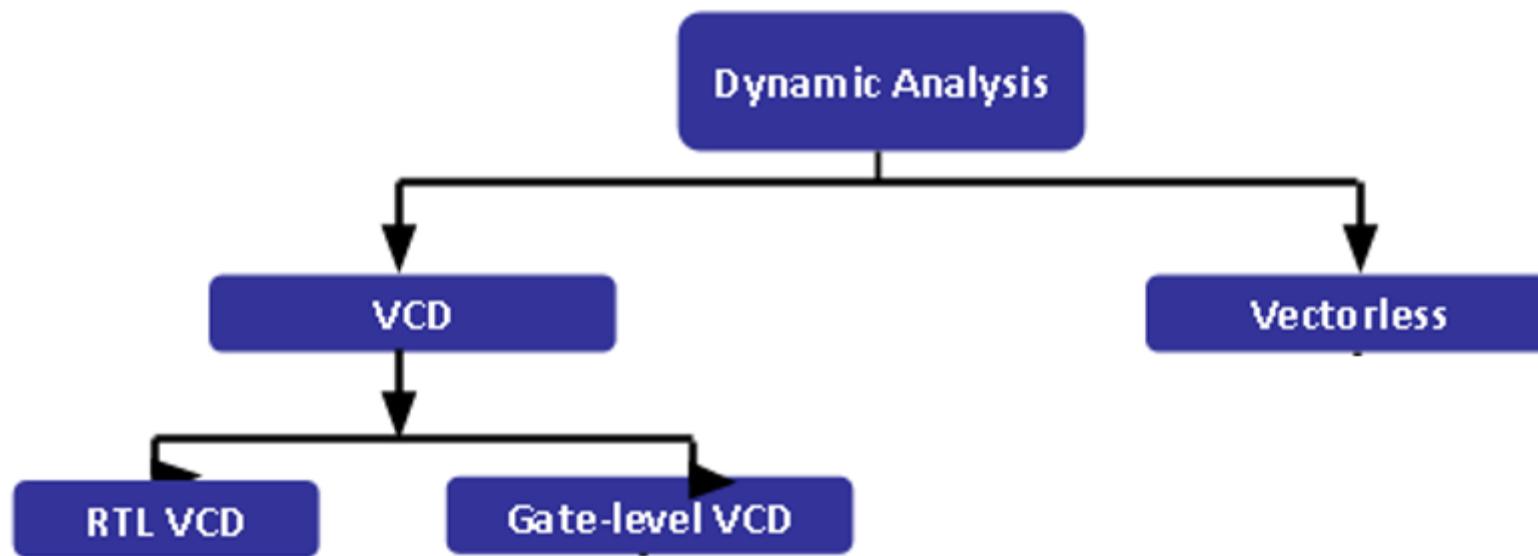
VERSION: V5.1-AL-RH112-07FEB2016



Agenda

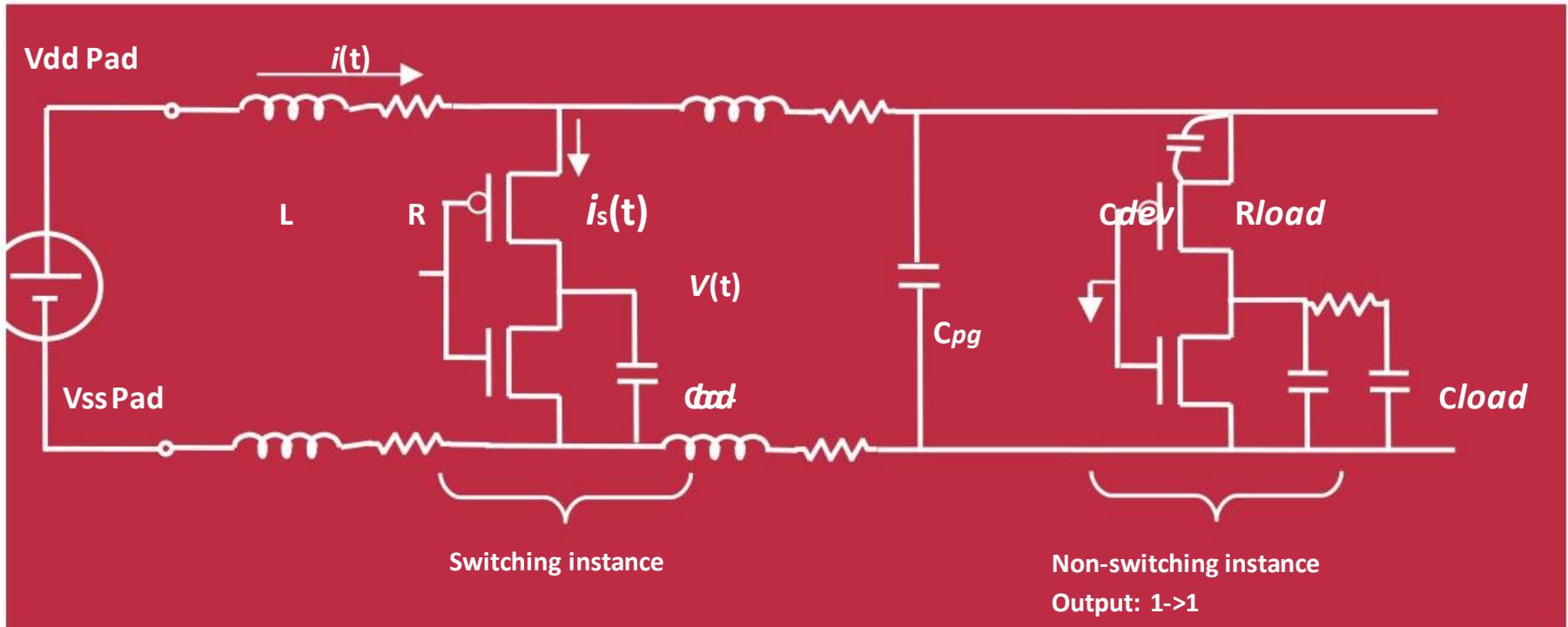
- Theory
- RedHawk Dynamic flow
- APL Introduction
- Analysis of results
- Conclusions

Dynamic Analysis-VCD and Vectorless



Dynamic Voltage Drop Modeling

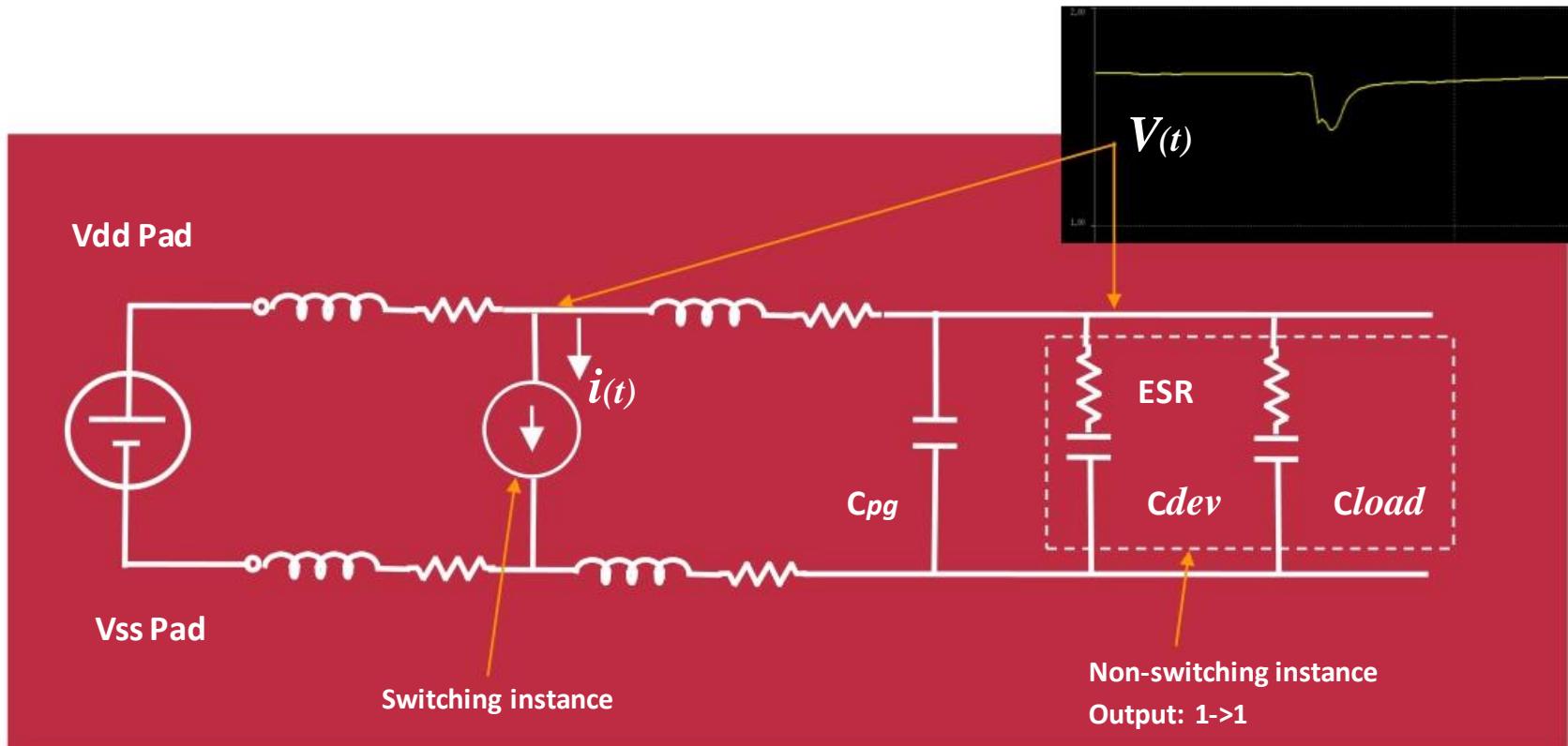
On-chip power/ground network



- On-chip power/ground network → R,L,Cmesh
- Switching instances → PWL current sources
- Non-switching instances → equivalent decaps

Dynamic Voltage Drop Modeling (Cont'd)

- PWL current for each instance (APL Current)
- Equivalent decaps (APL Cap)
- $V_{dynamic}$ waveform is computed at every node by transient simulation



Dynamic Analysis Which, When, and What

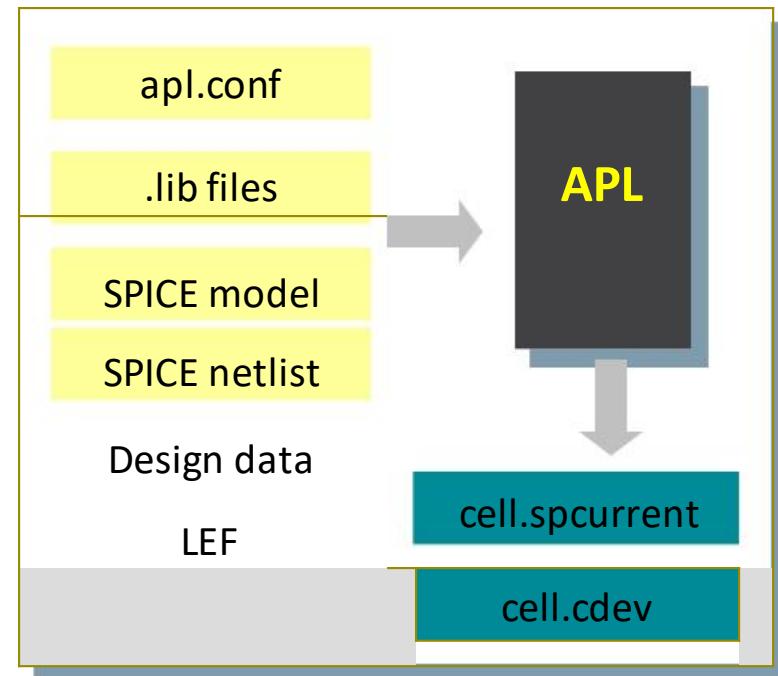
- **Logic: will an instance switch?**
 - VCD mode: switching pattern is provided by user
 - Vectorless mode: Constraint-based statistical switching(toggle rate)
- **Timing: if it switches, when will it switch?**
 - STA-based timing window, slew
- **Power: if it switches, what is its current profile?**
 - Spice-based library characterization (APL)

VCD-based Analysis

- **GATE VCD**
 - User specified switching interval (frame) simulated
 - RH vcdscan utility analyzes VCD and reports intervals with highest power
- **RTL VCD**
 - Uses toggle activity from VCD (entire or frame specific) to guide switching scenario creation
- **Supports RTL VCD and state propagation**

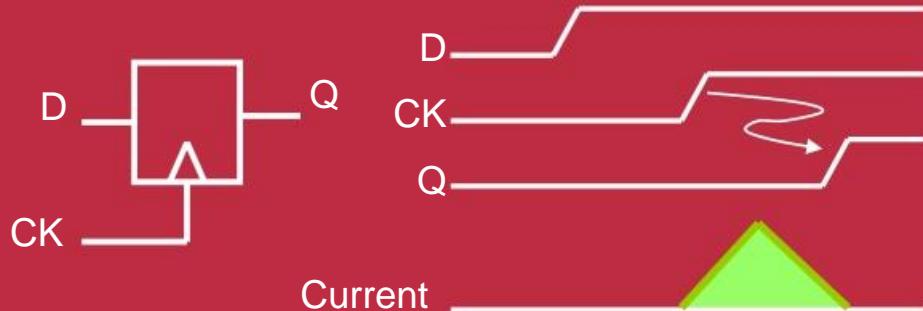
Apache Power Library

- Provides switching current, leakage current, intrinsic decap and leakage information
- For power gated designs provides switch model and PWL capacitance data
- w/o APL, .LIB is used to approximate $I(t)$
- Inputs for APL Characterization
 - Device model (Hspice/ELDO/Spectre format)
 - Spice Netlist (Hspice/ELDO/Spectre format)
 - .lib information
 - .lef information (optional)
 - Design data (optional)

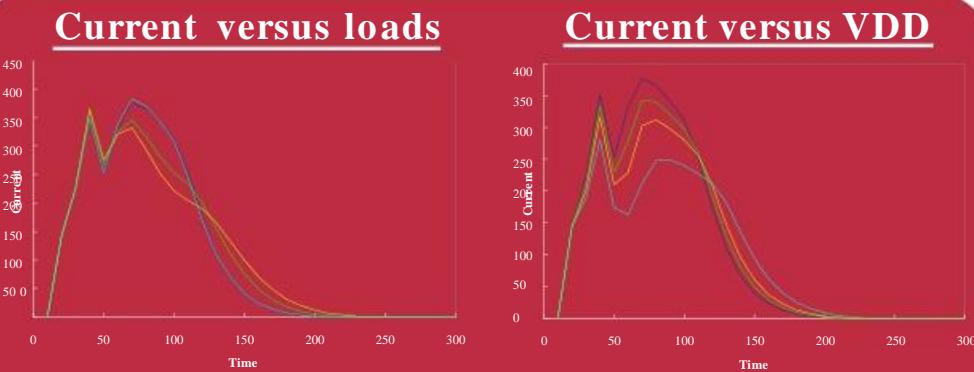


LB vs APL

.Lib: Triangular energy waveforms



APL: Multi-dimensional current profiles



APL model for a cell

- Cell level abstraction with transistor level characterization
- For standard cells, memories and macros

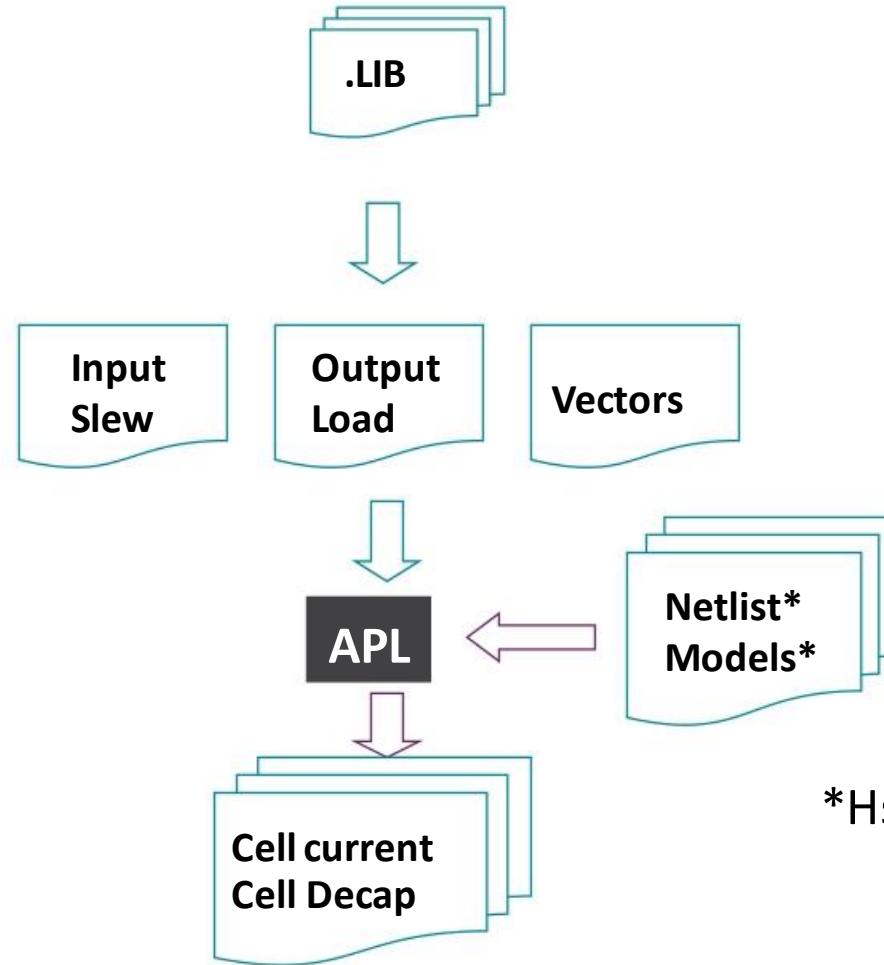
Contains:

Switching current
Leakage $\sim f(\text{state, temperature})$
Intrinsic capacitance
Effective series resistance
Cell delays and slews
...

APL (*Cont'd*)

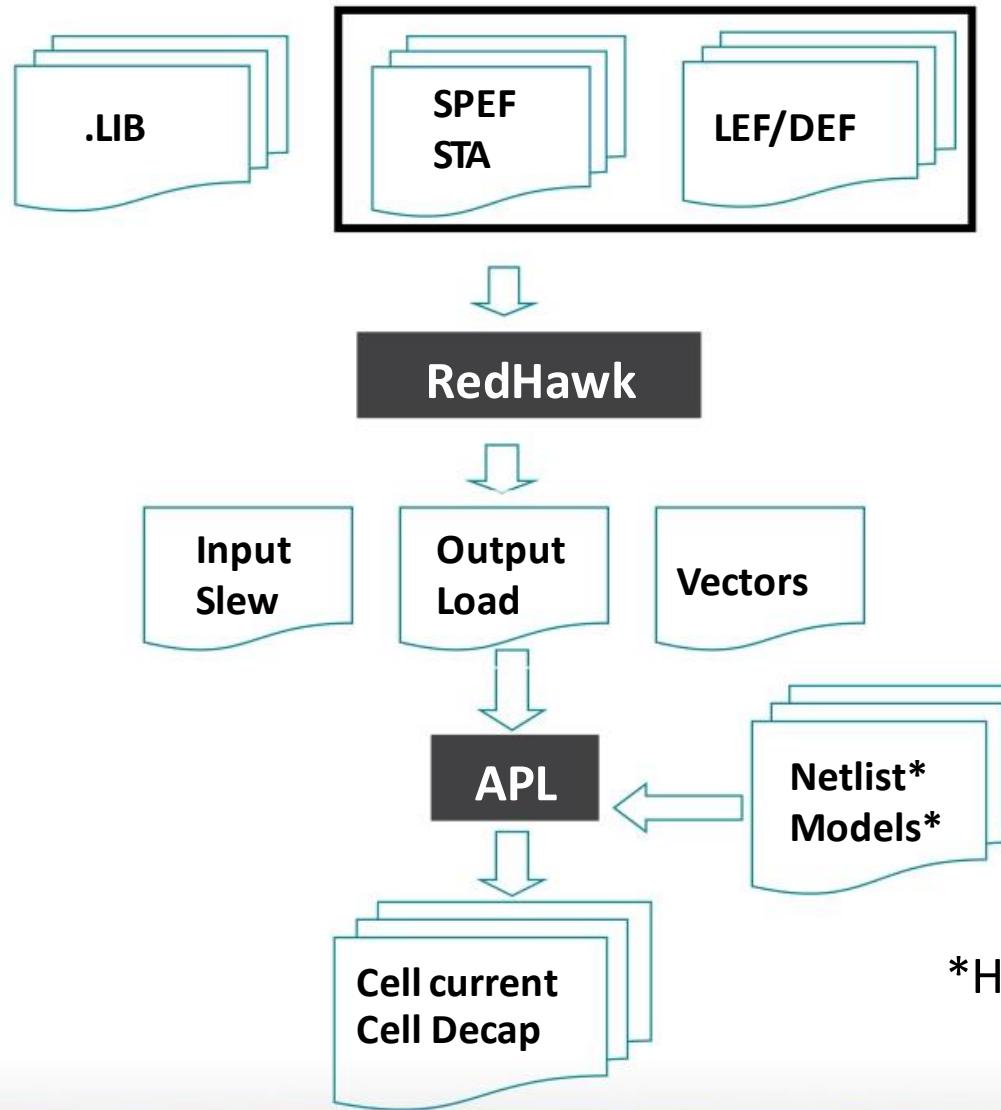
- **Advantages of APL**
 - Adaptively changes the current drawn based on cell's voltage during the simulation
 - Voltage drop at different parts of chip can vary significantly from ideal during operation
 - If current profiles are constructed based on ideal VDD and/or GND
 - ❖ Over-estimate of current profiles so pessimistic drop
 - ❖ Inaccurate modeling of switching current [cells consume same current irrespective of drop, placement, package, etc]
 - ❖ Like doing timing analysis assuming ideal slew at every cell pin – and not considering degraded slew in the paths

APL-DI(Design-Independent) Flow Overview



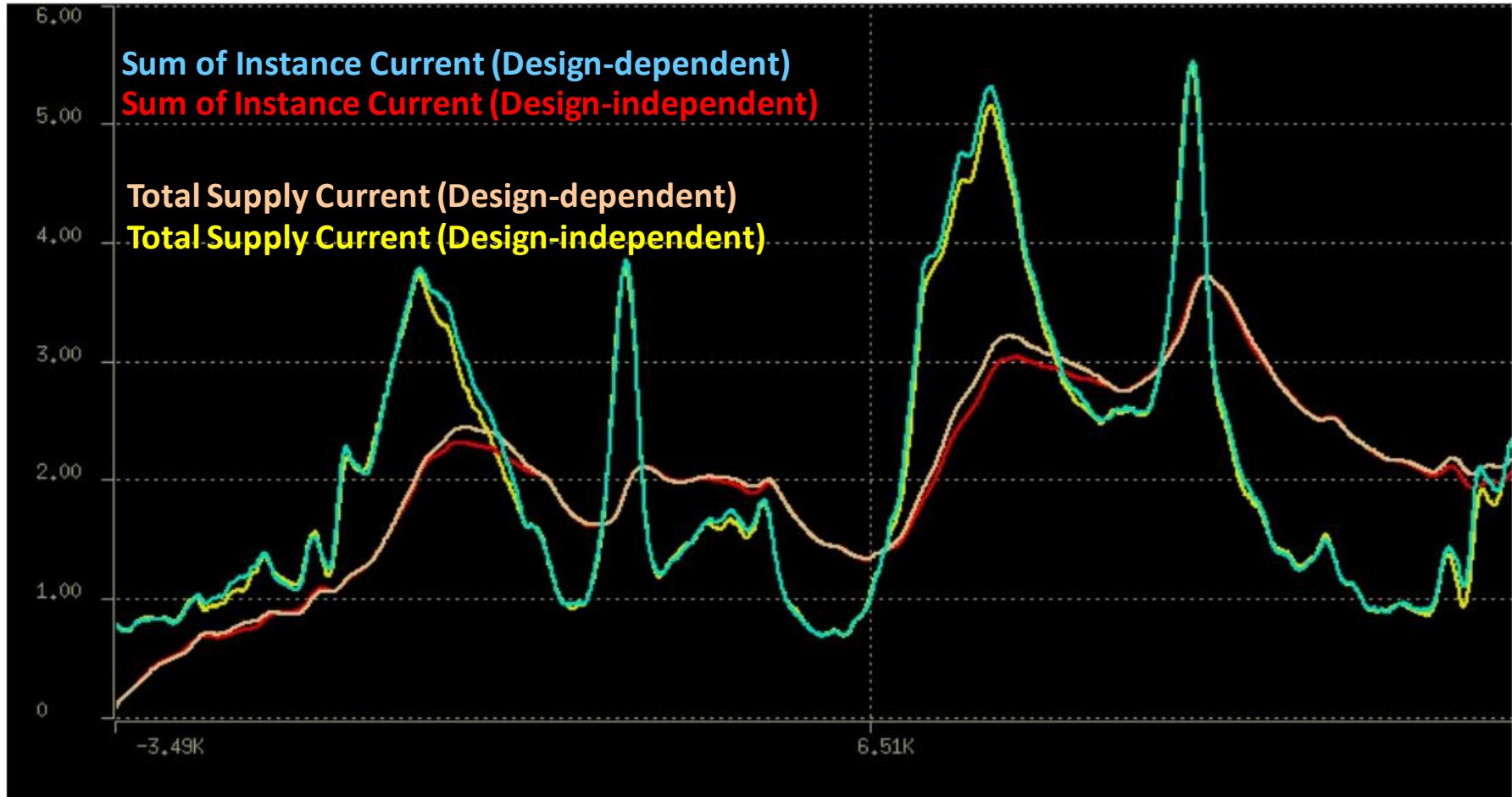
*Hspice compatible

APL-DD(Design-Dependent) Flow Overview



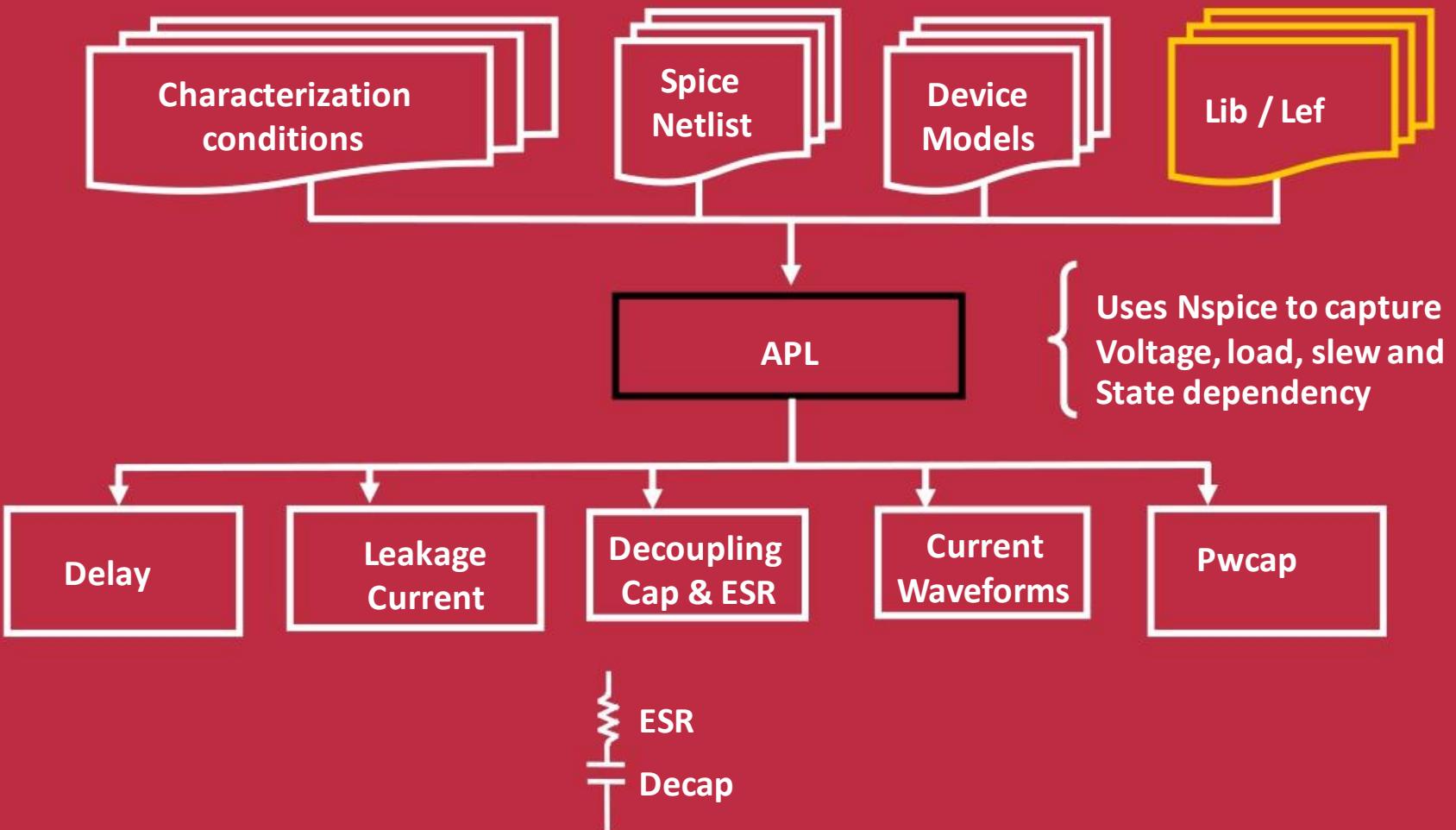
*Hspice compatible

Dynamic Analysis with APL

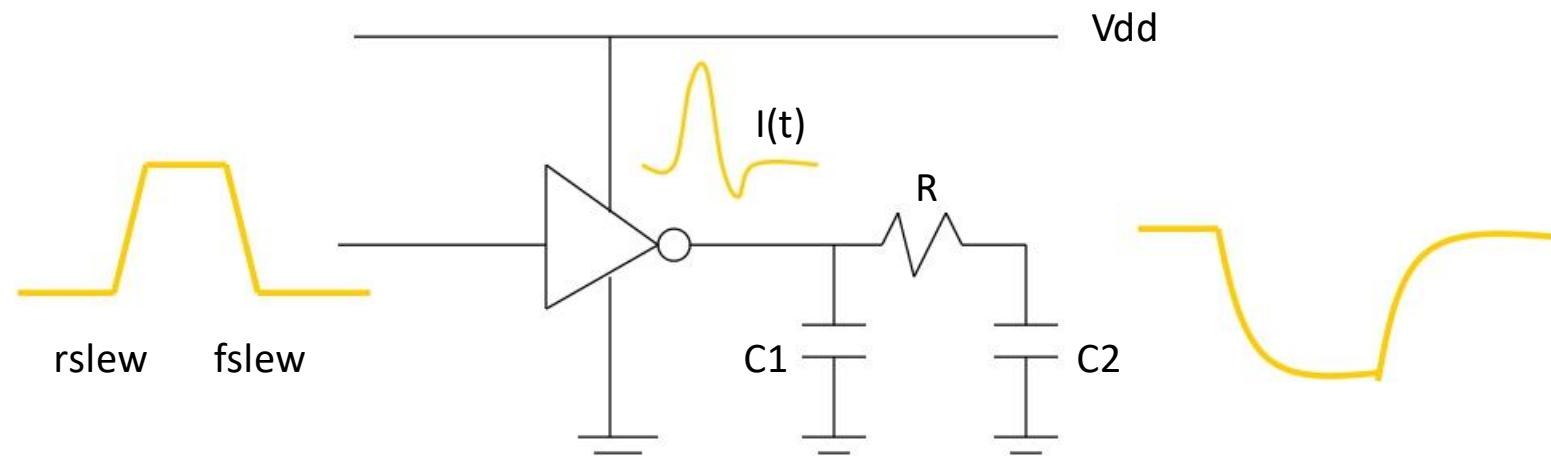


APL Basics and Std cell characterization

APL Data Requirements

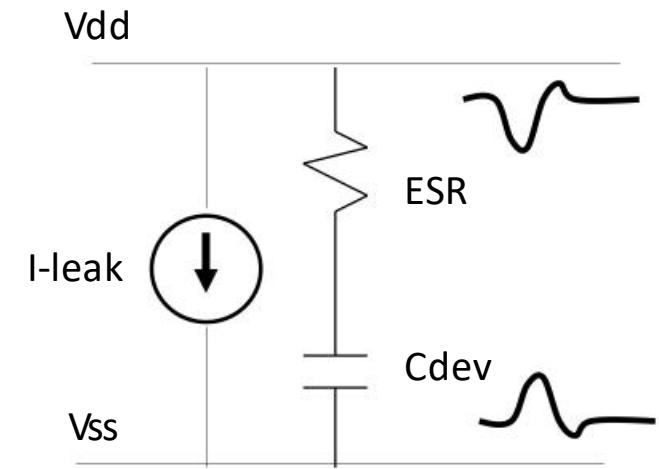
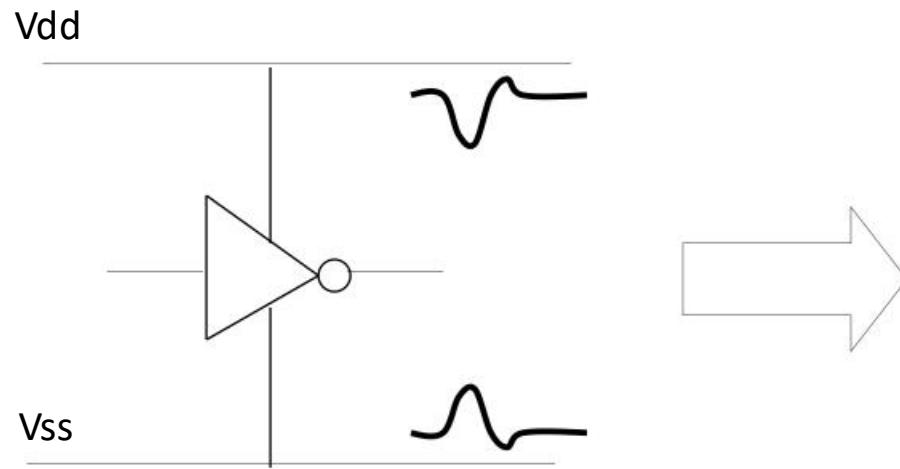


APL I(t) Characterization



- Capture the $I(t)$ for varying slews, cload and different voltages

APL Cdev Characterization



APL Design Independent

- Characterizes all cells found in .lib
- Range of slews/loads are derived from .lib lookup tables
 - Slews normalized from .lib threshold to full swing
 - Default: Average of 70 combinations of slew and load and 4 voltages
- Required inputs:
 - Synopsys .lib
 - Spice sub-circuits
 - Device models
 - Configuration file
 - LEF/custom lib files for multi-rail cell (P/G pin)
 - PG-ARC custom lib for Cdev characterization on multi-vdd(mvdd)/
multi-vss(mvss) cells

Basic APLDI Configuration File

```
APL_RUN_MODE DI
WORKING_DIR .

VDD_PIN_NAME VDD
GND_PIN_NAME VSS
APL_RESULT_DIRECTORY my_result

DESIGN_CORNER {
    TT {
        PROCESS TT
        TEMP 25
        VDD 1.6
    }
}
LIB_FILES {
    lib_dir
    stdcell_tt_1.6v.lib
}

SPICE_NETLIST foundry.cir
#SPICE_NETLIST_DIRECTORY
netlist_dir

# Option 1
INC spicel.models

# Option 2 - multiple .LIB
DEVICE_MODEL_LIBRARY c10131v.1 TT
```

Subckt P/G pin names to probe

Operating conditions – forms signature
of generated APL file

Synopsys .lib

Spice sub-circuits

Device models

APL Command File Checklist

- VDD value consistent with GSR and .LIB?
- Temperature consistent with .LIB, tech file?
- Name of Power/Ground nodes in Spice netlist may not be same as design
- Sizes in Spice netlist in um?
- Best to use extracted Spice netlist with RC parasitics
- PROCESS keyword defined correctly

APL Voltages

- APL configuration file keyword ‘APL_VOLTAGES’ specifies voltage values as a fraction of LIB nominal voltage, which are used for creating the current profiles. Voltage fractions should be specified in ascending or descending order.

Eg. Nominal Voltage of 1.5V

‘APL_VOLTAGES 6 0.7 0.8 0.9 1.0 1.1 1.2’

Will create current profiles for:

1.05V, 1.2V, 1.35V, 1.5V, 1.65V, 1.8V

- Default: APL_VOLTAGES 4 0.75 0.9 1.0 1.15

APLDI command line mode

apldi <config_file>

Options

- l <file> - characterize only listed cells
 - c - decap characterization
 - p <file> - intentional decap cells
 - j 1|2 - parallel execution
 - j = 1 use LSF bsub to submit job,
 - j = 2 uses LSF api to submit jobs
 - o - output current or decap file
 - s 1|2 - 1: generate apache.apldi, 2: skip sample generation
 - w - Piecewise cap characterization for Low Power
-
- **Intentional decap cells must be explicitly listed because they are not found in .lib**

Parallel Execution

- Setup LSF or Sungrid environment

`source /<lsf_setup_path>/cshrc.lsf`

`source /<lsf_setup_path>/settings.csh`

- Login to one of machines in LSF/Sungrid cluster

- In APL config file specify

`GRID_TYPE LSF`

`BATCH_QUEUING_COMMAND bsub`

- Monitor execution with

`aplstat <config_file>`

Running APL over LSF/SunGrid

- **APL config file options:**

LSF_JOB_COUNT	40
BATCH_QUEUING_OPTIONS	[-q <queue_name>] [-R <resource_name>] [-m <machine_name>] [-o /dev/null]
BATCH_QUEUING_COMMAND	bsub (default) qsub
LSF_SUBMIT_MODE	1 (default, bsub) 2 (LSF API)
GRID_TYPE	LSF (default) SUN_GRID

- **Batch-mode command:**

aplди -s 2 -j 2 apl.conf # for current characterization

aplди -s 2 -j 2 -c apl.conf # for cap/ESR/leakage characterization
(-j 1|2 will overwrite LSF_SUBMIT_MODE)

Finding APL Results

- **Summary log file**
 - adsRpt/apl.current.log
 - adsRpt/apl.cap.log
- **Warn/error log will also be present in adsRpt dir**
- **Current profiles of all characterized cells in one file. Default - corner<name>.current**
- **For each cell (depending on setting of APL_RESULT_DIRECTORY)**
 - In <APL_RESULT_DIRECTORY>/corner1/CURRENT/
 <cell>.current.<time>.log
 cell.spiprof - current profile
 - In <APL_RESULT_DIRECTORY>/corner1/CAP/
 <cell>.cap.<time>.log
 cell.cdev - device capacitance

APL Log File

- Log messages
 - Summary report *adsRpt/apl.{current,cap,pwlcap}.log*

```
Nominal VDD used: 1.8
Temperature used: 25
Netlist used: ../../spice/scc8q3rgenb.sp
Voltage range: 2.07 1.8 1.62 1.35
#                                     |----- slews -----|
stat #smpl #smpl_done c_min c_max rs_min rs_max fs_min fs_max vec cell_name
pass 70          70  1.00 278.80 0.012 2.500 0.012 2.500 LIB bufx1
...
...
```

- Detailed log files – all warning/error messages for each cell are logged to:
<APL_RESULT_DIRECTORY>/<corner>/CURRENT/<cell name>.{current,cap}.log

APLDI Characterization Modes

- APL sample mode controls number of samples.

APL_SAMPLE_MODE [FAST_CHECK | DEFAULT]

- **FAST_CHECK** : 1 Voltage ; 1 load-slew sample
- **DEFAULT** : 4 Voltage ; Adaptive load-slew samples (avg 70)
- Automatic slew normalization
All slews in RedHawk/APL normalized to 0-100% threshold
based on .lib thresholds

Recommended Procedure For Characterization of New Library

Step 1 - Run fast check mode

- Add to config file:
[APL_SAMPLE_MODE_FAST_CHECK](#)
One sample per cell – no need for LSF
- Run [apldi <config_file>](#)
- Check that most cells pass in *adsRpt/apl.current.log*

Sample range:

```
stat #smpl #smpl_done c_min c_max rsw_min rsw_max fsw_min fsw_max vec
cell_name
pass 1 1 1.000 1.000 0.012 0.012 0.012 0.012 LIB bufX1
pass 1 1 1.000 1.000 0.012 0.012 0.012 0.012 LIB andX1
...
...
```

Recommended Procedure (*Cont'd*)

Step 2 - Verify that LSF works

- `aplди -j 2 <config_file>`
- Use `aplstat <config_file>` to monitor, check `aplstat.log` for failure reason

```
##### 2 Cells Succeeded #####
bufX1  pass
andX1  pass
```

```
Total number of cells:    2
Number of cells succeeded: 2
Number of cells failed:   0
Number of cells pending:  0
```

- Test validity of generated current profiles:

`aplchk [-v] <directory>`

or

`aplchk [-v] corner<name>.current`

Recommended Procedure (*Cont'd*)

Step 3 – run full blown APLDI

(Do Run Time/File Size estimation)

- Remove `APL_SAMPLE_MODE FAST_CHECK` from apl config. file
- Run `apldi -j 2 <config_file>`
- Check success rate in `adsRpt/apl.current.log`
- Sanitize peak current and pulse width with `aplreader <current_file>`

```
cell=andX1
vdd=1.8 v; C1=0; R=0; C2=1; Slew1=11.667; Slew2=11.667
peak=74.02 uA; area=0.01577 pc; width= 0.456 ns ↗ vdd rise
peak=61.95 uA; area=0.01478 pc; width= 0.456 ns ↗ gnd rise
peak=72.51 uA; area=0.00573 pc; width= 0.133 ns ↗ vdd fall
peak=71.36 uA; area=0.00654 pc; width= 0.152 ns ↗ gnd fall
```

Common Issues: Missing include/model file(s)

- **Symptom** – in log file
##error## Can not find include file: models.all. Simulation stopped
- **Reason** – Device model files source other files
apldi.conf:
INC ../../models/tt.cor
tt.cor:
.inc "models.all"
- **Solution** – link all model files to \$cwd

Common Issues: Missing vectors

- **Symptom**
##error## Can not find vector or scanvector for cell
'scc8q3rgenb_a2111o_0' in file './apache/adsLib.output'. Exit.
- **Reason**
Cell is missing in .lib or has no function or state table
- **Solution**
fix your lib file or construct custom input vector

Common Issues: Undefined device models

- **Symptom**

##error## Undefined device model 'nch_bogus' ... Simulation stopped.

- **Diagnosis**

Run just that cell in the FAST_CHECK mode

- **Reason**

There are transistor whose device models were not found in device model files

- **Solution**

Load **all necessary** model with INCLUDE or
DEVICE_MODEL_LIBRARY statement (e.g. tt, hv_tt, lv_tt, dio)

- **Workaround**

Replace 'nch_bogus' with defined device model name. But check with the designer first (likely input data error!)

Common Issues: Undefined MOS Models

- **Symptom**

##error## Undefined device model 'nch' ... Simulation stopped.
But ... such model does exist in device model file(?!)

- **Reason**

Transistor width/lengths is outside bounds. Ex:
Mabc ... nch l=0.15 w=0.000001

- **Workaround**

Verify transistor size in the netlist, check the scaling factor in
the netlist

Debug on LSF

- Check whether the bsub command format is correct
- Check whether the data is accessible from the job running machine (read/write permission)
- Check available disk space

APL-DI Runtime Estimation

- Factors affect total run time for a library characterization

of cells

Char. Mode (# of samples)

Cell types (gates, dff/latches)

Computing resource (LSF farm)

$$\text{Total Run Time} = K * \text{mode} * \sum (\text{cell\#} * T_0) / \text{LSF_machine}$$

T0: one sample run time

Mode: char. Mode (sample#)

Fast check: Mode=1 Default: Mode=70

K: Overhead factor (network, job waiting, disk IO...) $1 < K < 10$

Example: 1000 std cell library, default mode, 10 LSF machines,
 $T_0=1\text{sec}$ (gate), $T_0=20\text{secs}$ (DFF)

Ideally, $K=1$, Total run time = $1 * 70 * (800*1 + 200*20) / 10 = 67.2\text{K secs} = 9.4\text{hrs}$

$K=2$, Total run time = $2 * 70 * (800*1 + 200*20) / 10 = 67.2\text{K secs} = 18.7\text{hrs}$

APL-DI File Size Estimation

- **Factors affect total file size for a library characterization**

of cells

Char. Mode (# of samples)

Cell types (gates, dff/latches)

$$\text{Total File Size} = K * \text{mode} * \sum (\text{cell\#} * S_0)$$

S0: one sample size (1 sample, 1 vdd, 70 current sample pts)

gate: (0.8K binary)

dff: (1.6K binary)

Mode: characterization Mode (sample#, vdd#)

Fast check: Mode=1 Default: Mode=70

K: Overhead factor (header, step, cellname, mP/G...) $1 < K < 5$

Example: 1000 std cell library, default mode (70 pts), S0=0.8K (gate), S0=1.6K(DFF)

$$\text{Total filesize} = 3 * 70 * (800 * 0.8 + 200 * 1.6) = 168 \text{MBytes}$$

Cell Functionality from .lib

- **Function definition in library (com. & simple seq. cells)**

```
function : "A&B&C";
```

- **State table definitions (complex seq. cells)**

```
statetable (" CLKIN EN TE","IQ") {  
    table : "L L L :- : L,\\"  
            "L L H :- : H,\\"  
            "L H L :- : H,\\"  
            "L H H :- : H,\\"  
            "H -- : - : N \";  
}
```

- **User provided vector (memory, user-defined full custom cell)**

Custom Vector File

- Complex Cells can be characterized using custom vector files
- Vectors can be written in an ASCII file. Filename could be <cell_name>.inv
- Vector files can be specified in a directory. This directory name can be specified in APL config file using VECTOR_DIR keyword
VECTOR_DIR ./vectors

Custom Vector File - example

<cell_name>.inv

```
dc pin_c vdd
dc pin_d 0
active_input a
active_output y
vector {
    vname a b
    tunit ps
    vih 1.1
    0 10
    1 01
    5 10
    7 01
}
```

Multi-VDD APL Characterization

- Multi Vdd APL characterization captures current/decap profile for different power pins separately (RH5v3)
- User Interface changes for mVdd APL char
 - APLDI : Need to define LEF_FILES keyword in config
 - For cells having multiple pgarcs, user need to provide PG arc information through Custom Libs file
 - Custom Lib file can be specified in the APL config file like this:

```
CUSTOM_LIBS_FILE { <custom_lib_file>
}
```

Multi-VDD APL Characterization

- Multi Vdd APL characterization captures current/decap profile for different power pins separately (available since RH5v3)
- User Interface changes for mVdd APL char
 - APLDI : Need to define LEF_FILES keyword in config. If LEF files are not available, need to specify power, ground pins through Custom Libs File
 - For cdev (decap) char of cells with multiple power, ground pins, user also needs to provide PG arc information through PGarc specific custom Lib file
 - For decap cells characterization, value for each VDD pin should be defined in config file

mVDD APL Characterization: Custom Lib File

- **Custom Lib file can be specified in the APL config file like this:**

```
CUSTOM_LIBS_FILE {  
    <custom_lib_file>  
}
```

- **Example Custom Lib File for specifying power/ground pins :**

```
cell LVL_IN_F12_PM {  
    pin VDDIN {  
        type vdd  
    }  
    pin VDD {  
        type vdd  
    }  
    pin VSS {  
        type gnd  
    }  
}
```

NOTE: LEF files overwrites custom lib files if both are given

mVDD/mVSS cdev char: PGarc specification

- Pgarc is required for cdev characterization of cells with multiple power, ground pins.
- It defines decap components between Power and Ground pins
- APL-DI mode: use PGarc specific custom lib file to define pgarc
 - Example in apldi.config:

```
LIB_FILES {  
    <lib_files>  
    pgarc.lib CUSTOM  
}
```

Where pgarc.lib contains:

```
pgarc {  
    <vdd_pin_name> <vss_pin_name>  
}
```
 - Run Command: apldi -l list -c apldi.config
- APL-DD mode: .apache/apache.pgarc is created by RedHawk.
 - APL will automatically search this file
 - Run command: apldi -s 2 -l list -c apl.config

mVDD/mVSS Decap cell char

- Decap cells (non-function cells) are not present in .lib
- Decap cells' PG Pin information is from PGarc custom lib file similar to cdev as explained in previous slide.
- Additionally value for each vdd pin should be defined in APL config file

```
DECAP_VDD_PIN {  
    vdd_name vdd_value  
    ...  
}
```

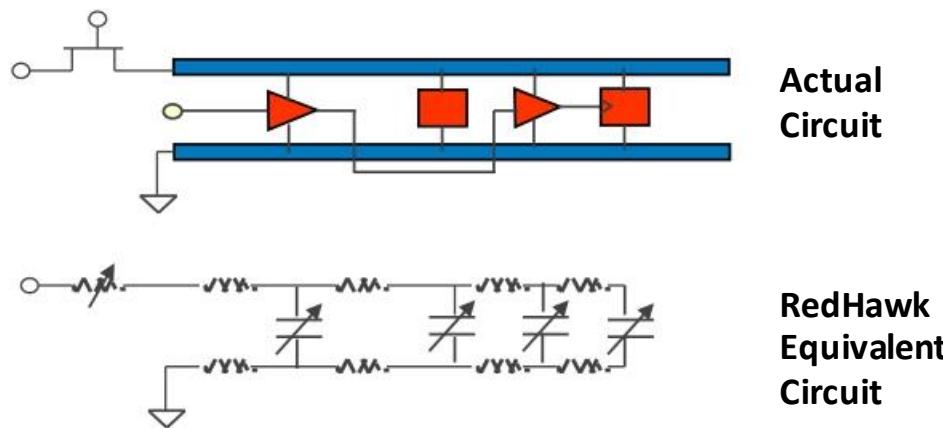
- If DECAP_VDD_PIN is not given, the vdd value specified by VDD keyword will be used for all vdd pins.

APL char for Power gated designs

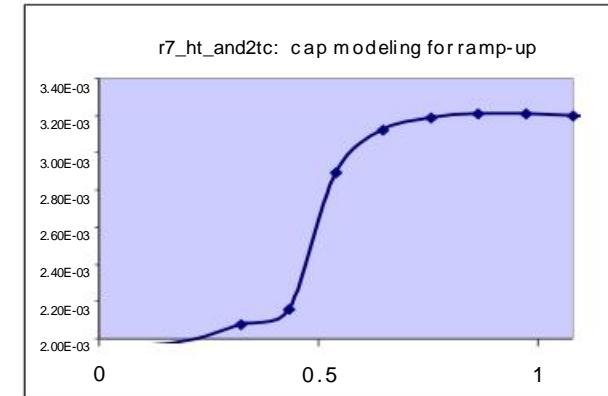
- **Switch cell characterization**
 - Need to characterize header/footer switches in low power designs.
 - Utility: aplsw <file containing list of switch cells & their configuration files>
 - Please refer RedHawk manual for details.
- **PWL cap characterization**
 - Need to characterize cells in the design to get the piecewise linear models for intrinsic capacitances, leakage currents, and effective series resistance, as a function of voltage.
 - APL utility “apldi –w <apl config file>
 - Please refer RedHawk manual for details.

APL Pwcap Data

- Power gates are non-linear elements in different modes
- Transition from “off” to “on” state requires charge transfer to/from design
- Design capacitance varies as function of node voltages
- Long simulation times to capture entire power-up process
- Required only for Powerup analysis; Not required for ON state analysis



Non-linear capacitor modeling



APL Utilities - aplreader

- **Function**
 - Read apl binary current profile (cell.spcurrent) and decap (cell.cdev) files and present user-readable summary report
- **Usage**
 - aplreader <cell.spcurrent> for current profile
 - aplreader -c <cell.cdev> for decap file
 - aplreader –pwc <cell.pwcap> for pwcap file
 - Use '-l <cell_list_file>' to print only the cells in the given file. Alternatively, use '-cells <name>' to specify cell name in the command line

APL Utilities - aplchk

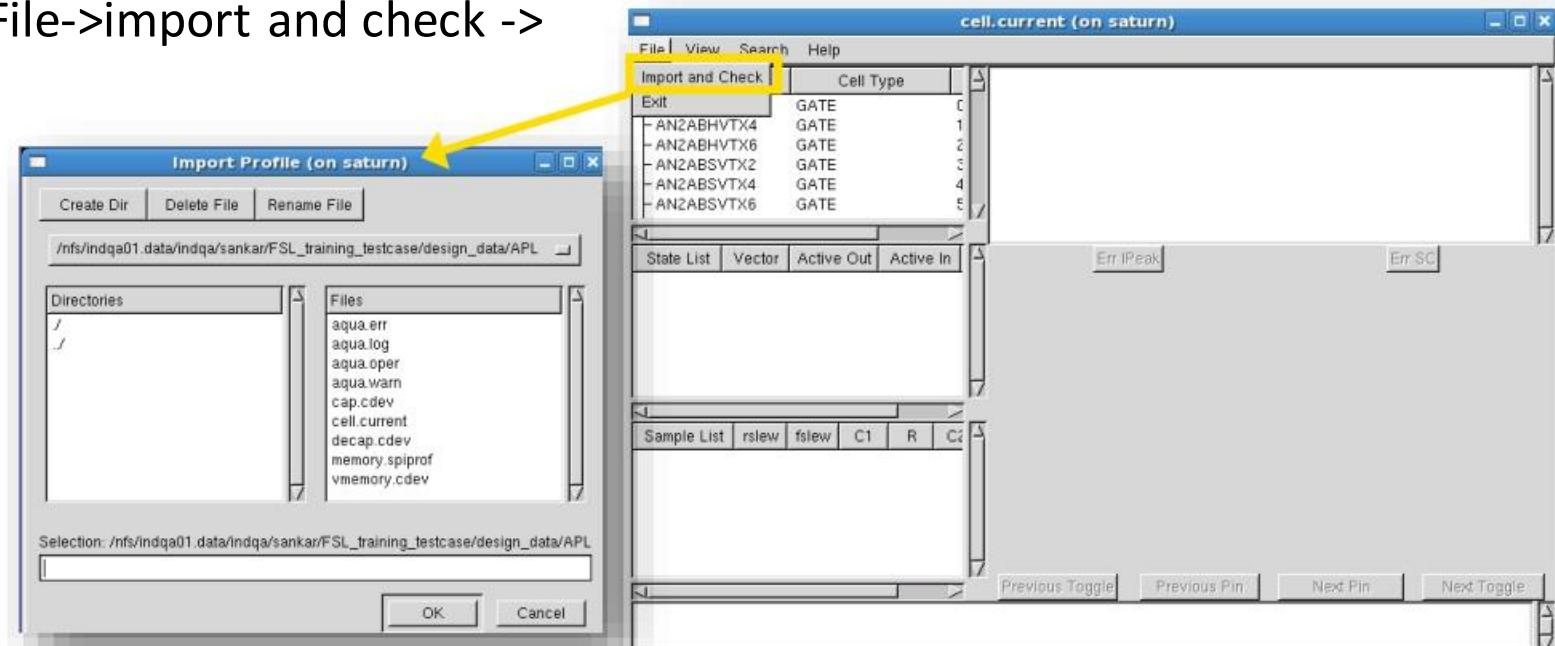
- **Check APL results data integrity**
- **aplchk [-c] [-pwc] [-ilimit] [-l <list_file>] [-w <output_file>] [-a2b <output_file>] <input_file>**
 - c : specifies checking cdev decap files
 - pwc : specifies checking pwcdev files
 - ilimit : ignore the error limit checks
 - l <list_file> : writes out result information on cells named in <list_file> to the specified <output_file>

APL Utilities - aplmerge

- Check the compatibility of corner conditions (P, V, T) for similar types of APL files and merge them into a single output file.
- `aplmerge [-c] [-pwc] [-ilimit] [-rep] [-im] [-t] [-ahead <cell_list> [-avm] [-l <cell_list>]] [-o <output_file>] [<file1> [<file2> [...]]]`
[directory]
 - c : specifies merging intrinsic decap files
 - pwc : specifies merging piecewise linear decap files
 - ilimit : ignore the error limit checks
 - rep : specifies replacing cells in the first file with cells with the same name in the second file. Cell information not duplicated in the second file remains the same in the output file.
 - im : ignore model library difference
 - t : specifies turbo mode, which runs faster by skipping duplicate cell checks

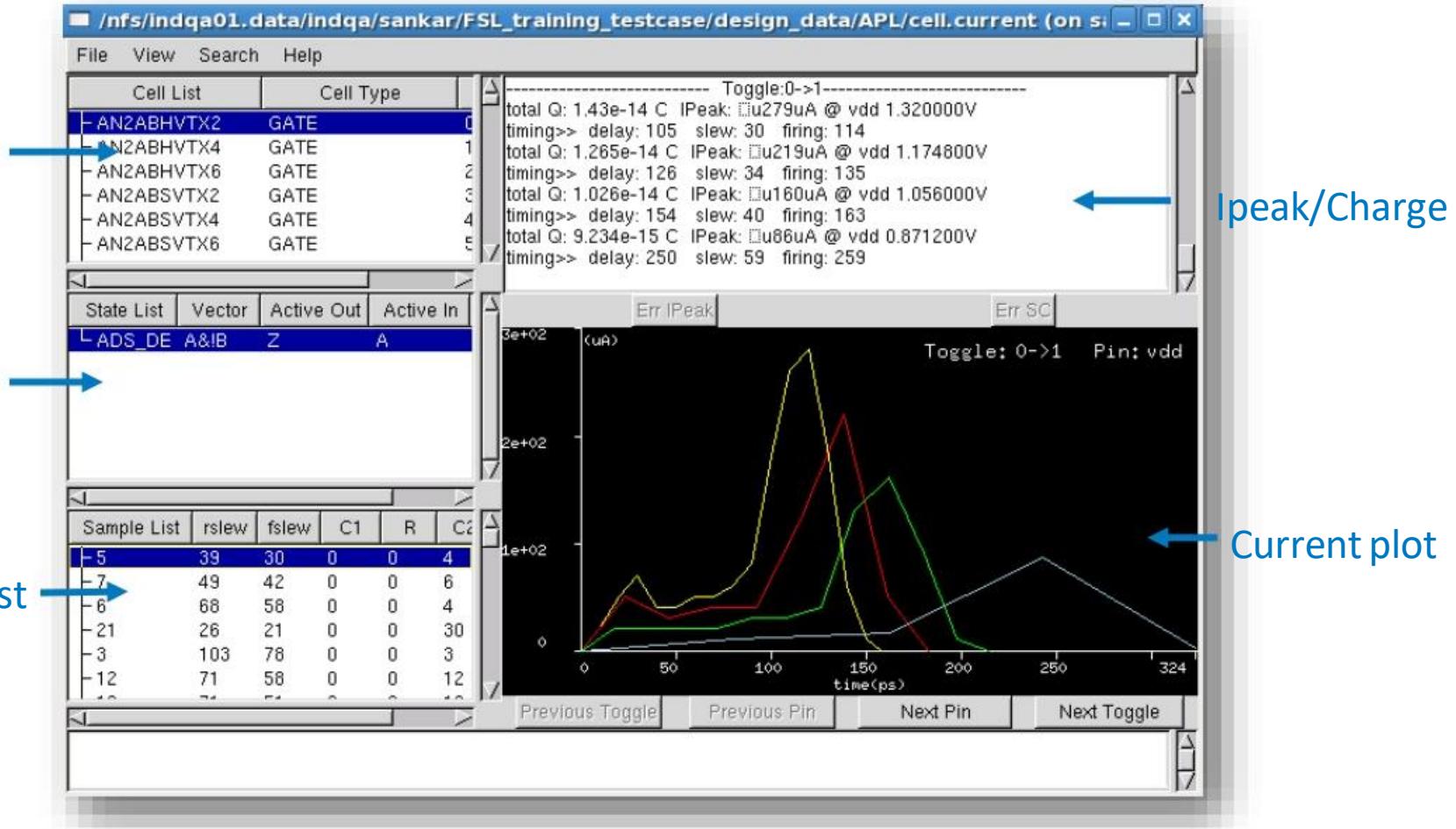
AQUA : APL Data Query Tool

- Utility to query/display APL/AVM current profiles
 - Input files: *.current ; *.spiprof
- Command : **\$APACHEROOT/bin/aqua**
- Import a file or directory
 - File->import and check ->



AQUA: Waveform Viewer

Cell List



Sample List

Importing Data into RedHawk

Importing APL Data into RedHawk

- APL files can be imported in GSR

```
APL_FILES {  
    <file> <type>  
    <dir> <type>  
}
```

Example:

```
APL_FILES {  
    cell.current current  
    cell.cap cap  
    cell.pwcap pwcap  
    avm.conf avm  
    ./APL_OUT/corner1/CURRENT/ current  
    ./APL_OUT/corner1/CAP/ cap  
}
```

NOTE: keyword

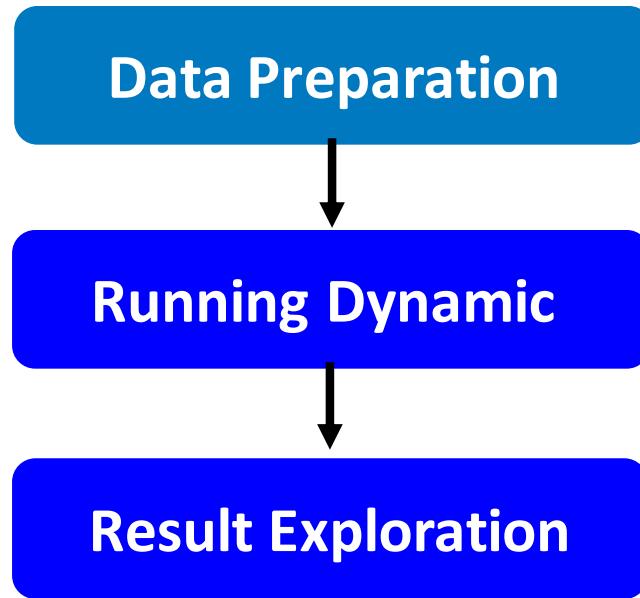
- Directories are assumed to have <cellname1.current>, <cellname1.current>, <cellname3.current>, etc...

Dynamic Analysis Using .LIB vs APL

- .lib profiles have a single peak only and cannot correctly capture multi-stage cell switching currents
- .lib profiles cannot capture the change of operating voltage for cells
- RedHawk using APL can adjust the switching current of cell based on its VDD and VSS voltage values

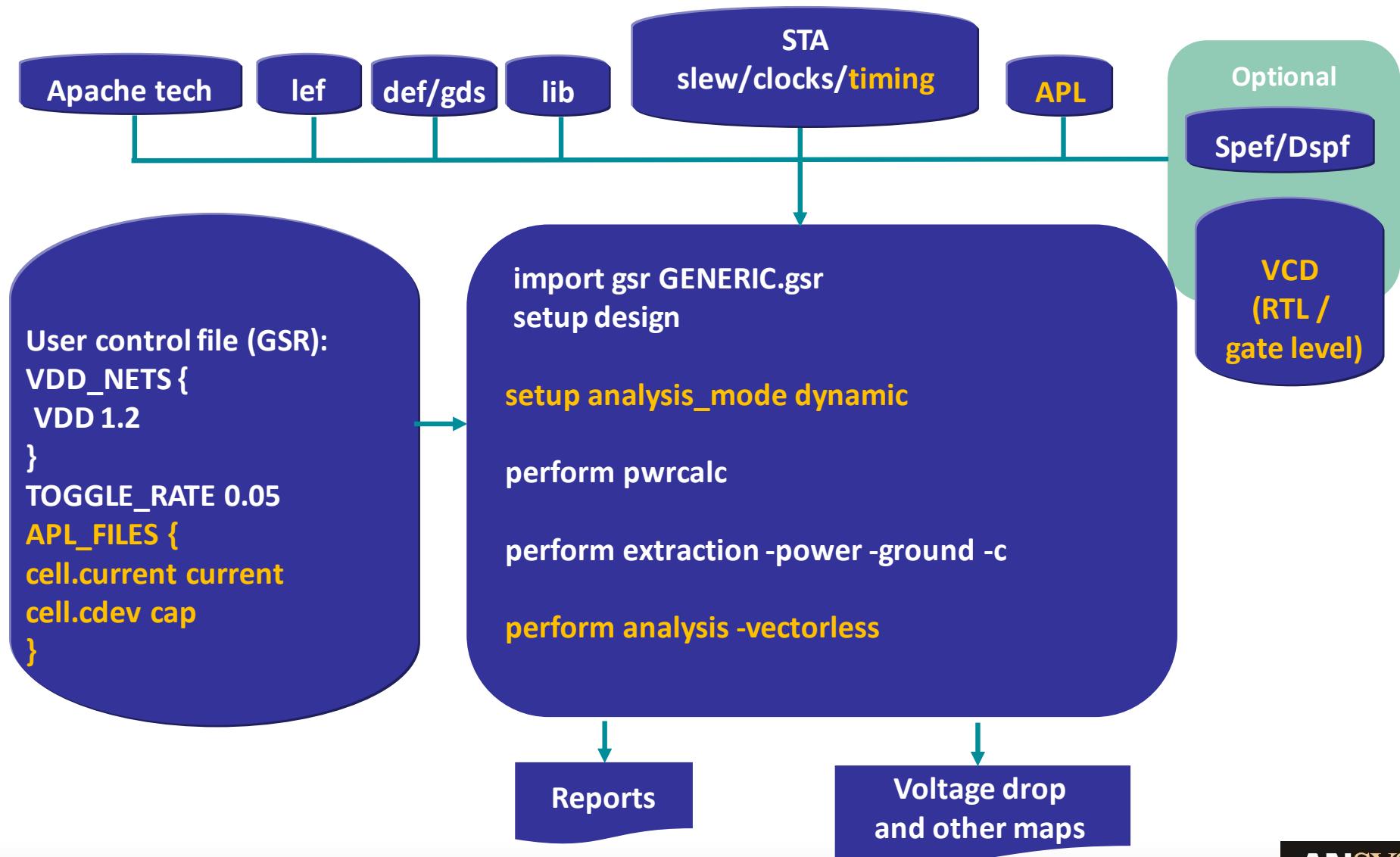
	APL based	.LIB based
Switching Current Profile	True spice current waveform	Triangular profile using .lib charge and delay
Intrinsic Decap and effective series resistance	True spice characterized value	None used
Leakage Current		.lib based value

Data Preparation for Dynamic



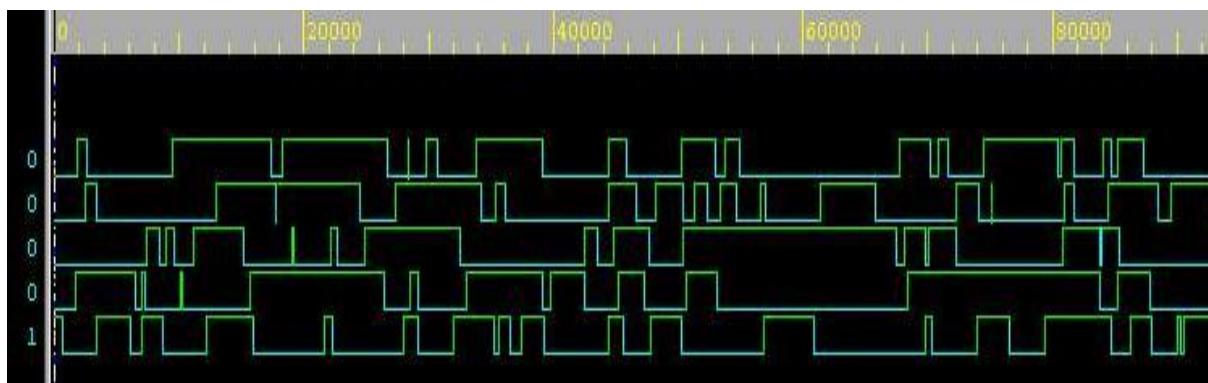
- Setup dynamic run
- Reviewing the additional GSR keywords and command file changes

Dynamic Analysis Flow



What is VCD ?

- **VCD or “Value change dump file”**
 - Contains the waveforms for different signal nets in the design
 - Created from 3rd party verification tools
 - Format is ASCII
 - Waveform can be viewed in 3rd party tools
- **Alternative format is FSDB (Fast signal Database)**
 - Format is binary
 - Much lesser file size compared to VCD
- **RedHawk supports both VCD and FSDB formats**



```
$version          APACHE      05.10.001-s
Tool:
$end

$timescale        1ps
$end

$scope module test_bench1 $end
$scope module GENERIC $end

$var wire    1 !!! net_63041 $end
$var wire    1 !!" net_18957 $end
$var wire    1 !!! net_15348 $end
$var wire    1 !!!$ net_18964 $end
$var wire    1 !!!% net_18963 $end
$var wire    1 !!!& net_18962 $end
$var wire    1 !!!' net_63034 $end
$var wire    1 !!!( net_99214 $end
$var wire    1 !!!) net_18958 $end
$var wire    1 !!!* net_18957 $end
$var wire    1 !!!+ net_18956 $end
$var wire    1 !!!, net_18955 $end
$var wire    1 !!!- net_18954 $end
$var wire    1 !!!. net_18953 $end
$var wire    1 )U\ net_16165 $end
$var wire    1 )U] net_16163 $end
$var wire    1 )U^ net_16161 $end
$var wire    1 )U_ net_16159 $end
$var wire    1 )U- net_16157 $end
$var wire    1 )Ua net_16155 $end
$var wire    1 )Ub net_16153 $end
$var wire    1 )Uc net_16151 $end
$var wire    1 )Ud net_16149 $end
$var wire    1 )Ue net_16147 $end
$var wire    1 )UF net_16145 $end
$var wire    1 )Ug net_16143 $end
$var wire    1 )Uh net_16054 $end
$upscope $end

$upscope $end
$enddefinitions $end

$dumpvars=0
0!!!"
1!!!#
1!!!%
0!!!%
0!!!-
1!!!+
1!!!(
1!!!)
1!!!*
1!!!+
0!!!-
0!!!-
1!!!-
```

Types of VCD

Gate Level VCD

- **Contains toggle information of all the gates in the design**
- **True time VCD**
 - SDF (Standard Delay Format) is used in verification
 - VCD generated from timing annotated functional/scan simulation
 - RedHawk will use switching scenario from VCD
 - RedHawk will use instance switching time from VCD
- **Non-true time VCD**
 - SDF not used in verification
 - VCD generated assuming unit-delay gate level functional/scan simulation
 - RedHawk will use switching scenario from VCD
 - RedHawk will use switching time from STA file
- **Do I need STA file for true-time based analysis ?**
 - Yes, you will still require this for slew information

Types of VCD (*Cont'd*)

RTL VCD

- Contains only activity at state points
- Registers/latches/memory/primary input
- RedHawk does logic propagation to derive the activity information for internal logic
- Mapping RTL VCD to gate netlist(DEF) name
 - RedHawk can use auto-name mapping and generate the mapping on its own
 - Mapping file can be generated from formal verification tools
- User control available for logic propagation through constraint file

- RTL VCD is useful during early stages of the design cycle
- Gate level simulation happens later in the design cycle
- RTL VCD file size will be much smaller compared to Gate level VCD
- RTL VCD is always non true time
- RedHawk will use switching scenario from VCD
- RedHawk will use switching time from STA file

VCD_FILE Specification in GSR

- **VCD_FILE Specification**

```
VCD_FILE
{
    <top_level name> <absolute or relative path to VCD or FSDB file>
    FILE_TYPE <VCD | FSDB | RTL_VCD | RTL_FSDB>
    FRONT_PATH <redundant path string that does not match the DEF path>
    SUBSTITUTE_PATH <the substitute path string from above>
    START_TIME <analysis start_time in ps; optional; default=0>
    TRUE_TIME [0|1]
    MAPPING <mapping_file_name>
}

DYNAMIC_SIMULATION_TIME <frame_width_sec>
```

- **Power Calculation will be done between:**
- **START_TIME and (START_TIME + DYNAMIC_SIMULATION_TIME)**

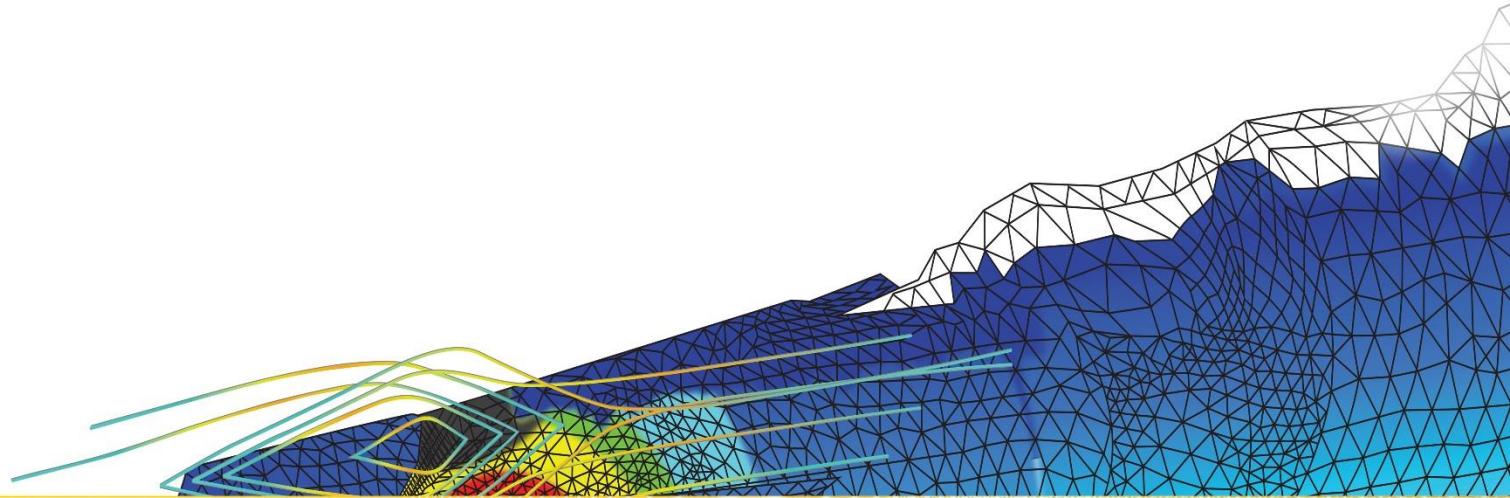
Hierarchical VCD_FILE Specification in GSR

- **BLOCK_VCD_FILE Specification**

```
BLOCK_VCD_FILE
{
    VCD_FILE {
        <hier_name(inst_name)> <absolute or relative path to VCD or FSDB file>
        FILE_TYPE <VCD | FSDB | RTL_VCD | RTL_FSDB>
        FRONT_PATH <redundant path string that does not match the DEF path>
        SUBSTITUTE_PATH <the substitute path string from above>
        START_TIME <analysis start_time in ps; optional; default=0>
        TRUE_TIME [0|1]
        MAPPING <mapping_file_name>
    }
    VCD_FILE {
        <hier_name2(inst_name2)> <absolute or relative path to VCD/FSDB file>
        FILE_TYPE <VCD | FSDB | RTL_VCD | RTL_FSDB>
        .....
    }
}
```

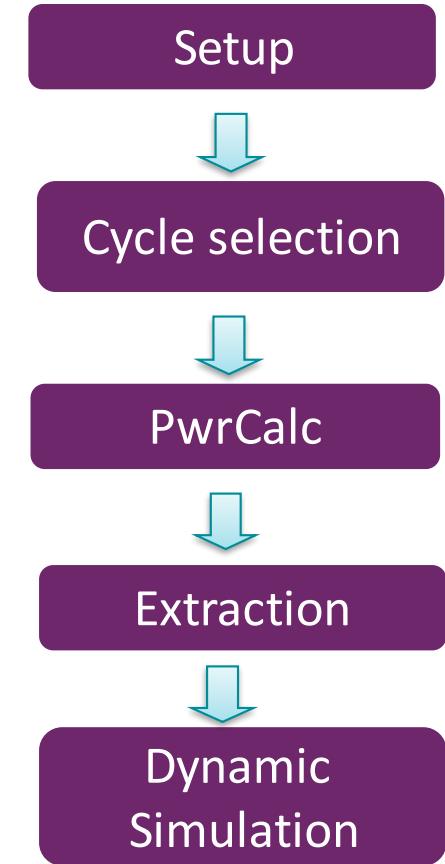


Cycle Select in VCD Based Dynamic Analysis

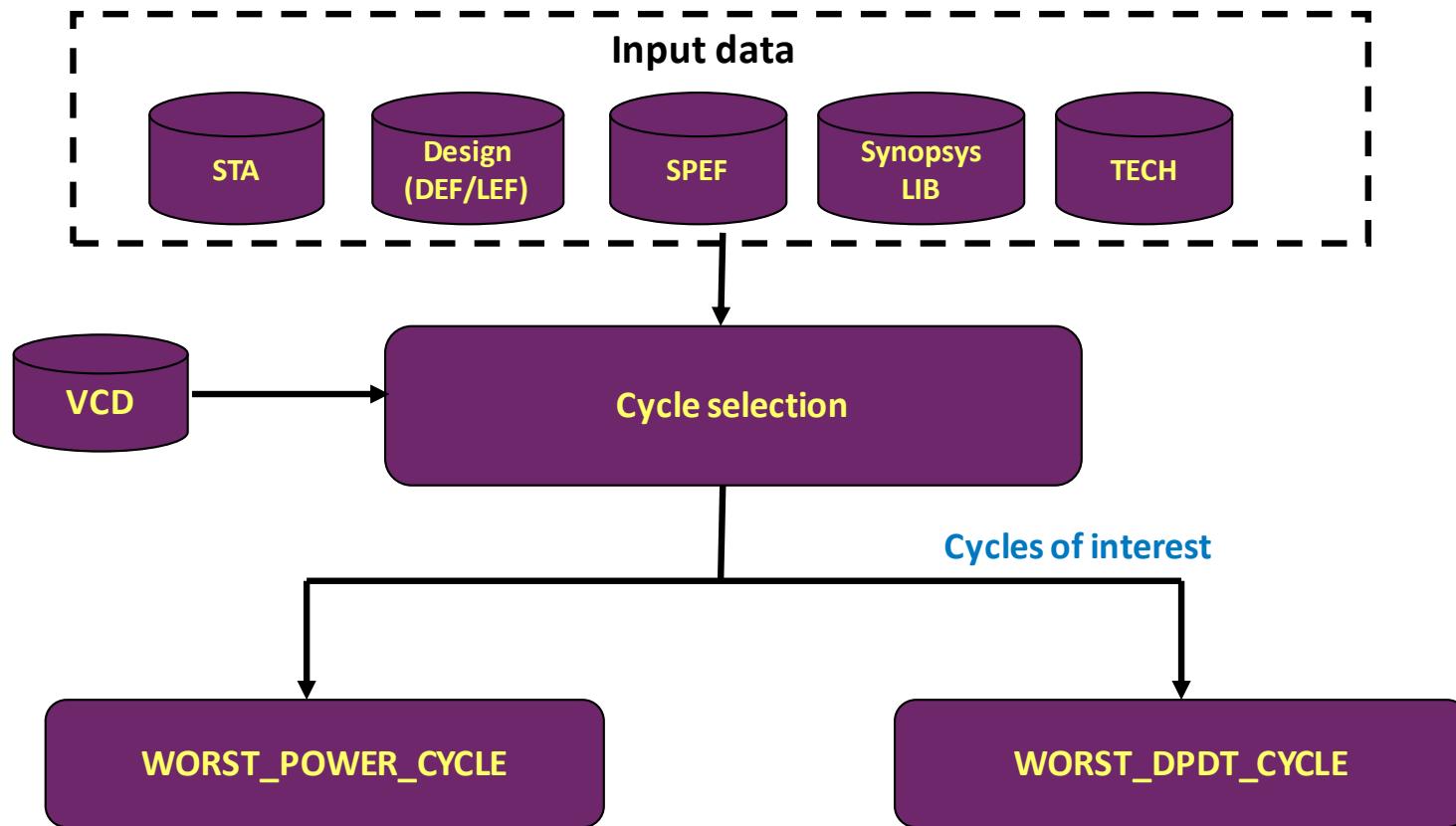


Cycle Select In VCD Based Dynamic Analysis

- **Challenges in VCD dynamic simulation**
 - Dynamic analysis is true transient simulation, not average analysis like static
 - VCDs can contain thousands of cycle. We cannot perform dynamic analysis for the complete VCD;
 - Need to intelligently filter out critical cycles in the VCD
- **Using Cycle selection to identify the critical cycles in the VCD**
- **Two methods to filter the critical cycles**
 - WORST_POWER_CYCLE
 - WORST_DPDT_CYCLE
- **Once the critical cycle is selected, RedHawk does dynamic simulation for this cycle**
 - Pre-simulation cycles (from VCD) will be attached to the selected cycle
- **Both True-time and Non-true time VCDs can be used in cycle selection**
- **Both RTL and Gate level VCDs can be used for cycle selection**
- **The keyword SELECT_RANGE activates cycle selection.**
 - The VCD time between the values provided in SELECT_RANGE will be considered for cycle selection.



Cycle Select In VCD Based Analysis Flow



```
VCD_FILE {  
SELECT_RANGE <start_time> <end_time>  
SELECT_TYPE WORST_POWER_CYCLE  
}
```

```
VCD_FILE {  
SELECT_RANGE <start_time> <end_time>  
SELECT_TYPE WORST_DPDT_CYCLE  
}
```

WORST_POWER_CYCLE

GSR and Command file examples

GSR:

```
VCD_FILE {  
    GENERIC GENERIC.vcd  
    FILE_TYPE VCD  
    FRONT_PATH "GENERIC/"  
    SUBSTITUTE_PATH ""  
    SELECT_RANGE <start_time> <end_time>  
    SELECT_TYPE WORST_POWER_CYCLE  
    TRUE_TIME 1  
}
```

TCL:

```
import gsr GENERIC.gsr  
setup design  
setup analysis_mode dynamic  
perform pwrcalc  
perform extraction -power -ground -c  
perform analysis -vcd
```

- **DYNAMIC_SIMULATION_TIME** decides the window width of each cycle
- User can set "SELECT_RANGE -1 -1" to allow RedHawk to do a cycle selection for the entire VCD range

WORST_POWER_CYCLE (*Cont'd*)

- RedHawk does cycle by cycle power calculation

adsRpt/worst_power_cycle.rpt

```
# VCD_FILE ../../../../design_data/vcd/GENERIC.vcd
# BLOCK_NAME GENERIC
# SELECT_RANGE 0 5000
# SELECT_TYPE WORST_POWER_CYCLE
# FRAME_SIZE 1280
# WINDOW_GRIDS 2

# cycle power rank (sorted by average_power)
#   cycle_time(ps)      average_power(W)
1       0 to    2560      1.45887
2     1280 to    3840      1.33492
3     2560 to    5120      0.64573
```

- Selects cycle having highest power for dynamic simulation

WORST_DPDT_CYCLE

GSR and Command file examples

GSR:

```
VCD_FILE {  
    GENERIC GENERIC.vcd  
    FILE_TYPE VCD  
    FRONT_PATH "GENERIC/"  
    SUBSTITUTE_PATH ""  
    SELECT_RANGE <start_time> <end_time>  
    SELECT_TYPE WORST_DPDT_CYCLE  
    TRUE_TIME 1  
}
```

TCL:

```
import gsr GENERIC.gsr  
setup design  
setup analysis_mode dynamic  
perform pwrcalc  
perform extraction -power -ground -c  
setup package  
perform analysis -vcd
```

- **DYNAMIC_SIMULATION_TIME** decides the window width of each cycle.
- User can set “**SELECT_RANGE -1 -1**” to allow RedHawk to do a cycle selection for the entire VCD range.

Accuracy In Cycle Selection Based Power Calculation

- Accuracy can be selected using the below keyword:
 - POWER_CYCLE_SELECT_MODE [0 | 1 | 2]
 - 0: default value, time usage: low, memory usage: low, accuracy: low
 - 1: time usage: low, memory usage: high, accuracy: middle
 - 2: time usage: high, memory usage: high, accuracy: high

Result Exploration and Debugging

```
*****
**** Start Cycle Selection
*****  
  
INFO: Consider memory switching states from VCD file(s) in p  
Running vcdscan ../../design_data/vcd/GENERIC.vcd -tt -w  
5000p -f 1280p -o .apache/cfilter.0.pwr -ap NOPRINT -qs  
Reading ../../design_data/vcd/GENERIC.vcd ...  
Turn on module handle on begin/fork.  
ERROR(EVP-164): VCD symbol 'inst_129422/net_4412' is defined more than once, ignored.  
ERROR(EVP-164): VCD symbol 'inst_129422/net_3418' is defined more than once, ignored.  
ERROR(EVP-164): VCD symbol 'inst_129422/net_3418' is defined more than once, ignored.  
    0 memory with control defined  
Traversing transitions ...  
.5%WARNING(VCD-311): For instance inst_129539/adsU1, state c10 at 400ps, is too close to previous state c01 (less than 0.4*cycles). This state will be ignored.  
.11% ..16% ..22% ..27% ..32% ..38% ..43% ..49% ..54% ..59% ..64% ..70% ..75% ..80% ..85% ..90%  
.96% ..100%  
WALLTIME (Traversing transitions): 5 secs  
  
Summary for VCD/FSDB file ../../design_data/vcd/GENERIC.vcd:  
VCD/FSDB start time (1 ps) : 0  
Sim start time (ps) : 0  
Pre-sim start time (ps) : 0  
Sim end time (ps) : 5000  
CPU TIME (vcdscan): 0 hrs 0 mins 9 secs  
MEMORY USAGE (vcdscan): 383 MBytes  
  
***** Cycle selection summary *****  
Selection resolution (grid size) is 1280ps, total cycle 3  
Selection from 0ps to 5000ps, total grids 4  
Average power of the entire selection range: 1.14651 W
```

adsRpt/redhawk.log

1422,2

63%

Debug Tips in VCD Analysis

- **Check whether the VCD is imported correctly in RedHawk**
 - adsRpt/vcd_missing_signal_nets
 - adsRpt/vcd_missing_clock_nets
- **If close to 100% of nets are reported as missing in the VCD check the “FRONT_PATH” keyword in GSR**
 - Make sure that there is a trailing slash in the string specification
 - FRONT_PATH "test_bench1/GENERIC/"
 - Open the VCD in text editor and verify the scope statements
 - Scope statements define the hierarchy in VCD
 - If the input is FSDB, you can convert it into VCD using 3rd party conversion utilities and check
 - Load the VCD/FSDB in a 3rd party waveform viewer to browse the hierarchy
- **Use switching histograms to verify the VCD switching**
 - For scan shift VCDs, make sure that ~100% flops and clocks are switching
 - For MBIST VCDs, make sure that ~100% memories are switching
- **For true-time VCD analysis, make sure that VCD is timing back annotated**

Lab Exercise : VCD Analysis

- **Steps to be followed**

- cd GENERIC_tutorial/vcd_run
- cd worst_power
- Review GSR and command file
- redHawk -f run_dynamic.tcl

User control file (GSR):

```
VCD_FILE {
    GENERIC ../../design_data/vcd
        /GENERIC.vcd
FILE_TYPE VCD
FRONT_PATH "test_bench1/Generic/"
TRUE_TIME 1
SELECT_RANGE -1 -1
SELECT_TYPE WORST_POWER_CYCLE
}
```

```
# Import data
import gsr GENERIC.gsr
setup design
setup analysis_mode dynamic

# Calculate power
perform pwrcalc

# Power grid extraction
perform extraction -power -ground -c

# Lumped resistance (in Ohms)
# for package, wirebond and pads
# Default values are all 0, i.e no off-chip impact
setup package -power -r 0.005 -l 2.5 -c 5
setup package -ground -r 0.005 -l 2.5 -c 5
setup wirebond -power -r 0.01 -l 2.2 -c 1.42
setup wirebond -ground -r 0.05 -l 1.7 -c 0.2
setup pad -power -r 0.001
setup pad -ground -r 0.001

# Dynamic IR analysis
perform analysis -vcd

explore design
```

Setting Up The Dynamic Run

- **cd GENERIC_tutorial/dynamic_run**
- **Review the GSR and Command file**
- **Kickoff the dynamic run**
 - redhawk –f run_dynamic.tcl

GSR Options for Dynamic Analysis

```
# Dynamic simulation time determines length of transient simulation
#( default: 1/Freq)
DYNAMIC_SIMULATION_TIME 20ns

# Turn on dynamic pre-simulation
# specify time or -1 for automatic setting
# The second entry is the time-step speed-up during
# pre-simulation (default = 1, same as the simulation time-step)
DYNAMIC_PRESIM_TIME -1

# Transient simulation time step (default: 10ps)
DYNAMIC_TIME_STEP 10ps
```

Dynamic Run Command File

Data Preparation

Running Dynamic

Result Exploration

```
# Import data
import gsr GENERIC.gsr
setup design

setup analysis_mode dynamic

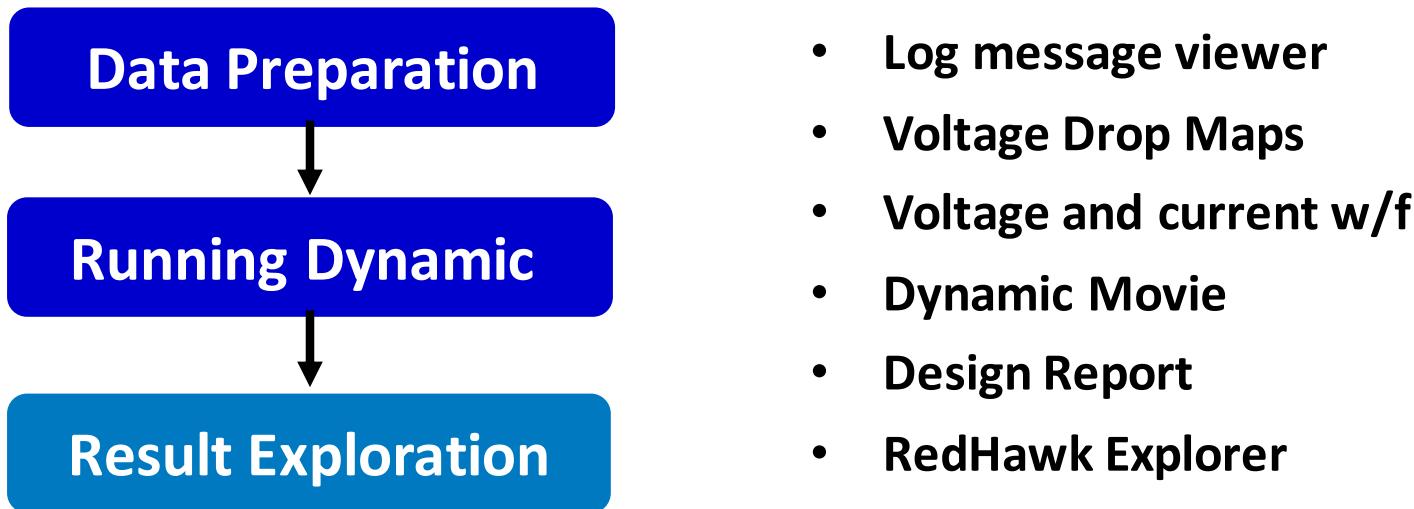
# Calculate power
perform pwrcalc

# Power/Ground grid extraction
# (extract capacitance too!)
perform extraction -power -ground -c

# Lumped resistance (in Ohms)
# for package, wirebond and pads
setup package -power -r 0.005 -l 2.5 -c 5
setup package -ground -r 0.005 -l 2.5 -c 5
setup wirebond -power -r 0.01 -l 2.2 -c 1.42
setup wirebond -ground -r 0.05 -l 1.7 -c 0.2
setup pad -power -r 0.001
setup pad -ground -r 0.001

# Dynamic IR analysis
perform analysis -vectorless
explore design
```

Result Exploration and Debugging



Examine Summary of Results

Log Message Viewer <@sjoindqa128-2.ansys.com>

Errors/Warnings Summary CPU/Memory and Usage Setup Design Power Results

Worst Dynamic Voltage Drop:

```
Type value net ideal_volt location name
-----
WIRE 194.10mV VDD 1.200 (623.800,1391.943) METAL3
WIRE 197.00mV VSS 0.000 (605.995,1476.103) METAL3
avgTW 298.54mV VDD 1.200 (2718.110,2804.189) inst_129422/inst_7730
maxTW 283.50mV VDD 1.200 (2718.110,2804.189) inst_129422/inst_7730
minTW 322.22mV VDD 1.200 (2137.970,2896.774) inst_129422/inst_7776
minWC 390.89mV VDD 1.200 (678.713,1374.708) inst_129400/adsU1
```

The worst instance voltage drops report file is adsRpt/Dynamic/GENERIC.dvd
The worst node voltage drops report file is adsRpt/Dynamic/GENERIC.ir.worst

Total Instance Count = 75618

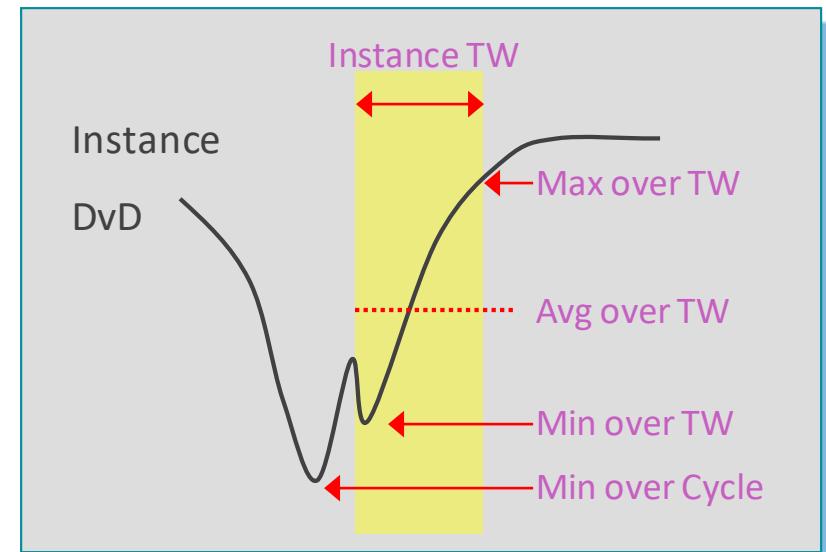
	Voltage Drop(%)	tw_avg	tw_max	tw_min	wc_min	min_vdd	max_vss
0 - 5		110	239	74	2	2554	13618
5 - 10		9912	16724	6232	434	67023	61992
10 - 15		47028	52601	40123	19110	6037	4
15 - 20		18162	6021	27843	48520	0	0
20 - 25		402	29	1340	7548	0	0
25 - 30		0	0	2	3	0	0
over 30		0	0	0	1	0	0

tw_avg: Instance average (VDD-VSS) drop over its timing window.
tw_max: Instance maximum (VDD-VSS) drop over its timing window.
tw_min: Instance minimum (VDD-VSS) drop over its timing window.
wc_min: Instance minimum (VDD-VSS) drop over simulation cycle.
min_vdd: Instance minimum VDD drop over simulation cycle.
max_vss: Instance maximum VSS bounce over simulation cycle.

Log file adsRpt/Log/redhawk.log.2016-02-11-04:31:47 Browse... Apply Refresh

DVD summary

Text report pointers



* Log/error/warnings/command history stored under adsRpt/<>.date

Examine Summary of Results (*Cont'd*)

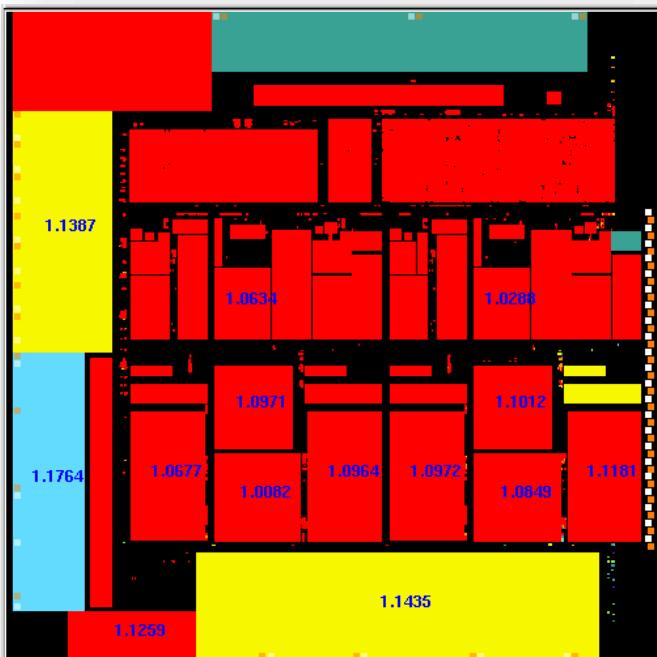
- Summarizes variation in current load for all switches
- Can identify the in-effective switches from this report
- Switches supplying high current also cause high voltage drop

```
#Report dynamic results of switch voltage and current
#instance_name  type  worst_int_Vdd/Vss(Volt)  maximal_Vsw(Volt)  maximal_Isw(Amp)
(SAT)
#SAT: maximal_Isw > saturation_current as specified in switch model file
inst_129973/switch_inst_R17_C52 header 1.119756e+00 1.922202e-02 9.611333e-04
inst_129973/switch_inst_R16_C52 header 1.119146e+00 1.525557e-02 7.628108e-04
inst_129973/switch_inst_R15_C52 header 1.118383e+00 1.235688e-02 6.178761e-04
inst_129973/switch_inst_R14_C52 header 1.117773e+00 1.022124e-02 5.110944e-04
inst_129973/switch_inst_R13_C52 header 1.117010e+00 8.848190e-03 4.424418e-04
inst_129973/switch_inst_R12_C52 header 1.116247e+00 7.932901e-03 3.966773e-04
inst_129973/switch_inst_R11_C52 header 1.115789e+00 7.475138e-03 3.737891e-04
inst_129973/switch_inst_R10_C52 header 1.115332e+00 7.475257e-03 3.737951e-04
inst_129973/switch_inst_R9_C52 header 1.115332e+00 7.475257e-03 3.737951e-04
inst_129973/switch_inst_R8_C52 header 1.115484e+00 7.932901e-03 3.966773e-04
inst_129973/switch_inst_R7_C52 header 1.116095e+00 8.695722e-03 4.348183e-04
inst_129973/switch_inst_R6_C52 header 1.116857e+00 9.458423e-03 4.729534e-04
inst_129973/switch_inst_R5_C52 header 1.117925e+00 1.067889e-02 5.339766e-04
inst_129973/switch_inst_R4_C52 header 1.119603e+00 1.220441e-02 6.102527e-04
```

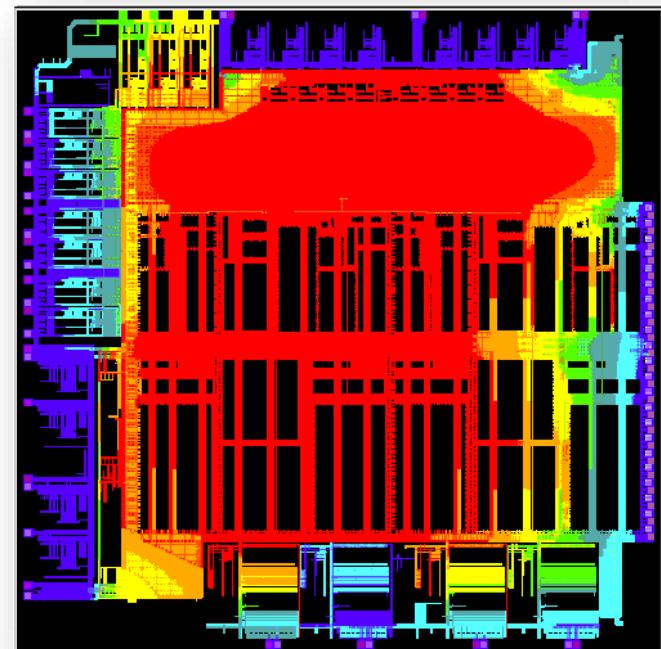
“switch_dynamic.rpt” stored under: adsRpt/Dynamic

Explore Dynamic Results

- **View → Dynamic Instance DvD**
 - Max Vdd-Vss Over Time Window
 - Min Vdd-Vss Over Time Window
 - Avg Vdd-Vss Over Time Window
 - Min Vdd-Vss Over Whole Cycle



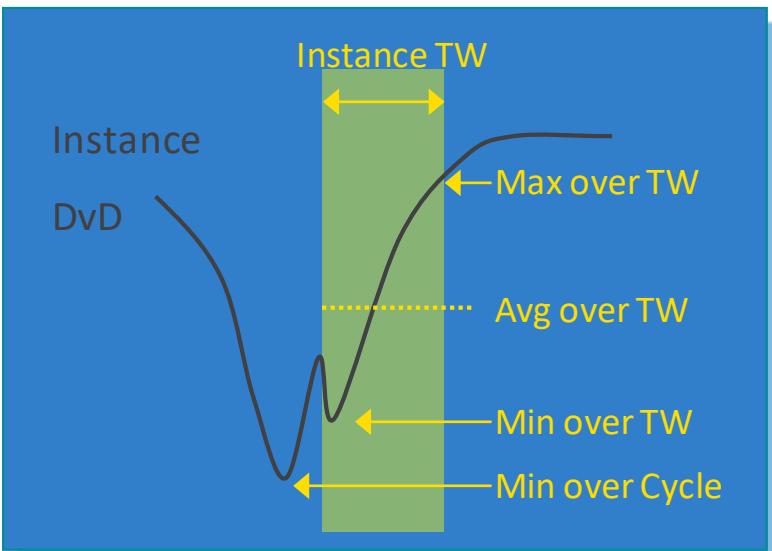
- **View → Voltage Drop Maps**
 - Wire & Via
 - Instance



Voltage Drop Map : Wire&Via

Explore Dynamic Results (Cont'd)

- Worst Instance DvD report
- Results -> List of Worst Instance DVD
- Avg/Max/Min over TW and Min Whole Cycle
- Need 'DYNAMIC_SAVE_WAVEFORM 1' to use 'DvD Plot' (disk space!)



A List of Worst instance DVD <@sjoindqa128-2.ansys.com>

	Ideal Vdd	Avg DV	Max DV	Min DV	Min DV WC	Location(x y)	Name
1	1.2000	0.9015	0.9165	0.8931	0.8931	2718.11 2804...	inst_129422/inst_7730
2	1.2000	0.9421	1.0050	0.8778	0.8507	2137.97 289...	inst_129422/inst_7776
3	1.2000	0.9453	1.0002	0.9453	0.9453	2683.41 388...	inst_129974/inst_492109
4	1.2000	0.9454	0.9631	0.9440	0.9440	2617.63 3895...	inst_129974/inst_492042
5	1.2000	0.9456	1.0000	0.9442	0.9442	2633.73 389...	inst_129974/inst_492036
6	1.2000	0.9458	1.0230	0.9450	0.9450	2591.41 3880...	inst_129974/inst_491655
7	1.2000	0.9458	0.9961	0.9447	0.9447	2648.68 385...	inst_129974/inst_495145
8	1.2000	0.9458	0.9641	0.9448	0.9448	2629.36 386...	inst_129974/inst_491807
9	1.2000	0.9459	0.9538	0.9450	0.9450	2591.41 3884...	inst_129974/inst_492082
10	1.2000	0.9459	0.9572	0.9453	0.9453	2679.27 387...	inst_129974/inst_492104
11	1.2000	0.9460	1.0226	0.9453	0.9453	2568.64 390...	inst_129974/inst_495307
12	1.2000	0.9461	1.0244	0.9453	0.9453	2640.40 382...	inst_129974/inst_495150
13	1.2000	0.9461	0.9650	0.9451	0.9451	2607.28 384...	inst_129974/inst_491520
14	1.2000	0.9461	0.9541	0.9455	0.9455	2616.25 3810...	inst_129974/inst_491393
15	1.2000	0.9463	0.9936	0.9447	0.9447	2623.38 384...	inst_129974/inst_495108

● Vdd Domain: All ○ Ideal Vdd: 1.200 SortBy: Avg Vdd-Vss Threshold: 5.00 % Apply

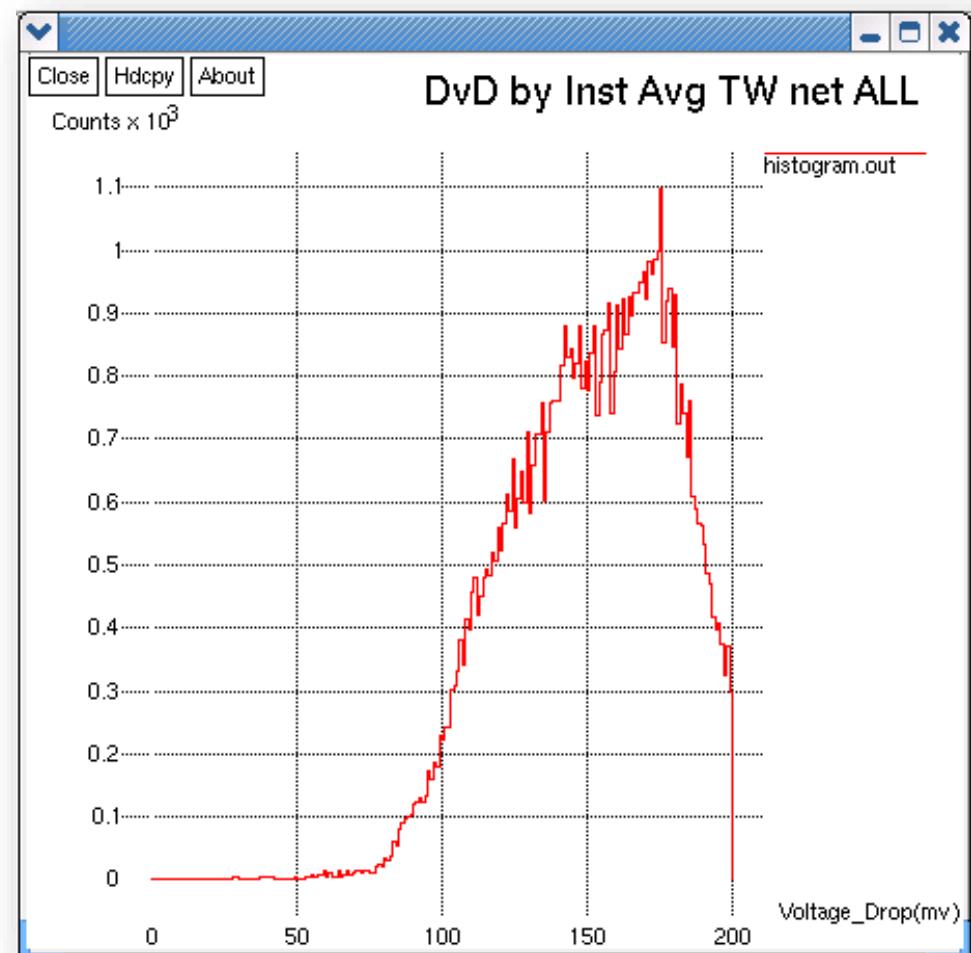
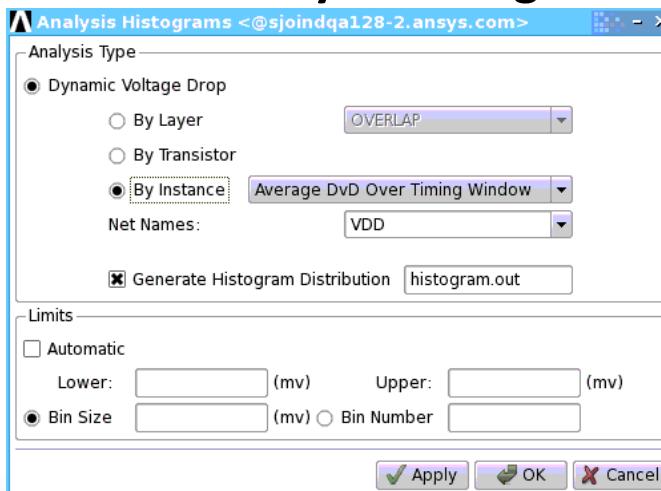
Zoom Export List DvD Plot Up Down First Last Prev Next Cancel

Dynamic Voltage Drop Histogram

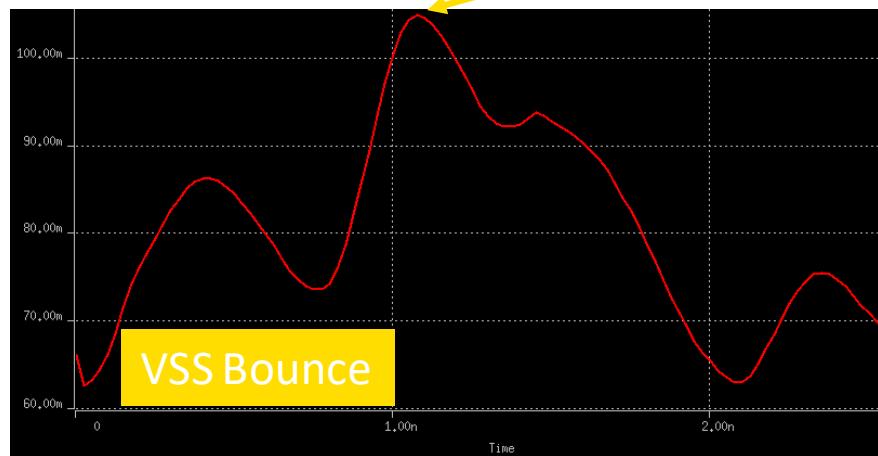
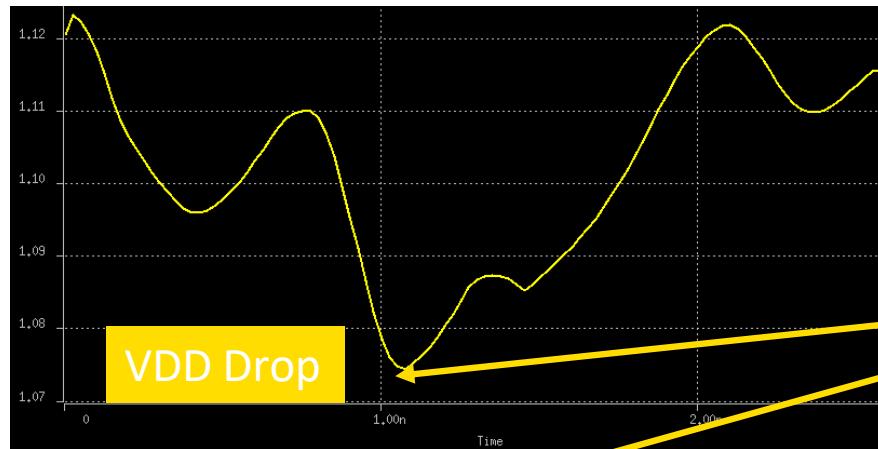
- **TCL command for generating histogram**

```
plot analysis -type DvD  
-instance avgTW  
-lower 0 -upper 200  
-binnumber 200
```

- **GUI option**
- **Results - > Analysis histograms**



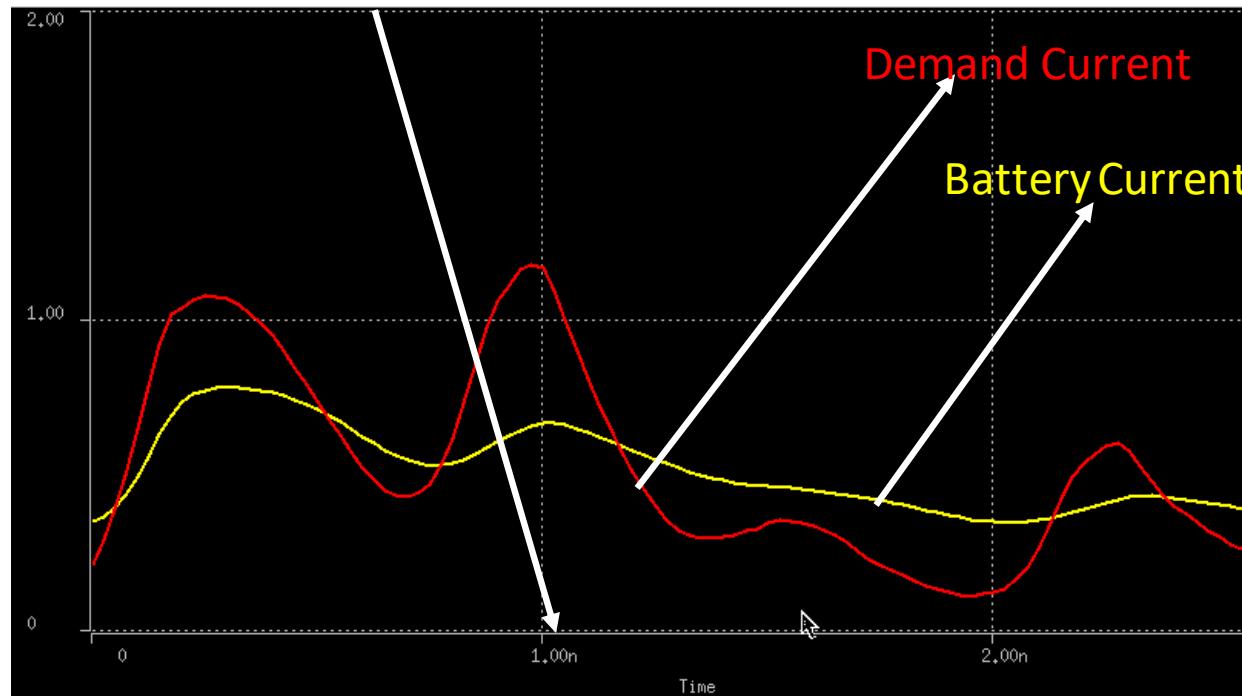
Instance Voltage Waveform



```
plot voltage -name inst_129734 -sv
```

Current Waveforms

Max Current at around 1ns !

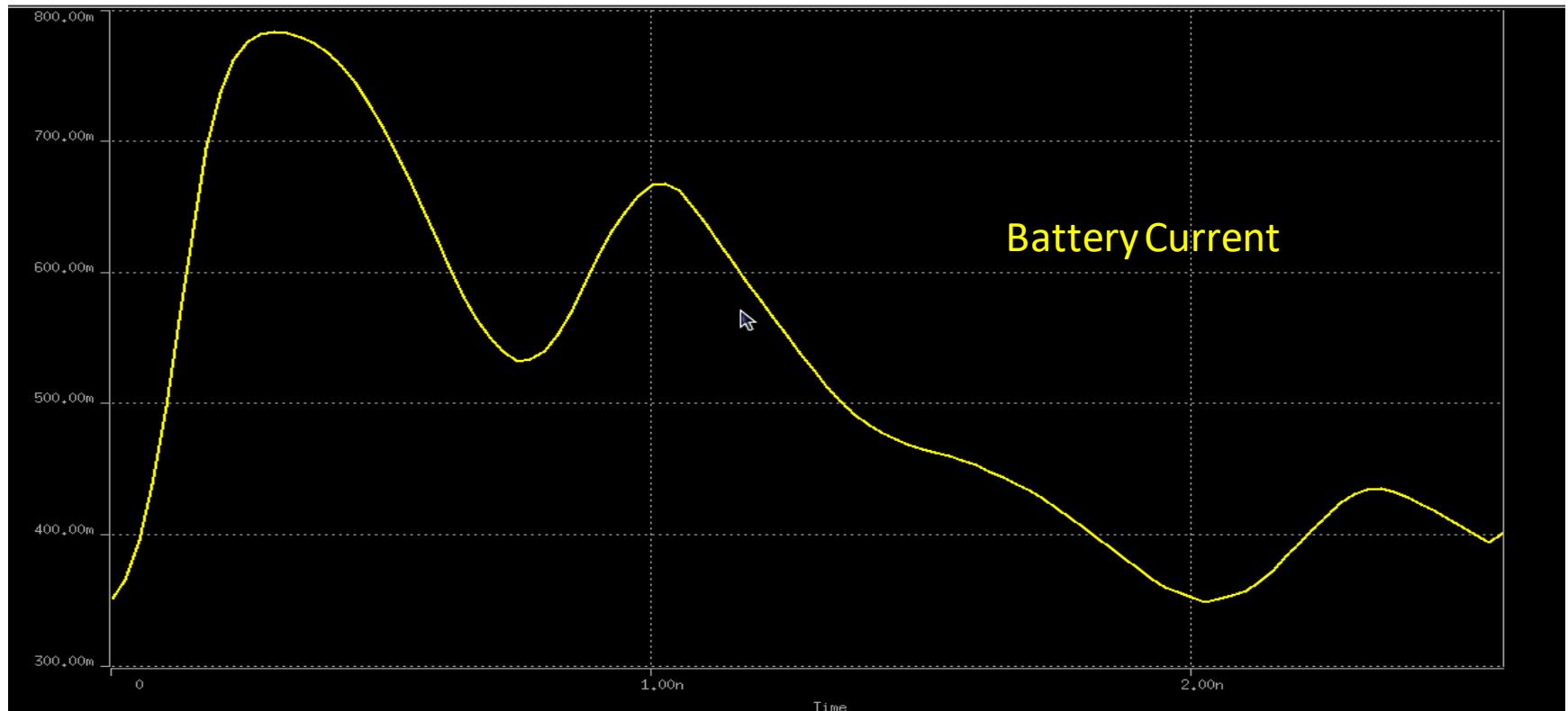


```
plot current -net -power -pad -overlay -sv
```

NOTE: Big difference between demand current and battery current

Indicates effectiveness of decaps

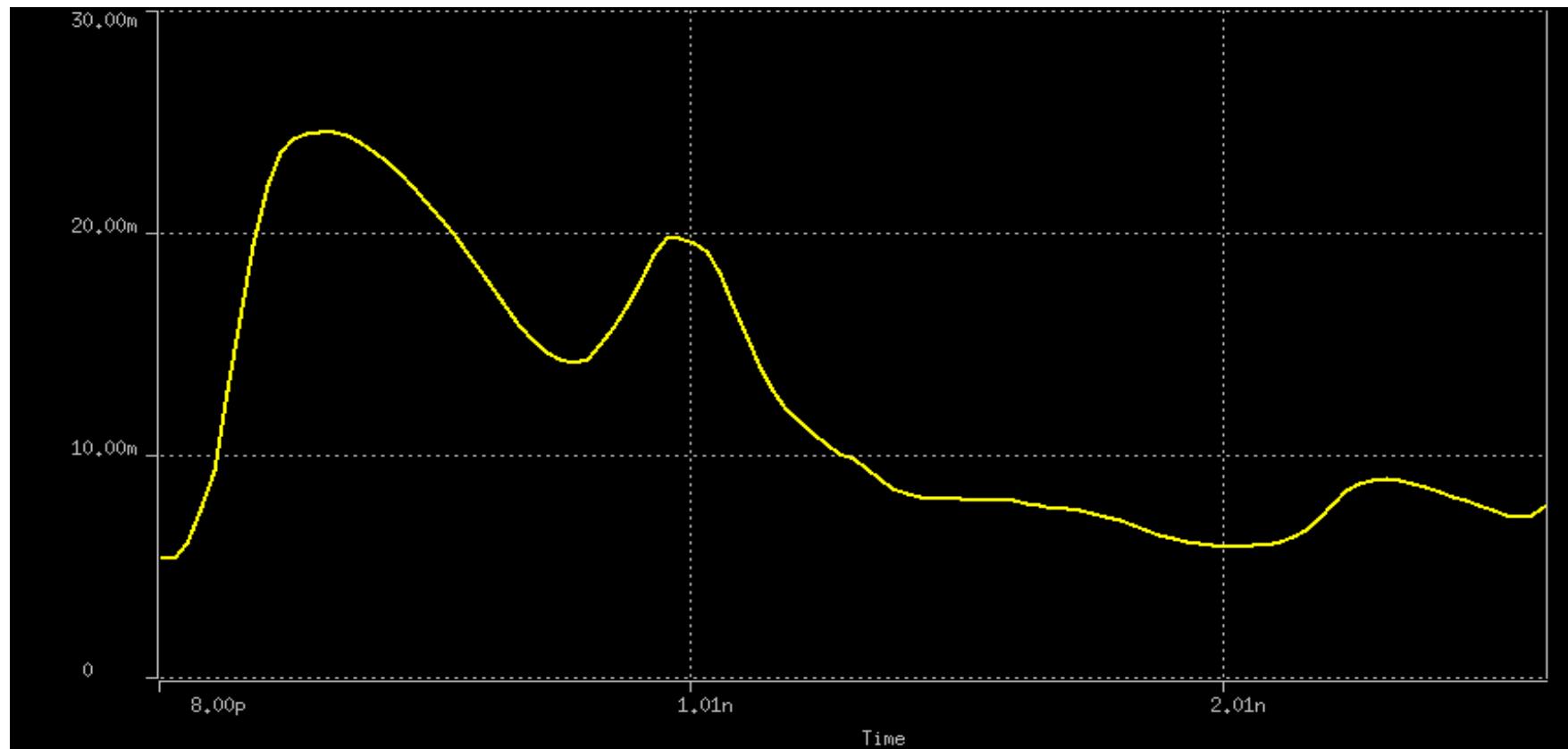
Current Waveforms (Cont'd)



```
plot current -net -name VDD -pad -sv
```

Current through all the pads with respect to net VDD

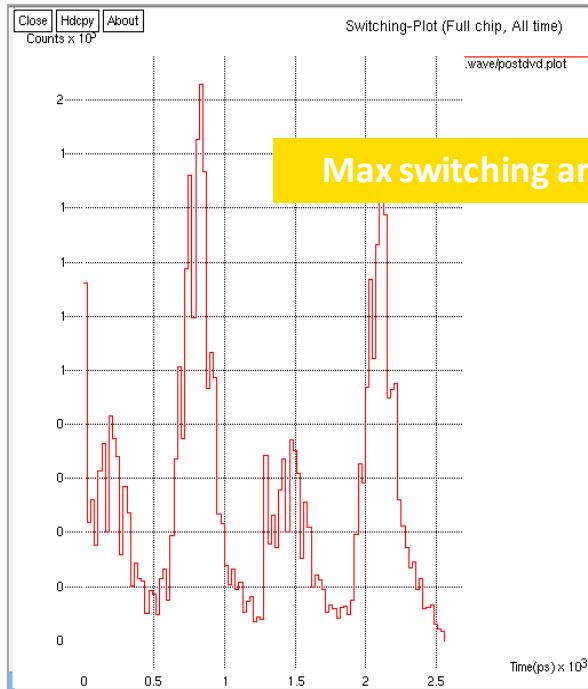
Current Waveforms (Cont'd)



```
plot current -pad -name DVDD1 -sv
```

Current through the pad DVDD1

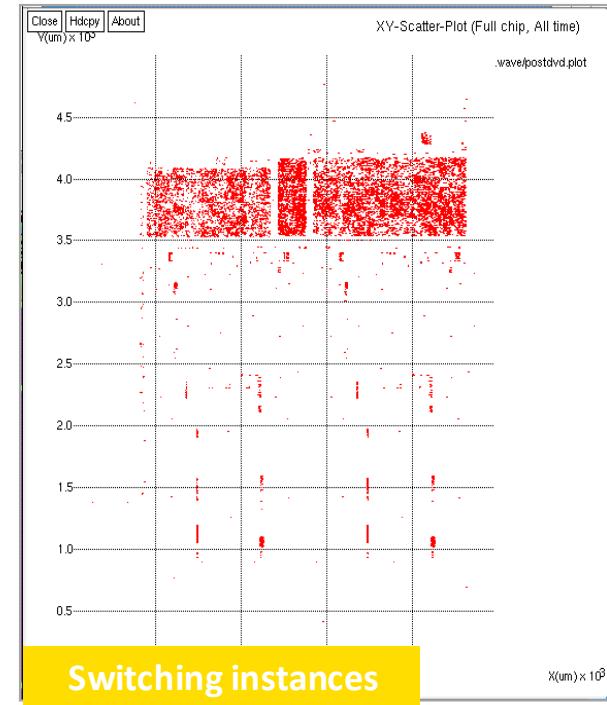
Switching Histogram



plot switching



plot charge



switching instances

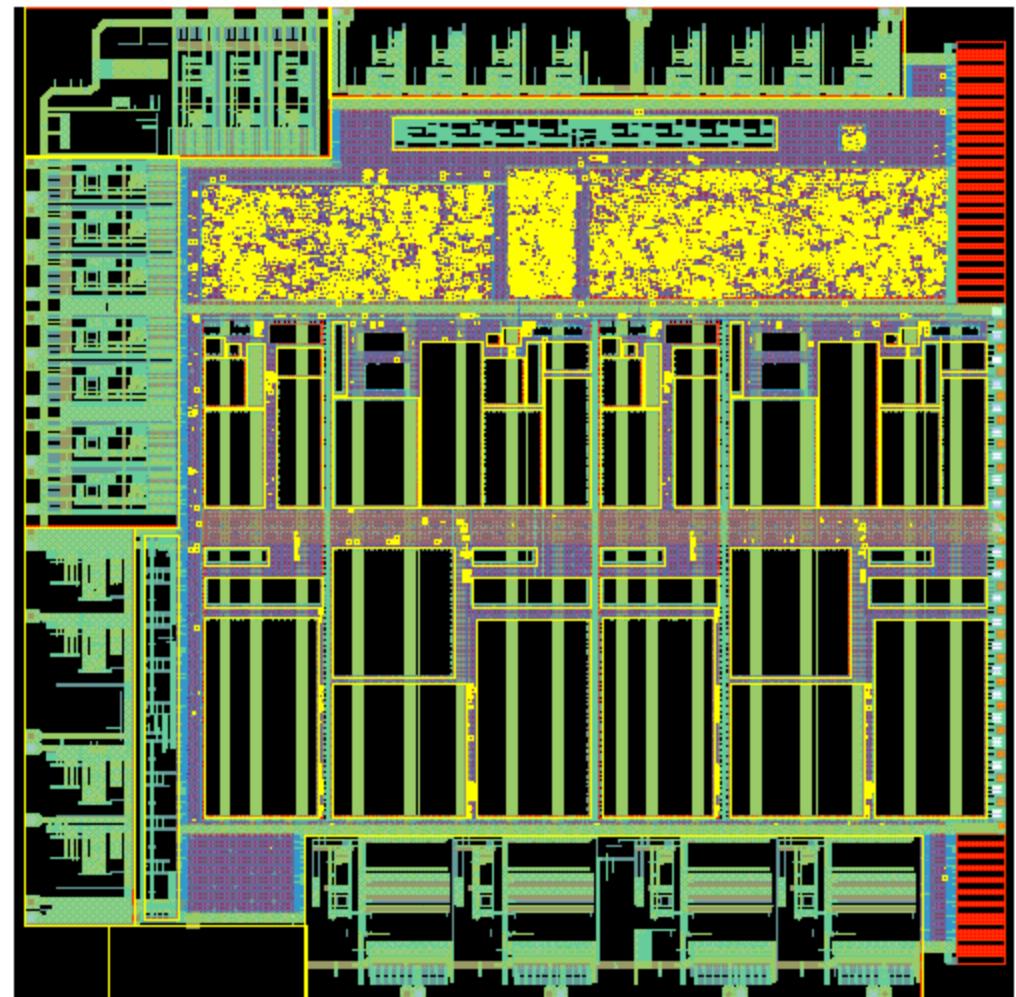
- Histograms can be generated for user given regions and time ranges with “condition set” command
- Plot switching w.r.t specific cell_type can be obtained. First use "condition set -type [all | combinational | sequential | clock| memory]" to pick the cell type and then do a “plot switching”

Analyzing the Switching Events

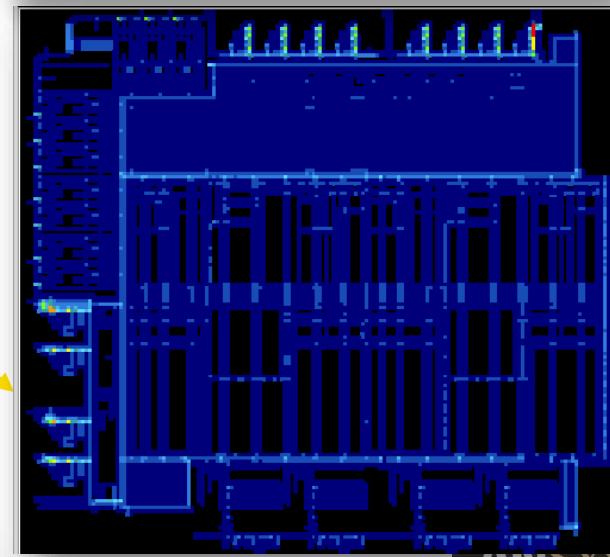
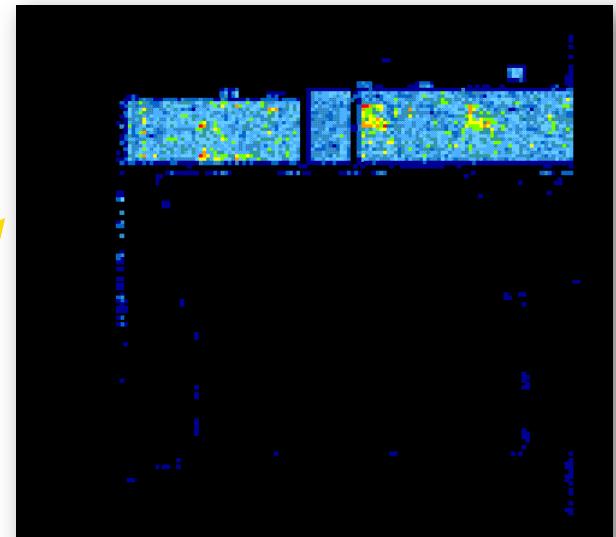
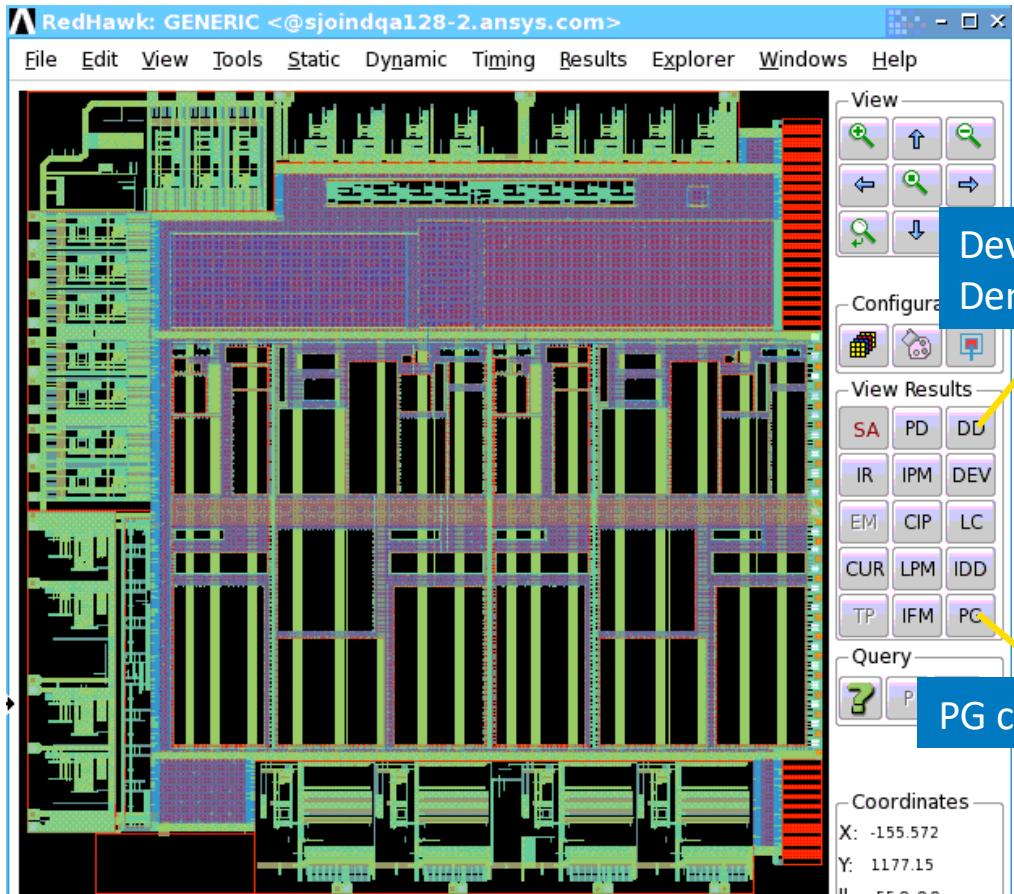
select add [print sw]

Command “print sw” lists all switching instances

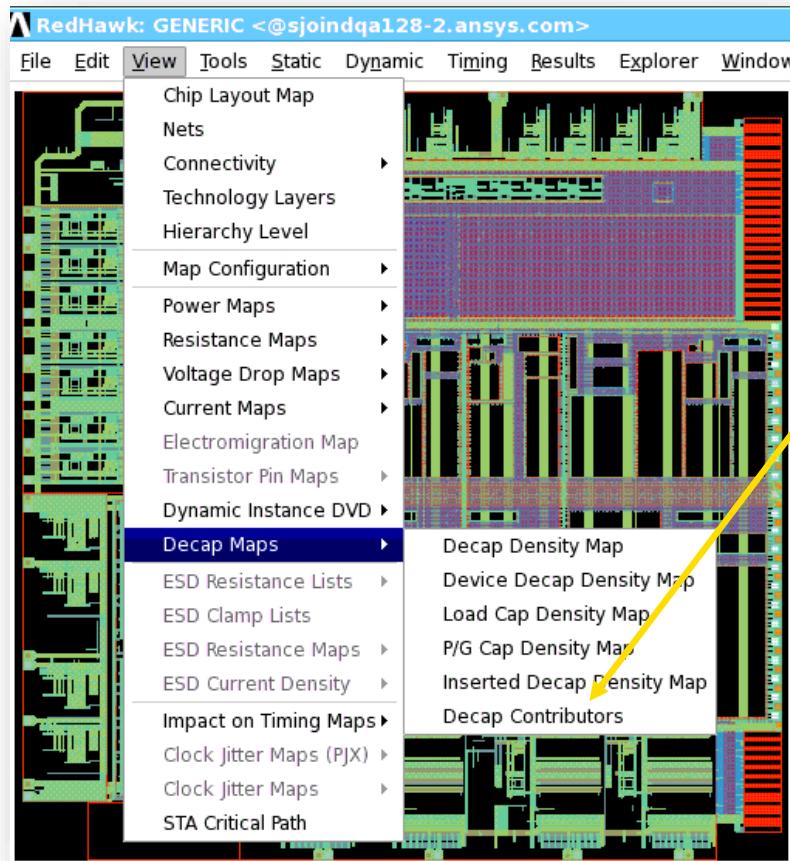
Simultaneous switching causes high voltage drop at around 1ns !!!



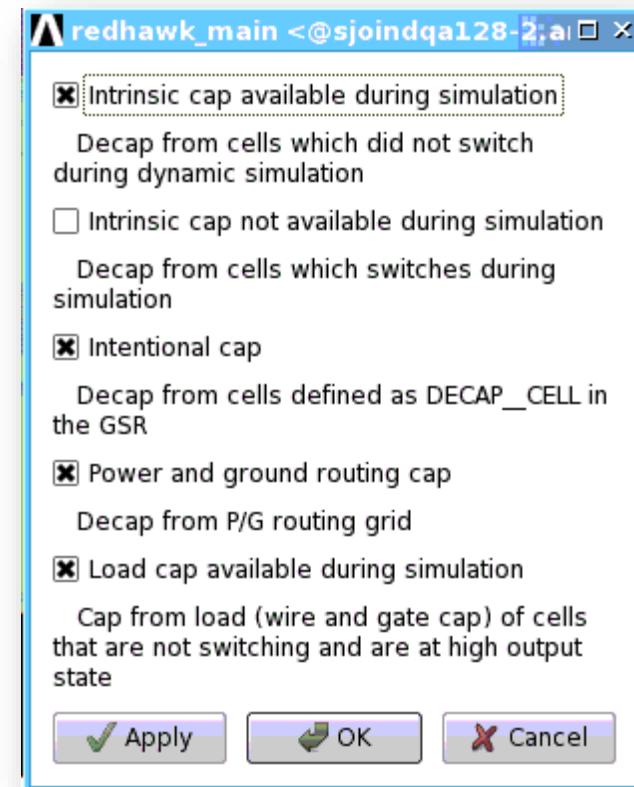
Decap Density Maps



Decap Density Maps (Cont'd)



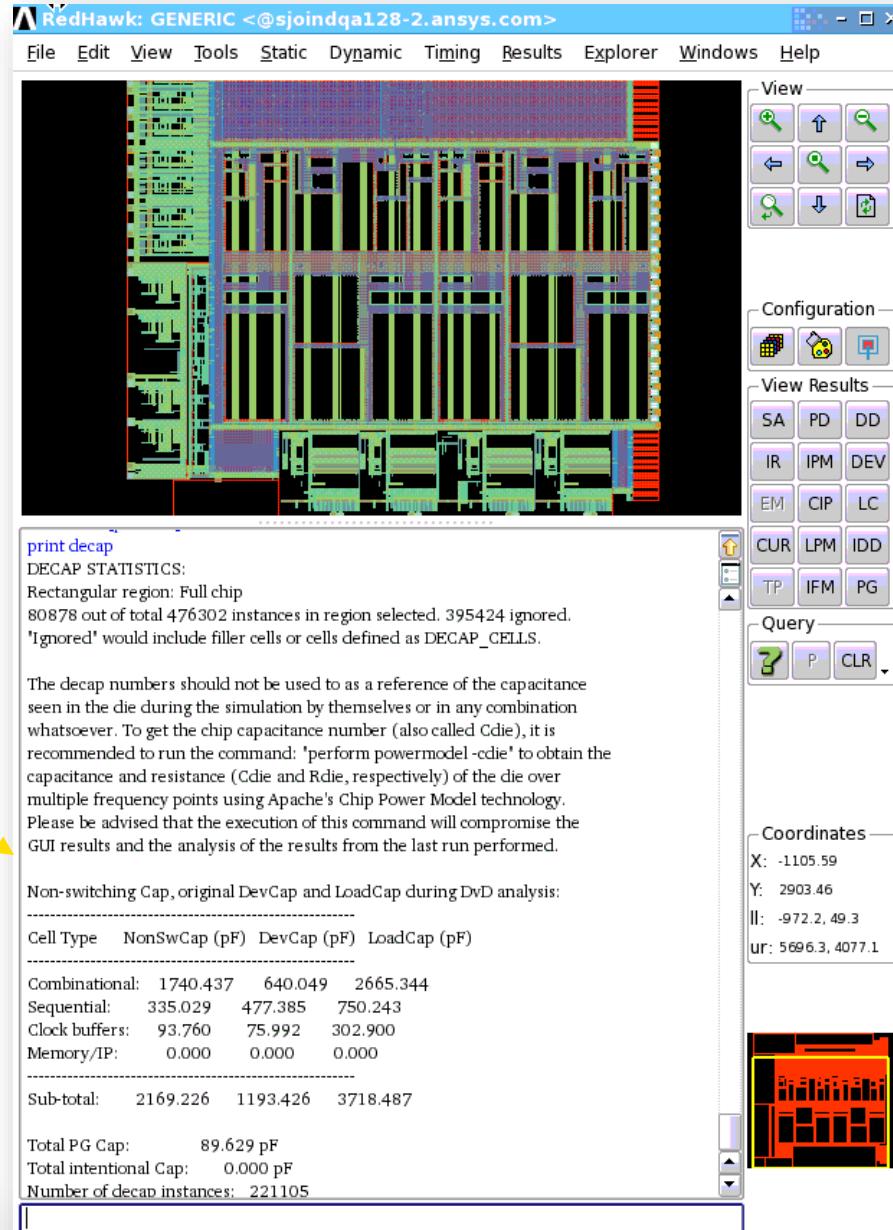
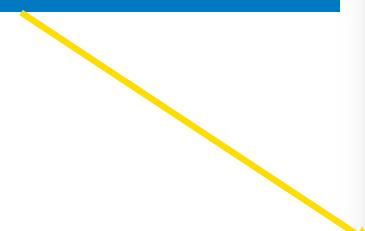
Select the decap contributors for Decap Density Map



Set GSR keyword DECAP_TILE_MAX for setting uniform tile size to all decap related maps

Decap Report

"print decap" command
showing detailed decap report



Dynamic Voltage Drop Movie



➤ Dynamic Movie

➤ *Results -> Movie -> Make*



Dynamic Analysis Reports

adsRpt/Dynamic/GENERIC.dvd	Dynamic instance voltage drop
adsRpt/Dynamic/GENERIC.ir.worst	Wire voltage drop
adsRpt/Dynamic/pad.current	Current waveforms: Current through each pad
adsRpt/apache.refCell.noApl*	Lists of cells without APL data

Dynamic Analysis - Summary

- **Data requirements and setup are similar to static, except:**
 - needs switching time for instances
 - uses APL data for accuracy
- **True transient simulation**
- **Considers**
 - On-chip and off-chip capacitance and inductance
 - Simultaneous cell switching
- **Much more realistic modeling of voltage drop than static**

Result Exploration using RedHawk Explorer

Summary Section

RedHawk™-Explorer

ANSYS

Summary Data Integrity Design Weakness Hotspots Performance

Back Forward 3D-IC FAQ

Design Summary Results Summary

Power Summary Static Voltage Drop Summary Dynamic Voltage Drop Summary Current w/f Summary Power EM Summary Signal EM Summary PathFinder Summary Low Power Analysis Summary CPM Summary

Run Details

Design Statistics

Key Parameters

Design Name	GENERIC
Design Size	4920.62u x 5000.36u
Instance Count	476302
No of Voltage domains	2(Power) & 1(Ground)
Total Power	0.75 W

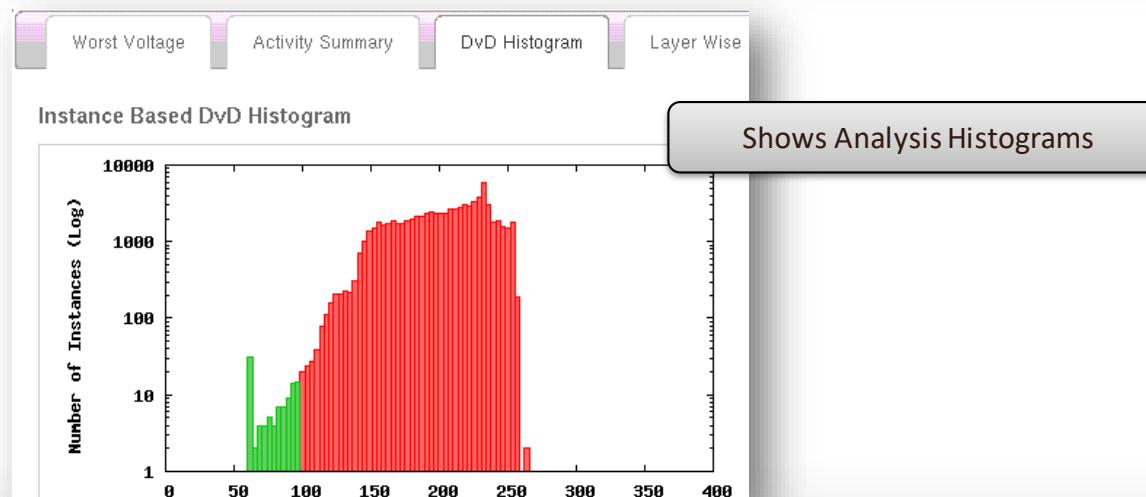
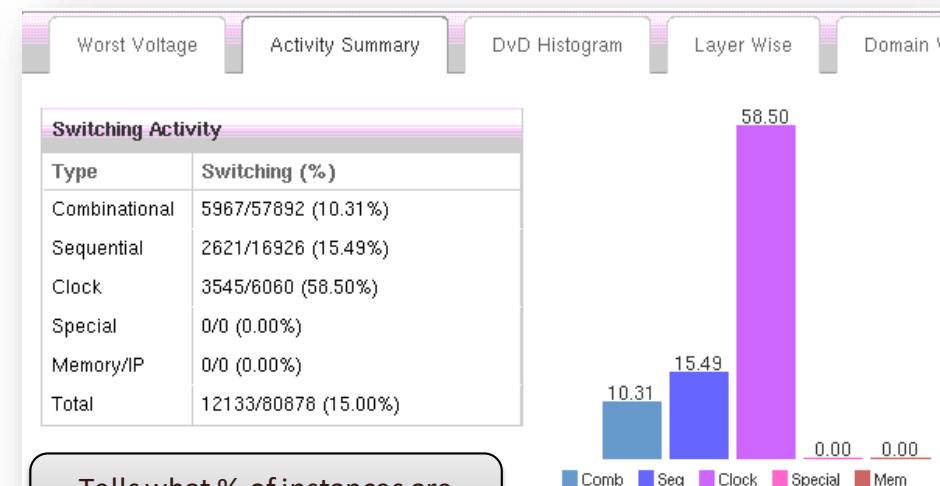
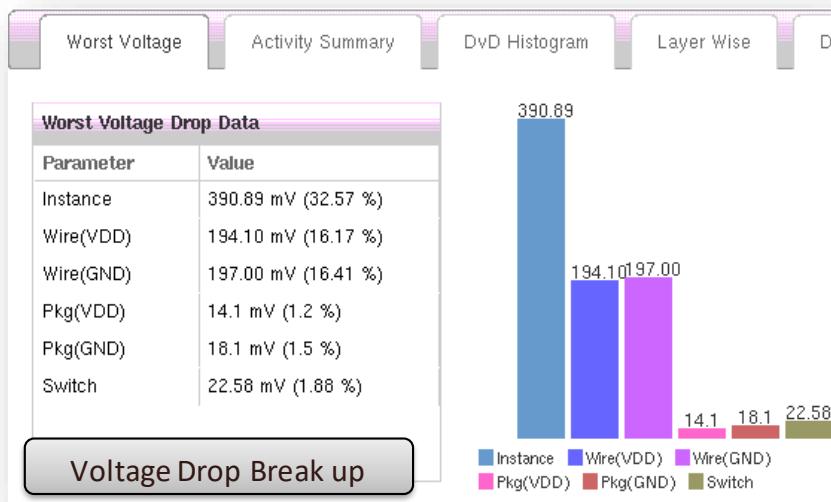
Design Summary Result Summary Power Summary Dynamic Voltage Drop Summary Power EM Summary Current W/f Summary Run Details

Chip Layout

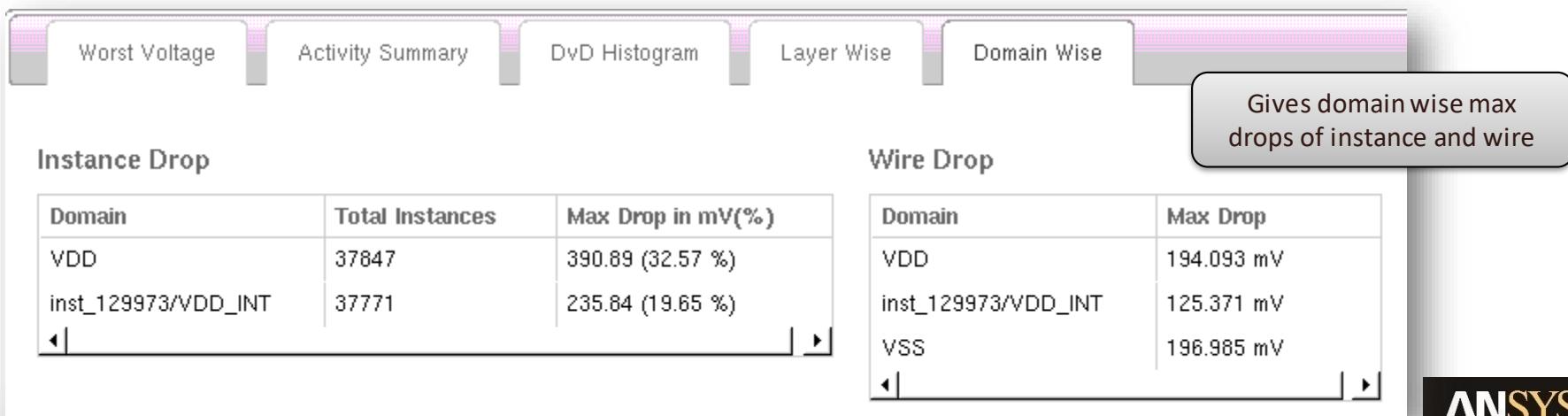
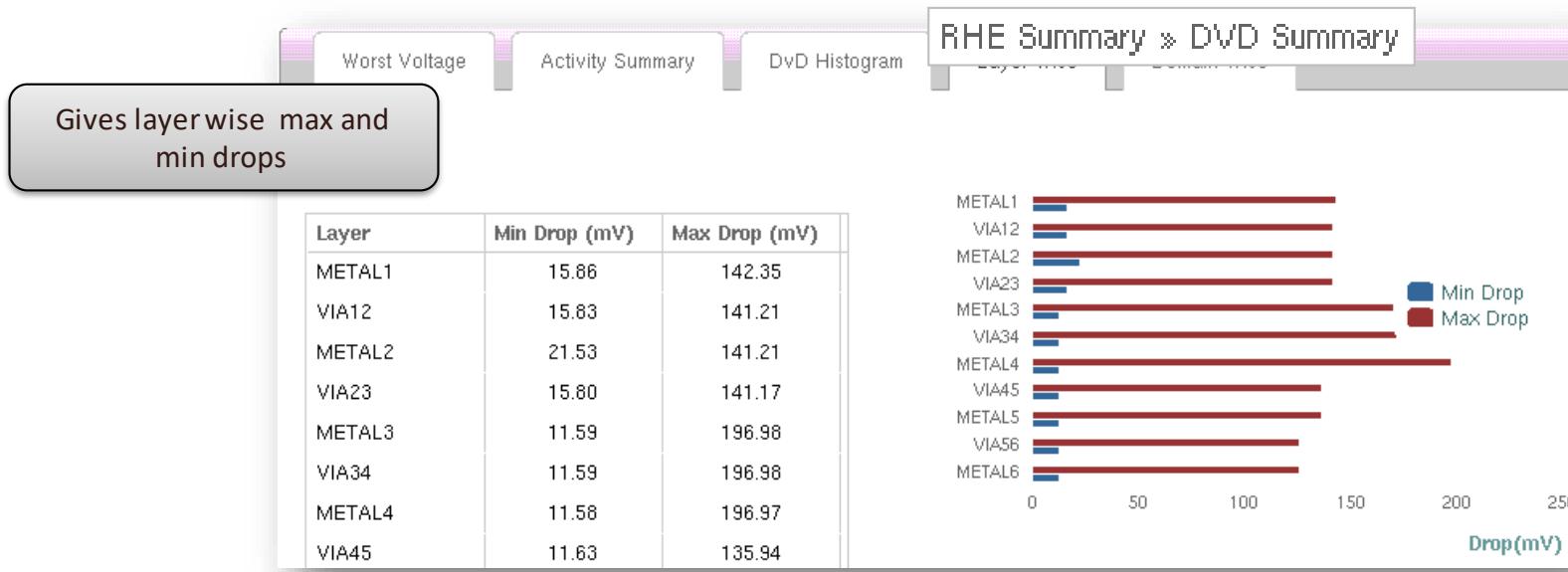
ANSYS

DVD Summary

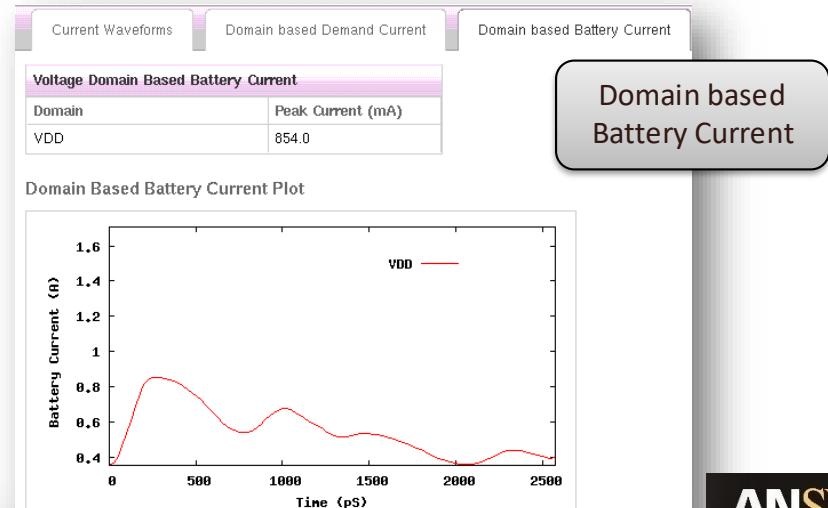
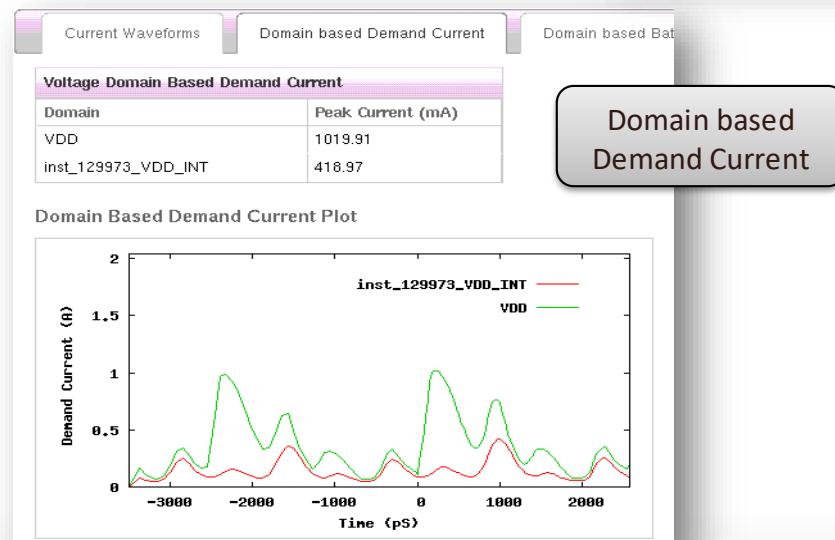
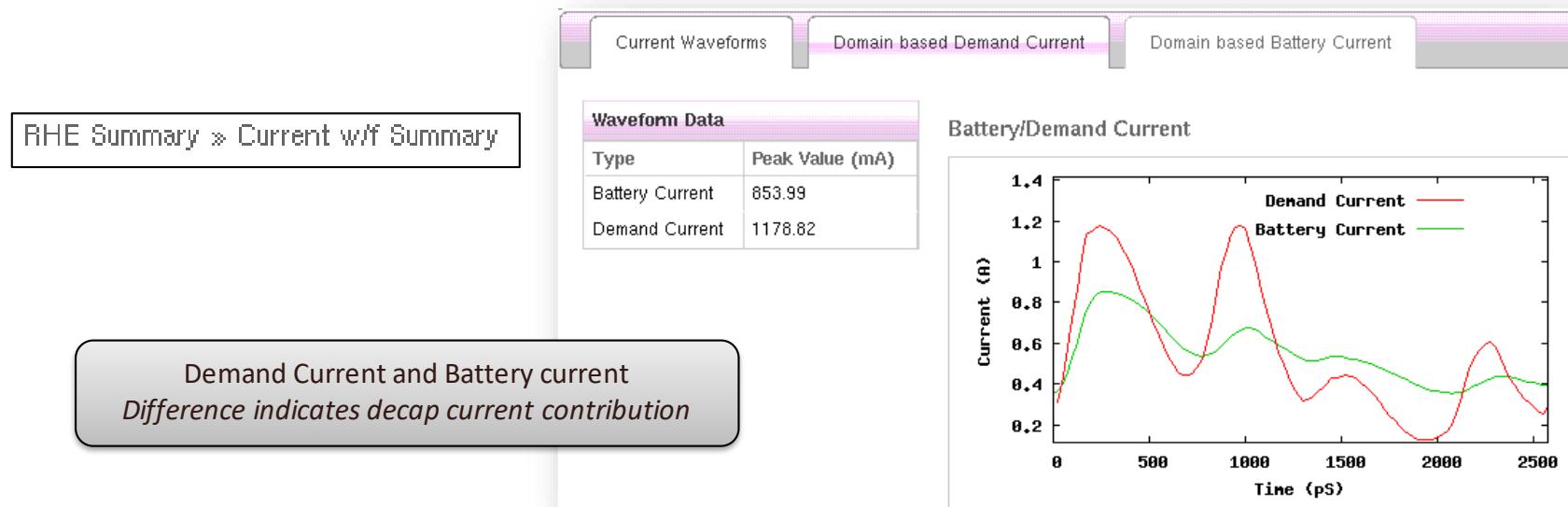
RHE Summary » DVD Summary



DVD Summary



Current Waveforms Summary



Data Integrity Check Summary

Summary **Data Integrity** Design Weakness Hotspots Performance

◀ Back Forward ▶ 3D-IC ↻ ⓘ FAQ

Library Data

APL Current Check	✓
APL Cap Check	✗
APL Pwcap Check	
LIB Check	✓
LEF Check	✓
CMM Check	
Gds2def Check	✗

Design Data

DEF Check	✗
SPEF Check	✓
IPF Check	
STA Check	✓
VCD Check	

RedHawk Data

GSR Tcl Check	✗
Package Settings	✓
PAD_FILES	✓
GSC FILE	

Log Summary

ERROR Check	✗
WARNING Check	✗

Data Integrity Summary

Analysis Summary

Input Data	Status	Summary Description
APL Current Check	✓	APL Current coverage is 99.08 %
APL Cap Check	✗	APL Cap coverage is only 17.00 %
SPEF Check	✓	SPEF coverage is 95.10 %
STA Check	✓	STA coverage is 99.21 %
LEF Check	✓	LEF coverage is 100.00 %

RED cross indicates that there is a problem with this input

Move the mouse pointer above the table rows to highlight the corresponding violation area.

Violation Areas

- Design specific data integrity check
- Helps to identify and understand impact of missing data
- Breaks design into regions and presents missing data for each region

Data Integrity Check : DEF Check

Missing Via Debug

The screenshot illustrates a data integrity check process, specifically a 'MISSING VIAS CHECK'. At the top, there are three tabs: 'Shorts Check', 'Instance Unconnect', and 'Wire Unconnect'. A blue arrow points from the 'Wire Unconnect' tab to a callout box containing the text: 'Direct zoom into RH GUI by clicking on the image'.

The main area displays a 'MISSING VIAS CHECK' report:

- Check the number of missing vias in a design is not more than 10000
- Number of missing vias Reported : 116

Below the report, a section titled 'Highlighting Regions with Missing Via in GUI' shows a schematic or layout view with several small white squares scattered across it. A blue arrow points from this section to a callout box containing the text: 'Highlights Regions with missing vias (User can click and zoom into RH)'.

To the right, a RedHawk tool window titled 'RedHawk: GENERIC <@mercury>' is shown. It displays a complex grid-based layout with various colored lines and markers. A white arrow points from the 'Exact locations highlighted with marker' callout box to a specific location in the RedHawk window where a yellow marker is placed on a wire segment.

Highlights Regions with missing vias
(User can click and zoom into RH)

Direct zoom into RH GUI by clicking on the image

Exact locations highlighted with marker

DEF Check: Related Reports

Data Integrity » Def Check » Related Reports

Def Check

Related Output Reports

Report	Line Count	Definition
adsRpt/apache.missingVias	116	Provides a list of missing via locations in the design
adsRpt/shorts.rpt	0	Provides a list of short locations in the design
adsRpt/GENERIC.power.unused	0	Provides list of instances that are not hooked to the power network
adsRpt/GENERIC.PG.unconnect	0	Provides list of instances belonging to analyzed PG network that are physically isolated from VDD and GND
		Provides list of in

Data Integrity » Def Check » Related Reports » adsRpt/apache.missingVias

```
VSS METAL4 METAL3 805.23 2302.97 -0.00518688
VDD METAL4 METAL3 4242.55 2120.86 -0.00518692
VDD METAL4 METAL3 4078.84 2474.49 -0.00533938
VDD METAL4 METAL3 4077.41 2474.49 -0.00533938
VDD METAL4 METAL3 4075.97 2474.49 -0.00533938
VDD METAL4 METAL3 4817.96 1988.02 -0.00549197
VSS METAL4 METAL3 4820.38 2124.7 -0.00564455
VDD METAL4 METAL3 3961.59 3020.98 -0.00564456
VDD METAL4 METAL3 910.08 2263.74 -0.00579703
VSS METAL5 METAL4 4689.33 1991.86 -0.0057971
VDD METAL4 METAL3 3544.54 2484.56 -0.00579715
```

GSR/Tcl Check

Data Integrity » GSR TCL Check

GSR TCL Check

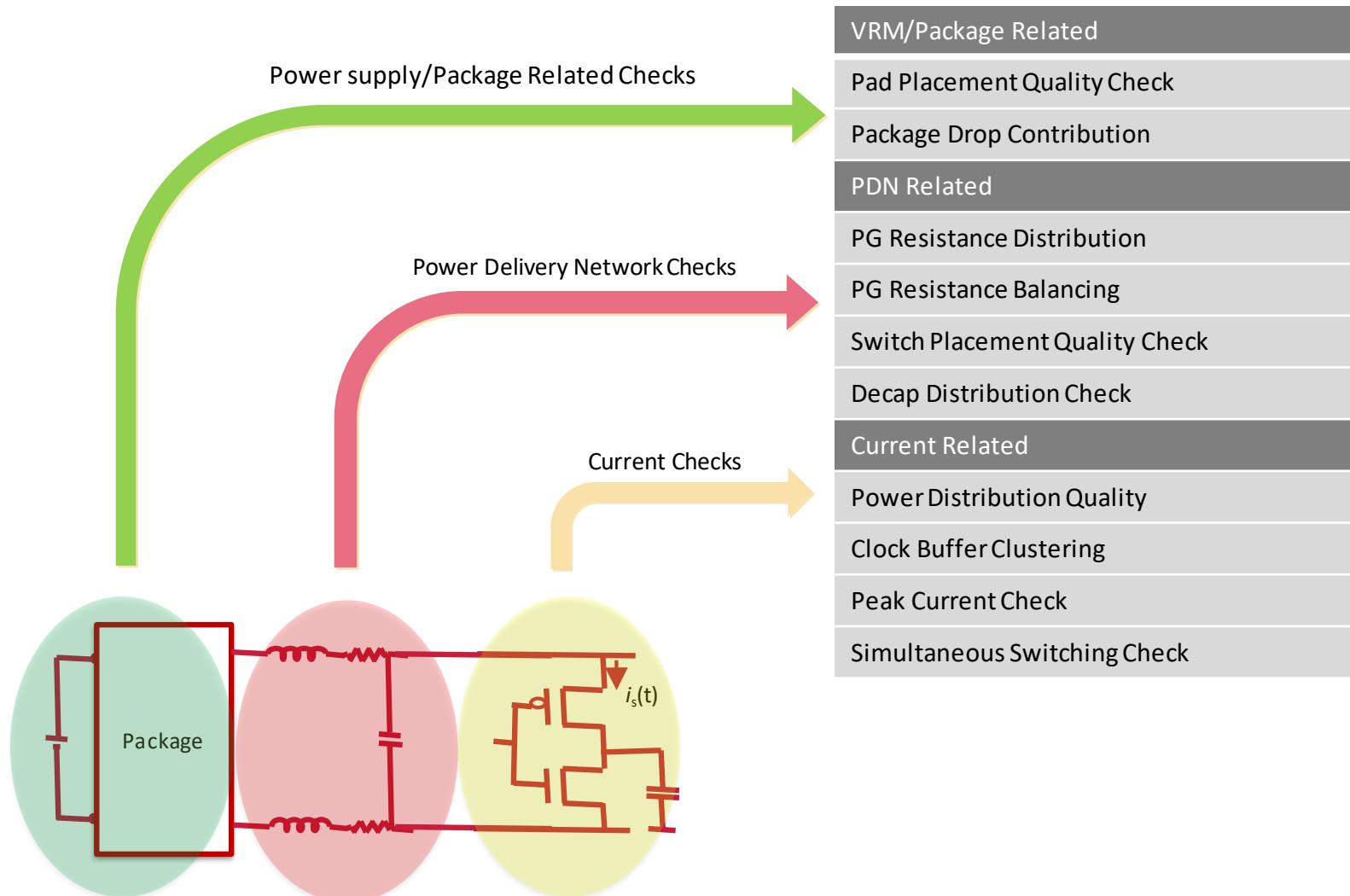
- Performs Checks on GSR/TCL Parameters

GSR ::Parameter	Given Value/Total	Recommended Value/Total	Status
GSR::PUSH_PININST	1	When set to 1 this keyword produces more accurate LEF modeling of power/ground pins	
GSR::DYNAMIC_SIMULATION_TIME	2.575 ns	> 2.56 ns	
GSR::DYNAMIC_TIME_STEP	25 ps	5 ps - 100 ps	
GSR::DYNAMIC_PRESIM_TIME	3 ns	1 ns - 50 ns	
GSR::FREQUENCY	390.0 MHz	≈ 390.62 MHz	
GSR::CACHE_MODE	0	Set it to 1 if memory usage is a concern	
GSR::DYNAMIC_SAVE_WAVEFORM	1	Set it to 0 if disk usage is a concern	
GSR: INPUT_TRANSITION	3e-10	≤ 1ns	
GSR : SPLIT_SPARSE_VIA_ARRAY	-1.0	.	
GSR::TOGGLE_RATE	AVG_CLOCK_TOGGLE_RATE : 0.64 AVG_SIGNAL_TOGGLE_RATE : 0.12	1.0 - 2.0 0.15 - 0.30	 
GSR:VDD_NETS	Total 2 power nets specified in GSR	There are 0 power nets missing in GSR	
GSR:VSS_NETS	Total 1 ground nets specified in GSR	There are 0 ground nets missing in GSR	

NOTE : GSR/TCL check is just an advisory section. There can be several cases where user wants to override the recommended settings displayed above; Purpose of this check is to identify gross issues made by the user like INPUT_TRANSITION keyword set to 100 instead of 100e-12 so that RedHawk interprets the default slew as 100 secs instead of 100ps

Common mistakes made in GSR/TCL are identified here

Overall Design Weakness Exploration



Design Weakness Checks Summary

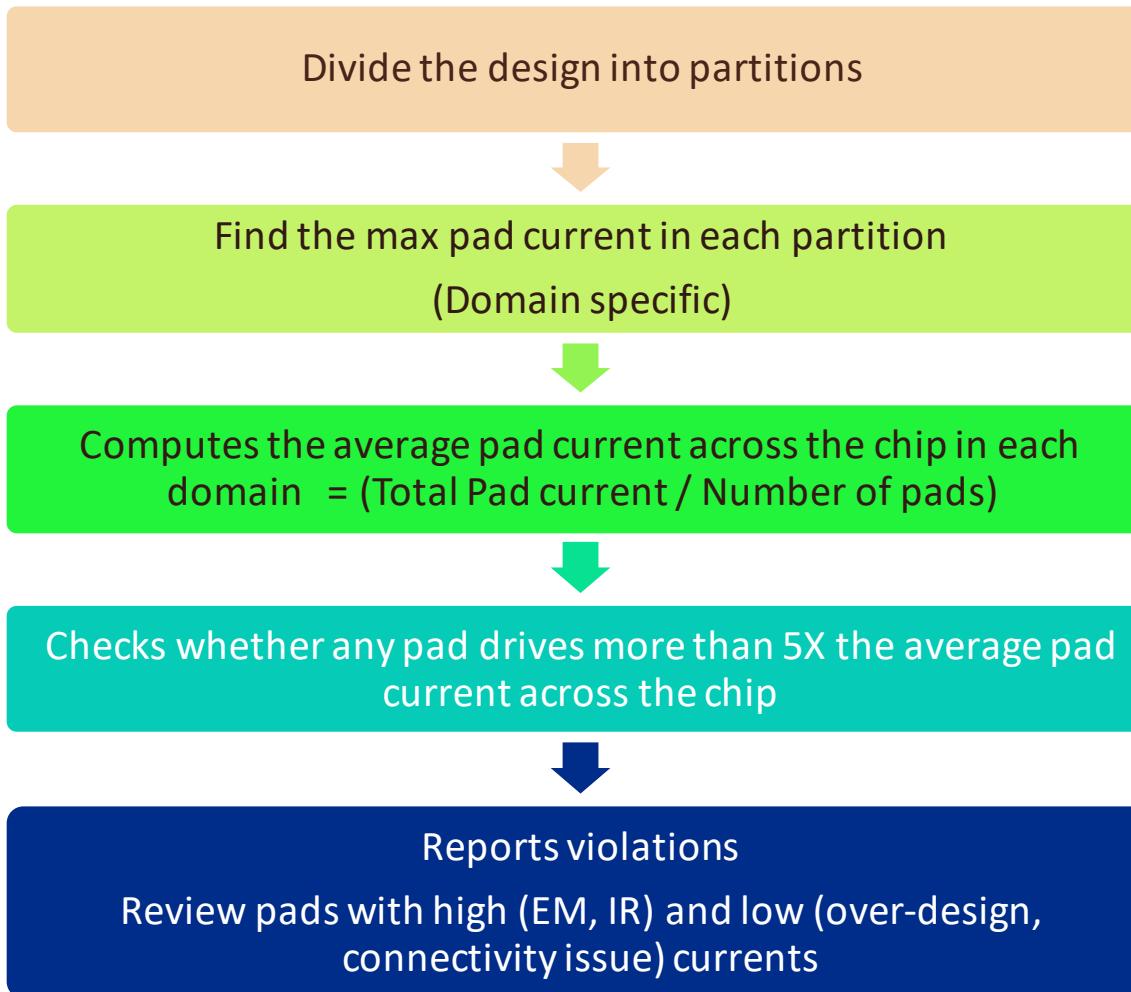
The screenshot shows the RedHawk™-Explorer interface with the 'Design Weakness' tab selected. On the left, a sidebar lists various check categories with their status (e.g., Pad Placement Quality: X, Package Drop Contribution: X). The main area displays a 'Design Weakness Summary' and an 'Analysis Summary' table.

Parameter	Summary Description
<input type="checkbox"/> POWER DISTRIBUTION QUALITY	Percentage of violating regions : 2/329 (0 %)
<input checked="" type="checkbox"/> PAD PLACEMENT QUALITY	Percentage of violating regions : 4/44 (9 %)
<input checked="" type="checkbox"/> PG RESISTANCE DISTRIBUTION	Percentage of violating regions : 42/304 (13 %)
<input checked="" type="checkbox"/> PG RESISTANCE IMBALANCE	Percentage of violating regions : 55/86 (63 %)
<input checked="" type="checkbox"/> PEAK CURRENT DISTRIBUTION	Percentage of violating regions : 4/329 (1 %)
<input checked="" type="checkbox"/> DECAP DISTRIBUTION	Number of Violating Non-Zero Decap Regions : 133/245 (54.0 %) Number of Zero Decap Regions : 417/662 (62 %)
<input type="checkbox"/> PACKAGE DROP CONTRIBUTION	Worst Package Drop For Power Domain : 12.8 mV (1 %) Worst Package Drop For Ground Domain : 16.5 mV (1 %)

Move the mouse pointer above the table rows to highlight the corresponding violation area.

- Ranks Different Regions in the design for Various Design Weakness Parameters
- Identifies Regions Affected with Design Quality Issues

Pad Current Check Example



Pad Current Check

Summary Data Integrity Design Weakness Hotspots Performance

Back Forward 3D-IC FAQ

VRM/Package Checks

- Pad Placement Quality X
- Package Drop Contribution X

PDN Related Checks

- PG Resistance Distribution X
- PG Resistance Imbalance X

Current Related Checks

- Switch Placement Quality ✓
- Decap Distribution X

Design Weakness » Pad Placement Quality Check

Pad Placement Quality Check ?

- Checks whether the Max Pad Current in any region is greater than 3 times Average Pad Current(28.100 mA)
- Number of Regions with Violations : 4/44 (9.09 %)

Top Max Violations

Region	Pad Current Ratio	Details
1	4.87	Details
2	3.66	Details
3	3.55	Details

Issues Highlighted in GUI

RedHawk: GENERIC <@mercury> <2>

File Edit View API Tools Static Dynamic Timing Results Explorer Help

Details

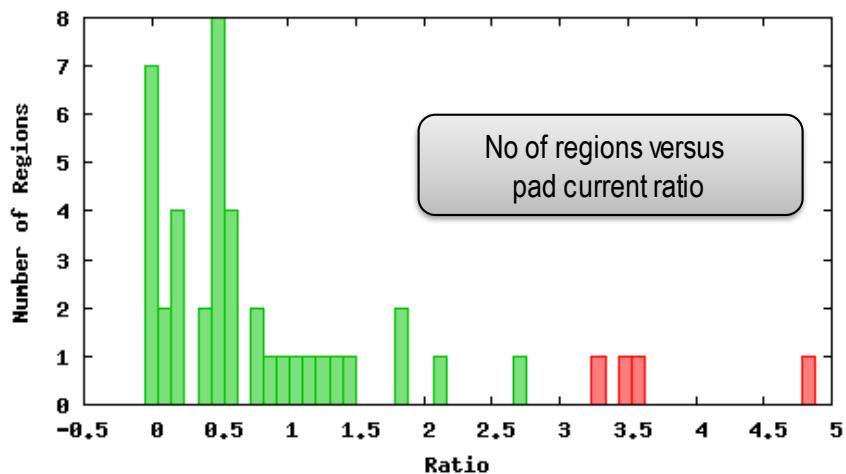
Parameter Value

Region	4815.45 2324.70 4981.50 2490.75
Worst Pad	DVDD14
Worst Pad Location	4905 2438.85
Worst Pad Domain	VDD
Worst Pad Current	1.37e-01 A
Worst Pad Voltage	1.187185 V

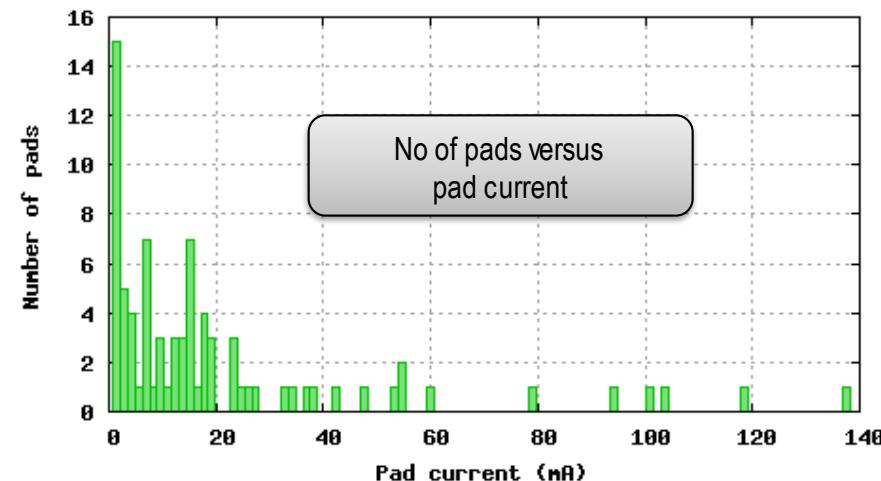
ANSYS

Pad Current Check - Details

Pad Current Distribution Histogram



Pad Current Histogram



Histogram Voltage Drop Domain Based Check Cross Probing

VOLTAGE DOMAIN BASED PAD PLACEMENT QUALITY CHECK

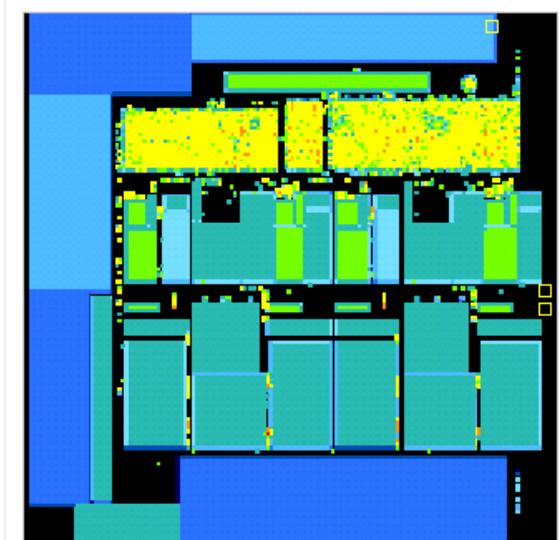
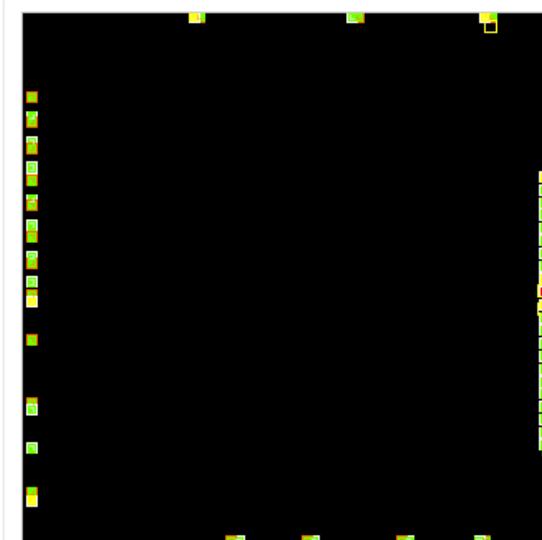
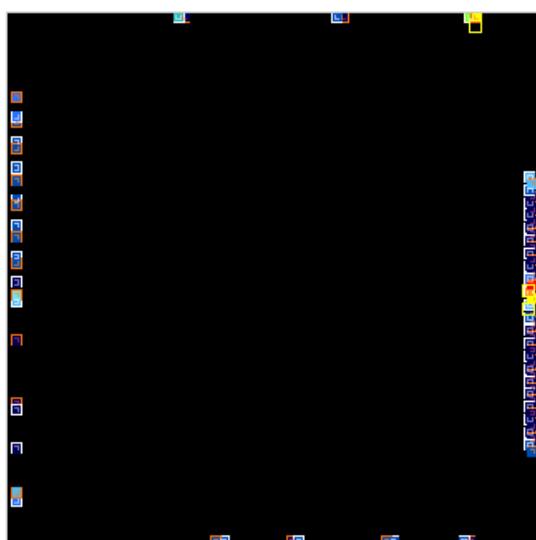
Domain	Avg Pad Current(A)	Max Pad Current(A)	Worst Pad
VDD	0.021129	0.136911	DVDD14
VSS	0.0217236	0.119063	DVSS13

Domain wise details

Pad Current Check - Details

Design Weakness Summary » Pad Placement Quality Check » Related Maps

Design Weakness Summary » Pad Placement Quality Check » Related Maps



Data Integrity » Pad Placement Quality » Related Reports

Related Output Reports

Report	Line Count	Definition
adsRHE/adsDWE/reports/pad.report	80	Provides details of current and voltage of each pad

Click on the hyperlink to view the report

Decap Distribution Check

Summary Data Integrity Design Weakness Hotspots Performance

Back Forward 3D-IC FAQ

VRM/Package Checks

- Pad Placement Quality X
- Package Drop Contribution X

PDN Related Checks

- PG Resistance Distribution X
- PG Resistance Imbalance X
- Switch Placement Quality ✓

Decap Distribution X

Current Related Checks

- Power Distribution Quality X
- Clock Buffer Clustering ✓
- Peak Current X
- Simultaneous Switching ✓

Design Weakness » Decap Distribution Check

Decap Distribution Check ?

- Checks whether more than 70 % of buckets have Apl cap coverage
- Number of Regions with Apl cap coverage : 245/662 (37.0 %)
- Checks whether the Decap Density in any region is less than 1/5 times Average Decap Density
- Number of Regions with Violations : 133/245 (54.28 %)

Top Violations

Region	Decap Density Ratio	Zoom
1	0.0007	
2	0.002	
3	0.0022	
4	0.0026	
5	0.0026	

Issues Highlighted in GUI

BLUE: Regions with zero apl cap coverage
ORANGE: Regions with apl cap coverage less than 1/5 Th Of Overall Chip Apl Cap Coverage

Histogram Decap Efficiency Voltage Drop Decap Report

Decap Distribution Histogram

Number of Regions

Decap distribution histogram

Ratio

Decap Efficiency Check

Histogram Decap Efficiency Voltage Drop Decap Report

DECAP EFFICIENCY CHECK

- Check whether the peak demand current is at least 20% more than the peak battery current is supplied by decaps)

The graph displays two current profiles over time. The red line represents the Demand Current, which shows several sharp peaks. The green line represents the Battery Current, which is relatively smooth and lower in magnitude. The x-axis is labeled 'Time (ps)' and ranges from 0 to 2500. The y-axis is labeled 'Current (A)' and ranges from 0.2 to 1.4.

Histogram Decap Efficiency Voltage Drop Decap Report

DECAP STATISTICS:
Rectangular region: Full chip
80878 out of total 476302 instances in region selected. 395424 ignored.
"Ignored" would include filler cells or cells defined as DECAP_CELLS.

The decap numbers should not be used to as a reference of the capacitance seen in the die during the simulation by themselves or in any combination whatsoever. To get the chip capacitance number (also called Cdie), it is recommended to run the command: "perform powermodel -cdie" to obtain the capacitance and resistance (Cdie and Rdie, respectively) of the die over multiple frequency points using Apache's Chip Power Model technology. Please be advised that the execution of this command will compromise the GUI results and the analysis of the results from the last run performed.

Non-switching Cap, original DevCap and LoadCap during DvD analysis:

Cell Type	NonSwCap (pF)	DevCap (pF)	LoadCap (pF)
Combinational:	1743.752	640.049	2666.374
Sequential:	337.494	477.385	748.005
Clock buffers:	92.140	75.992	302.900
Memory/IP:	0.000	0.000	0.000
Sub-total:	2173.386	1193.426	3717.279
Total PG Cap:	89.632 pF		
Total intentional Cap:	0.000 pF		
Number of decap instances:	221105		

ANSYS

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Simultaneous Switching Check

Summary Data Integrity Design Weakness Hotspots Performance

Back Forward 3D-IC FAQ

VRM/Package Checks

- Pad Placement Quality X
- Package Drop Contribution X

PDN Related Checks

- PG Resistance Distribution X
- PG Resistance Imbalance X
- Switch Placement Quality ✓
- Decap Distribution X

Current Related Checks

- Power Distribution Quality X
- Clock Buffer Clustering ✓
- Peak Current X
- Simultaneous Switching ✓

Design Weakness > Simultaneous Switching Check

Simultaneous Switching Check ?

Switching Activity Demand Current Check Switching Event Clustering

- OVERALL SWITCHING ACTIVITY CHECK
- Checks If Overall Number Of Switching Instances Is Between 10 and 30 % Of Total Number Of Instances

Switching Report

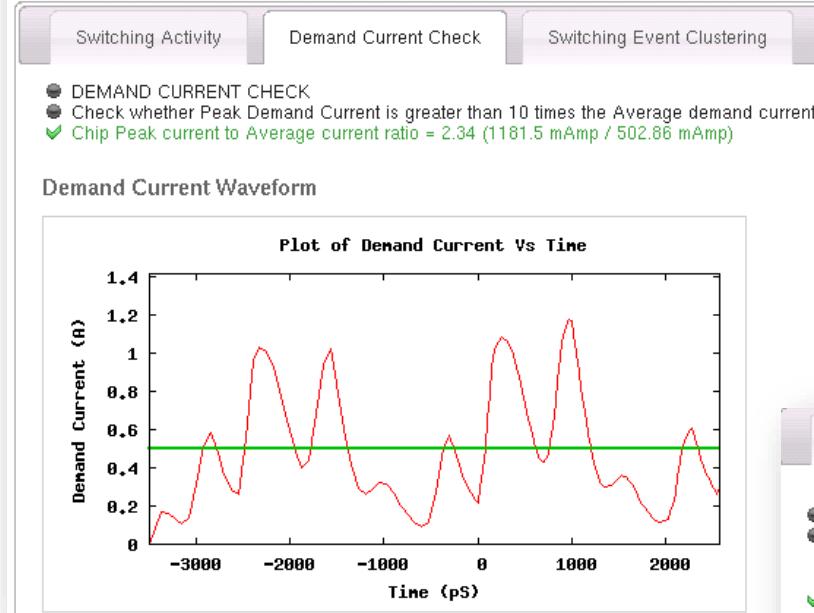
Type	Switching/Total	Switching %
Combinational	6006/57892	10.37%
Sequential	2729/16926	16.12%
Clock	3553/6060	58.63%
Special	0/0	0.00%
Memory/IP	0/0	0.00%
Total	12288/80878	15.19%

✓ Number Of Instances Switching : 12288/80878 (15.19 %)

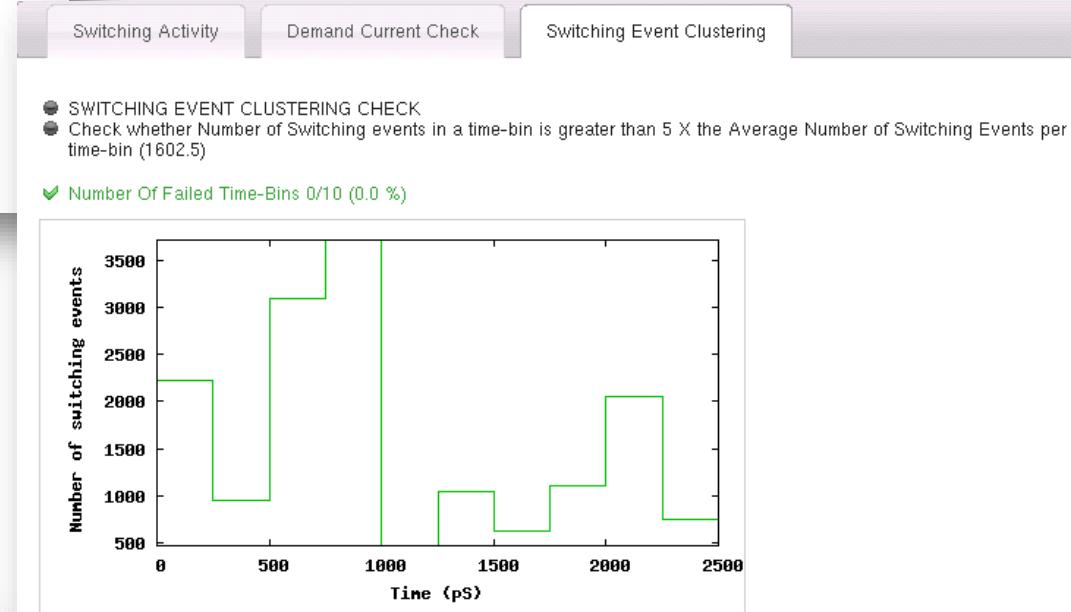
Celltype Based Switching Check
Frequency Domain Based Demand Current Check
Voltage Domain Based Demand Current Check

Simultaneous Switching Check

Simultaneous Switching Check [?](#)



Demand Current Check



Switching Event Clustering Check

Simultaneous Switching Check

Frequency Domain based Demand Current Check

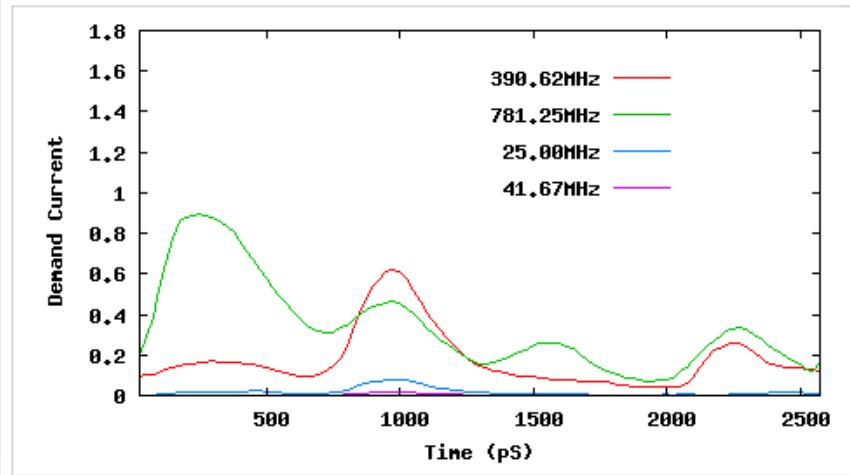
Design Weakness » Simultaneous Switching Check » Frequency Based

Simultaneous Switching Check [?](#)

Frequency Domain Based Demand Current Check

Frequency	Peak Current (mA)	Ratio	Status
25.00MHz	80.6	4	✓
781.25MHz	899.94	2	✓
390.62MHz	621.91	3	✓
41.67MHz	19.33	5	✓

Frequency Domain Based Demand Current Plot

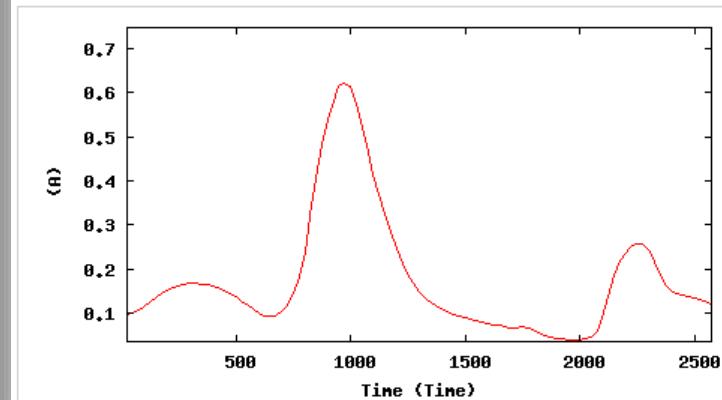


Design Weakness » Simultaneous Switching Check » Simultaneous Switching Check For Frequency inst_129973_VDD_INT

Simultaneous Switching Check [?](#)

- Demand Current Check For freq : 390.62MHz
- Check whether Peak Demand Current for this frequency is greater than 10 times the Average demand current for this frequency
- ✓ Chip Peak current to Average current ratio = 3 (621.91 mA / 177.99 mA)

Demand Current Waveform For Frequency 390.62MHz



Simultaneous Switching Check

Voltage Domain Based Demand Current Check

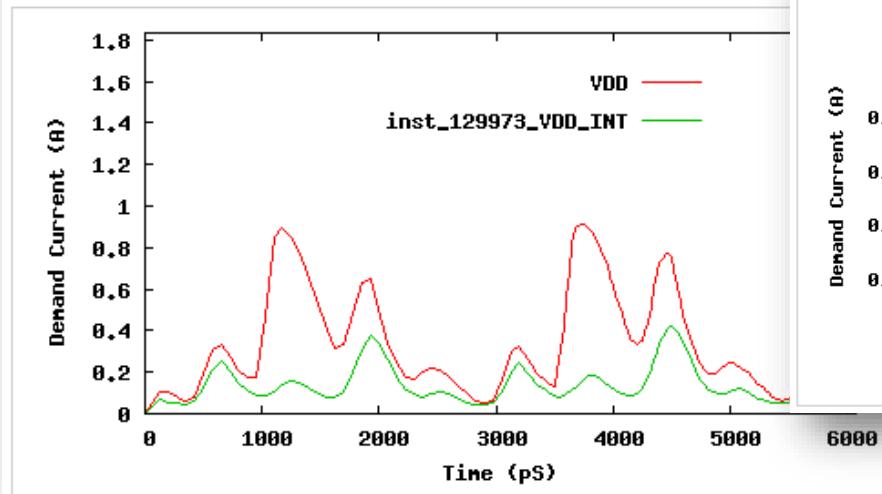
Design Weakness » Simultaneous Switching Check » Domain Based

Simultaneous Switching Check [?](#)

Voltage Domain Based Demand Current Check

Domain	Peak Current (mA)	Ratio	Status
VDD	916.89	2	✓
inst_129973_VDD_INT	418.12	2	✓

Voltage Domain Based Demand Current Plot

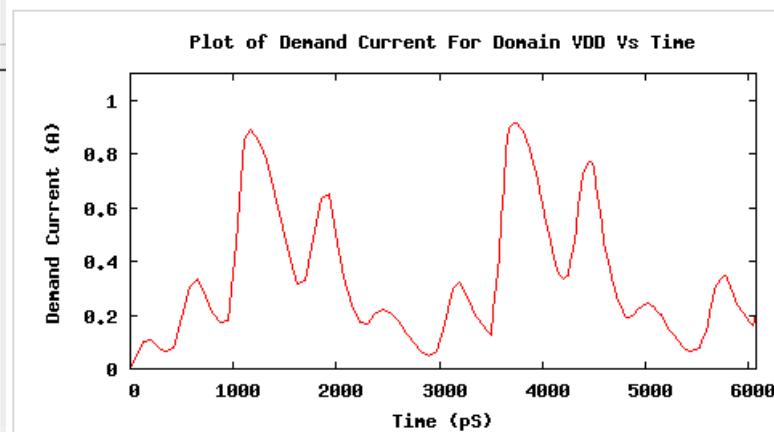


Design Weakness » Simultaneous Switching Check » Simultaneous Switching Check For Domain VDD

Simultaneous Switching Check [?](#)

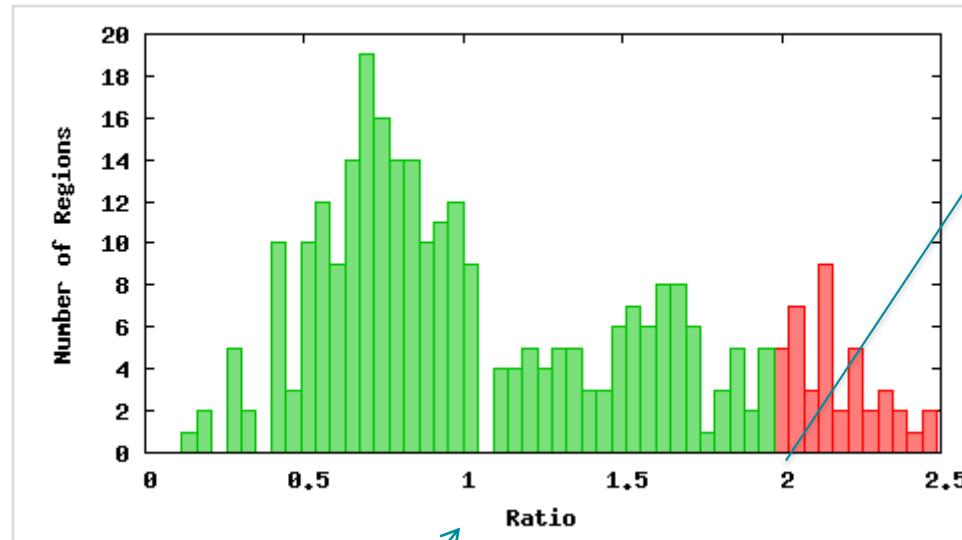
- Demand Current Check For Domain : VDD
- Check whether Peak Demand Current for this domain is greater than 10 times the Average demand current for this domain
- ✓ Chip Peak current to Average current ratio = 2 (916.89 mA / 355.0 mA)

Demand Current Waveform For Domain VDD



Interpreting Histograms in RHE

PG Resistance Distribution Histogram



Simple interpretation:
Ratio 2 means this region is 2X weaker
than other part of the design

How is this ratio computed in this example ?

- STEP-1 : RHE computes the peak resistance for each region (REGION-R)
- STEP-2 : Average resistance across all the regions is computed (AVG-R)
- STEP-3 : PGR Design Weakness Ratio for each region is computed as $\text{REGION-R}/\text{AVG-R}$

Cross-probing Violations in RedHawk GUI

PG Resistance Distribution Check

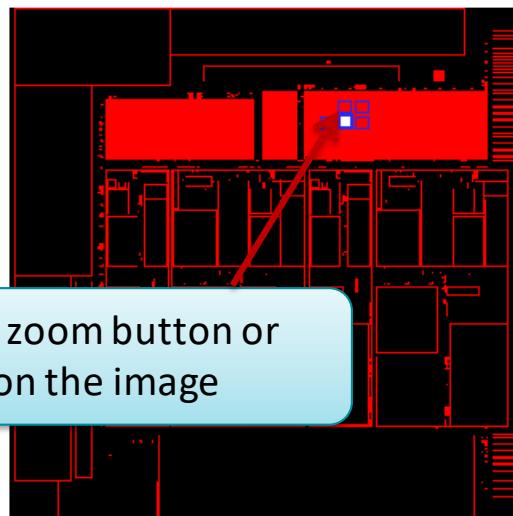
Checks whether the PG Resistance in any region is greater than 2 times Average PG Resistance(24.350 ohm)
Number of Regions with Violations : 42/304 (13.81 %)

Top Violations

Region	PG Resistance Ra	Zoom	Details
1	2.94		Details
2	2.91		Details
3	2.86		Details
4	2.85		Details
5	2.84		Details

Move the mouse pointer to highlight the corner

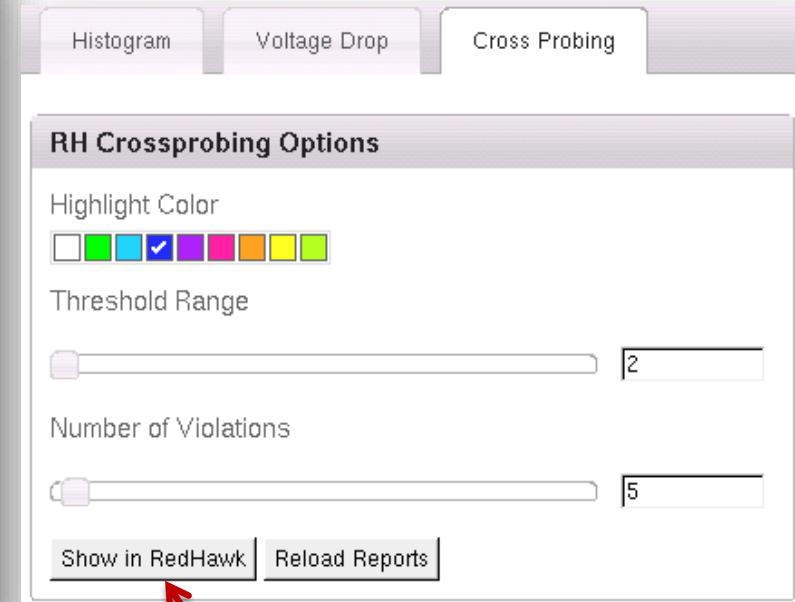
Issues Highlighted in GUI



User can click on zoom button or directly click on the image

When you click on the image, RH/RHE does 3 things:

- Zooms into the violating regions
- Highlights the worst instance within the regions
- Update the map with some relevant views
 - Example, PG resistance map will display SPT for the worst instance



Click on the Show in RedHawk button to view the violations in RH GUI

Hotspot Analysis Summary

Summary Data Integrity Design Weakness **Hotspots** Performance

Back Forward 3D-IC FAQ

Dynamic Voltage Drop Check

Static IR Check X

Power EM Check X

Signal EM Check

RMS

AVG

Peak

Max Cap Check

Memory Check

DVD Check

Static IR Check

Power EM Check

Low Power Check

Voltage & Current w/f

Differential Voltage Check

Noise Coupling Check

Switch Id-sat Check

Switch Off State Check

CPM

GSR/Tcl Settings

Average Current Check

FFT Check

HotSpot Summary

Analysis Summary

Parameter	Summary Description
<input type="checkbox"/> Dynamic Voltage Drop Check	Check Not Performed
<input checked="" type="checkbox"/> Static IR CHECK	Worst Static Drop : 213.19 mV
<input checked="" type="checkbox"/> Power EM CHECK	Worst EM violation : 1523.20 %
<input type="checkbox"/> Low Power CHECK	Check Not Performed

Move the mouse pointer above the table rows to highlight the corresponding Hotspots

Violation Areas



DVD Check : Summary

RedHawk™-Explorer

Summary Data Integrity Design Weakness Hotspots Performance

Back Forward 3D-IC FAQ

Dynamic Voltage Drop Check X

Static IR Check

Power EM Check X

Signal EM Check

RMS

Avg

Peak

Max Cap Check

Memory Check

DVD Check

Static IR Check

Power EM Check

Low Power Check

Voltage & Current w/f

Differential Voltage Check

Noise Coupling Check

Switch Id-sat Check

Switch Off State Check

CPM

GSR/Tcl Settings

Hot Spot Summary » DvD Check

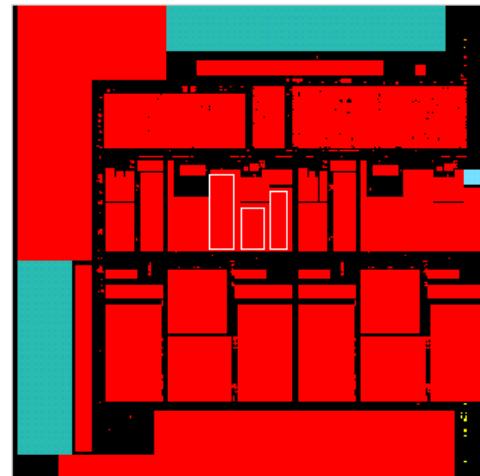
DvD Check ?

- Dynamic Hot Spot Exploration
- Analysis Type : minWC
- Highlighting Top 3 DVD Hot spots in the design
- DVD Threshold used for PASS/FAIL : 100 mV

● Number of failing regions : 287/304 (94.4 %)
● Number of failing instances : 75489/75618 (99.8294 %)

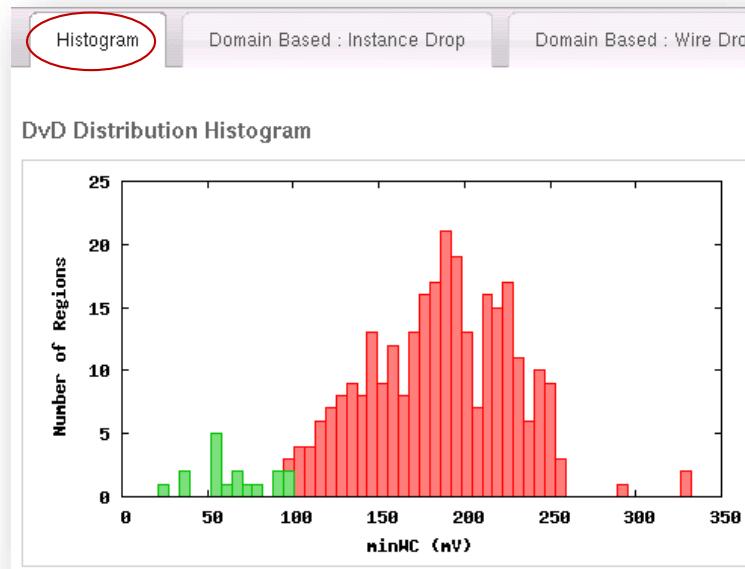
Top Violations

Region	Drop (mV)	Failed Instances	Status
Q Hot Spot : 1	335.01 (27.92 %)	1/1 (100.0 %)	X
Q Hot Spot : 2	333.64 (27.80 %)	1/1 (100.0 %)	X
Q Hot Spot : 3	298.09 (24.84 %)	1/1 (100.0 %)	X



Show in RedHawk »

DVD Check : Summary



Histogram Domain Based : Instance Drop Domain Based : Wire Drop CrossProbing

RH Crossprobing Options

Highlight Color

Dynamic Voltage Drop Limit (mV) 100

Number of Violations 3

Show in RedHawk

Histogram Domain Based : Instance Drop Domain Based : Wire Drop

Voltage Domain Based Hot spot Exploration

Domain	Failed Instances	Max Drop in mV(%)	Status	
inst_129973/VDD_	37771/37771	237.22 (19.77 %)	✗	
VDD	37718/37847	335.01 (27.92 %)	✗	

Histogram Domain Based : Instance Drop Domain Based : Wire Drop

Voltage Domain Based Hot spot Exploration

Domain	Max Drop
VDD	178.337 mV
inst_129973/VDD_	125.095 mV

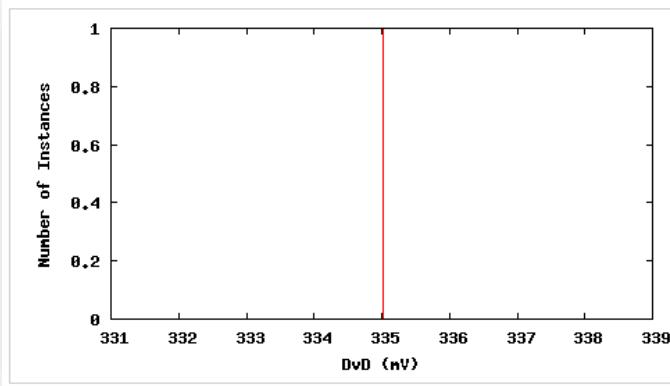
DVD Check

Checking Hot-spot #1

Top Violations

Region	Drop (mV)	Failed Instances	Status
Hot Spot : 1	335.01 (27.92 %)	1/1 (100.0 %)	✗
Hot check - 1	333.64 (27.80 %)	1/1 (100.0 %)	✗
Hot spot : 3	298.09 (24.84 %)	1/1 (100.0 %)	✗

Dynamic Drop Histogram inside Region : 1



Instance level histogram
within hot-spot 1

Hot Spot Summary » DvD Check » Hotspot : 1

DvD Check

- Dynamic Hot Spot Exploration inside HOT SPOT : 1
- Hot spot region : 2304.64 2482.54 2592.46 2963.24
- Region id : 1281
- Instance Threshold used for PASS/FAIL : 100 mV

- Number of instances failing : 1/1 (100.0 %)
Displaying Top 1 instances inside this HOT SPOT

Instance	DROP (mV)	Status
Hot Instance : 1	335.01 (27.92 %)	✗

HotSpot Map

DVD HOTSPOT MAP



Detailed analysis inside the
region

Root Cause Identification

Design Weakness Analysis

Root Cause : Design Weakness

Root Cause : Data Integrity

Histogram

Root Cause : Design Weakness

Check	Status	Value	Ratio	Rank
POWER DISTRIBUTION QUALITY	✓	Total Power = 0.009012 W	1.10	108/662
PAD PLACEMENT QUALITY	✓	Current from nearest pad of Domain VSS : -14.35 mA Current from nearest pad of Domain VDD : 6.92 mA	NA	NA
CLOCK BUFFER CLUSTERING CHECK	NA	NA	NA	NA
PG RESISTANCE DISTRIBUTION	✓	Max Instance Resistance = 1.00 Ohm	1.00	160/662
PG RESISTANCE IMBALANCE	NA	NA	NA	NA
PEAK CURRENT DISTRIBUTION	✓	Total Peak Current = 46.38 mA	0.59	144/662
DECAP DISTRIBUTION	✗	Total Decap = 0.00 pF	0.00	35/662
PACKAGE DROP CONTRIBUTION	✓	Package Drop in Domain VSS : 10 mV (0 %) Package Drop in Domain VDD : 10 mV (0 %)	NA	NA
SIMULTANEOUS_SWITCHING_CHECK *	✓	Overall Switching Activity = 12288/80878 (15.19 %) Peak current/Average Current Ratio = 1181.5 mA/502.86 mA(2.34)	NA	NA

* These checks are not for this hot bucket but they belong to the entire design

There are no decaps in this region

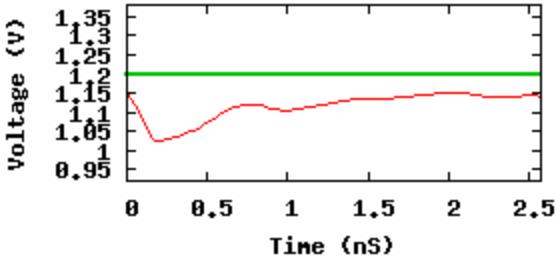
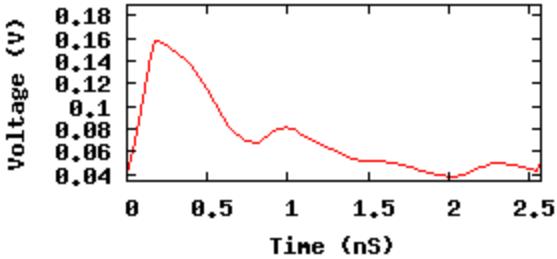
DvD Check

Instance Level Debug

Hot Spot Summary » DvD Check » Hotspot : 1 » Hot Instance : 1

DvD Check

- Dynamic Hot Spot Exploration for Hot Instance : 1
- Instance : inst_129422/inst_7778
- Instance Pin Threshold used for PASS/FAIL : 50.0 mV
- Pin Based Voltage Drop Details

Pin	Domain	Drop (mV)	Status	Pin DVD Waveform
VDD	VDD 	177.0 (14.75 %)	Fail	<p>Plot for pin VDD</p>  <p>This plot shows the voltage drop over time for the VDD pin. The y-axis is labeled 'Voltage (V)' and ranges from 0.95 to 1.35. The x-axis is labeled 'Time (nS)' and ranges from 0 to 2.5. A horizontal green line represents the threshold at 1.2V. The red waveform starts at approximately 1.2V, drops to about 1.05V at 0.2nS, and then fluctuates between 1.1V and 1.2V.</p>
VSS	VSS 	158.0 (13.16 %)	Fail	<p>Plot for pin VSS</p>  <p>This plot shows the voltage drop over time for the VSS pin. The y-axis is labeled 'Voltage (V)' and ranges from 0.04 to 0.18. The x-axis is labeled 'Time (nS)' and ranges from 0 to 2.5. The red waveform starts at 0V, rises to a peak of about 0.16V at 0.2nS, and then gradually declines to around 0.04V by 2.5nS.</p>

Pin based voltage drop details
of the hot instance

DVD Check

Instance Level Debug

The image shows three overlapping windows from a software interface for 'cell_28'.

Properties Window:

Cellname	cell_28
Peak Current	VDD 46378.0 uA VSS 46378.0 uA
Decap	0 pF
Frequency	7.8125e+08 Hz
Fanout	72
Load	0.328 pF
Switching Status	Switching
Average Power	0.00901237 W
Leakage Power	0 W
Toggle Rate	1.00575
Gridcheck Resistance	VDD Resistance : 9.68153 Ohm VSS Resistance : 9.73051 Ohm

Data Integrity Window:

Data	Status
ApI Current	✗
ApI Cap	✗
ApI Pwcap	NA
Lef	✓
Lib	✗
Sta	✓
Specf	✗
Gds2def	✗

Design Weakness Window:

Check	Status	Value	Rank
Peak Current	✗	46378.0 uA	1/1
Resistance	✗	19.412 Ohm	1/1
Power	✗	0.00901237 W	1/1
Load	✗	0.328 pF	1/1

DVD Check

Instance Level Debug: SPT and Resistance Report

The screenshot shows the DVDCheck software interface. At the top, there are tabs: Properties, Data Integrity, Design Weakness, Path Tracing, and Resistance Report. The Resistance Report tab is highlighted with a blue oval. A large blue arrow points from the 'Path Tracing' tab to a callout box. Another blue arrow points from the 'Resistance Report' tab to a table below.

SPT Map: A red heatmap showing the shortest resistance path from power/ground pads to internal nodes. A green box highlights a specific area on the map.

Callout Box: Highlights Shortest Resistance Path to P/G Pads

Path Tracing Results:

- Instance: inst_129422/inst_7778
Pin VDD
Resistance : 9.68153 Ohm
Net: VDD
- Instance: inst_129422/inst_7778
Pin VSS
Resistance : 9.73051 Ohm
Net: VSS

Resistance Report Table:

Point	Resistance	Length (um)	Drop (mV)	Zoom
DVDD14	--	--	12.815	
METAL4	0.010	3.46	0.892	
via4Array_23_26x21_67108863_2228496	0.000	--	0.063	
METAL5	0.007	6.26	0.403	
via5Array_11_10x11_1023_1023_1	0.000	--	0.016	

Equivalent Tcl Command:

`perform min_res_path -o res_path.rpt`

User can directly zoom into the bottleneck segments

Power EM Check : Summary

Summary Data Integrity Design Weakness Hotspots Performance

Back Forward 3D-IC FAQ

Dynamic Voltage Drop Check X

Static IR Check

Power EM Check X

Signal EM Check

RMS

AVG

Peak

Max Cap Check

Memory Check

DVD Check

Static IR Check

Power EM Check

Low Power Check

Voltage & Current w/f

Hot Spot Summary » Power EM Check

Power EM Check ②

- Power EM Hot Spot Exploration
- Highlighting Top 3 Power EM Hot Spots in the design
- Power Em Threshold used for PASS/FAIL : 100 %

② Number of failing regions : 127/127 (100.0 %)
② Number of failing nodes : 1000/1287283 (0.0 %)

Top Violations

Region	EM Percentage	Failed nodes	Status
Hot Spot : 1	5810.26	2/2	X
Hot Spot : 2	5619.98	2/2	X
Hot Spot : 3	2752.38	4/4	X

EM Distribution Histogram CrossProbing Domain Based

Power EM Distribution Histogram

Number of Nodes

Power EM (%)

800
700
600
500
400
300
200
100
0

8 1000 2000 3000 4000 5000 6000

Voltage Domain Based EM Hot spot Exploration

Domain	Failed Nodes	Max Em Percentage	Status
VDD	497/497	1189.4	X
VSS	498/498	5810.26	X
inst_129973/VDD_INT	5/5	203.238	X

ANSYS

Power EM Check

Checking Hot-spot#1

Hot Spot Summary » Power EM Check » Hotspot : 1

Power EM Check [?](#)

- Power EM Hot Spot Exploration inside HOT SPOT : 1
- Hot spot region : 3985.200000 1660.500000 4151.250000 1826.550000
- EM Threshold used for PASS/FAIL : 100 %

✖ Number of nodes failing : 2/2 (100.00 %)

- Displaying Top 1 nodes inside this HOT SPOT

Node	EM Percentage	Status
Q Hot Node : 1	5810.26	✖

Hot Spot Summary » Power EM Check » Hotspot : 1 » Hot Node :

Power EM Check [?](#)

- PowerEM Hot Spot Exploration for Hot node : 1
- Node : node1

WIRE/VIA PROPERTIES

Location	4.146085e+03,1.824885e+0
Em percentage	5810.26 %
Layer	METAL4
Node Type	WIRE
Net	VSS
Width	2.000000e+00 um

HotSpot Map Zoomed View PD IPM

EM HOTSPOT MAP ZOOMED

Show in RedHawk »

Thank You!!!