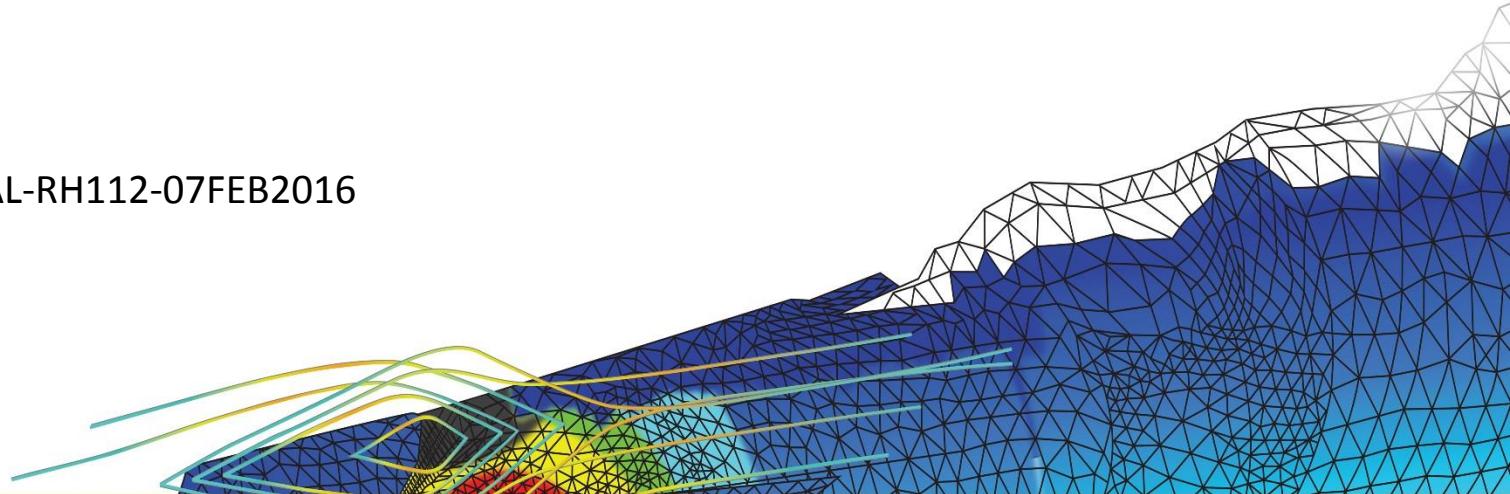




Average Power Calculation & Static Analysis

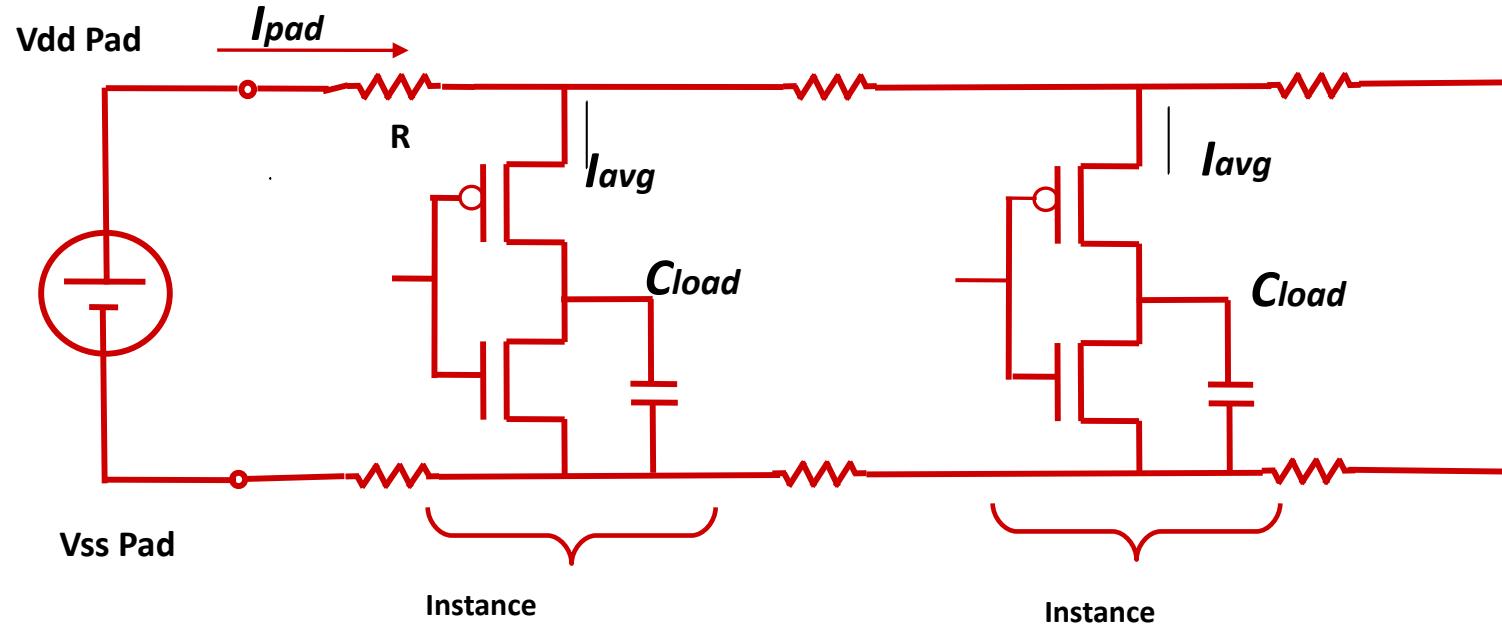
VERSION: V5.2-AL-RH112-07FEB2016



Agenda

- **Static Analysis Theory**
- **RedHawk Static IR/EM Analysis Flow**
- **Analysis of Results**
- **Conclusions**

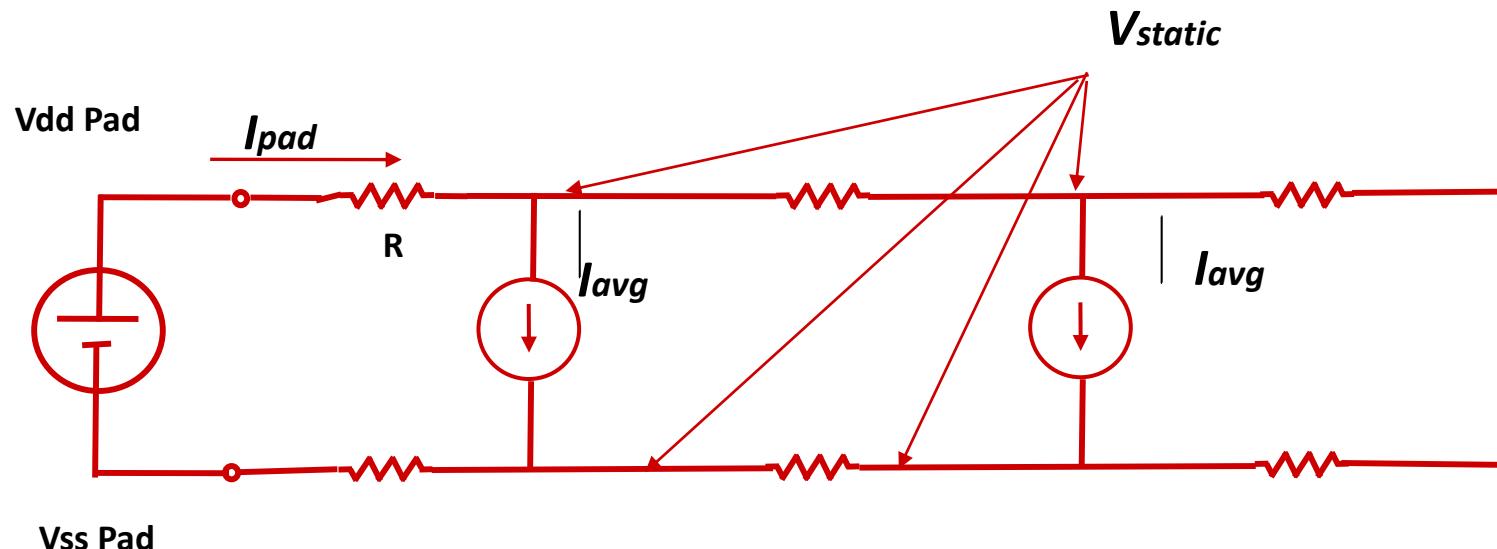
Static Voltage Drop Background



- On-chip power/ground network → mesh of resistors
- Instances → DC current sources

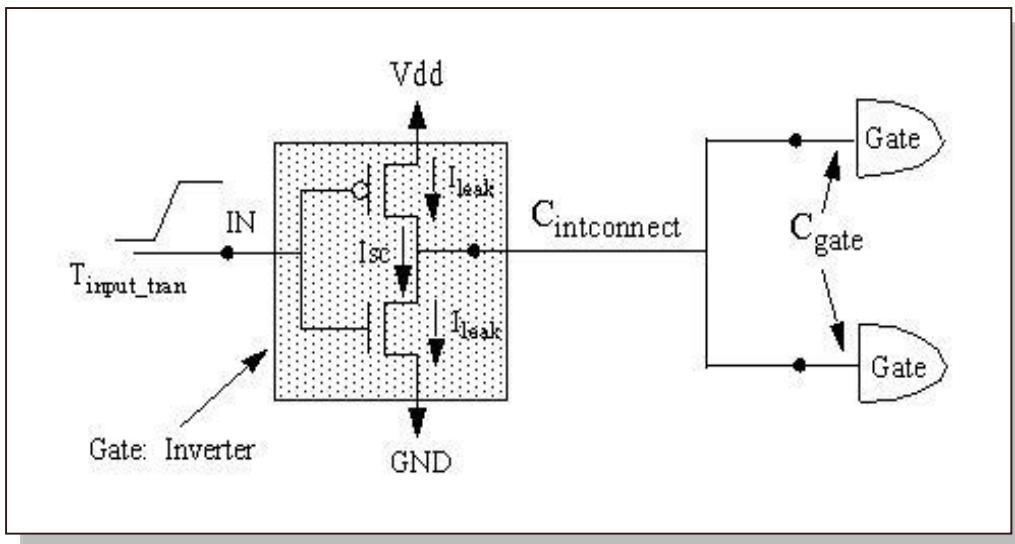
Static Voltage Drop on P/G Network

- Average current is calculated for each instance
- V_{static} is computed at every node (Ohm's law ...)
- Wire / via electromigration (EM) is post-processed from static current density



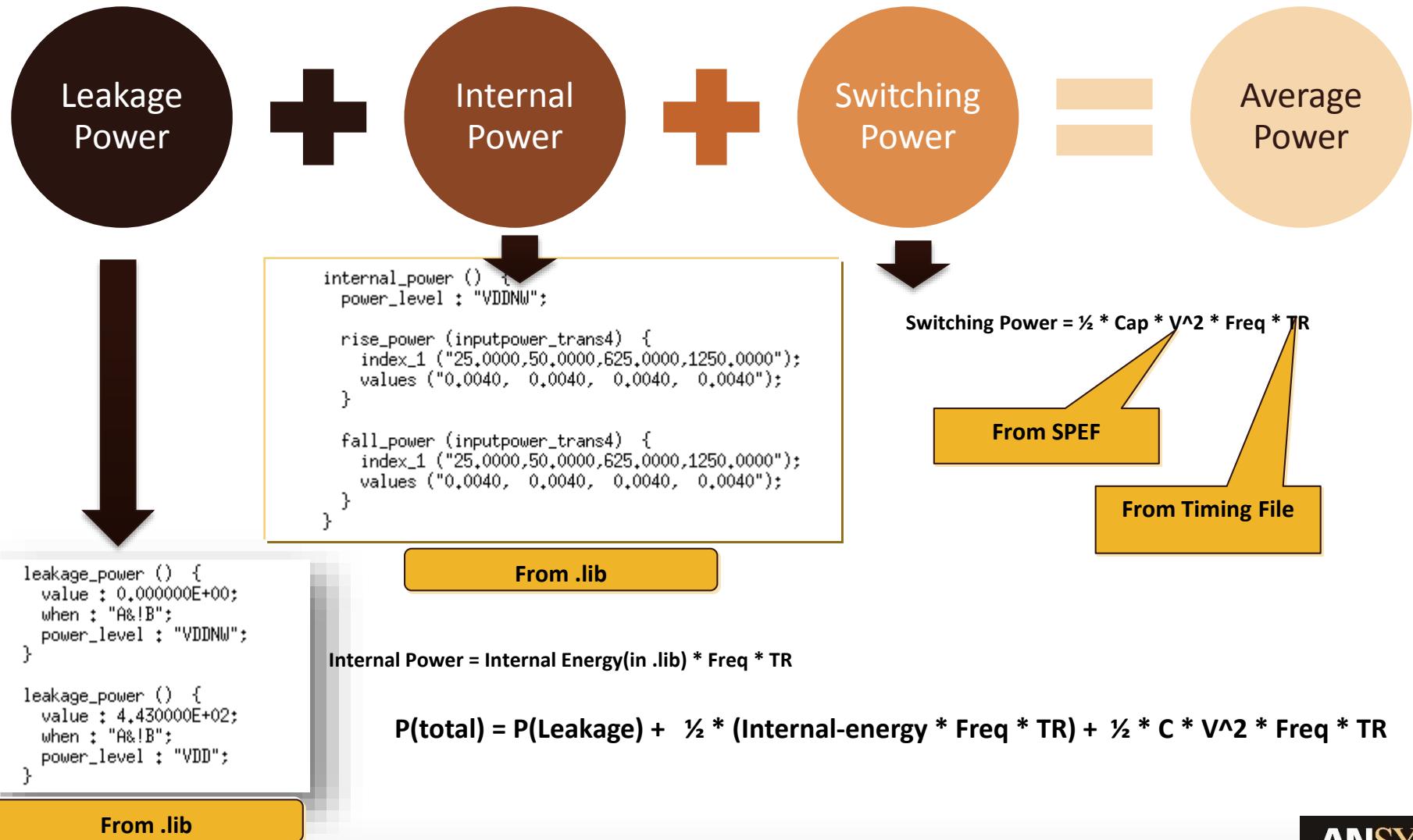
Gate-level Static Power and DC Current

$$P_{avg} = P_{leakage} + P_{internal} + P_{switching}$$



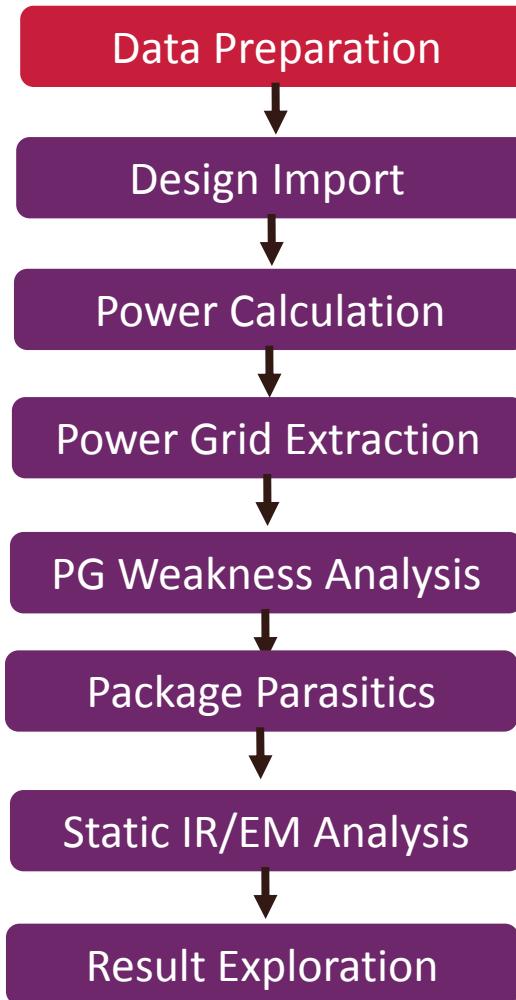
Gate Active Average Power is
➤ function of input slew, output load (.lib power tables)
➤ linearly proportional to frequency and toggle rate

Gate-level Average Power Calculation



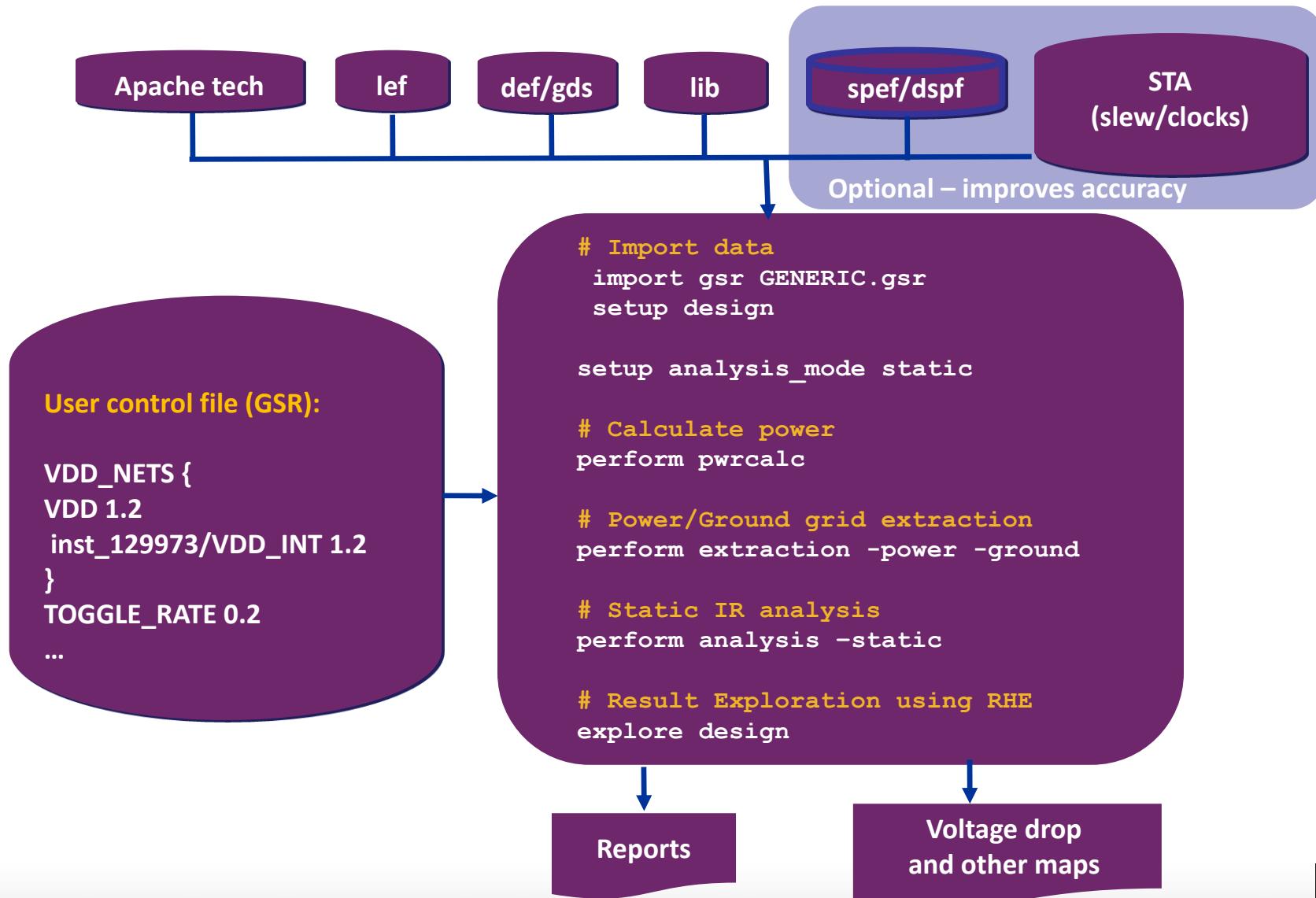
REDHAWK STATIC IR/EM ANALYSIS FLOW

Data Preparation

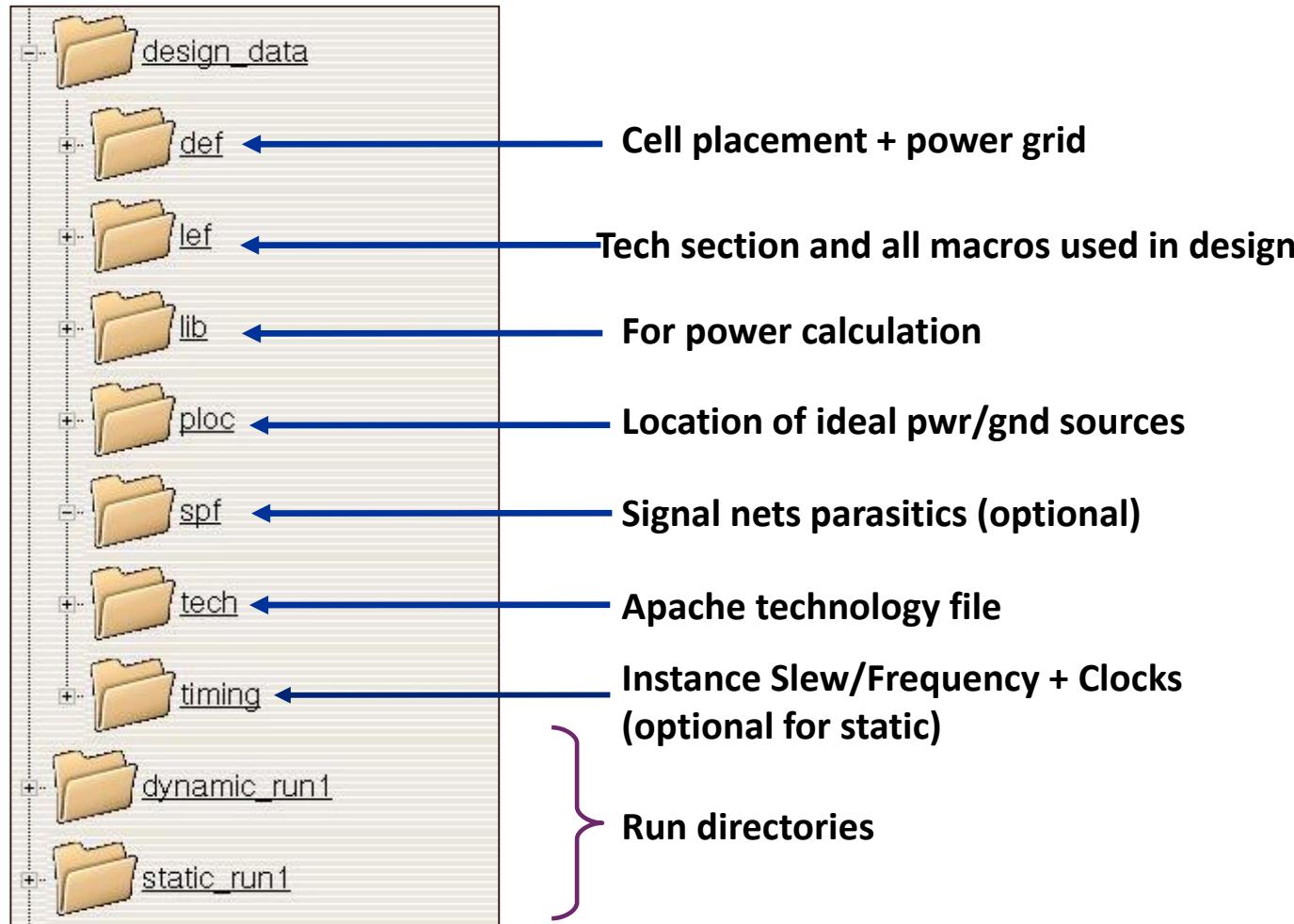


- **Copying the training tarball**
- **Creating GSR and run command file**
- **Setting up the environment**
- **Reviewing the user inputs**

Static Analysis Flow and Required Data



Recommended Directory Structure



Setting Up The Training Testcase

- `cp -R <original_path>/GENERIC_tutorial.tar.gz`
- `tar -xvzf GENERIC_tutorial.tar.gz`
- Follow the instructions in README to run static analysis

Step 1: Data Preparation

- `cd GENERIC_tutorial/static_run`
- Review the GSR and Command File
- `source setup.csh` : This will set APACHEROOT, PATH and LM_LICENSE_FILE.

GSR File Overview

```
TECH_FILE ads.tech
```

```
LIB_FILES {  
<path to lib file>  
<path to lib directory> (all *.lib files in dir)  
<path to custom lib file> custom  
}
```

```
LEF_FILES {  
<lef file path>/name1.lef << tech definition  
<lef file path>/name2.lef  
}
```

```
DEF_FILES {  
<def file path>/name1.def  
<def file path>/name2.def TOP < last one to be TOP DEF  
}
```

OR

```
LIB_FILES {  
<design>.libs  
}
```

OR

```
LEF_FILES {  
<design>.lefs  
}
```

OR

```
DEF_FILES {  
<design>.defs  
}
```

Static Run Command File

```
# Import data
import gsr GENERIC.gsr
setup design
setup analysis_mode static

# Calculate power
perform pwrcalc

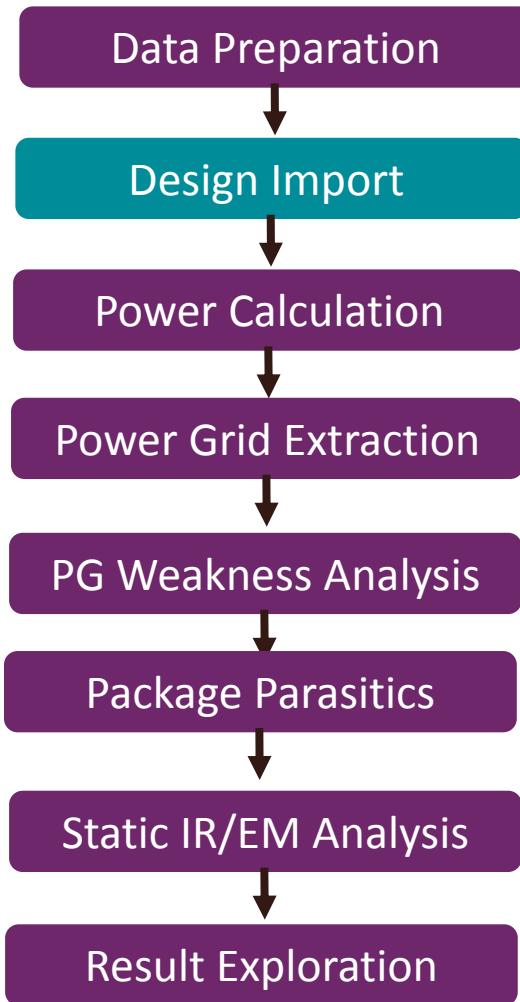
# Power/Ground grid extraction
perform extraction -power -ground

# Lumped resistance (in Ohms)
# for package, wirebond and pads
setup package -power -r 0.005 -l 2.5 -c 5
setup package -ground -r 0.005 -l 2.5 -c 5
setup wirebond -power -r 0.01 -l 2.2 -c 1.42
setup wirebond -ground -r 0.05 -l 1.7 -c 0.2
setup pad -power -r 0.001
setup pad -ground -r 0.001

# Static IR analysis
perform analysis -static

# Result Exploration using RHE
explore design
```

Step 2: Importing the Design



```
# Import data
import gsr GENERIC.gsr
setup design

setup analysis_mode static

# Calculate power
perform pwrcalc

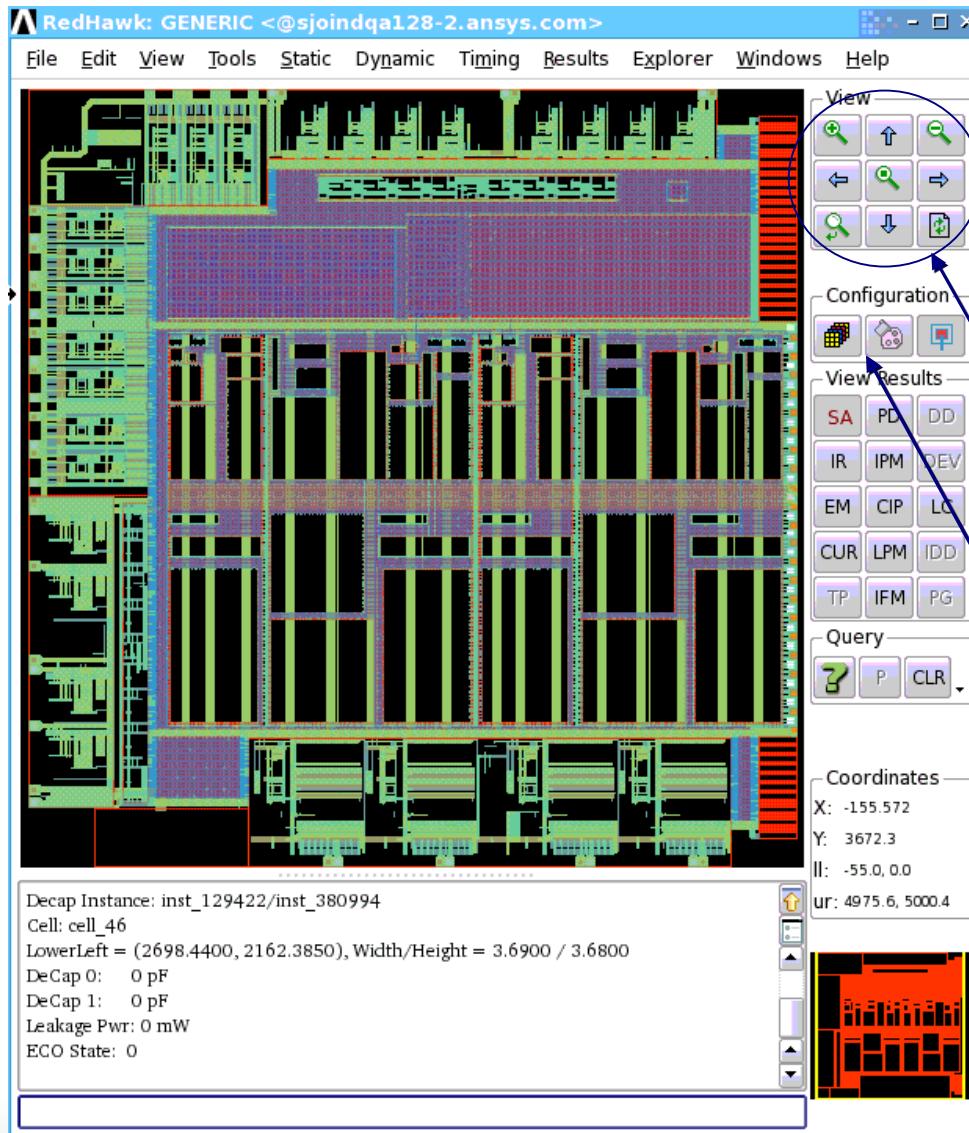
# Power/Ground grid extraction
perform extraction -power -ground

# Lumped resistance (in Ohms)
# for package, wirebond and pads
setup package -power -r 0.005 -l 2.5 -c 5
setup package -ground -r 0.005 -l 2.5 -c 5
setup wirebond -power -r 0.01 -l 2.2 -c 1.42
setup wirebond -ground -r 0.05 -l 1.7 -c 0.2
setup pad -power -r 0.001
setup pad -ground -r 0.001

# Static IR analysis
perform analysis -static

# Result Exploration using RHE
explore design
```

Starting RedHawk and Setting Up the Design



- Start RedHawk
- Execute commands:
`import gsr GENERIC.gsr`
`setup design`
- Zoom in/out/scroll
 - Drag Right mouse button (Zoom in)
- Layer dialog box
 - Turn on/off Layer/Instance
 - Fill/Outline

Tech File Viewer

RedHawk: GENERIC <@sjoindqa128-2.ansys.com>

File Edit View Tools Static Dynamic Timing Results Explorer Windows Help

Chip Layout Map
Nets
Connectivity
Technology Layers
Hierarchy Level
EM Mode
Map Configuration
Power Maps
Resistance Maps
Voltage Drop Maps
Current Maps
Electromigration Map
Transistor Pin Maps
Dynamic Instance DVD
Decap Maps
ESD Resistance Lists
ESD Clamp Lists
ESD Resistance Maps
ESD Current Density
Impact on Timing Maps
Clock Jitter Maps (PJX)
Clock Jitter Maps
STA Critical Path

Decap Instance: inst_129422/inst_380994
Cell: cell_46
LowerLeft = (2698.4400, 2162.3850), Width/Height = 3.6900 / 3.6800

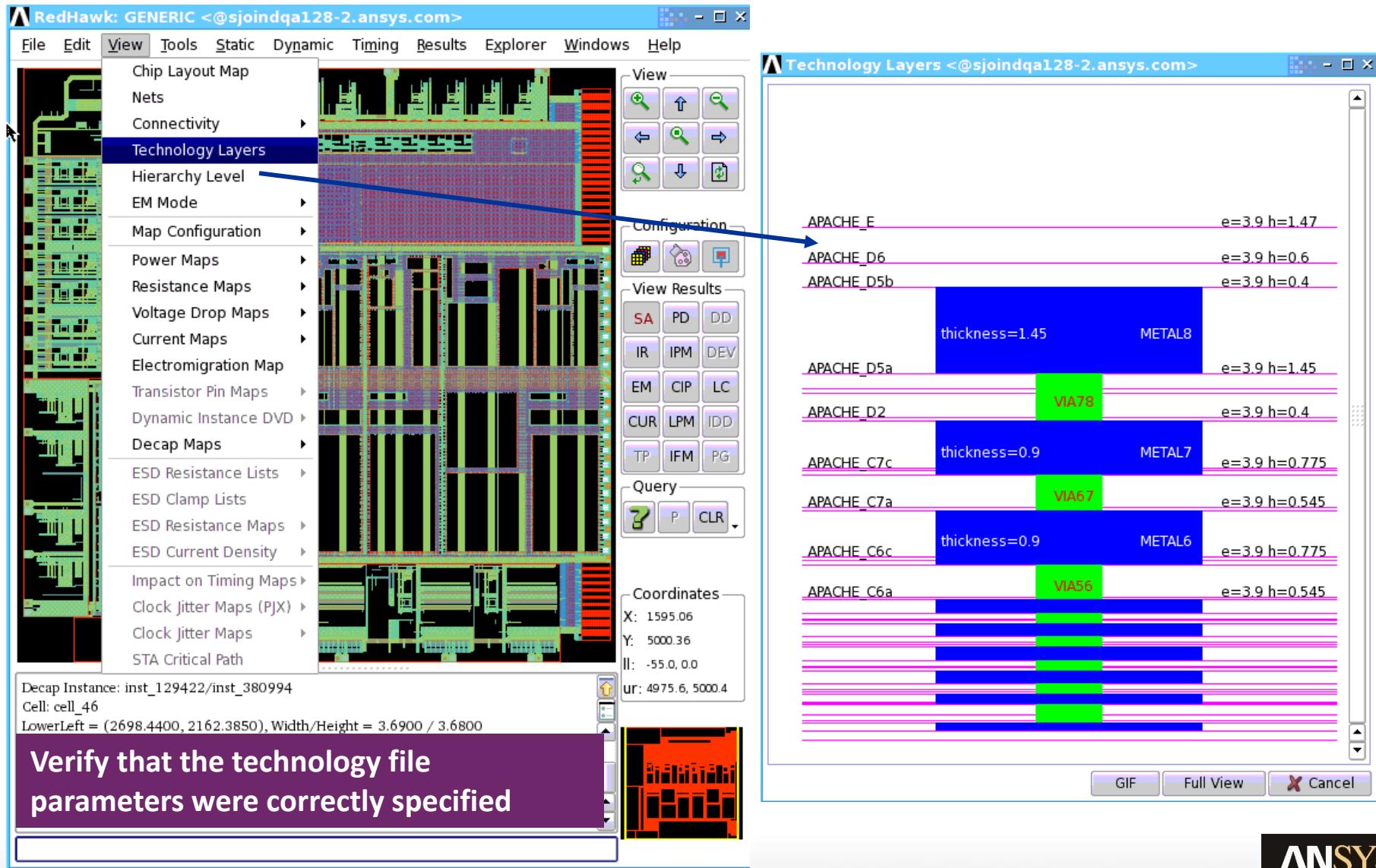
View
Configuration
View Results
Query
Coordinates
X: 1595.06
Y: 5000.36
II: -55.0, 0.0
ur: 4975.6, 5000.4

Technology Layers <@sjoindqa128-2.ansys.com>

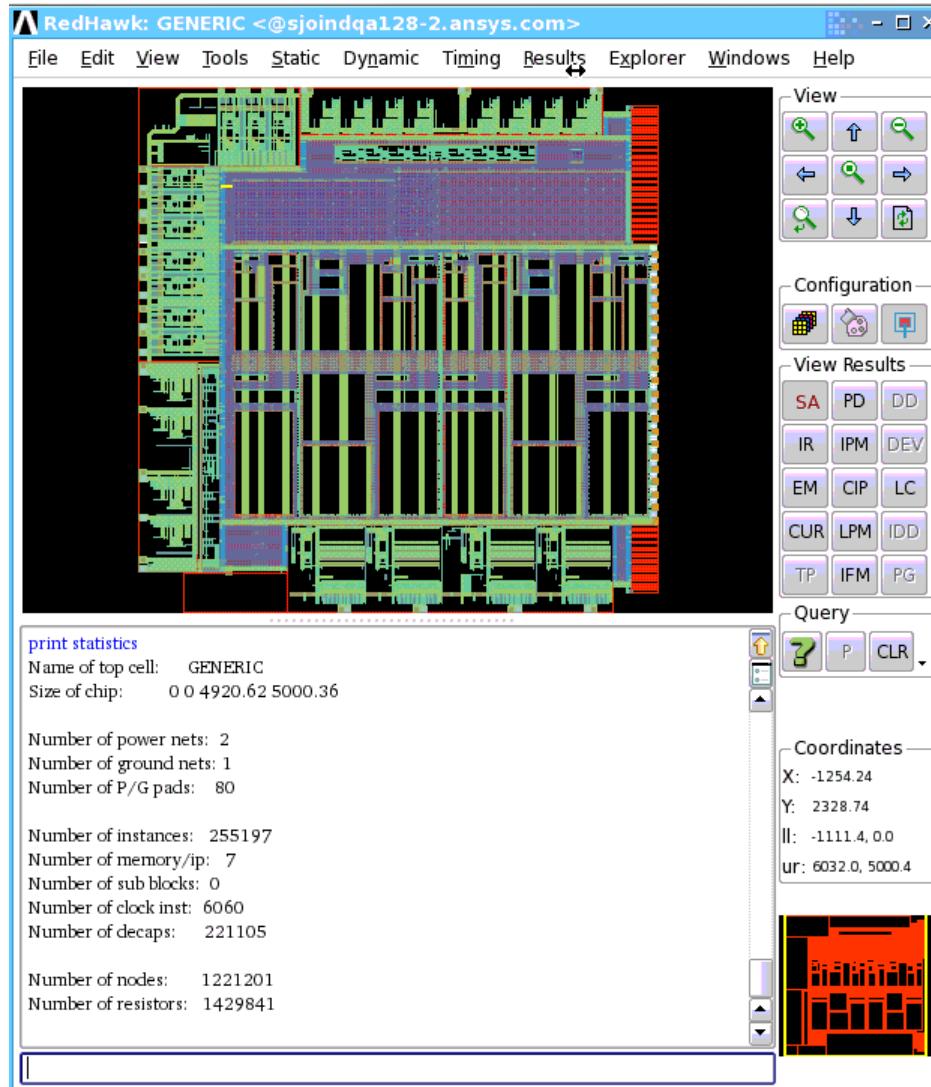
APACHE_E e=3.9 h=1.47
APACHE_D6 e=3.9 h=0.6
APACHE_D5b e=3.9 h=0.4
APACHE_D5a thickness=1.45 METAL8 e=3.9 h=1.45
APACHE_D2 VIA78 e=3.9 h=0.4
APACHE_C7c thickness=0.9 METAL7 e=3.9 h=0.775
APACHE_C7a VIA67 e=3.9 h=0.545
APACHE_C6c thickness=0.9 METAL6 e=3.9 h=0.775
APACHE_C6a VIA55 e=3.9 h=0.545

GIF Full View Cancel

Verify that the technology file parameters were correctly specified



Design Information



TCL query: *print statistics*

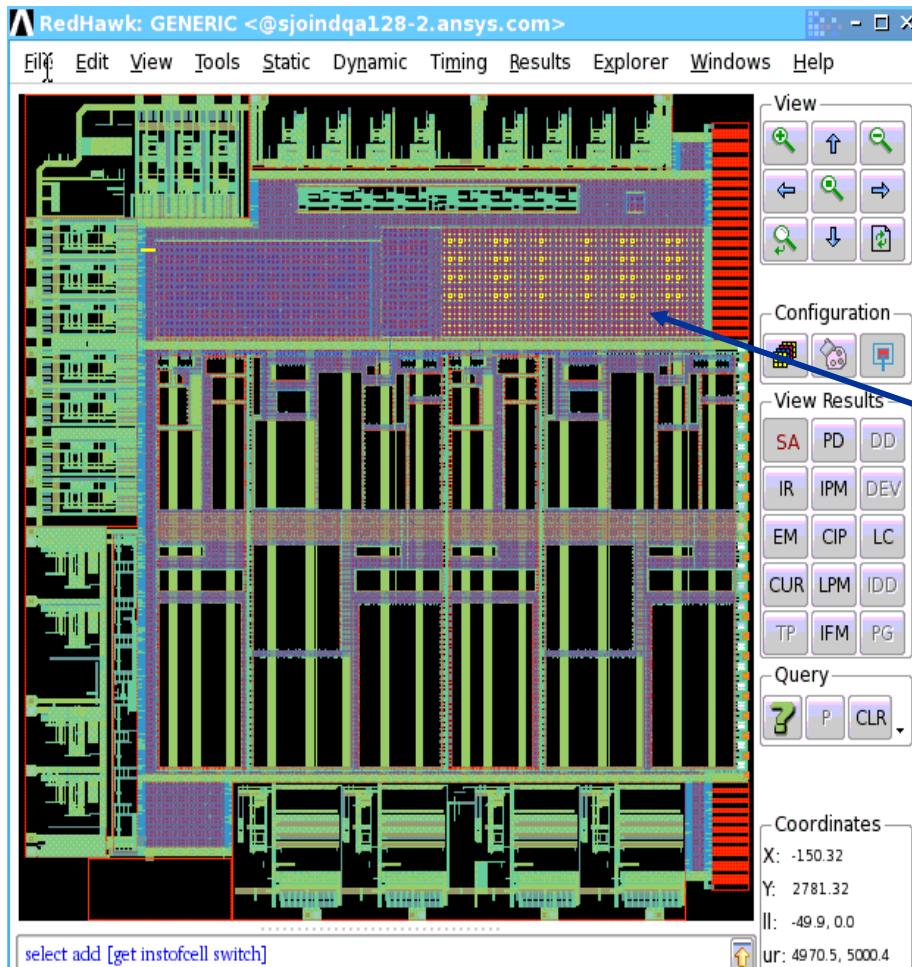
Name of top cell: GENERIC
Size of chip: 0 0 4920.62 5000.36

Number of power nets: 2
Number of ground nets: 1
Number of P/G pads: 80

Number of instances: 255197
Number of memory/ip: 7
Number of sub blocks: 0
Number of clock inst: 6060
Number of decaps: 221105

Number of nodes: 1234696
Number of resistors: 1447700

Some GUI Features



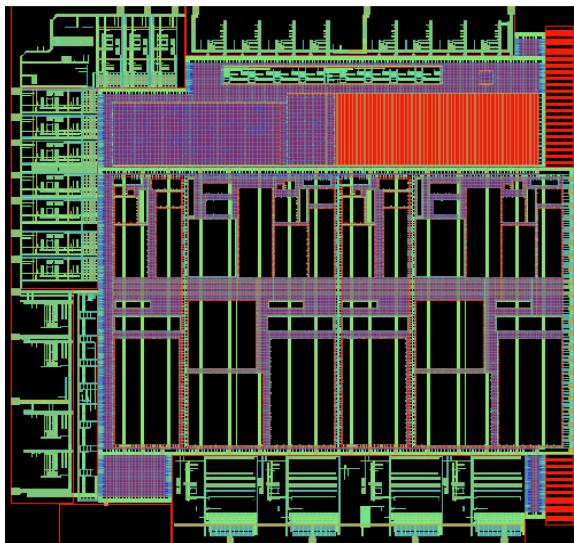
- **TCL query**

```
select add [get instofcell switch]
```

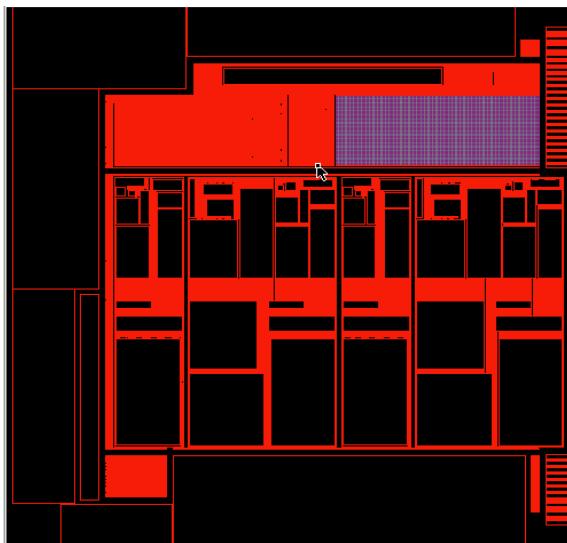
Some GUI Features

Net Selection Options

Constant VDD Domain

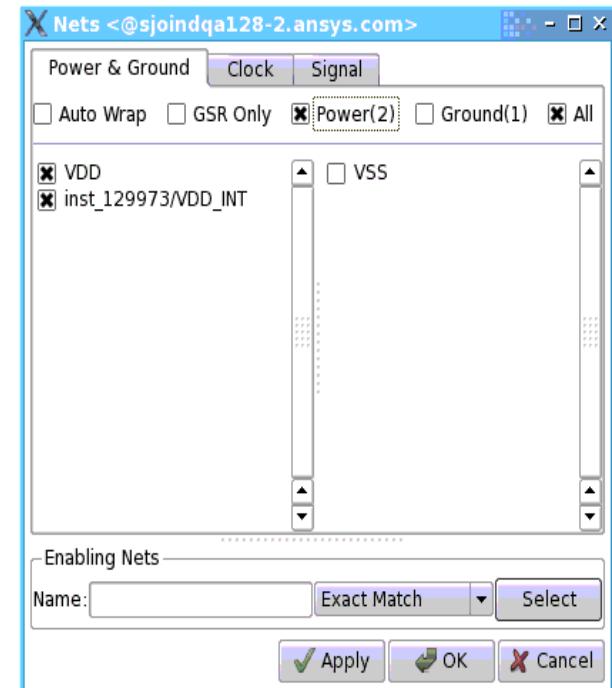


Virtual VDD_INT Domain



```
config viewnet -name all -mode off  
config viewnet -name VDD -mode on
```

```
config viewnet -name all -mode off  
config viewnet -name inst_129973/VDD_INT -mode on
```



Same can be done with
View -> Nets Menu

Layer Options



Name	Invisible	Color	Brush	Fill	Outline	Selectable	Pin Inst
OVERLAP	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>
OVERLAPCont	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>
VIA23	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
METAL3	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
VIA34	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
METAL4	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
VIA45	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
METAL5	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
VIA56	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
METAL6	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>

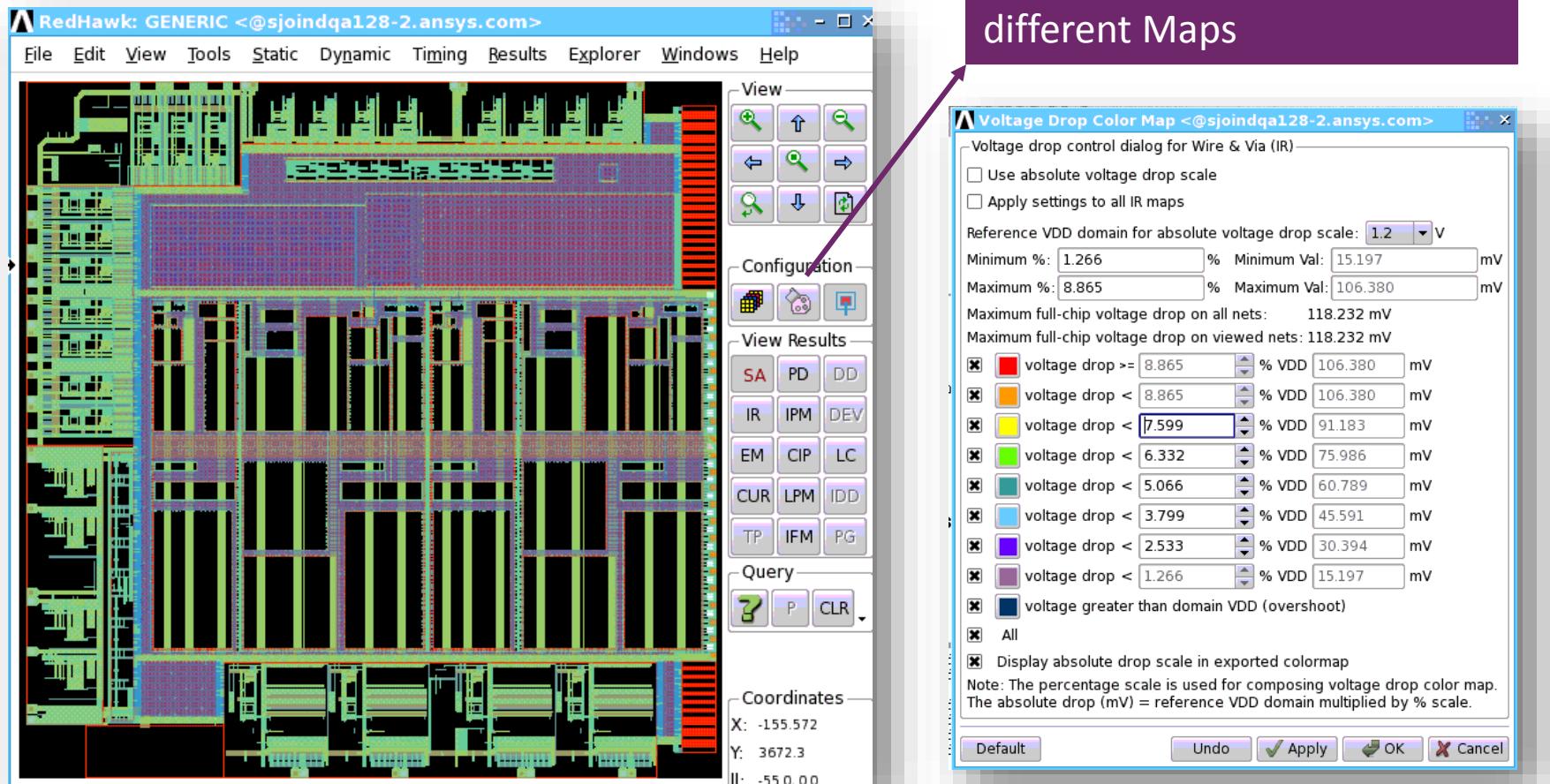
Select layer options

Layer Selectability

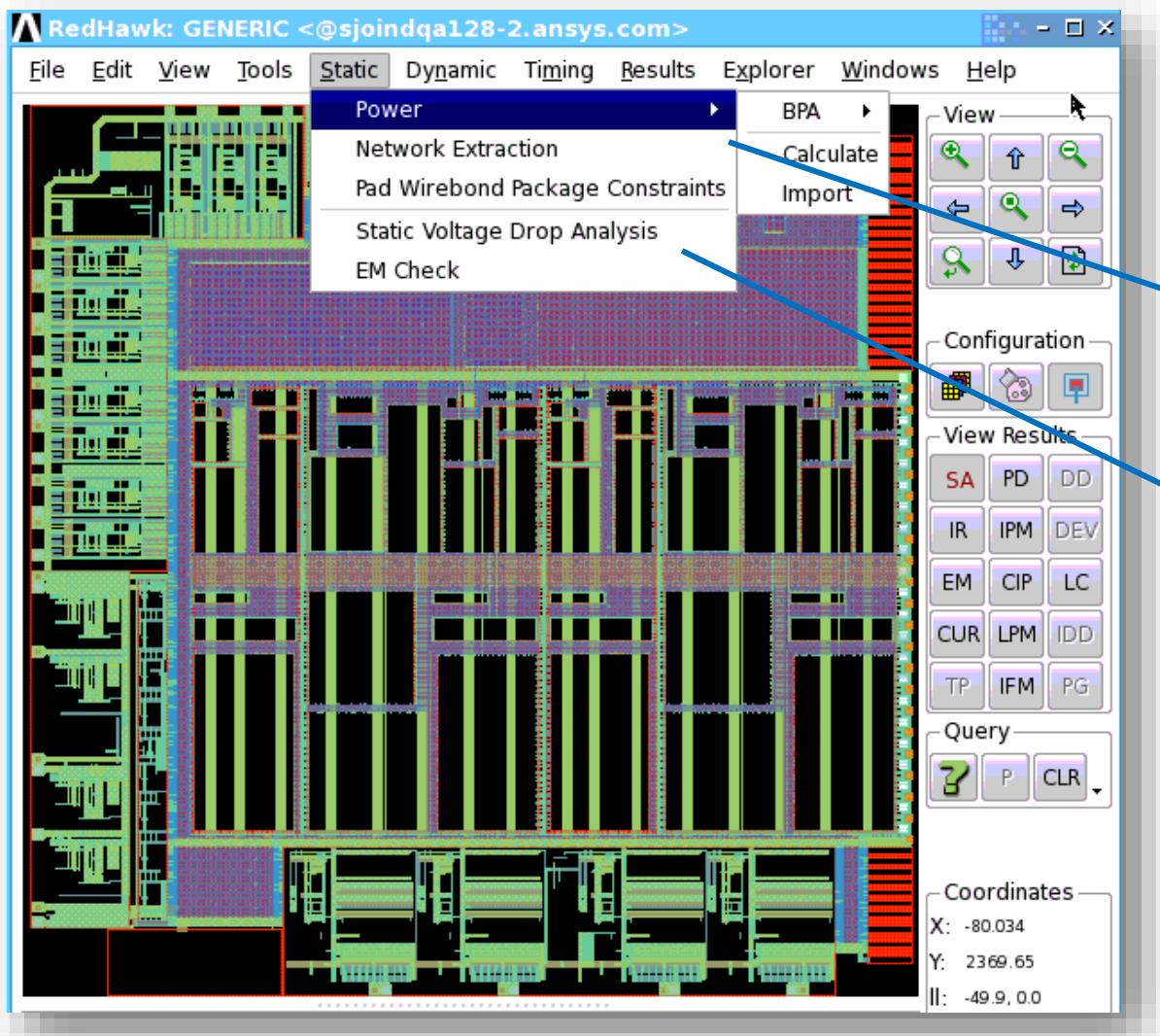
Select or Deselect metal layers and via

Select Mode: Fill or Outline

Set Color Range

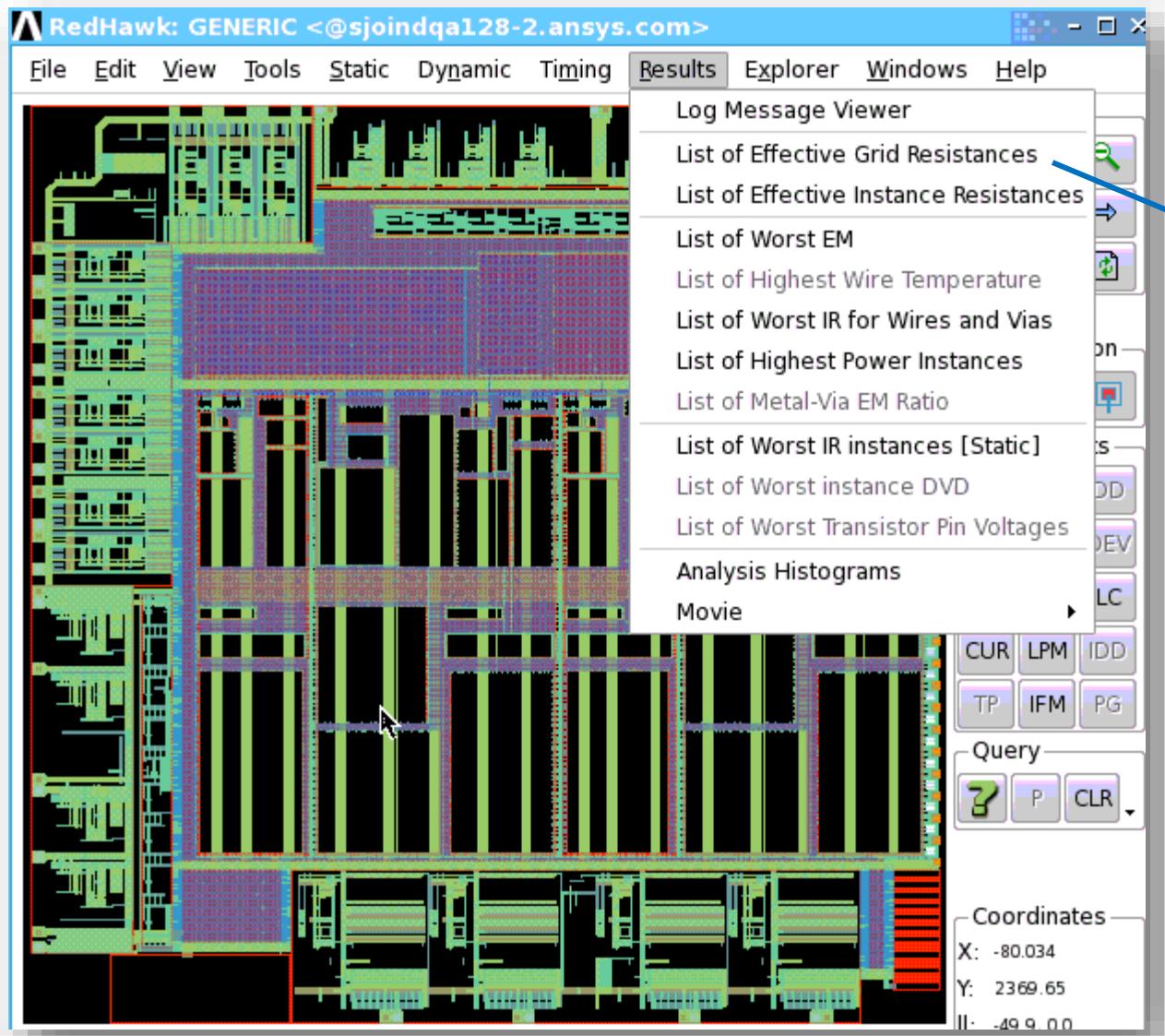


GUI Menu Overview



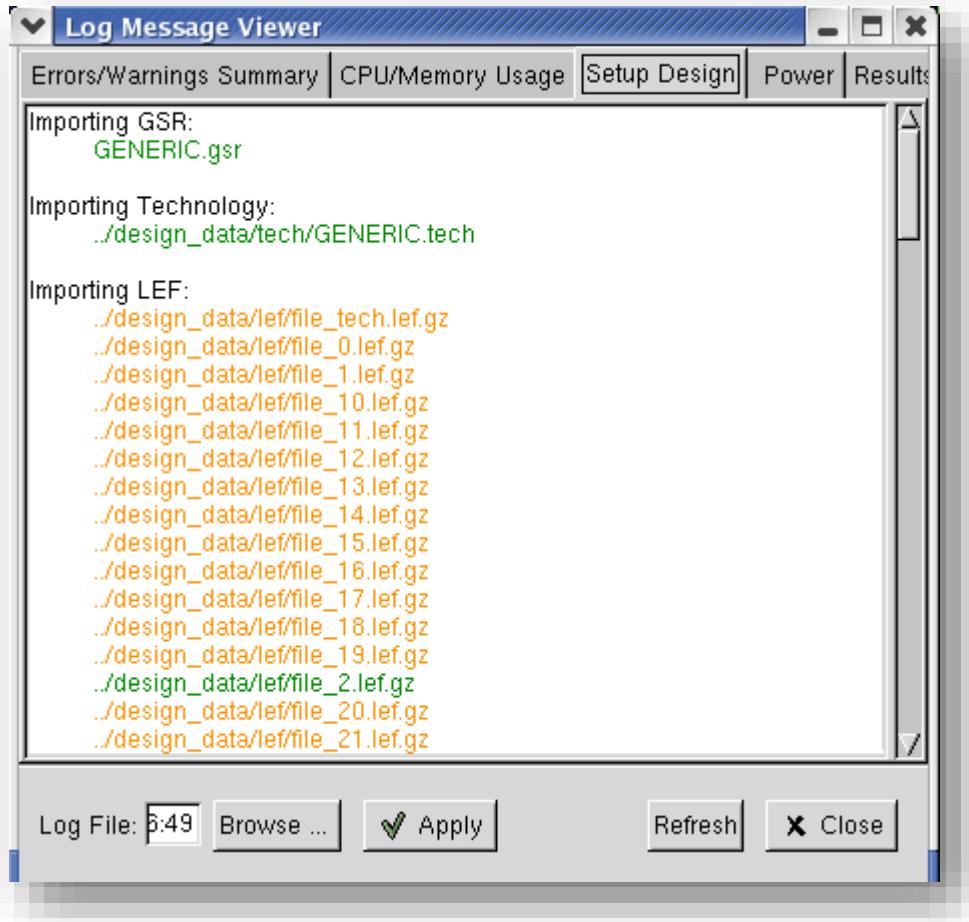
- **Static Analysis Steps**
 - Power calculation and Extraction options
- **Static IR/EM analysis options**

GUI Menu Overview (Cont'd)



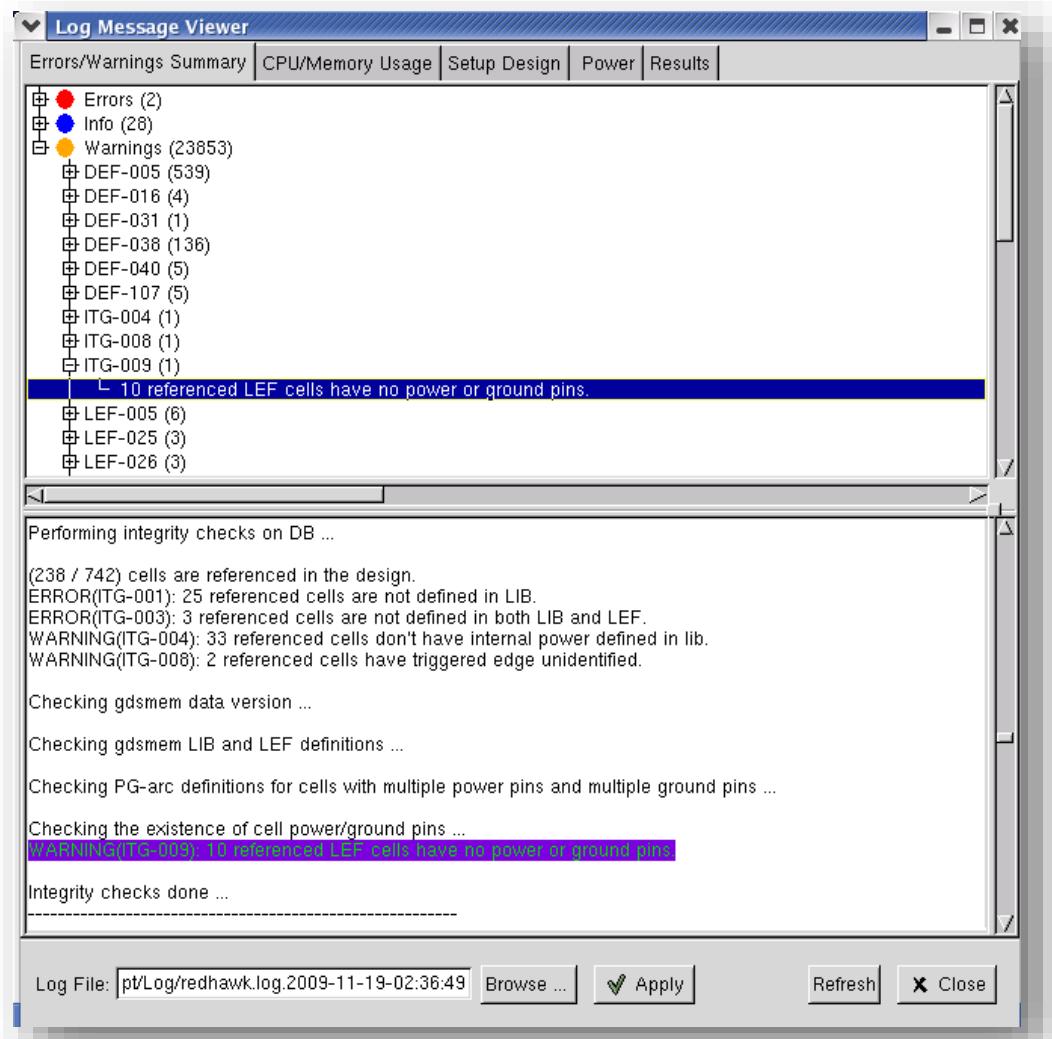
- Result viewing options

Log Message Viewer



- **Select Results → Log Message Viewer**
- **Click on Setup Design Tab**
- **Error tagging on files read-in**
 - **Red** → Error during import
 - **Orange** → Warnings
 - **Green** → No issues seen

Log Message Viewer (Cont'd)



Common LEF/DEF Issues

- **Power pins in LEF**
 - Both power and ground pins must be defined
 - Must contain geometries
 - USE POWER and USE GROUND specified?
- **Power pins in DEF**
 - Block level DEF must have logical definition
 - Top level DEF need not have pins defined, unless 'ADD_PLOC_FROM_TOP_DEF 1' is set in GSR
 - Example
 - VDD + NET VDD + USE POWER + DIRECTION INOUT
 - + LAYER MET6 + RECT (0 0) (100 100) + PLACED N (12340 23450)

Common LEF/DEF Issues (Cont'd)

- **Power/Ground nets in DEF**
 - Power and ground nets in SPECIAL NETS and/or NETS section must have USE POWER and USE GROUND attributes
- **P/G nets must establish logical connectivity**
 - - VDD (I1 VDD) (I1/MUX1 VDD) (RAM1 VDD) + MET1
 - - VDD (* VDD) + MET1

PG-arc Issues

- **ERROR(ITG-016): Missing PG-arc definitions for cell**
 - To support cells with multiple Vdd and multiple Vss pins, you need to specify the P/G arcs to define the current path between each VDD node to the associated GND node pair.
 - Example of pgarc defined in custom lib file for a cell

```
cell ram_mvdd {  
    pgarc {  
        VDD VSS  
        VDD2 VSS2  
        VDDL VSS  
    }  
}
```

PG-arc Issues (*Cont'd*)

- Specify the custom.lib under the LIB_FILES section of the GSR

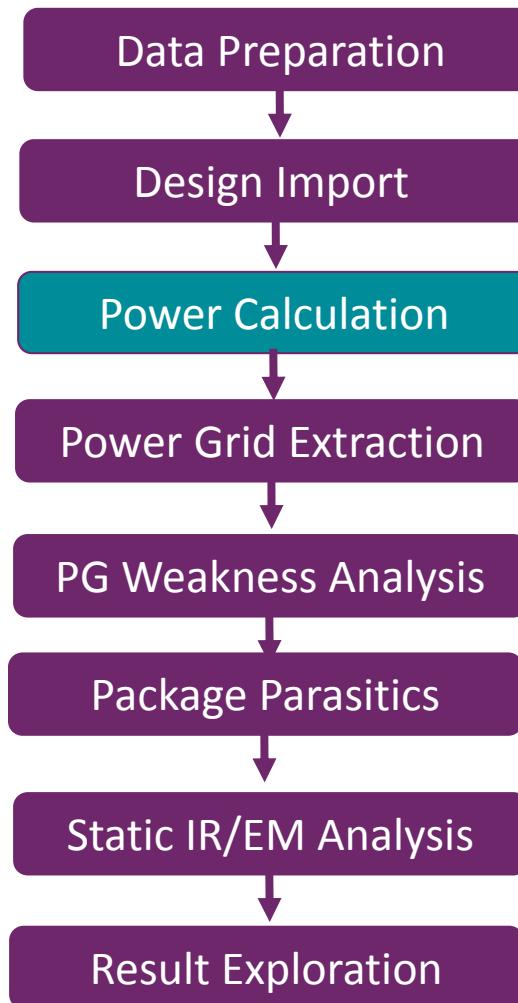
```
LIB_FILES {  
    <lib_filename> CUSTOM  
    ...  
}
```

- If you are unsure as to which cells need to be specified in a custom library, then run the design through 'setup design' and look at the data in the file adsRpt/apache.refCell.noPAGArc
- RedHawk detects cells with multiple ground pins that have no custom LIB file and reports them in the report adsRpt/apache.refCell.noPAGArc, along with all power and ground pins for each cell.

Example:

```
#<cell_name> <vdd_pin_names> <gnd_pin_names>  
<SC_ANALOG> <VDD1A VDD2A> <VSS1A VSS2A>
```

Step 3: Power Calculation



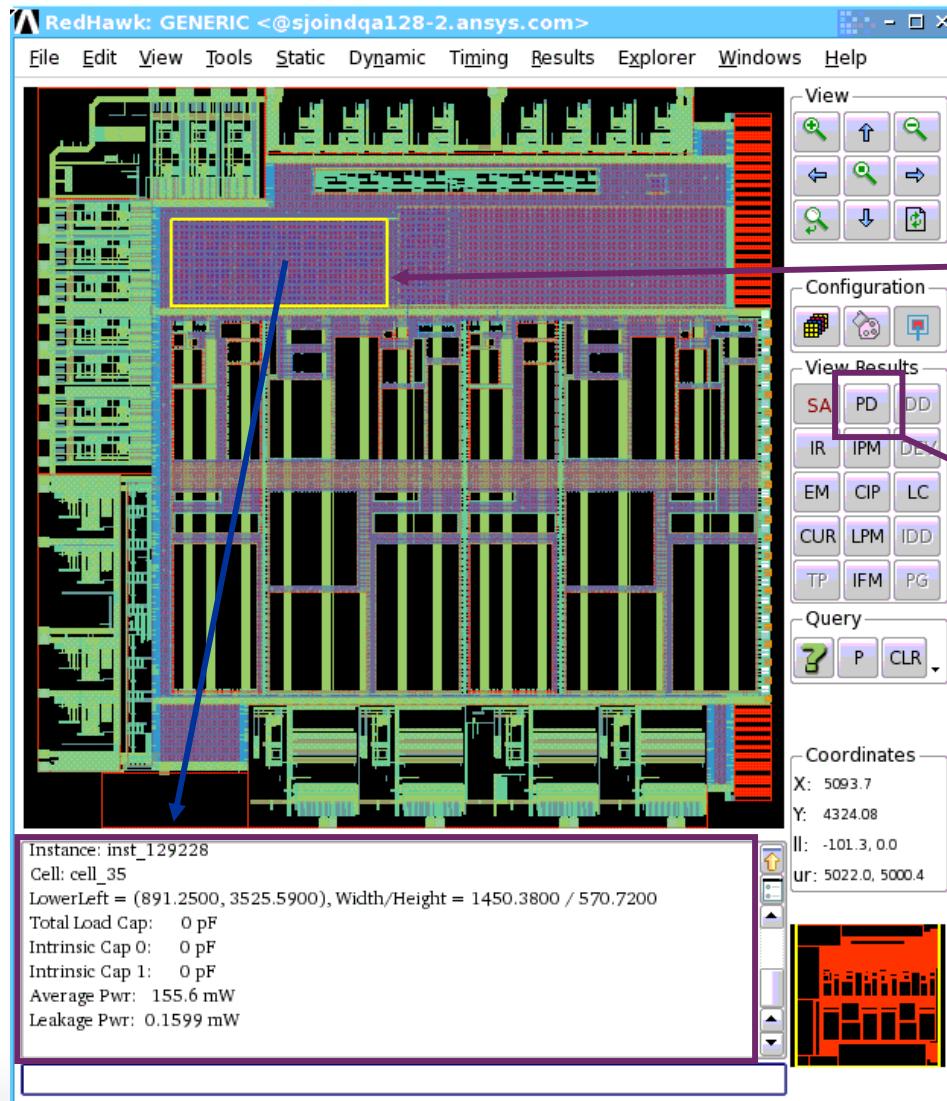
```
# Import data  
import gsr GENERIC.gsr  
setup design  
setup analysis_mode static  
  
# Calculate power  
perform pwrcalc  
  
# Power/Ground grid extraction  
perform extraction -power -ground  
  
# Lumped resistance (in Ohms)  
# for package, wirebond and pads  
setup package -power -r 0.005 -l 2.5 -c 5  
setup package -ground -r 0.005 -l 2.5 -c 5  
setup wirebond -power -r 0.01 -l 2.2 -c 1.42  
setup wirebond -ground -r 0.05 -l 1.7 -c 0.2  
setup pad -power -r 0.001  
setup pad -ground -r 0.001  
  
# Static IR analysis  
perform analysis -static  
  
# Result Exploration using RHE  
explore design
```

* In GUI : *Static -> Power -> Calculate Power*

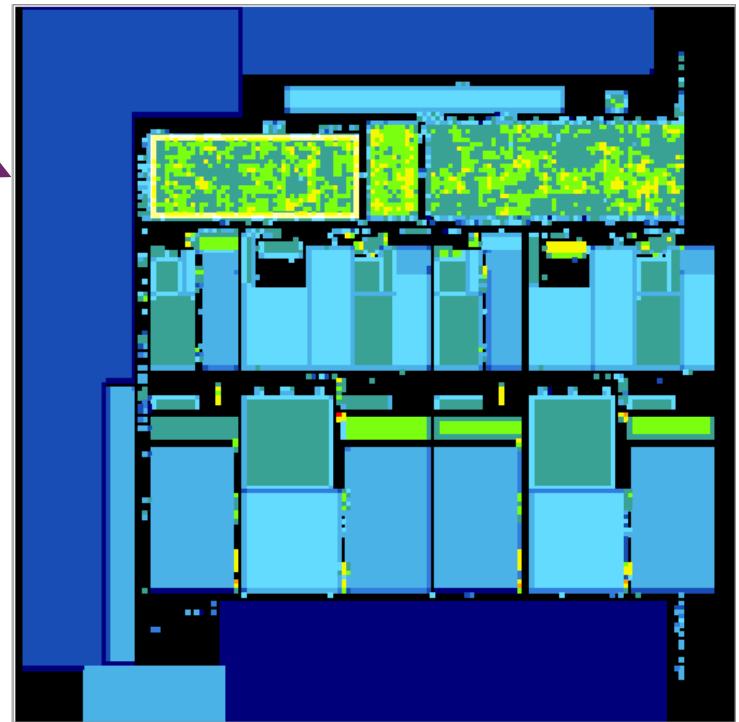
Power Calculation

- Calculates power of cells and blocks in the design and total power of the design
- Can also import power from 3rd party tools
- Power DB created has the name: adsPower
- Can be imported for subsequent static and dynamic analysis if the design netlist and parameters do not change
- Important: Check for cell with missing .lib or power models during run or in RedHawk™ log file
 - adsRpt/apache.refCell.noLib
 - adsRpt/apache.refCell.noPwr

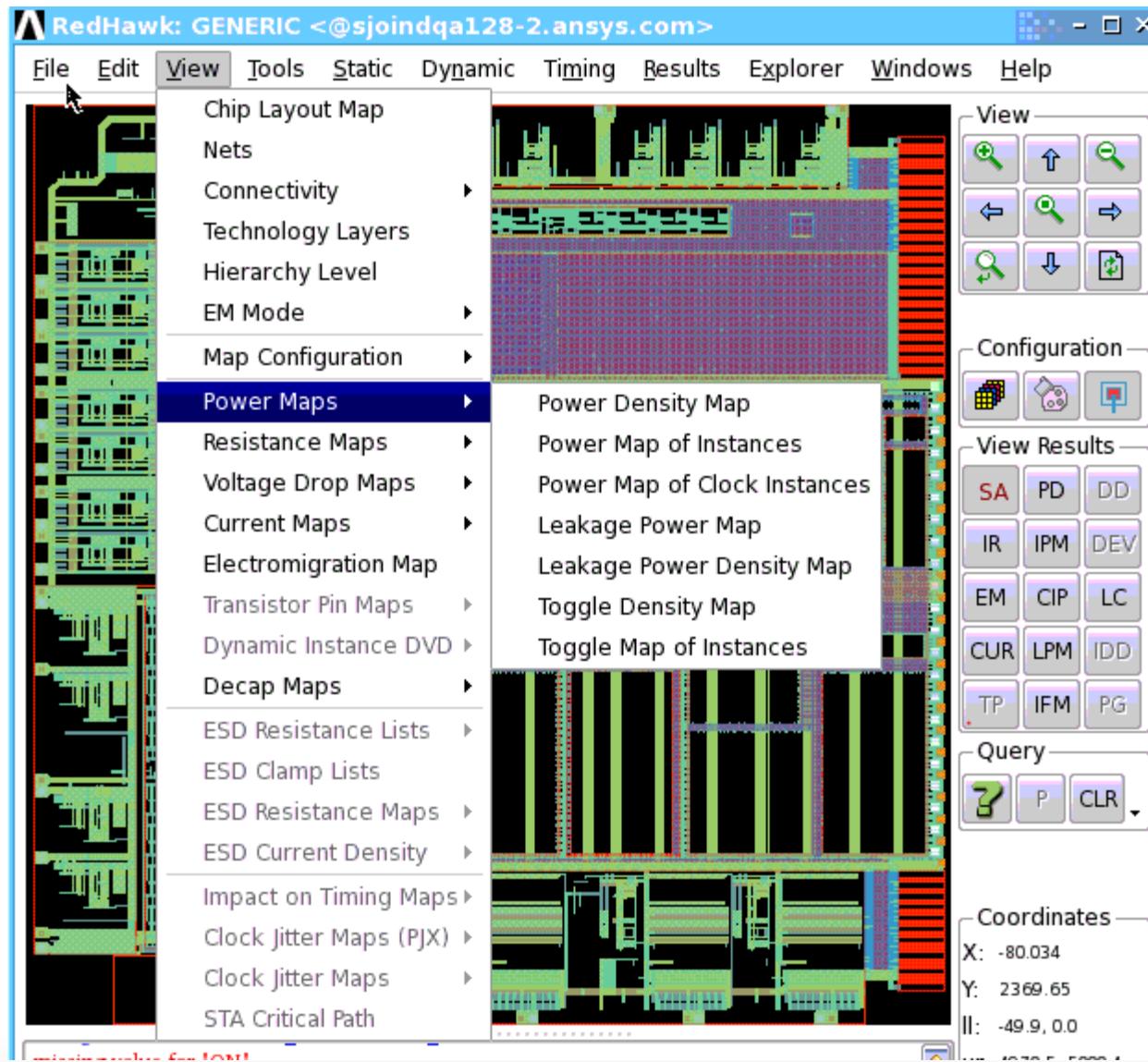
Power Calculation (Cont'd)



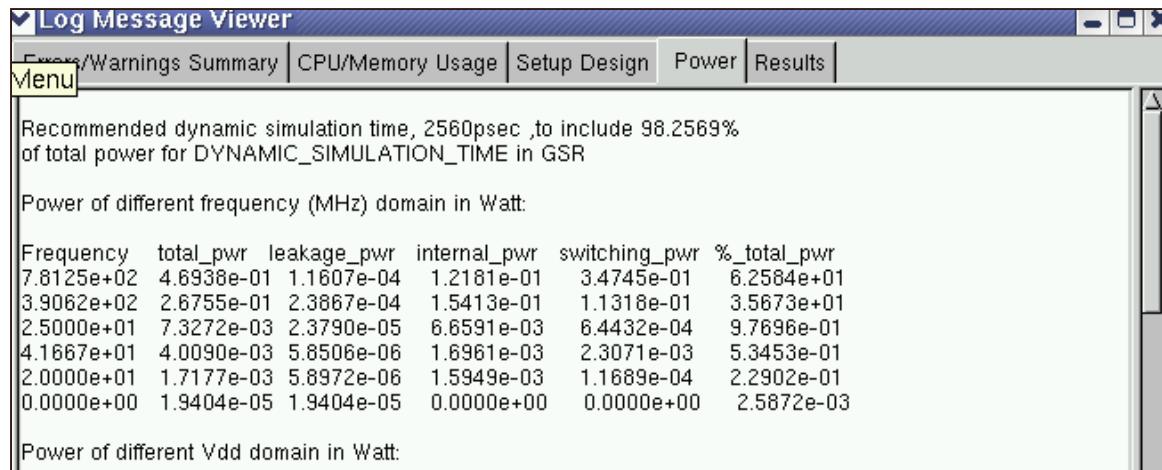
- Examine Power Density (PD) map and Instance Power (IPM) map
- Click on instance to query the power



Viewing Power Maps



Power Analysis Reports



Select

Results → Log Message Viewer

Then select **Power** tab

Examine power summary

adsRpt/power_summary.rpt - Summary of power consumption

Domain

Frequency

Clock, non-clock

tcl command: report power –o power.rpt

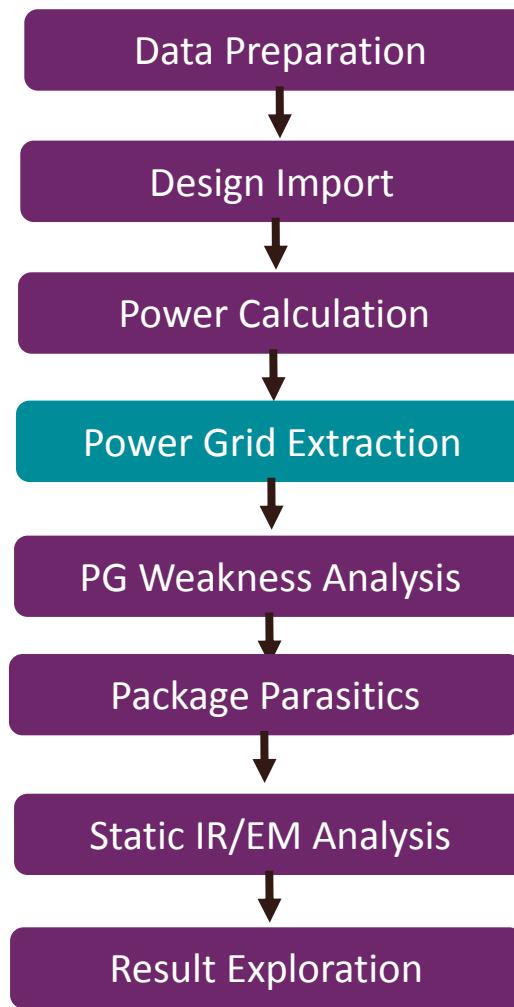
gives instance level power, frequency, toggle, location, cell name

* Same report as in Log Message Viewer

Power Calculation Issues/Checks

- Does the Total Power number make sense?
- Clock network power and Clock power reasonable?
 - Clock network power is power of clock tree/mesh, typically ~ 20-30% of total
 - Clock power is network power + clock pin power, typically ~ 30-40% of total
- Power per clock frequency domain reasonable?
 - Determined by clock roots or Primetime STA file
 - Incorrect clock roots or PT case analysis?

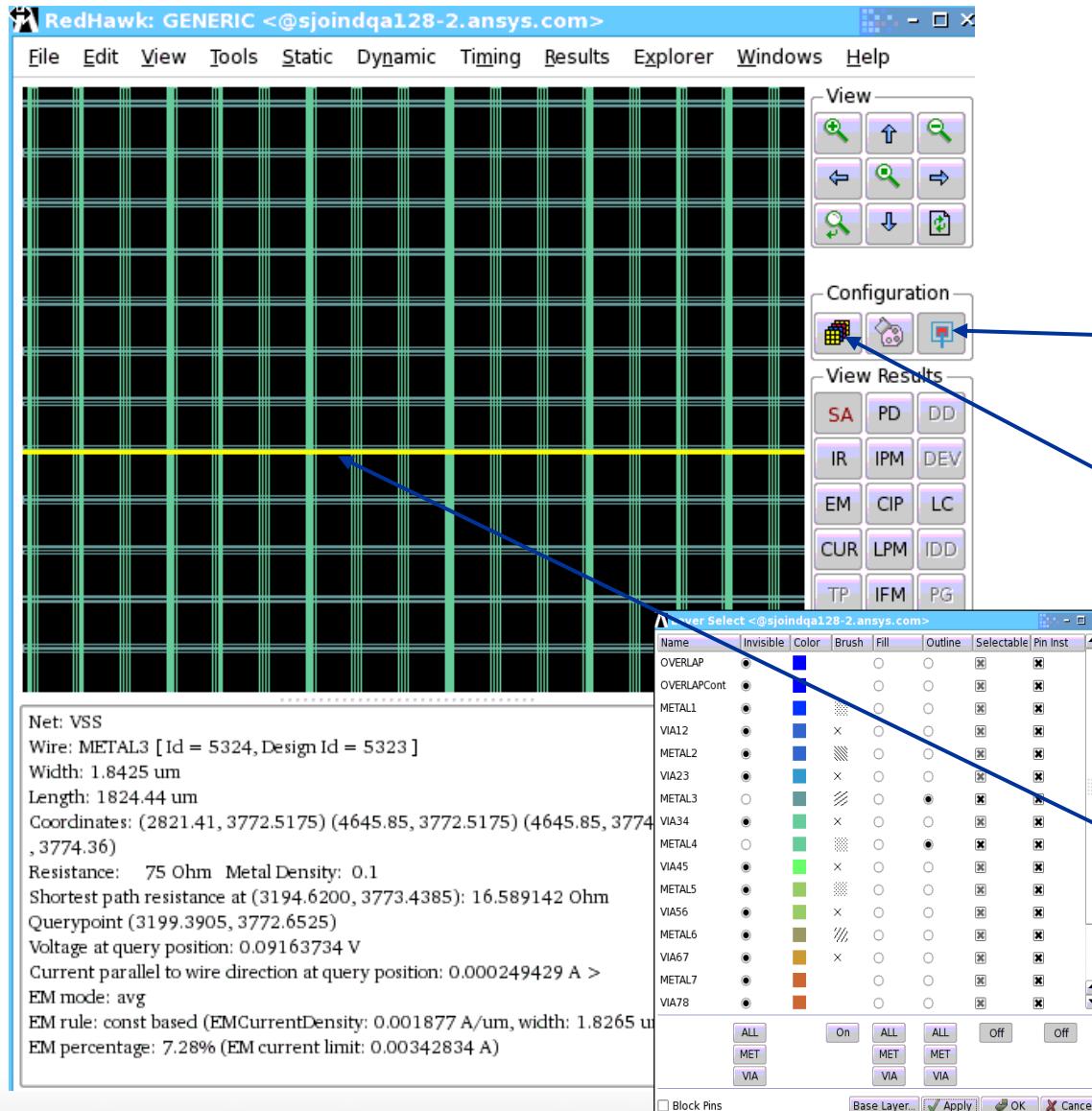
Step 4: Network Extraction



```
# Import data  
import gsr GENERIC.gsr  
setup design  
setup analysis_mode static  
  
# Calculate power  
perform pwrcalc  
  
# Power/Ground grid extraction  
perform extraction -power -ground  
  
# Lumped resistance (in Ohms)  
# for package, wirebond and pads  
setup package -power -r 0.005 -l 2.5 -c 5  
setup package -ground -r 0.005 -l 2.5 -c 5  
setup wirebond -power -r 0.01 -l 2.2 -c 1.42  
setup wirebond -ground -r 0.05 -l 1.7 -c 0.2  
setup pad -power -r 0.001  
setup pad -ground -r 0.001  
  
# Static IR analysis  
perform analysis -static  
  
# Result Exploration using RHE  
explore design
```

* In GUI: **Static -> Network Extraction**

Extraction

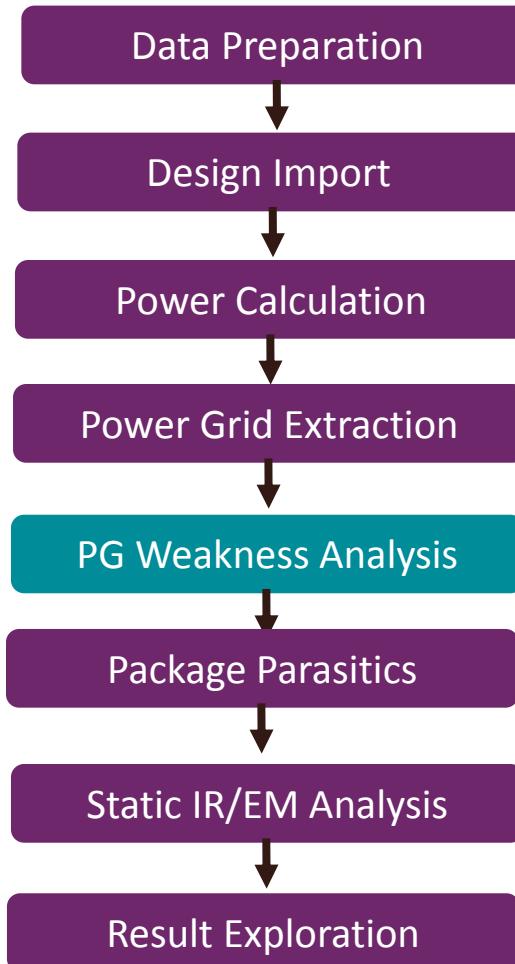


- Execute:
perform extraction -power -ground
- Click on Show Power Pad button to see location of voltage sources
- Bring up ***View Layers*** Dialog box. Choose some metals/via layers
- Click on wires/vias to query resistance

PG Network Extraction Issues

- **Is Power or Ground net connected to ideal source?**
 - “Net VDD not driven by any pad, pcell or ploc”
- **Any disconnected PinInst, wire or vias?**
 - Check adsRpt/<design>_VDD.*.unconnect
 - Check adsRpt/<design>_VSS.*.unconnect
 - Check adsRpt/<design>.*.unconnect
- **Any shorts between nets?**
 - Watch out for CON-109, CON-110 and CON-111 errors
 - These can result from either physical shorts or from lack of logical connectivity between DEFs and LEFs
- **Look for power and/or ground pins that are incorrectly placed**
 - either wrong polarity or not placed on a wire

Step 5: PG Weakness Analysis



- **Early analysis capability for power grid robustness**
 - PG Resistance Analysis
 - Missing Vias
 - Analyzing Shorts
 - Disconnected wires / Vias
 - Disconnected instances
 - Perform Resistance Calculation
- **Can be performed as early as in the floor-plan stage**

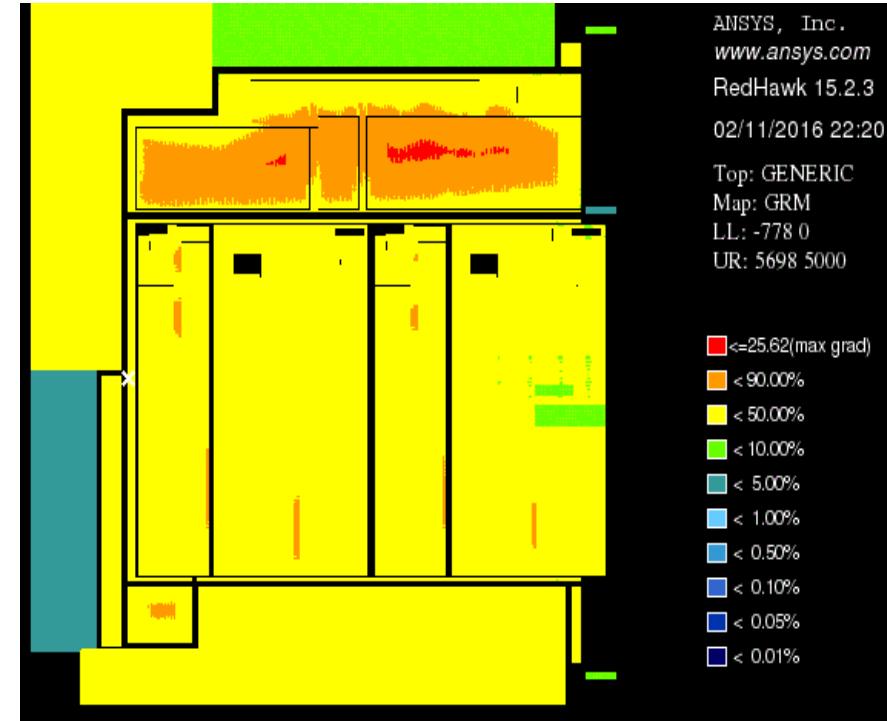
Resistance Maps

GUI: View → Resistance Maps

VDD Resistance



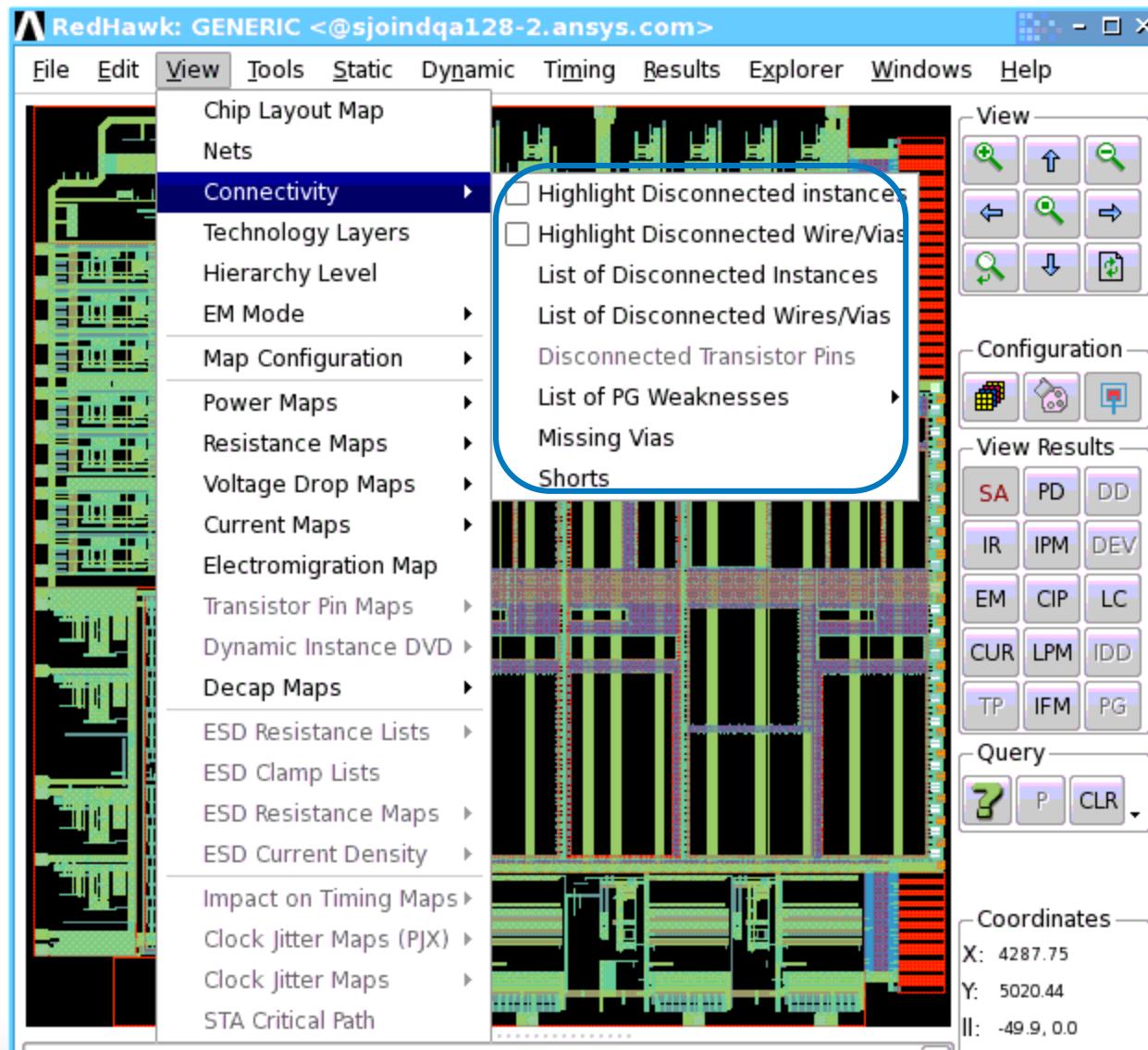
VSS Resistance



Asymmetry between power and ground resistance

Helps identifying weak regions

Connectivity Checks



Explore 'perform res_calc' Command

- '**perform res_calc**' command calculates effective PG grid resistance from all pads to selected instances or locations.
- It gives the absolute resistance value whereas '**perform gridcheck**' gives the normalized resistance.
- **Syntax**

```
perform res_calc ?[-instance <name>]? ?[-inst_file <file>]?  
? -incremental? ?[-cell <name>]? ?-all_point? ?-worst_point?  
?-box <llx lly urx ury>? ?-gnd <name>? ?-pwr <name>?  
?-layer <name>? ?-limit <num>? ?-o <file>? ?-append? ?-verbose?  
?-thread <num>? ?-xtor <name_list>? ? -loopmode ?  
?-pin <name_list>? ?-all_pin? ? -cell_file <CellFile>?
```

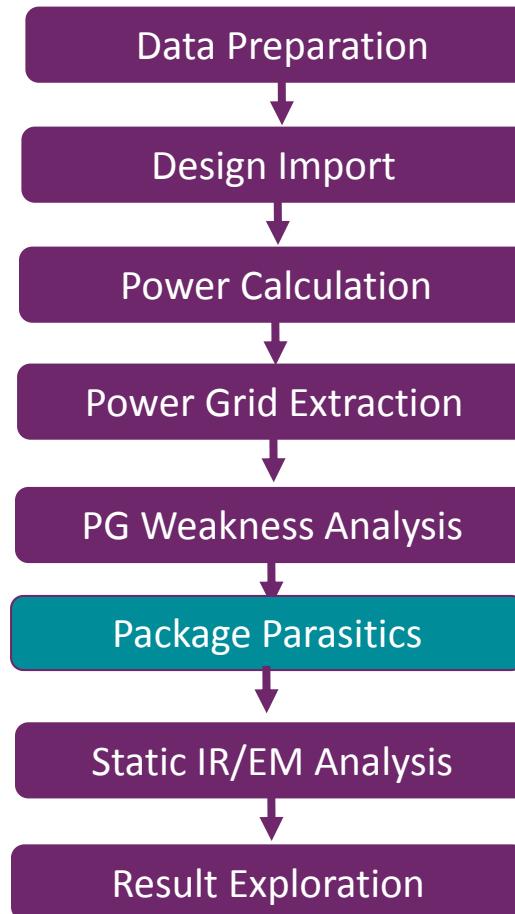
- Please refer to the RedHawk Manual for details about each option.
- The default, without any option '**perform res_calc**' gives the resistance report for worst instances as indicated by quick estimation
- The default output file is *adsRpt/<design_name>.res_calc*

'perform res_calc' - Output

```
# Grid Resistance Calculation Report
#
# Resistances from all pads to the listed points
# Ohm  Location(x y)  Layer  Net      Instance
67.3972 4459.77 443.855 METAL3  VDD      inst_129747/adsU1
4.42445 2839.61 3959.78 METAL1 inst_129973/VDD_INT inst_129973/inst_375304
4.30808 2840.44 3952.4  METAL1 inst_129973/VDD_INT inst_129973/inst_367447
4.12397 2841.42 3952.4  METAL1 inst_129973/VDD_INT inst_129973/inst_431199
4.03733 2841.88 3952.4  METAL1 inst_129973/VDD_INT inst_129973/inst_431200
3.9507  2842.34 3952.4  METAL1 inst_129973/VDD_INT inst_129973/inst_431201
3.86406 2842.8   3952.4  METAL1 inst_129973/VDD_INT inst_129973/inst_431203
3.77742 2843.26 3952.4  METAL1 inst_129973/VDD_INT inst_129973/inst_368305
3.69078 2843.72 3952.4  METAL1 inst_129973/VDD_INT inst_129973/inst_431205
2.92883 2871.29 3981.92 METAL1 inst_129973/VDD_INT inst_129973/inst_304473
2.92823 2870.86 3981.92 METAL1 inst_129973/VDD_INT inst_129973/inst_304472
2.92575 2870.4   3981.92 METAL1 inst_129973/VDD_INT inst_129973/inst_304471
```

- The first column shows the absolute resistance of P/G pads from the selected points, the second and third column give the (x,y) co-ordinates of the instance ,the fourth ,fifth and sixth columns give the Layer name, Net name and instance name respectively.**

Step 6: Package and Pad Constraints



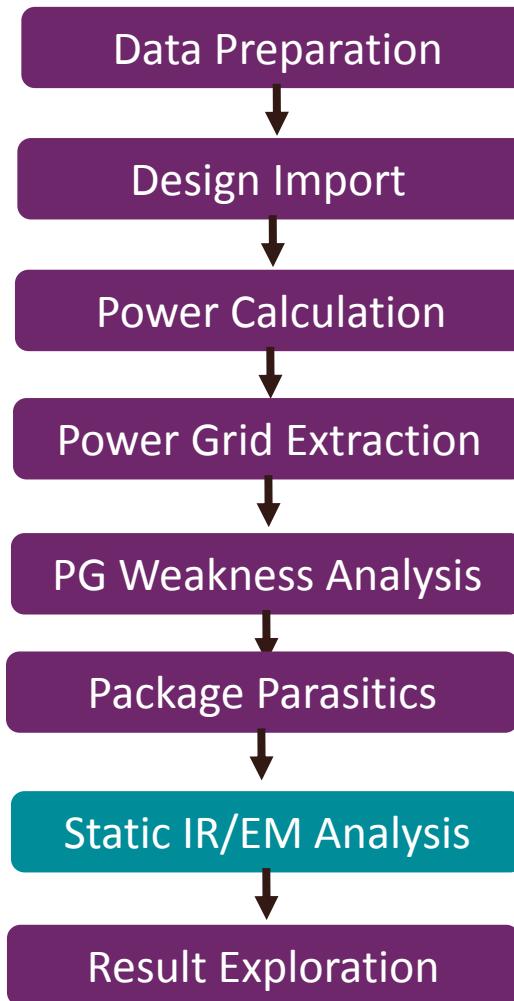
```
# Import data
import gsr GENERIC.gsr
setup design
setup analysis_mode static
# Calculate power
perform pwrcalc
# Power/Ground grid extraction
perform extraction -power -ground

# Lumped resistance (in Ohms)
# for package, wirebond and pads
setup package -power -r 0.005 -l 2.5 -c 5
setup package -ground -r 0.005 -l 2.5 -c 5
setup wirebond -power -r 0.01 -l 2.2 -c 1.42
setup wirebond -ground -r 0.05 -l 1.7 -c 0.2
setup pad -power -r 0.001
setup pad -ground -r 0.001

# Static IR analysis
perform analysis -static
# Result Exploration using RHE
explore design
```

- **GUI: Static -> Pad, Wirebond / Bump and Package Constraint**
- **Distributed Package model in spice / S-parameter format also supported**

Step 7: Static Analysis



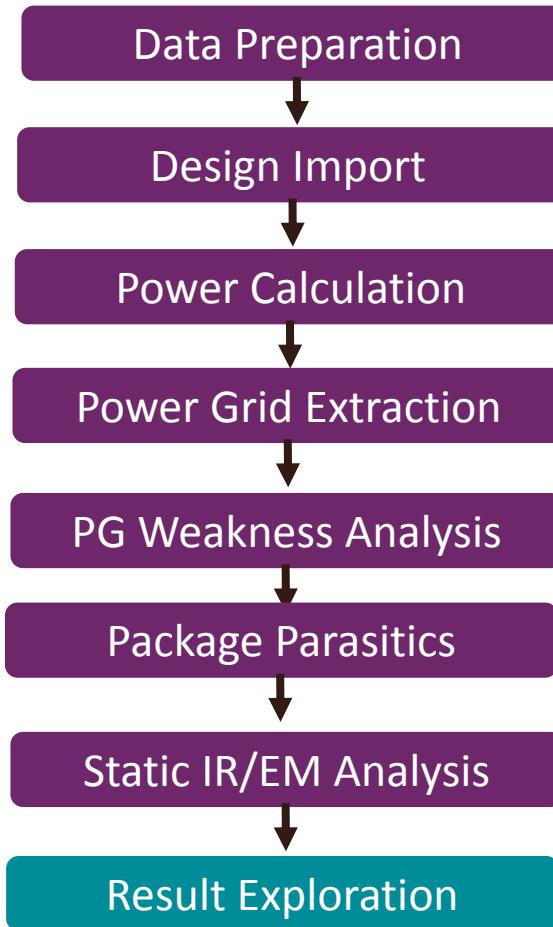
```
# Import data
import gsr GENERIC.gsr
setup design
setup analysis_mode static
# Calculate power
perform pwrcalc
# Power/Ground grid extraction
perform extraction -power -ground
# Lumped resistance (in Ohms)
# for package, wirebond and pads
setup package -power -r 0.005 -l 2.5 -c 5
setup package -ground -r 0.005 -l 2.5 -c 5
setup wirebond -power -r 0.01 -l 2.2 -c 1.42
setup wirebond -ground -r 0.05 -l 1.7 -c 0.2
setup pad -power -r 0.001
setup pad -ground -r 0.001
```

```
# Static IR analysis
perform analysis -static
```

```
# Result Exploration using RHE
explore design
```

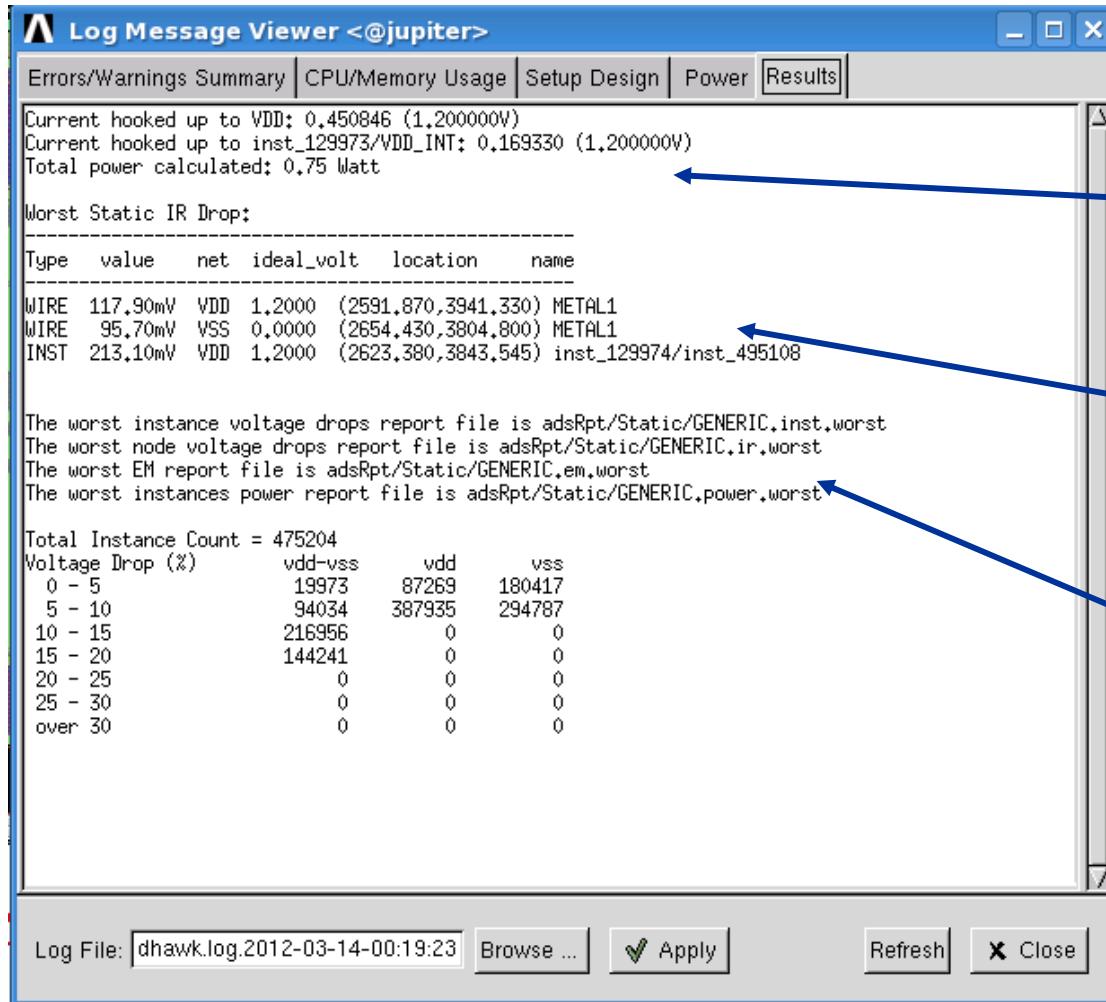
**GUI: Static -> Static IR-drop & EM Analysis*

Step 8: Result Exploration and Debugging



- **Result summary**
- **Log message viewer**
- **Result Maps**
- **EM violations**
- **Text Results**
- **RedHawk Explorer**

Examine Summary of Results



Total power of cells hooked to the network

IR drop summary

Text report pointers

* Log/error/warnings/command history stored under adsRpt

Examine Summary of Results (Cont'd)

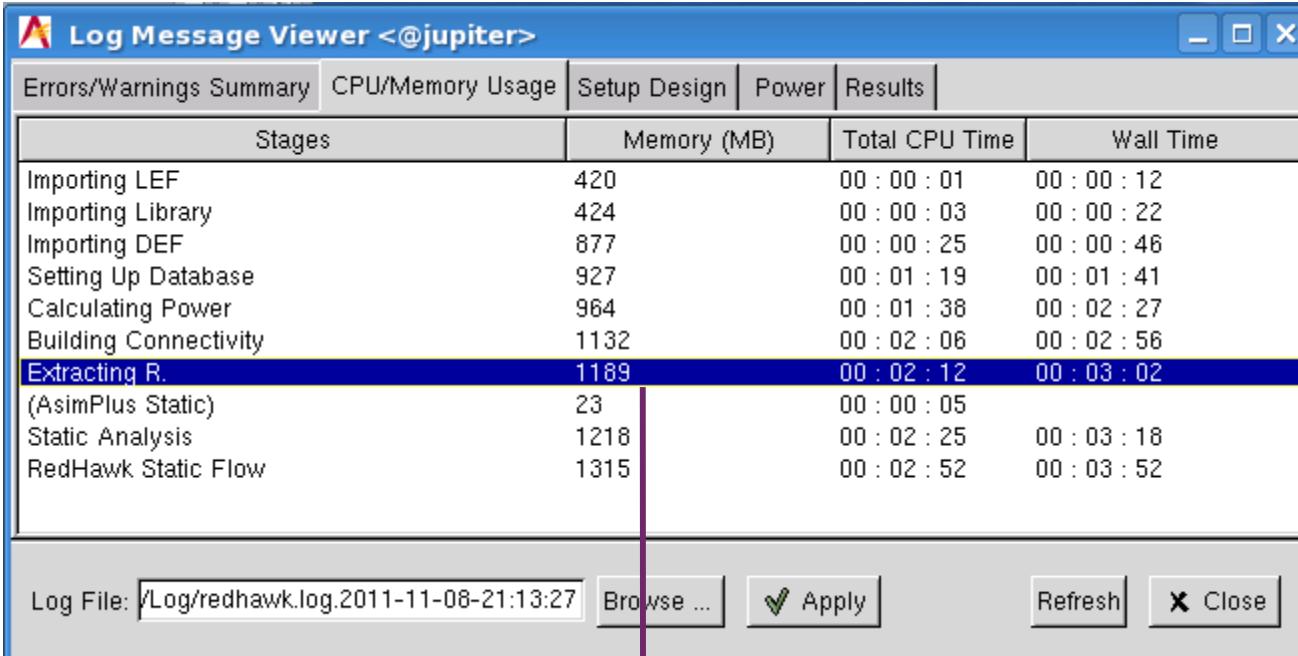
- **Summarizes variation in current load for all switches**
- **Can identify the ineffective switches from this report**
- **Switches supplying high current also cause high voltage drop**

#Report static results of switch voltage and current (milli-amperes)				
#instance_name	type	internal_node_volt	volt_across_switch	avg_current
inst_129973/switch_inst_R1_C37	header	1.120460e+00	7.119894e-03	3.559953e-01
inst_129973/switch_inst_R2_C37	header	1.120161e+00	5.535722e-03	2.767889e-01
inst_129973/switch_inst_R3_C37	header	1.119729e+00	4.471302e-03	2.235622e-01
inst_129973/switch_inst_R4_C37	header	1.119197e+00	3.818512e-03	1.909233e-01
inst_129973/switch_inst_R5_C37	header	1.118597e+00	3.499985e-03	1.750022e-01
inst_129973/switch_inst_R6_C37	header	1.118092e+00	3.330708e-03	1.665321e-01
inst_129973/switch_inst_R7_C37	header	1.117795e+00	3.185511e-03	1.592779e-01
inst_129973/switch_inst_R8_C37	header	1.117690e+00	3.070951e-03	1.535502e-01
inst_129973/switch_inst_R9_C37	header	1.117705e+00	3.050566e-03	1.525241e-01
inst_129973/switch_inst_R10_C37	header	1.117875e+00	3.087044e-03	1.543536e-01
inst_129973/switch_inst_R11_C37	header	1.118198e+00	3.185987e-03	1.593002e-01
inst_129973/switch_inst_R12_C37	header	1.118591e+00	3.437638e-03	1.718832e-01
inst_129973/switch_inst_R13_C37	header	1.119055e+00	3.858209e-03	1.929125e-01
inst_129973/switch_inst_R14_C37	header	1.119729e+00	4.336834e-03	2.168394e-01
inst_129973/switch_inst_R15_C37	header	1.120405e+00	5.117297e-03	2.558678e-01
inst_129973/switch_inst_R16_C37	header	1.120906e+00	6.428599e-03	3.214287e-01
inst_129973/switch_inst_R17_C37	header	1.121169e+00	8.426189e-03	4.213073e-01
inst_129973/switch_inst_R1_C5	header	1.093288e+00	4.444599e-03	2.222256e-01
inst_129973/switch_inst_R2_C5	header	1.093037e+00	3.346086e-03	1.673064e-01
inst_129973/switch_inst_R3_C5	header	1.092635e+00	2.631903e-03	1.315955e-01

/adsRpt/Static/switch_static.rpt

CPU/Memory Usage

Select **Results → Log Message Viewer**
Then select **CPU/Memory usage** tab



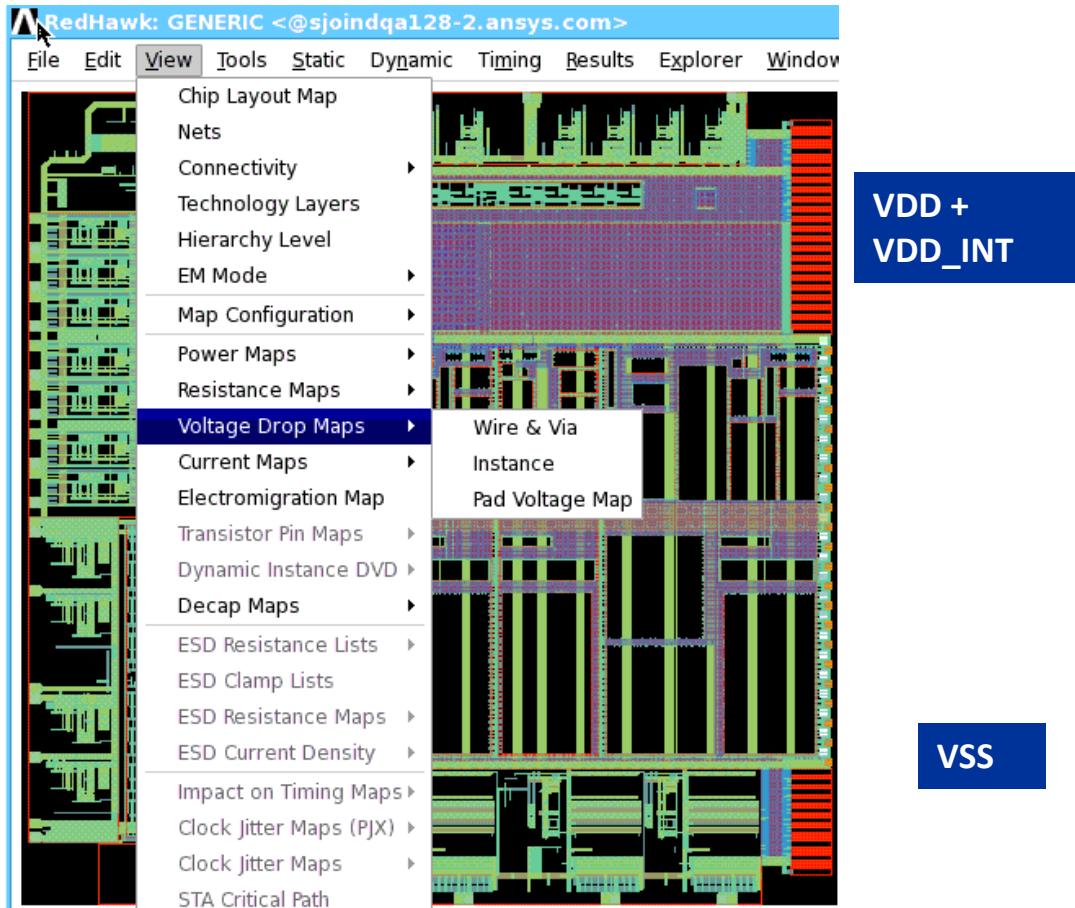
Stages	Memory (MB)	Total CPU Time	Wall Time
Importing LEF	420	00 : 00 : 01	00 : 00 : 12
Importing Library	424	00 : 00 : 03	00 : 00 : 22
Importing DEF	877	00 : 00 : 25	00 : 00 : 46
Setting Up Database	927	00 : 01 : 19	00 : 01 : 41
Calculating Power	964	00 : 01 : 38	00 : 02 : 27
Building Connectivity	1132	00 : 02 : 06	00 : 02 : 56
Extracting R. (AsimPlus Static)	1189	00 : 02 : 12	00 : 03 : 02
Static Analysis	23	00 : 00 : 05	
RedHawk Static Flow	1218	00 : 02 : 25	00 : 03 : 18
	1315	00 : 02 : 52	00 : 03 : 52

Log File: /Log/redhawk.log.2011-11-08-21:13:27

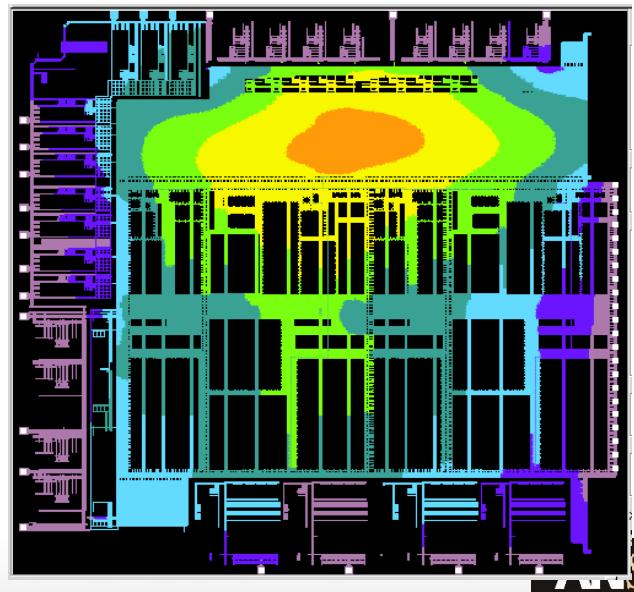
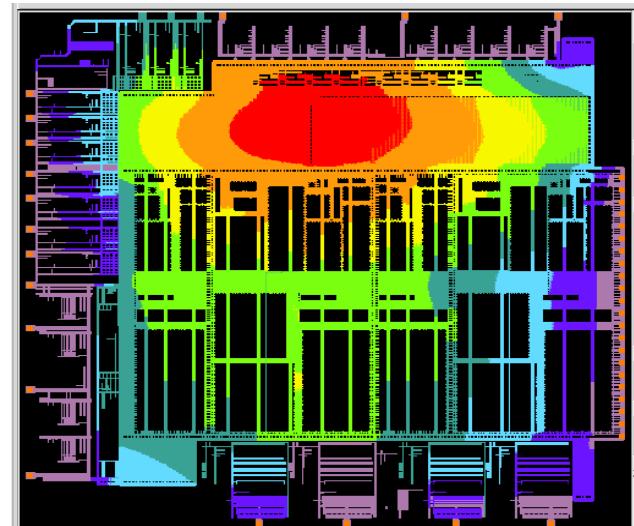
Both Power and Ground Nets solved simultaneously

Viewing Voltage Drop Map for Wires

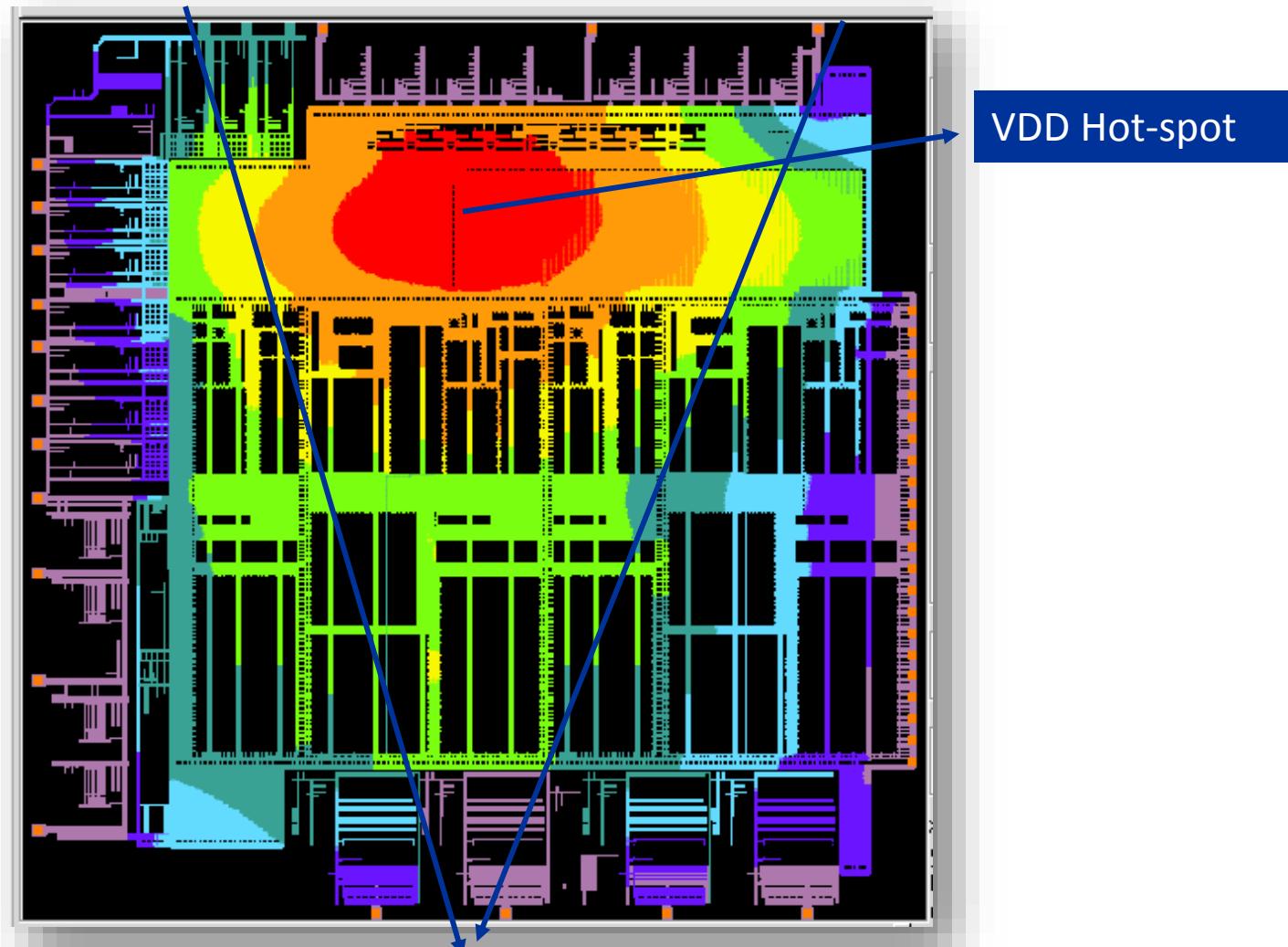
View > Voltage Drop Maps > Wire&Via



Use View -> Nets Menu for selecting individual nets



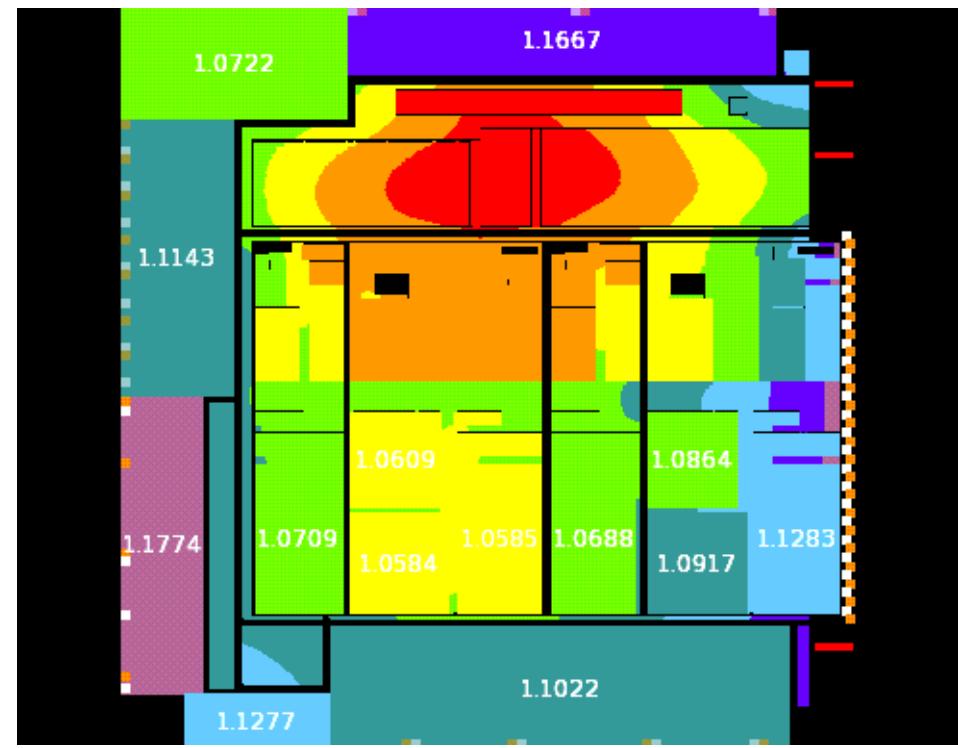
Debugging Voltage Drop



Drop is due to inadequate number of pads at the corner and at the top

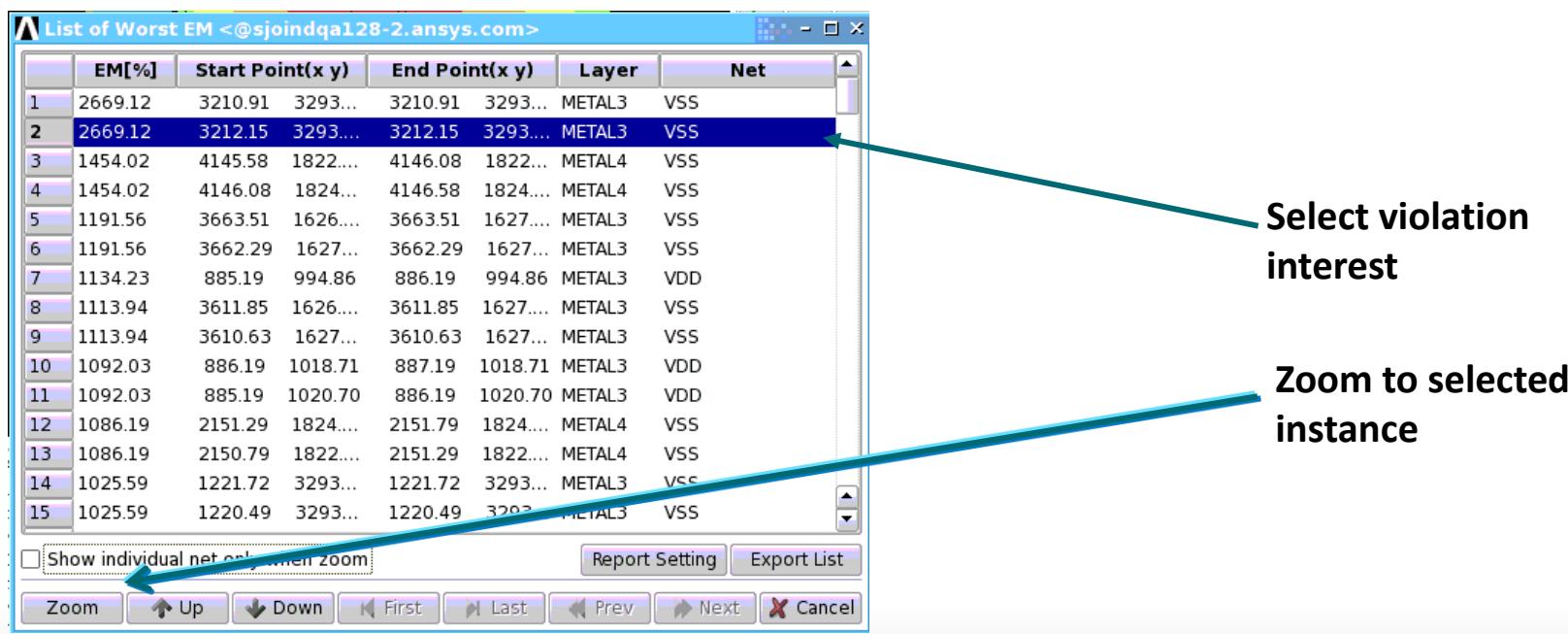
Viewing Voltage Drop Map for Instances

View > Voltage Drop Maps > Instance



Violations Browsing

- **Purpose:** Enables browsing of IR,EM violations
- **View report**
 - Results → List of Worst IR Instances for Static Simulation
 - Results → List of Worst EM for Static Simulation
 - Results → List of Worst IR for Wire & Via for Static Simulation
 - Results → List of Highest Power Instances for Static Simulation



	EM[%]	Start Point(x y)	End Point(x y)	Layer	Net
1	2669.12	3210.91	3293...	3210.91	VSS
2	2669.12	3212.15	3293....	3212.15	VSS
3	1454.02	4145.58	1822....	4146.08	VSS
4	1454.02	4146.08	1824...	4146.58	VSS
5	1191.56	3663.51	1626....	3663.51	VSS
6	1191.56	3662.29	1627...	3662.29	VSS
7	1134.23	885.19	994.86	886.19	VDD
8	1113.94	3611.85	1626....	3611.85	VSS
9	1113.94	3610.63	1627...	3610.63	VSS
10	1092.03	886.19	1018.71	887.19	VDD
11	1092.03	885.19	1020.70	886.19	VDD
12	1086.19	2151.29	1824....	2151.79	VSS
13	1086.19	2150.79	1822....	2151.29	VSS
14	1025.59	1221.72	3293...	1221.72	VSS
15	1025.59	1220.49	3293...	1220.49	VSS

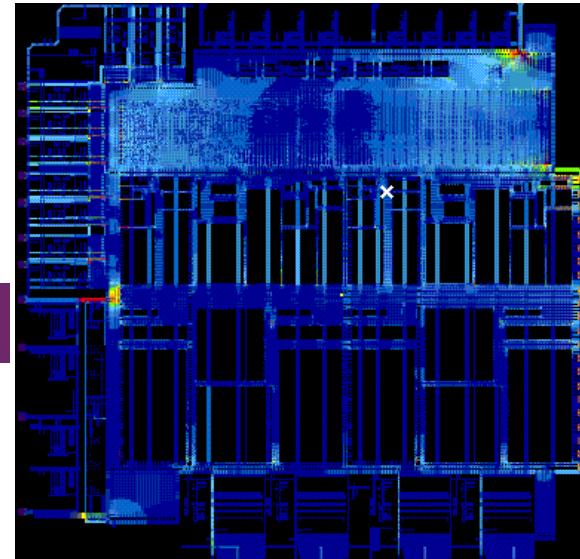
Select violation interest

Zoom to selected instance

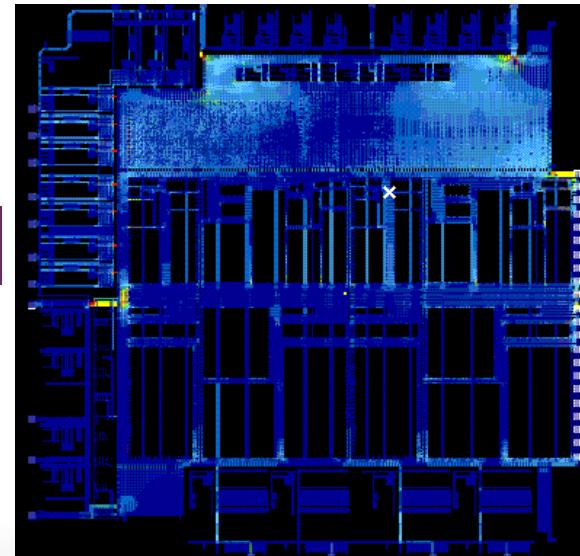
Zoom Up Down First Last Prev Next Cancel

Example – EM Issues

	EM[%]	Start Point(x y)	End Point(x y)	Layer	Net
1	2669.12	3210.91 3293...	3210.91 3293...	METAL3	VSS
2	2669.12	3212.15 3293....	3212.15 3293....	METAL3	VSS
3	1454.02	4145.58 1822....	4146.08 1822...	METAL4	VSS
4	1454.02	4146.08 1824...	4146.58 1824....	METAL4	VSS
5	1191.56	3663.51 1626....	3663.51 1627....	METAL3	VSS
6	1191.56	3662.29 1627...	3662.29 1627...	METAL3	VSS
7	1134.23	885.19 994.86	886.19 994.86	METAL3	VDD
8	1113.94	3611.85 1626....	3611.85 1627....	METAL3	VSS
9	1113.94	3610.63 1627...	3610.63 1627...	METAL3	VSS
10	1092.03	886.19 1018.71	887.19 1018.71	METAL3	VDD
11	1092.03	885.19 1020.70	886.19 1020.70	METAL3	VDD
12	1086.19	2151.29 1824....	2151.79 1824....	METAL4	VSS
13	1086.19	2150.79 1822....	2151.29 1822....	METAL4	VSS
14	1025.59	1221.72 3293...	1221.72 3293...	METAL3	VSS
15	1025.59	1220.49 3293...	1220.49 3293...	METAL3	VSS



VDD



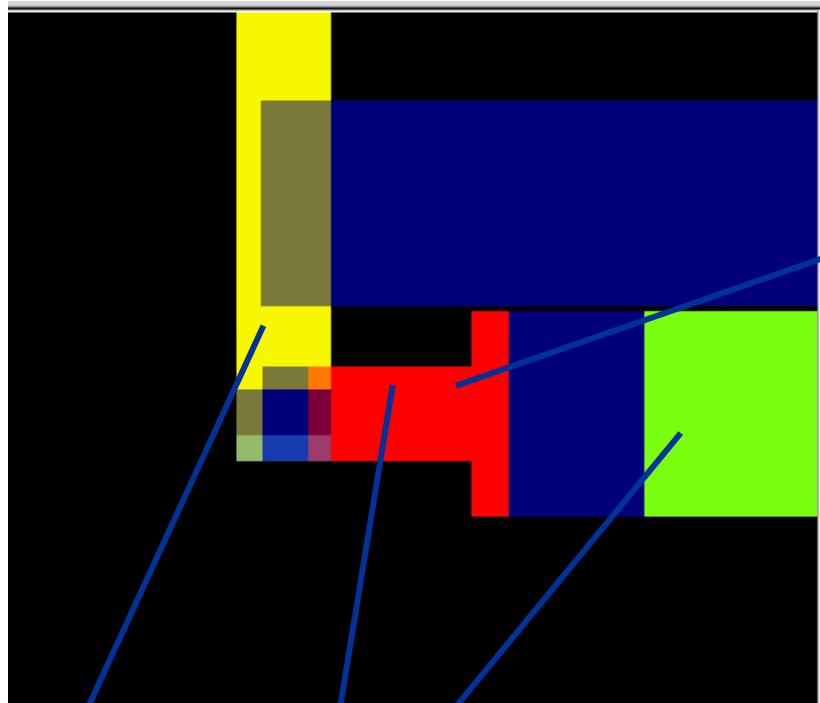
VSS

Less false EM violations due to accurate prediction of current direction

Debugging EM Violations

GUI> zoom rect 1500 4480 1600 4500

Highlight only METAL5 and METAL6, then click on the EM map button



METAL6

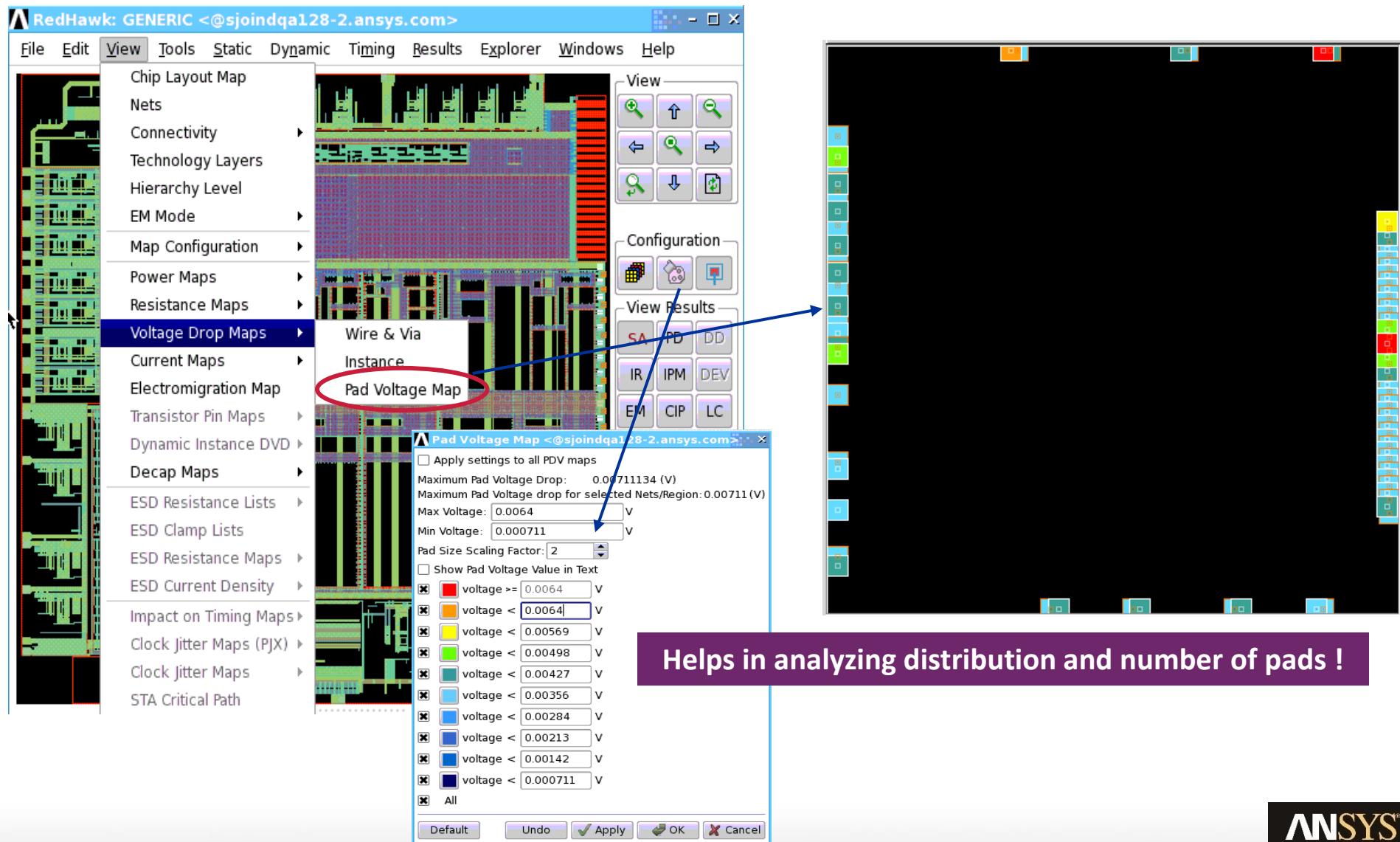
METAL5

EM violation is caused due to narrowing of METAL5

The EM limit for METAL6 is very high compared to METAL5, hence there is no violation

Pad Voltage Map

View > Voltage Drop Maps > Pad Voltage Map



Static Analysis Reports

In adsRpt/Static/

GENERIC.inst.worst GENERIC.inst GENERIC.inst.arc	Instance voltage drop
GENERIC.ir.worst <i>GENERIC.ir(Use tcl command: report ir -routing -o adsRpt/Static/GENERIC.ir)</i>	Wire voltage drop
GENERIC.em.worst	List of EM violations
pad.current	DC current through each voltage source

Result Exploration using RedHawk Explorer

Summary Section

RedHawk™-Explorer

ANSYS

Summary Data Integrity Design Weakness Hotspots Performance

Back Forward 3D-IC FAQ

Design Summary Results Summary

Power Summary Static Voltage Drop Summary Dynamic Voltage Drop Summary Current w/f Summary Power EM Summary Signal EM Summary PathFinder Summary Low Power Analysis Summary CPM Summary

Run Details

Design Statistics

Key Parameters	
Design Name	GENERIC
Design Size	4920.62u x 5000.36u
Instance Count	476302
No of Voltage domains	2(Power) & 1(Ground)
Total Power	0.75 W
Dominant Frequency	390.62 MHz
Temperature	Details
Min Supply Voltage	1.2 V

Chip Layout



Power Summary

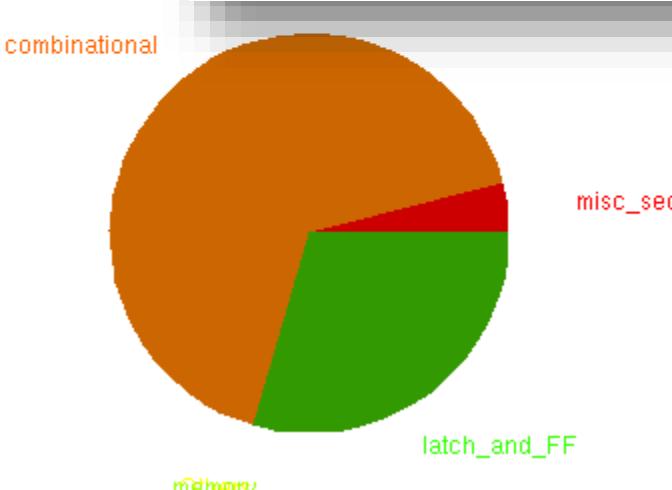
RHE Summary > Power Summary

Power Summary

- Total Chip Power calculated: 0.75 W [Details](#)

Cell Type	Frequency	Voltage Domain	Power C
misc_seq	4.0 %		
combinational	65.6 %		
Others	0.8 %		
memory	0.0 %		
latch_and_FF	29.6 %		

Power Data



Celltype	Power
misc_seq	4.0 %
combinational	65.6 %
Others	0.8 %
memory	0.0 %
latch_and_FF	29.6 %

RHE Summary > Power Summary > Power Summary Report

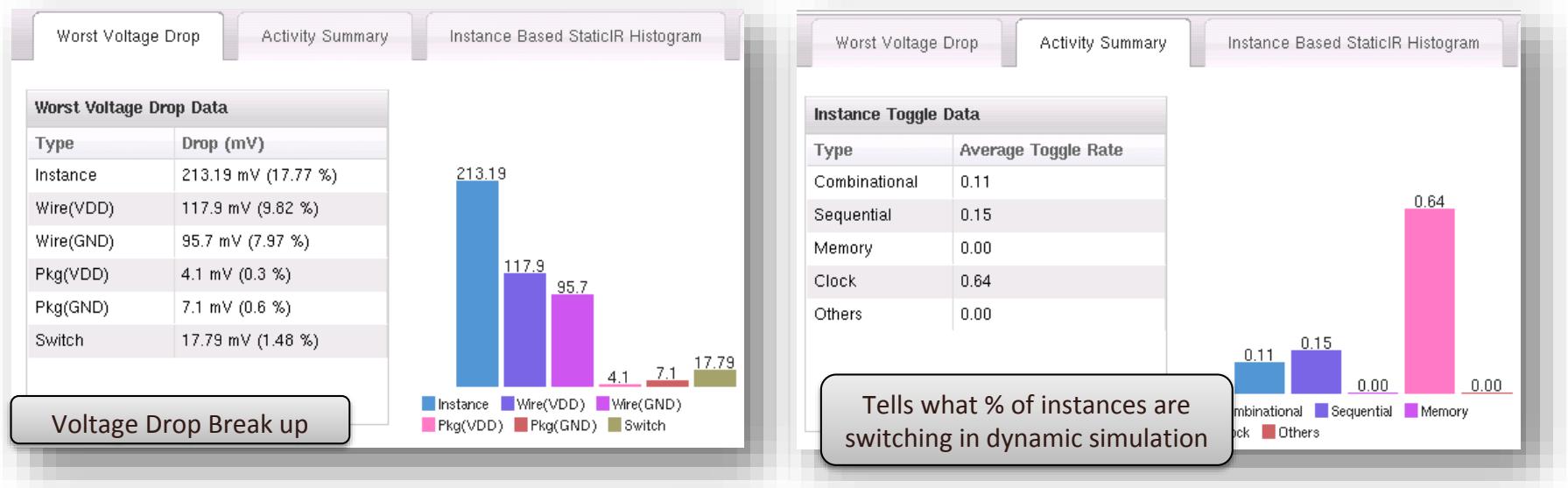
Power Summary Report

Recommended dynamic simulation time, 2560psec ,to include 98.2581% of total power for DYNAMIC_SIMULATION_TIME in GSR

Power of different frequency (MHz) domain in Watt:

Frequency	total_pwr	leakage_pwr	internal_pwr	switching_pwr	%_total_pwr
7.8125e+02	4.6938e-01	1.1897e-04	1.3589e-01	3.3338e-01	6.2584e+01
3.9062e+02	2.6755e-01	2.4451e-04	1.5310e-01	1.1421e-01	3.5674e+01
2.5000e+01	7.3277e-03	2.4365e-05	6.6499e-03	6.5344e-04	9.7703e-01
4.1667e+01	4.0091e-03	5.9996e-06	1.6939e-03	2.3092e-03	5.3455e-01
2.0000e+01	1.7178e-03	6.0175e-06	1.5939e-03	1.1782e-04	2.2904e-01
0.0000e+00	9.8109e-06	9.8109e-06	0.0000e+00	0.0000e+00	1.3081e-03

Static Analysis Summary



Data Integrity Check Summary

Summary **Data Integrity** Design Weakness Hotspots Performance

◀ Back Forward ▶ 3D-IC

Library Data

APL Current Check	✓
APL Cap Check	✗
APL Pwcap Check	
LIB Check	✓
LEF Check	✓
CMM Check	
Gds2def Check	✗

Design Data

DEF Check	✗
SPEF Check	✓
IPF Check	
STA Check	✓
VCD Check	

RedHawk Data

GSR Tcl Check	✗
Package Settings	✓
PAD_FILES	✓
GSC FILE	

Log Summary

ERROR Check	✗
WARNING Check	✗

Move the mouse pointer above the table rows to highlight the corresponding violation area.

Data Integrity Summary

Analysis Summary

Input Data	Status	Summary Description
APL Current Check	✓	APL Current coverage is 99.08 %
APL Cap Check	✗	APL Cap coverage is only 17.00 %
SPEF Check	✓	SPEF coverage is 95.10 %
STA Check	✓	STA coverage is 99.21 %
LEF Check	✓	LEF coverage is 100.00 %
Gds2def Check	✗	Gds2def coverage is only 2.0 %
LIB Check	✓	LIB coverage is 98.84 %

Number Of :
1) Shorts : 0
2) Unconnected Instances : 3
3) Unconnected Wires : 15122
4) Unconnected Vias : 19574
5) Missing Vias : 84

DEF Check

Package Check

GSR Tcl Check

Pad Files Check

Violation Areas

RED cross indicates that there is a problem with this input

- Design specific data integrity check
- Helps to identify and understand impact of missing data
- Breaks design into regions and presents missing data for each region

Data Integrity Check : DEF Check

Missing Via Debug

The screenshot illustrates a CAD tool interface for performing a 'Missing Via' check. At the top, a navigation bar includes tabs for 'Shorts Check', 'Instance Unconnect', 'Wire Unconnect', 'Via Unconnect', and 'Missing Via'. The 'Missing Via' tab is currently selected.

MISSING VIAS CHECK

- Check the number of missing vias in a design is not more than 10000
- Number of missing vias Reported : 84

Highlighting Regions with Missing Via in GUI

A callout box points from the 'Missing Via' tab to a screenshot of the CAD interface. This screenshot shows a circuit board layout with several blue rectangular boxes highlighting specific regions. A tooltip indicates "Zoom In RedHawk".

RH Crossprobing Options

Below the CAD interface, a panel titled "RH Crossprobing Options" contains the following settings:

- Highlight Color: A color palette with various colored squares.
- Show in RedHawk: A checkbox that is checked.

A callout box points from the "Show in RedHawk" checkbox to the RedHawk interface, stating "User can click and zoom into RH".

RedHawk: GENERIC <@mercury>

The RedHawk interface shows a detailed circuit board layout with a white rectangular box highlighting a specific area. A white arrow points to this highlighted area. A callout box states "Exact locations highlighted with marker".

Direct zoom into RH GUI by clicking on the image

A blue arrow points from the "Show in RedHawk" checkbox to the RedHawk interface, indicating that clicking on the highlighted image will direct the user to the RedHawk GUI for further investigation.

DEF Check: Related Reports

Data Integrity » Def Check » Related Reports

Def Check

Related Output Reports

Report	Line Count	Definition
adsRpt/apache.missingVias	84	Provides a list of missing via locations in the design
adsRpt/shorts.rpt	0	Provides a list of short locations in the design
adsRpt/GENERIC.power.unused	0	Provides list of instances that are not hooked to the power network
adsRpt/GENERIC.Via.unconnect	19574	Provides list of vias belonging to the net that are physically isolated from a power source
adsRpt/GENERIC.Wire.unconnect	15122	Provides list of wires belonging to the net that are physically isolated from the driving

Data Integrity » Def Check » Related Reports » adsRpt/apache.missingVias

```
VDD METAL4 METAL3 3975.53 2474.49 -0.00523877  
VDD METAL4 METAL3 4518.32 3301.97 -0.00572753  
VSS METAL4 METAL3 4580.9 2998.95 -0.00573893  
VSS METAL5 METAL4 2227.14 941.685 -0.0060776  
VDD METAL4 METAL3 779.47 2336.18 -0.00682867  
VDD METAL4 METAL3 779.47 2358.32 -0.0071094  
VDD METAL4 METAL3 3405.7 3437.64 -0.00721896  
VDD METAL4 METAL3 3433.3 3437.64 -0.00793719  
VSS METAL5 METAL4 4517.14 1979.99 -0.00812891  
VSS METAL5 METAL4 4517.14 1962.88 -0.00814722  
VSS METAL5 METAL4 4517.14 1935.28 -0.00817344  
VSS METAL5 METAL4 2522.34 1935.28 -0.00854228
```

Design Weakness Checks Summary

RedHawk™-Explorer

Summary Data Integrity **Design Weakness** Hotspots Performance

Back Forward 3D-IC FAQ

VRM/Package Checks

Pad Placement Quality	✗
Package Drop Contribution	✗

PDN Related Checks

PG Resistance Distribution	✗
PG Resistance Imbalance	✗
Switch Placement Quality	✓
Decap Distribution	

Current Related Checks

Power Distribution Quality	✗
Clock Buffer Clustering	✓

Design Weakness Summary

Analysis Summary

Parameter	Summary Description
<input type="checkbox"/> POWER DISTRIBUTION QUALITY	Percentage of violating regions : 2/329 (0 %)
<input checked="" type="checkbox"/> PAD PLACEMENT QUALITY	Percentage of violating regions : 5/44 (11 %)
<input checked="" type="checkbox"/> PG RESISTANCE DISTRIBUTION	Percentage of violating regions : 42/304 (13 %)
<input checked="" type="checkbox"/> PG RESISTANCE IMBALANCE	Percentage of violating regions : 55/86 (63 %)
<input type="checkbox"/> PACKAGE DROP CONTRIBUTION	Worst Package Drop For Power Domain : 4.1 mV (0 %) Worst Package Drop For Ground Domain : 7.1 mV (0 %)

Move the mouse pointer above the table rows to highlight the corresponding violation area.

- Ranks Different Regions in the design for Various Design Weakness Parameters
- Identifies Regions Affected with Design Quality Issues

Design Weakness Analysis Example

PG Resistance Distribution Check

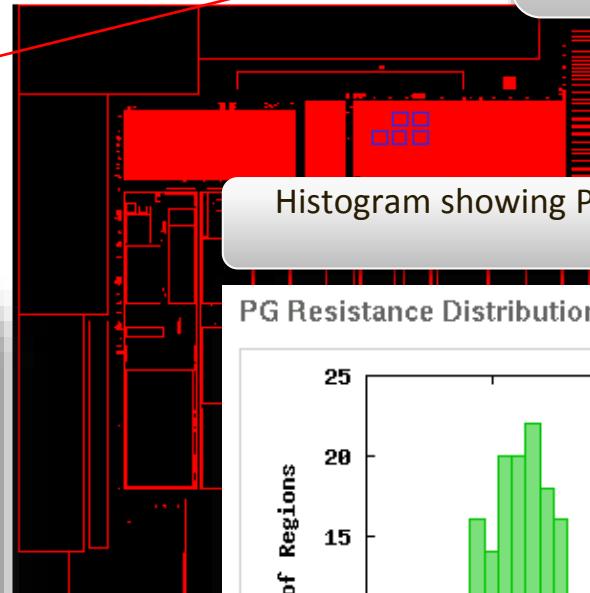
PG Resistance Distribution Check

- Checks whether the PG Resistance in any region is greater than 2 times Average PG Resistance(24.3)
- Number of Regions with Violations : 42/304 (13.81 %)

Top Violations

Region	PG Resistance Ratio	Zoom	Details
1	2.94	 Details	
2	2.91	 Details	
3	2.86	 Details	
4	2.85	 Details	
5	2.84	 Details	

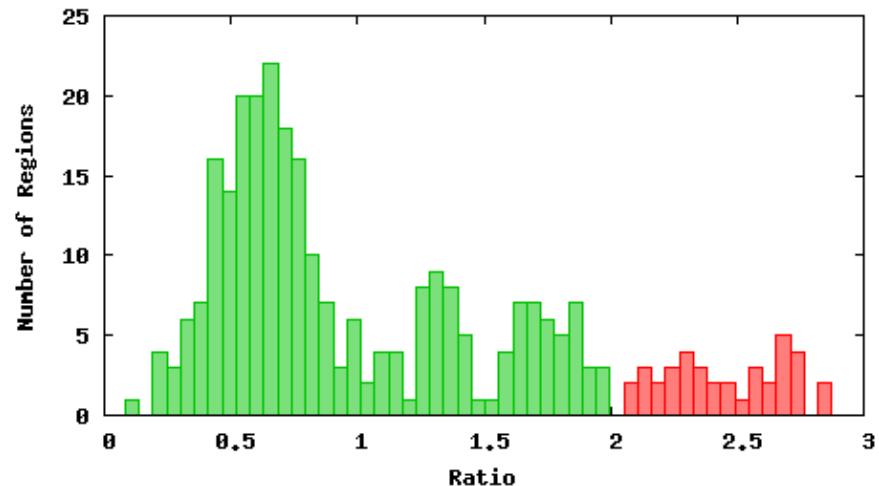
Issues Highlighted in GUI



Indicates that PG Resistance in this region is **2.94 X** higher than the average PG Resistance obtained from all regions

Histogram showing PG Resistance distribution in different regions

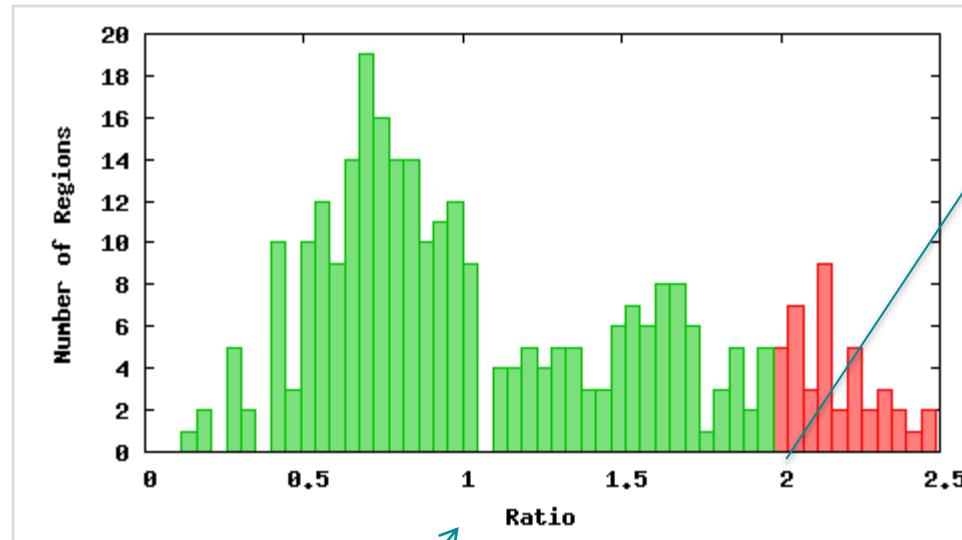
PG Resistance Distribution Histogram



Changing the constraints on-the-fly through cross-probing menu

Interpreting Histograms in RHE

PG Resistance Distribution Histogram



Simple interpretation:
Ratio 2 means this region is 2X weaker
than other part of the design

How is this ratio computed in this example ?

- STEP-1 : RHE computes the peak resistance for each region (REGION-R)
- STEP-2 : Average resistance across all the regions is computed (AVG-R)
- STEP-3 : PGR Design Weakness Ratio for each region is computed as $\text{REGION-R}/\text{AVG-R}$

Cross-probing violations in RedHawk GUI

PG Resistance Distribution Check

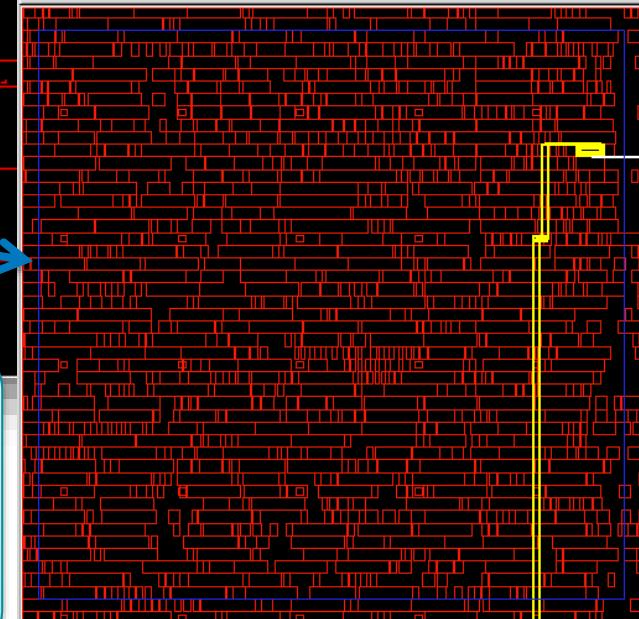
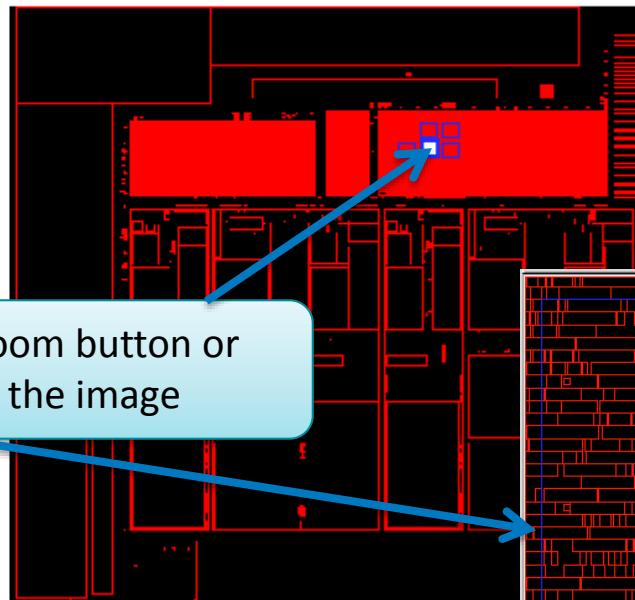
- Checks whether the PG Resistance in any region is greater than 2 times Average PG Resistance(24.350 ohm)
- Number of Regions with Violations : 42/304 (13.81 %)

Top Violations

Region	PG Resistance Ra	Zoom	Details
1	2.94		Details
2	2.91		Details
3	2.86		Details
4	2.85		Details
5	2.84		

Move the mouse pointer to highlight the corresponding region

Issues Highlighted in GUI



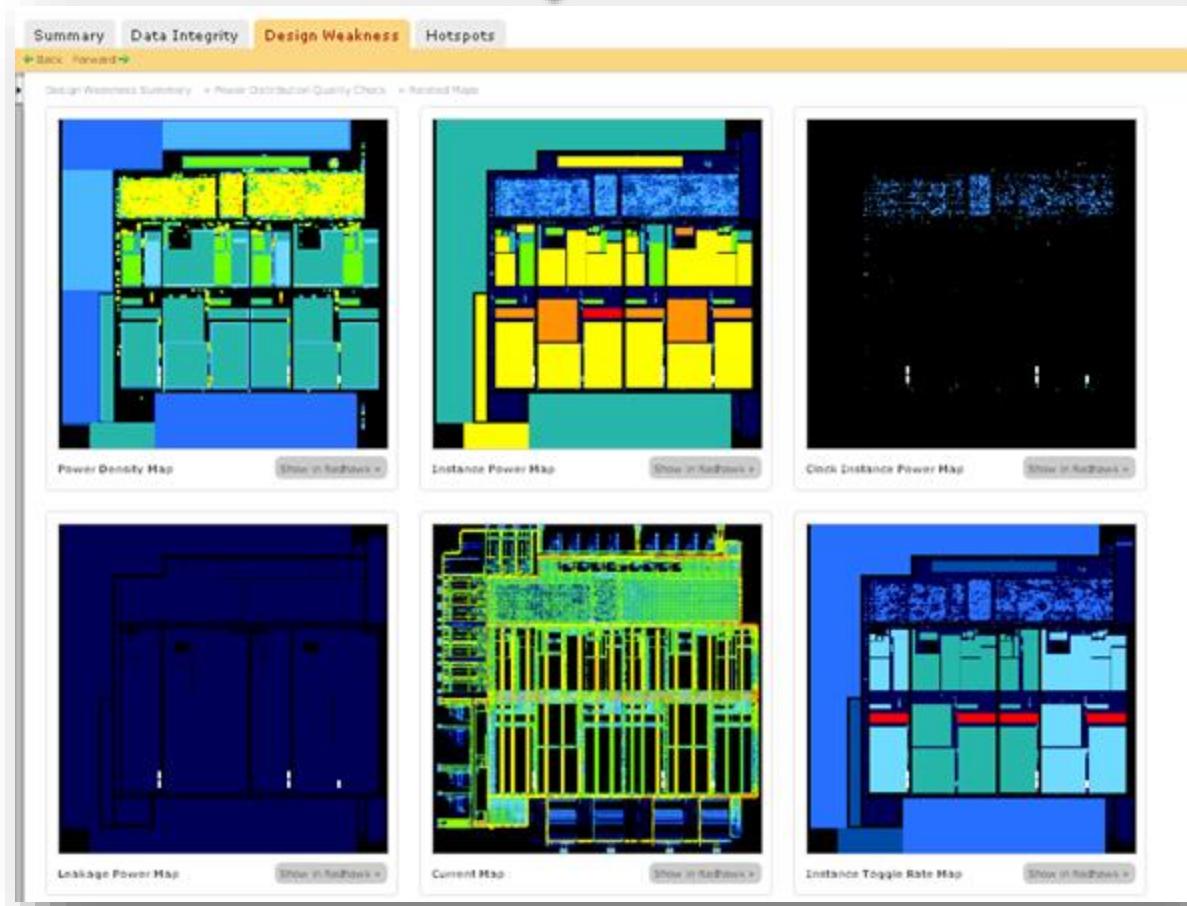
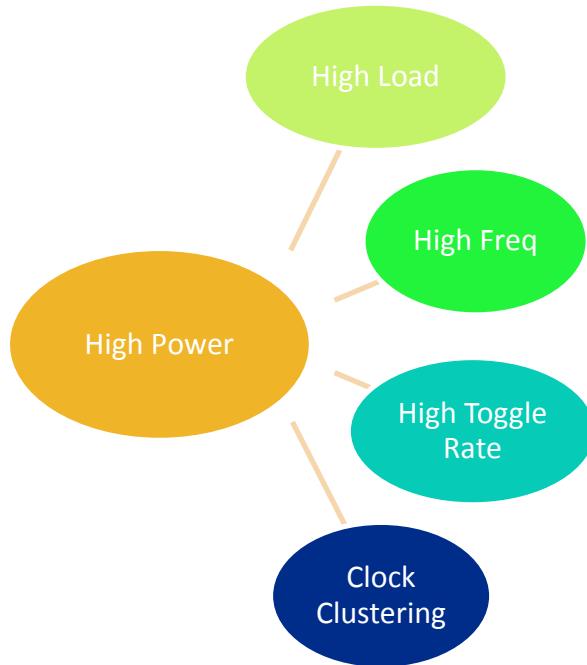
When you click on the image, RH/RHE does 3 things:

- Zooms into the violating regions
- Highlights the worst instance within the regions
- Update the map with some relevant views
 - Example, PG resistance map will display SPT for the worst instance

Design Weakness Analysis

Related Maps Section

Design Weakness -> Power Distribution Quality -> Related Maps



Related maps section helps identifying the exact cause for a weakness

Hotspot Analysis Summary

Summary Data Integrity Design Weakness **Hotspots** Performance

Back Forward 3D-IC FAQ

Dynamic Voltage Drop Check

Static IR Check X

Power EM Check X

Signal EM Check

RMS

Avg

Peak

Max Cap Check

Memory Check

DVD Check

Static IR Check

Power EM Check

Low Power Check

Voltage & Current w/f

Differential Voltage Check

Noise Coupling Check

Switch Id-sat Check

Switch Off State Check

CPM

GSR/Tcl Settings

Average Current Check

FFT Check

HotSpot Summary

Analysis Summary

Parameter	Summary Description
<input type="checkbox"/> Dynamic Voltage Drop Check	Check Not Performed
■ Static IR CHECK	Worst Static Drop : 213.19 mV
■ Power EM CHECK	Worst EM violation : 1523.20 %
<input type="checkbox"/> Low Power CHECK	Check Not Performed

Move the mouse pointer above the table rows to highlight the corresponding Hotspots

Violation Areas



Static IR Check : Summary

Summary Data Integrity Design Weakness **Hotspots** Performance

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Differential Voltage Check

Noise Coupling Check

Switch Id-sat Check

Switch Off State Check

CPM

ESR & L-Sim

Hot Spot Summary » Static IR Check

Static IR Check ?

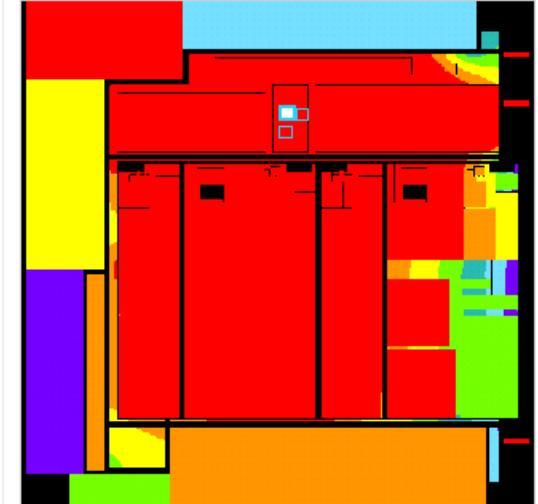
- Static IR Hot Spot Exploration
- Highlighting Top 3 Static IR Hot spots in the design
- Static IR Threshold used for PASS/FAIL : 100 mV

Number of failing regions : 245/304 (80.59 %)

Number of failing instances : 80156/80878 (99.1073 %)

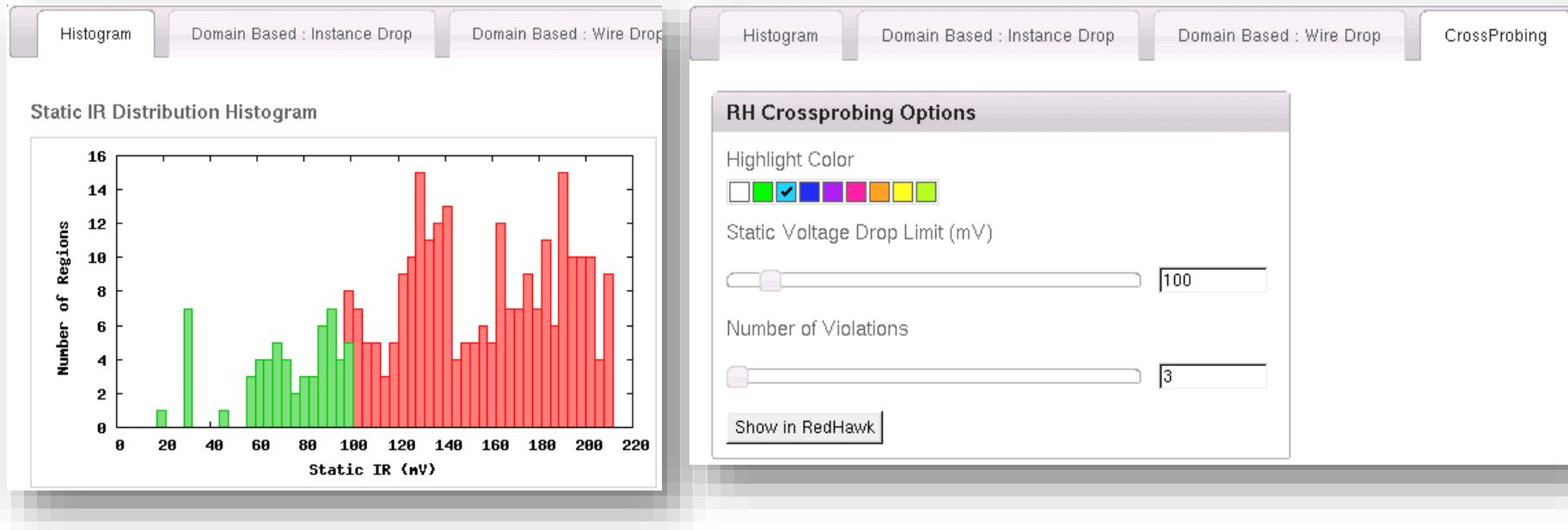
Top Violations

Region	Drop (mV)	Failed Instances	Status
Hot Spot : 1	213.19 (17.77 %)	845/845 (100.0 %)	X
Hot Spot : 2	213.03 (17.75 %)	548/548 (100.0 %)	X
Hot Spot : 3	212.78 (17.73 %)	794/794 (100.0 %)	X



Show in RedHawk »

Static IR Check : Summary



Histogram Domain Based : Instance Drop Domain Based : Wire Drop

Voltage Domain Based Hot spot Exploration

Domain	Failed Instances	Max Drop in mV(%)	Status
inst_129973/VDD_	40971/40971	202.73 (16.89 %)	✗
VDD	39185/39907	213.19 (17.77 %)	✗

Histogram Domain Based : Instance Drop Domain Based : Wire Drop

Voltage Domain Based Hot spot Exploration

Domain	Max Drop
VDD	117.943 mV
inst_129973/VDD_	108.496 mV

Static IR Check

Checking Hot-spot #1

Top Violations

Region	Drop (mV)	Failed Instances	Status
Hot Spot : 1	213.19 (17.77 %)	845/845 (100.0 %)	✗
Hot Spot : 2	213.03 (17.75 %)	548/548 (100.0 %)	✗
Hot Spot : 3	212.78 (17.73 %)	794/794 (100.0 %)	✗

Hot Spot Summary » Static IR Check » Hotspot : 1

Static IR Check [?](#)

- Static IR Hot Spot Exploration inside HOT SPOT : 1
- Hot spot region : 2490.9 3819.56 2669.38 3985.61
- Region ID : 552
- Instance Threshold used for PASS/FAIL : 100 mV

- Number of instances failing : 845/845 (100.0 %)
Displaying Top 1 instances inside this HOT SPOT

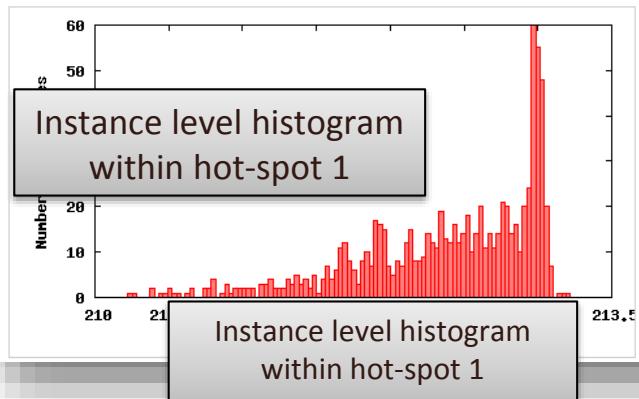
Instance	DROP (mV)	Status
Hot Instance : 1	213.19 (17.77 %)	✗

Root Cause : Design Weakness

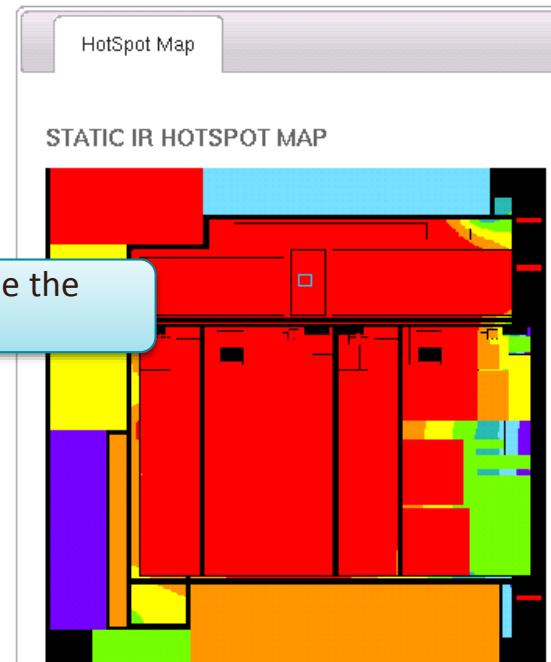
Root Cause : Data Integrity

Histogram

Static IR Drop Histogram inside Region : 1



Detailed analysis inside the region



Root Cause Identification

Design Weakness Analysis

Root Cause : Design Weakness Root Cause : Data Integrity Histogram

Indicates that this hot-spot region has power issue

Root Cause : Design Weakness

Check	Status	Value	Ratio	Rank
POWER DISTRIBUTION QUALITY	✗	Total Power = 0.006641 W	4.08	8/662
PAD PLACEMENT QUALITY	✓	Current from nearest pad of Domain VSS : -11.55 mA Current from nearest pad of Domain VDD : 5.75 mA	NA	NA
CLOCK BUFFER CLUSTERING CHECK	✗	Total Clock Power = 0.002012 W	2.16	8/105
PG RESISTANCE DISTRIBUTION	✗	Max Instance Resistance = 1.18 Ohm	1.18	54/662
PG RESISTANCE IMBALANCE	✓	Max Res Imbalance Ratio = 1.12	1.12	82/662

*These checks are not for this hot bucket but they belong to the entire design

Design Weakness Ranking

This hot-spot region ranks 8th among all regions in the design based on
Power Distribution Quality Ranking
(Rank-1 indicates the weakest region)

Static IR Check

Instance Level Debug

Instance	DROP (mV)	Status
Hot Instance : 1	213.19 (17.77 %)	X

[static_ir_hotinst-1](#)

Hot Spot Summary » Static IR Check » Hotspot : 1 » Hot Instance : 1

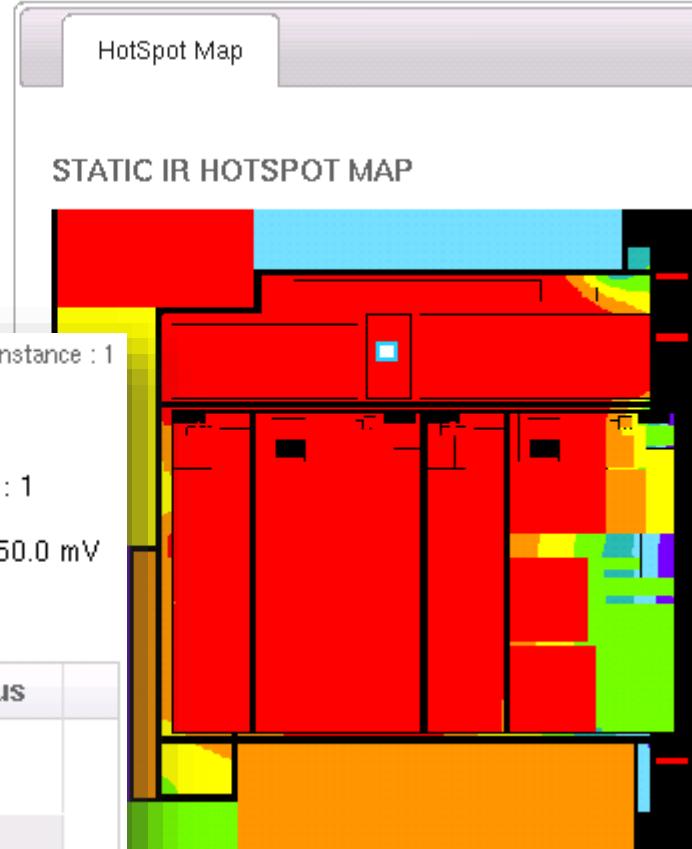
Static IR Check ?

- Static IR Hot Spot Exploration for Hot Instance : 1
- Instance : inst_129974/inst_495108
- Instance Pin Threshold used for PASS/FAIL : 50.0 mV
- Pin Based Voltage Drop Details

Pin	Domain	Drop (mV)	Status
VDD	VDD ?	117.54 (9.79 %)	Fail
VSS	VSS ?	95.64 (7.97 %)	Fail

HotSpot Map

STATIC IR HOTSPOT MAP



Static IR Check

Instance Level Debug

The screenshot displays three panels of a software interface for static IR check and instance-level debug:

- Properties:** Shows basic instance properties for cell_426.
- Data Integrity:** Shows a table of data integrity status for various checks.
- Design Weakness:** Shows a table of design weakness checks with their status, value, and rank.

Properties (Left Panel):

Cellname	cell_426
Decap	0.0227534 pF
Frequency	7.8125e+08 Hz
Fanout	1
Load	0.0962002 pF
Average Power	3.79106e-05 W
Leakage Power	5.47877e-09 W
Toggle Rate	0.583045

Data Integrity (Middle Panel):

Data	Status
ApI Current	✓
ApI Cap	✓
ApI Pwcap	NA
Lef	✓
Lib	✓
Sta	✓
Spf	✓

Design Weakness (Right Panel):

Check	Status	Value	Rank
Resistance	✓	39.6209 Ohm	1610/3824
Power	✓	3.79106e-05 W	10/3824
Load	✓	0.0962002 pF	28/3824

Static IR Check

Instance Level Debug: SPT and Resistance Report

The screenshot shows a software interface for static IR analysis. At the top, there are tabs: Properties, Data Integrity, Design Weakness, Path Tracing, and Resistance Report. The Path Tracing and Resistance Report tabs are highlighted with blue circles and arrows pointing to callout boxes.

SPT Map: A red-colored map of the chip layout, highlighting the shortest resistance path from power and ground pads to internal nodes. A yellow line highlights a specific path segment.

Path Tracing Callout: Highlights Shortest Resistance Path to P/G Pads

Resistance Report Callout:

Instance: inst_129974/inst_495108	Pin VDD	Resistance : 19.9008 Ohm	Net: VDD
Instance: inst_129974/inst_495108	Pin VSS	Resistance : 19.7201 Ohm	Net: VSS

Resistance Report Table:

Point	Resistance	Length (um)	Drop (mV)	Zoom
DVDD14	--	--	4.145	🔍
METAL4	0.010	3.46	0.620	🔍
via4Array_23_26x21_67108863_2228496	0.000	--	0.044	🔍
METAL5	0.007	6.26	0.260	🔍

Equivalent Tcl Command:

```
perform min_res_path -o res_path.rpt
```

User can directly zoom into the bottleneck segments

Power EM Check : Summary

Summary Data Integrity Design Weakness Hotspots Performance

Back Forward 3D-IC FAQ

Dynamic Voltage Drop Check

Static IR Check X

Power EM Check X

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DVD Check

Static IR Check

Power EM Check

Low Power Check

Voltage & Current wif

Differential Voltage Check

Hot Spot Summary > Power EM Check

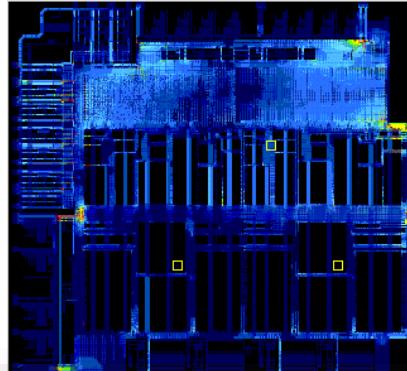
Power EM Check X

- Power EM Hot Spot Exploration
- Highlighting Top 3 Power EM Hot Spots in the design
- Power Em Threshold used for PASS/FAIL : 100 %

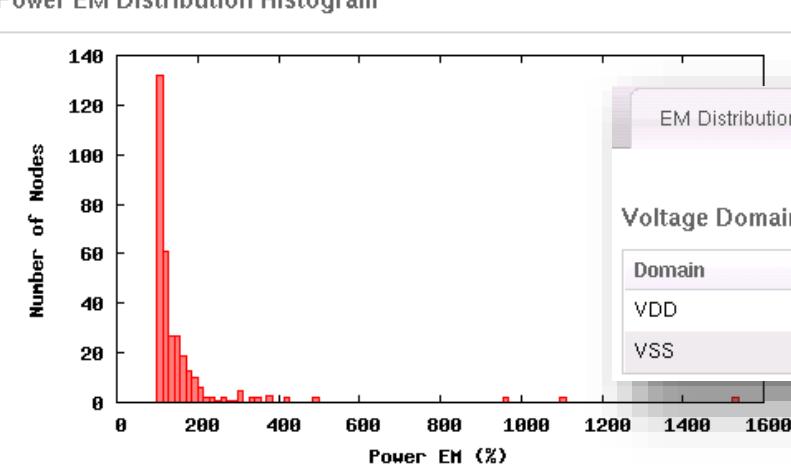
✖ Number of failing regions : 57/57 (100.0 %)
✖ Number of failing nodes : 326/1287283 (0.0 %)

Top Violations

Region	EM Percentage	Failed nodes	Status
Hot Spot : 1	1523.20	4/4	X
Hot Spot : 2	1105.35	2/2	X
Hot Spot : 3	959.86	2/2	X



Power EM Distribution Histogram



Domain	Failed Nodes	Max Em Percentage	Status
VDD	178/178	485.641	X
VSS	150/150	1523.2	X

Voltage Domain Based EM Hot spot Exploration

EM Distribution Histogram CrossProbing Domain Based

ANSYS

Power EM Check

Checking Hot-spot #1

Hot Spot Summary » Power EM Check » Hotspot : 1

Power EM Check [?](#)

- Power EM Hot Spot Exploration inside HOT SPOT : 1
- Hot spot region : 3154.950000 3154.950000 3321.000000 3321.000000
- EM Threshold used for PASS/FAIL : 100 %
- Number of nodes failing : 4/4 (100.00 %)
- Displaying Top 1 nodes inside this HOT SPOT

Node	EM Percentage	Status
Hot Node : 1	1523.20	

Hot Spot Summary » Power EM Check » Hotspot : 1 » Hot Node : 1

Power EM Check [?](#)

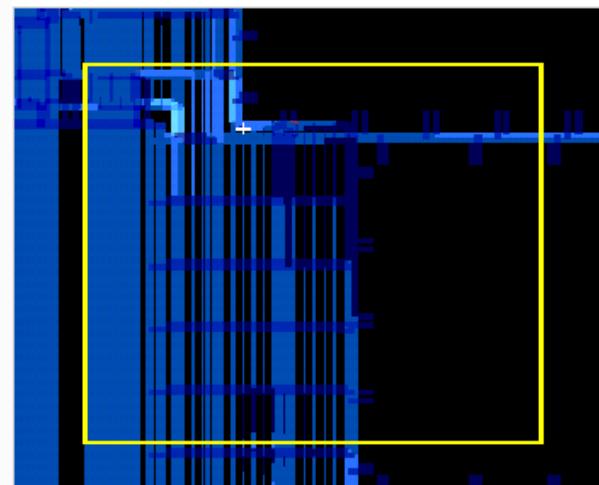
- PowerEM Hot Spot Exploration for Hot node : 1
- Node : node1

WIRE/VIA PROPERTIES

Location	3.212145e+03,3.293045e+0
Em percentage	1523.20 %
Layer	METAL3
Node Type	WIRE
Net	VSS
Width	5.000000e-01 um



EM HOTSPOT MAP ZOOMED



How to get Help!!

- Apache Online Customer Support Center
 - <http://support.apache-da.com>
 - Email: support@apache-da.com

The screenshot shows the ANSYS Apache website's support section for RedHawk. The top navigation bar includes links for PRODUCTS, FLOWS, SUPPORT, COMMUNITY, and COMPANY, along with a search bar and user authentication information. A banner at the top says "RedHawk Support". The left sidebar has a "Support" menu with "PowerArtist Support" and "RedHawk Support" selected. The main content area displays general information about RedHawk and a list of available technical resources.

ANSYS Apache

Logged in as aleena Log out

PRODUCTS FLOWS SUPPORT COMMUNITY COMPANY Search...

RedHawk Support

Home > Support

RedHawk Support

RedHawk™ is a full-chip, dynamic power analysis and sign-off solution for high-performance SoCs, including advanced low-power designs.

The following technical resources are available for the RedHawk products:

- Documentation
- Release Notes
- Known Issues
- Download Instructions
- Installation Instructions
- Quick Start Guides
- Application Notes
- Training
- Resources

Support

- + PowerArtist Support
- RedHawk Support**

Documentation

Release Notes

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Installation Instructions

Quick Start Guides

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Training

Resources

ANSYS

Thank You!!!