Fixed Frequency VLSI Phase-Locked Loop (PLL) circuit

Experiment

Design and Development of a Phase Locked Loop

A Phase Locked Loop (PLL) is a feedback control circuit that is designed to allow one circuit to synchronize the phase and frequency of a device's onboard clock with an external timing source (typically a quartz crystal that is operating at several 10's to 100's of MHZ). A PLL operates by comparing a required operating frequency with a reference source and adjusts the output to match the input phase and frequency.

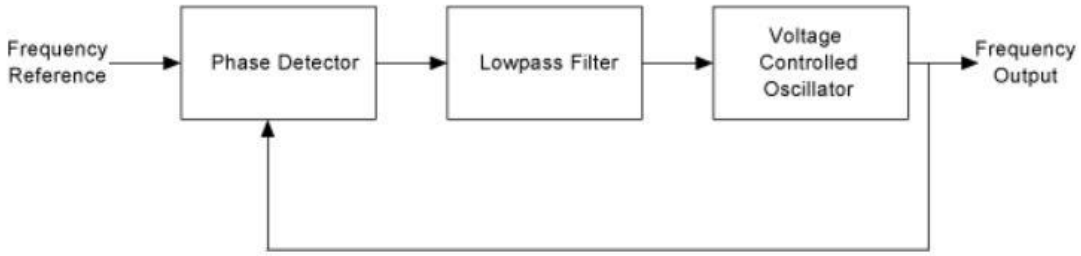

Figure.1 Basic PLL Architecture

The typical architecture comprises three main components regardless of the topology. A phase detector, a low pass filter (or loop filter) and the voltage-controlled oscillator.

- Phase and Frequency Detector (PFD): The phase frequency detector compares the frequency of two different incoming signals (A reference signal and the feedback signal) and then estimates the phase difference between the two. This phase and frequency difference is then translated to an error voltage that is proportional to the differences between the signals. The PFD is always accompanied by a charge pump, the charge pump generates a current that is switched based on the phase detector outputs (either source or sink currents). The variation in current generates a pulse width modulated signal.

- Loop Filter (or Low Pass Filter): The output of the PFD is typically a PWM (Pulse Width Modulated Signal) the basic function of the loop filter is to eliminate the frequency components and generate a pure DC signal that is proportional to the frequency and phase shifts.

- Voltage Controlled Oscillator (VCO): The Voltage controlled oscillator that generates an output signal that is then compared with the reference signal. The basic methodology behind the operation of the VCO is to generate a signal that varies in frequency and phase in accordance with the applied input or control voltage.

Features:

- Buffered outputs that allow for full CMOS swing.
- Supply Voltage operating range 1.8V +/-10%.
- Four Phase Clock Generation that is compatible with state-of-the-art CDRs and DRCs.
- Fixed Reference of 100MHz.
- Multiplied clock frequency of 800MHZ.
- Total Power Dissipation of 11.56 mW.
- Locking in time of 5us.

Development:

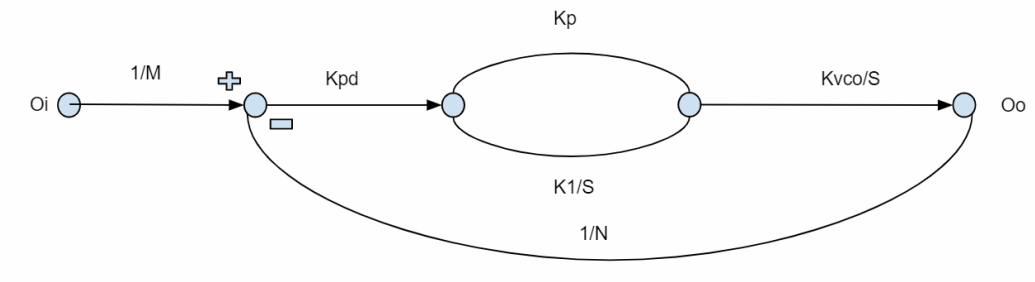

Figure.2 Second order phase domain model

The figure represents a phase domain (S-domain) model of a typical second order phase locked loop. The constants represent the performance metrics of each component that forms the overall PLL architecture.

- 1/M represents the input clock divider.
- 1/N represents the output frequency divider.
- Kpd represents the gain of the phase detector circuit.
- Kp represents the proportion constant of the loop filter.
- K1/s represents the integral component of the loop filter.
- Kvco/S represents the gain of the VCO modeled in the S-domain.

The S-domain Transfer function of the second order phase locked loop is represented as:

$$H(s) = (N/M)\ [\{(1/Q)\,S + 1\}/\{S^2 + (1/Q)S + 1\}]$$

Phase error transfer function can be modeled as:

$$He(s) = (1/M)\ [S^2/\{S^2 + (1/Q)S + 1\}]$$

❖ Natural Frequency

$$wn = (Kpd * k1 * Kvco/N)^{(1/2)}$$

❖ Damping Factor:

$$\zeta = Kp/2 * ((kpd * Kvco)/(N * K1))^{(1/2)}$$

❖ Phase Error:

$$oe = Oi/M - Oo/N$$

❖ Quality Factor:

$Q = 2 * ʒ$

Estimated Specifications:

- Wn = 5MHz.
- KVCO = 1.18G
- KPD = ICP/2*pi = 318.30u.
- $ʒ$ = 0.9

A damping factor is 0.9 is considered to ensure the control loop settles swiftly and the oscillations are suppressed, the transient step response shows this in the plots

Behavioral Modeling

The S-domain model is used to develop an approximate phase response of the PLL in the frequency domain.

Cadence Modeling

The S-Domain model of the circuit was developed to perform stability analysis on the feedback loop.

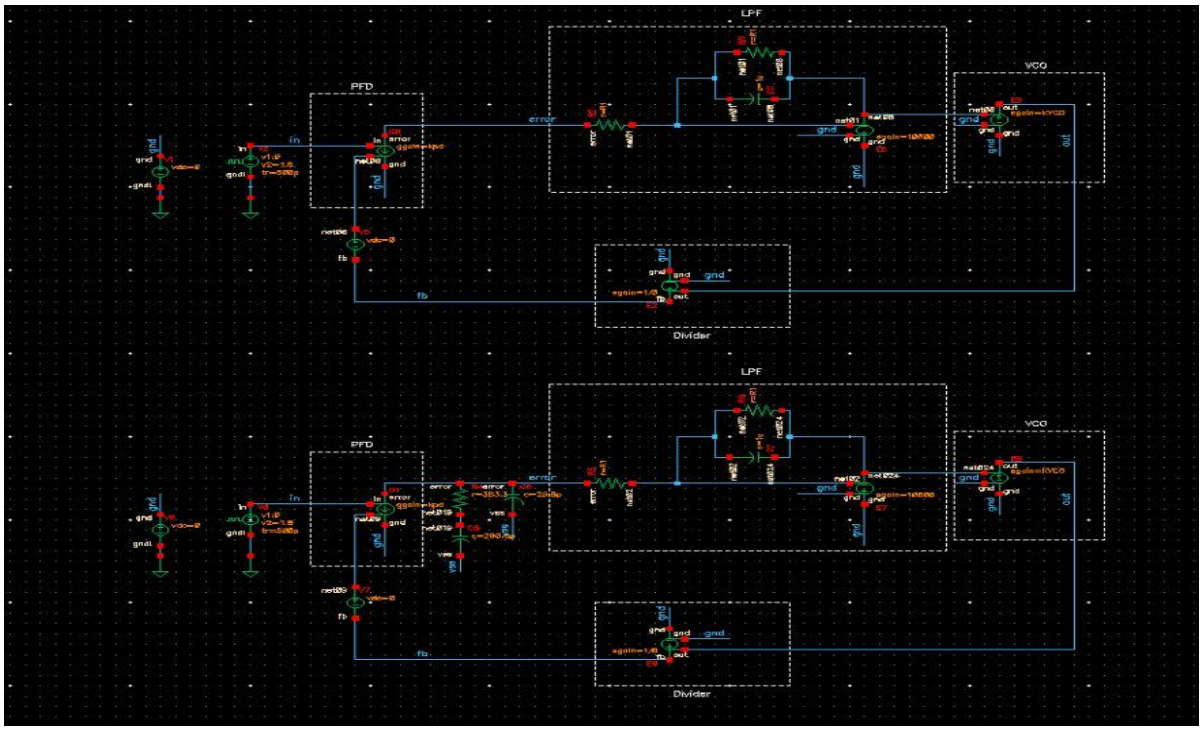

Figure.3 Second order phase domain model

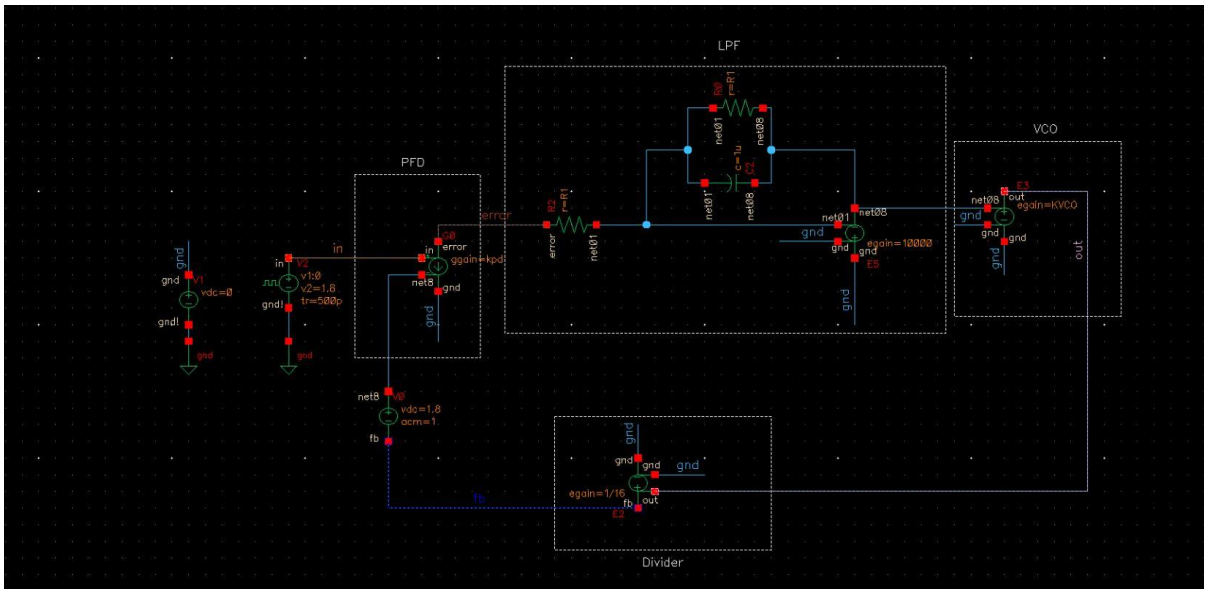

Figure.4 Second order phase domain Stability model

Simulations:

Stability Analysis:

For the Stability analysis, the loop is broken using a DC voltage source set at zero volts, the loop is then simulated from a frequency range of 1Hz to 100GHZ. The corresponding Phase Margin, Loop gain and phase are determined. These parameters are used to estimate the stability criteria of the entire loop.

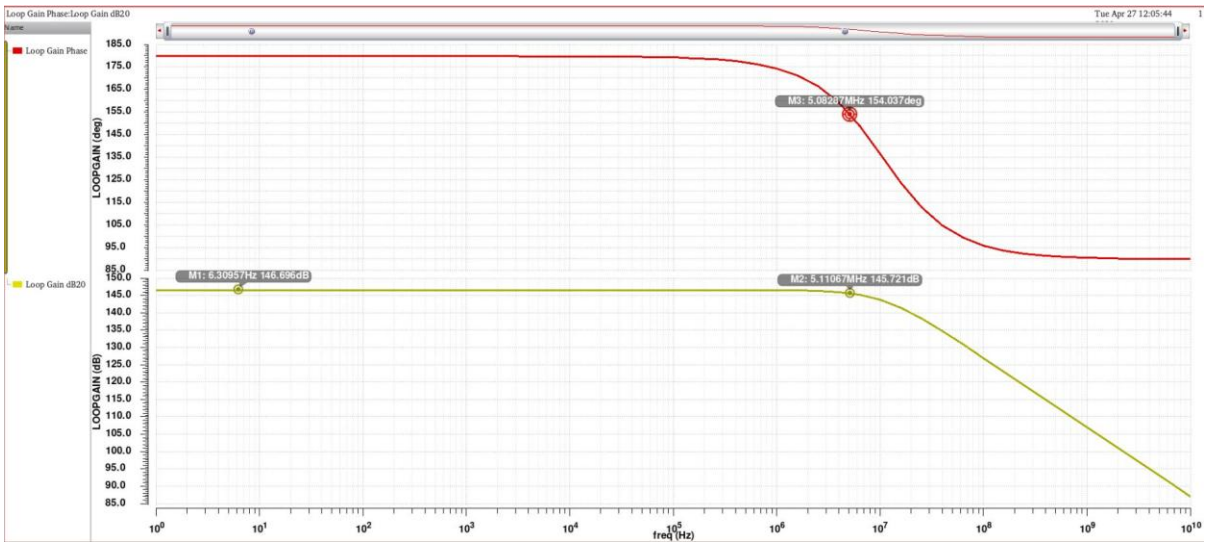

Figure.5 Second order phase domain stability response

Figure.6 Second order phase domain stability summary.

Step Response:

Step response analysis is used to determine the stability of the loop in the time domain. A simple rising step function with a large pulse width is applied to the circuit. Stability conditions like ringing, settling time, and damping factors are determined to estimate the stability of the system.

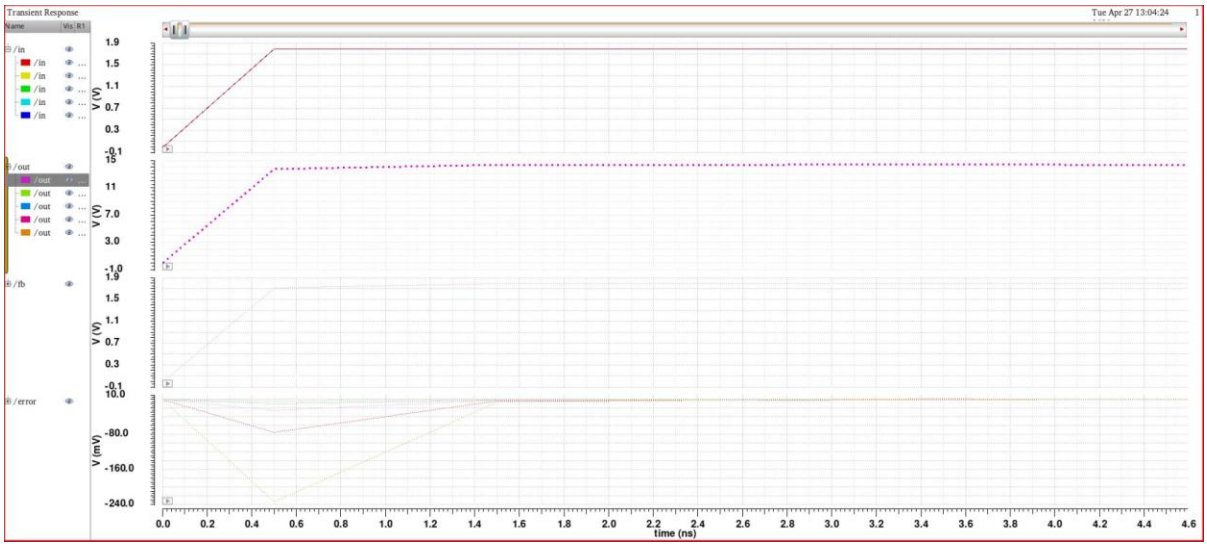

Figure.7 Second order phase domain step response analysis

Programmable Frequency Divider

Abstract:

Newer Phase locked loops can be modified to operate at several multiples of the input reference clock signals, one such technique is by dividing the output of the PLL by a required ratio to ensure the output signal is divided down to the reference frequency. This is possible by using a frequency divider, this project entails the design and development of a programmable frequency divider that divides the output frequencies of 100MHz to 1.2GHz by a factor of 8 and 10.

Specification	Unit	Value
Supply	V	1.8 +/- 10%
Process	nm	300
Input Frequency Range	GHz	0.1 - 1.2
Temperature	C	27
Process Corner	-	TT/FF/SS
Division Ratios	-	8/10

Table.1 Clock Divider Specifications

Architecture:

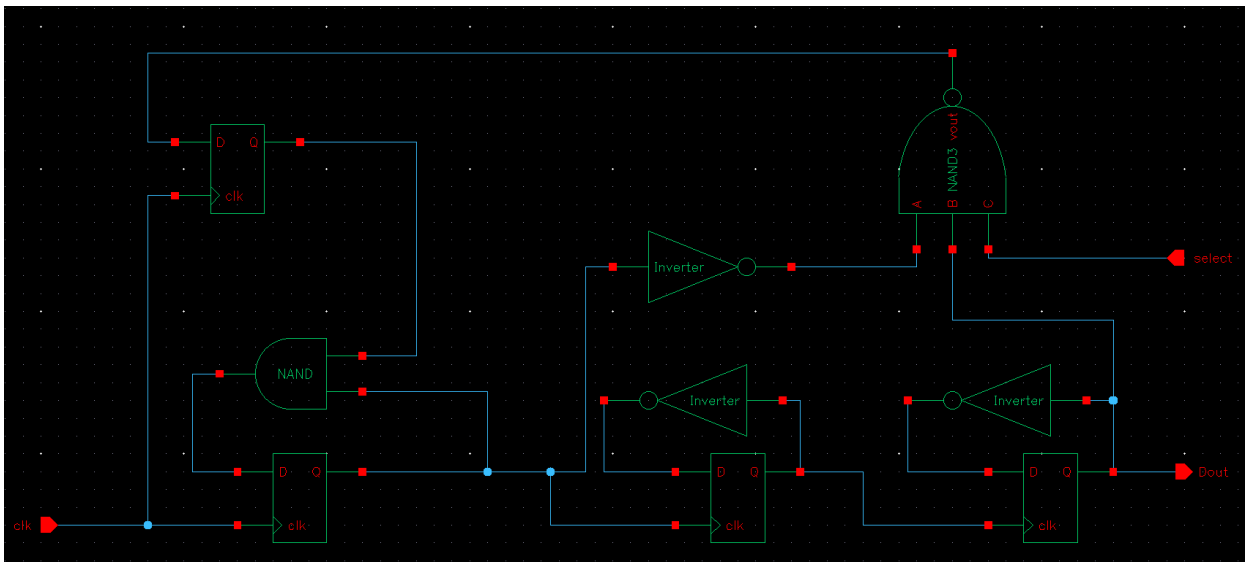

Figure.5 Frequency Divider

The architecture comprises three asynchronous counter circuits that yields a division ratio of 1/(2^n), as we employ three stages the division ratio is 1/8 of the applied input. The final flip flop is used to eliminate any misalignment or jitter that is induced by the divider circuit.

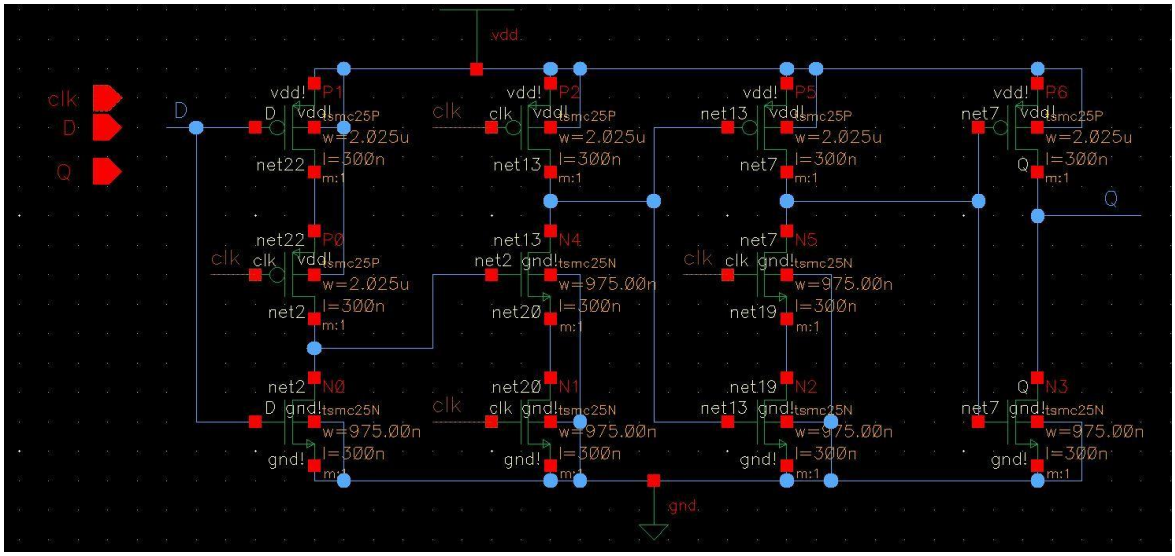

Figure.6 Flip Flop Schematic

The heart of the Divider architecture is the Flip-flop. For optimal design availability and speed, we consider the True Single-Phase Clocked Logic. The Flip-Flop is of the positive edge triggered type that reads data in at the transition from the lower to higher end of the clock. The topology is based on the Domino CMOS Logic structure to ensure High-Speed Operations by reducing the number of clock cycles, interconnects and the number of devices required to implement the logic.

Device	**Width**	**Length**
P0 - P6	3u	300n
N0 - N5	1u	300n

Table.2 TPSC Flip-Flop

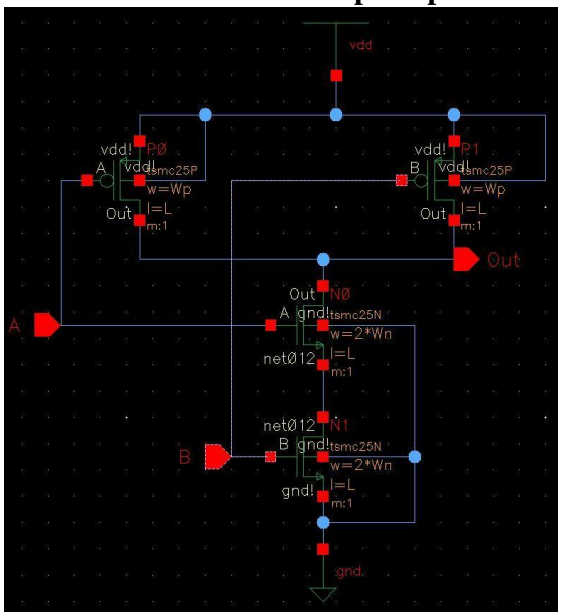

Figure.7 NAND2 Schematic

Device	Width	Length
P0 - P1	3u	300n
N0 - N1	1u	300n

Table.3 NAND2 Sizing Chart

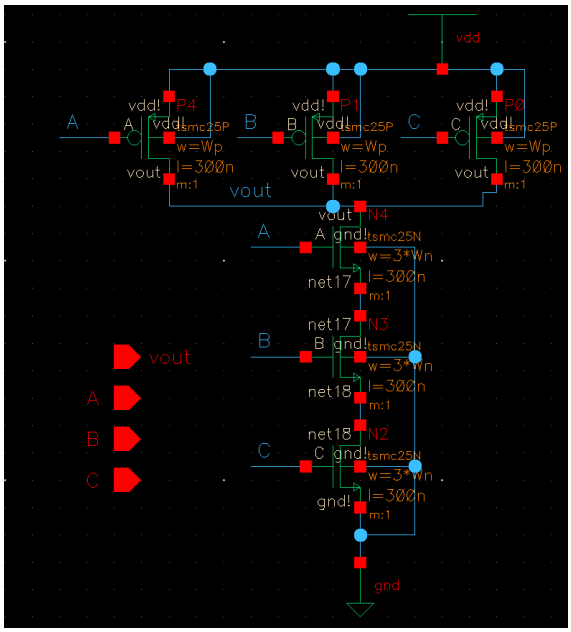

Figure.8 NAND3 Schematic

Device	Width	Length
P0 - P6	3u	300n
N0 - N5	1u	300n

Table.4 NAND3 Sizing Chart

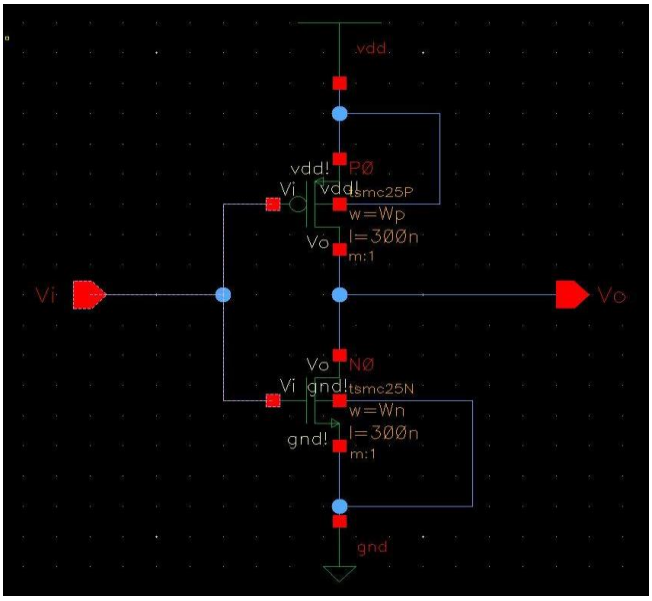

Figure.9 Inverter Schematic

Device	**Width**	**Length**
P0 - P6	3u	300n
N0 - N5	1u	300n

Table.5 Inverter Sizing Chart

- Logic Gates are sized so as to achieve the least possible rise and fall time delay.
- The NAND logic is sized by tying the most capacitive node vdd and then sizing the devices as per the least possible averaged rise and fall time delay.

Simulations:

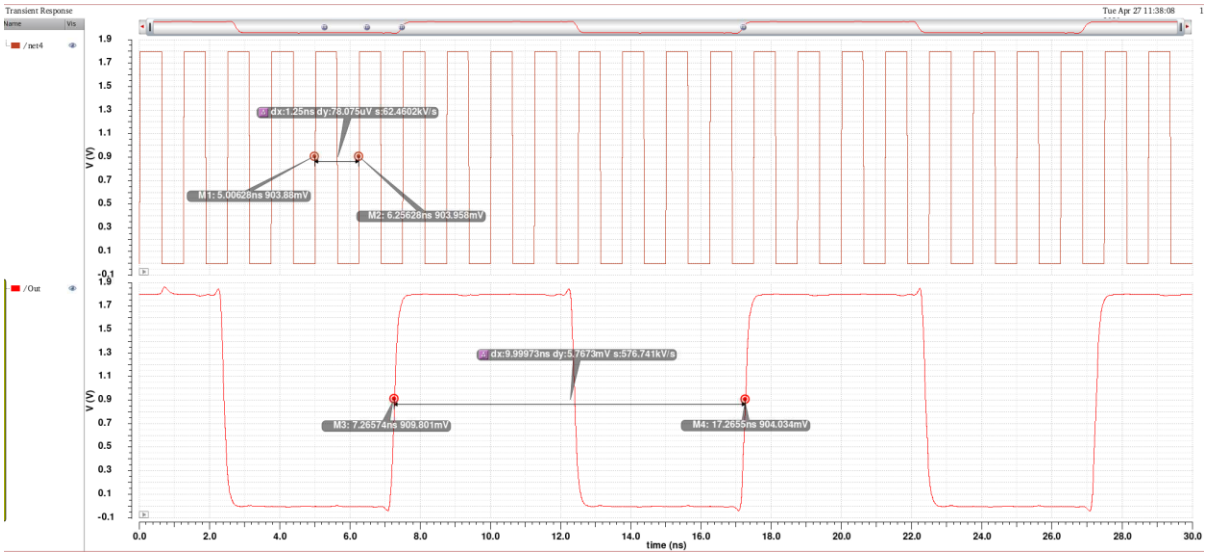

Figure.10 Divide by 8 waveform

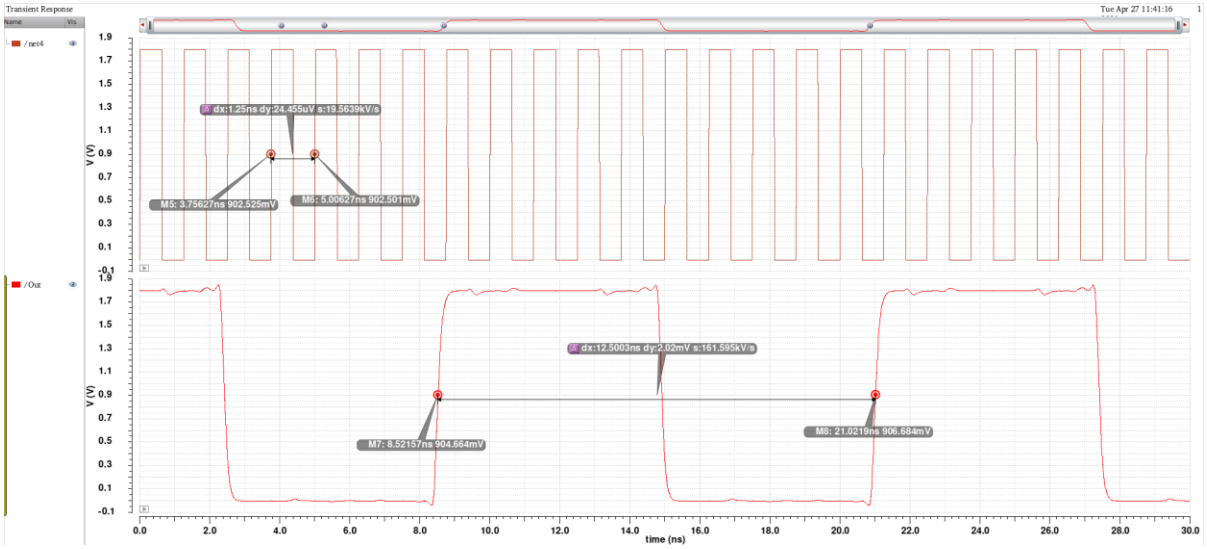

Figure.11 Divide by 10 waveform

The simulation graphs represent perfect division of the input signal by a factor of 8 when the select line is nil and factor of 10 when the select line is at VDD.

Phase Frequency Detector

Abstract:

Phase Locked loop employs the negative feedback loop that compares the phase of the reference signal to the required output that is generated by the loop, PFDs typically operate at the reference frequency ranges. The design employs the novel pre-charge PFD architecture to reduce large clock jitters and reduction in acquisition time. The device is selected to operate with a clock frequency range of 100 - 200 MHz

Specification	**Unit**	**Value**
Supply	V	1.8 +/- 10%
Process	nm	300
Input Frequency Range	GHz	0-0.2
Temperature	C	27
Process Corner	-	TT/FF/SS

Table.6 Phase Frequency Detector Specifications.

Architecture:

- The entire architecture is implemented on the 300nm process node operating at a supply of 1.8V.
- The employed architecture is based on the 0 -phase offset architecture.
- The gain of the PFD is estimated as follows:
  $K = vdd/(4 * pi)$
  $K = 143\ (mV/rad)$
- The proposed architecture is designed to eliminate the dead zone, at the cost of power draw and larger jitter.

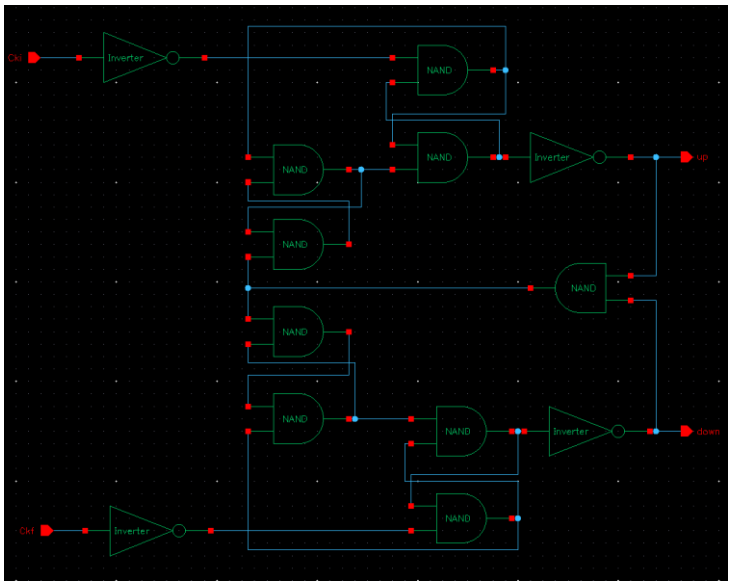

Figure.12 PFD Schematic

Simulations:

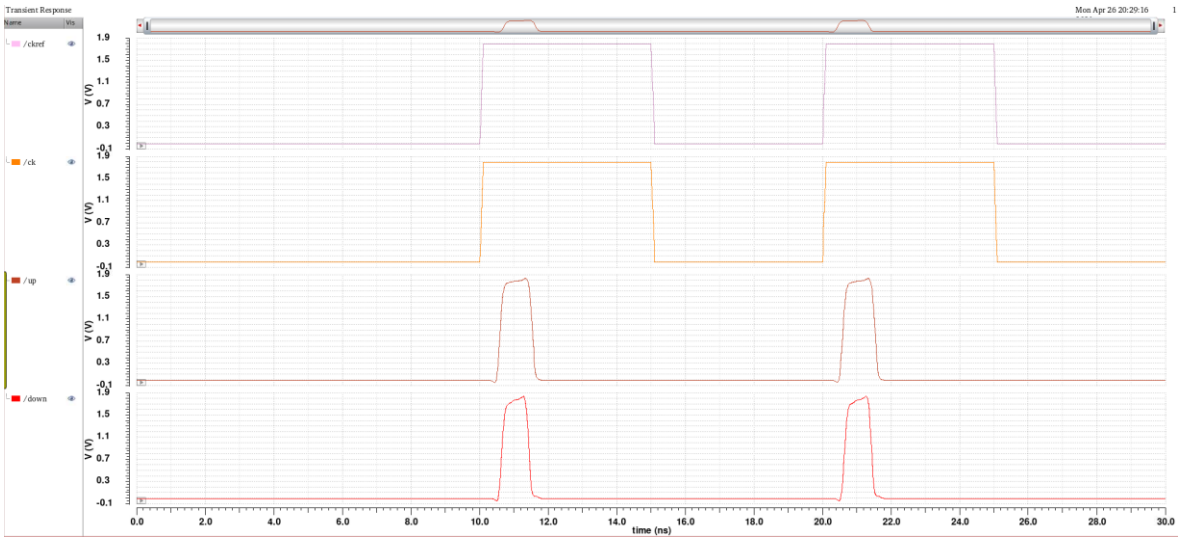

Figure.13 In-phase waveforms

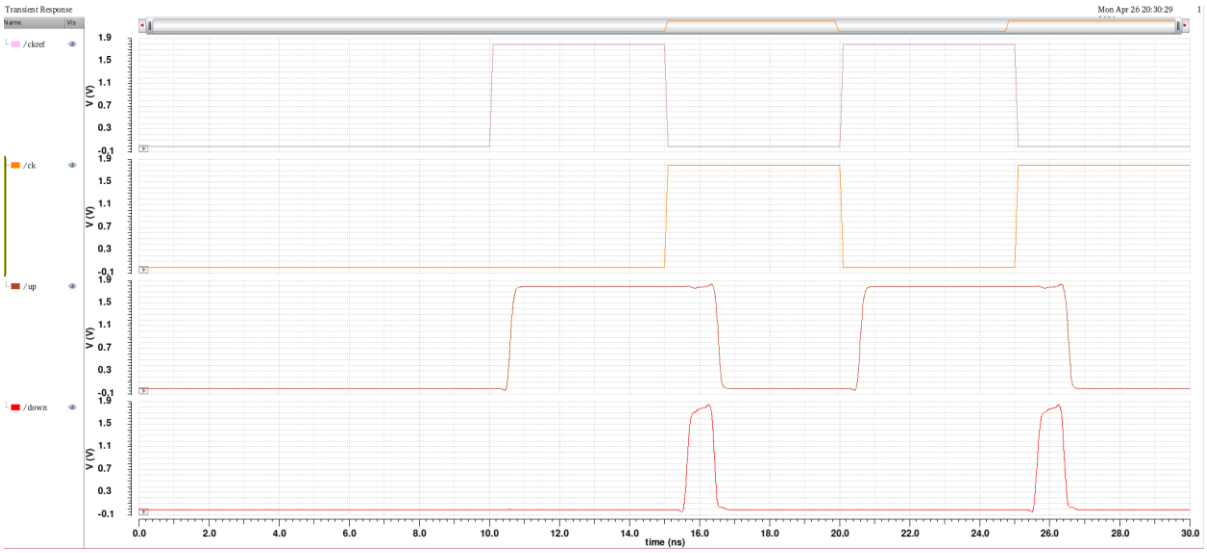

Figure.14 Out-of-phase waveforms

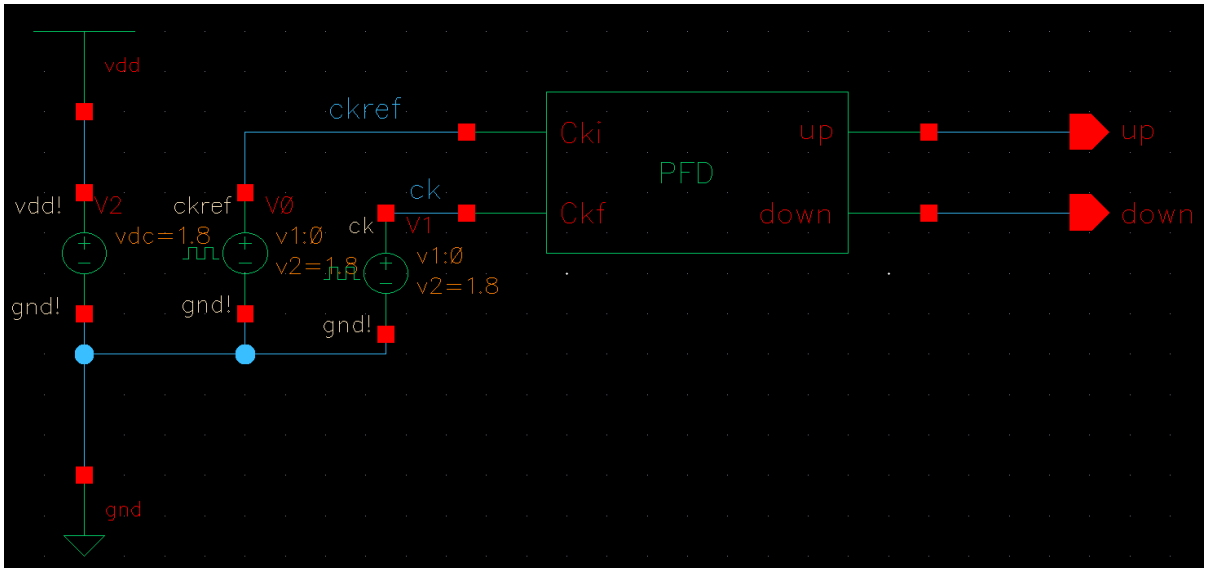

Figure.15 Phase sensitivity testbench

The figure represents the test bench that was created to test the circuit. There are two sources of the same frequency and phase offset between them. The waveforms indicate the phase offset detection between the two applied sources that results in a corresponding output voltage related to the phase by a proportionality factor K.

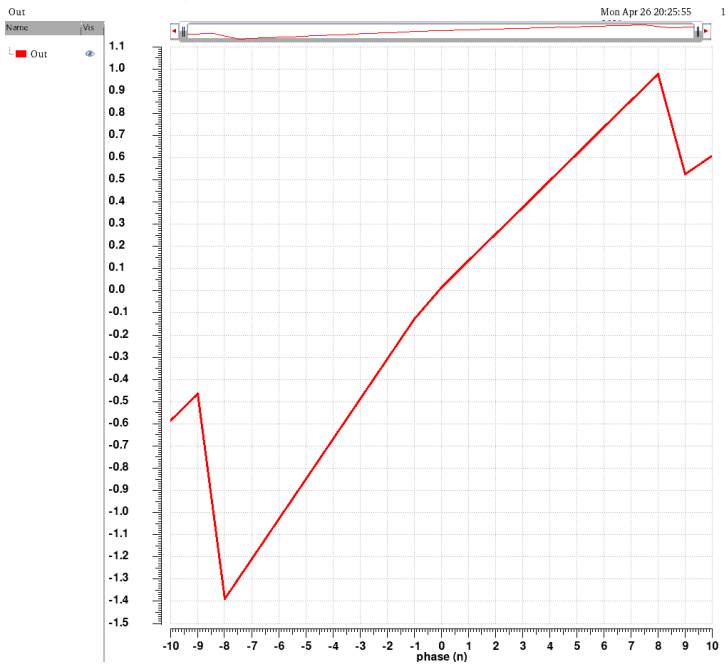

Figure.15 Phase Sensitivity -pi to pi

The figure is of the PFD transfer function the average sensitivity of the device over the range -2π to 2π. The sensitivity ranges from -1400mV to 998mV. The phase on the x-axis is the phase shift in the time domain by changing the initial time delay of each pulse.

Charge Pump

Abstract:

A charge pump is a DC- DC converter that uses capacitors for energy to raise or lower voltages based on applied clock signals, charge pump circuits offer high efficiencies up to 95%. The charge pump typically used in the PLL is a bipolar switched current source that outputs positive and negative current pulses based on the applied control signals (These charge pumps cannot charge voltages higher than the supply as the regular topologies.

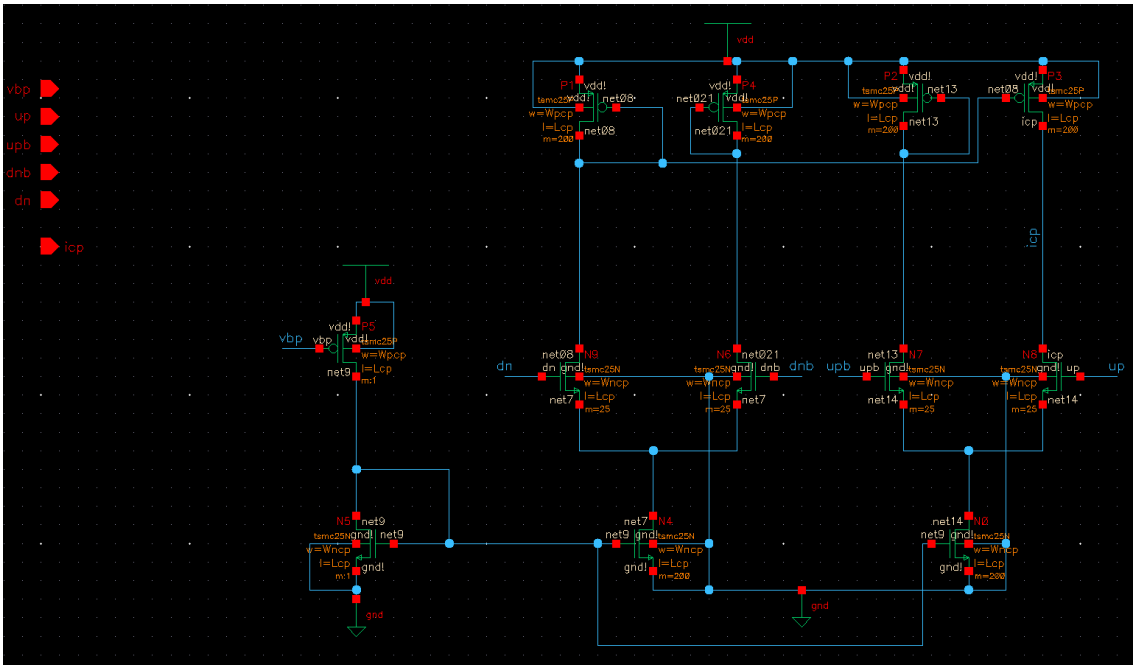

Figure.16 Differential symmetric load charge pump

In typical design the PFD is typically accompanied by the charge pump that generates pulse modulated current waveform typically conforming with bias current. In order to ensure the control voltage offered to the VCO is not PWM, a device known as the loop filter is added to remove the high frequency components, thereby yielding a purely stair stepped DC waveform that controls the VCO output frequency in a more controlled manner.

Loop Filter:

The loop filter is a low pass filter that is used to sink the current from the bipolar switched current source into a capacitor and simultaneously eliminate the higher order frequency components that are generated due to the constant switching of the current source and sink elements.

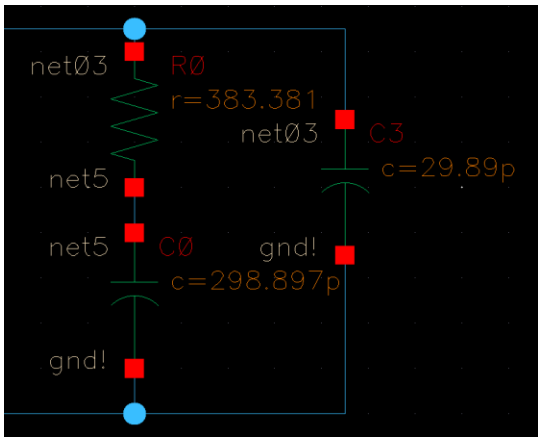

Figure.17 Loop Filter.

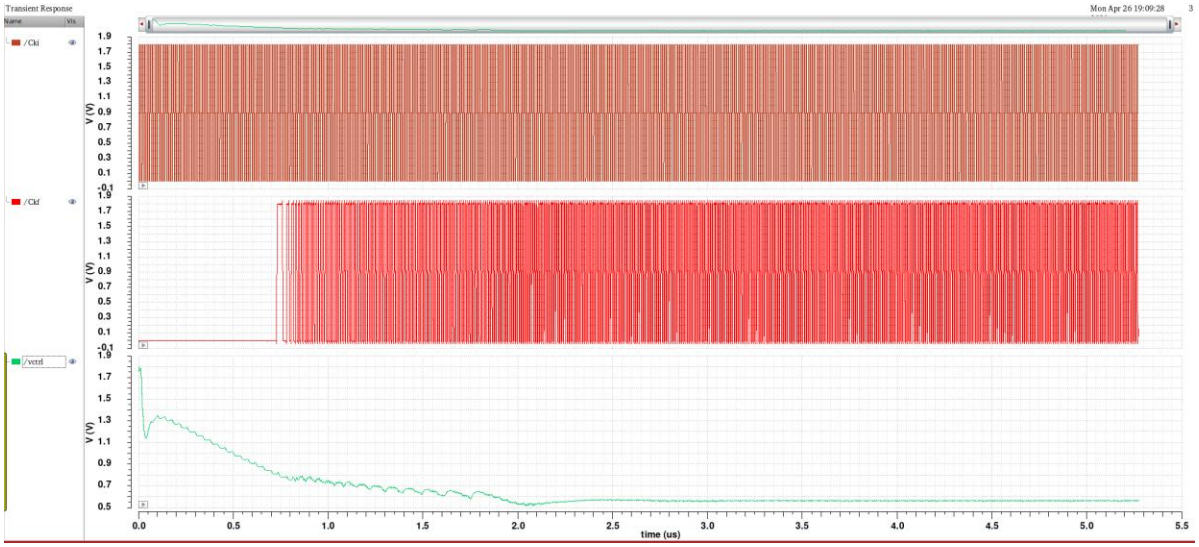

Figure.18 PLL Vctrl Transient

Loop Filter and Charge Pump Design Estimates:

- Loop bandwidth = 5MHz
- Damping factor = 0.9
- ICP = 2mA
- KVCO = 1.18e9
- N = 8

$$wn = sqrt\,(Kvco * Icp/(N * C1))\ rad/sec$$

$$C1 = (Kvco * Icp/(N * wn^2))$$
$$C1 = 298.8975\ pF$$

$$\zeta = Rlpf * C1 * wn/2$$

$$Rlpf = \zeta/(C1 * wn/2)$$
$$Rlpf = 191.69\ Ohms$$

Voltage Controlled Oscillator

Abstract:

At the heart of every serial interconnect is a clocking system, these systems signals that are used to reference data, synchronize and transmit data over long distances. These clocking systems comprise a vital element referred to as the VCO (Voltage Controlled Oscillator) that generates signals oscillating between the supply and the ground rails. This experiment explores the design and measurement of a fully differential VCO operating off a 1.8V supply with a wide tuning range of 1GHz to 3GHz.

Specification	**Unit**	**Value**
Supply	V	1.8 +/- 10%
Process	nm	300
Tuning Range	GHz	0-1.04
Temperature	C	27
Process Corner	-	TT/FF/SS

Table.7 Design Specifications.

Architecture:

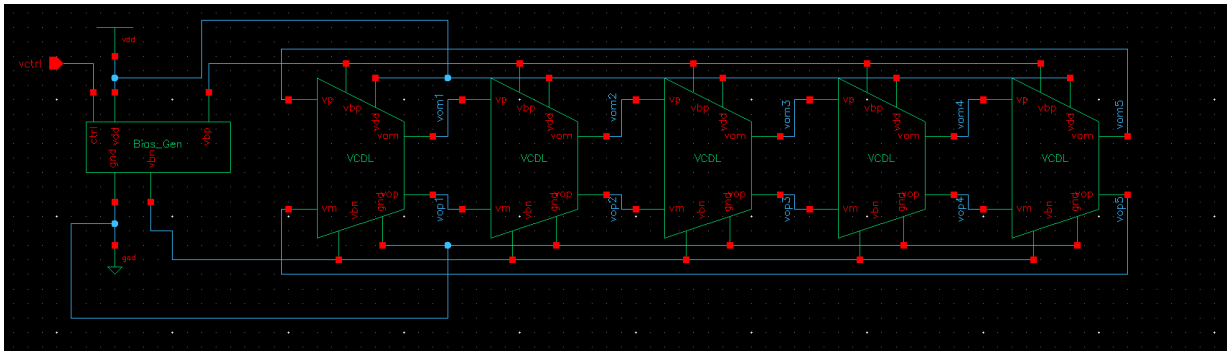

Figure.19 Fully Differential VCO

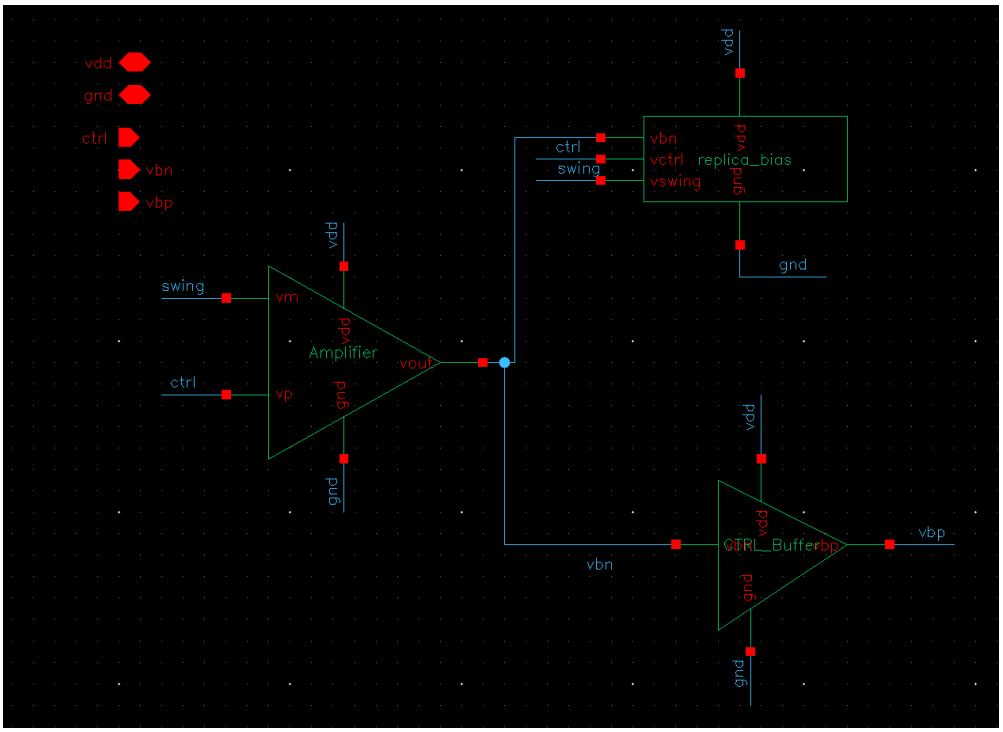

Figure.20 Biasing Circuit

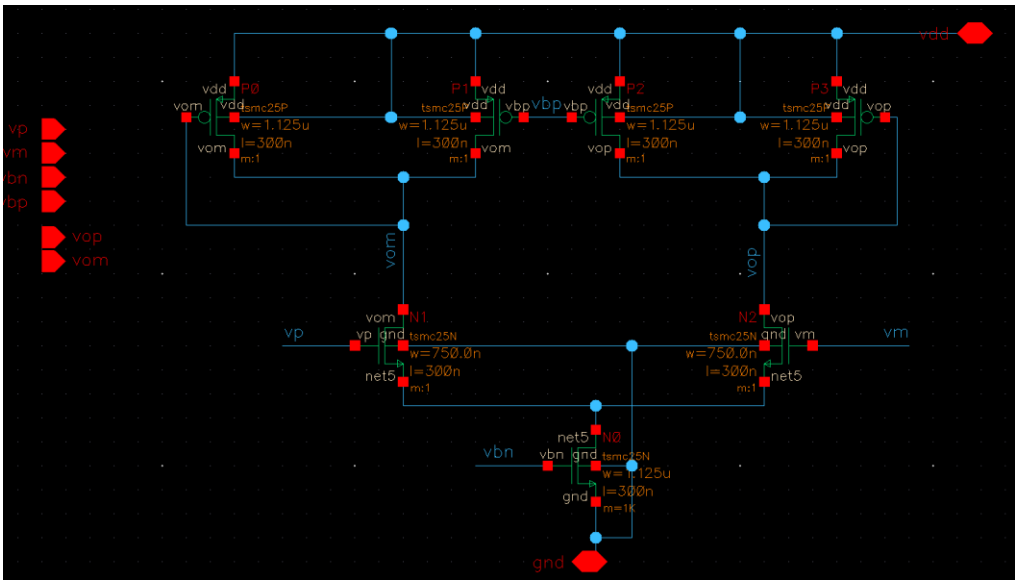

Figure.21 VCDL (Voltage Controlled Delay Line)

Biasing:

The Biasing circuit comprises 3 different subcircuits, each of which plays a vital role in the functioning of the VCO across various operating conditions.

Feedback Amplifier:

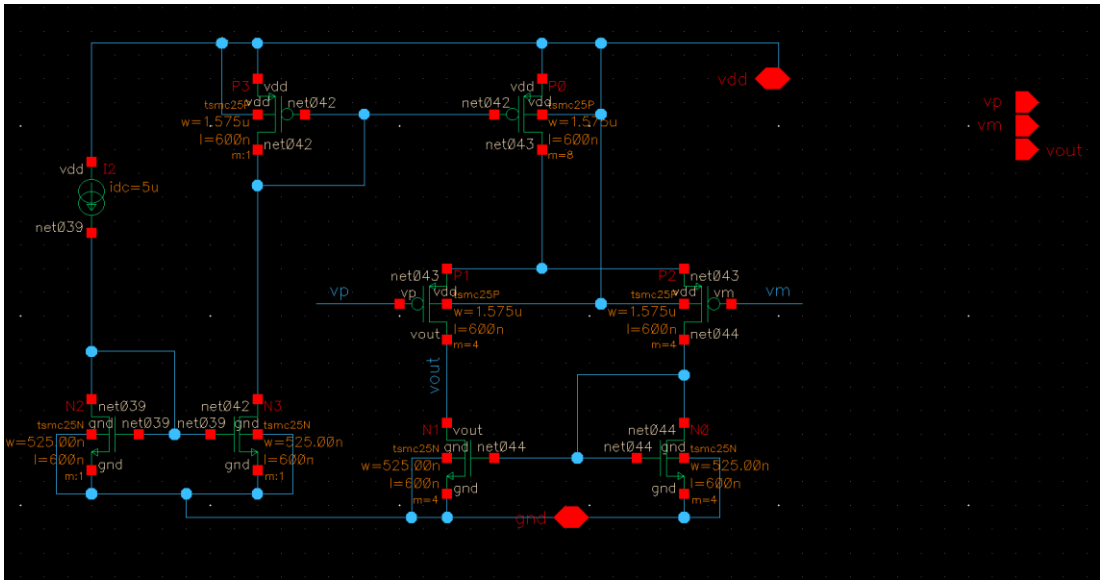

Figure.22 Feedback Amplifier

- The Feedback amplifier is connected in feedback to the output swing node of the replica Bias generator and the control signal.

Replica Bias:

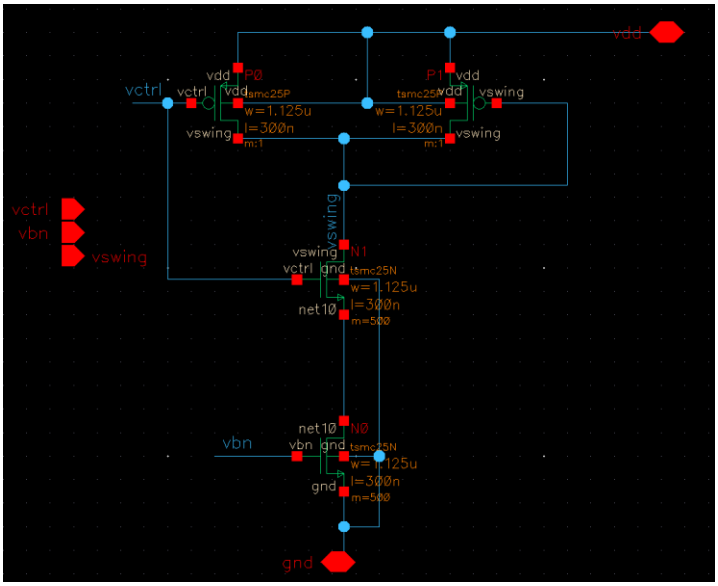

Figure.23 Replica Bias Generator

- The Half Buffer replica in conjunction with the feedback amplifier generates VBn the biasing voltage from the control signal.

❖ The Replica Bias also establishes a current that is independent of the supply voltage variation.

Control Buffer:

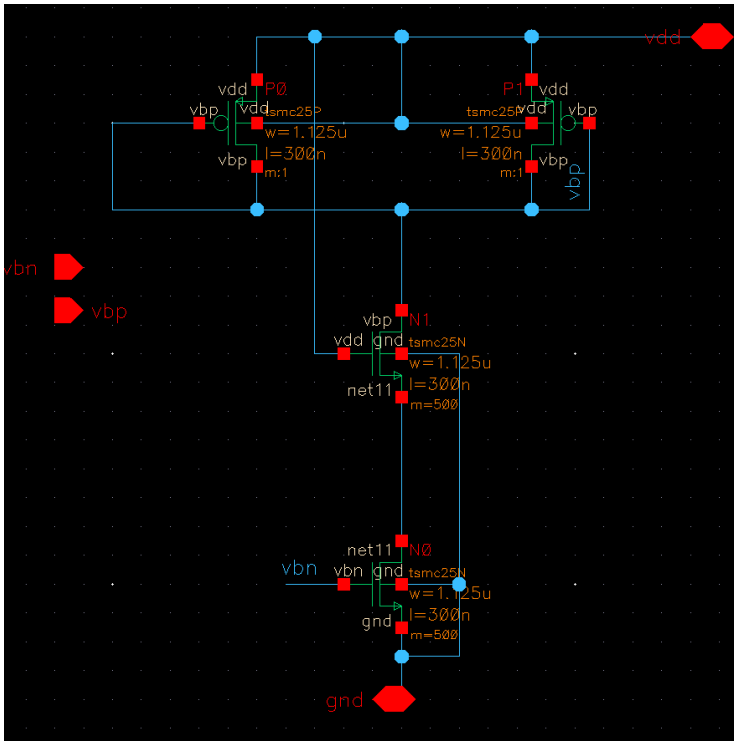

Figure.24 Control Buffer

❖ The Control Buffer is to continuously adjust the bias current thereby adjusting the lower limit set by the control signal.

Device Sizing Considerations:

Device Type	Length(m)	Width(m)	Multiplier
PMOS (Diode)	300n	1.125u	1
PMOS (Ctrl)	300n	1.125u	1
NMOS 1	300n	1.125u	500
NMOS 2	300n	1.125u	500

Table.8 Replica Bias Generator

Device Type	Length(m)	Width(m)	Multiplier

PMOS (Diode)	300n	1.125u	1
NMOS 1	300n	1.125u	500
NMOS 2	300n	1.125u	500

Table.9 Control Buffer

Device Type	**Length(m)**	**Width(m)**	**Multiplier**
PMOS (Tail)	600n	1.575u	8
PMOS (Input Pair)	600n	1.575u	4
NMOS (Load)	600n	525n	4

Table.10 Feedback Amplifier

Device Type	**Length(m)**	**Width(m)**	**Multiplier**
PMOS (VCTRL)	300n	1.125u	1
PMOS (Diode)	300n	1.125u	1
NMOS (Input Pair)	300n	750n	1
NMOS (Tail)	300n	1.125u	1000

Table.11 Voltage Controlled Delay Line

Simulations:

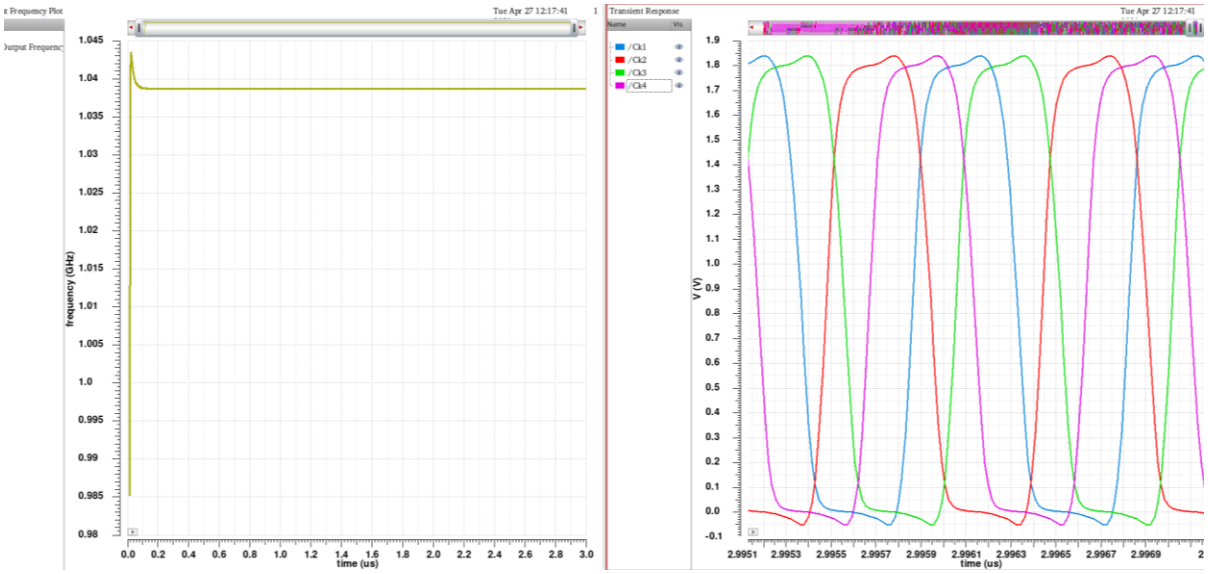

Figure.25 Full Swing Output

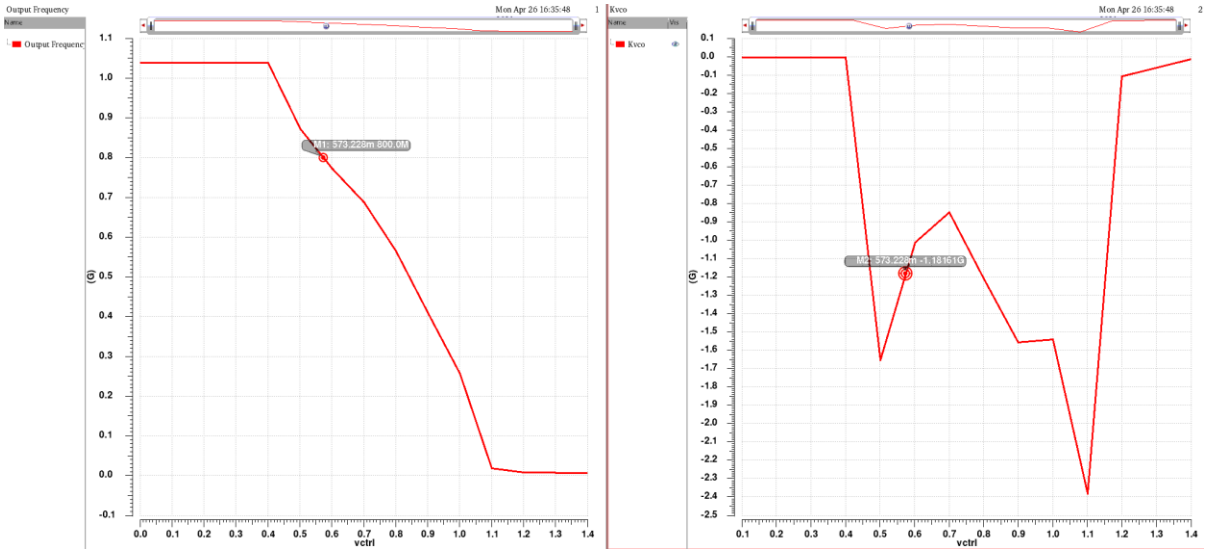

Figure.26 Frequency Tuning and KVO estimated as per PSS analysis

PLL Test Setup

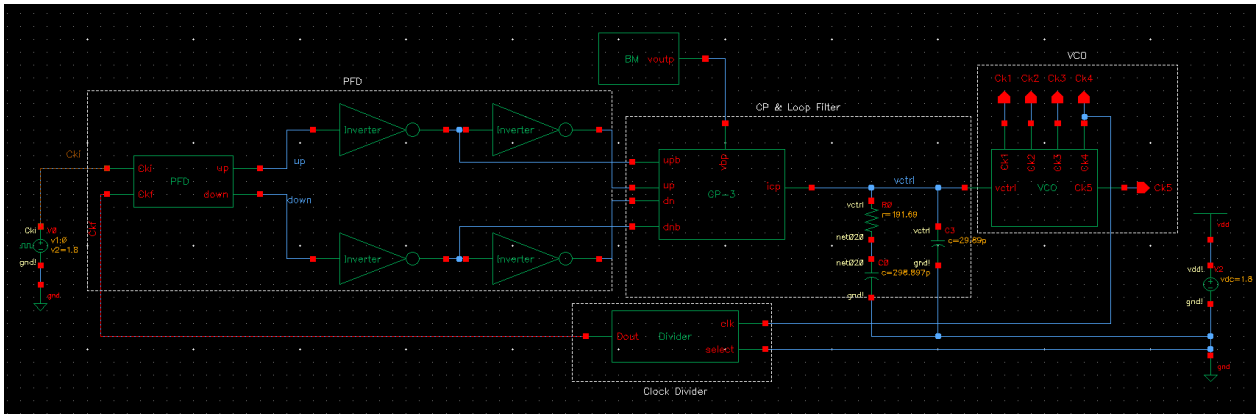

Figure.27 Phase Locked Loop

Simulation:

Transient Simulation:

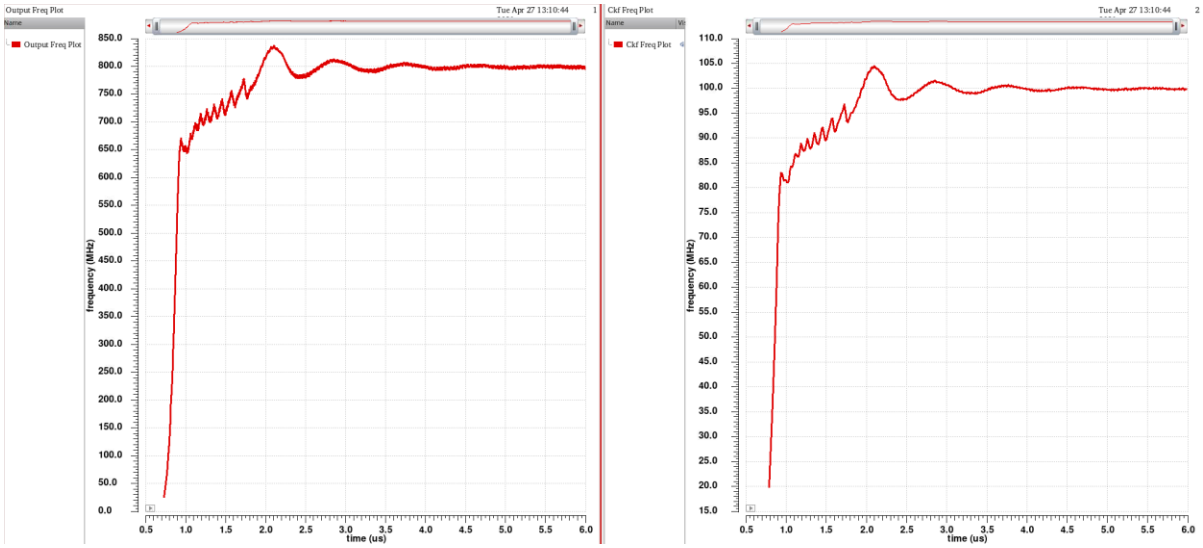

Figure.28 Locking and Transient frequency response in the time domain

From the above figure we can identify that the PLL requires a locking period of 5us and the system is underdamped in order to obtain stability to meet the locking requirements.

Noise Analysis

Phase noise can be described as the short-term frequency fluctuations of a signal. Frequency stability is a measure of how constant the oscillator output signal is. Phase noise is typically described in terms of decibel comparison for every hertz (dBc/Hz).

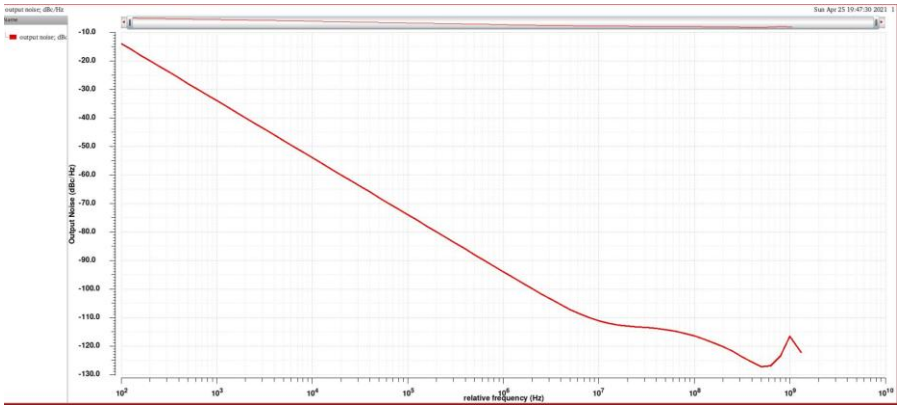

Figure.29 PLL Phase noise due to VCO estimated as per PSS simulation.

Jitter analysis:

To determine the jitter models, the transient simulation is used to generate an eye diagram with a sampling interval that is equal to the 1/fosc. Two samples were collected to estimate both the crest and trough of the generated clock signal.

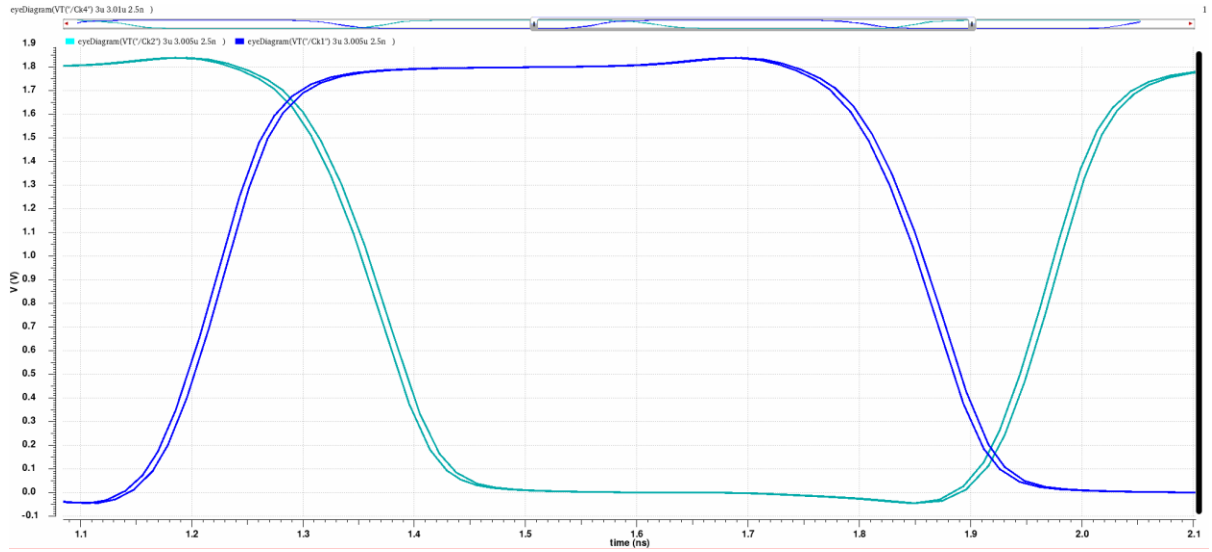

Figure.30 PLL Eye Diagram for Two Out of Phase Clock Signals.

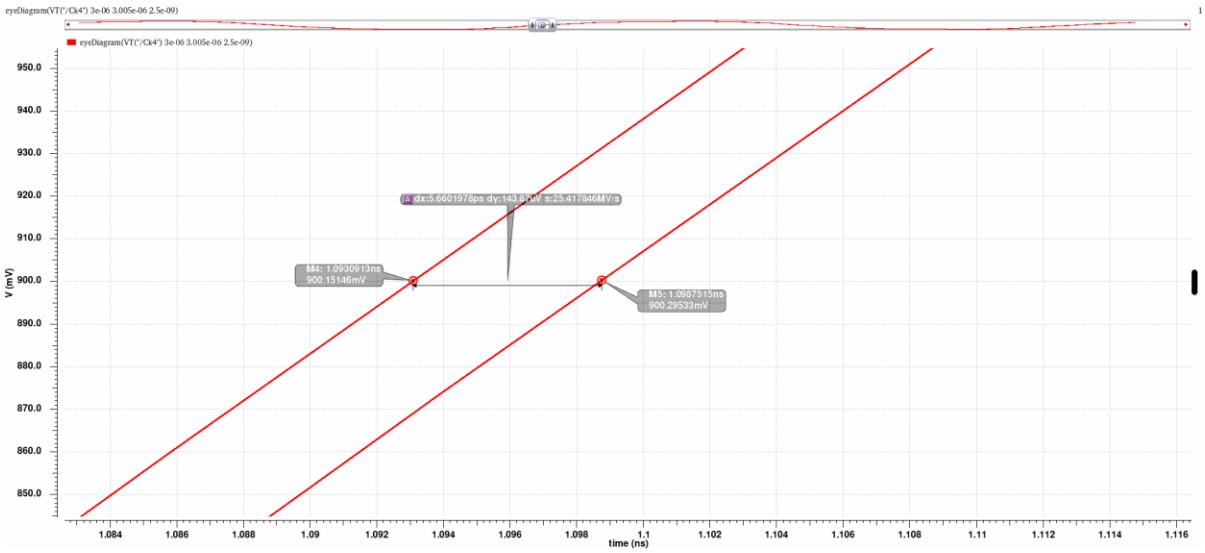

Figure.31 PLL Jitter Estimated over two UIs for the eye diagram.

The clock diagram is blown up to indicate the discrepancy that is estimated between the two UI and from this we can identify that the system offers an overall jitter of 5.6ps from the reference.

Phase Spacing Error:

The phase spacing error is the measure of how accurately the clocks are spaced in a multiphase clock reference generator. It is measured as the difference in time between a reference and the subsequent clock signals that are computed in degrees.

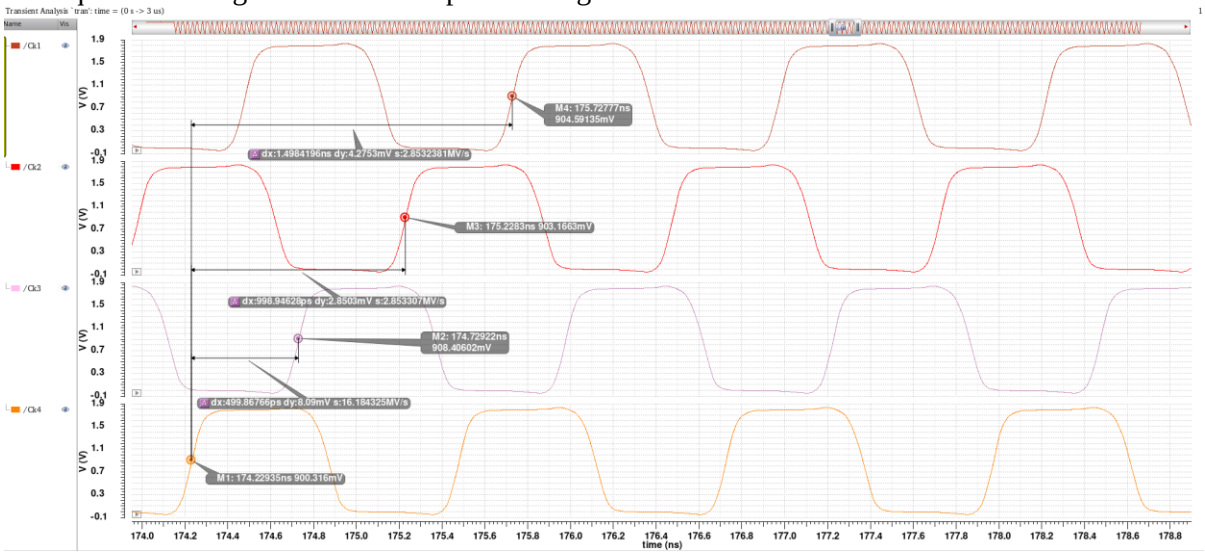

Figure.32 PLL phase clocking shifts and phase error between the clock signals.

Estimated Phase Error:

The phase shift between two signals can be estimated as the difference in time with respect to the total expected period of the signal:

Assuming clock 4 as the reference signal, we can estimate the phase shift on the other clock signals as so,

$$Phase\ shift\ =\ (td\ /T) * 360$$

td: time difference between two specific points on the waveform (threshold of 0.5*vdd).
T: Overall clock period.

Phase shift clk 2 : 287	phase spacing error :17	Timing error : 59pS
Phase shift clk 3 : 143	phase spacing error : 8	Timing error : 27pS
Phase shift clk 4 : 424	phase spacing error : 64	Timing error : 222pS

Power Dissipation:

The total estimated power dissipation from the device is approximately 11.56 mW as observed from the dc current below:

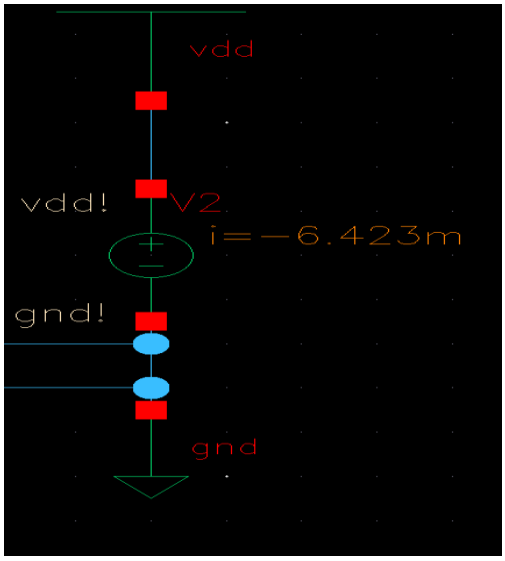

Figure.33 Total VDD Power Dissipation

Design Area:

Circuit	Area
PFD w/Pre-CP Inverters	$3.627\ mm^2$
CP	$9.2819\ mm^2$
VCO	$33.0972\ mm^2$
Divider	$3.393\ mm^2$

Total Area = $49.4\ mm^2$

Figure of Merit (FOM) :

The Figure of merit is the derived formula that estimates the performance of PLL as per set standards.

$$FOM = 10log\{(Frequency * Tuning\ Range)/(Power * Lock\ Time)\}$$

Parameters	Value	Units
Process	300	nm
Frequency	800M	Hz
Tuning Range	800M - 1G	Hz
Jitter	5.6	pS
Power	11.56m	W
Lock	5u	S
FOM	244	-

Table. Estimated Device Parameters.

Conclusion

An 800 MHz PLL with an overall jitter of 5.6pS and a locking time of 5u is presented. The PLL can provide and lock an output frequency of 800MHz=1GHz. With 300nm technology, an overall power consumption of 11.56mW is achieved.