Logic Design
Assignment 5
2014-12071
이은도

1. Problem Approach.

Type0 Mealy Machine, which outputs 1 when 101 is seen, and Type1 Mealy Machine, which outputs 1 when 0101 is seen are conceived. State minimizations for both machines are conducted below. The machines' outputs are connected to a counter, which increments its internal register when the input is 1. The top moduule selects which value to connect to output Y using a mux with TYPE as its sel value.

TYPE = 0

Enum	S_2	S_1	S_0	x	Enum	S_2^+	S_1^+	S_1^+	out
S0	0	0	0	0	S0	0	0	0	0
S0	0	0	0	1	S1	0	0	1	0
S1	0	0	1	0	S2	0	1	0	0
S1	0	0	1	1	S3	0	1	1	0
S2	0	1	0	0	S4	1	0	0	0
S2	0	1	0	1	S5	1	0	1	1
S3	0	1	1	0	S6	1	1	0	0
S3	0	1	1	1	S7	1	1	1	0
S4	1	0	0	0	S0	0	0	0	0
S4	1	0	0	1	S1	0	0	1	0
S5	1	0	1	0	S2	0	1	0	0
S5	1	0	1	1	S3	0	1	1	0
S6	1	1	0	0	S4	1	0	0	0
S6	1	1	0	1	S5	1	0	1	1
S7	1	1	1	0	S6	1	1	0	0
S7	1	1	1	1	S7	1	1	1	0

Initial Partition:
(S0, S1, S2, S3, S4, S5, S6, S7)

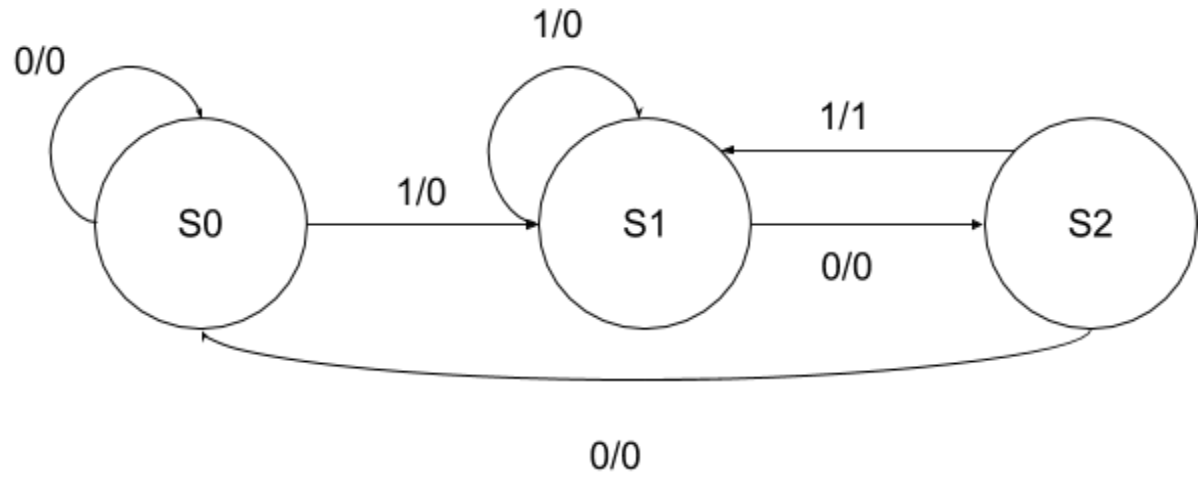
Partition According to Output Difference:
(S0, S1, S3, S4, S5, S7), (S2, S6)

Partition According to Next State:

(S0, S4), (S1, S3, S5, S7), (S2, S6)

The partitions created above will be newly named S0, S1, S2 from left to right.

The Mealy machine state diagram is shown below.



TYPE = 1

Enum	S_3	S_2	S_1	S_0	x	Enum	S_3^+	S_2^+	S_1^+	S_1^+	out
S0	0	0	0	0	0	S0	0	0	0	0	0
S0	0	0	0	0	1	S1	0	0	0	1	0
S1	0	0	0	1	0	S2	0	0	1	0	0
S1	0	0	0	1	1	S3	0	0	1	1	0
S2	0	0	1	0	0	S4	0	1	0	0	0
S2	0	0	1	0	1	S5	0	1	0	1	1
S3	0	0	1	1	0	S6	0	1	1	0	0
S3	0	0	1	1	1	S7	0	1	1	1	0
S4	0	1	0	0	0	S8	1	0	0	0	0
S4	0	1	0	0	1	S9	1	0	0	1	0
S5	0	1	0	1	0	S10	1	0	1	0	0
S5	0	1	0	1	1	S11	1	0	1	1	0

S6	0	1	1	0	0	S12	1	1	0	0	0
S6	0	1	1	0	1	S13	1	1	0	1	0
S7	0	1	1	1	0	S14	1	1	1	0	0
S7	0	1	1	1	1	S15	1	1	1	1	0
S8	1	0	0	0	0	S0	0	0	0	0	0
S8	1	0	0	0	1	S1	0	0	0	1	0
S9	1	0	0	1	0	S2	0	0	1	0	0
S9	1	0	0	1	1	S3	0	0	1	1	0
S10	1	0	1	0	0	S4	0	1	0	0	0
S10	1	0	1	0	1	S5	0	1	0	1	1
S11	1	0	1	1	0	S6	0	1	1	0	0
S11	1	0	1	1	1	S7	0	1	1	1	0
S12	1	1	0	0	0	S8	1	0	0	0	0
S12	1	1	0	0	1	S9	1	0	0	1	0
S13	1	1	0	1	0	S10	1	0	1	0	0
S13	1	1	0	1	1	S11	1	0	1	1	0
S14	1	1	1	0	0	S12	1	1	0	0	0
S14	1	1	1	0	1	S13	1	1	0	1	0
S15	1	1	1	1	0	S14	1	1	1	0	0
S15	1	1	1	1	1	S15	1	1	1	1	0

Initial Partition:
(S0, S1, S2, S3, S4, S5, S6, S7, S8, S9, S10, S11, S12, S13, S14, S15).

Partition According to Output Difference:
(S0, S1, S3, S4, S5, S6, S7, S8, S9, S11, S12, S13, S14, S15), (S2, S10).

Partition According to Next State:
(S0, S3, S4, S6, S7, S8, S11, S12, S14, S15), (S1, S5, S9, S13), (S2, S10).

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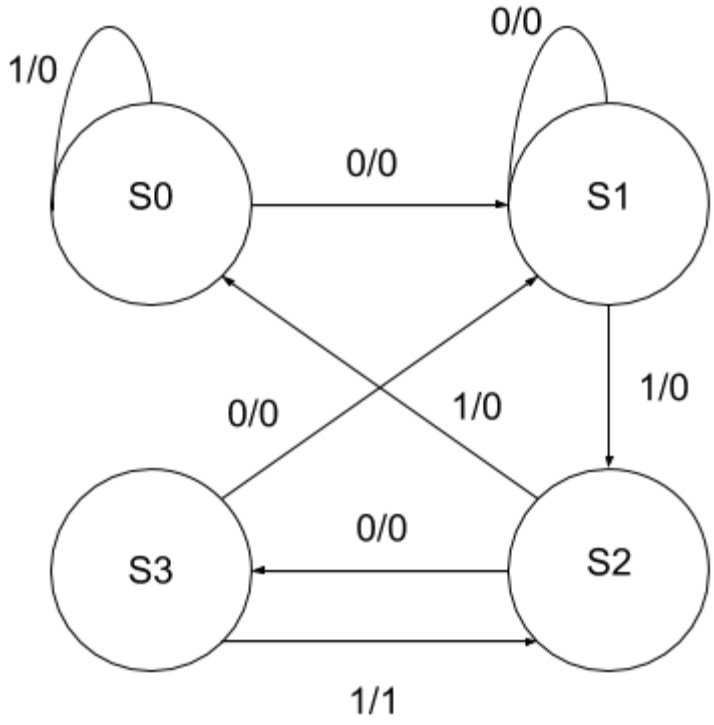
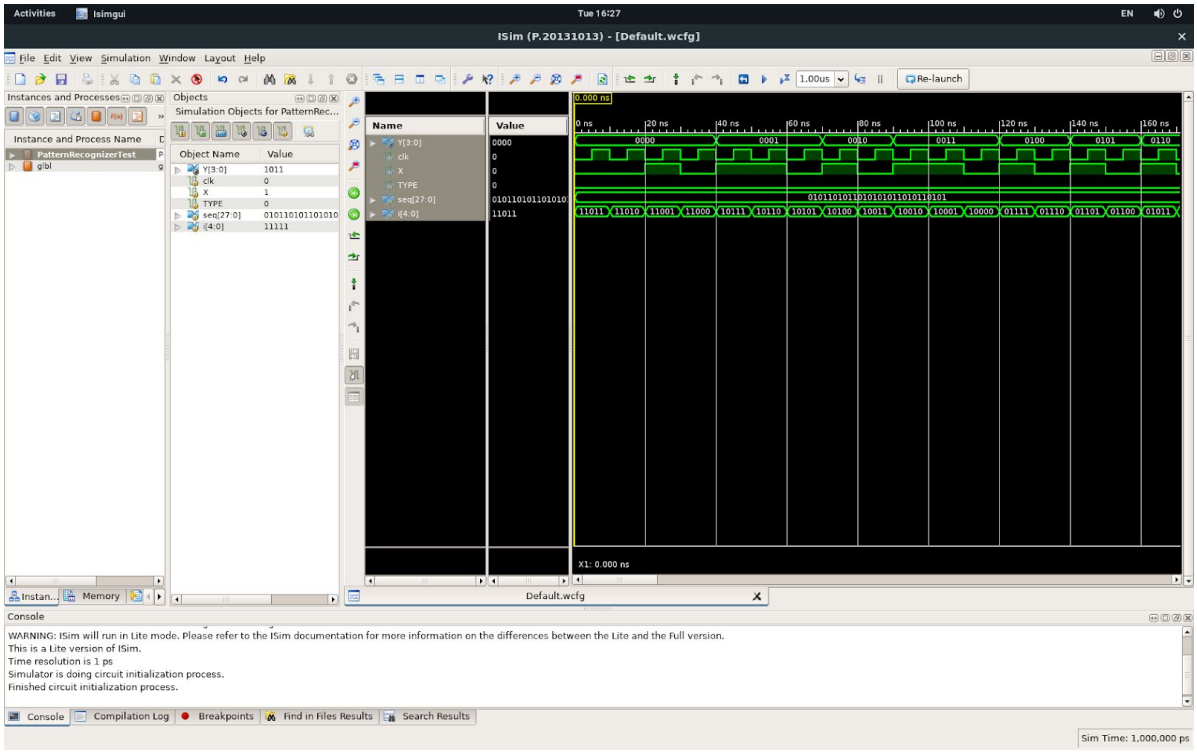
Partition According to Next State:
(S3, S7, S11, S15), (S0, S4, S6, S8, S12, S14), (S1, S5, S9, S13), (S2, S10).

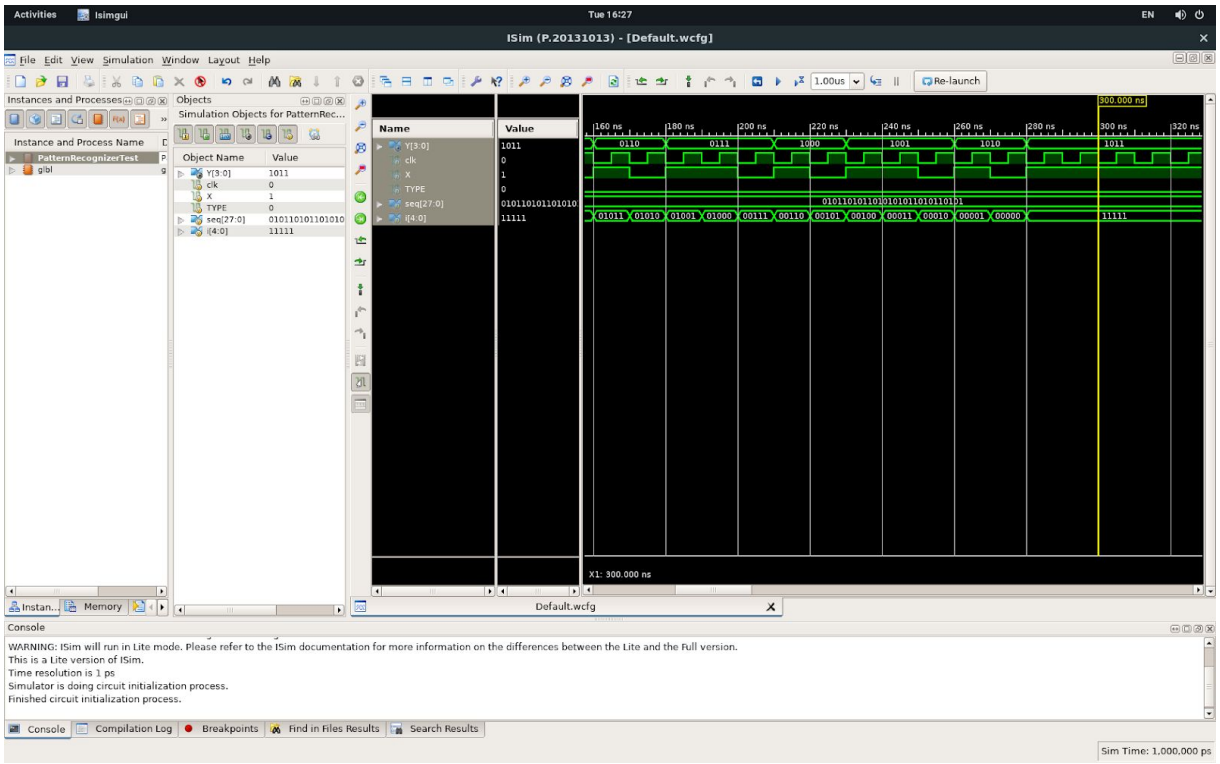
The partitions created above will be newly named S0, S1, S2, S3 from left to right.

The Mealy machine state diagram is shown below.

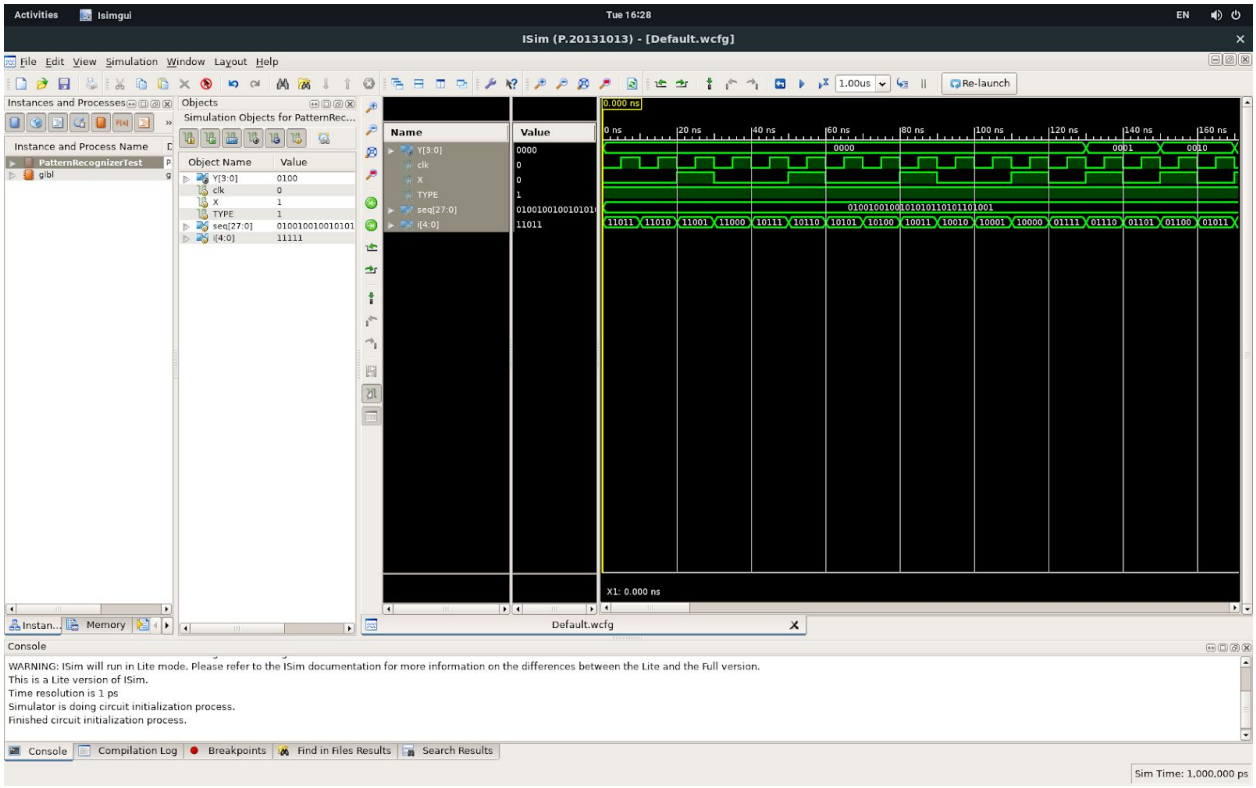


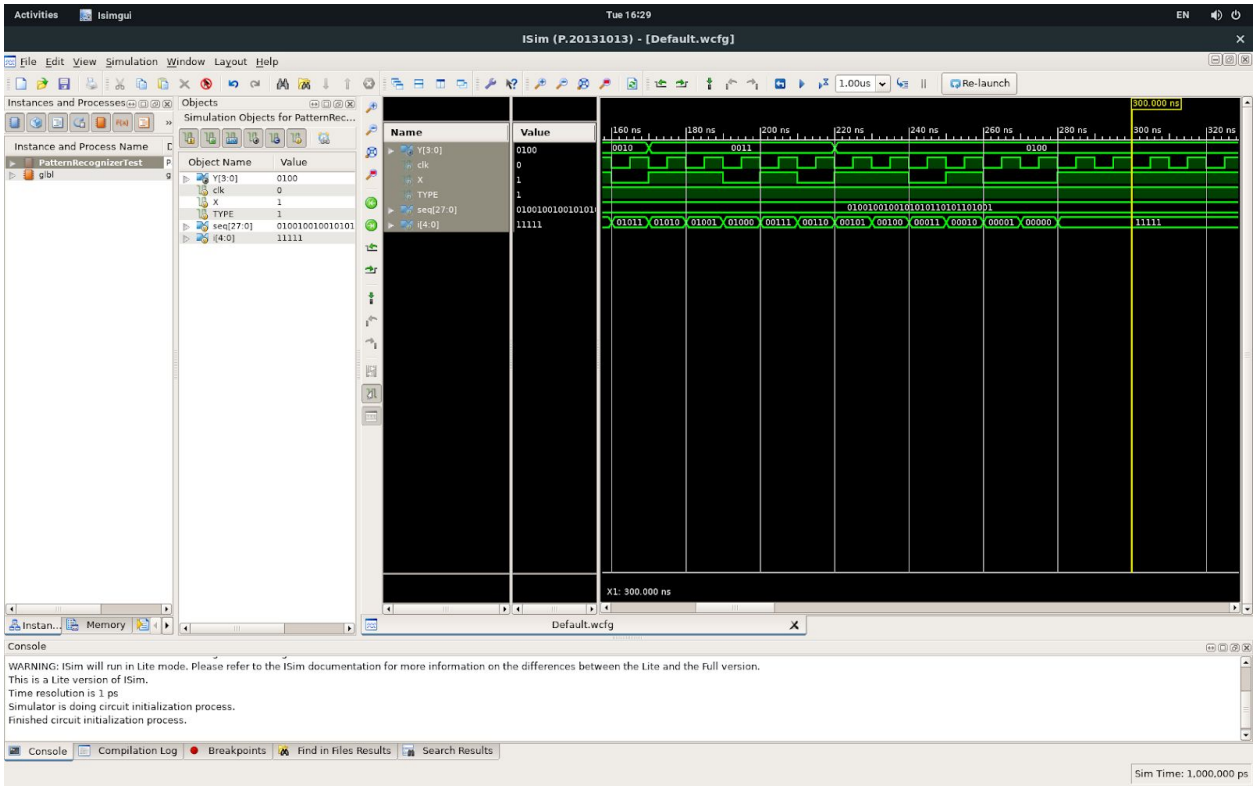
2. Printouts of Output Waveforms
(registers “seq” and “i” are used just for testing purposes. “seq” is the given input sequence and “i” is used to access each bit in seq.)
Test 1:



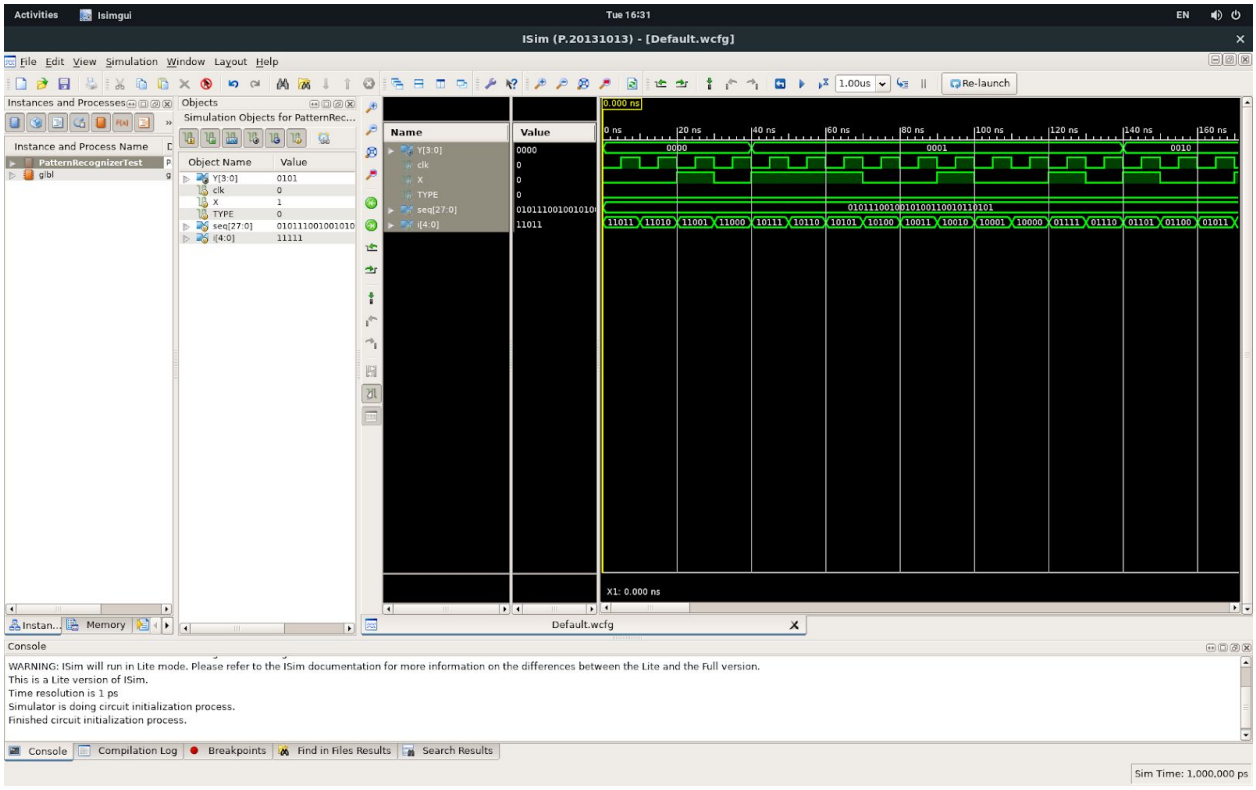


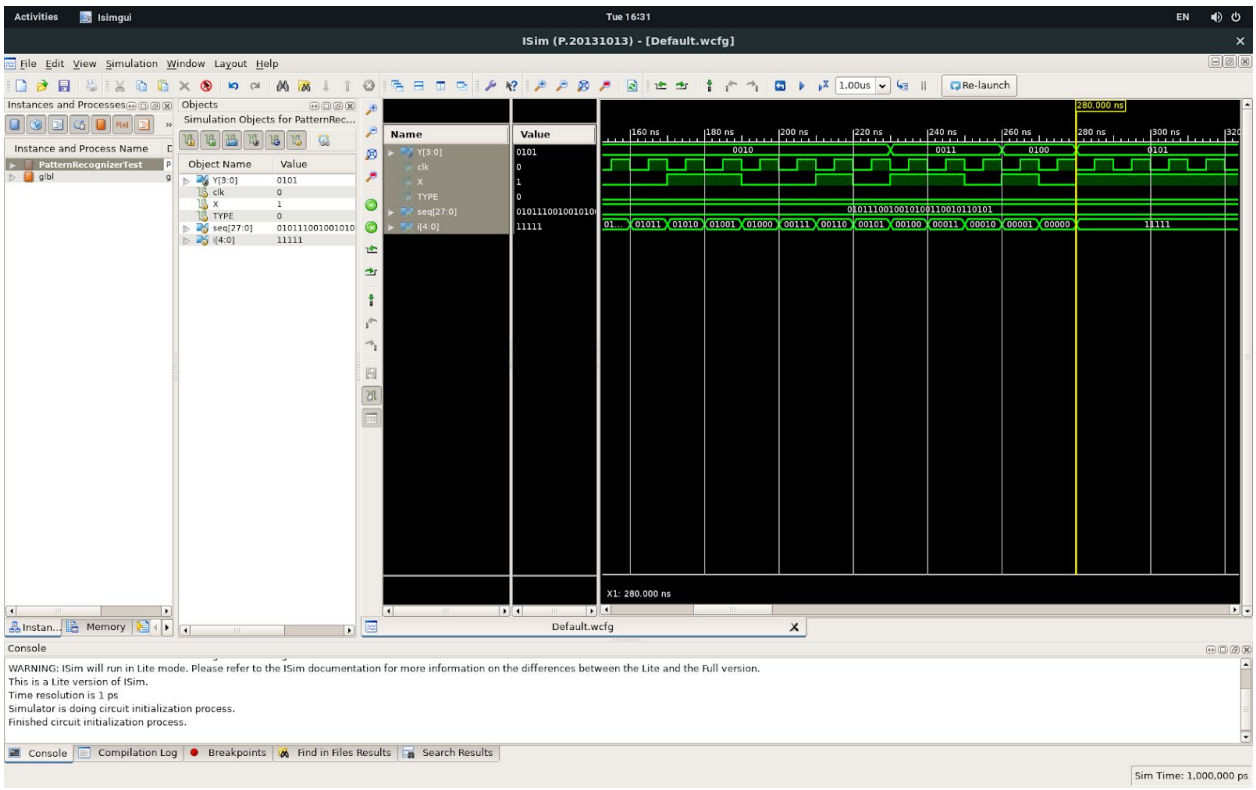
Test 2:


Activities
Isimgui
Tue 16:28
EN
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Objects
Simulation Objects for PatternRec...
Instance and Process Name
PatternRecognizerTest
glbl
Object Name
Value
Y[3:0]
clk
X
TYPE
seq[27:0]
i[4:0]
Name
0000
0
1
0100100100101011011011001
11011
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
0000
0001
0010
11011 11010 11001 11000 10111 10110 10101 10100 10011 10010 10001 10000 01111 01110 01101 01100 01011
X1: 0.000 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps


Activities
Isimgui
Tue 16:29
EN
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Objects
Simulation Objects for PatternRec...
Instance and Process Name
PatternRecognizerTest
glbl
Object Name
Value
Y[3:0]
clk
X
TYPE
seq[27:0]
i[4:0]
Name
0100
0
1
1
0100100100101011011011001
11111
160 ns
180 ns
200 ns
220 ns
240 ns
260 ns
280 ns
300 ns
320 ns
300.000 ns
0010
0011
0100
01011 01010 01001 01000 00111 00110 00101 00100 00011 00010 00001 00000
11111
X1: 300.000 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps

Test 3:


Activities
Isimgui
Tue 16:31
EN
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Objects
Simulation Objects for PatternRec...
Instance and Process Name
PatternRecognizerTest
glbl
Object Name
Value
Y[3:0]
clk
X
TYPE
seq[27:0]
i[4:0]
Name
Value
0000
0001
0010
X1: 0.000 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps


Activities
Isimgui
Tue 16:31
EN
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Objects
Simulation Objects for PatternRec...
Instance and Process Name
PatternRecognizerTest
glbl
Object Name
Value
Name
Value
0101
0011
0100
X1: 280.000 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps

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Test 4: