

ADAS Kit Developer Manual









Behavioral description and example diagrams to assist engineers interfacing their software with the Dataspeed ADAS Kit

Point of Contact: (support@dataspeedinc.com)

Contents

1	Overview		2
	1.1	Independent Operation	2
	1.2	Command Bits	2
		1.2.1 Enable Bit	2
		1.2.2 Clear Bit	2
		1.2.3 Ignore Bit	2
	1.3	Report Bits	3
		1.3.1 Enable Bit	3
		1.3.2 Driver Bit	3
		1.3.3 Override Bit	3
		1.3.4 Timeout Bit	3
		1.3.5 Fault Bits	3
2	Star	ndard Enable Sequence	4
	2.1	Example Flowchart	4
	2.2	Example Waveform	5
3	Overrides		
	3.1	Latching	6
	3.2	Clearing	6
	3.3	Ignoring	7
4	Tim	peouts	7
5	Aud	lible Warning	8
6	Use	e Cases	9
	6.1	Fully Autonomous Driving	9
	6.2	Adaptive Cruise Control (ACC)	9
	6.3	Active Park Assist (APA)	9
	6.4	Automatic Emergency Braking (AEB)	9
7	ROS	S Implementation	9
8	Fau	i <mark>lts</mark>	10
	8.1	Brake	0
	8.2	Throttle	0
	8.3	Steering	

1 Overview

The drive-by-wire system allows control of the four vehicle actuators: brake/throttle/steering/shifting. These subsystems share similar command and enable interfaces to be described in this document.

1.1 Independent Operation

Each subsystem has its own bits for enable, clear, ignore, driver, override, and fault. Each of the subsystems (brake/throttle/steering) are independent and can be operated independently with the following exceptions:

- An override on the brake will also cause an override on the throttle
- An override on the throttle will also cause an override on the brake
- Gear shift commands will be rejected if the override bit is set in any subsystem report message

1.2 Command Bits

The command messages for each subsystem have the following control bits that affect the behavior of the subsystem:

1.2.1 Enable Bit

The enable bit (EN) requests that the subsystem enables and responds to commands. The subsystem will not enable if there is an override or any faults.

1.2.2 Clear Bit

The clear bit (CLEAR) requests that the subsystem clear a latched override. The override will not clear if the subsystem is continually being overridden.

1.2.3 Ignore Bit

The ignore bit (IGNORE) disables consideration of new overrides, but does not clear a latched override. The ignore bit can be used with the clear bit to always enable computer control of the subsystem, regardless of human driver input.

1.3 Report Bits

The report messages for each subsystem have the following control bits that indicate the state of the subsystem:

1.3.1 Enable Bit

The enable bit (EN) is true when the subsystem is active (under computer control), otherwise false.

1.3.2 Driver Bit

The driver bit (DRIVER) indicates driver activity on the subsystem. This is not necessarily enough driver activity for an override. The criteria for each subsystem is unique. See individual datasheets for more details. The driver bit is not implemented on the steering subsystem.

1.3.3 Override Bit

The override bit (OVERRIDE) indicates enough driver activity on the subsystem to cause an override, or a latched override. The override bit is latched when an override causes the subsystem to transition from enabled to disabled. Use the clear bit to clear a latched override. The override criteria for each subsystem is unique. See individual datasheets for more details.

1.3.4 Timeout Bit

The timeout bit (TIMEOUT) indicates that a command message has not been received by the subsystem for more than 100ms.

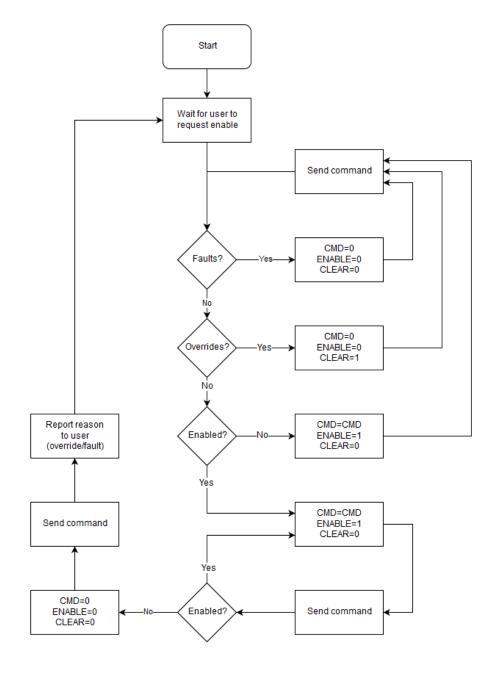
1.3.5 Fault Bits

Each subsystem has unique fault bits to report that the subsystem is non-functional. These are described in more detail in Section 8.

2 Standard Enable Sequence

2.1 Example Flowchart

The diagram below shows the logic to implement a standard enable state machine. More details on the next page.



Notes:

¹Expected update rate is 20ms or 50Hz

²The phrase 'CMD' refers to command field in each subsystem's command message: PCMD/PCMD/SCMD

³The phrase 'Send command' refers to sending commands for all subsystems: brake/throttle/steering

⁴The phrase 'Faults' refers to faults from any subsystem. See Section 8 for more detail.

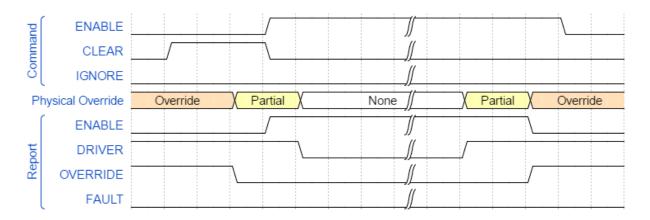
⁵The phrase 'Overrides' refers to overrides from any subsystem: brake/throttle/steering

⁶The phrase 'Enabled' refers to all subsystems enabled: brake/throttle/steering

2.2 Example Waveform

The waveform below shows the drive-by-wire system reacting to a program that implements the flowchart logic above. In this example, the user starts by pressing the brake pedal. However, it is not necessary to press the brake pedal to start the enable sequence.

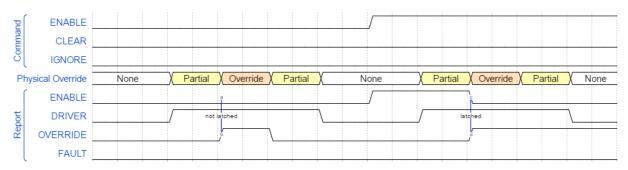
- The user starts by pressing the brake pedal and requesting the logic to enable.
- The logic checks for faults. There are no faults.
- The logic attempts to clear the OVERRIDE by setting the CLEAR bit.
- The user allows the OVERRIDE to clear by releasing the brake pedal.
- The logic sets ENABLE=1 and CLEAR=0 in the command.
- The system is under normal operation for some time.
- The user presses the brake pedal to override the system.
- The logic sets ENABLE=0 and informs the user about the reason for the disable.



3 Overrides

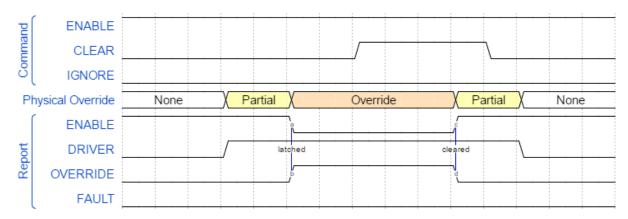
3.1 Latching

An override condition is latched if the override causes a transition from enabled to disabled, otherwise the override is not latched. The waveform below shows both conditions.



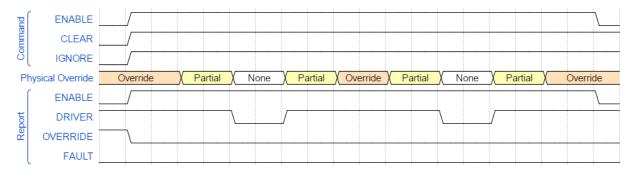
3.2 Clearing

A latched override condition must be cleared before the subsystem will enable by setting the CLEAR bit. This is only a request. The override will not clear if the subsystem is continually being overridden. The waveform below shows both conditions.



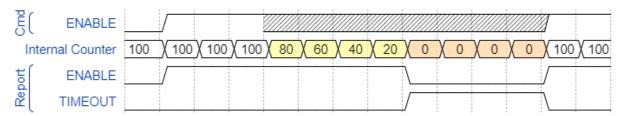
3.3 Ignoring

Overrides can be disabled with a combination of the IGNORE and CLEAR bits. The IGNORE bit will disable present and future overrides, but not latched overrides. The CLEAR bit will clear latched overrides. Use both IGNORE and CLEAR to completely disable overrides. This does not affect the DRIVER bit.



4 Timeouts

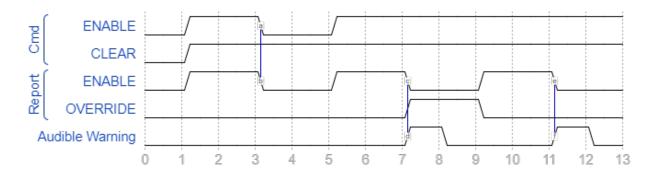
The timeout bit indicates that the command message has not been received by the subsystem for more than 100ms. This forces the subsystem to disable (ENABLE=0). The figure below shows this behavior. The shaded area indicates that the command message has disappeared from the CAN bus. The subsystem disables 100ms later, and the TIMEOUT bit is set. Normal operation resumes when the next command message is received.



5 Audible Warning

The audible warning alerts the human driver of any unintentional transition from computer control back to manual control. An unintentional transition is defined by the report ENABLE bit changing from 1 to 0 while the command ENABLE bit persists at 1. An intentional transition is defined by the command and report ENABLE bits changing from 1 to 0 simultaneously.

- Tick 3: Intentional transition caused by the change in the command ENABLE bit. No warning.
- Tick 7: Unintentional transition caused by the OVERRIDE bit. This triggers the audible warning.
- **Tick 11:** Unintentional transition with an unknown cause (maybe one of the fault bits). This triggers the audible warning.



6 Use Cases

6.1 Fully Autonomous Driving

Desired Behavior: Full control of all subsystems while allowing the driver to override with any

subsystem

Implementation: Use the standard enable sequence from Section 2

6.2 Adaptive Cruise Control (ACC)

Desired Behavior: Full control of all subsystems, but allow the driver to press the throttle pedal

without causing an override

Implementation: Modify the standard enable sequence from Section 2 to set the IGNORE and

CLEAR bits for the throttle subsystem only

6.3 Active Park Assist (APA)

Desired Behavior: Full control of all subsystems and allow the steering wheel to enable while the

driver's foot is still on the brake pedal

Implementation: Modify the standard enable sequence from Section 2 to send steering commands

as soon as steering is ready, even if the brake pedal is not ready

6.4 Automatic Emergency Braking (AEB)

Desired Behavior: Full control of only the brake pedal regardless of the human driver

Implementation: Only send commands to the brake subsystem, and set the IGNORE and CLEAR

bits to disable overrides

7 ROS Implementation

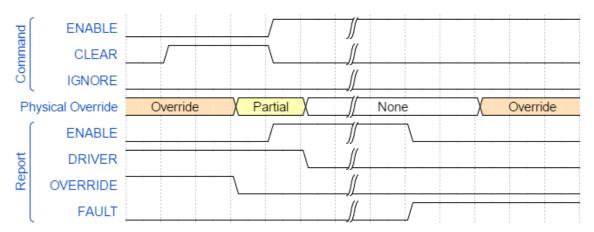
The Robot Operating System (ROS) driver provided by Dataspeed can be found at the link below. The ROS driver implements a form of the standard enable sequence found in Section 2 using C++ and ROS.

https://bitbucket.org/DataspeedInc/dbw_mkz_ros/src

8 Faults

Faults are unique to each subsystem. See individual datasheets for more details. If any faults are present, address the hardware issue before continuing operation of the vehicle.

Some faults prevent the subsystem from operating, and may cause information to be untrustworthy. This is shown in the diagram below. When FAULT goes true, ENABLE goes false. Also, OVERRIDE and DRIVER are no longer correctly reported.



8.1 Brake

- FLT1: Channel 1 signal is out of range. Pedal input, override bit, and driver bit are not trustworthy.
- FLT2: Channel 2 signal is out of range. Pedal input, override bit, and driver bit are not trustworthy.
- FLTPWR: Power has dropped below the acceptable range. This subsystem cannot be enabled.
- **FLTWDC:** The optional Watchdog Counter has been enabled and faulted. This subsystem cannot be enabled until power has been cycled.

8.2 Throttle

- FLT1: Channel 1 signal is out of range. Pedal input, override bit, and driver bit are not trustworthy.
- FLT2: Channel 2 signal is out of range. Pedal input, override bit, and driver bit are not trustworthy.
- FLTPWR: Power has dropped below the acceptable range. This subsystem cannot be enabled.
- **FLTWDC:** The optional Watchdog Counter has been enabled and faulted. This subsystem cannot be enabled until power has been cycled.

8.3 Steering

- FLT1: Vehicle CAN bus fault. Steering will not enable. Vehicle speed is not trustworthy.
- FLT2: Steering motor CAN bus fault. Steering will not enable. Steering wheel angle and torque are not trustworthy.
- **FLTCAL:** Steering wheel calibration fault. Steering will not enable. Steering wheel angle is not trustworthy. See datasheet for steering calibration procedure.
- FLTPWR: Power has dropped below the acceptable range. This subsystem cannot be enabled.
- **FLTWDC:** The optional Watchdog Counter has been enabled and faulted. This subsystem cannot be enabled until power has been cycled.

APPENDIX A: REVISION HISTORY

Revision A-00 (May 2017)

Modifications:

1. Initial release of this document. (DRAFT)

Revision A-01 (January 2018)

Modifications:

- 1. Added description of the TIMEOUT bit.
- 2. Added description of the Audible Warning.
- 3. Added FLTPWR to the list of faults.