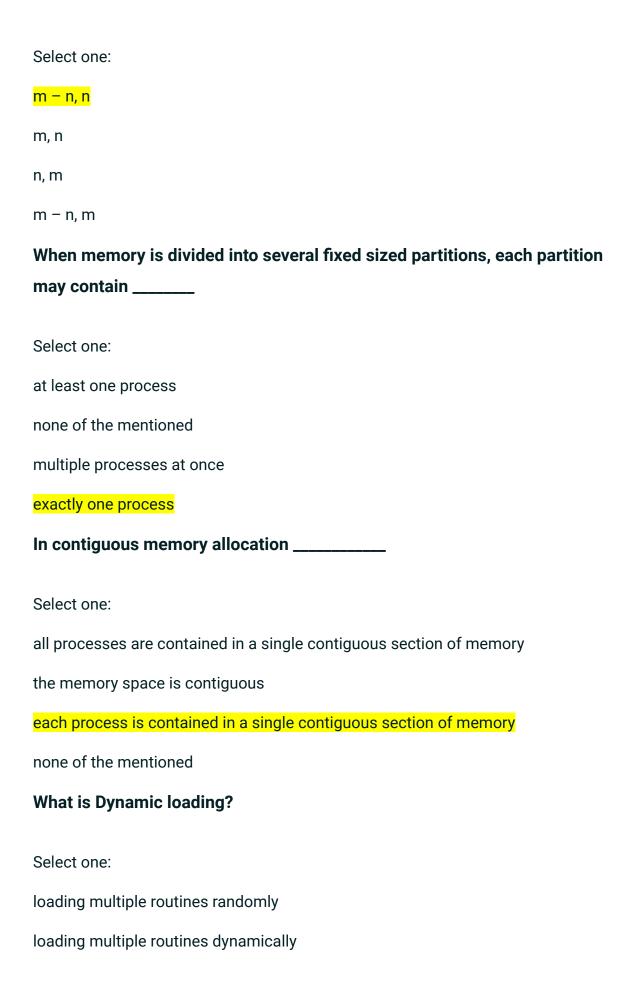
With paging there is no fragmentation.
Select one:
either type of
internal
none of the mentioned
<mark>external</mark>
Transient operating system code is code that
Select one:
stays in the memory always
comes and goes as needed
is not easily accessible
never enters the memory space
The operating system and the other processes are protected from being
modified by an already running process because
Select one:
every address generated by the CPU is being checked against the relocation and limit
<mark>registers</mark>
they are in different memory spaces
they have a protection algorithm
they are in different logical addresses
If the size of logical address space is 2 to the power of m, and a page size is 2 to the power of n addressing units, then the high order bits of a
logical address designate the page number, and the low order bits
designate the page offset.



loading a routine only when it is called Smaller page tables are implemented as a set of \_\_\_\_\_ Select one: stacks queues registers counters For larger page tables, they are kept in main memory and a \_\_\_\_\_ points to the page table. Select one: page table register pointer page table base pointer page table base register page table base The offset 'd' of the logical address must be \_\_\_\_\_ Select one: between 0 and the segment number greater than the segment number between 0 and segment limit

none of the mentioned

greater than segment limit

If a higher priority process arrives and wants service, the memory manager can swap out the lower priority process to execute the higher priority process. When the higher priority process finishes, the lower priority process is swapped back in and continues execution. This variant of swapping is sometimes called?

Select one:
pull out, push in
priority swapping
roll out, roll in
none of the mentioned
If there are 32 segments, each of size 1Kb, then the logical address should
have
Select one:
13 bits
14 bits
16 bits
15 bits
Each entry in a segment table has a
Select one:
none of the mentioned
segment value
segment base
segment peak

Time taken in memory access through PTBR is
Select one:
extended by a factor of 3
extended by a factor of 2
slowed by a factor of 2
slowed by a factor of 3
In fixed size partition, the degree of multiprogramming is bounded by
Select one:
the number of partitions
all of the mentioned
the CPU utilization
the memory size
What is Address Binding?
Select one:
going to an address in memory
locating an address with the help of another address
binding two addresses together to form a new address in a different memory space
a mapping from one address space to another
Paging increases the time.
Select one:
waiting

execution
all of the mentioned
context - switch
The must design and program the overlay structure.
Select one:
system designer
programmer
system architect
none of the mentioned
When the entries in the segment tables of two different processes point to
the same physical location
Select one:
all of the mentioned
segments are shared
the processes get blocked
the segments are invalid
The operating system maintains a table that keeps track of how many frames have been allocated, how many are there, and how many are available.
Select one:
memory
<mark>frame</mark>
page

mapping	

The first fit, best fit and worst fit are strategies to select a
Select one:
all of the mentioned
process from a queue to put in memory
free hole from a set of available holes
processor to run the next process
What location is the operating system?
Select one:
in the low memory
either low or high memory (depending on the location of interrupt vector)
none of the mentioned
in the high memory
In paging the user provides only which is partitioned by the hardware
into and
Select one:
one address, page number, offset
none of the mentioned
one offset, page number, address
page number, offset, address
The segment limit contains the
Select one:

segment length
starting physical address of the segment in memory
none of the mentioned
Logical memory is broken into blocks of the same size called
Select one:
none of the mentioned
pages
backing store
frames
A multilevel page table is preferred in comparison to a single level page table for translating virtual address to physical address because
Select one:
Select one: it is required by the translation lookaside buffer
it is required by the translation lookaside buffer  it helps to reduce the size of page table needed to implement the virtual address
it is required by the translation lookaside buffer
it is required by the translation lookaside buffer  it helps to reduce the size of page table needed to implement the virtual address
it is required by the translation lookaside buffer  it helps to reduce the size of page table needed to implement the virtual address  space of a process
it is required by the translation lookaside buffer  it helps to reduce the size of page table needed to implement the virtual address space of a process  it reduces the memory access time to read or write a memory location
it is required by the translation lookaside buffer  it helps to reduce the size of page table needed to implement the virtual address space of a process  it reduces the memory access time to read or write a memory location  it helps to reduce the number of page faults in page replacement algorithms
it is required by the translation lookaside buffer  it helps to reduce the size of page table needed to implement the virtual address space of a process  it reduces the memory access time to read or write a memory location  it helps to reduce the number of page faults in page replacement algorithms  The swaps processes in and out of the memory.

User
CPU
The relocation register helps in
Select one:
providing more address space to processes
none of the mentioned
a different address space to processes
to protect the address spaces of processes
The primary memory can hold
Select one:
all of the mentioned
cpu
user processes
operating system
Using transient code, the size of the operating system during
program execution.
Select one:
decreases
increases
changes
maintains
If the offset is legal

Select one:
it is subtracted from the segment base to produce the physical memory address
none of the mentioned
it is used as a physical memory address itself
it is added to the segment base to produce the physical memory address
The idea of overlays is to
Select one:
all of the mentioned
enable a process to be larger than the amount of memory allocated to it
data that are needed at any given time
keep in memory only those instructions
The segment base contains the
Select one:
segment length
none of the mentioned
none of the mentioned starting logical address of the process
starting logical address of the process
starting logical address of the process starting physical address of the segment in memory
starting logical address of the process  starting physical address of the segment in memory  For every process there is a
starting logical address of the process  starting physical address of the segment in memory  For every process there is a  Select one:
starting logical address of the process  starting physical address of the segment in memory  For every process there is a  Select one:  pointer to page table

page table
Physical memory is broken into fixed-sized blocks called
Select one:
backing store
frames
pages
none of the mentioned
If the process can be moved during its execution from one memory segment
to another, then binding must be
Select one:
preponed to load time
preponed to compile time
none of the mentioned
delayed until run time
The page table registers should be built with
Select one:
a large memory space
none of the mentioned
very high speed logic
very low speed logic
In a system that does not support swapping

Select one:

binding of symbolic addresses to physical addresses normally takes p execution	lace during
the compiler normally binds symbolic addresses (variables) to relocate	<mark>able addresses</mark>
the compiler normally binds symbolic addresses to physical addresses	S
the loader binds relocatable addresses to physical addresses	
The is used as an index into the page table.	
Select one:	
page offset	
frame bit	
page number	
frame offset	
Consider a computer with 8 Mbytes of main memory and a 128k cache block size is 4 K. It uses a direct mapping scheme for cac management. How many different main memory blocks can magiven physical cache block?	che
Select one:	
2048	
8	
256	
64	
With relocation and limit registers, each logical address must be limit register.	ethe
Select one:	

greater than
equal to
less than
none of the mentioned
Every address generated by the CPU is divided into two parts. They are
Select one:
frame bit & page number
frame offset & page offset
page number & page offset
page offset & frame bit
The protection bit is 0/1 based on
Select one:
write only
none of the mentioned
read – write
read only
Binding of instructions and data to memory addresses can be done at
<del></del>
Select one:
Compile time
Load time

## Execution time

## All of the mentioned

In segmentation, each address is specified by
Select one:
a segment number & offset
a key & value
a value & segment number
an offset & value
The table contains the base address of each page in physical memory
Select one:
page page
memory
process
frame
If there are 32 segments, each of size 1Kb, then the logical address should
have
Select one:
16 bits
13 bits
15 bits
14 bits

If binding is done at assembly or load time, then the process be moved to different locations after being swapped out and in again.
Select one:
can
can never
may
must
Which of the following is TRUE?
Select one:
When overlays are used, the size of a process is not limited to the size of the
physical memory
Overlays are used to increase the logical address space
Overlays are used whenever the physical address space is smaller than the logical address space
Overlays are used to increase the size of physical memory
The size of a page is typically
Select one:
varied
power of 4
none of the mentioned
power of 2
What is the advantage of dynamic loading?
Select one:

## An unused routine is never loaded

CPU utilization increases

All of the mentioned

A used routine is used multiple times