Exercises: Cache coherence

This is not a homework!

Questions

1. We have multi-core processor illustrated in Figure 1. In this processor, we use coherency protocol described in Figure 2. Timing parameters are presented in Figure 3.

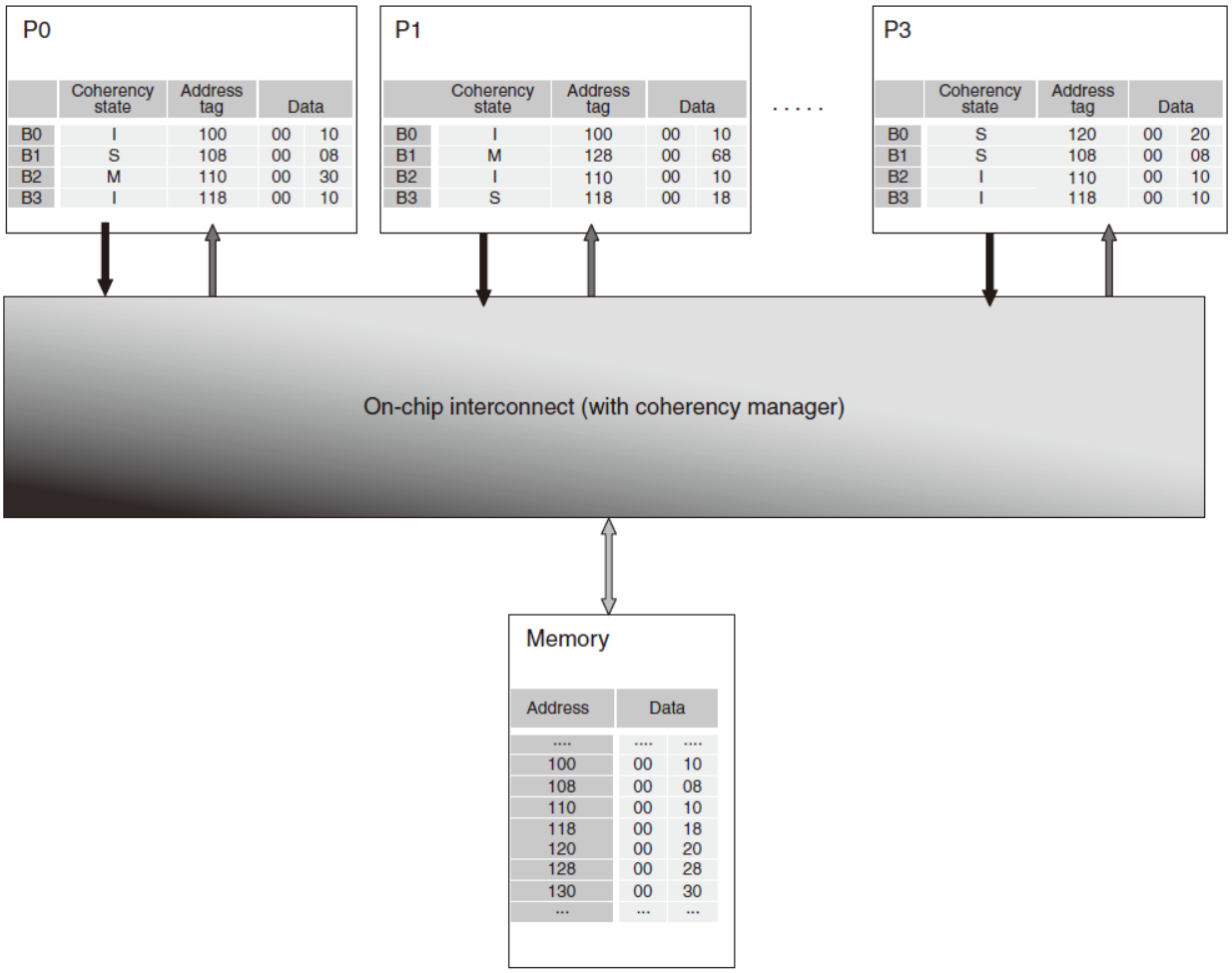

Figure 1. Multicore (point-to-point) multiprocessor.

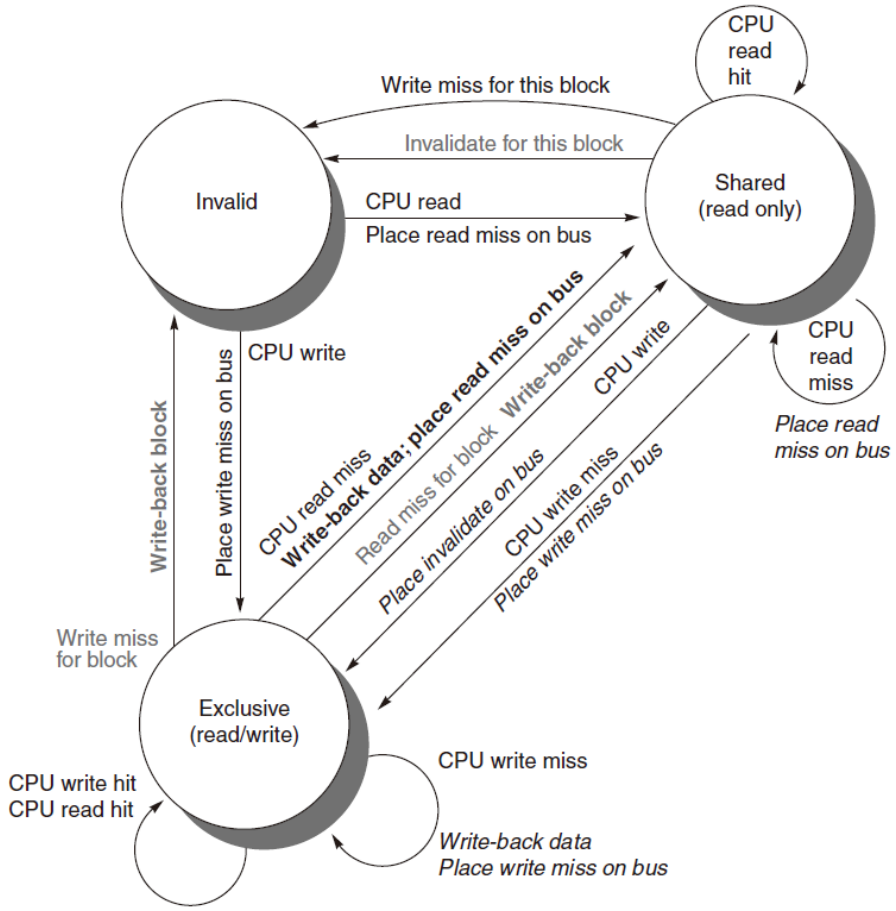

Figure 2. Cache coherence state diagram with the state transitions induced by the local processor shown in black and by the bus activities shown in gray. The activities on a transition are shown in bold.

Parameter	Implementation 1
N_{memory}	100
N_{cache}	40
$N_{invalidate}$	15
$N_{writeback}$	10

Figure 3. Snooping coherence latencies.

For the following code sequences, compute the total stall cycles for the base MSI protocol. Assume that state transitions that do not require bus transactions incur no additional stall cycles.

a. P1: read 110
   P3: read 110
   P0: read 110

b. P1: read 120
   P3: read 120
   P0: read 120

c. P0: write 120 ← 80
   P3: read 120
   P0: read 120

d. P0: write 108 ← 88
   P3: read 108
   P0: write 108 ← 98

2. Explain and draw the state transition diagram of MOESI protocol.