CS510: Computer Architecture

Instructor: Prof. Soontae Kim
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Course Web: Embedded Computing Lab at http://ecl.kaist.ac.kr
Office hours: right after class or via prior appointments

TA: Jungwoo Park, Jesung Kim

Classroom: Classroom #1101 (제 1 강의실)) in computer science building
Class hours: W/F 1:00 ~ 2:15PM

Course description: The class will review fundamental structures in modern microprocessor and computer system architecture design. Topics include performance metric, memory system design, pipelining, exploiting instructional-level parallelism and its limits, multiprocessors, thread-level parallelism, and data-level parallelism.

Prerequisite: undergraduate computer architecture course, “Computer Organization & Design” by Patterson and Hennessy is preferred as the text of your undergraduate course. However, I will review pipelining and memory basics for you.

Textbook: Computer Architecture: A Quantitative Approach, 5th Edition, John L. Hennessy and David A. Patterson, Morgan Kaufmann Publishers

Grading:
Midterm Exam: 30%
Final Exam: 20%
Homework: 20%

- Four homework assignments

Project: 30%

- Make a team of at most three students. You choose specific topics such as caches, memory, pipeline, ILP, DLP, TLP, GPU, power, reliability, etc. and perform experiments using simulators and other tools. More details will be announced later.
- Two project presentations each 5%, proposal report each 5%, final report 15%

Cheating: All forms of cheating are not allowed in this class. Examples include the followings.

- Do not copy solutions obtained from Internet, etc.
- Do not copy other students’ solutions. Discussion is OK but you should not discuss about detailed solutions.
- Cheater will be given zero point and those who allow cheating will be given 50% of their earned points.

*Subject to change

Week	Date	Topic	Reading (textbook)	Assignments
1	3/1	No class	삼일절	
	3/3	Chapter1. Fundamentals of computer design	Ch1	
2	3/8	Chapter1. Fundamentals of computer design	Ch1	
	3/10	MIPS CPU design #1	Appendix A, undergraduate textbook	
3	3/15	MIPS CPU design #2	Appendix A, undergraduate textbook	
	3/17	Review-pipelining#1	Appendix C	
4	3/22	Review-pipelining#2	Appendix C	HW#1
	3/24	Instruction-level parallelism#1	Ch3	
5	3/29	Instruction-level parallelism#2	Ch3	
	3/31	Instruction-level parallelism#3	Ch3	
6	4/6	Instruction-level parallelism#4	Ch3	
	4/7	Limits of ILP#1	Ch3	HW#2
7	4/12	Review-caches#1	Appendix B	
	4/14	Review-caches#2	Appendix B	
8	4/19	Midterm exam		
	4/21	Midterm exam		
9	4/26	Proposal presentations		Submit proposal reports
	4/28	Advanced caches#1	Ch2	
10	5/3	No class	석가탄신일	
	5/5	No class	어린이날	
11	5/10	Advanced caches#2	Ch2	
	5/12	Memory#1	Ch2	HW#3
12	5/17	Memory#2	Ch2	
	5/19	Vector architecture	Ch4	
13	5/24	GPU	Ch4	
	5/26	Multiprocessors#1	Ch5	
14	5/31	Multiprocessors#2	Ch5	
	6/2	Multiprocessors#3	Ch5	HW#4
15	6/7	Final project presentation#1		
	6/9	Final project presentation#2		
16	6/14	Final exam		
	6/16	Final exam		Submit project reports