Solution of Exercises: Cache coherence

This is not a homework!

Question 1.

a.
P1: read 110, Read miss, P0's cache
P3: read 110, Read miss, MSI satisfies in memory, MOSI satisfies in P0's cache
P0: read 110, Read hit
MSI: 40 + 10 + 100 + 0 = 150 stall cycles

b.
P1: read 120, Read miss, satisfied in memory
P3: read 120, Read hit
P0: read 120, Read miss, satisfied in memory
MSI: 100 + 0 + 100 = 200 stall cycles

c.
P0: write 120 ← 80, Write miss, invalidates P3
P3: read 120, Read miss, P0's cache
P0: read 120, Read hit
MSI: 100 + 40 + 10 + 0 = 150 stall cycles

d.
P0: write 108 ← 88, Send invalidate, invalidate P3
P3: read 108, Read miss, P0's cache
P0: write 108 ← 98, Send invalidate, invalidate P3
MSI: 15 + 40 + 10 + 15 = 80 stall cycles