OrCAD, Pspice 복습

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OrCAD and PSpice

PSpice is a SPICE analog circuit and digital logic simulation program for Microsoft Windows. The name is an acronym for Personal Simulation Program with Integrated Circuit Emphasis.

http://en.wikipedia.org/wiki/PSPICE

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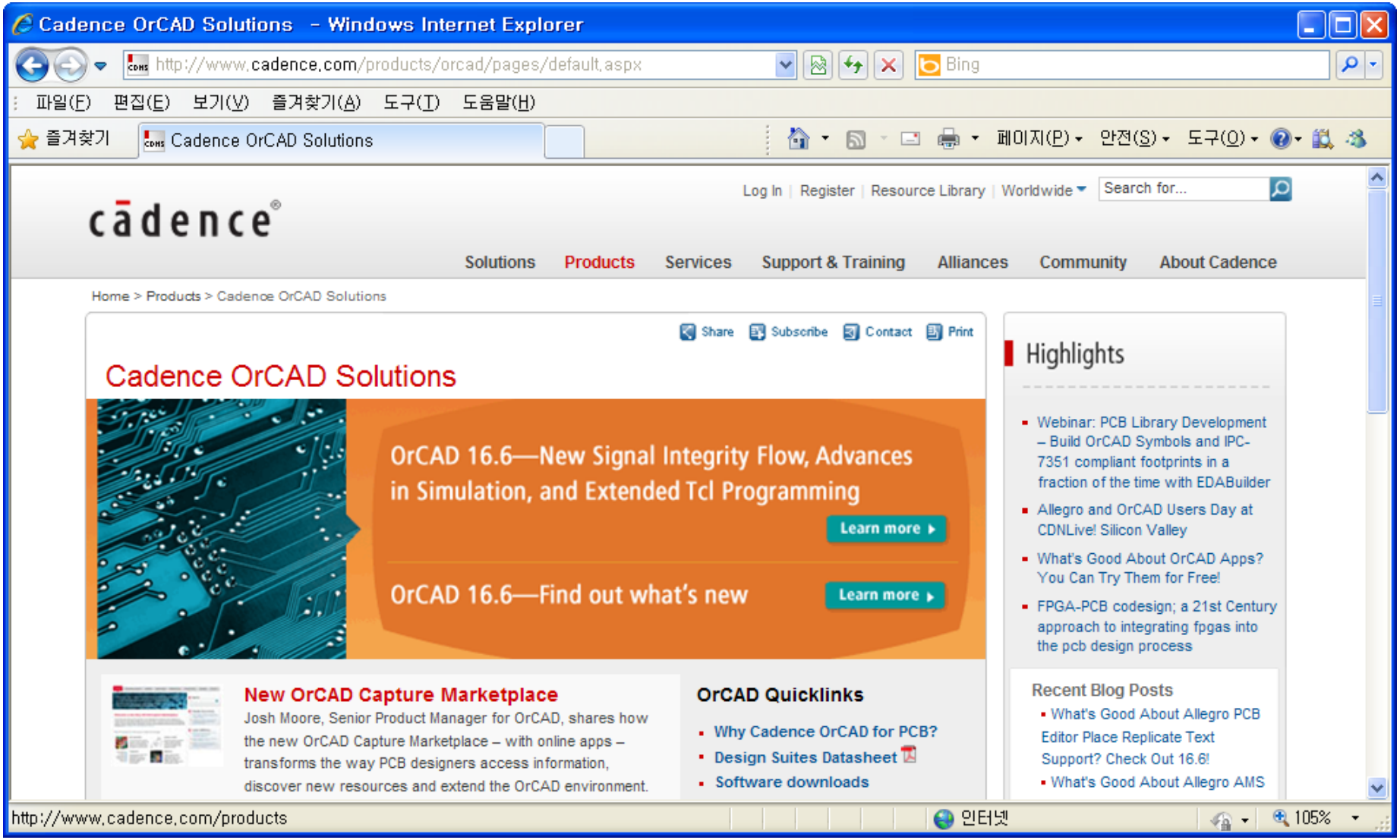
OrCAD and PSpice



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OrCAD and PSpice

Products

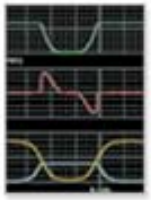
OrCAD FPGA System Planner new
Provides a complete, scalable solution for FPGA-PCB co-design that allows users to create an optimum correct-by-construction pin assignment.
Read more »

OrCAD Capture and Capture CIS
Offers full-featured schematic editing for fast, intuitive design capture with hierarchical and variant capabilities. Component information system (CIS) promotes use of preferred, current parts to accelerate the design process and reduce project costs.
Read more »

OrCAD PCB Designer
Offers a proven, scalable, easy-to-use PCB editing and routing solution. Delivers a comprehensive feature set and seamless PCB design environment to take designs from concept to production.
Read more »

ActiveParts Portal new
Automates the process of part selection and extends the reach of engineers. APP is FREE for users on the most current releases of OrCAD Capture CIS
Read more »

OrCAD Signal Explorer
Enables pre- and post-layout signal integrity analysis and topology design/exploration at any stage of the design cycle improving circuit reliability and performance to reduce prototypes and re-spins.
Read more »



PSpice A/D and Advanced Analysis
Provides simulation of analog/mixed-signal circuits as well as analysis for by determining which components are over-stressed and component yields. Full integration with OrCAD Capture improves productivity and data integrity.
Read more »

http://www.cadence.com/products/orcad/Pages/default.aspx

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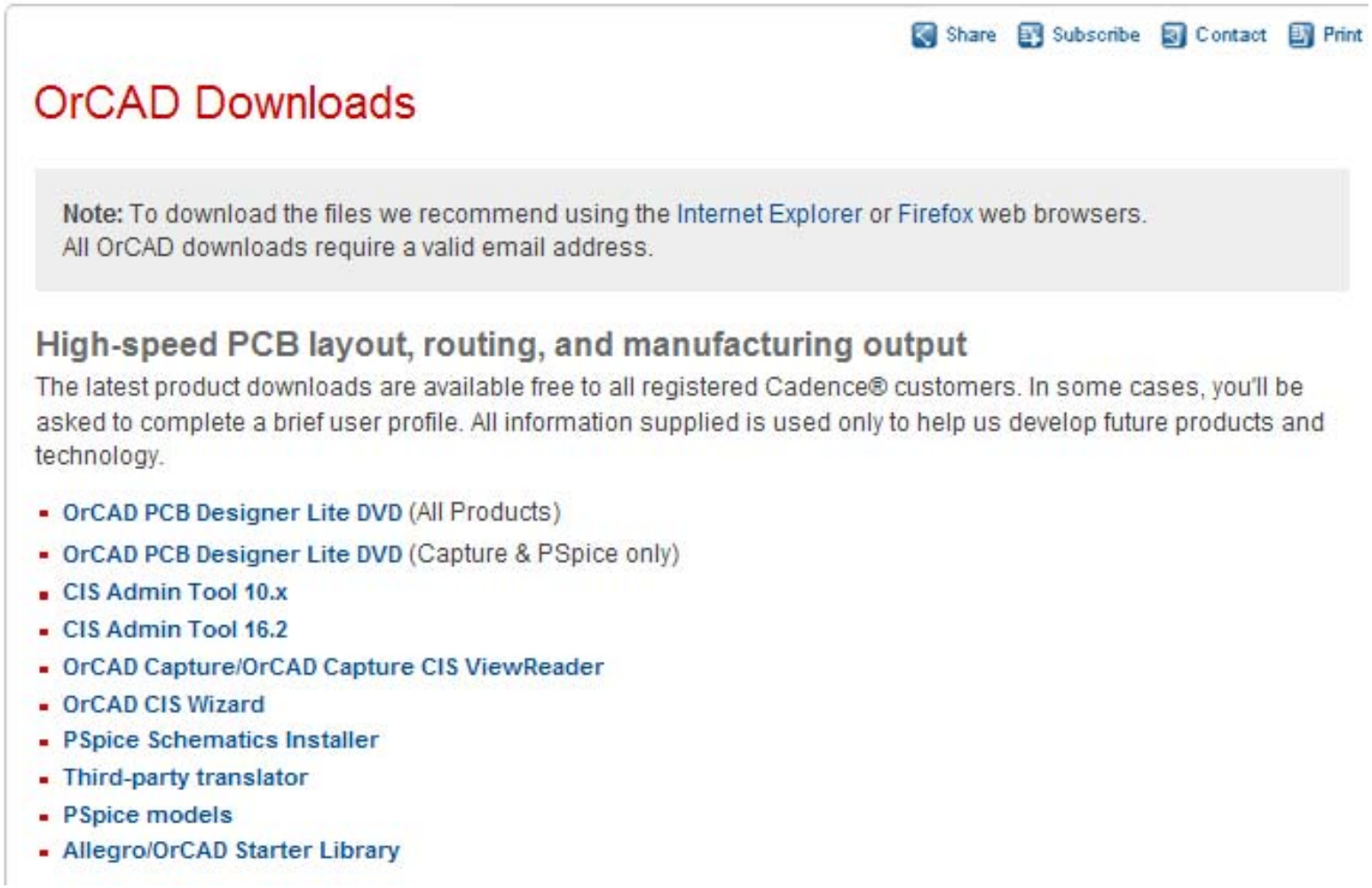
OrCAD and PSpice



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OrCAD Downloads

Note: To download the files we recommend using the Internet Explorer or Firefox web browsers.
All OrCAD downloads require a valid email address.

High-speed PCB layout, routing, and manufacturing output

The latest product downloads are available free to all registered Cadence® customers. In some cases, you'll be asked to complete a brief user profile. All information supplied is used only to help us develop future products and technology.

- **OrCAD PCB Designer Lite DVD** (All Products)
- **OrCAD PCB Designer Lite DVD** (Capture & PSpice only)
- **CIS Admin Tool 10.x**
- **CIS Admin Tool 16.2**
- **OrCAD Capture/OrCAD Capture CIS ViewReader**
- **OrCAD CIS Wizard**
- **PSpice Schematics Installer**
- **Third-party translator**
- **PSpice models**
- **Allegro/OrCAD Starter Library**

http://www.cadence.com/products/orcad/pages/downloads.aspx

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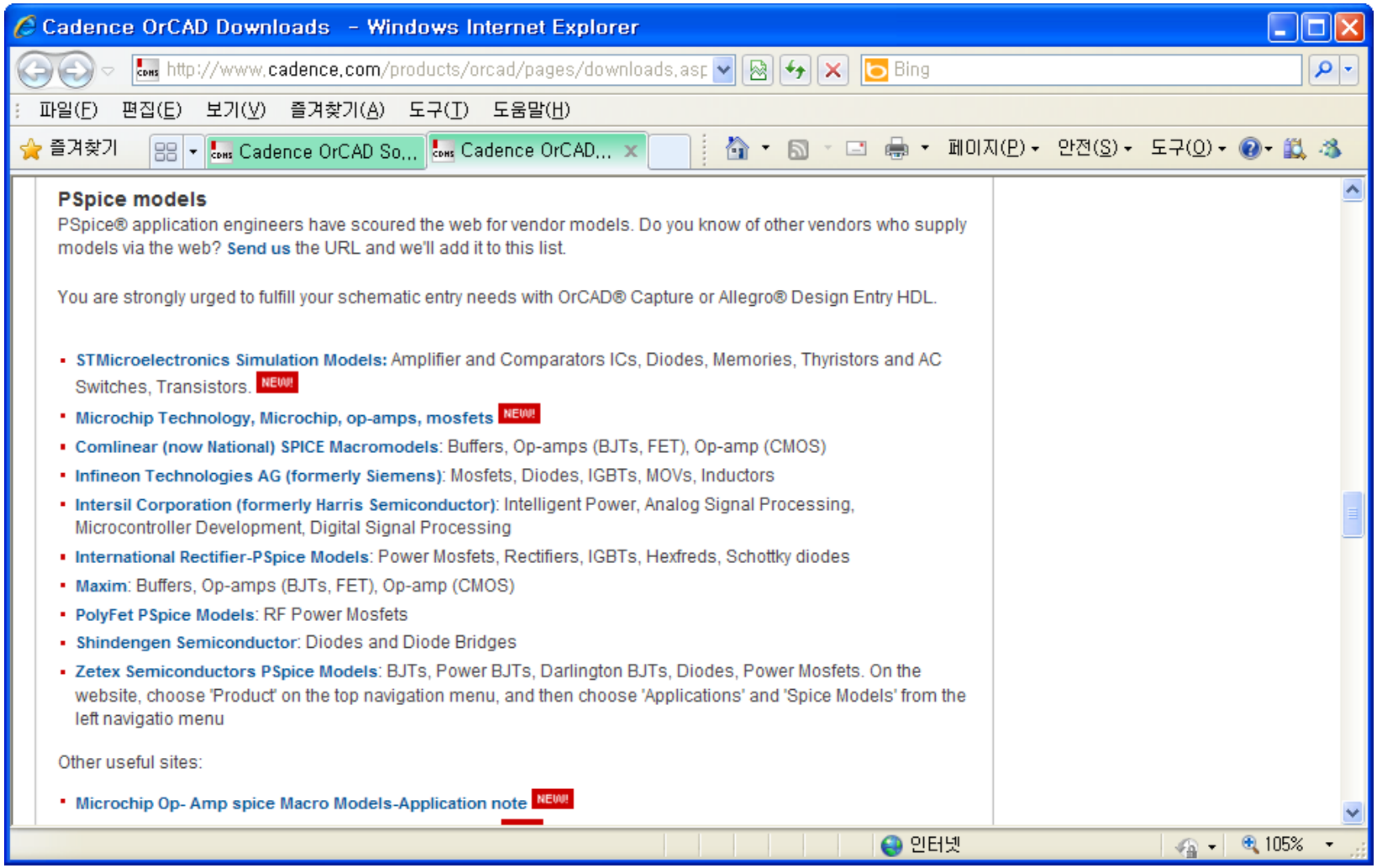
OrCAD and PSpice



http://www.cadence.com/products/orcad/pages/downloads.aspx

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OrCAD and PSpice

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Email: jhchoi@newlinktek.com
Web site: www.newlinktek.com

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Web site: www.veritytech.co.kr
Serves Korea.

http://www.cadence.com/alliances/channel_partner/pages/default.aspx

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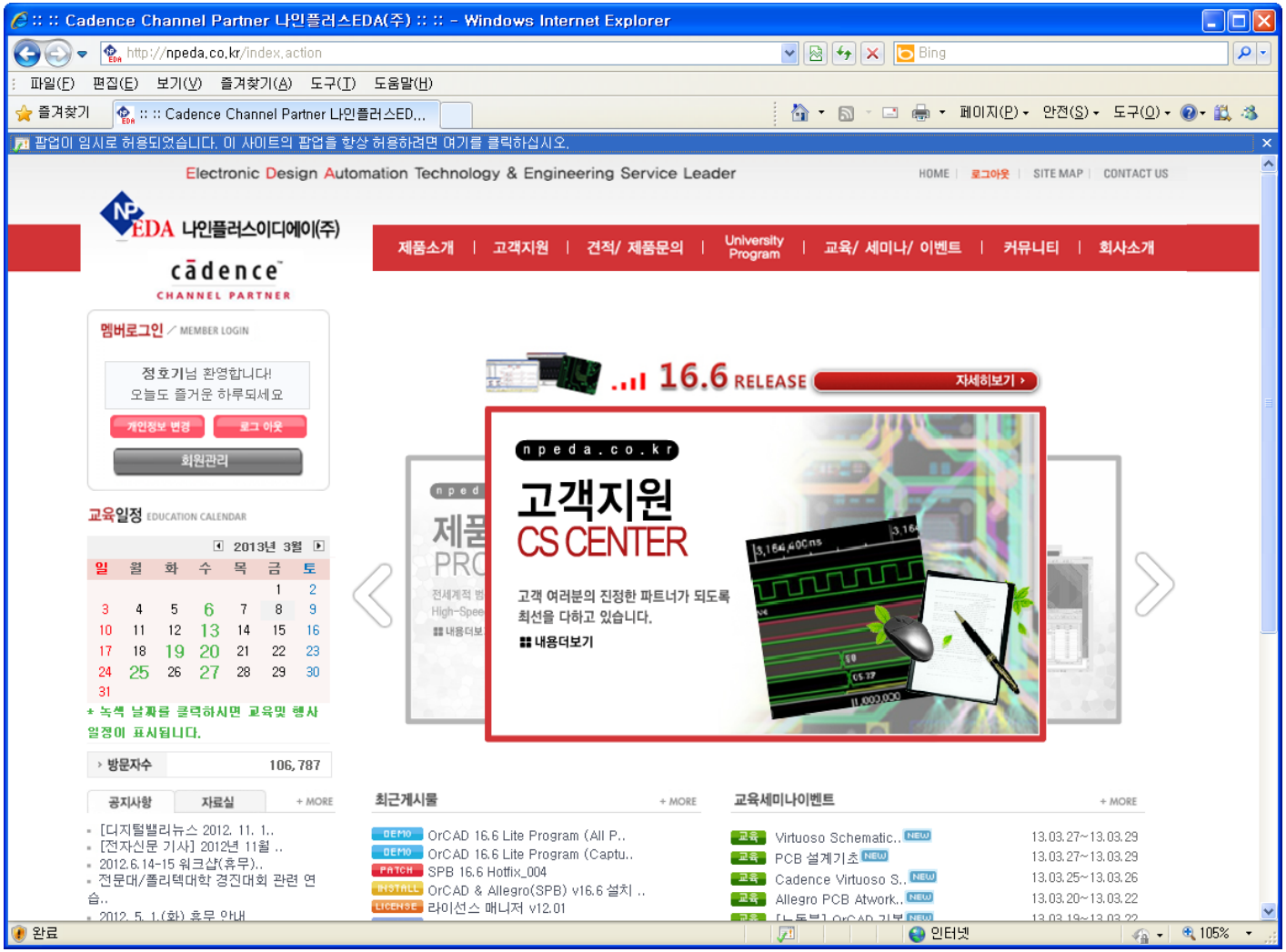
OrCAD 16.6 Lite Program



http://npeda.co.kr/index.action

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OrCAD 16.6 Lite Program

OrCAD 16.6 Lite Program (Capture & Pspice Only)

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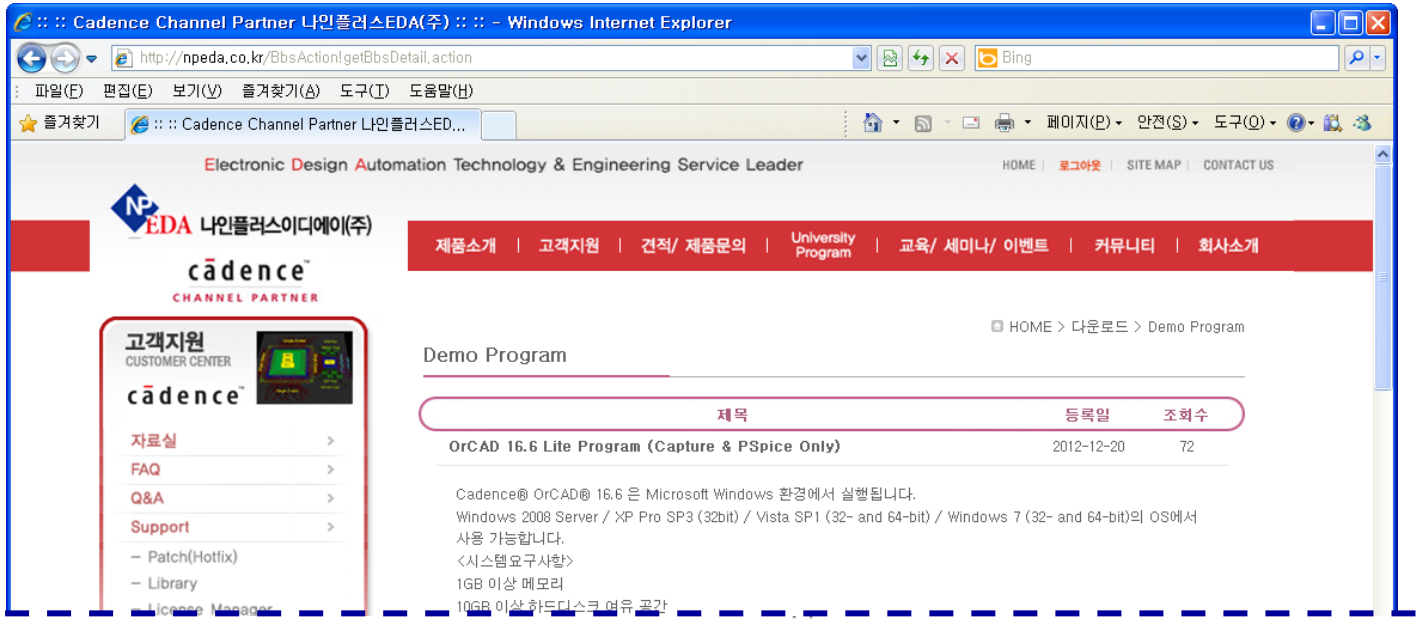
OrCAD 16.6 Lite Program



■ Sensitivity Analysis
- ❑ Only one measurement specification is allowed.
- ❑ A maximum of three devices with tolerance are supported.
- ❑ Maximum of 20 runs are supported.

■ Encrypted parameterized models cannot be simulated.

■ The Optimizer Random Engine can make a maximum of 5 runs.

다운로드

(위 파일은 Zip파일로 압축되어 있습니다. 임의의 폴더에 압축을 푸신 다음 실행하시면 됩니다.)

(해당 자료에 대하여 링크하거나 재배포 행위를 금합니다.)

http://npeda.co.kr/BbsAction!getBbsDetail.action

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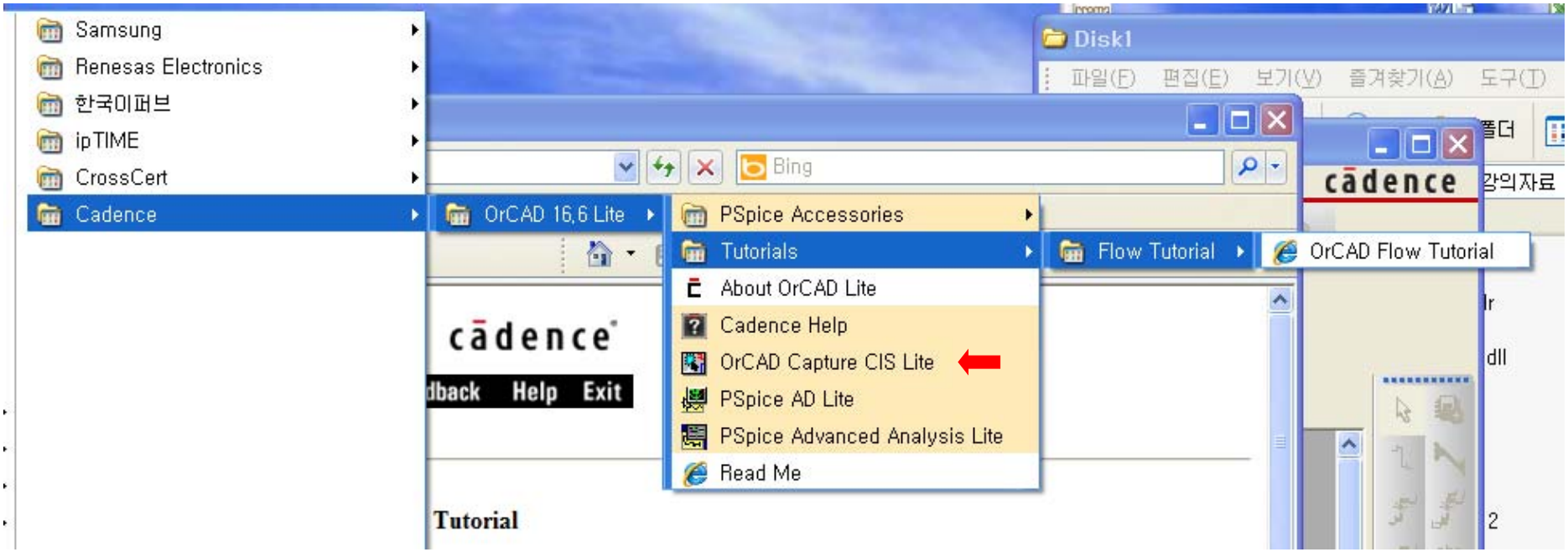

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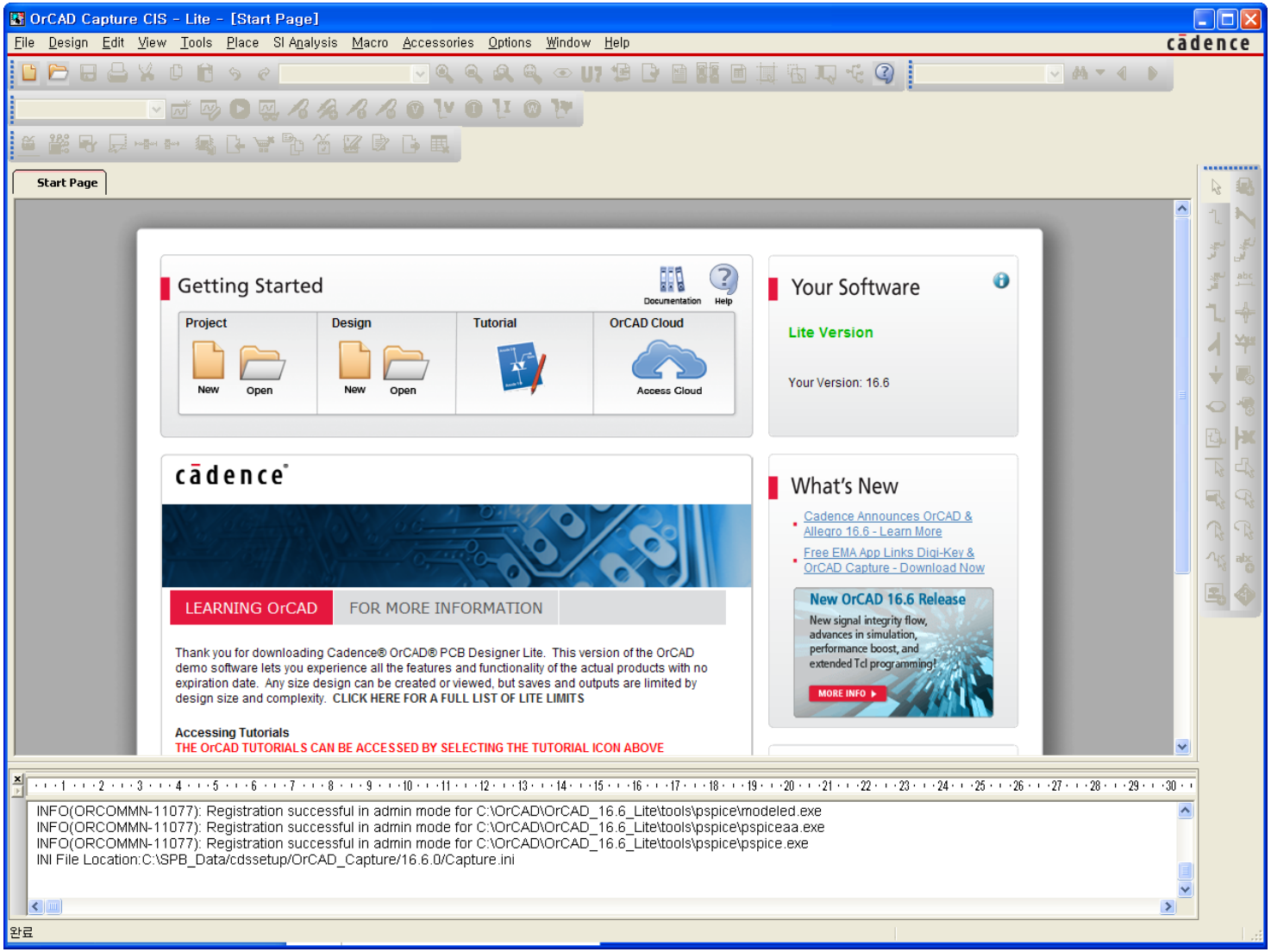

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OrCAD 16.6 Lite Program

Cadence® OrCAD® 16.6 은 Microsoft Windows 환경에서 실행됩니다.
Windows 2008 Server / XP Pro SP3 (32bit) / Vista SP1 (32- and 64-bit) / Windows 7 (32- and 64-bit)의 OS에서 사용 가능합니다.

<시스템요구사항>
1GB 이상 메모리
10GB 이상 하드디스크 여유 공간
300MB 이상 가상메모리
CD-ROM/ 드라이브
해상도 1024 x 768 이상의 64,000 컬러 윈도우 디스플레이 (1280 x 1024 권장)
OrCAD PCB Editor는 그래픽 카드가 OpenGL 지원해야 함

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OrCAD 16.6 Lite Program

OrCAD Capture CIS Lite

■ You cannot save designs that have more than 75 nets, including the hierarchical blocks in the design. You can still view or create larger designs.

■ You cannot save a design with more than 60 parts, including the hierarchical blocks in the design. You can still view or create larger designs.

■ You cannot have more than 1000 parts in the Capture CIS database.

■ The Internet Component Assistant (ICA) tab in the CIS Explorer window opens the About ActiveParts page (www.activeparts.com) and not the component search page.

■ You cannot create parts with more than 100 pins.

■ The Capture FPGA flow is not available.

■ You cannot validate Electrical Csets

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OrCAD 16.6 Lite Program

PSpice A/D Lite

■ Circuit simulation limited to circuits with up to 75 nodes, 20 transistors, no sub-circuit limits but 65 digital primitive devices, and 10 transmission lines (ideal or non-ideal) with not more than four pairwise coupled lines.

■ Device characterization and parameterized part creation using the PSpice Model Editor limited to diodes.

■ No limit to stimulus generation using Stimulus Editor.

■ Sample model library named eval.lib (containing analog and digital parts) and evalp.lib (containing parameterized parts) are provided.

■ The library nomd.lib is configured for simulations. The nomd.lib file references the set of libraries that can be used with the lite version.

■ You cannot simulate parameterized parts that are not from the evalp.lib library. This library consists of parametrized resistor, source, and diode.

■ You cannot use Level 3 of Core model (Tabrizi), MOSFET BSIM 3.2, or MOSFET BSIM 4 models.

■ Displays only simulation data created using the lite version of the simulator.

■ Magnetic Parts Editor allows you to design power transformers only. The database shipped with Magnetic Parts Editor cannot be edited and contains a single core.

■ The Model Import Wizard supports parts and simulation models that have a maximum of two pins or two terminals, respectively.

■ The maximum nodes in a digital circuit can be equal to or less than 250.

■ The non-ideal Tline is limited to 4.

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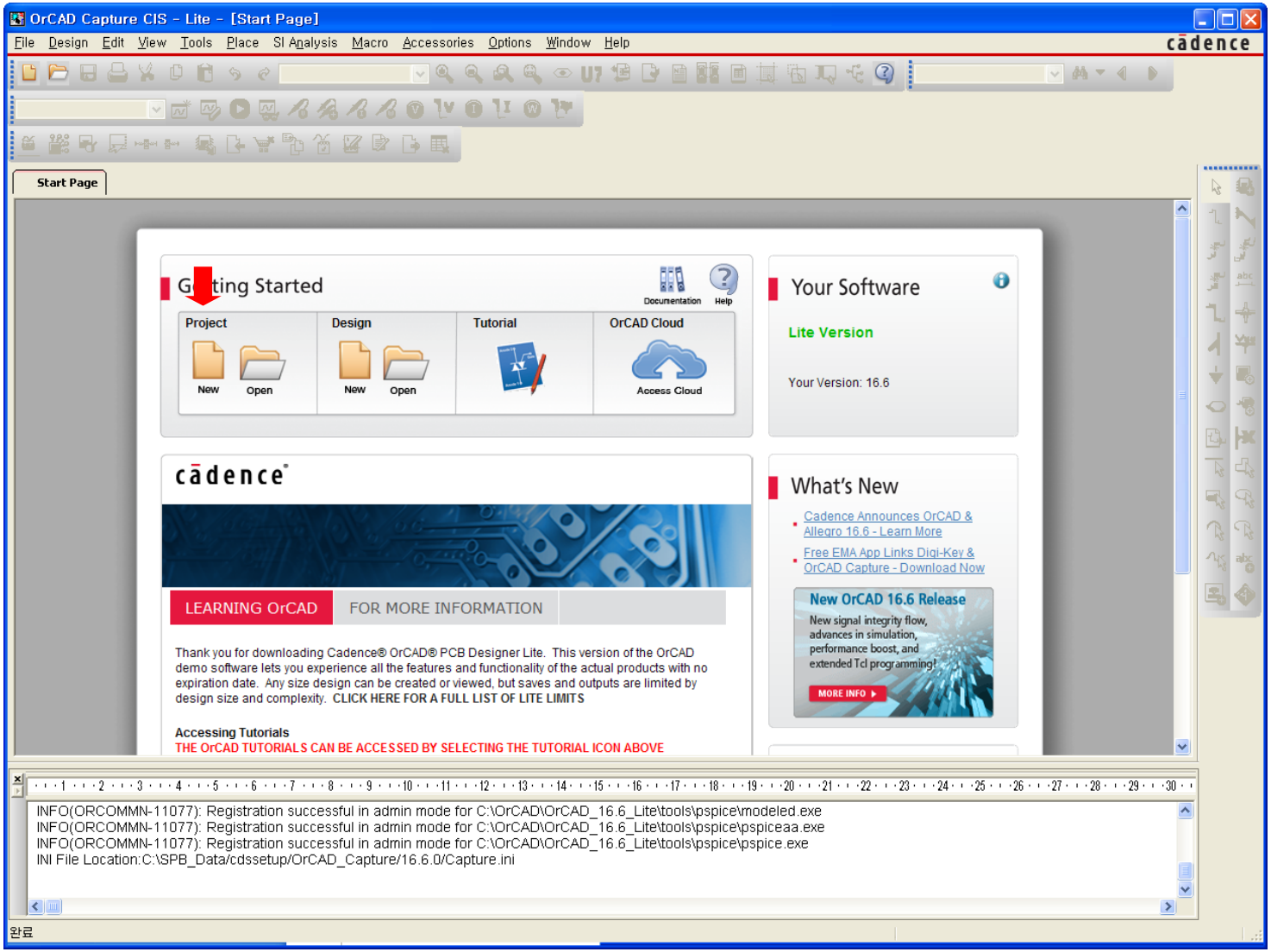
Project



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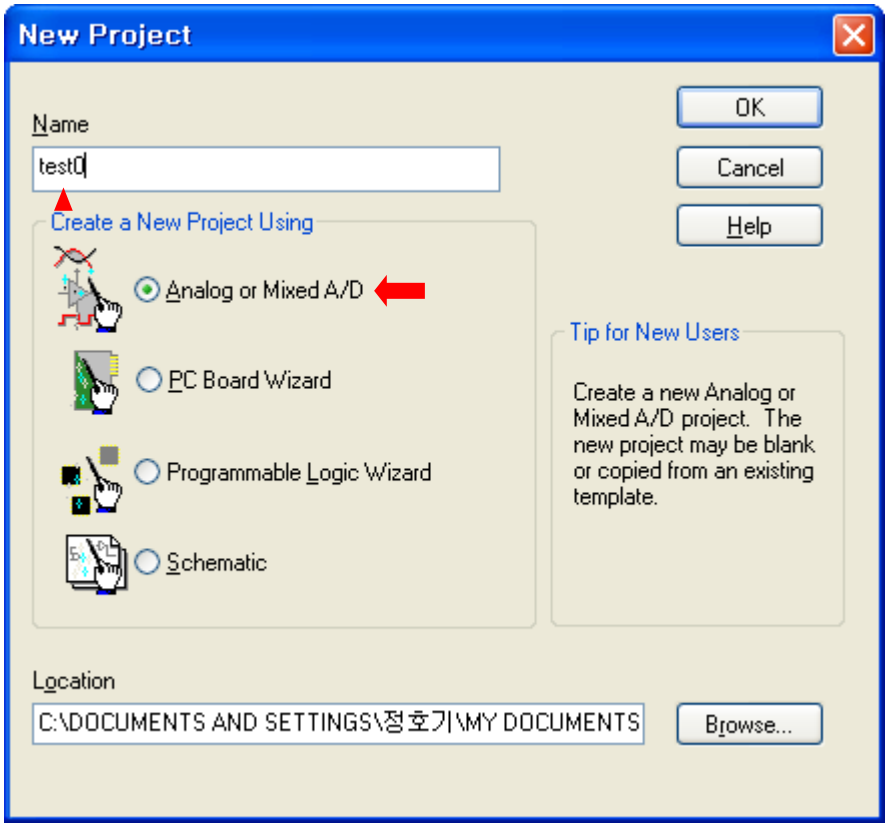

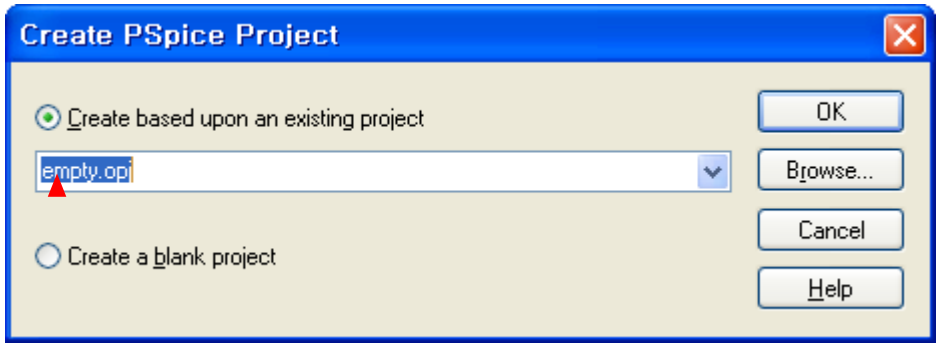

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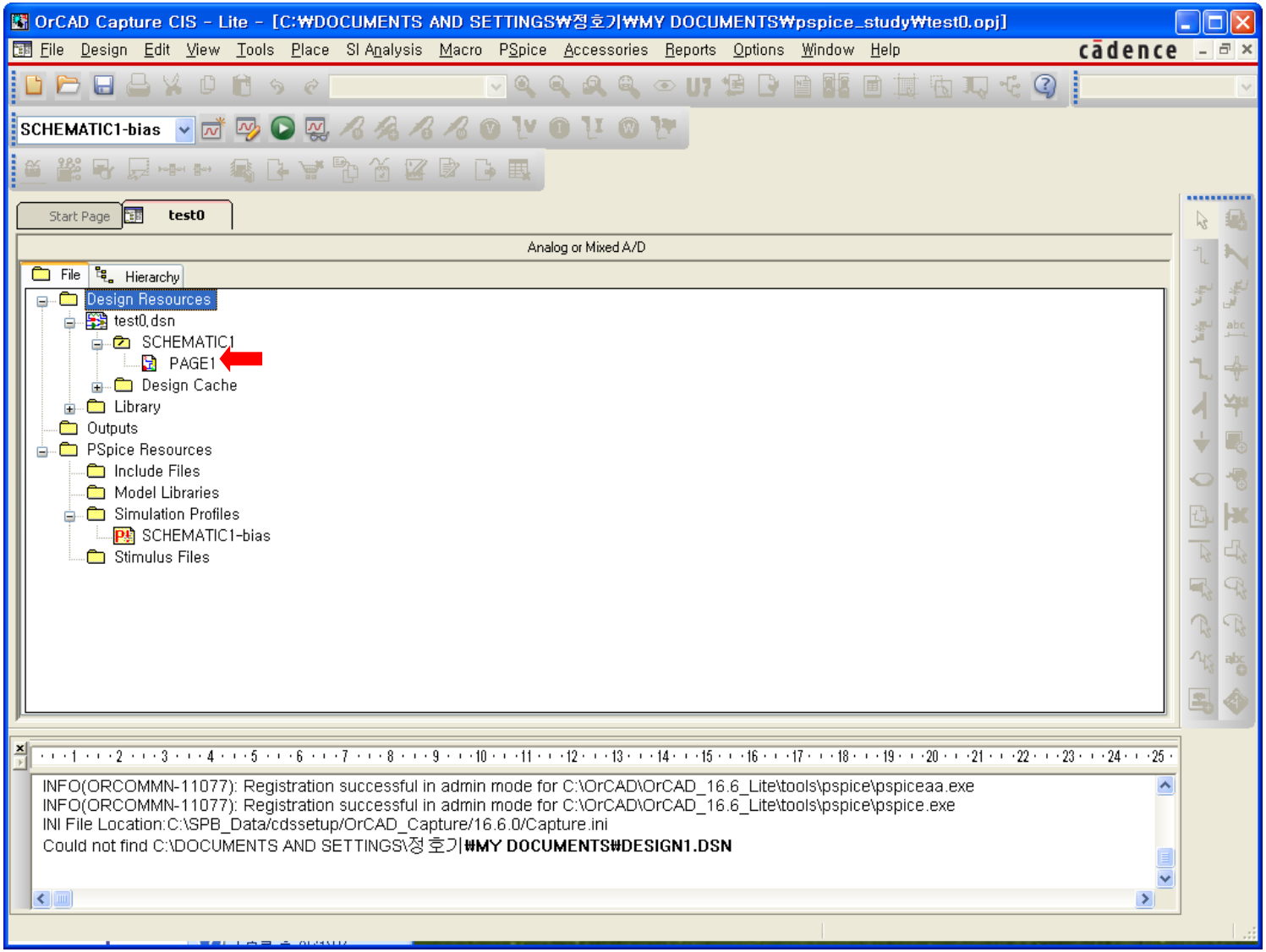
Project



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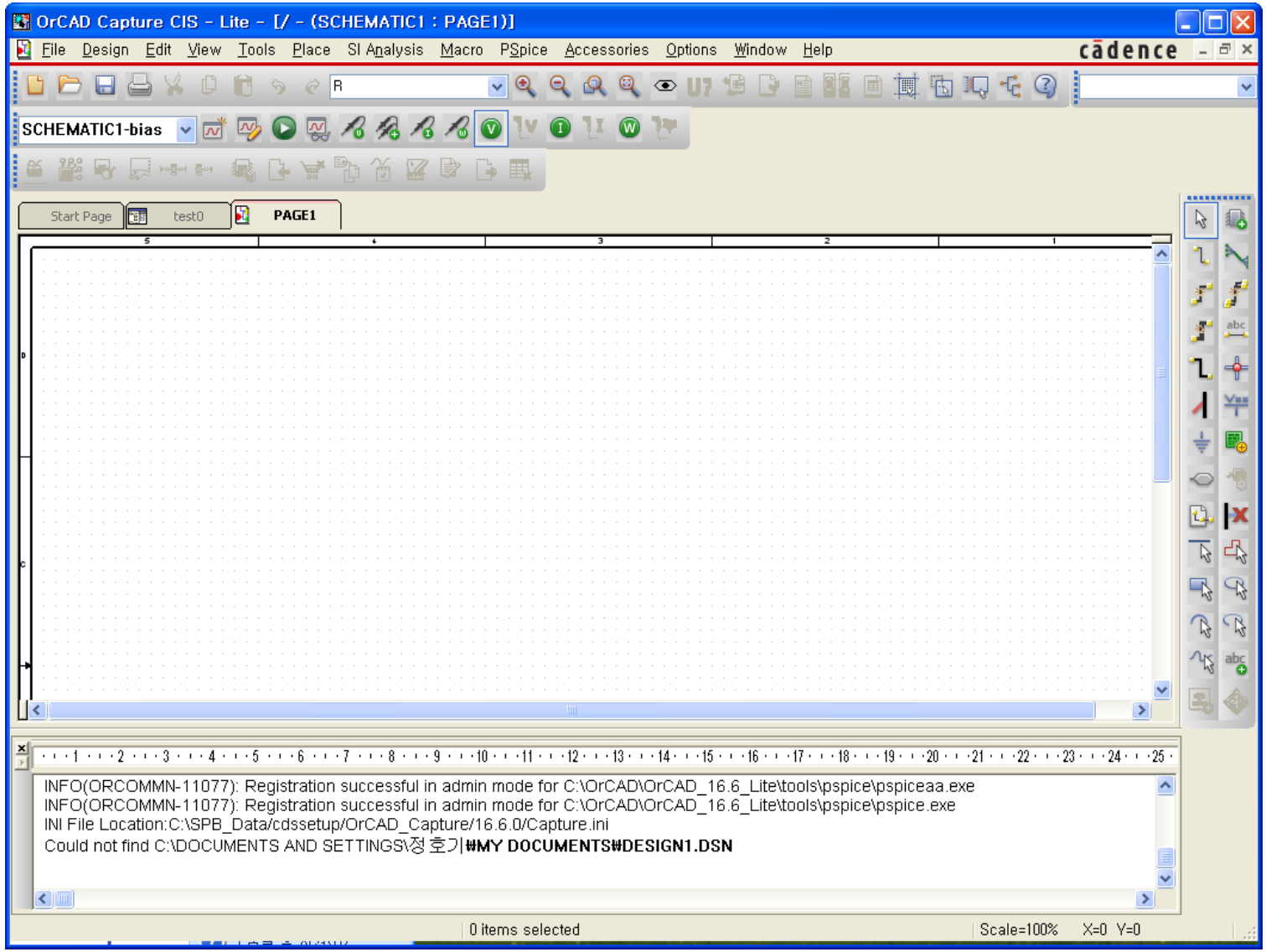
Design



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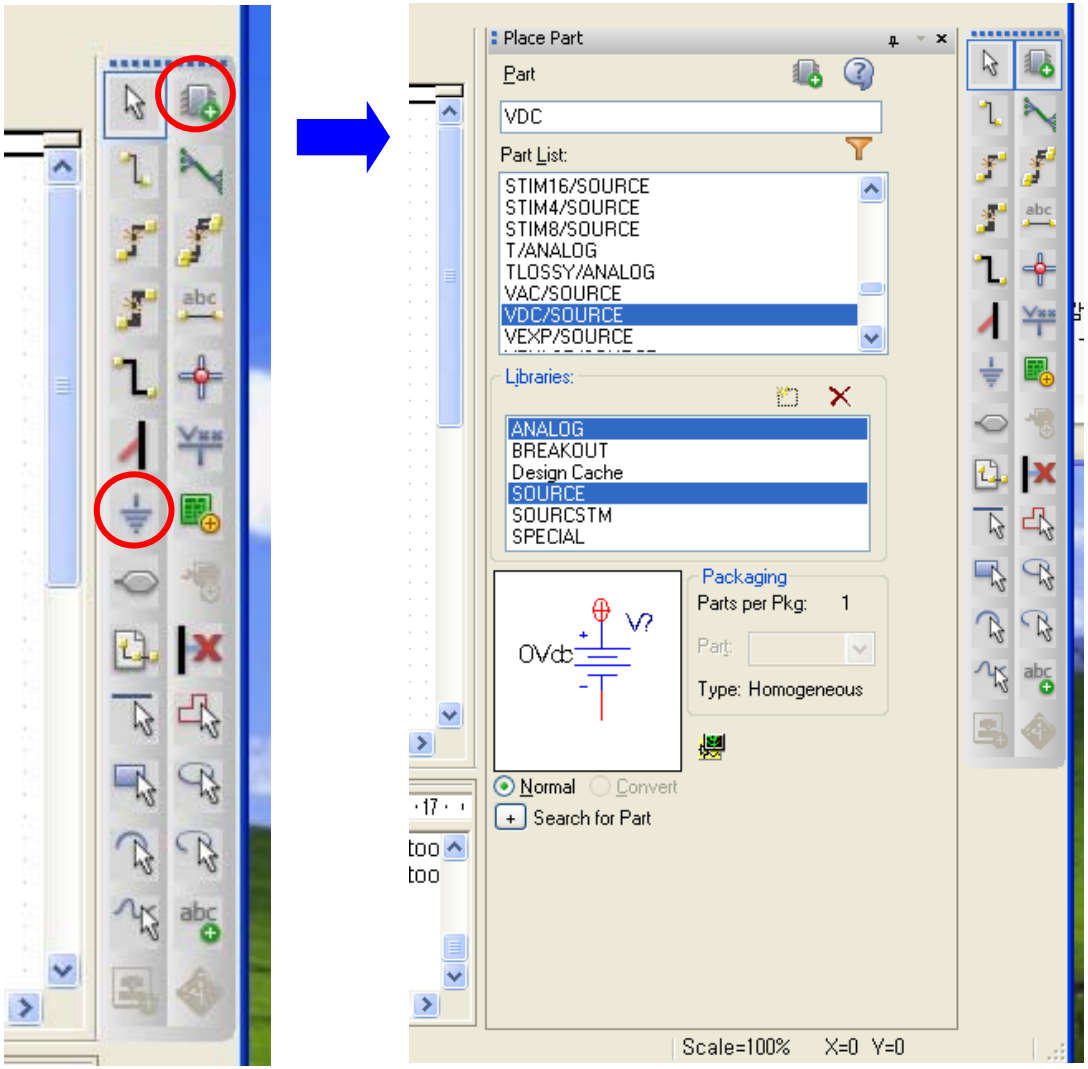
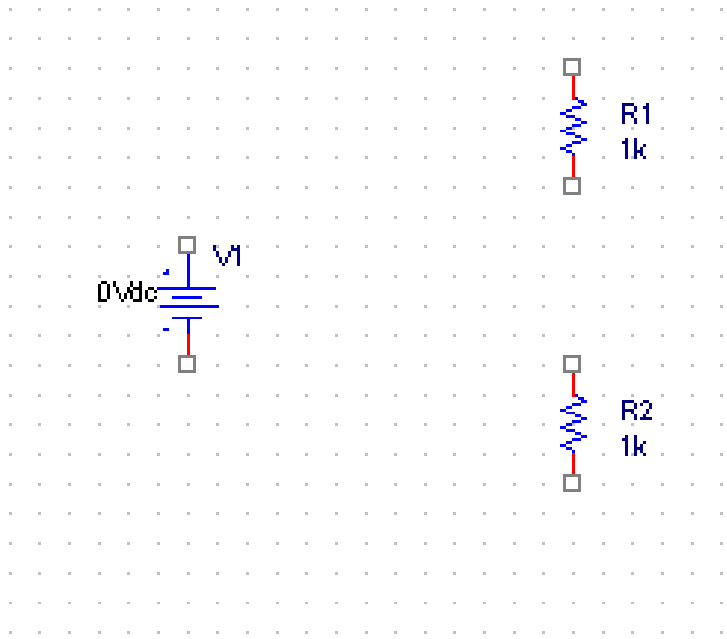
Design





Libraries>>Part List

SOURCE>>VDC

ANALOG>>R

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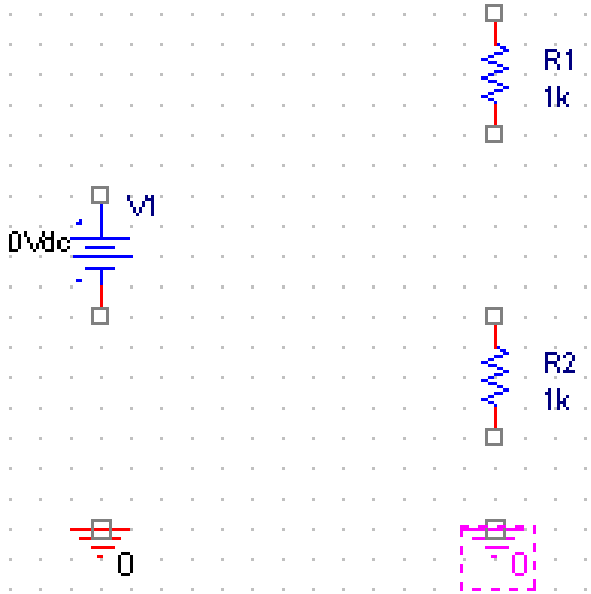
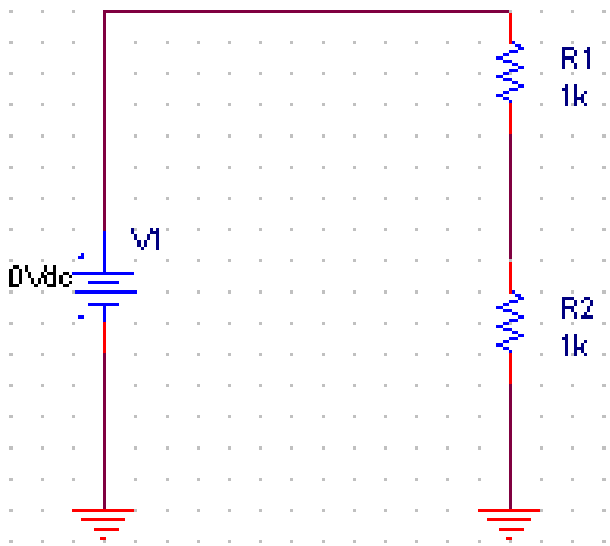


CAPSYM>>0/CAPSYM



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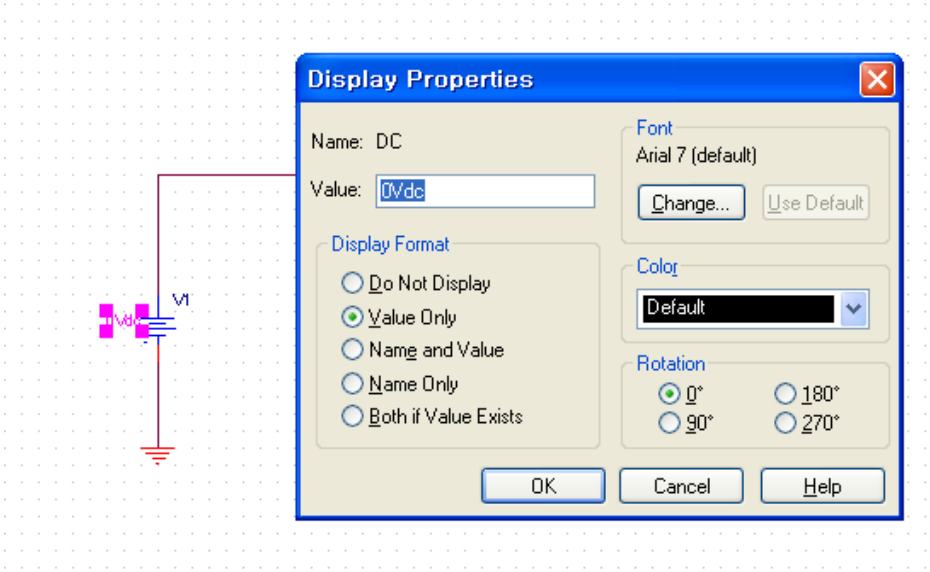

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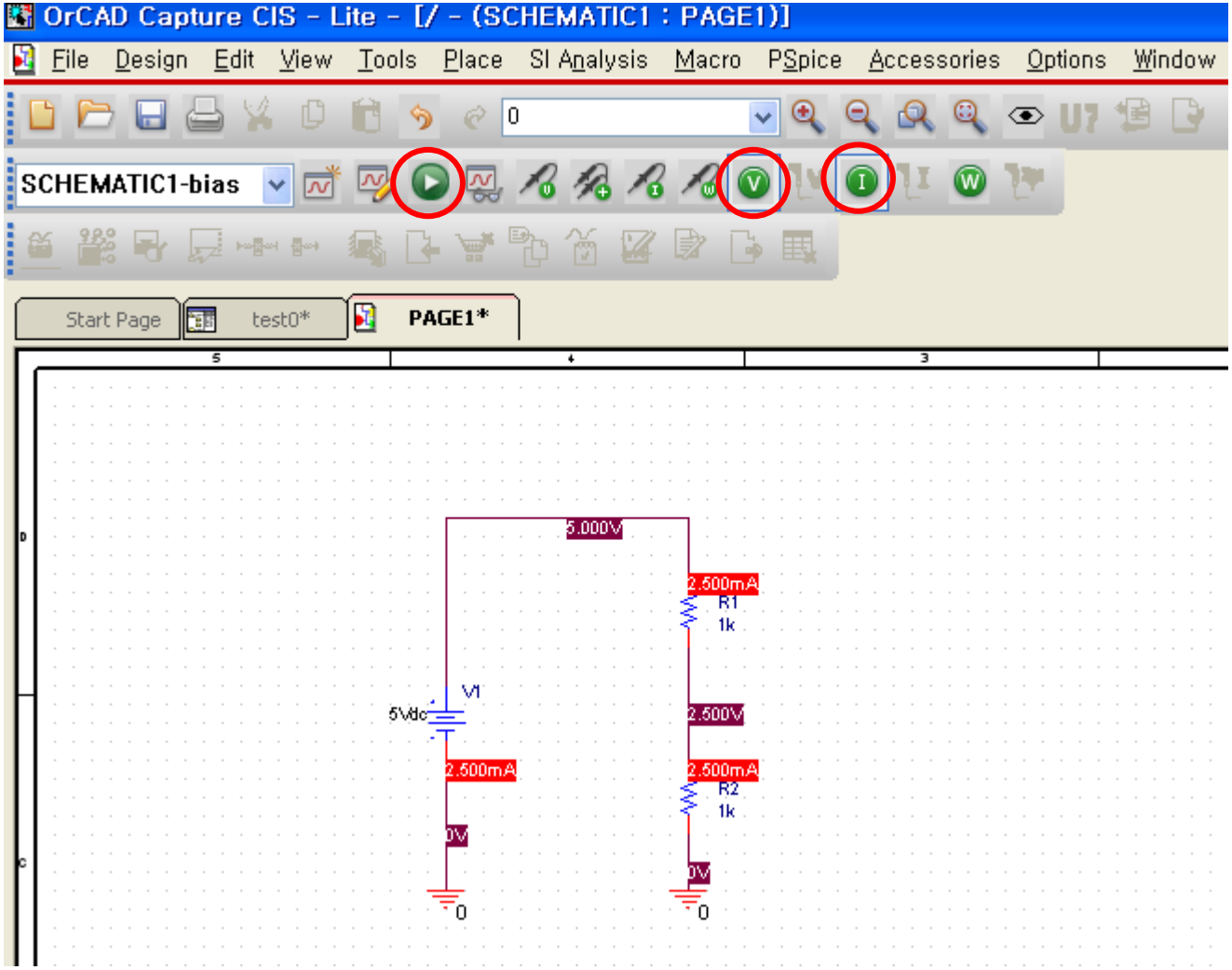
Simulation



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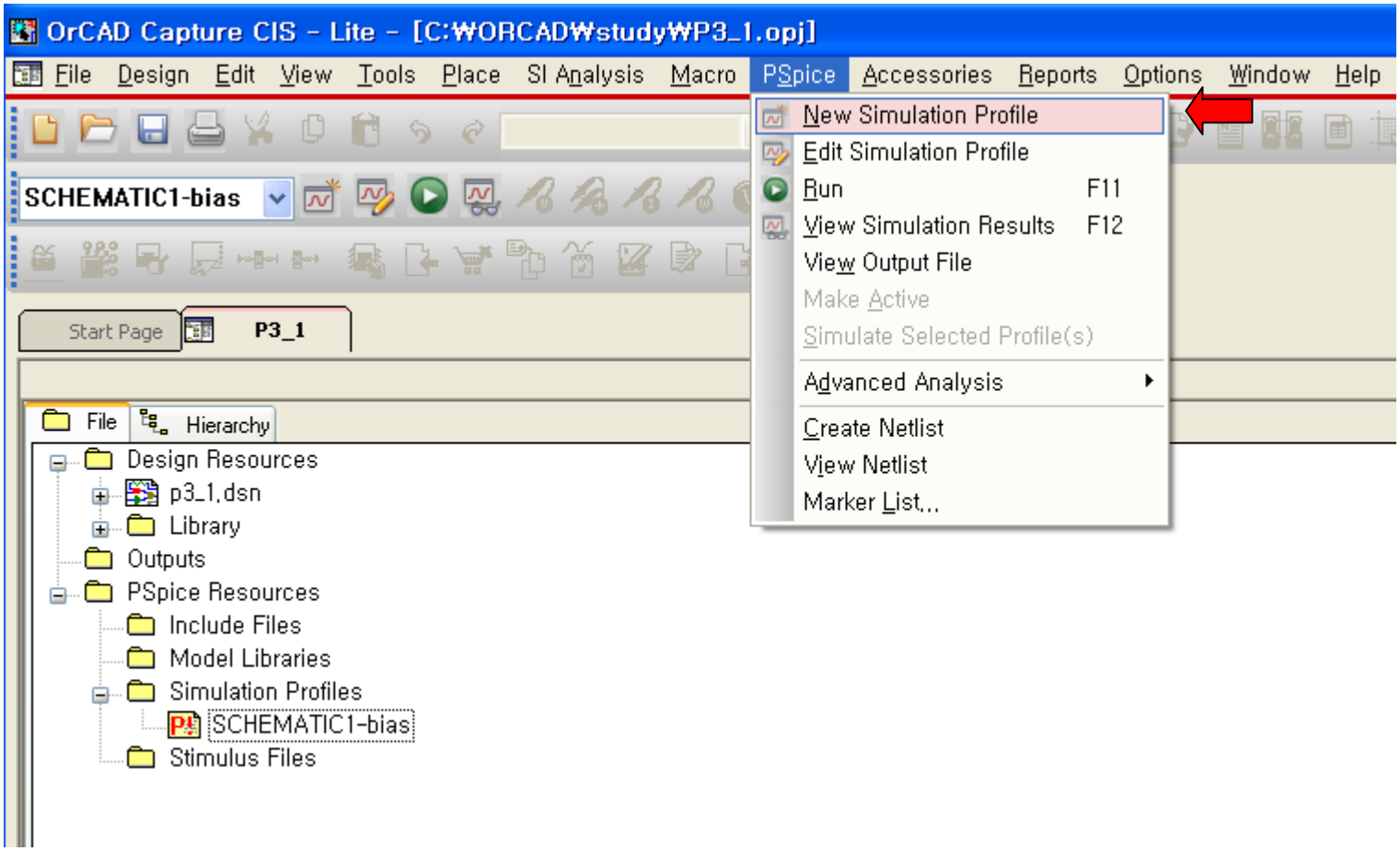
Simulation Profile 추가



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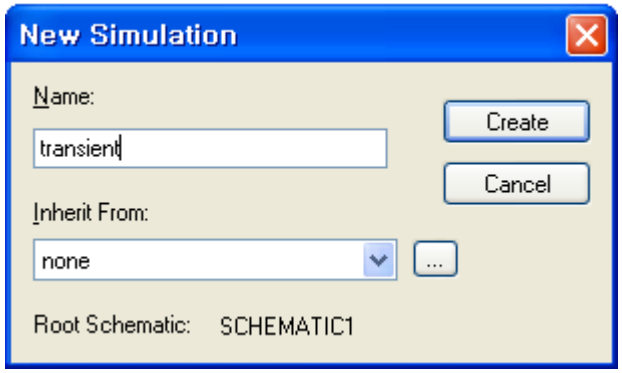

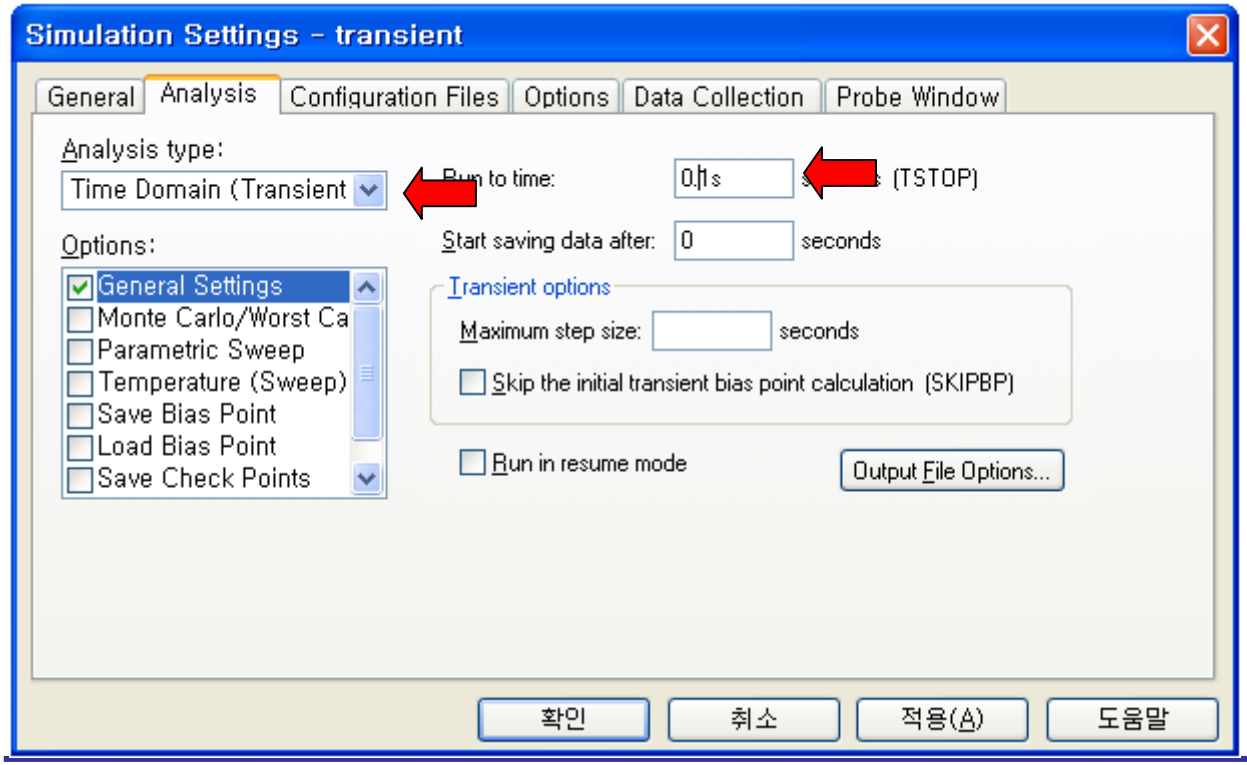

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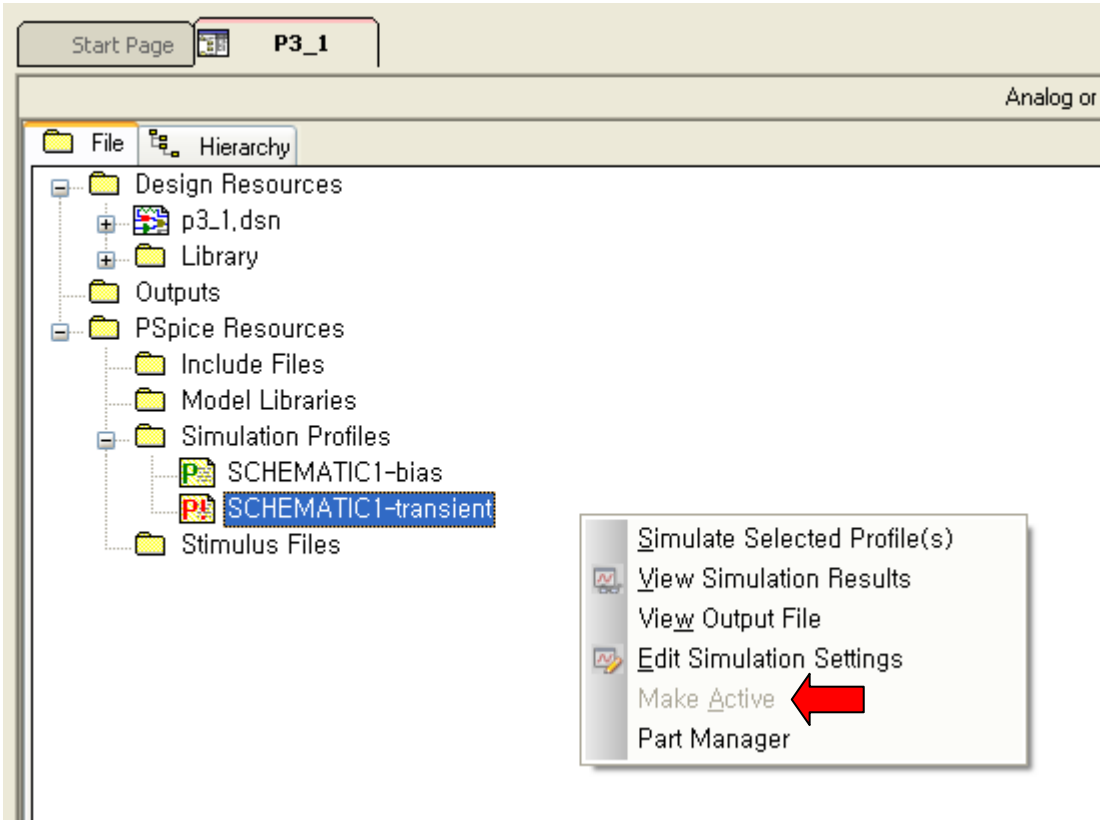

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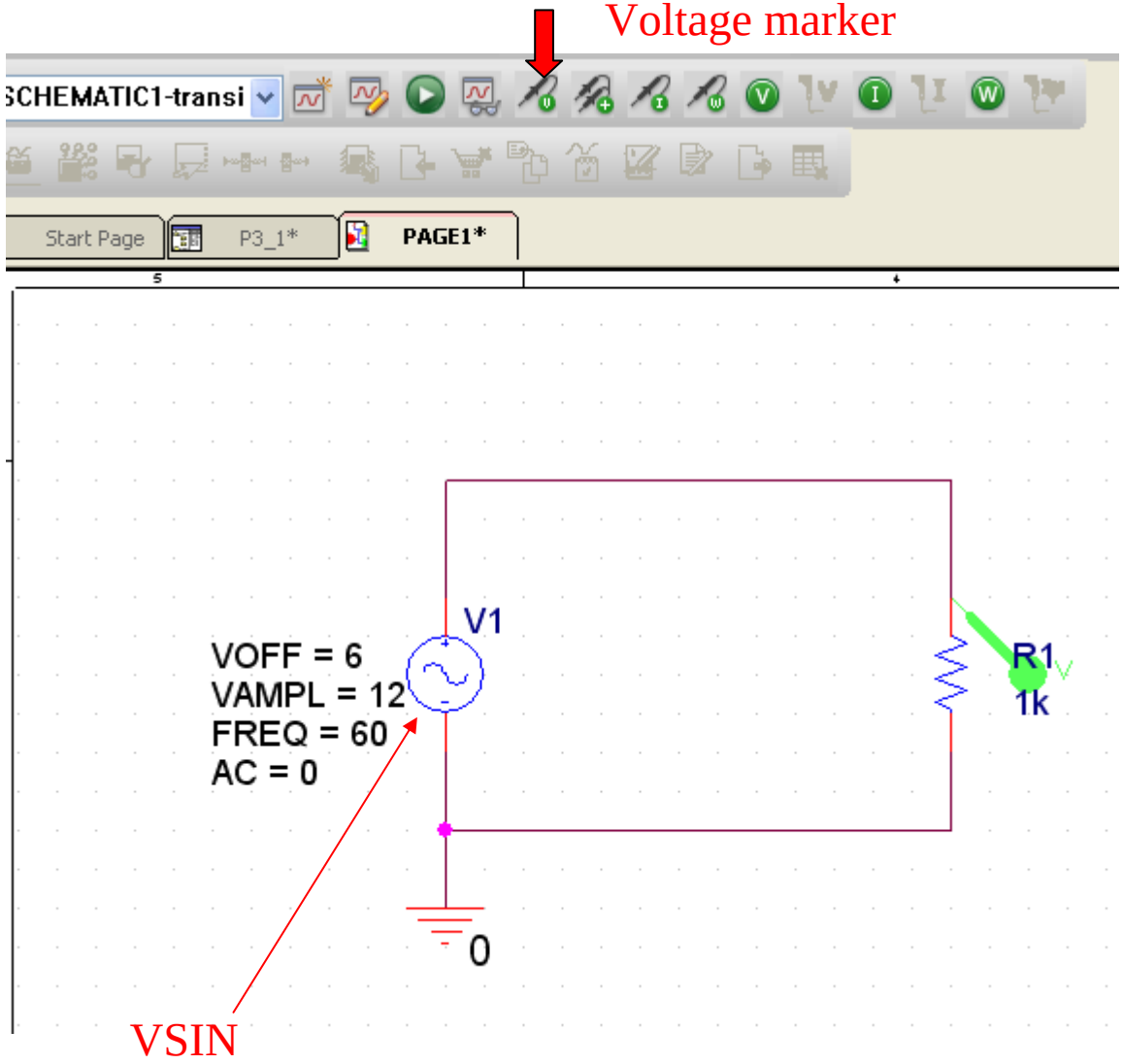
Marker



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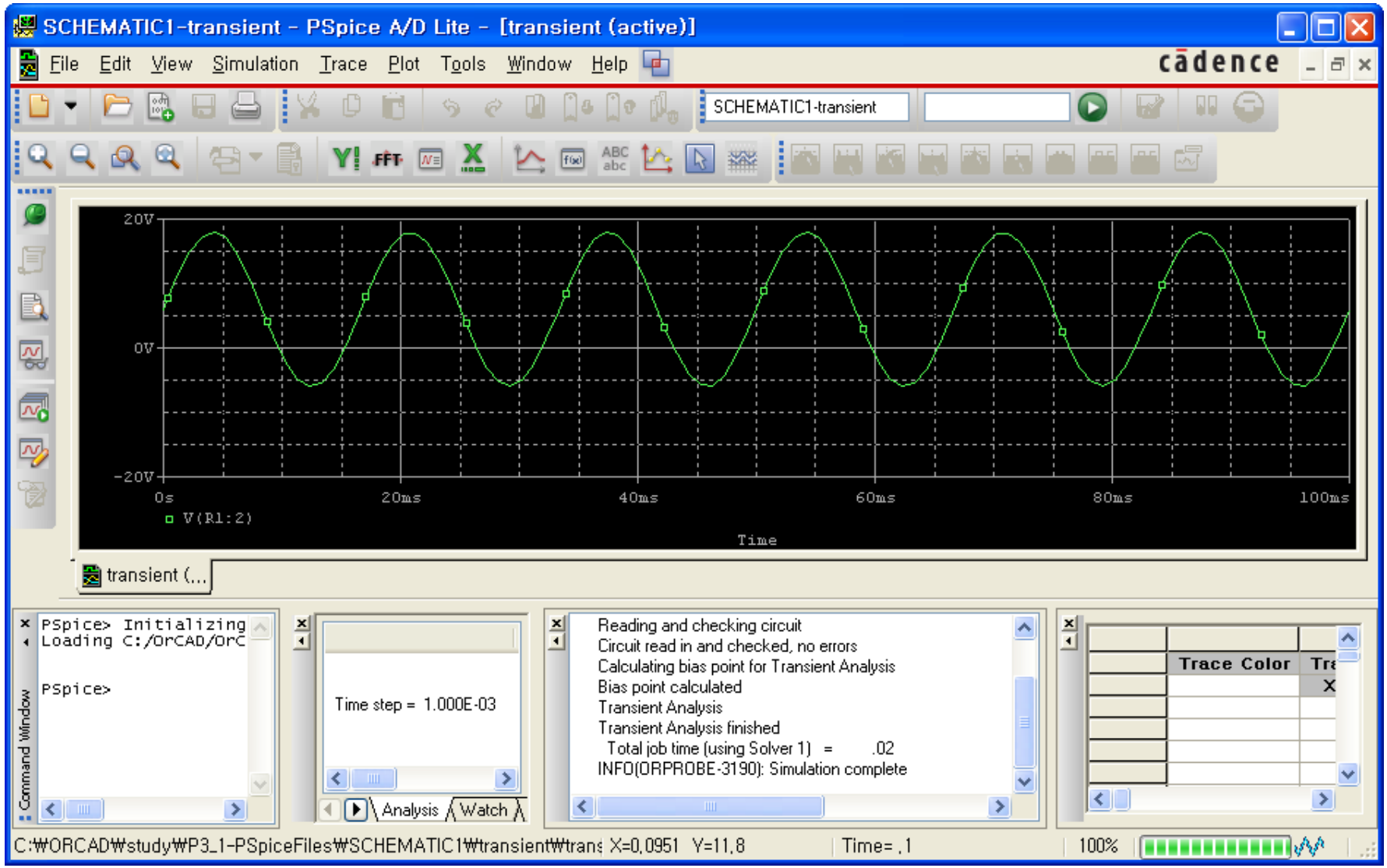
Simulation 결과



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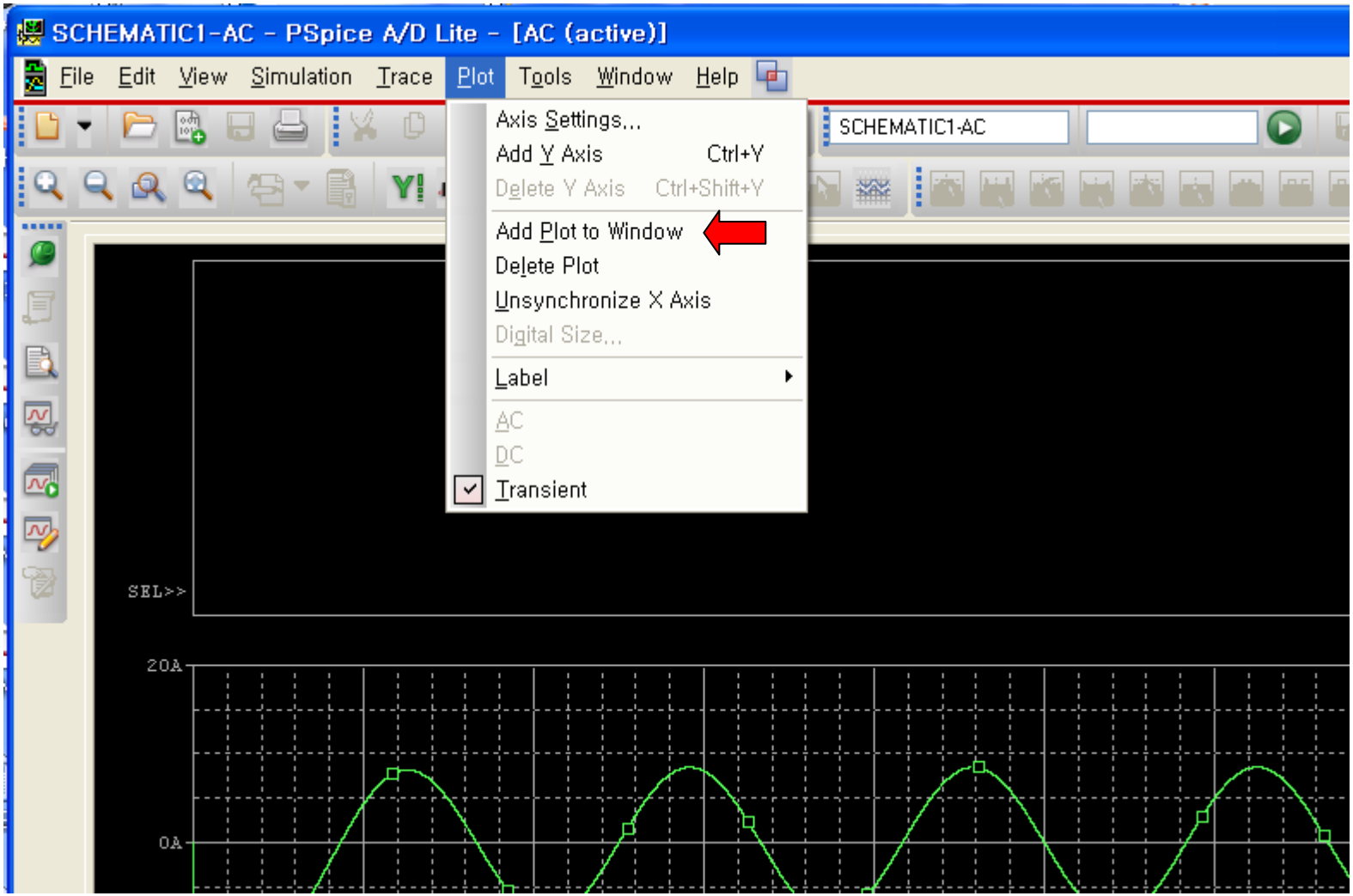
Plot 추가



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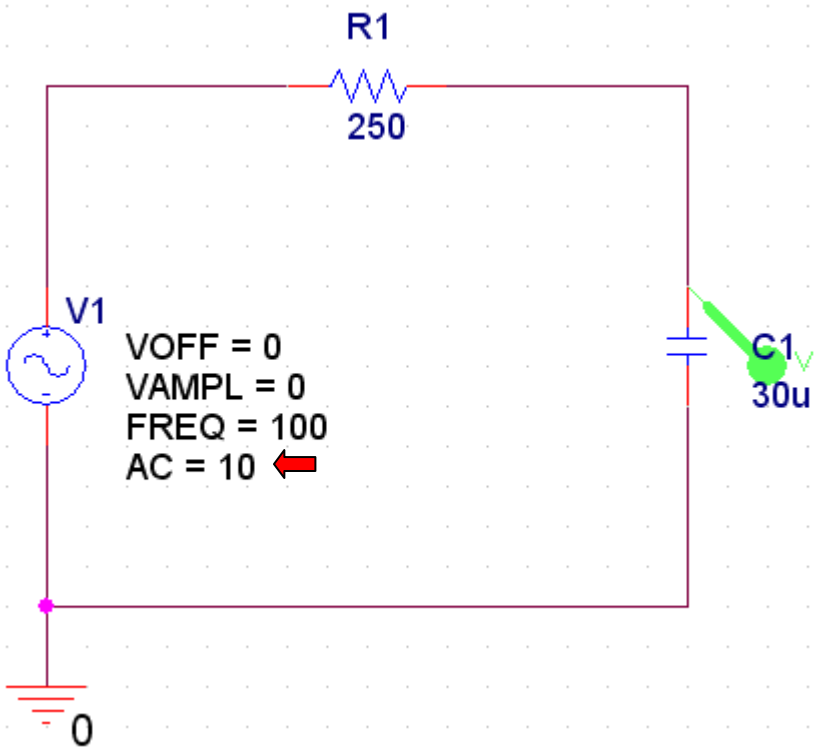
AC SWEEP

문) 아래 회로의 주파수 응답을 구하라.



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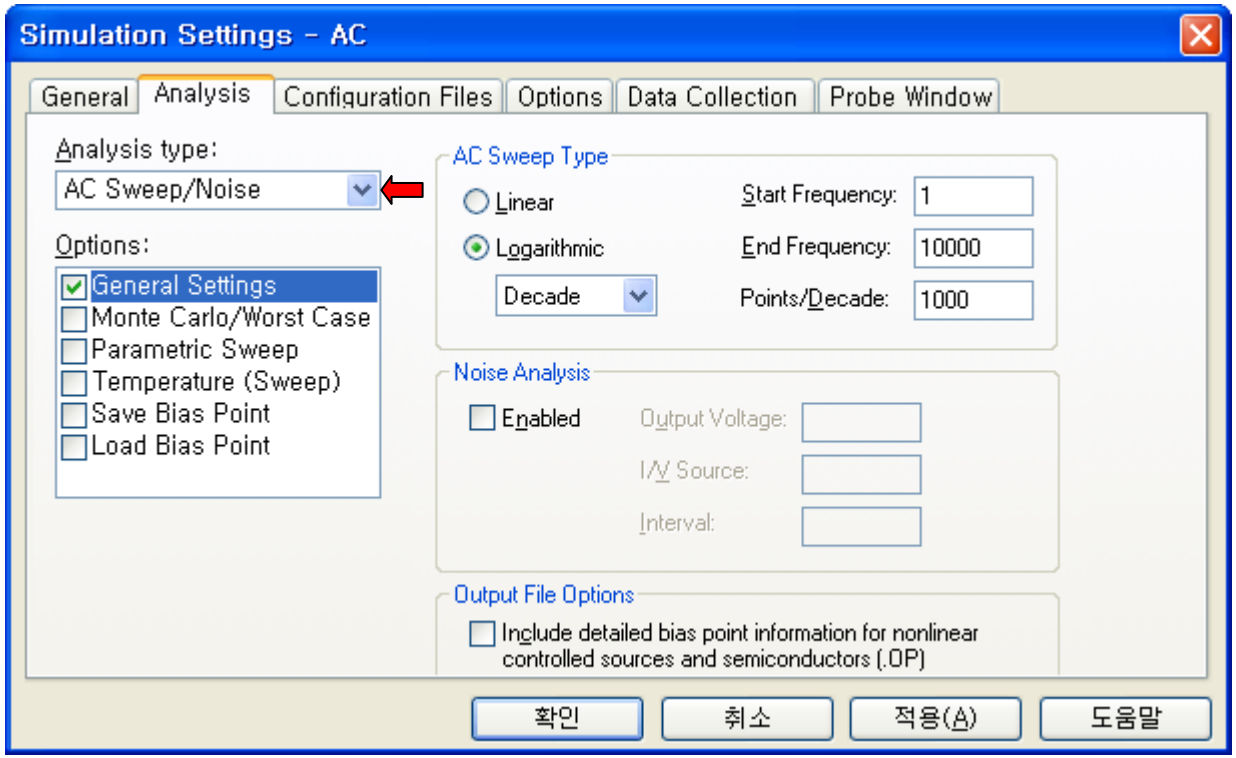
AC SWEEP

PSpice>>New Simulation Profile로 새로운 simulation profile 만들고,

Analysis type을 “AC Sweep/Noise”로 선택.



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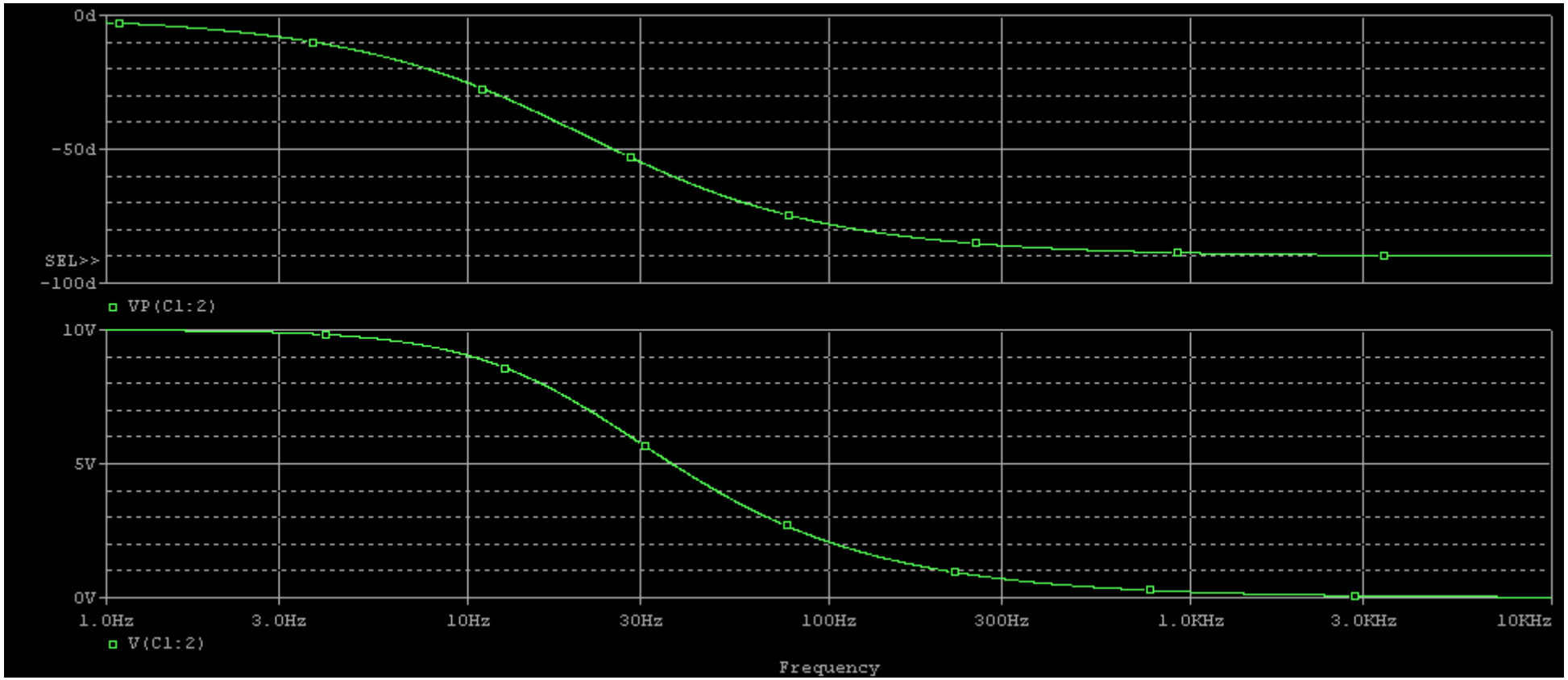
주파수 응답



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