ECE 5730
Memory Systems
Spring 2009

DRAM Access Protocol

Cornell University

Announcements

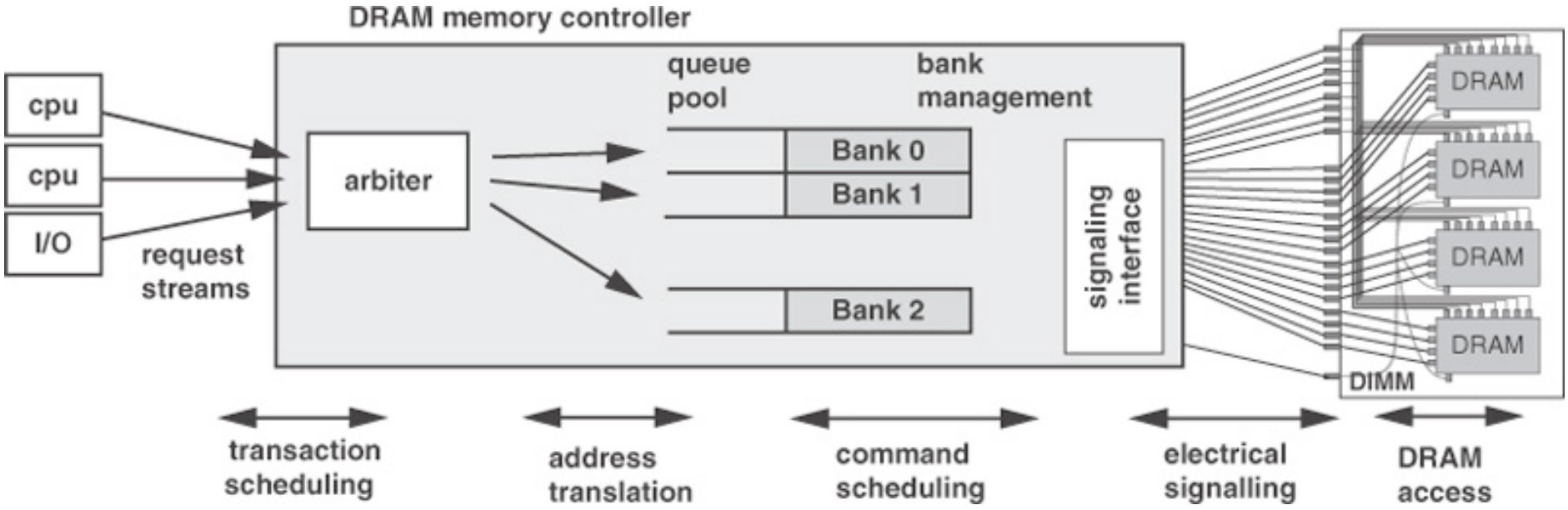
- **Quiz 7 on Tuesday**
- **Quiz 6**
  - **Average = 5.65/10**
- **Quiz 5 (Feb 24): I'll give credit for 2(c) and 3(d)**
- **Exam I**
  - **Wednesday, March 11, 6:30-9:30pm, location TBD**
  - **Friday, March 13, 1:30-4:30pm, location TBD**

Where We're Headed

- ✓ Overall DRAM organization
- ✓ Evolution of DRAMs and their basic operation
- ✓ DRAM internals

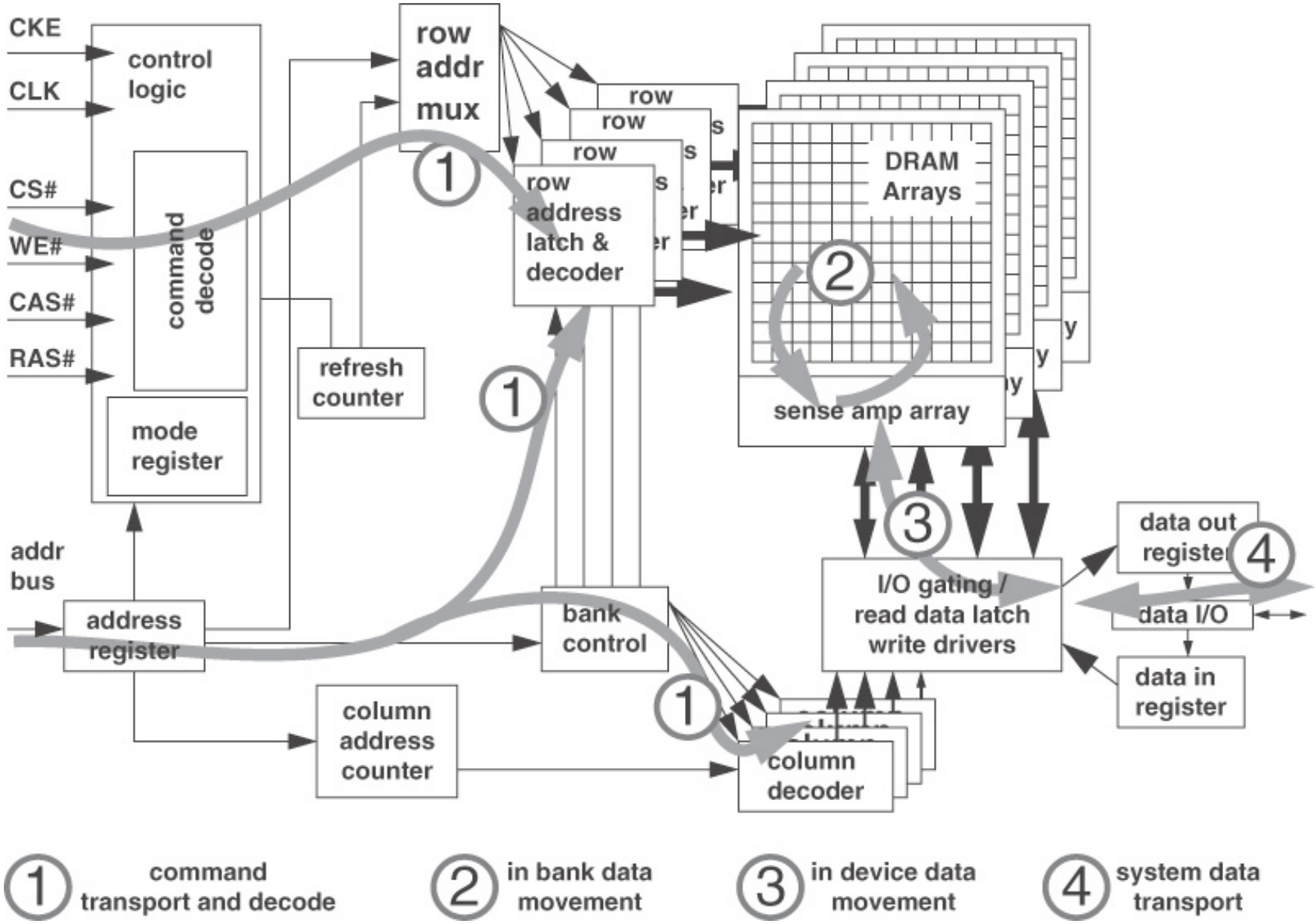
- DRAM access protocol and constraints
- Memory controllers
- Case studies

Sneak Peak at a Memory Controller



- **A high performance MC must know**
  - how do you order accesses?
  - **How addresses map to banks and ranks** (+translation)
  - **Open page in each bank (what row address will *hit*)**
    - ⇒ do I do a precharge?
  - **Required intra- and inter-command latencies**
  - **DRAM max power constraints**
    - ⇒ doing repeated access may cause overheating

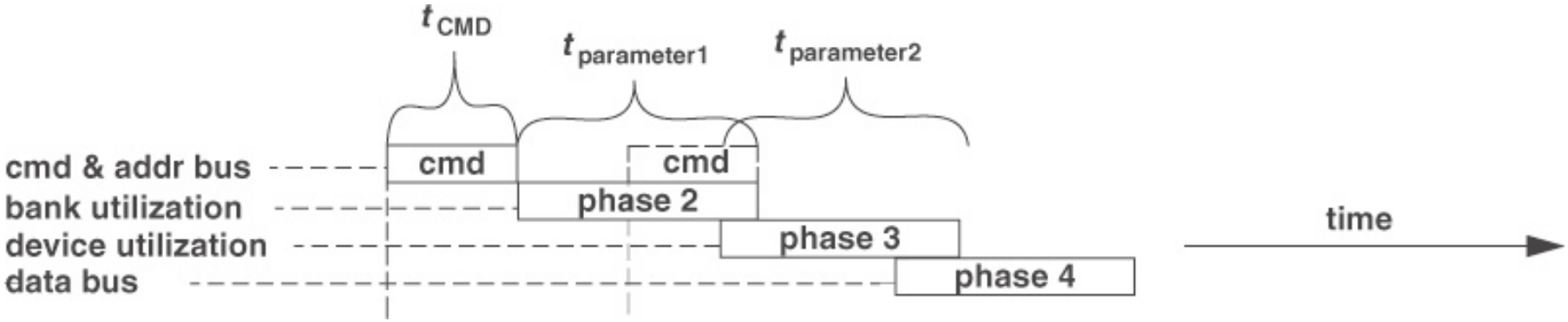
SDRAM Command and Data Movement



→ may include transfer on I/O circuitry

(abstract)

Generic DRAM Command Format



how long do I have to wait till I can issue another cmd for the bank?

t_{CMD}: max time to transport cmd from MC to DRAM
$t_{parameter1}$: min time required between two cmds sharing same bank
$t_{parameter2}$: min time required between two cmds sharing other resources

↑ usually I/O circuitry

Major SDRAM Timing Parameters

Parameter	Description
t_{AL}	Added Latency to column accesses, used in DDRx SDRAM devices for posted CAS commands.
t_{BURST}	Data burst duration. The time period that data burst occupies on the data bus. Typically 4 or 8 beats of data. In DDR SDRAM, 4 beats of data occupy 2 full clock cycles.
t_{CAS}	Column Access Strobe latency. The time interval between column access command and the start of data return by the DRAM device(s). Also known as t_{CL}.
t_{CCD}	Column-to-Column Delay. The minimum column command timing, determined by internal burst (prefetch) length. Multiple internal bursts are used to form longer burst for column reads. t_{CCD} is 2 beats (1 cycle) for DDR SDRAM, and 4 beats (2 cycles) for DDR2 SDRAM.
t_{CMD}	Command transport duration. The time period that a command occupies on the command bus as it is transported from the DRAM controller to the DRAM devices.
t_{CWD}	Column Write Delay. The time interval between issuance of the column-write command and placement of data on the data bus by the DRAM controller.
t_{FAW}	Four (row) bank Activation Window. A rolling time-frame in which a maximum of four-bank activation can be engaged. Limits peak current profile in DDR2 and DDR3 devices with more than 4 banks.

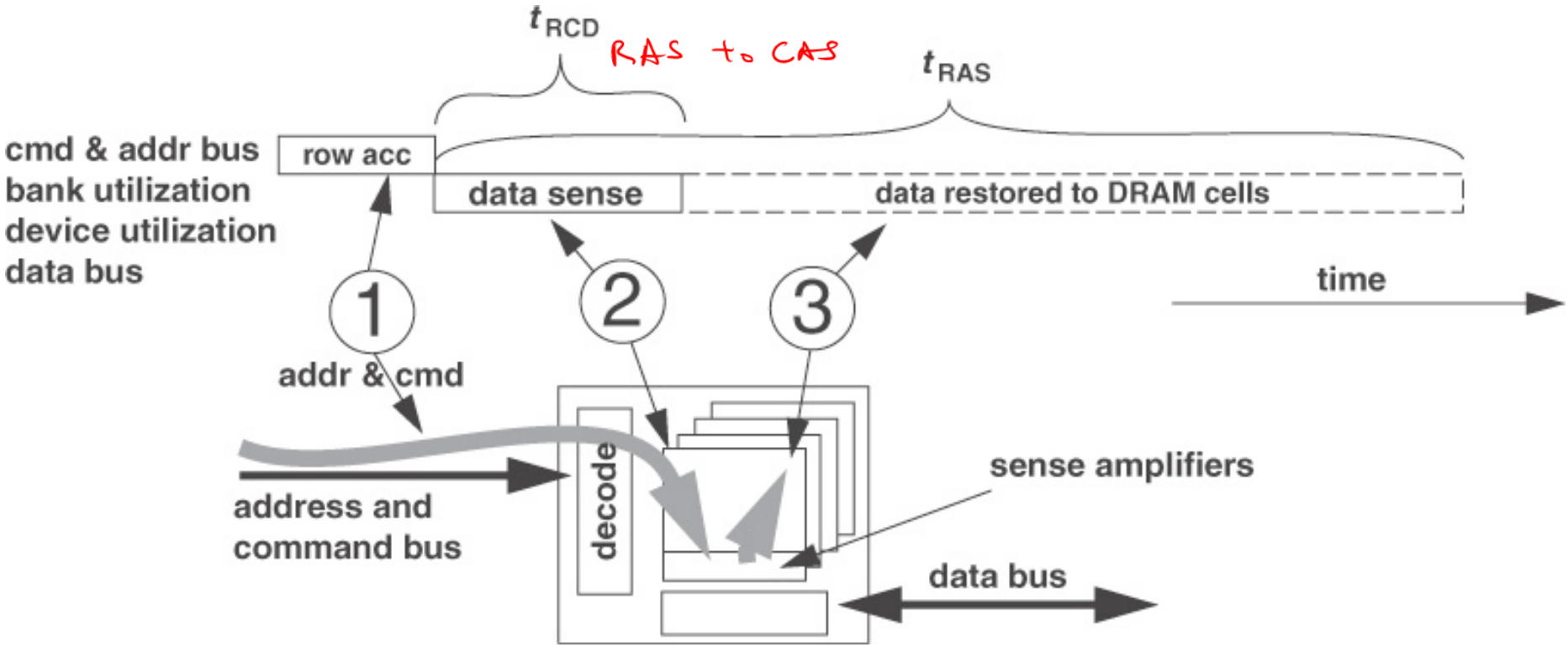
Major SDRAM Timing Parameters

Parameter	Description
t_{OST}	ODT Switching Time. The time interval to switching ODT control from rank to rank.
t_{RAS}	Row Access Strobe. The time interval between row access command and data restoration in a DRAM array. A DRAM bank cannot be precharged until at least t_{RAS} time after the previous bank activation.
t_{RC}	Row Cycle. The time interval between accesses to different rows in a bank. $t_{RC} = t_{RAS} + t_{RP}$.
t_{RCD}	Row to Column command Delay. The time interval between row access and data ready at sense amplifiers.
t_{RFC}	Refresh Cycle time. The time interval between Refresh and Activation commands.
t_{RP}	Row Precharge. The time interval that it takes for a DRAM array to be precharged for another row access.

Major SDRAM Timing Parameters

Parameter	Description
t_{RRD}	Row activation to Row activation Delay. The minimum time interval between two row activation commands to the same DRAM device. Limits peak current profile.
t_{RTP}	Read to Precharge. The time interval between a read and a precharge command.
t_{RTRS}	Rank-to-rank switching time. Used in DDR and DDR2 SDRAM memory systems; not used in SDRAM or Direct RDRAM memory systems. One full cycle in DDR SDRAM.
t_{WR}	Write Recovery time. The minimum time interval between the end of a write data burst and the start of a precharge command. Allows sense amplifiers to restore data to cells.
t_{WTR}	Write To Read delay time. The minimum time interval between the end of a write data burst and the start of a column-read command. Allows I/O gating to overdrive sense amplifiers before read command starts.

Row Access



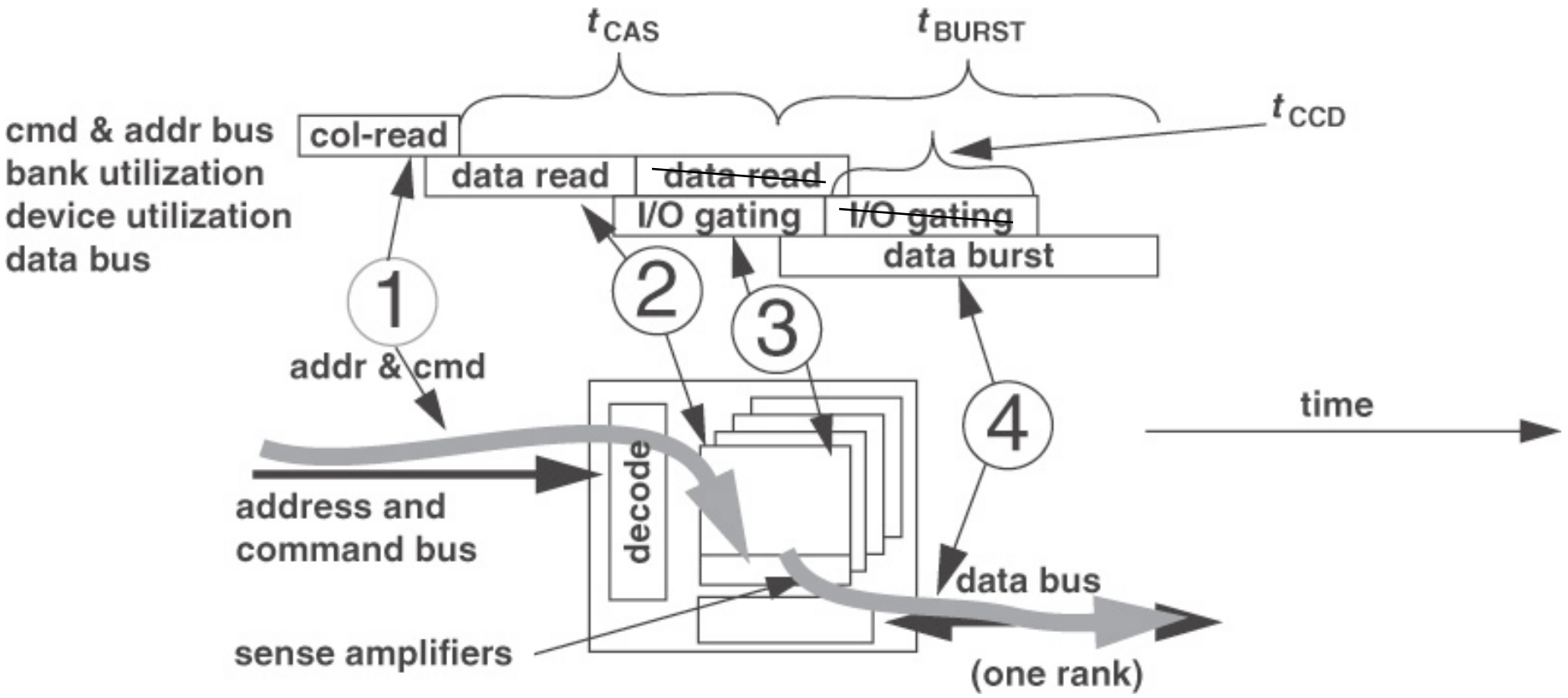
RAS to data

t_{RCD}: max time to access data and move into sense amps

t_{RAS}: min time required before next row precharge

how long do we need to wait before changing rows

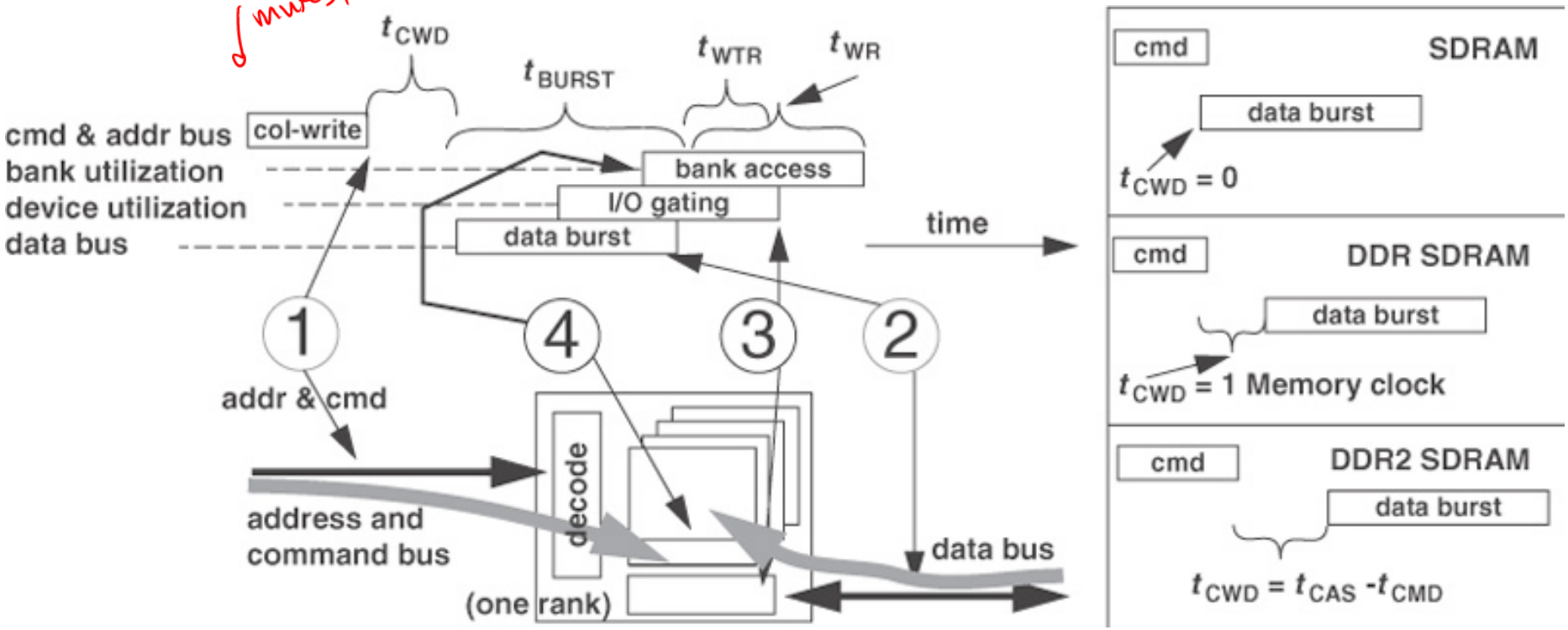
Column Read



t_{CAS}: max time to move data from sense amps to data bus
t_{CCD}: internal DRAM burst length (1 for DDR, 2 for DDR2, 4 for DDR3)
t_{BURST}: data bus burst length

pushing bus speed is fine, but you have to beware of internal workings

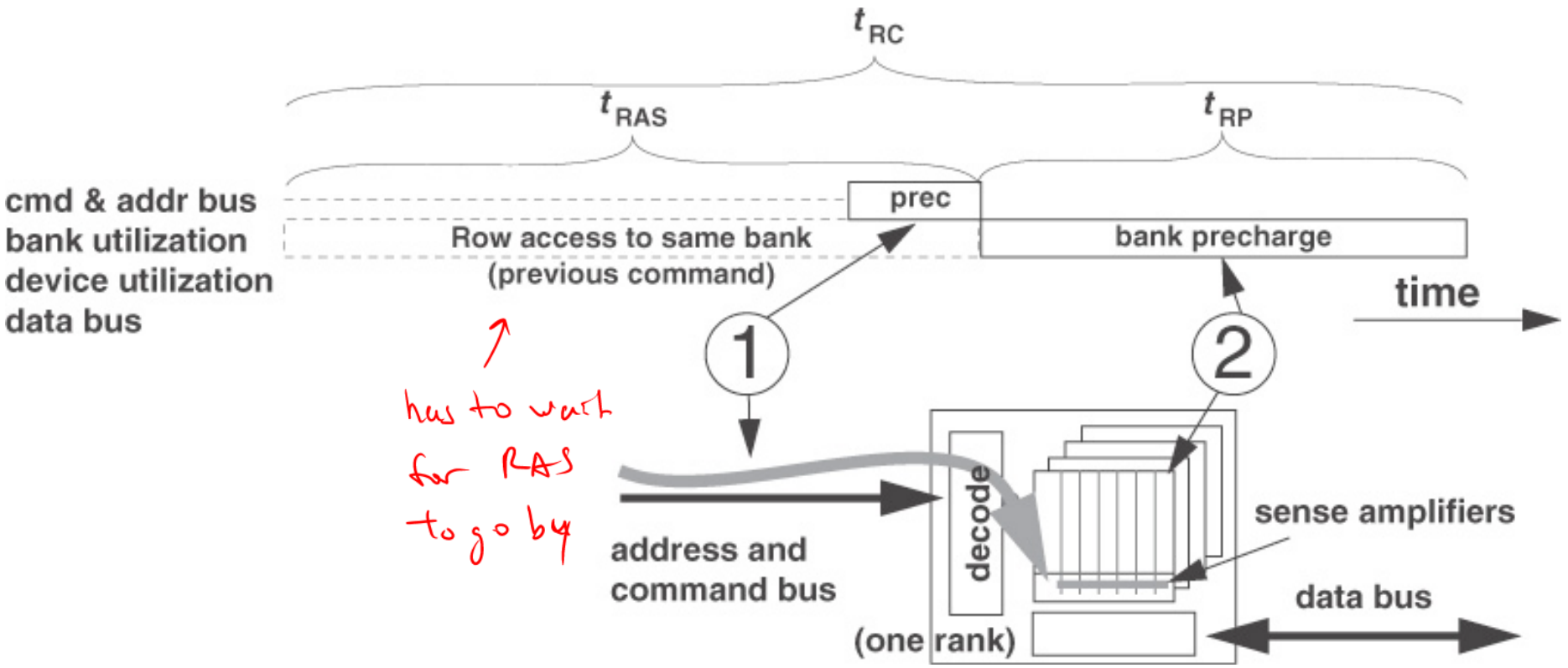
Column Write



t_{CWD}: min time between cmd and data (to select column)
t_{BURST}: bus burst length → length of data transfer
t_{WTR}: min time between end of write data and read to same page
t_{WR}: min time between end of write data and precharge

how long before I can read? (due to internal gating circuitry)

Precharge (within a bank?)



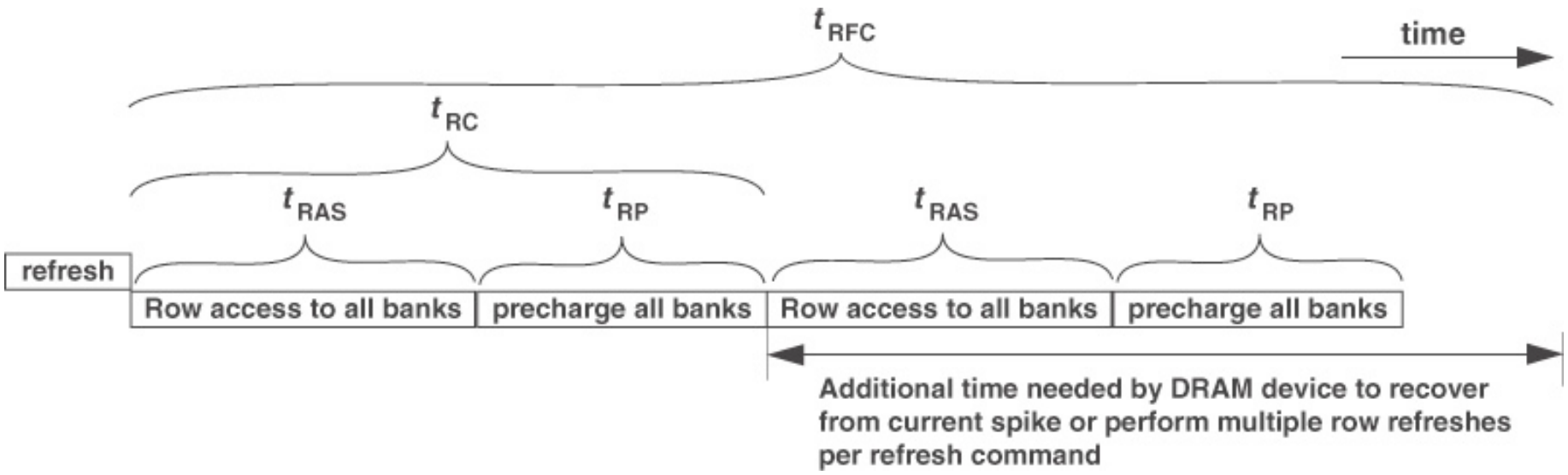
t_{RP}: min time to precharge a new row

t_{RC}: min time between back-to-back row accesses

→ 2 consecutive accesses on 2 different rows (pages)

→ do I precharge? or do I assume I'll get another access to a different column?

Refresh



t_{RFC}: max time to complete refresh cmd

→ opening a particular row is basically a refresh

→ typically open tons of stuff simultaneously

→ high current operation

→ do things in series, stagger precharges

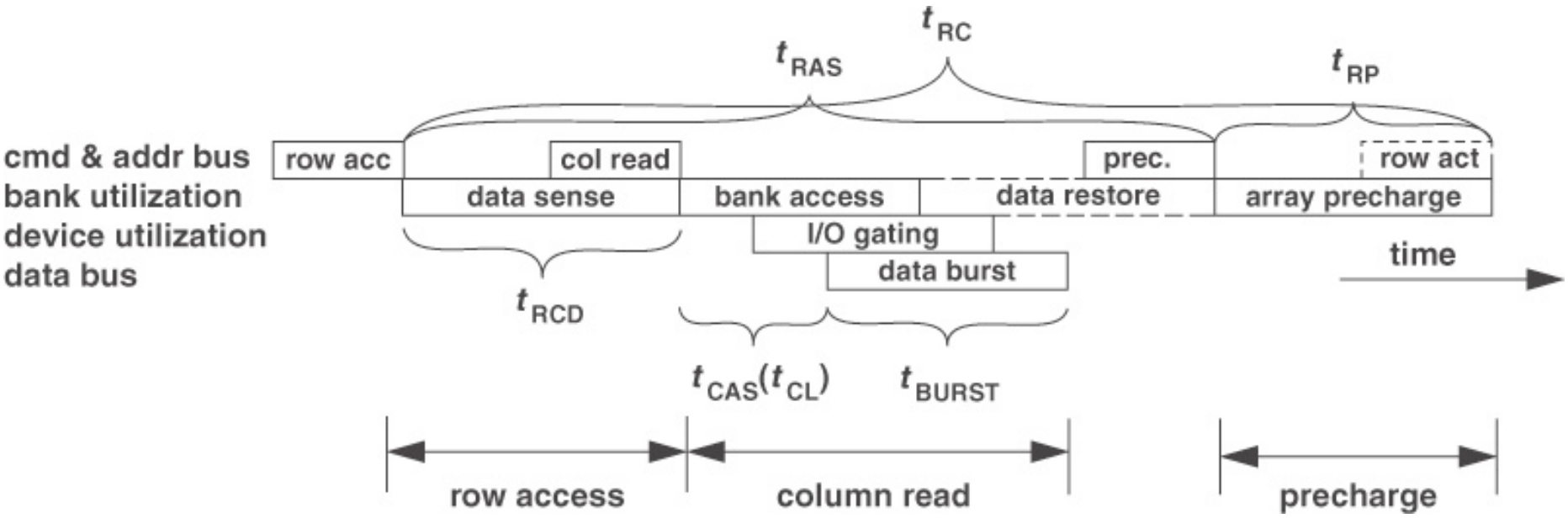
Refresh Cycle Times

DRAM Device Family	Voltage	DRAM Device Capacity	Number of Banks	Number of Rows	Row Size	Refresh Count	t_{RC}	t_{RFC}
DDR	2.5 V	256 Mb	4	8192	1 kB	8192	60 ns	67 ns
		512 Mb	4	8192	2 kB	8192	55 ns	70 ns
DDR2	1.8 V	256 Mb	4	8192	1 kB	8192	55 ns	75 ns
		512 Mb	4	16384	1 kB	8192	55 ns	105 ns
		1024 Mb	8	16384	1 kB	8192	54 ns	127.5 ns
		2048 Mb	8	32768	1 kB	8192	~	197.5 ns
		4096 Mb	8	65536	1 kB	8192	~	327.5 ns

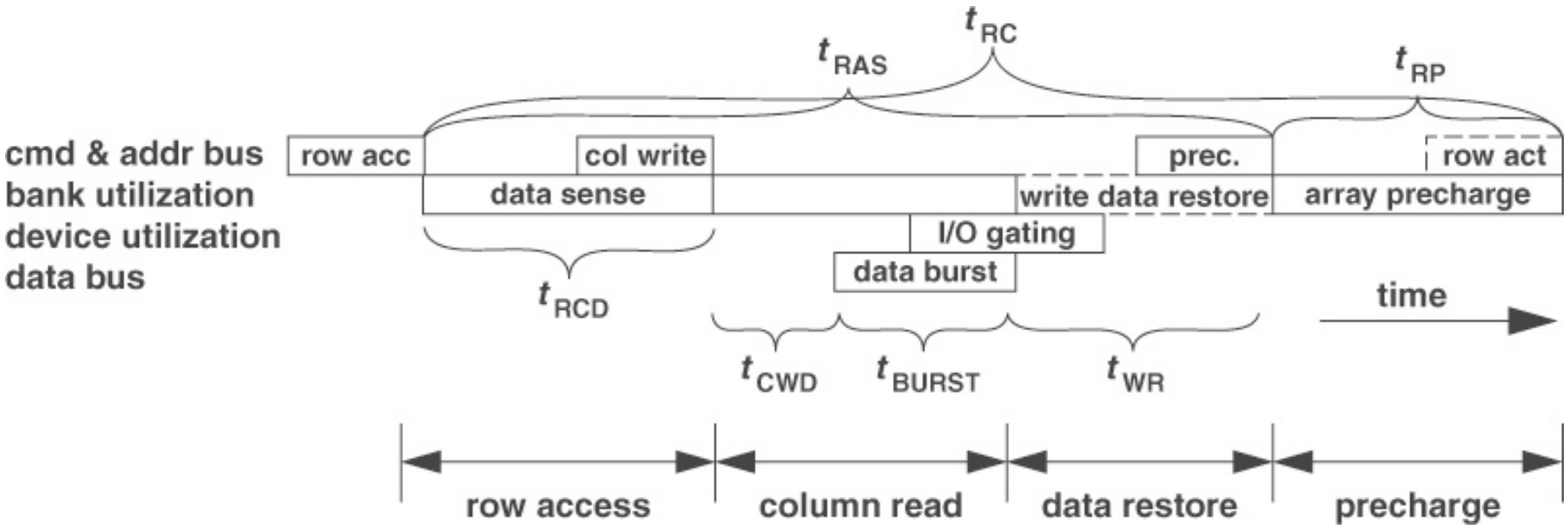
lots of bits ⇒ lots of current to refresh

a lot longer (due to current constraint)

Read Cycle


t_{RC}
t_{RAS}
t_{RP}
cmd & addr bus
bank utilization
device utilization
data bus
row acc
col read
prec.
row act
data sense
bank access
data restore
array precharge
I/O gating
data burst
time
t_{RCD}
$t_{CAS}(t_{CL})$
t_{BURST}
row access
column read
precharge

Write Cycle


t_{RC}
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prec.
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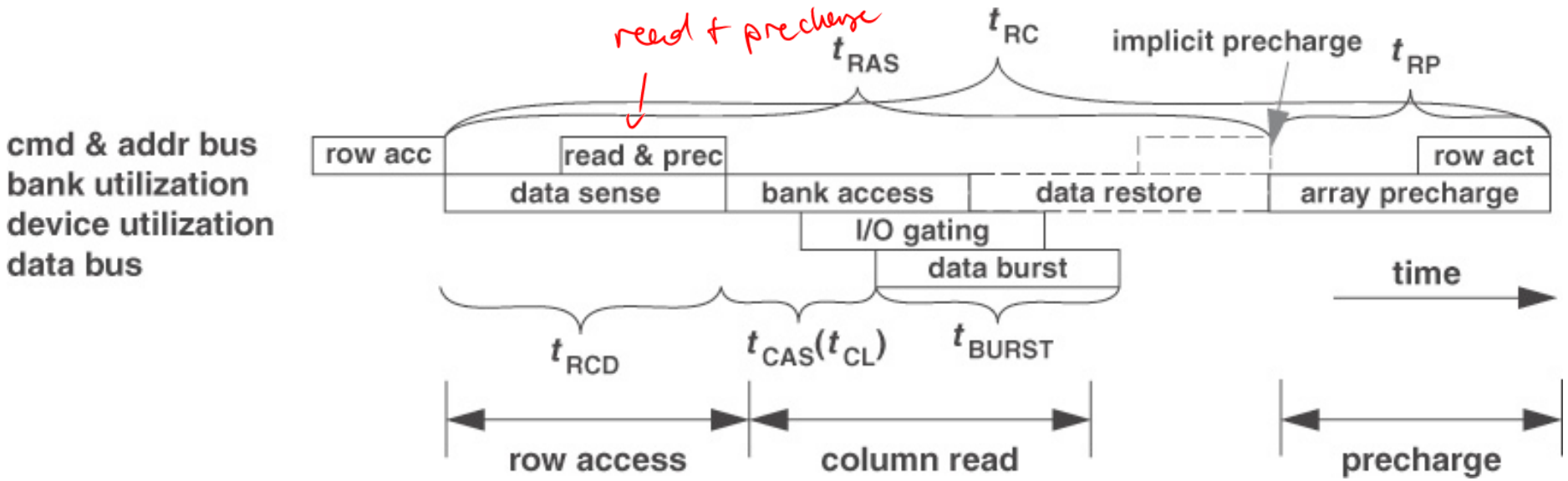
data sense
write data restore
array precharge
I/O gating
data burst
t_{RCD}
time
t_{CWD}
t_{BURST}
t_{WR}
row access
column read
data restore
precharge

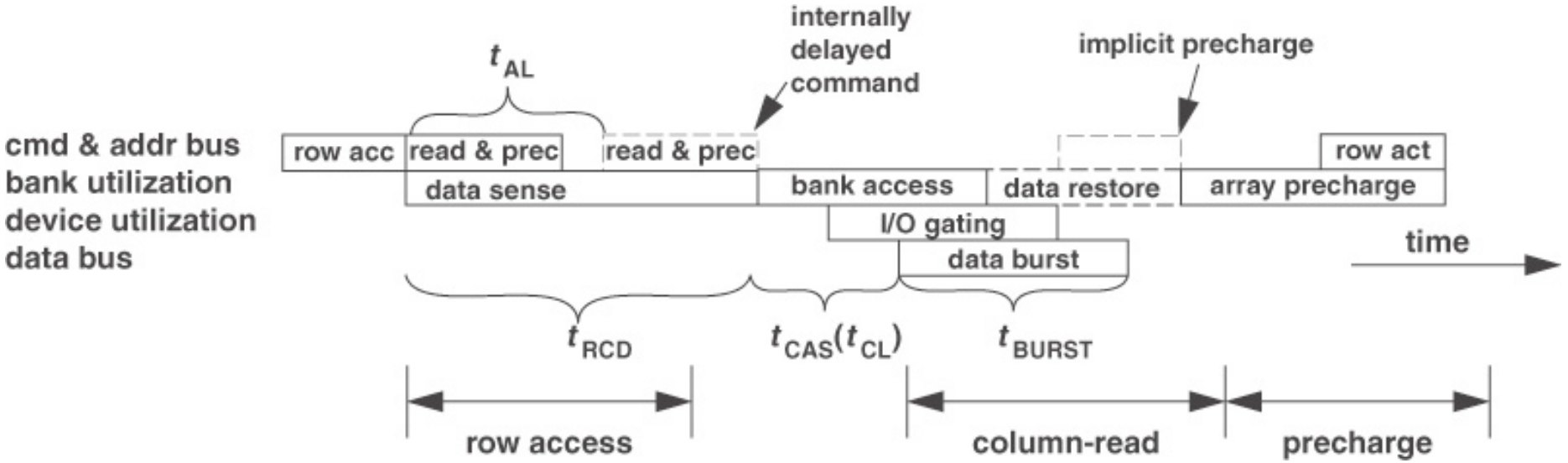
Column Read with Auto Precharge



Normal column read cmd with a particular address bit =1

we're going to have to precharge on read, so let's just do it automatically.

Row Access with Posted CAS

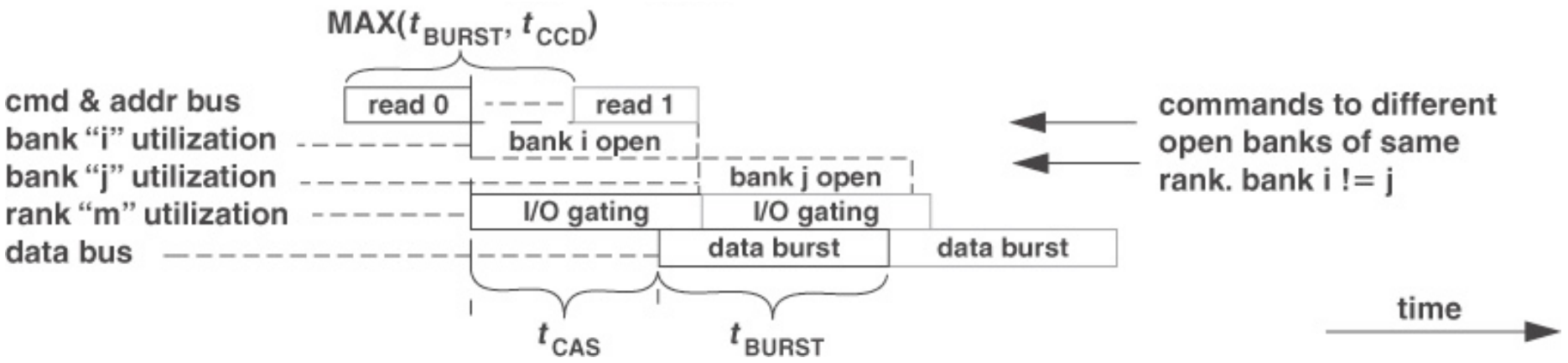


t_{AL} = delay until the column read takes effect (programmed into mode reg)

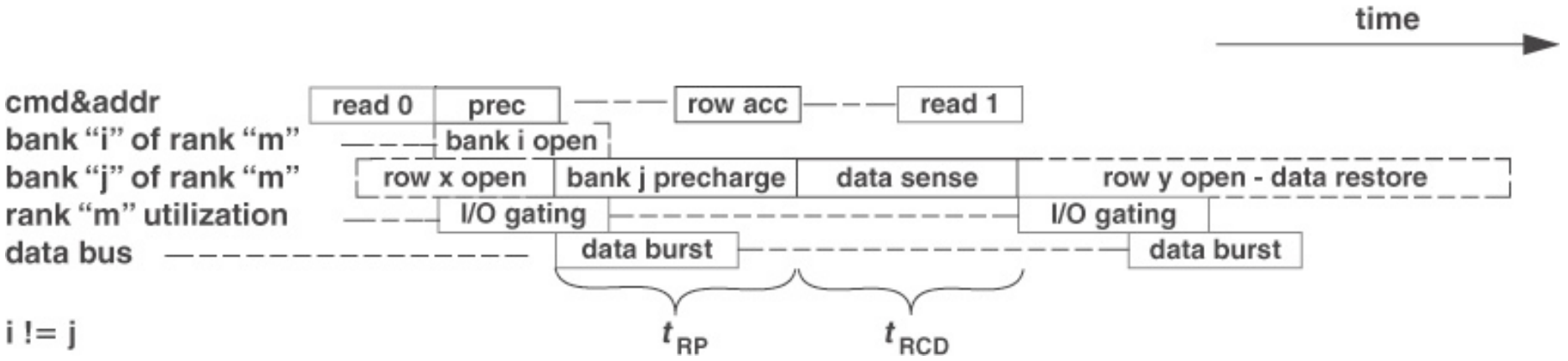
DRAM Command Interactions

- DRAM commands can be scheduled consecutively subject to resource constraints
  - Banks
  - Sense amps
  - I/O circuits
  - Command/address and data buses
- Maximum device current limitations must be respected as well
- Note: I'm not covering every detail
  - See book if interested

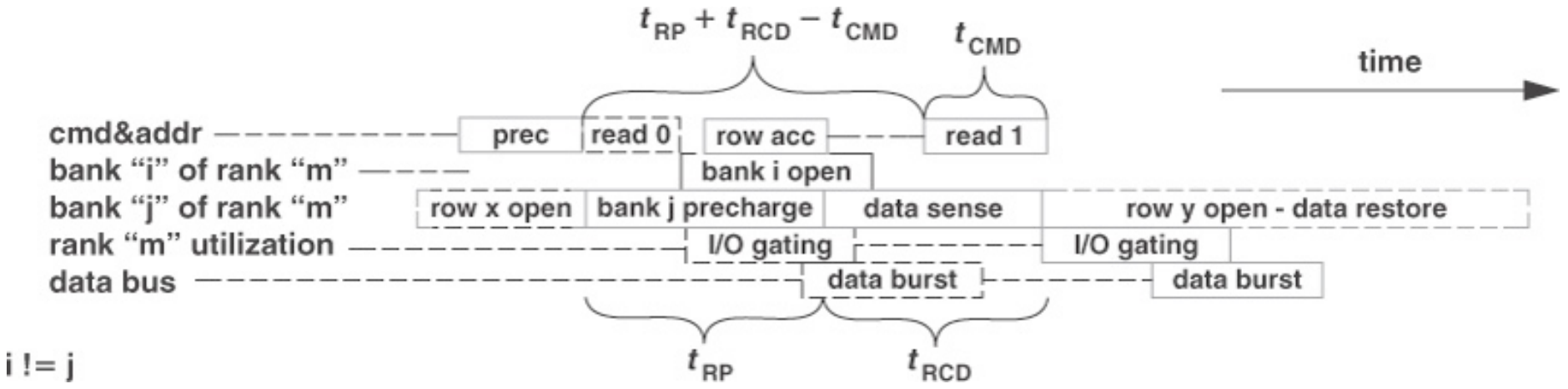
Read Page Hits in Two Banks



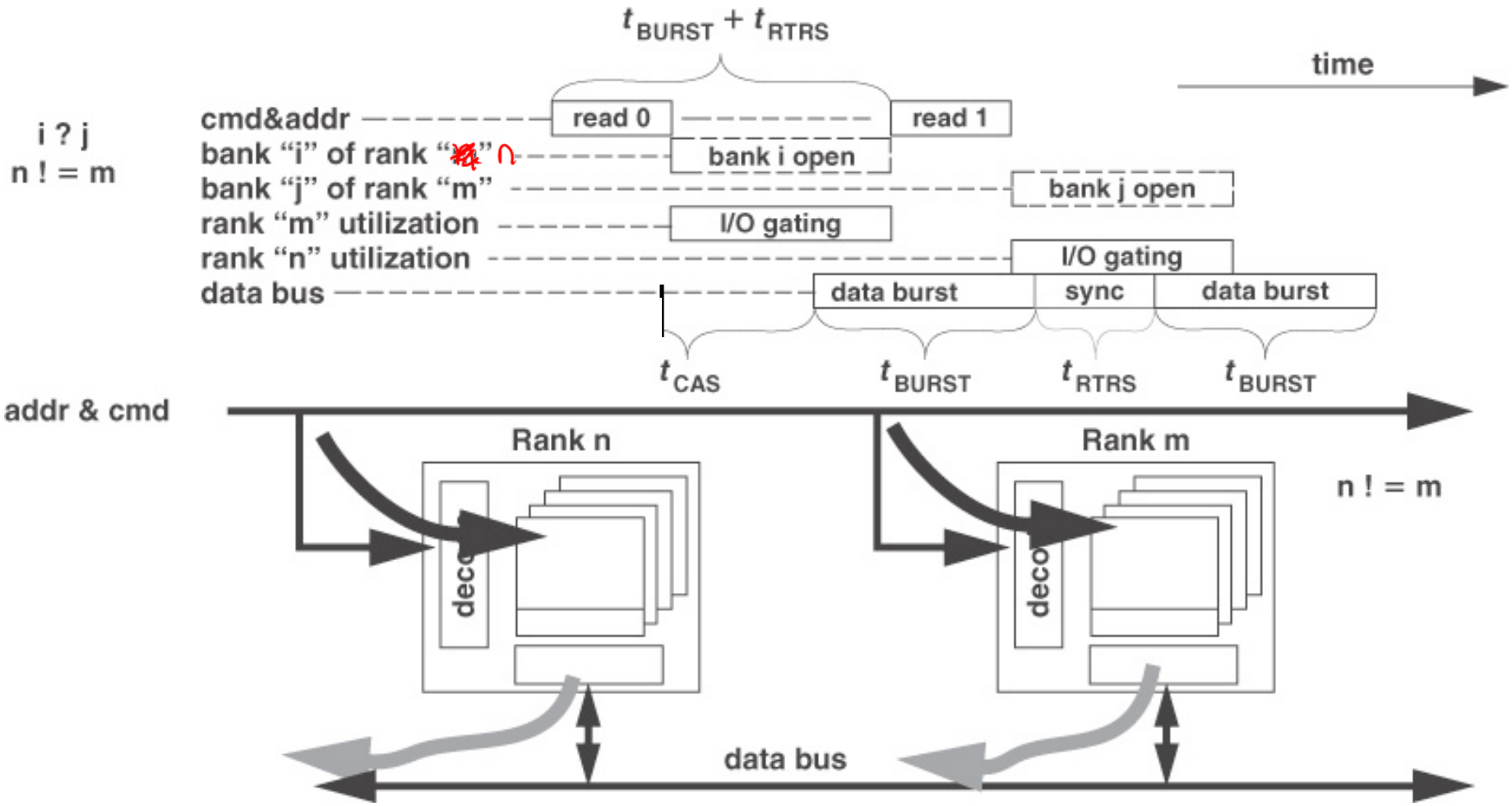
Page Hit Followed by Page Miss



With Command Reordering

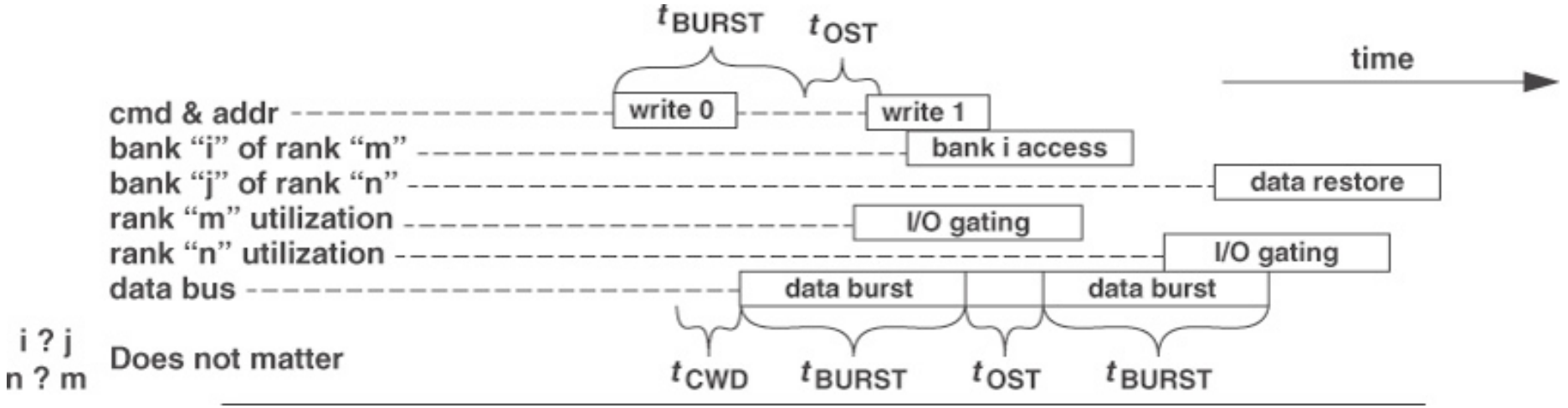


Column Reads to Different Ranks



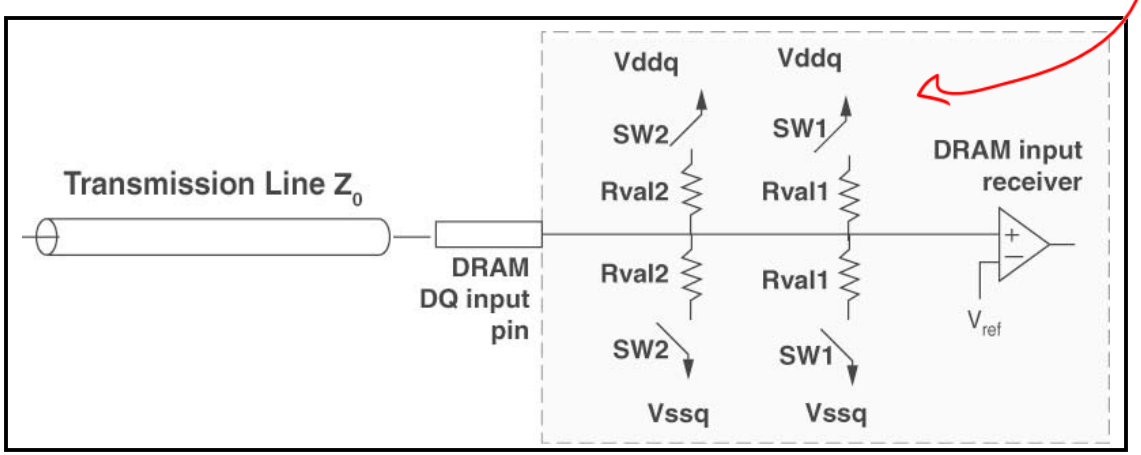
t_{RTRS} = dead time to hand-off DQS control to other rank

Column Writes to Different Ranks



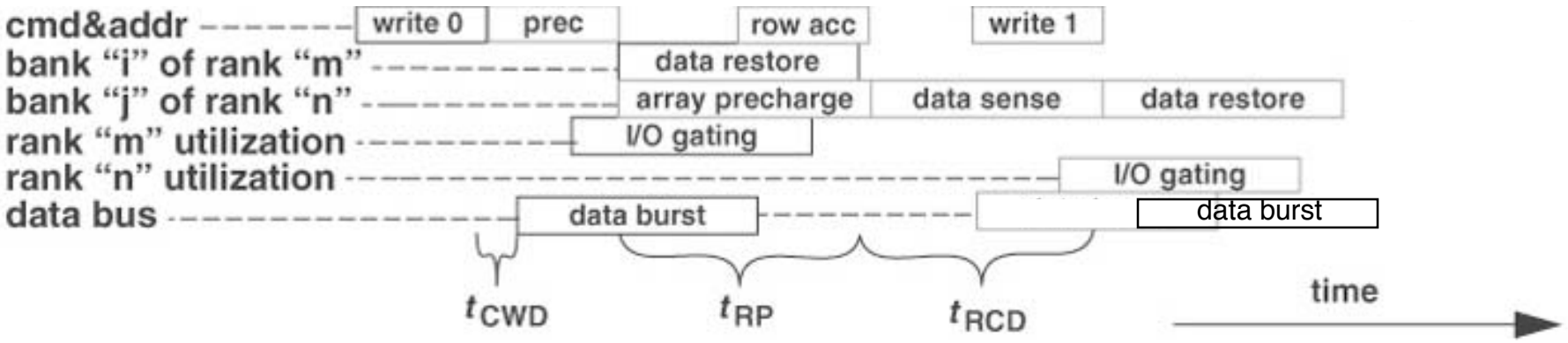
can change termination characteristics

t_{OST} = time to switch off on-die termination (OTD) - time to switch on ODT (DDR2 and DDR3)

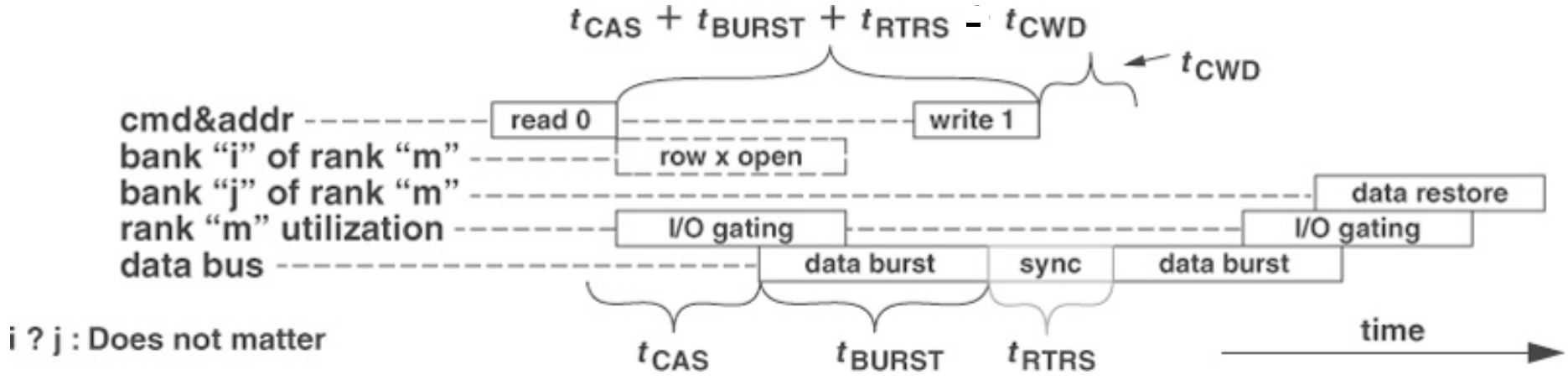


[11.19, 9.22]

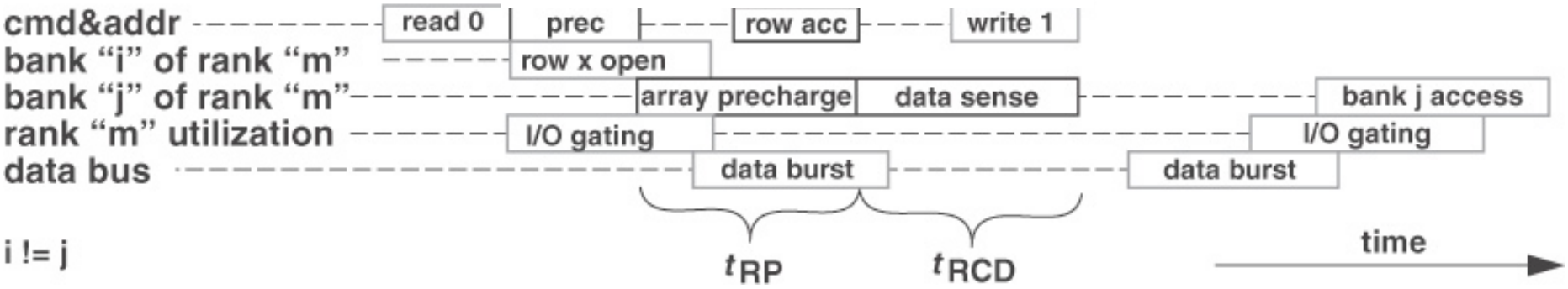
Write Page Hit, Page Miss (Diff Ranks)



Read Page Hit, Write Page Hit

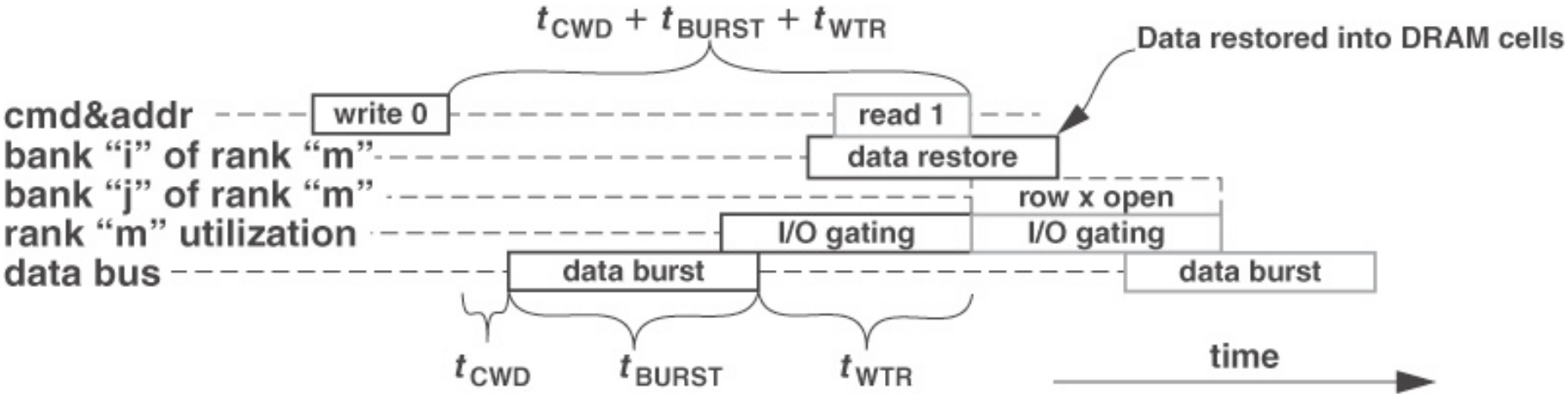


Read Page Hit, Write Page Miss

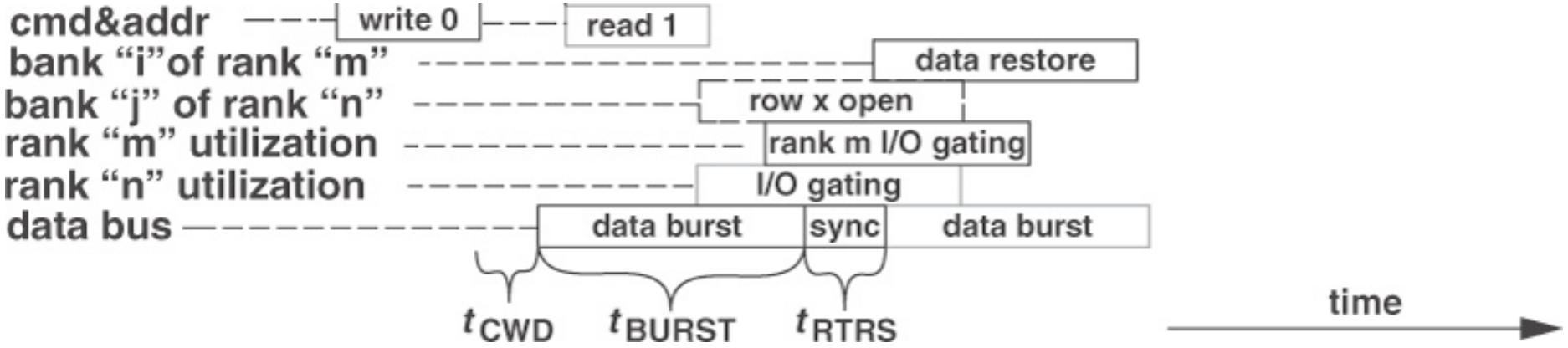


reorder read 0 and prec?

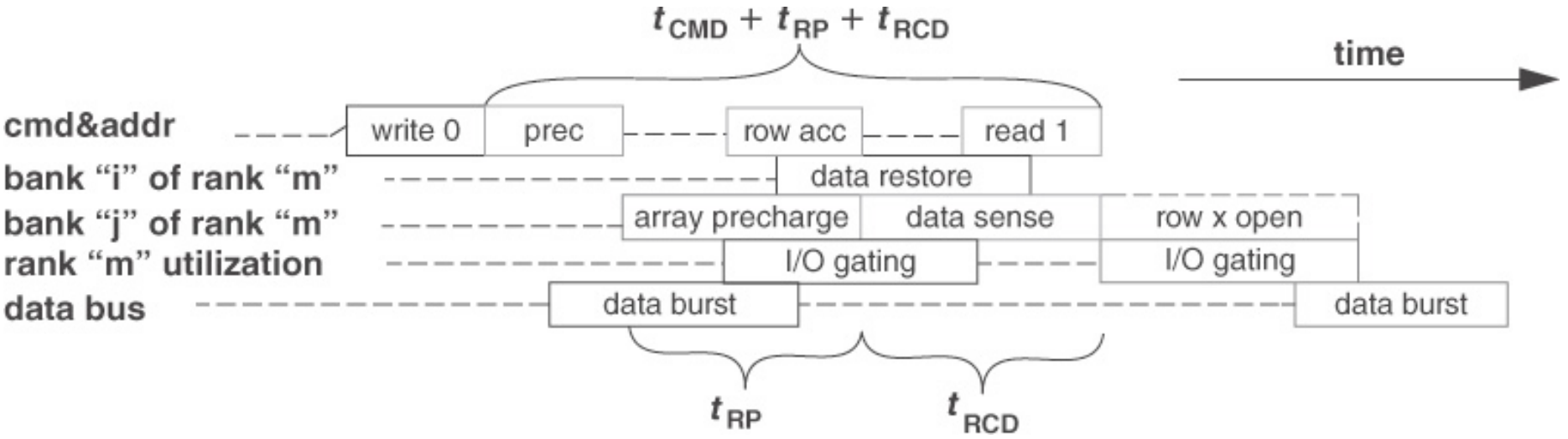
Write Page Hit, Read Page Hit



Write Hit, Read Hit (Diff Ranks)



Write Page Hit, Read Page Miss

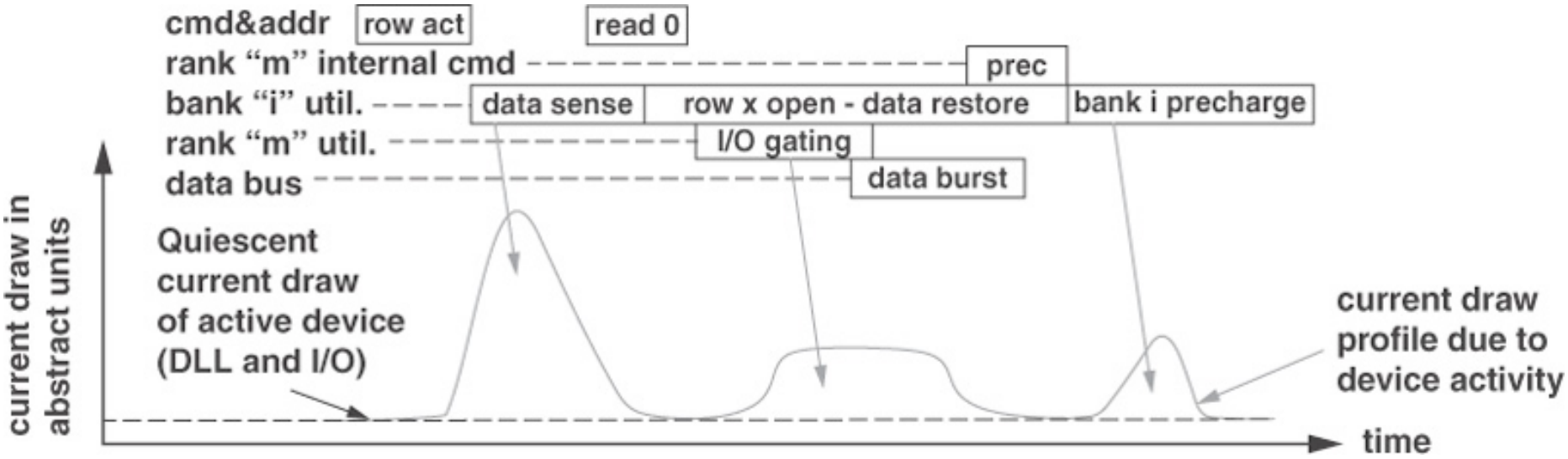


DRAM Power Constraints

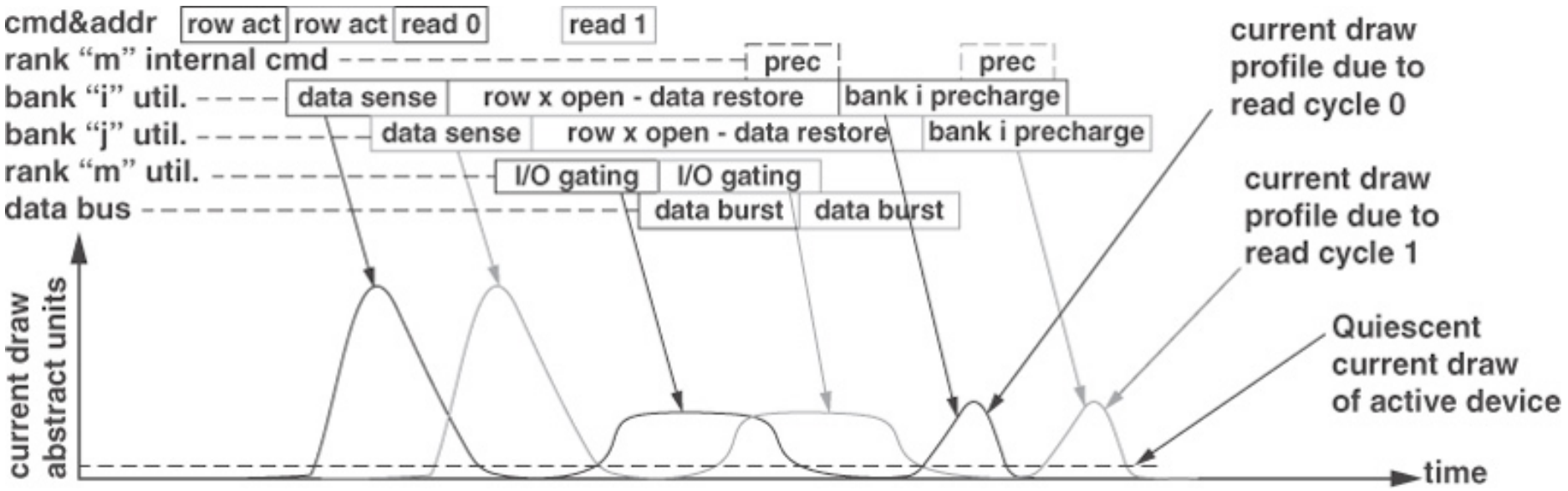
- The cost of rapidly increasing DRAM clock rates is increased power consumption

- DRAM manufacturers constrain the activity rate so as not to exceed thermal limits

DRAM Current Profile of Read



Back-to-Back Reads to Different Banks

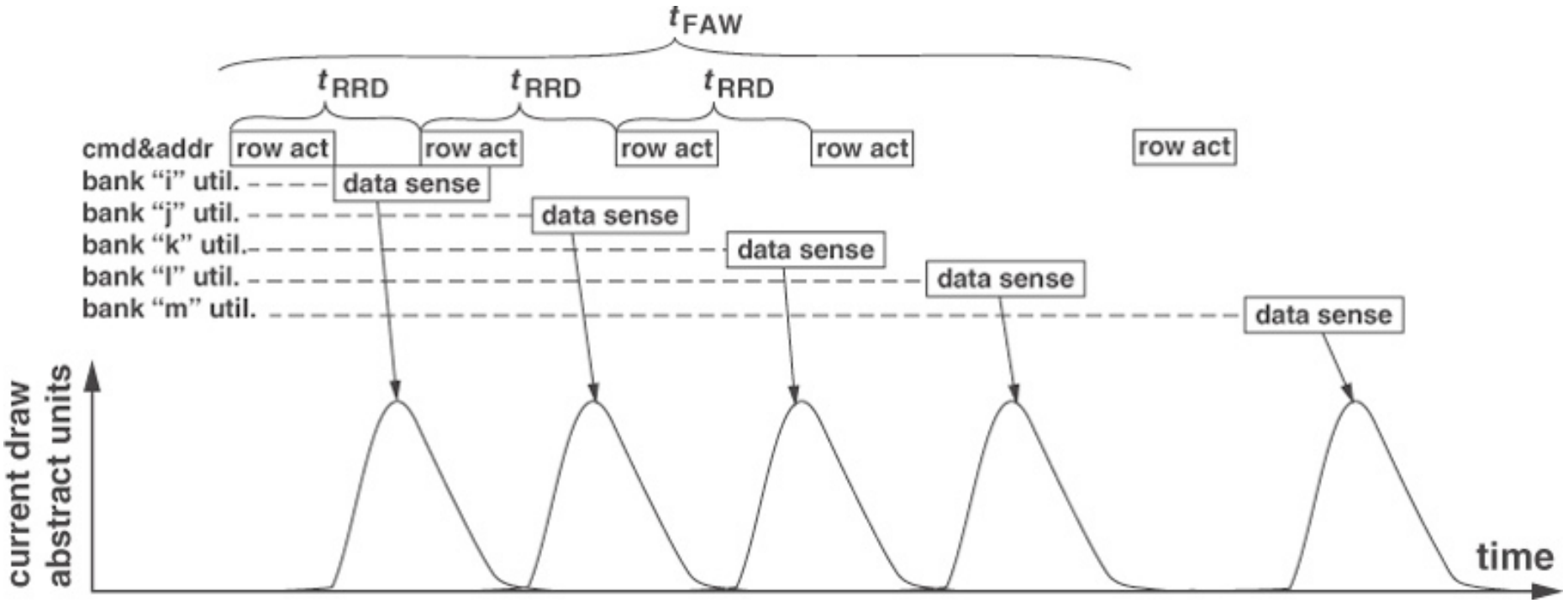


DDR2 Power-related Parameters

Device Configuration	512 Mbit x 4	256 Mbit x 8	128 Mbit x 16
Data bus width	4	8	16
Number of banks	8	8	8
Number of rows	16384	16384	8192
Number of columns	2048	1024	1024
Row size (bits)	8192	8192	16384
t_{RRD} (ns)	7.5	7.5	10
t_{FAW} (ns)	37.5	37.5	50

t_{RRD} = min time between row activations
t_{FAW} = min time in which four row activations can occur

DDR2 Power-related Parameters



Some MC Decisions

- How to map the address into rank and bank
- When to close an open page
- Ordering of queued operations (scheduling)
  - Low latency
  - High cmd/address and bus utilization

Next Time

Memory Controllers