
OrCAD, Pspice 복습

OrCAD and PSpice

PSpice is a SPICE analog circuit and digital logic simulation program for Microsoft Windows. The name is an acronym for **Personal Simulation Program with Integrated Circuit Emphasis**.

<http://en.wikipedia.org/wiki/PSPICE>

OrCAD and PSpice

The screenshot shows a Windows Internet Explorer browser window displaying the Cadence OrCAD Solutions website. The address bar shows the URL <http://www.cadence.com/products/orcad/pages/default.aspx>. The browser's menu bar includes File (F), Edit (E), View (V), Favorites (A), Tools (T), and Help (H). The toolbar shows various icons for navigation and utility. The website header features the Cadence logo, navigation links (Solutions, Products, Services, Support & Training, Alliances, Community, About Cadence), and a search bar. The main content area is titled "Cadence OrCAD Solutions" and features a large orange banner for "OrCAD 16.6—New Signal Integrity Flow, Advances in Simulation, and Extended Tcl Programming" with a "Learn more" button. Below the banner, there are sections for "New OrCAD Capture Marketplace" and "OrCAD Quicklinks". The right sidebar contains "Highlights" and "Recent Blog Posts". The status bar at the bottom shows the URL <http://www.cadence.com/products> and the page zoom level at 105%.

Cadence OrCAD Solutions

OrCAD 16.6—New Signal Integrity Flow, Advances in Simulation, and Extended Tcl Programming

Learn more

OrCAD 16.6—Find out what's new

Learn more

New OrCAD Capture Marketplace

Josh Moore, Senior Product Manager for OrCAD, shares how the new OrCAD Capture Marketplace – with online apps – transforms the way PCB designers access information, discover new resources and extend the OrCAD environment.

OrCAD Quicklinks

- Why Cadence OrCAD for PCB?
- Design Suites Datasheet
- Software downloads

Highlights

- Webinar: PCB Library Development – Build OrCAD Symbols and IPC-7351 compliant footprints in a fraction of the time with EDABuilder
- Allegro and OrCAD Users Day at CDNLive! Silicon Valley
- What's Good About OrCAD Apps? You Can Try Them for Free!
- FPGA-PCB codesign; a 21st Century approach to integrating fpgas into the pcb design process

Recent Blog Posts

- What's Good About Allegro PCB Editor Place Replicate Text Support? Check Out 16.6!
- What's Good About Allegro AMS

OrCAD and PSpice

Products



OrCAD FPGA System Planner new

Provides a complete, scalable solution for FPGA-PCB co-design that allows users to create an optimum correct-by-construction pin assignment.

[Read more »](#)



OrCAD Capture and Capture CIS

Offers full-featured schematic editing for fast, intuitive design capture with hierarchical and variant capabilities. Component information system (CIS) promotes use of preferred, current parts to accelerate the design process and reduce project costs.

[Read more »](#)



OrCAD PCB Designer

Offers a proven, scalable, easy-to-use PCB editing and routing solution. Delivers a comprehensive feature set and seamless PCB design environment to take designs from concept to production.

[Read more »](#)



ActiveParts Portal new

Automates the process of part selection and extends the reach of engineers. APP is FREE for users on the most current releases of OrCAD Capture CIS

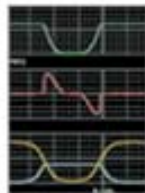
[Read more »](#)



OrCAD Signal Explorer

Enables pre- and post-layout signal integrity analysis and topology design/exploration at any stage of the design cycle improving circuit reliability and performance to reduce prototypes and re-spins.

[Read more »](#)



PSpice A/D and Advanced Analysis

Provides simulation of analog/mixed-signal circuits as well as analysis for by determining which components are over-stressed and component yields. Full integration with OrCAD Capture improves productivity and data integrity.

[Read more »](#)

<http://www.cadence.com/products/orcad/Pages/default.aspx>

OrCAD and PSpice

 Share  Subscribe  Contact  Print

OrCAD Downloads

Note: To download the files we recommend using the [Internet Explorer](#) or [Firefox](#) web browsers.
All OrCAD downloads require a valid email address.

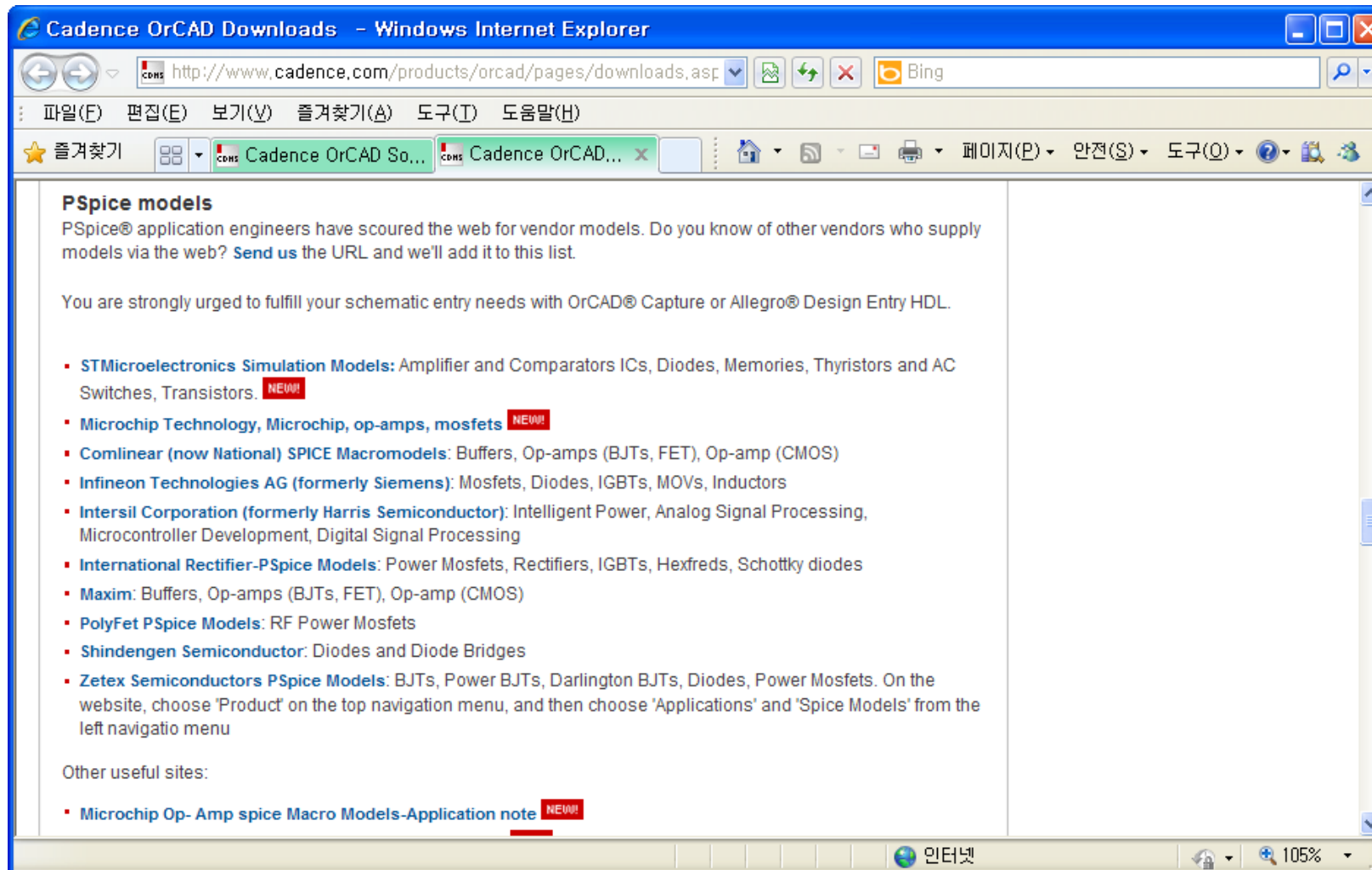
High-speed PCB layout, routing, and manufacturing output

The latest product downloads are available free to all registered Cadence® customers. In some cases, you'll be asked to complete a brief user profile. All information supplied is used only to help us develop future products and technology.

- [OrCAD PCB Designer Lite DVD \(All Products\)](#)
- [OrCAD PCB Designer Lite DVD \(Capture & PSpice only\)](#)
- [CIS Admin Tool 10.x](#)
- [CIS Admin Tool 16.2](#)
- [OrCAD Capture/OrCAD Capture CIS ViewReader](#)
- [OrCAD CIS Wizard](#)
- [PSpice Schematics Installer](#)
- [Third-party translator](#)
- [PSpice models](#)
- [Allegro/OrCAD Starter Library](#)

<http://www.cadence.com/products/orcad/pages/downloads.aspx>

OrCAD and PSpice



<http://www.cadence.com/products/orcad/pages/downloads.aspx>

OrCAD and PSpice

Korea

NewLink Technology
UnionCenter #1009, 837-11, Yeoksam-1dong, Gangnam-gu,
Seoul, 135-754
Phone: 82-70.7138.1231
Fax: 82-505.827.1231
Email: jhchoi@newlinktek.com
Web site: www.newlinktek.com

Korea

NINEPLUS EDA
1502ho, Ace High-end Tower 8 Cha, 345-4, Gasan-dong, Geumcheon-gu, Seoul, 153-802
Phone: 82.2.6123.3355
Fax: 82.2.6123.3350
Email: sjkim@npeda.co.kr
Web site: www.npeda.co.kr

Korea

NINEPLUS EDA
AceHitech 21-1410, 1470, U-dong, Haeundae-gu,
Busan, 612-020
Phone: 82.51.758.4841, 4844~5
Fax: 82.51.758.4866
Email: sjkim@npeda.co.kr
Web site: www.npeda.co.kr

Korea

VT Korea
Duksan B/D 3F
114 Yangjae-dong, Seocho-gu
Seoul, 137-130
Phone: 82.2.2057.8815
Fax: 82.2.2057.8810
Email: jhkim@veritytech.co.kr
Web site: www.veritytech.co.kr
Serves Korea.

http://www.cadence.com/alliances/channel_partner/pages/default.aspx

OrCAD 16.6 Lite Program

The screenshot shows the npeda.co.kr website in Internet Explorer. The browser title is "Cadence Channel Partner 나인플러스EDA(주) :: - Windows Internet Explorer". The address bar shows "http://npeda.co.kr/index.action". The website header includes "Electronic Design Automation Technology & Engineering Service Leader" and navigation links like HOME, 로그인, SITE MAP, and CONTACT US. A red banner at the top lists categories: 제품소개, 고객지원, 견적/제품문의, University Program, 교육/세미나/이벤트, 커뮤니티, and 회사소개. The main content area features a "16.6 RELEASE" banner with a "자세히보기" link. Below this is a "고객지원 CS CENTER" section with the text "고객 여러분의 진정한 파트너가 되도록 최선을 다하고 있습니다." and a "내용더보기" link. To the left, there is a "멤버로그인 / MEMBER LOGIN" section with a login form and a "회원관리" button. Below that is an "교육일정 EDUCATION CALENDAR" for March 2013, showing dates 1 through 31. At the bottom, there are sections for "공지사항" (Notice) with a list of dates and events, "최근게시물" (Recent Posts) with links to OrCAD 16.6 Lite Program (All P., Captu., SPB 16.6 Hotfix_004), and "교육세미나이벤트" (Education Seminar Event) with a table of seminars.

날짜	제목
1	2
3	4
5	6
7	8
9	10
11	12
13	14
15	16
17	18
19	20
21	22
23	24
25	26
27	28
29	30
31	

날짜	제목
13.03.27~13.03.29	Virtuoso Schematic..
13.03.27~13.03.29	PCB 설계기초
13.03.25~13.03.26	Cadence Virtuoso S..
13.03.20~13.03.22	Allegro PCB Atwork..
13.03.19~13.03.22	OrCAD 기본

<http://npeda.co.kr/index.action>

OrCAD 16.6 Lite Program

국립 행사

106,783

+ MORE

최근게시물

+ MORE

교육세미나이벤트

DEMO OrCAD 16.6 Lite Program (All P..

DEMO OrCAD 16.6 Lite Program (Captu..

PATCH SPB 16.6 Hotfix_004

INSTALL OrCAD & Allegro(SPB) v16.6 설치 ..

LICENSE 라이선스 매니저 v12.01

LIBRARY OrCAD PCB Editor 라이브러리 v16.3, ..

INSTALL Allegro Free viewer v16.5

DEMO OrCAD 16.5 Lite Program (Captu..

DEMO OrCAD 16.5 Lite Program (All P..

INSTALL OrCAD & Allegro(SPB) v16.5 설치 ..

교육 Virtuoso Schematic..

교육 PCB 설계기초 NEW

교육 Cadence Virtuoso S..

교육 Allegro PCB Atwork..

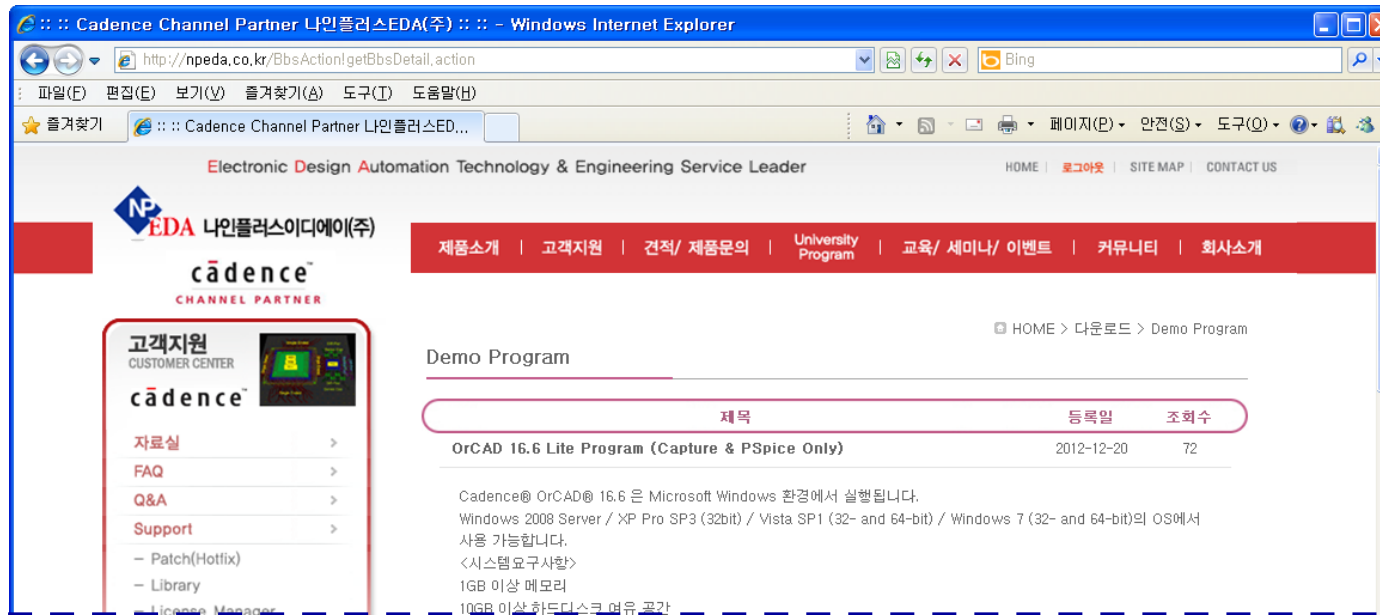
교육 [노동부] OrCAD 기본

교육 OrCAD PSpice A/D

OrCAD 16.6 Lite Program (Capture & Pspice Only)

<http://npeda.co.kr/index.action>

OrCAD 16.6 Lite Program



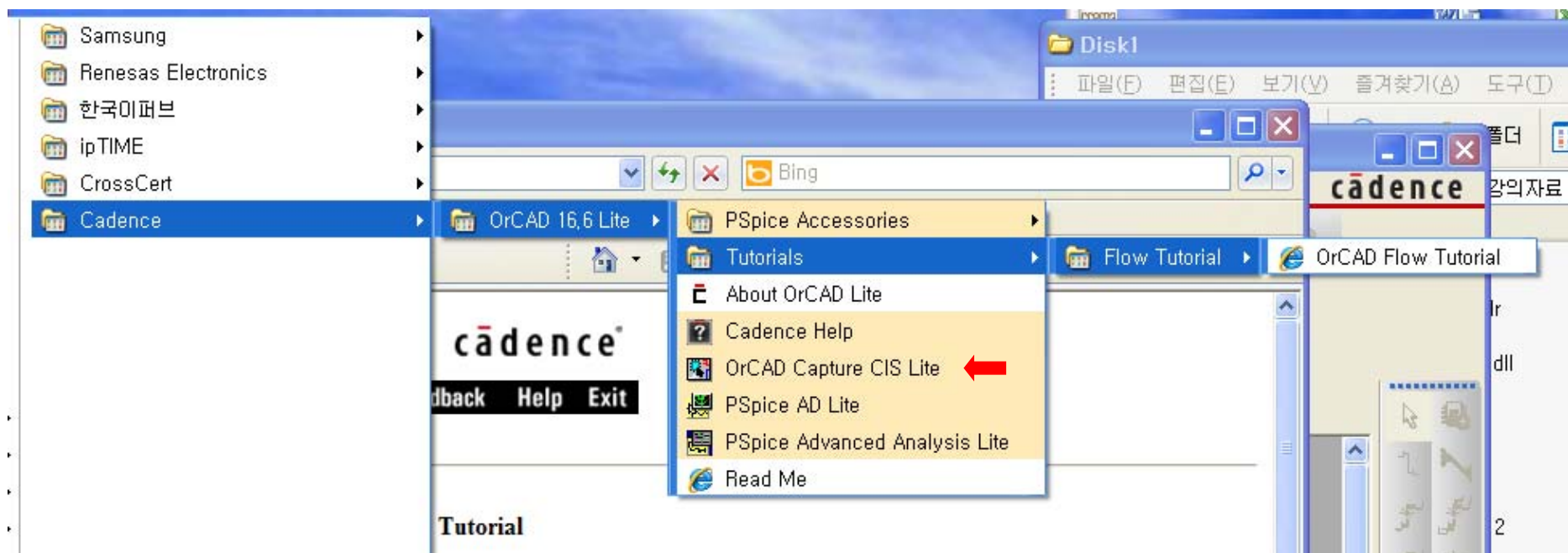
- Sensitivity Analysis
 - ☐ Only one measurement specification is allowed.
 - ☐ A maximum of three devices with tolerance are supported.
 - ☐ Maximum of 20 runs are supported.
- Encrypted parameterized models cannot be simulated.
- The Optimizer Random Engine can make a maximum of 5 runs.

다운로드

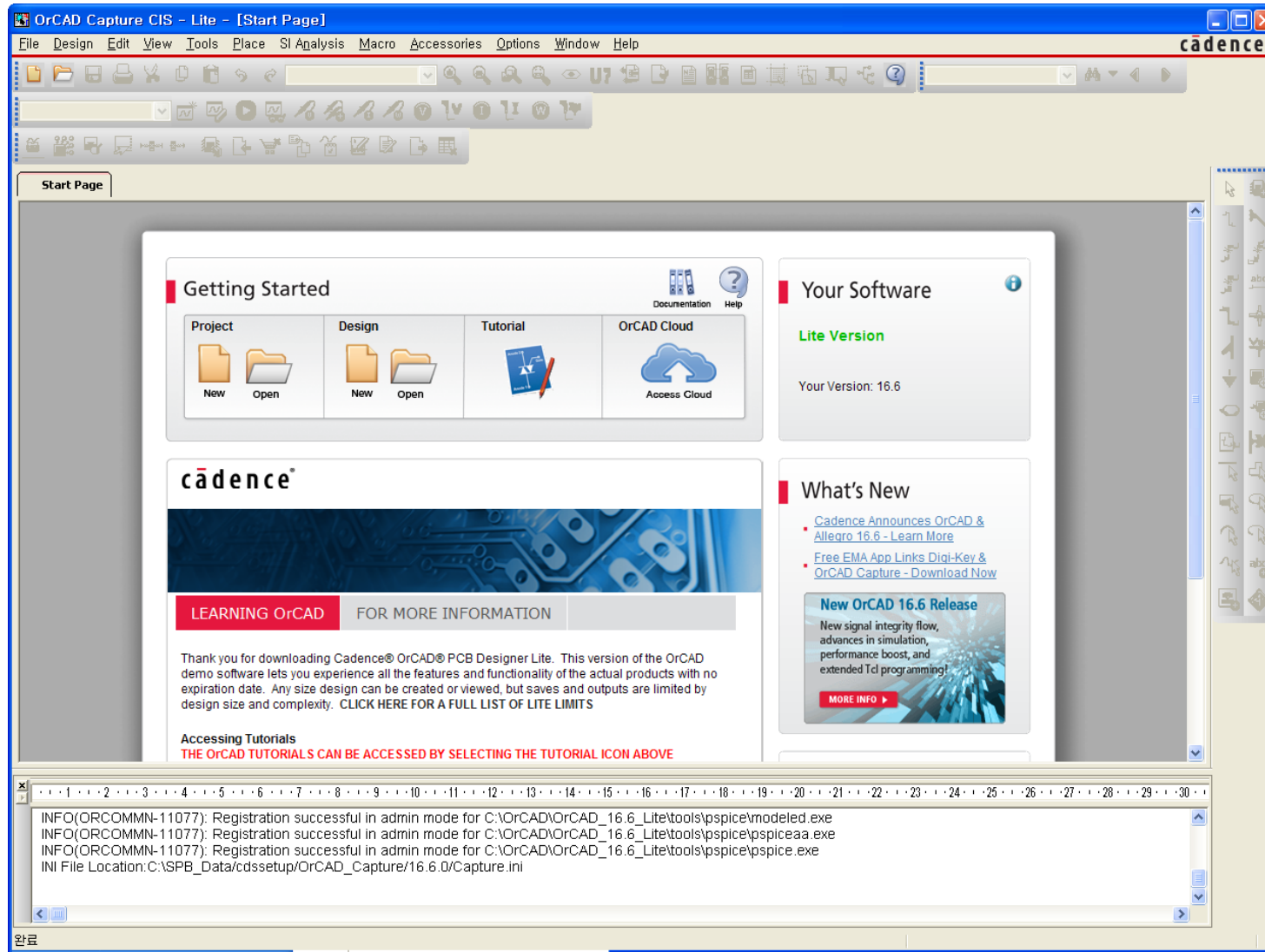
(위 파일은 Zip파일로 압축되어 있습니다. 임의의 폴더에 압축을 푸신 다음 실행하시면 됩니다.)
(해당 자료에 대하여 링크하거나 재배포 행위를 금합니다.)

<http://npeda.co.kr/BbsAction!getBbsDetail.action>

OrCAD 16.6 Lite Program



OrCAD 16.6 Lite Program



OrCAD 16.6 Lite Program

Cadence® OrCAD® 16.6 은 Microsoft Windows 환경에서 실행됩니다.

Windows 2008 Server / XP Pro SP3 (32bit) / Vista SP1 (32- and 64-bit) / Windows 7 (32- and 64-bit)의 OS에서 사용 가능합니다.

<시스템요구사항>

1GB 이상 메모리

10GB 이상 하드디스크 여유 공간

300MB 이상 가상메모리

CD-ROM/ 드라이브

해상도 1024 x 768 이상의 64,000 컬러 윈도우 디스플레이 (1280 x 1024 권장)

OrCAD PCB Editor는 그래픽 카드가 OpenGL 지원해야 함

OrCAD 16.6 Lite Program

OrCAD Capture CIS Lite

- You cannot save designs that have more than **75 nets**, including the hierarchical blocks in the design. You can still view or create larger designs.
- You cannot save a design with more than **60 parts**, including the hierarchical blocks in the design. You can still view or create larger designs.
- You cannot have more than **1000 parts in the Capture CIS database**.
- The Internet Component Assistant (ICA) tab in the CIS Explorer window opens the About ActiveParts page (www.activeparts.com) and not the component search page.
- You cannot create parts with more than 100 pins.
- The Capture FPGA flow is not available.
- You cannot validate Electrical Csets

OrCAD 16.6 Lite Program

PSpice A/D Lite

- Circuit simulation limited to circuits with up to **75 nodes**, **20 transistors**, no sub-circuit limits but 65 digital primitive devices, and 10 transmission lines (ideal or non-ideal) with not more than four pairwise coupled lines.

- **Device characterization and parameterized part creation using the PSpice Model Editor limited to diodes.**

- No limit to stimulus generation using Stimulus Editor.

- Sample model library named eval.lib (containing analog and digital parts) and evalp.lib (containing parameterized parts) are provided.

- The library nomd.lib is configured for simulations. The nomd.lib file references the set of libraries that can be used with the lite version.

- You cannot simulate parameterized parts that are not from the evalp.lib library. This library consists of parametrized resistor, source, and diode.

- You cannot use Level 3 of Core model (Tabrizi), MOSFET BSIM 3.2, or MOSFET BSIM 4 models.

- Displays only simulation data created using the lite version of the simulator.

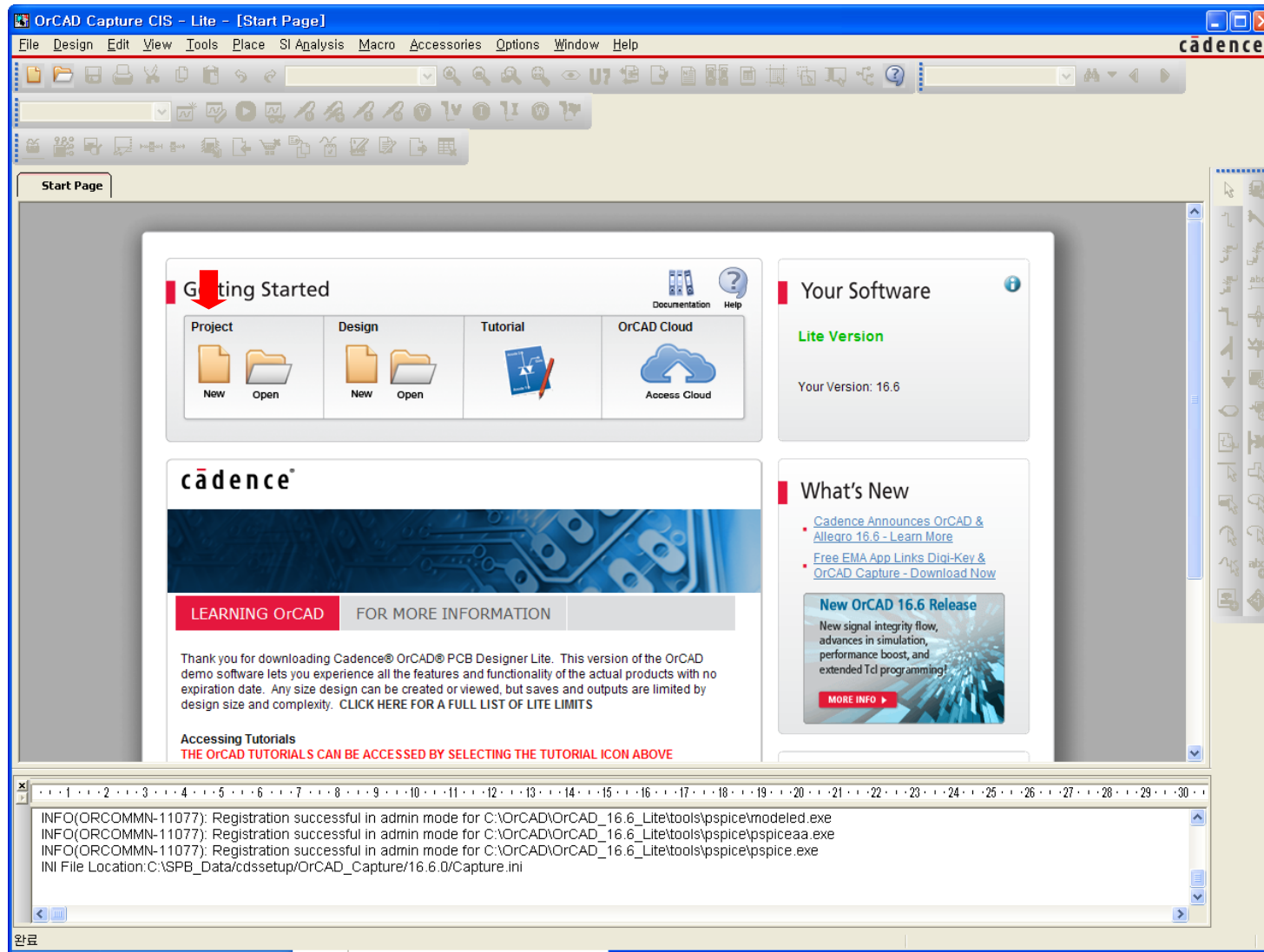
- Magnetic Parts Editor allows you to design power transformers only. The database shipped with Magnetic Parts Editor cannot be edited and contains a single core.

- The Model Import Wizard supports parts and simulation models that have a maximum of two pins or two terminals, respectively.

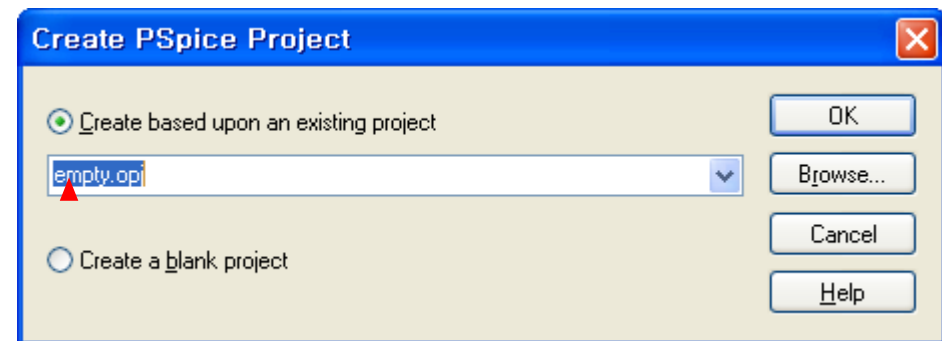
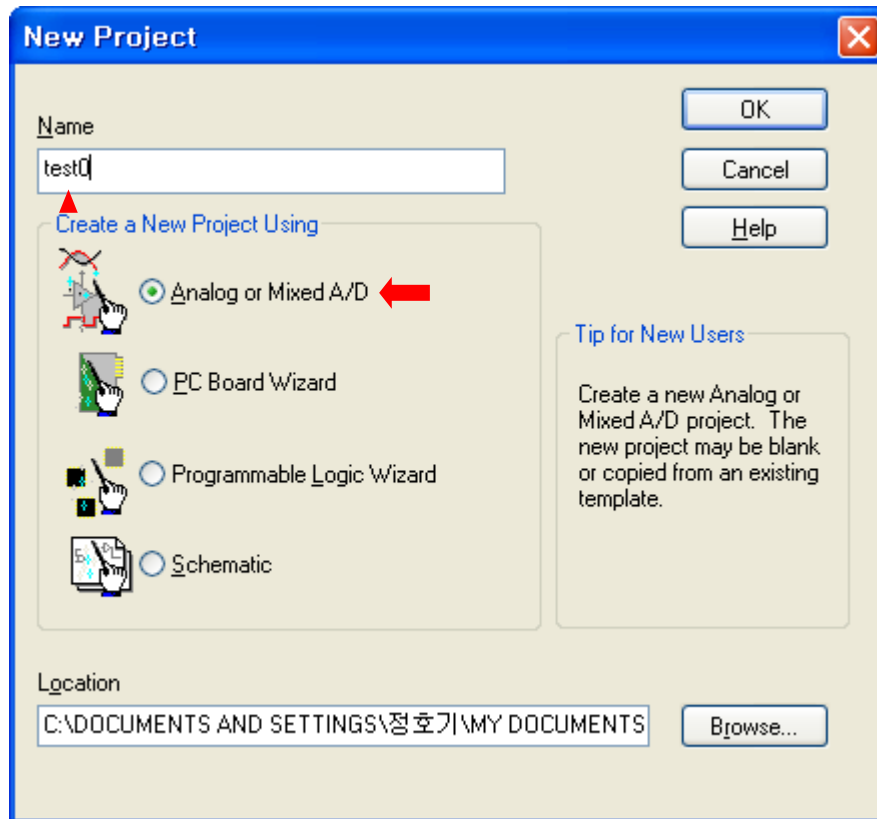
- The maximum nodes in a digital circuit can be equal to or less than 250.

- The non-ideal Tline is limited to 4.

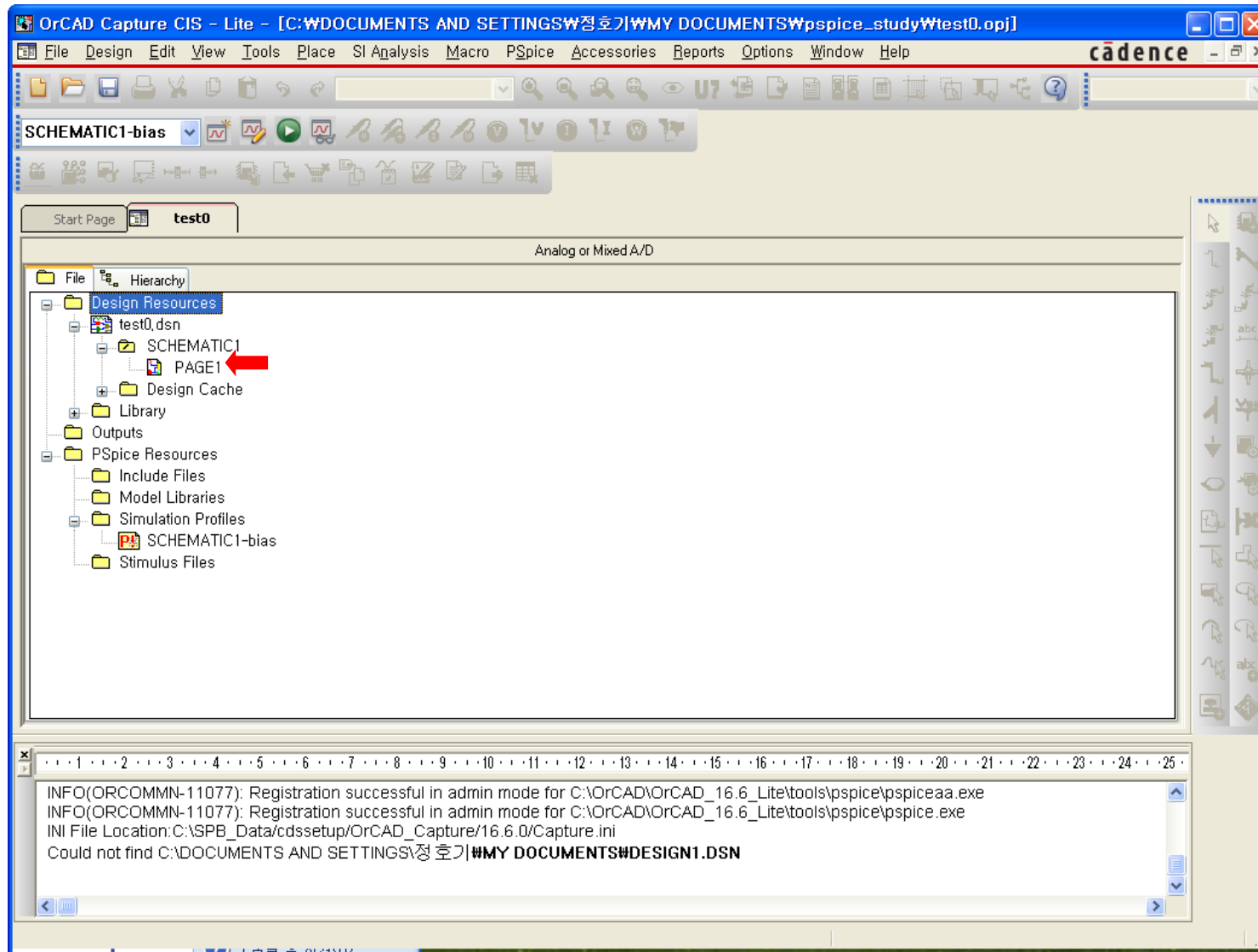
Project



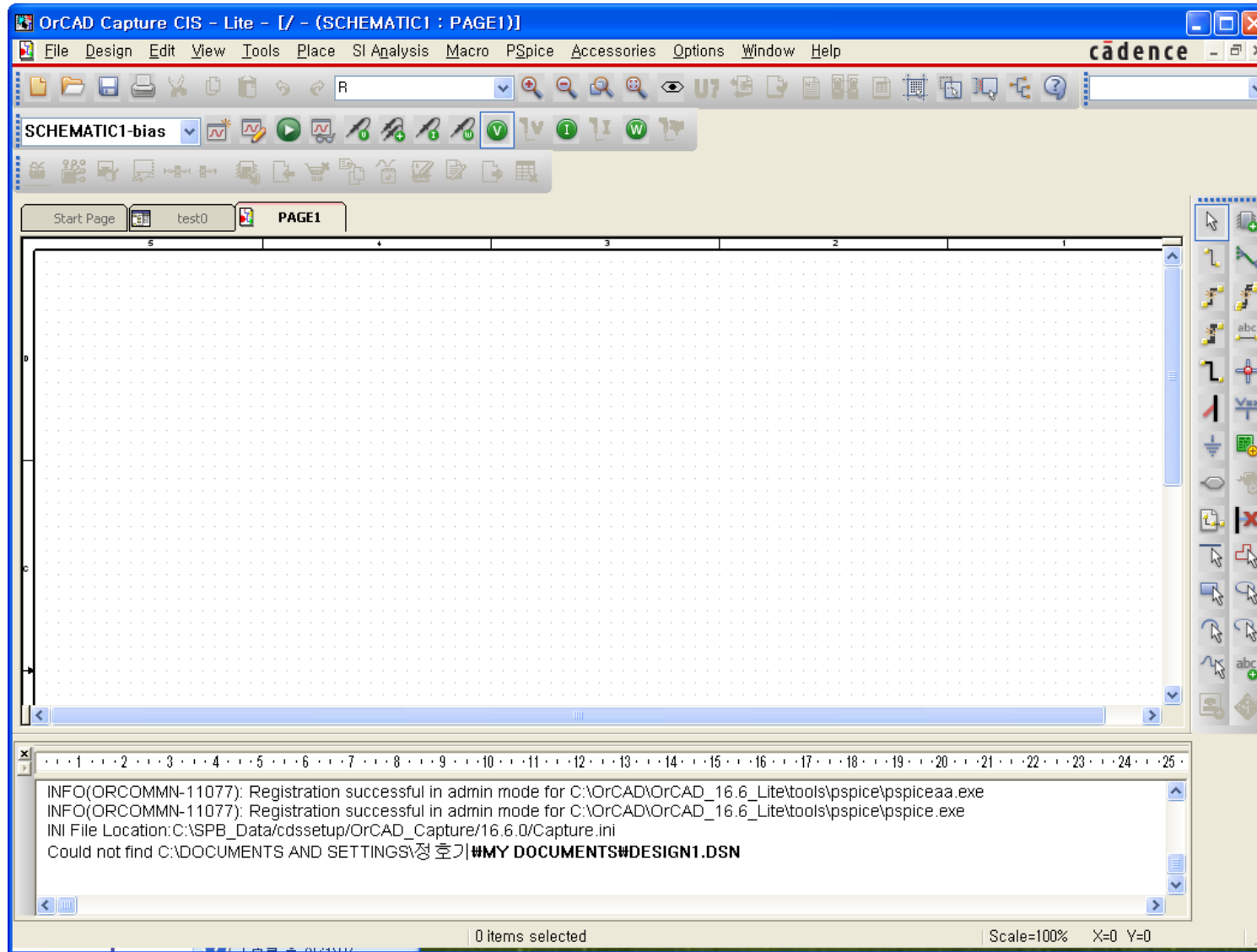
Project



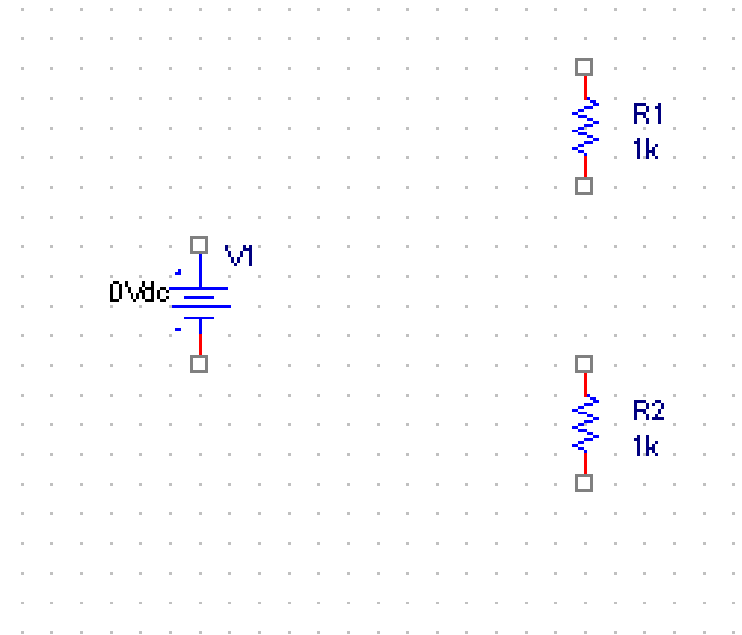
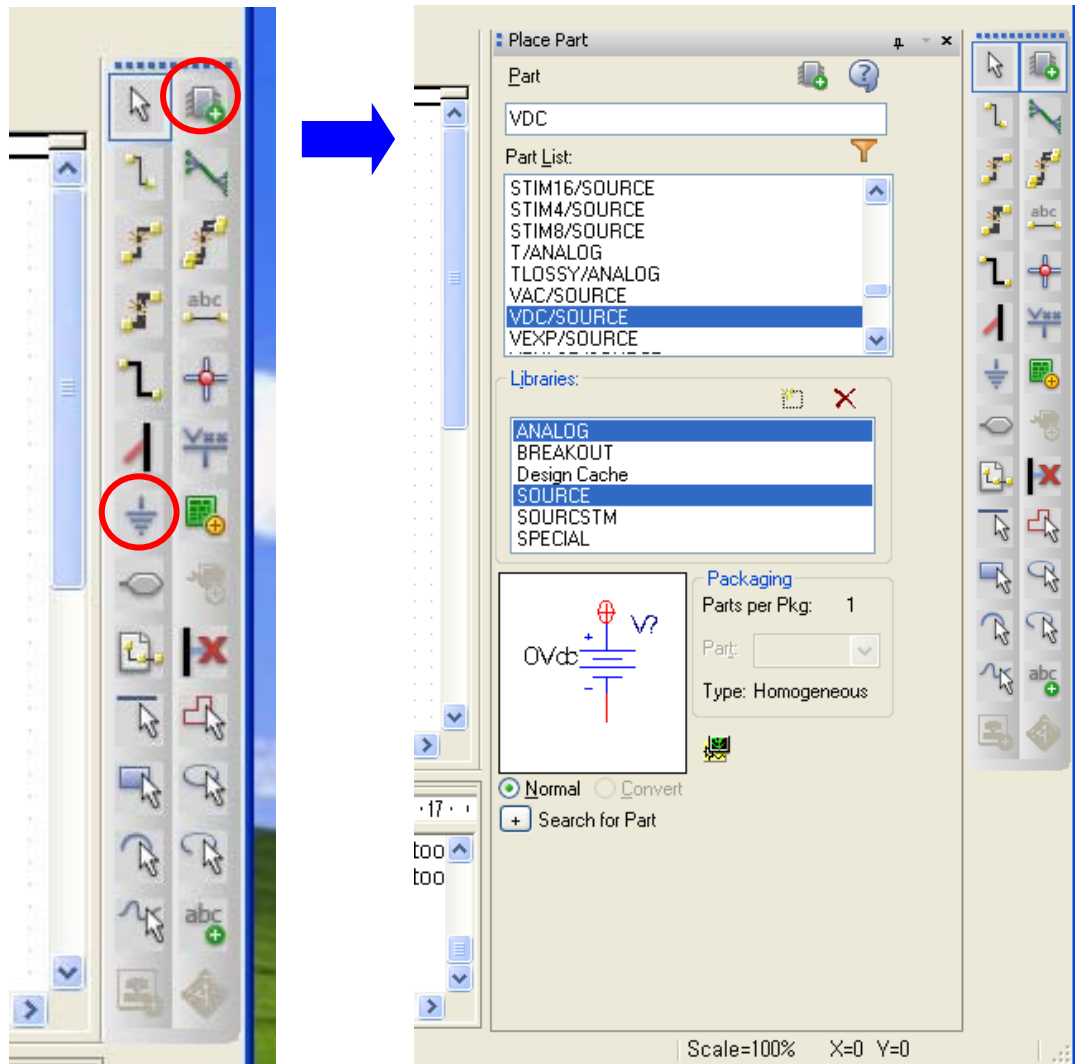
Project



Design



Design

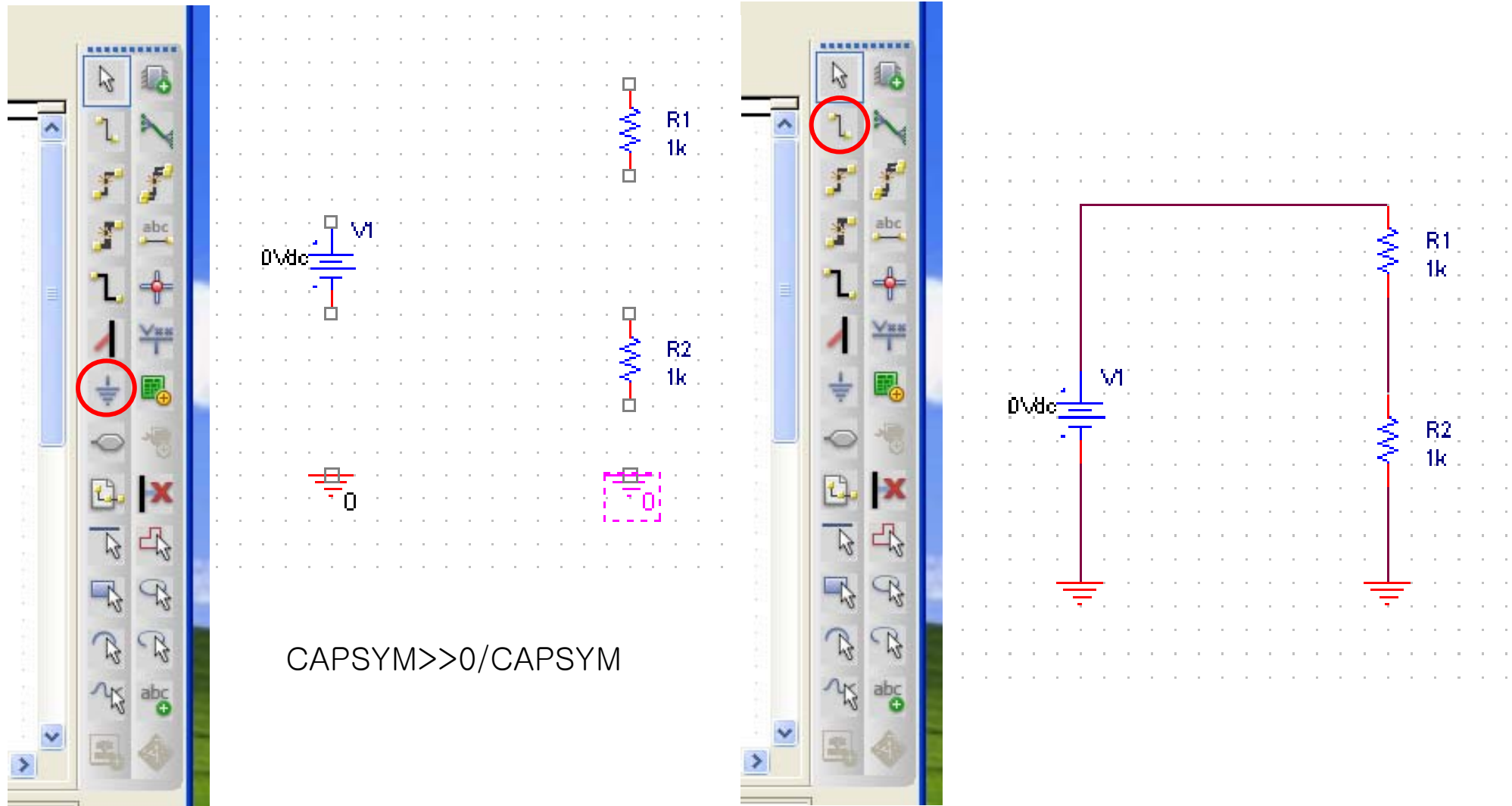


Libraries>>Part List

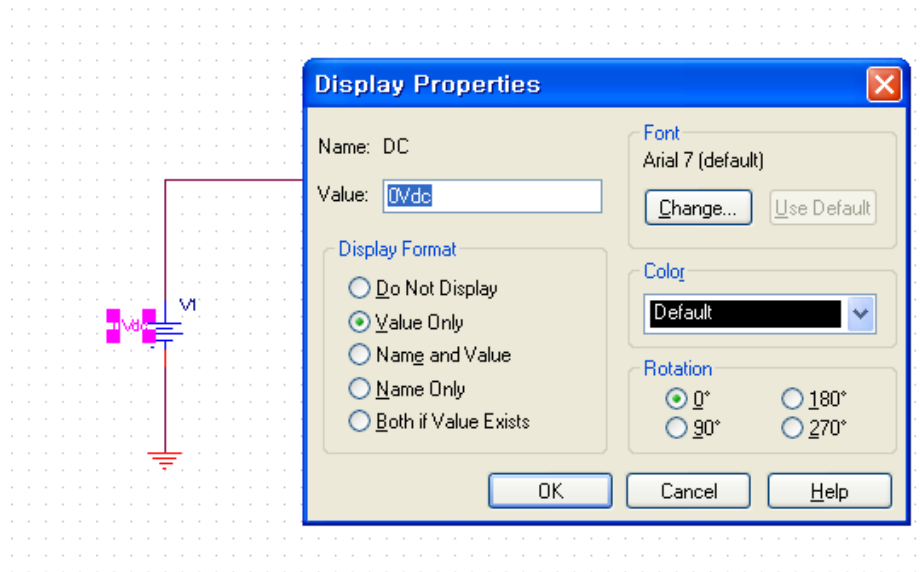
SOURCE>>VDC

ANALOG>>R

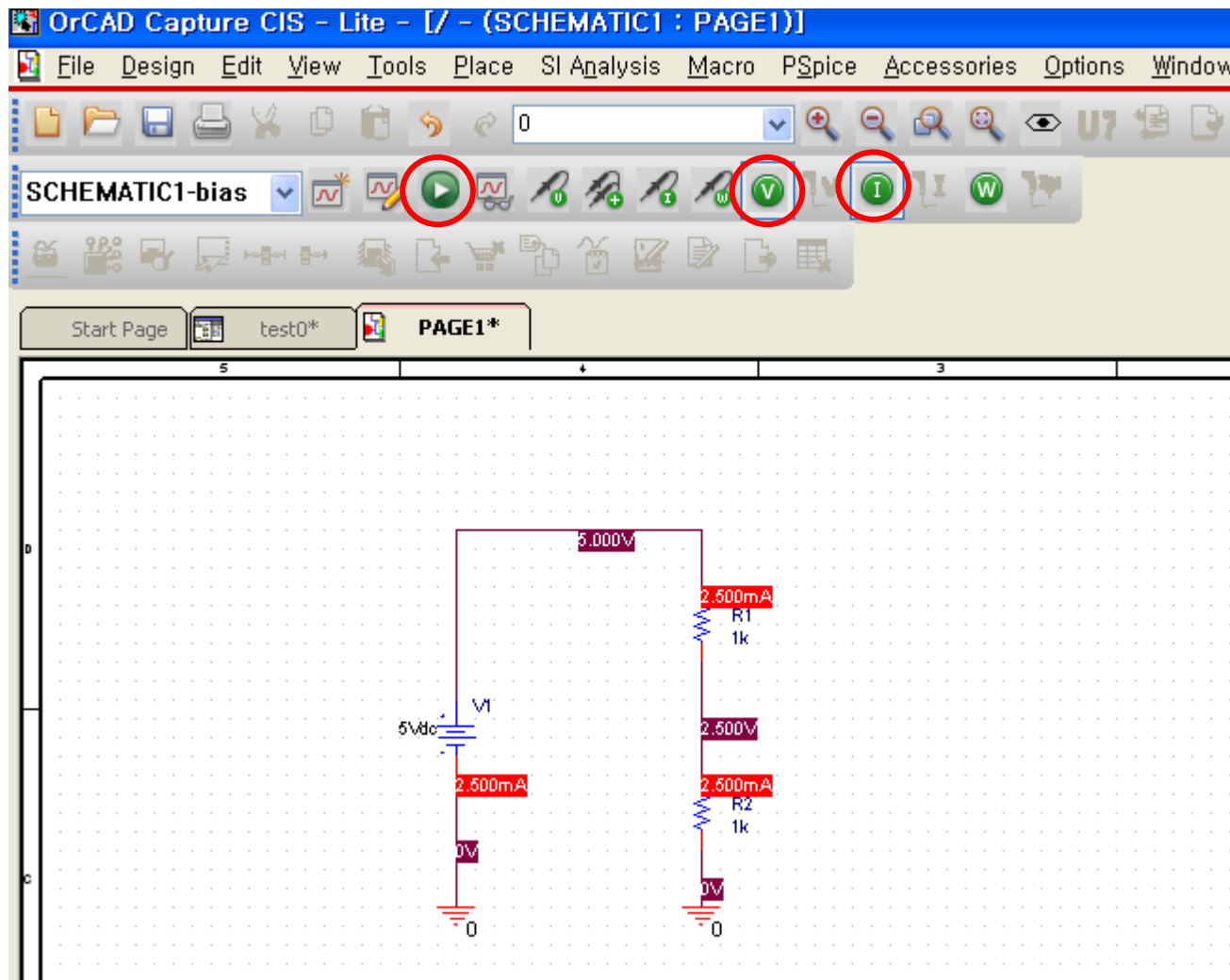
Design



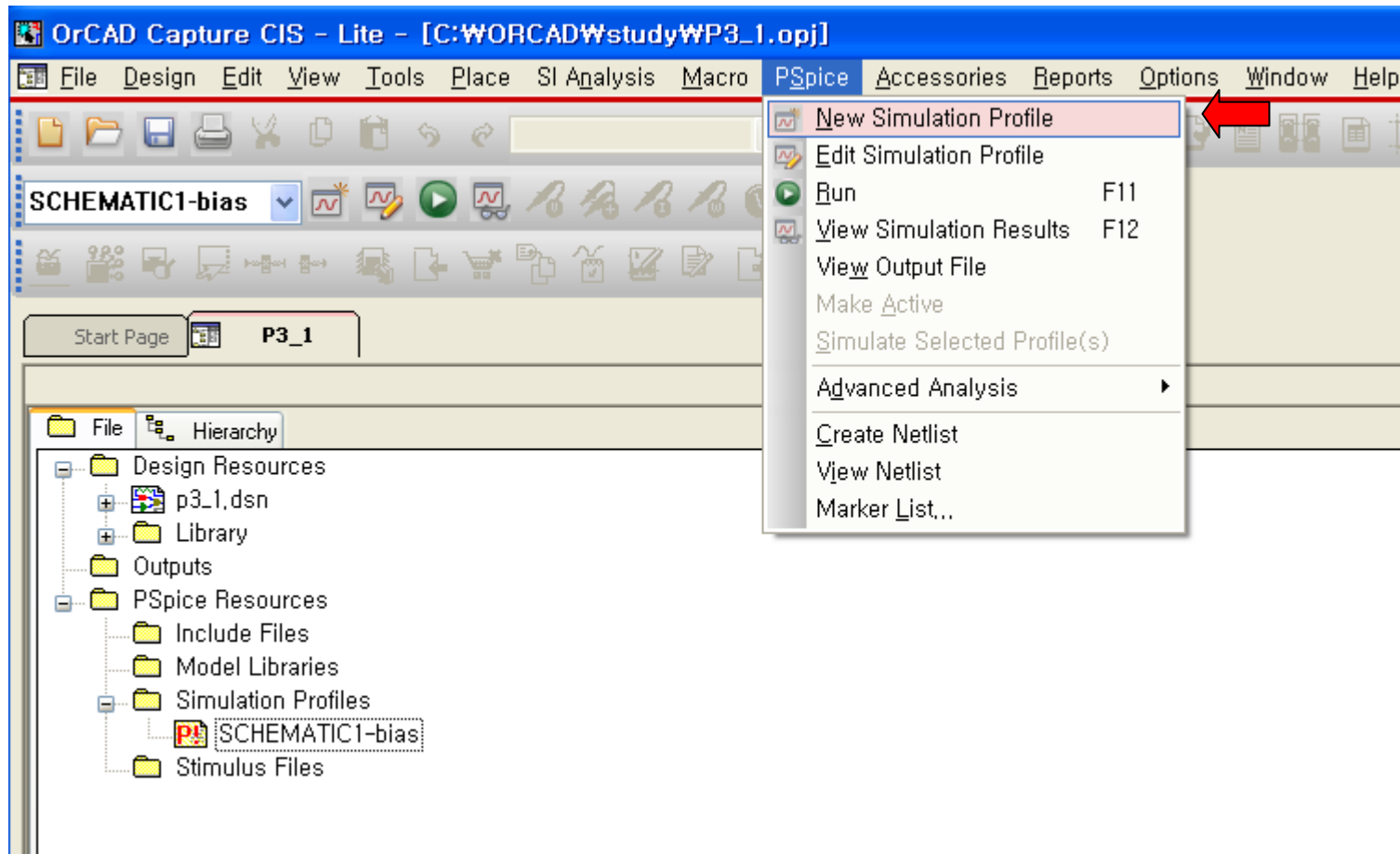
Design



Simulation



Simulation Profile 추가



Simulation Profile 추가

New Simulation

Name:

Inherit From: ...

Root Schematic: SCHEMATIC1

Simulation Settings - transient

General Analysis Configuration Files Options Data Collection Probe Window

Analysis type:

Options:

- ☒ General Settings
- ☐ Monte Carlo/Worst Case
- ☐ Parametric Sweep
- ☐ Temperature (Sweep)
- ☐ Save Bias Point
- ☐ Load Bias Point
- ☐ Save Check Points

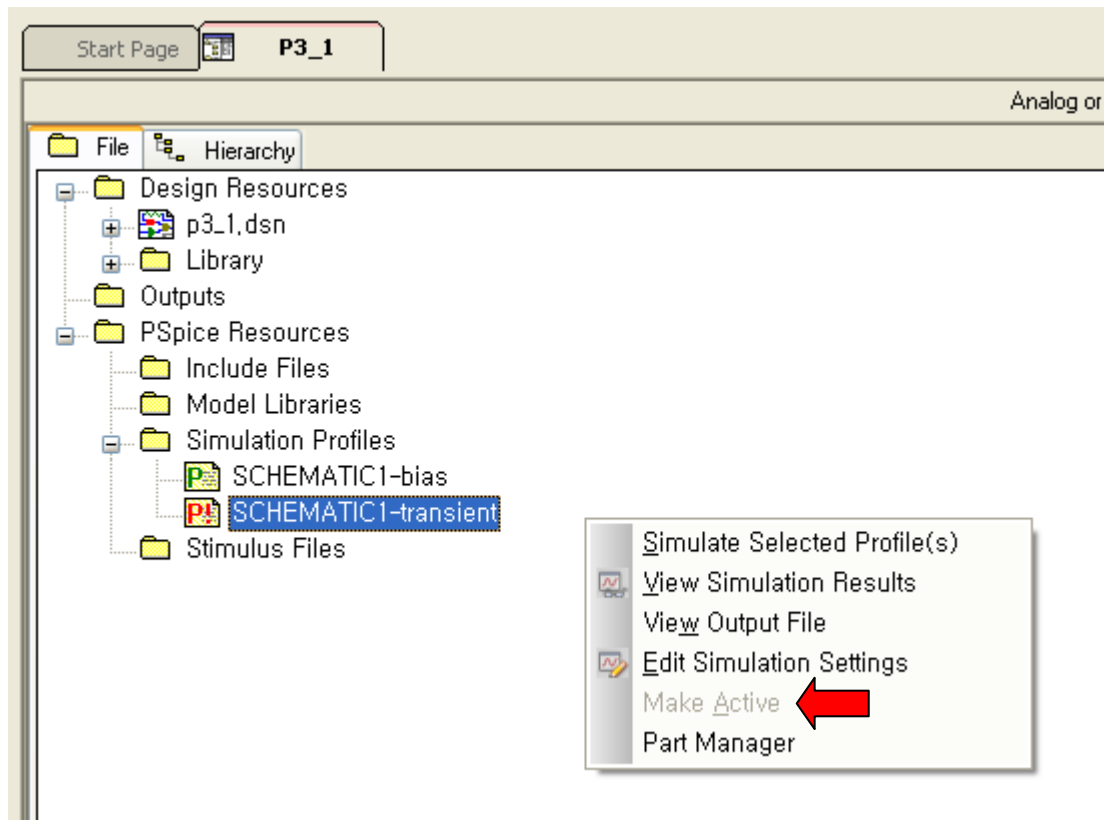
Transient options

Maximum step size: seconds

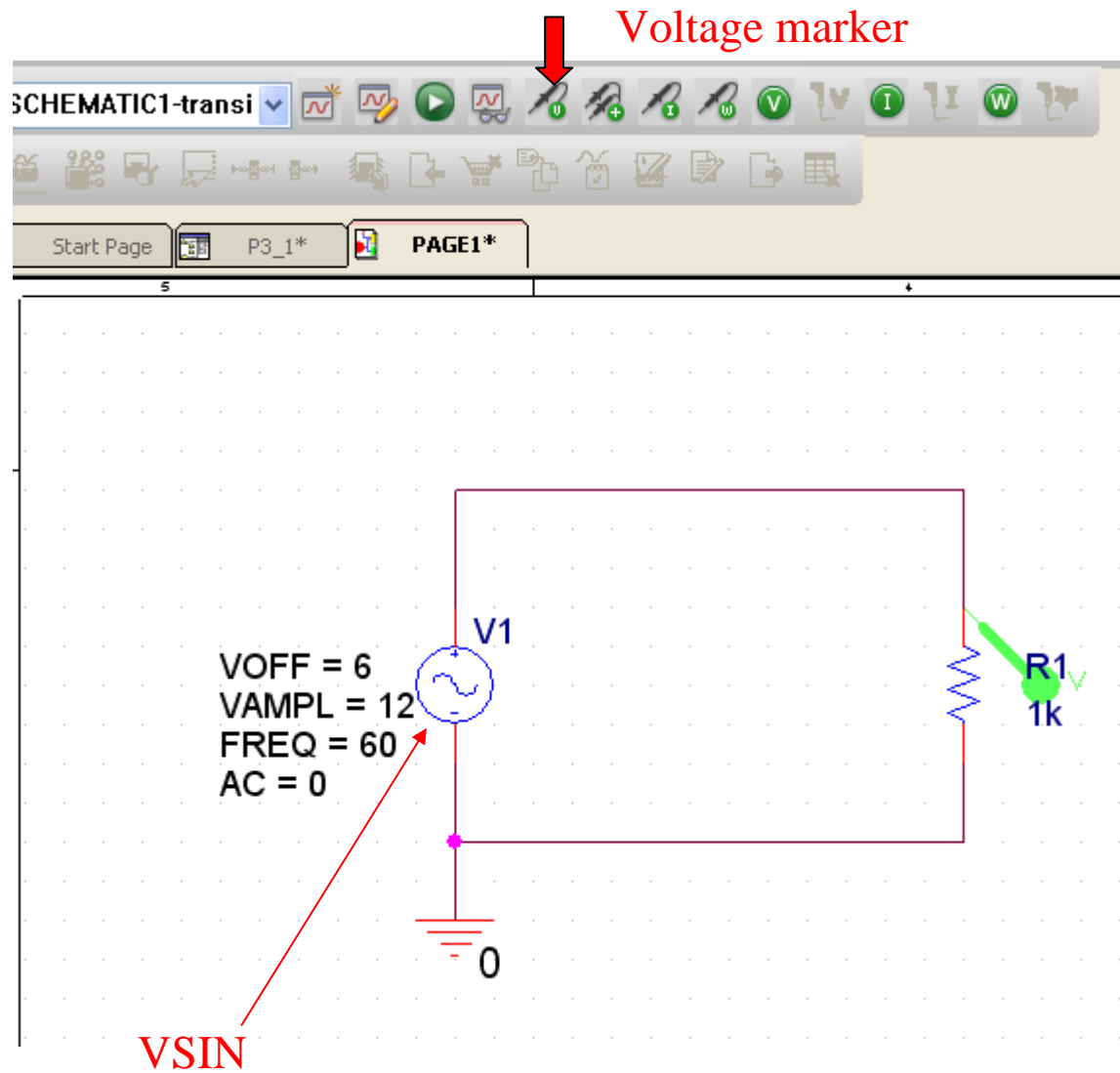
☐ Skip the initial transient bias point calculation (SKIPBP)

☐ Run in resume mode

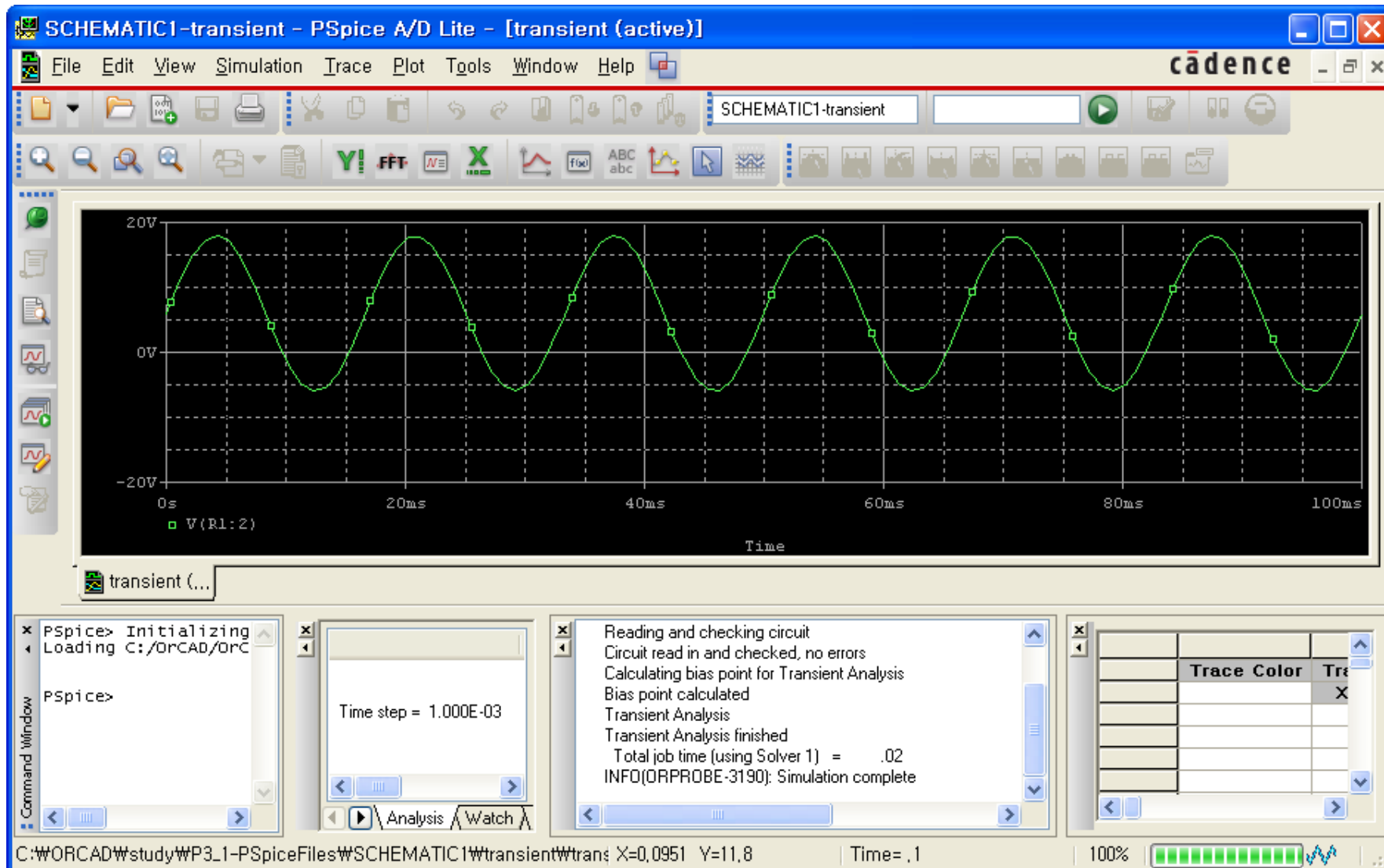
Simulation Profile 추가



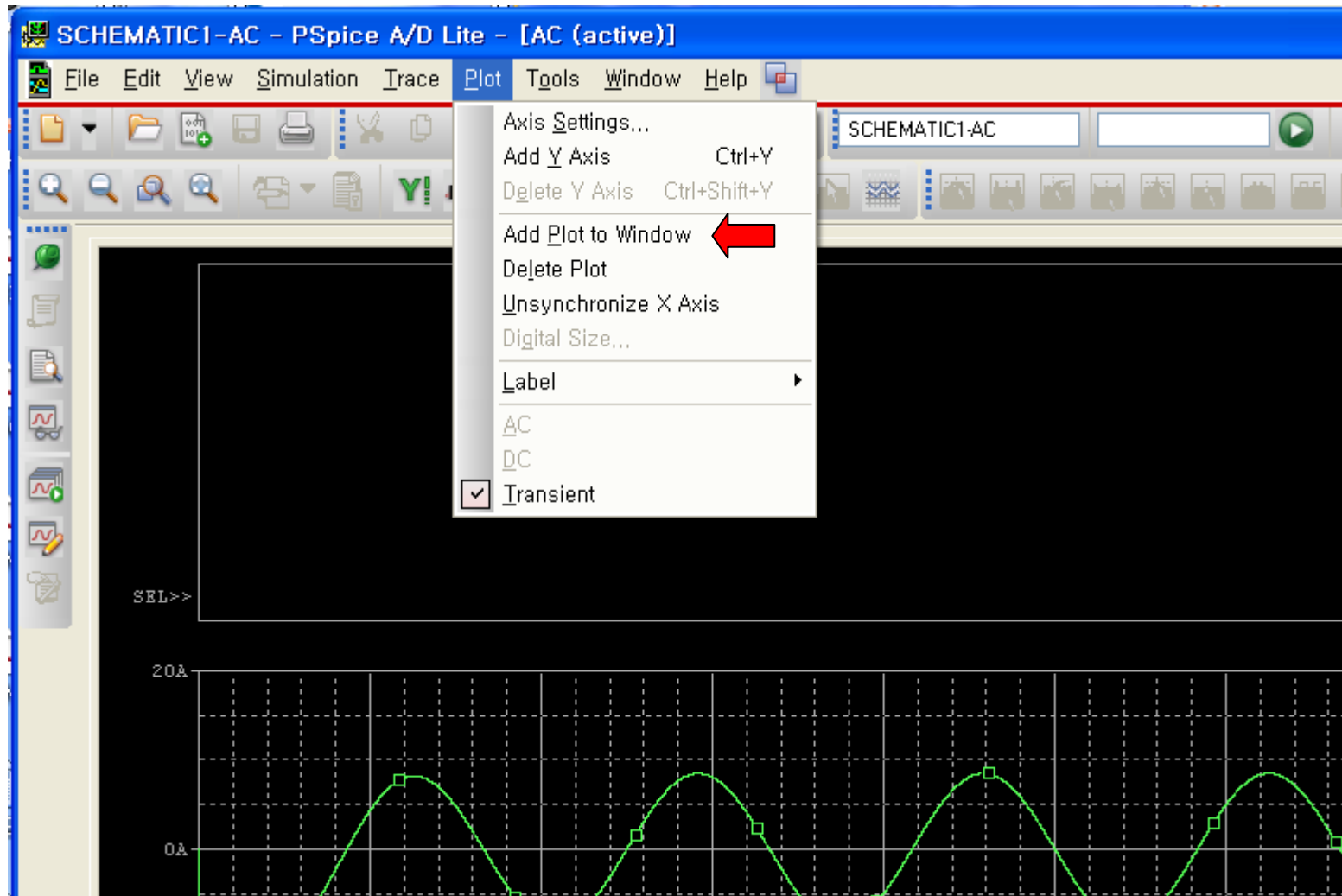
Marker



Simulation 결과

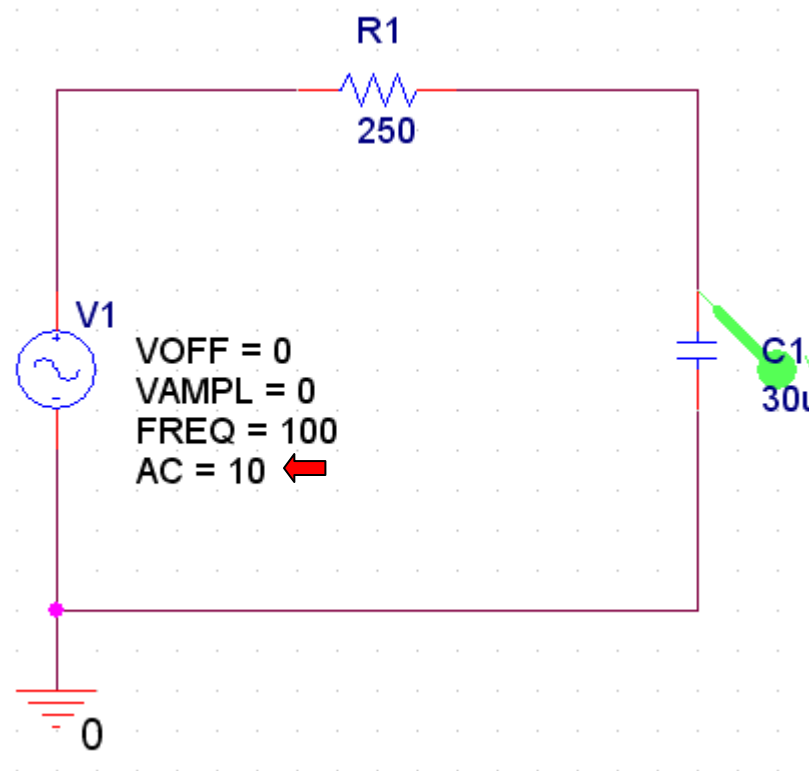


Plot 추가



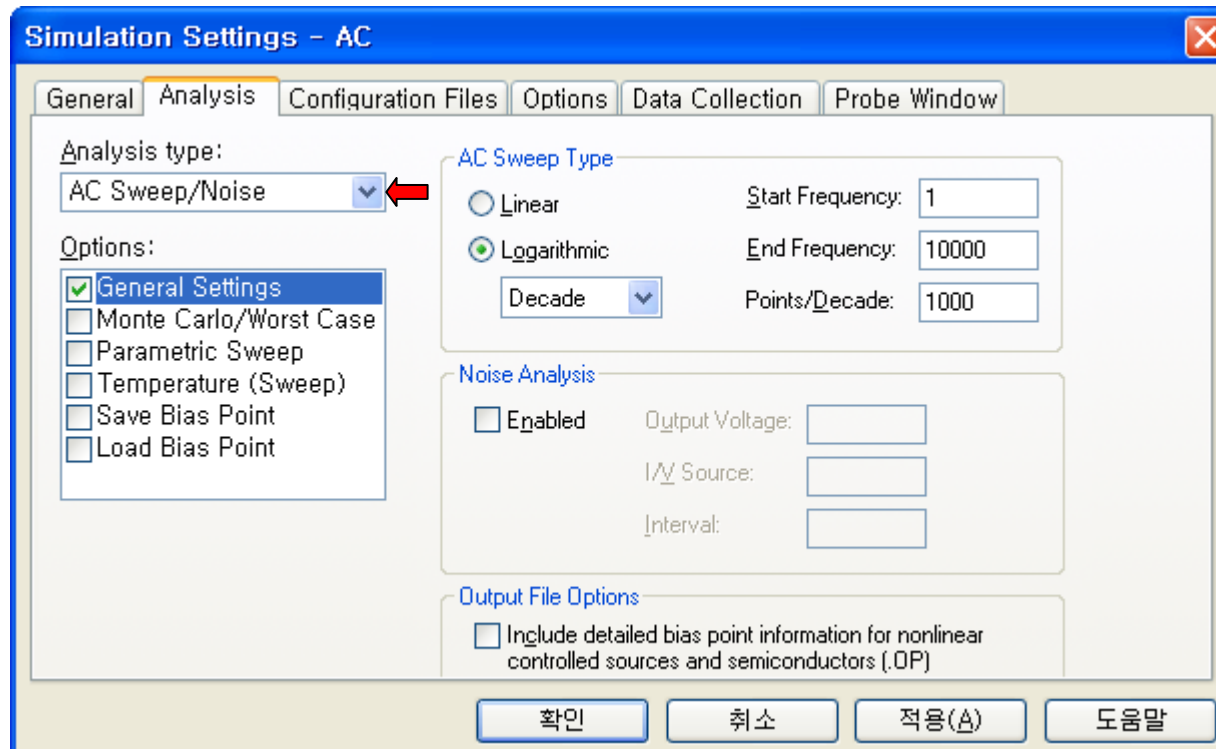
AC SWEEP

문) 아래 회로의 주파수 응답을 구하라.



AC SWEEP

PSpice>>New Simulation Profile로 새로운 simulation profile 만들고,
Analysis type을 “AC Sweep/Noise”로 선택.



주파수 응답

