Introduction to Embedded Hardware

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Outline

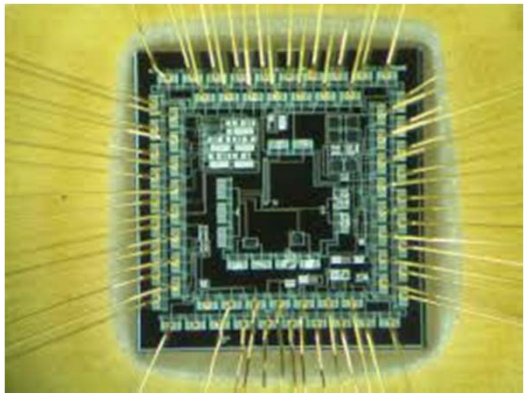
1. Integrated circuits
2. Circuit boards

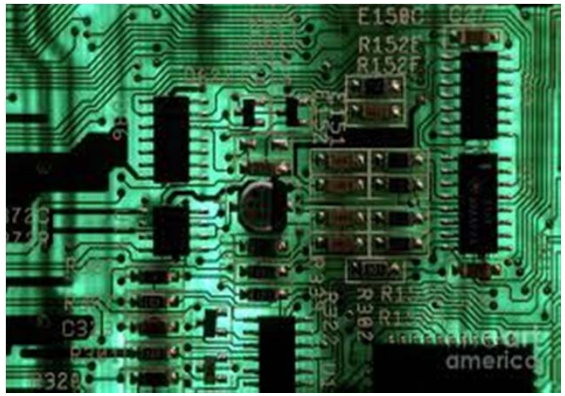
Integrated Circuits

Integrated Circuit (IC)

❒ Integrated circuit

- Electrical network of miniaturized electronic components on a monolithic semiconductor substrate by photolithography





❒ Electronic components

- Transistors, resistors, capacitors and the metallic interconnect of these components
- Created onto a piece of semiconductor, typically silicon

Complexity

- Modern ICs are enormously complicated
  - A large chip, as of 2009, has close to 1 billion transistors
  - Apple's A8 processor has 2 billion transistors on a 20 nm process

Complexity

- **The rules for what can and cannot be manufactured are also extremely complex**
  - An IC process as of 2006 may well have more than 600 rules
  - Designers must account for its statistical nature

- **The complexity of modern IC design has led to the extensive use of automated design tools**
  - **EDA software is used for the design, test, and verification of IC under development**

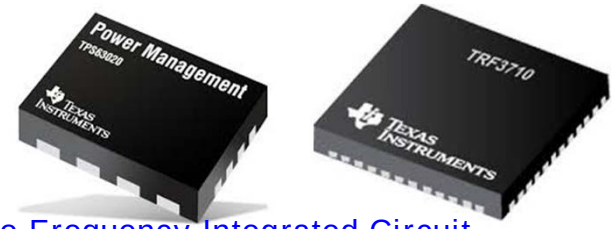
Two Types of IC Design

❒ Digital IC design

- Microprocessors, FPGAs, memories (RAM, ROM, and flash) and digital ASICs
- Focus on logical correctness, maximizing circuit density, and placing circuits so that clock and timing signals are routed efficiently

❒ Analog IC design

- Power management ICs and RF ICs



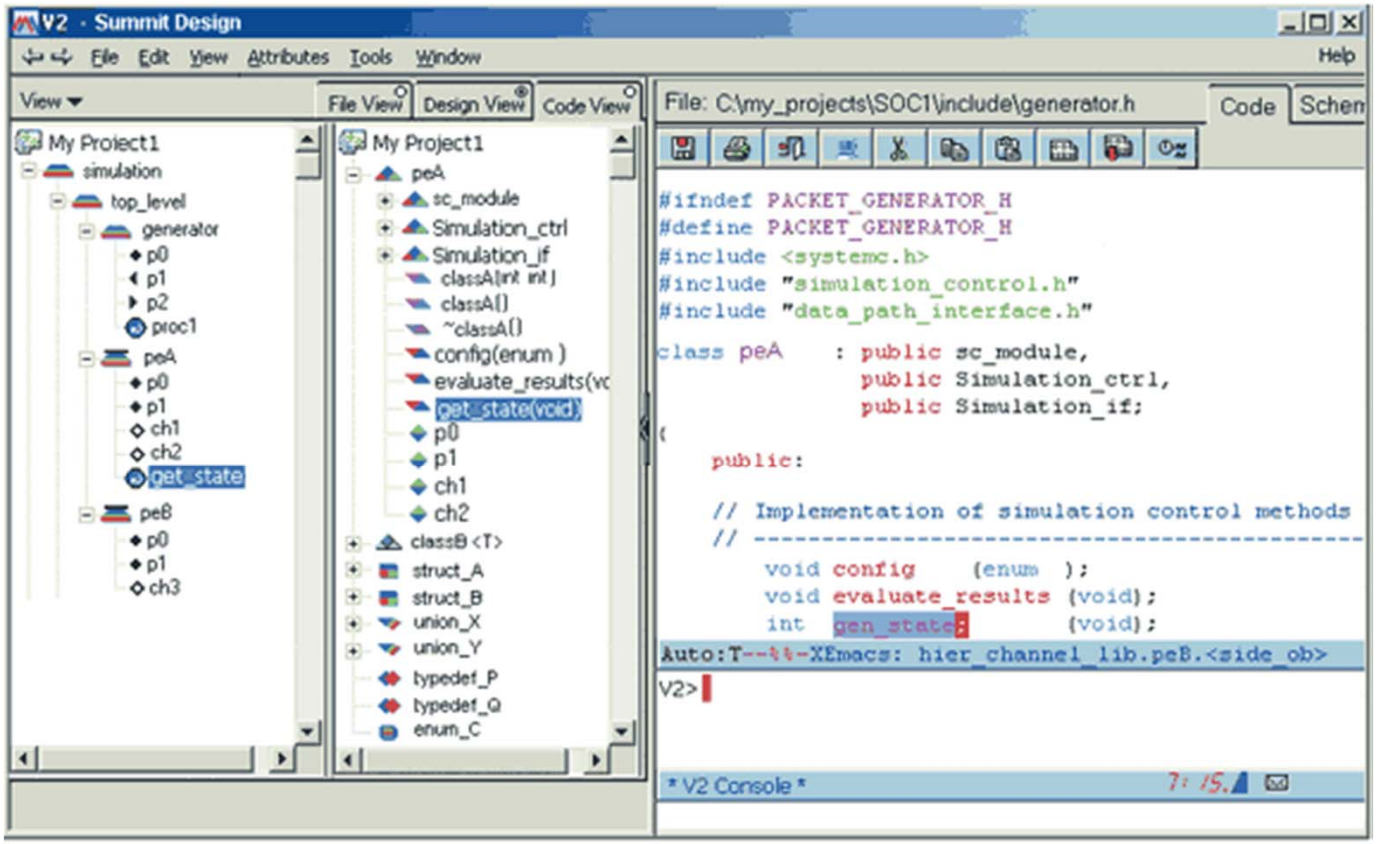
Radio Frequency Integrated Circuit

- Used in the design of op-amps, linear regulators, phase locked loops, oscillators and active filters
- More concerned with the physics of the semiconductor devices such as gain, matching, power dissipation, and resistance
- Analog ICs use larger area than digital ICs

Digital IC Design

- **Three parts**
  - **System-level design**
    - Create the user functional specification
    - The user may use a variety of languages and tools
      - ✓ C/C++, SystemC, SystemVerilog Transaction Level Models, Simulink and MATLAB
  - **RTL design**
    - Convert the user specification into a register transfer level (RTL) description
      - ✓ Describe the exact behavior of the digital circuits on the chip as well as the interconnections to inputs and outputs.
  - **Physical design**
    - Take the RTL and a library of available logic gates, and create a chip design
    - Involves figuring out which gates to use, defining places for them, and wiring them together

System-Level Design (C++)



1. Visual Elite 4.0 is a SystemC-centric design platform that provides both hardware- and software-oriented views into designs.

RTL Design (Verilog)

```
module mymod (i1, clk, o1);
input wire i1;
input wire clk;
output reg o1;
always @(clk) begin
    if (clk) o1 <= i1;
end
endmodule;
```

Latch example

```
module mymod (i1, i2, sel, clk, o1);
input wire i1, i2, sel;
input wire clk;
output reg o1;
wire mux_out;

assign mux_out = (sel) ? i1 : i2;

always @(posedge clk) begin
    o1 <= mux_out;
end
endmodule;
```

MUX example

Logic Synthesis in Physical Deisgn (RTL to netlist)

- Lower-level representation than RTL
  - Represents transistor-level logic
  - If synthesized, transistors wrapped in library cells
  - Library cells contain true transistor logic

```
always @(posedge clk) begin
  for (int i=0; i<3; i++)
  begin
    if (enable[i]) begin
        foo[i] <= newval[i];
    end
  end
end
```

RTL

```
y00EnFlop(foo_0,newval_0,enable_0,
clk);
y00EnFlop(foo_1,newval_1,enable_1,
clk);
y00EnFlop(foo_2,newval_2,enable_2,
clk);
y00EnFlop(foo_3,newval_3,enable_3,
clk);
```

netlist

RTL Design and Physical Design

- RTL design is responsible for the chip doing the right thing
  - This is the hardest part, and the domain of functional verification
- The third step, physical design, does not affect the functionality at all (if done correctly) but determines how fast the chip operates and how much it costs
  - There is not a straightforward progression
  - Considerable iteration is required to ensure all objectives are met simultaneously (design closure)

Physical Design Process

1. Floorplanning: The RTL of the chip is assigned to gross regions of the chip, input/output (I/O) pins are assigned and large objects (arrays, cores, etc.) are placed.
2. Logic synthesis: The RTL is mapped into a gate-level netlist in the target technology of the chip.
3. Placement: The gates in the netlist are assigned to nonoverlapping locations on the die area.
4. Logic/placement refinement: Iterative logical and placement transformations to close performance and power constraints.
5. Clock insertion: Clock signal wiring is (commonly, clock trees) introduced into the design.
6. Routing: The wires that connect the gates in the netlist are added.
7. Postwiring optimization: Performance (timing closure), noise (signal integrity), and yield (Design for manufacturability) violations are removed.
8. Design for manufacturability: The design is modified, where possible, to make it as easy and efficient as possible to produce. This is achieved by adding extra vias or adding dummy metal/diffusion/poly layers wherever possible while complying to the design rules set by the foundry.
9. Final checking: Since errors are expensive, time consuming and hard to spot, extensive error checking is the rule, making sure the mapping to logic was done correctly, and checking that the manufacturing rules were followed faithfully.
10. Tapeout and mask generation: the design data is turned into photomasks in mask data preparation.
    - Tapeout: artwork for the photomask of a circuit

Electronic Design Automation (EDA)

- Electronic design automation (EDA or ECAD) is a category of designing electronic systems such as integrated circuits and printed circuit boards
  - Design
  - Simulation
  - Analysis and verification

Design with EDA tools

- High-level synthesis (or behavioral synthesis, algorithmic synthesis) - high-level design description (e.g. in C/C++) is converted into RTL
- Logic synthesis - translation of RTL design description (e.g. written in Verilog or VHDL) into a discrete netlist of logic gates
- Schematic Capture For standard cell digital, analog, RF-like Capture CIS in Orcad by CADENCE and ISIS in Proteus
- Layout, usually schematic-driven layout, like Layout in Orcad by Cadence, ARES in Proteus

Simulation with EDA tools

- Transistor simulation – low-level transistor-simulation of a schematic/layout's behavior, accurate at device-level
- Logic simulation – digital-simulation of an RTL or gate-netlist's digital (boolean 0/1) behavior, accurate at boolean-level
- Behavioral Simulation – high-level simulation of a design's architectural operation, accurate at cycle-level or interface-level
- Hardware emulation – Use of special purpose hardware to emulate the logic of a proposed design. Can sometimes be plugged into a system in place of a yet-to-be-built chip; this is called in-circuit emulation
- Technology CAD simulate and analyze the underlying process technology
  - Electrical properties of devices are derived directly from device physics
- Electromagnetic field solvers, or just field solvers, solve Maxwell's equations directly for cases of interest in IC and PCB design

Analysis and Verification with EDA Tools

- Functional verification
- Clock Domain Crossing Verification (CDC check): Similar to linting, but these checks/tools specialize in detecting and reporting potential issues like data loss, meta-stability due to use of multiple clock domains in the design
- Formal verification, also model checking: Attempts to prove, by mathematical methods, that the system has certain desired properties, and that certain undesired effects (such as deadlock) cannot occur
- Equivalence checking: algorithmic comparison between a chip's RTL-description and synthesized gate-netlist, to ensure functional equivalence at the logical level
- Static timing analysis: Analysis of the timing of a circuit in an input-independent manner, hence finding a worst case over all possible inputs
- Physical verification, PV: checking if a design is physically manufacturable, and that the resulting chips will not have any function-preventing physical defects, and will meet original specifications

Top EDA Companies

- **Market capitalization and company as of Dec, 2011**
  - **$5.77 billion – Synopsys**
  - **$4.46 billion – Cadence**
  - **$2.33 billion – Mentor Graphics**
  - **$489 million – Magma Design Automation**
    - Synopsys acquired Magma in February 2012
  - **NT$6.44 billion – SpringSoft**
    - Synopsys acquired SpringSoft in August 2012
  - **¥11.95 billion – Zuken Inc**

Circuit Boards

Printed Circuit Board (PCB)

- Printed circuit board
  - A printed circuit board (PCB) mechanically supports and electrically connects electronic components using conductive tracks, pads and other features etched from copper sheets laminated onto a non-conductive substrate

아로새기다

- PCBs can be single sided (one copper layer), double sided (two copper layers) or multi-layer
  - Conductors on different layers are connected with plated-through holes called vias
  - Advanced PCBs may contain components - capacitors, resistors or active devices - embedded in the substrate

Electronic Components

❒ Passive components

- **Electronics components that cannot supply energy themselves**
  - Resistors, capacitors, inductors,

❒ Active components

- **Electronic components that can inject power into a circuit**
  - Transistors, triode vacuum tubes, and tunnel diodes

❒ Electromechanical components

- **Components that can carry out electrical operations by using moving parts or by using electrical connections**
  - Piezoelectric devices, crystals, resonators

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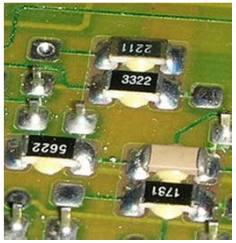
Passive Components

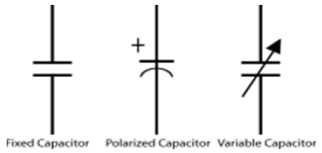
❒ Resistors

- Control current flow and voltage



❒ Capacitors

- Store and release electrical charge
- Used for filtering power supply lines, tuning resonant circuits, and for blocking DC voltages while passing AC signals



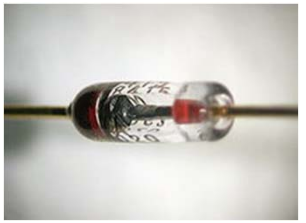
❒ Inductors

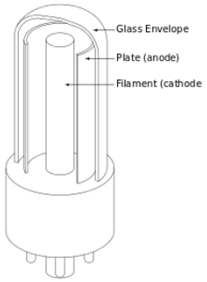
- Store electrical energy in a magnetic field

Active Components

❒ Diodes

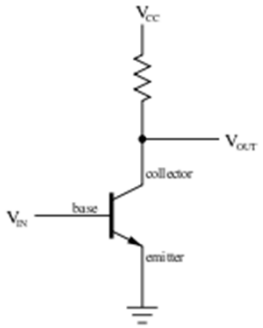
- Conduct electricity easily in one direction





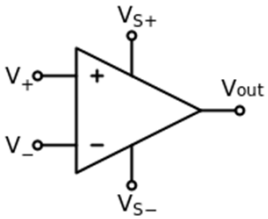
❒ Transistors

- Amplify and switch electronic signals and electrical power

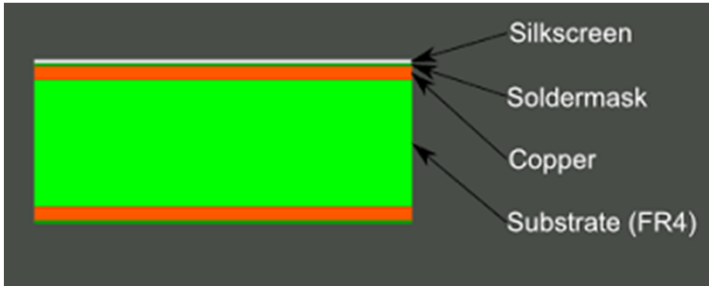


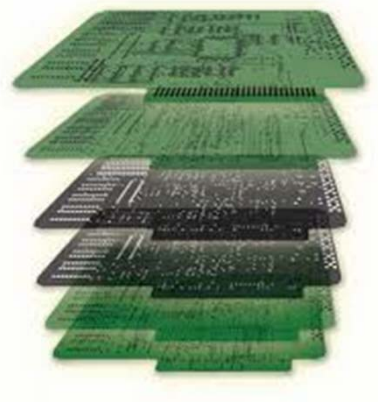
❒ OP-Amp (Operational Amplifier)

- A voltage amplifier with a differential input and, usually, a single-ended output
- An op-amp produces an output potential that is typically hundreds of thousands of times larger than the potential difference between its input terminals

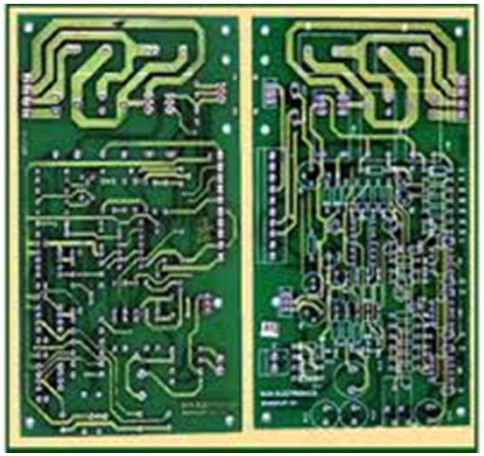


Printed Circuit Board (PCB)

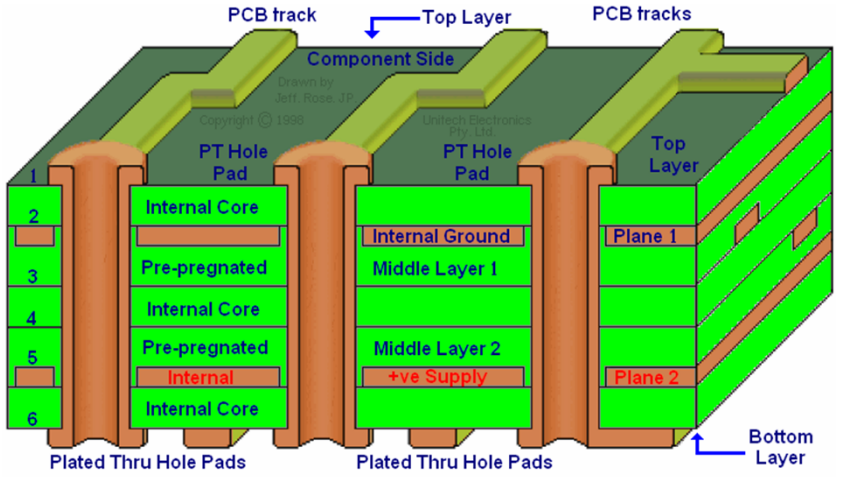




Multi-layer PCB



Double-sided PCB

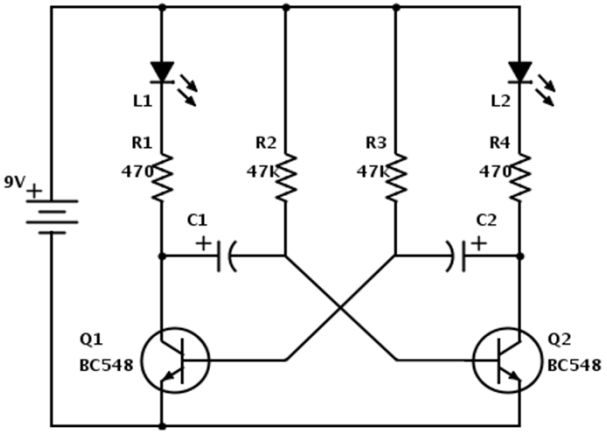


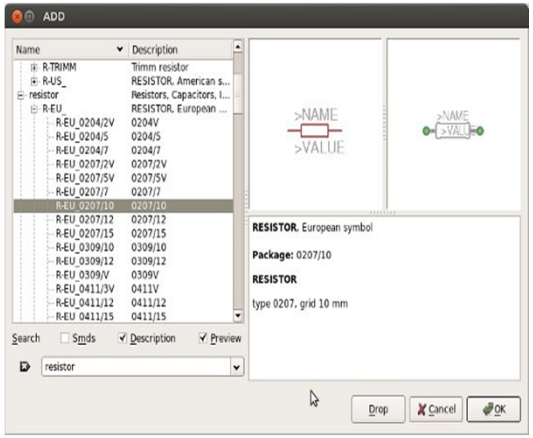
An Example of the construction of a six layer Printed Circuit Board

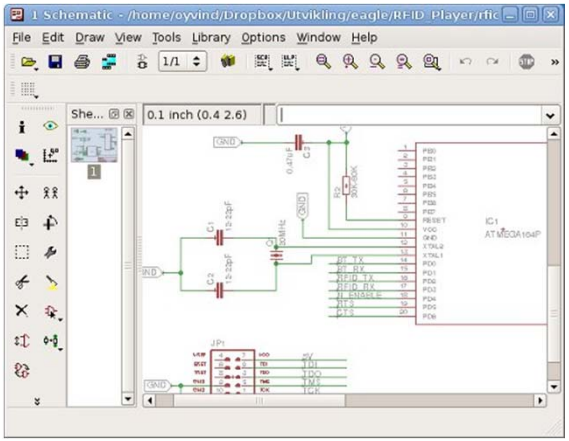
Creating a Circuit Board

1. **Start by drawing a schematic diagram with a SW tool**
   - Create a new project and schematic
   - Add components and their values
   - Add connection between components
   - Add power connection
   - Run an ERC (Electrical Rule Check)

OrCAD, EAGLE, MentoGraphics PADS,



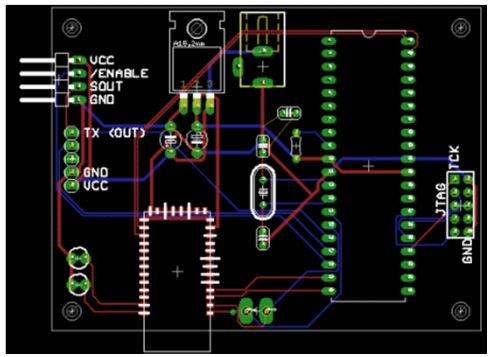




Creating a Circuit Board

2. Preparing the board layout (artwork)

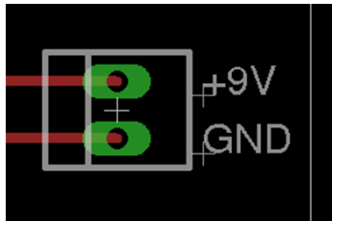
- **Transfer the schematic diagram into a drawing of printed circuit board**



❒ Guidelines

- **Board size and trace width**
- **Placement of components**
  - Connectors should be placed on the side for simple connection
  - If you are going to place the finished PCB in a box, keep in mind any large components and how they will fit in the box
- **Using labels**

Item	Specs	
	Unit: mm	Unit: mil
Available Board Thickness	0.6, 0.8, 1.0, 1.2, 1.6, 2.0	23.6, 31.5, 39.4, 47.2, 63.0, 78.7
Thickness Tolerance	(t≥1.0) ± 10%	(t≥39.4) ± 10%
Thickness Tolerance	(t<1.0) ± 0.1%	(t<39.4) ± 0.1%
Insulation Layer Thickness	0.075 — 5.00	2.95 — 196.85
Minimum trace width	0.1524	6
Minimum trace/vias/pads space	0.1524	6
Minimum silkscreen width	0.1524	6
Minimum silkscreen text size	0.8128	32
Out Layer Copper Thickness	>0.03	>1.18
Inner Layer Copper Thickness	0.01 — 0.018	0.39 — 0.71
Drilling Hole (Mechanical)	0.3 — 6.35	11.81 — 250.00
Finish Hole (Mechanical)	0.8 — 6.35	31.50 — 250.00
Diameter Tolerance (Mechanical)	±0.2	±7.87
SMT min Solder Mask Width	0.1	3.94
Min Solder Mask Clearance	0.13	5.12
Aspect Ratio	8:1	
Solder Mask Type	Photosensitive ink	



Creating a Circuit Board

❒ Guidelines (cont'd)

- **Trace angles**
  - If you are making an RF circuit board, you should avoid 90 degree angles on your PCB traces
    - ✓ Otherwise, weird effects might occur
  - 45 degree angles looks more professional

- **Visual check**
  - Print your board on paper and check it for any problems with connectors and such

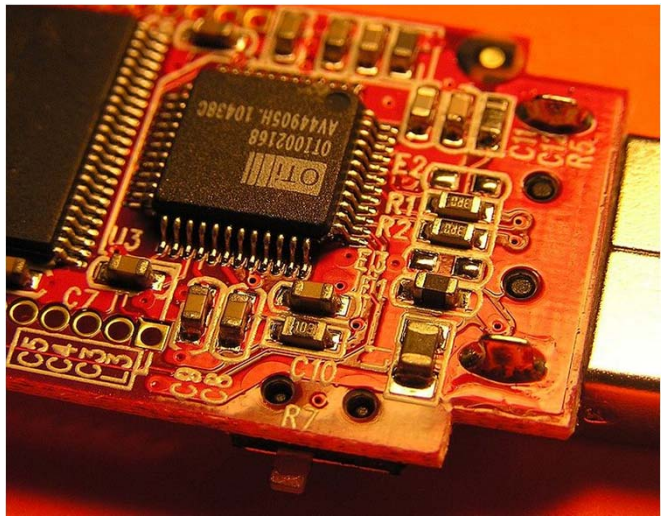
Creating a Circuit Board

3. Preparation of PCB manufacturing

- **Check the board for errors**
  - Check for unrouted nets and schematic/board layout consistency
  - Use the design rule check (DRC)
    - ✓ To make sure your drill holes, trace widths, spacings and such are within the capabilities of your PCB manufacturer
- **Create gerber files from the board layout**
  - *.cmp (Copper, component side)
  - *.drd (Drill file)
  - *.dri (Drill Station Info File) – Usually not needed
  - *.gpi (Photoplotter Info File) – Usually not needed
  - *.plc (Silk screen, component side)
  - *.pls (Silk screen, solder side)
  - *.sol (Copper, solder side)
  - *.stc (Solder stop mask, component side)
  - *.sts (Solder stop mask, solder side)
- **Choose a manufacturer**

SMT (surface mount technology)

- SMT(표면실장) is a method for producing electronic circuits in which the components are mounted or placed directly onto the surface of printed circuit boards (PCBs)



Surface mount components on
a USB flash drive's circuit board

Assembly line with
SMT placement machines

Ready made embedded boards

- PC/104 and PC/104+ are examples of standards for ready made computer boards intended for small, low-volume embedded systems, mostly x86-based
  - These are often physically small compared to a standard PC, although still quite large compared to most simple (8/16-bit) embedded systems
  - They often use DOS, Linux, NetBSD, or an embedded real-time operating system such as MicroC/OS-II, QNX or VxWorks

Ready made embedded boards

❒ Raspberry Pi

- Credit card-sized single-board computers developed in the UK by the Raspberry Pi Foundation with the intention of promoting the teaching of basic computer science in schools
- The original Raspberry Pi is based on the Broadcom BCM2835 system on a chip (SoC) which includes an ARM1176JZF-S 700 MHz processor, VideoCore IV GPU,[8] and was originally shipped with 256 megabytes of RAM, later upgraded (models B and B+) to 512 MB

Ready made embedded boards

❒ Odroid

- The Odroid is a series of single-board computers and tablet computers created by Hardkernel Co., Ltd., an open-source hardware company located in South Korea
- Even though the name ‘Odroid’ is a portmanteau of ‘open’ + ‘Android’, the hardware isn't actually open because some parts of the design are retained by the company
- Many Odroid systems are capable of running not only Android, but also Linux