Homework assignment #1

Due: **Friday, March 31, 23:59**

Total points: **100**

Questions

1. Your company is trying to choose between purchasing the Opteron or Itanium 2. You have analyzed your company's applications, and 60% of the time it will be running applications similar to **wupwise**, 20% of the time applications similar to **ammp**, and 20% of the time applications similar to **apsi**.
   (*Note that **wupwise, ammp** and **apsi** are benchmarks that included in the SPEC CPU 2000 Benchmark Suit.*)

   A. If you were choosing just based on overall SPEC performance, which would you choose and why? (**10 points**)

   B. What is the weighted average of execution time ratios for this mix of applications for the Opteron and Itanium 2? (**10 points**)

   Hint: You should identify the characteristics and performance results of wupwise, ammp and apsi first. You will also need performance details for Opteron and Itanium 2. These information are easily available through the Internet.

2. Use the following code fragment:

```
Loop:   LD      R1,0(R2)    ;load R1 from address 0+R2
        DADDI   R1,R1,#1    ;R1=R1+1
        SD      R1,0,(R2)   ;store R1 at address 0+R2
        DADDI   R2,R2,#4    ;R2=R2+4
        DSUB    R4,R3,R2    ;R4=R3-R2
        BNEZ    R4,Loop     ;branch to Loop if R4!=0
```

   Assume that the initial value of R3 is R2 + 396.

   A. Data hazards are caused by data dependences in the code. Whether a dependency causes a hazard depends on the machine implementation (i.e., number of pipeline stages). **List all of the data dependences in the code above.** Record the register, source instruction, and destination instruction; for example, there is a data dependency for register **R1** from the **LD** to the **DADDI**. (**20 points**)

   B. Show the timing of this instruction sequence for the 5-stage RISC pipeline without any forwarding or bypassing hardware but assuming that a register read and a write in the same clock cycle "forwards" through the register file, as shown in **Figure C.6**. Use a pipeline timing chart like that in **Figure C.5**. Assume that the branch is handled by flushing the pipeline. If all memory references take 1 cycle, how many cycles does this loop take to execute? (**20 points**)
   (*Figure C.6 and Figure C.5 are given in the next page. You can also refer to Appendix C-15 and C-17 in the textbook.*)

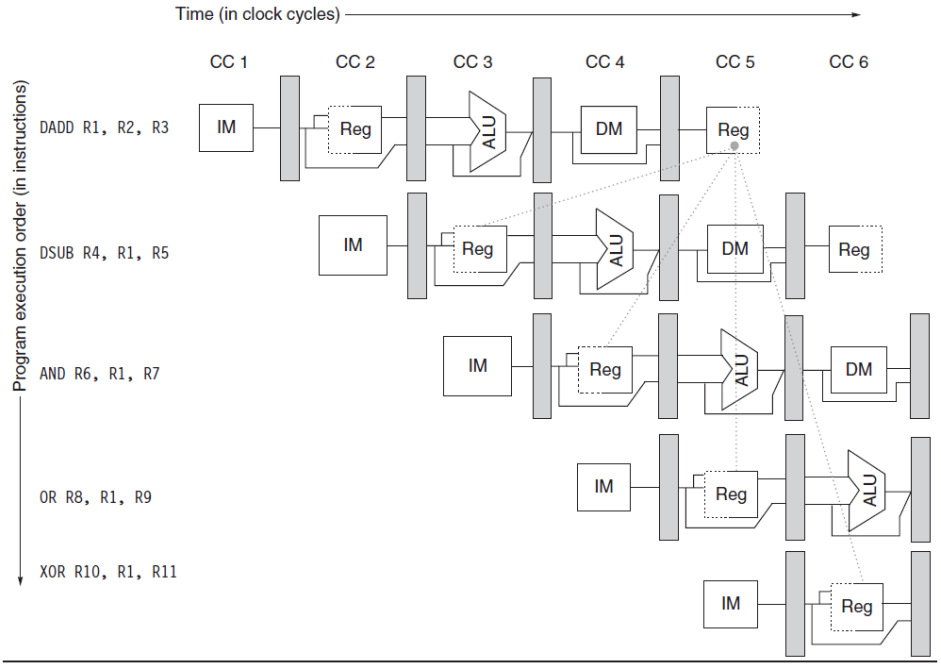

Figure C.6 The use of the result of the DADD instruction in the next three instructions causes a hazard, since the register is not written until after those instructions read it.

	Clock cycle number									
Instruction	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
Load instruction	IF	ID	EX	MEM	WB					
Instruction $i + 1$		IF	ID	EX	MEM	WB				
Instruction $i + 2$			IF	ID	EX	MEM	WB			
Instruction $i + 3$				Stall	IF	ID	EX	MEM	WB	
Instruction $i + 4$						IF	ID	EX	MEM	WB
Instruction $i + 5$							IF	ID	EX	MEM
Instruction $i + 6$								IF	ID	EX

Figure C.5 A pipeline stalled for a structural hazard—a load with one memory port. As shown here, the load instruction effectively steals an instruction-fetch cycle, causing the pipeline to stall—no instruction is initiated on clock cycle 4 (which normally would initiate instruction $i + 3$). Because the instruction being fetched is stalled, all other instructions in the pipeline before the stalled instruction can proceed normally. The stall cycle will continue to pass through the pipeline, so that no instruction completes on clock cycle 8. Sometimes these pipeline diagrams are drawn with the stall occupying an entire horizontal row and instruction 3 being moved to the next row; in either case, the effect is the same, since instruction $i + 3$ does not begin execution until cycle 5. We use the form above, since it takes less space in the figure. Note that this figure assumes that instructions $i + 1$ and $i + 2$ are not memory references.

3. Suppose the branch frequencies (as percentages of all instructions) are as follows:

Conditional branches	15%
Jumps and calls	1%
Taken conditional branches	60% are taken

A. We are examining a four-deep pipeline where the branch is resolved at the end of the second cycle for unconditional branches and at the end of the third cycle for conditional branches. Assuming that only the first pipe stage can always be done independent of whether the branch goes and ignoring other pipeline stalls, how much faster would the machine be without any branch hazards? (**20 points**)

B. Now assume a high-performance processor in which we have a 15-deep pipeline where the branch is resolved at the end of the fifth cycle for unconditional branches and at the end of the tenth cycle for conditional branches. Assuming that only the first pipe stage can always be done independent of whether the branch goes and ignoring other pipeline stalls, how much faster would the machine be without any branch hazards? (**20 points**)

Grading

1. You will be given 0 point for any kind of cheating.
2. Please give detailed process that how you solved it. Otherwise, no points will be charged.

Submission

1. Submit your homework (hardcopy) into HW box prepared near room #922 in N1 building.
2. Late submissions will not be accepted. Please keep the submission deadline.

If you have questions about this homework assignment, please send email to TA

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