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# E1. Introduction to OrCAD and PSpice

# OrCAD and PSpice

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PSpice is a SPICE analog circuit and digital logic simulation program for Microsoft Windows. The name is an acronym for **Personal Simulation Program with Integrated Circuit Emphasis**.

<http://en.wikipedia.org/wiki/PSPICE>

# OrCAD and PSpice

The screenshot shows a Windows Internet Explorer browser window displaying the Cadence OrCAD Solutions website. The address bar shows the URL <http://www.cadence.com/products/orcad/pages/default.aspx>. The browser's menu bar includes options like '파일(F)', '편집(E)', '보기(V)', '즐거찾기(A)', '도구(T)', and '도움말(H)'. The website header features the Cadence logo, navigation links (Solutions, Products, Services, Support & Training, Alliances, Community, About Cadence), and a search bar. The main content area is titled 'Cadence OrCAD Solutions' and features a large orange banner for 'OrCAD 16.6—New Signal Integrity Flow, Advances in Simulation, and Extended Tcl Programming'. Below the banner, there are sections for 'New OrCAD Capture Marketplace' and 'OrCAD Quicklinks'. A sidebar on the right contains 'Highlights' and 'Recent Blog Posts'. The status bar at the bottom shows the URL <http://www.cadence.com/products> and the page zoom level at 105%.

**Cadence OrCAD Solutions**

OrCAD 16.6—New Signal Integrity Flow, Advances in Simulation, and Extended Tcl Programming

OrCAD 16.6—Find out what's new

**New OrCAD Capture Marketplace**

Josh Moore, Senior Product Manager for OrCAD, shares how the new OrCAD Capture Marketplace – with online apps – transforms the way PCB designers access information, discover new resources and extend the OrCAD environment.

**OrCAD Quicklinks**

- Why Cadence OrCAD for PCB?
- Design Suites Datasheet
- Software downloads

**Highlights**

- Webinar: PCB Library Development – Build OrCAD Symbols and IPC-7351 compliant footprints in a fraction of the time with EDABuilder
- Allegro and OrCAD Users Day at CDNLive! Silicon Valley
- What's Good About OrCAD Apps? You Can Try Them for Free!
- FPGA-PCB codesign; a 21st Century approach to integrating fpgas into the pcb design process

**Recent Blog Posts**

- What's Good About Allegro PCB Editor Place Replicate Text Support? Check Out 16.6!
- What's Good About Allegro AMS

# OrCAD and PSpice

## Products



### OrCAD FPGA System Planner new

Provides a complete, scalable solution for FPGA-PCB co-design that allows users to create an optimum correct-by-construction pin assignment.

[Read more »](#)



### OrCAD Capture and Capture CIS

Offers full-featured schematic editing for fast, intuitive design capture with hierarchical and variant capabilities. Component information system (CIS) promotes use of preferred, current parts to accelerate the design process and reduce project costs.

[Read more »](#)



### OrCAD PCB Designer

Offers a proven, scalable, easy-to-use PCB editing and routing solution. Delivers a comprehensive feature set and seamless PCB design environment to take designs from concept to production.

[Read more »](#)



### ActiveParts Portal new

Automates the process of part selection and extends the reach of engineers. APP is FREE for users on the most current releases of OrCAD Capture CIS

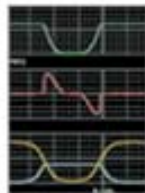
[Read more »](#)



### OrCAD Signal Explorer

Enables pre- and post-layout signal integrity analysis and topology design/exploration at any stage of the design cycle improving circuit reliability and performance to reduce prototypes and re-spins.

[Read more »](#)



### PSpice A/D and Advanced Analysis

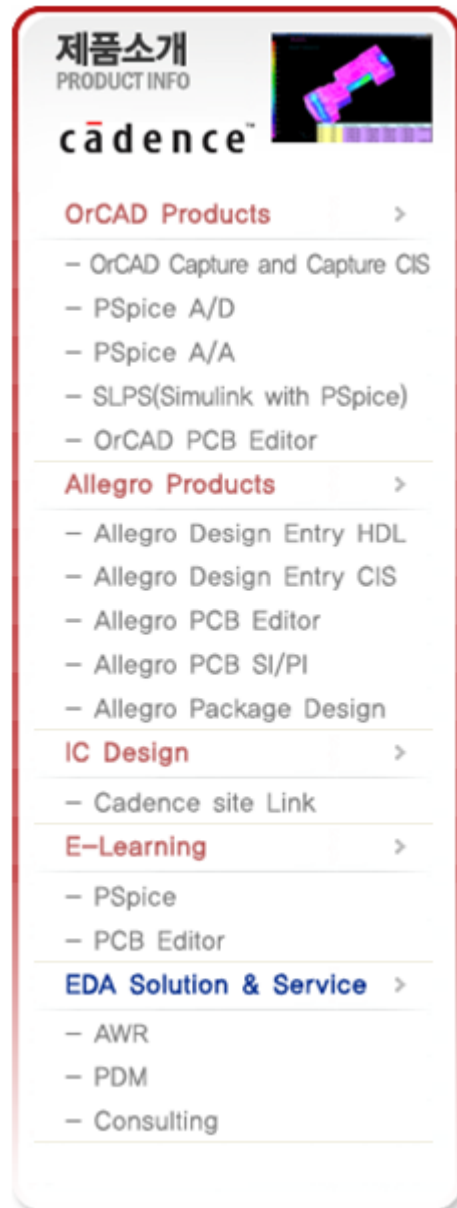
Provides simulation of analog/mixed-signal circuits as well as analysis for by determining which components are over-stressed and component yields. Full integration with OrCAD Capture improves productivity and data integrity.

[Read more »](#)

<http://www.cadence.com/products/orcad/Pages/default.aspx>

# OrCAD and PSpice

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[http://npeda.co.kr/jsp/layout/MainLayout.jsp?callType=JSP&menuId=product&callJsp=/jsp/product/orcad\\_02.jsp](http://npeda.co.kr/jsp/layout/MainLayout.jsp?callType=JSP&menuId=product&callJsp=/jsp/product/orcad_02.jsp)

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<http://web.yonsei.ac.kr/hgijung>

# OrCAD and PSpice

Cadence OrCAD Capture / Capture CIS  
Allegro Design Entry CIS

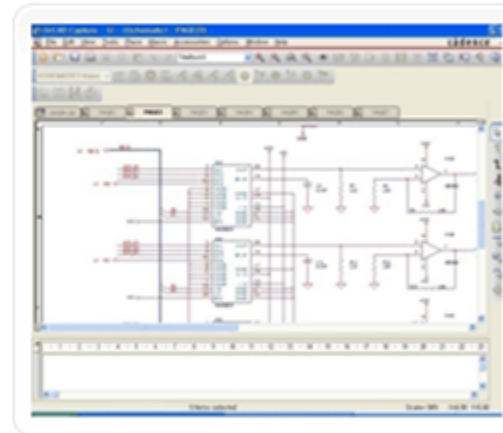
## Cadence OrCAD Capture and Capture CIS

An industry standard in schematic design entry

**OrCAD Capture design entry**는 오늘날 전자회로 설계분야에서 가장 보편적으로 사용되는 빠르고 강력한 업계 표준의 범용 회로설계편집 도구입니다. 통합 환경에 의해 일반적인 회로도 입력은 물론 Block Diagram, 복잡한 PCB Block PCB, FPGA, CPLD등의 설계 대상에 관계없이 입력 Tool로 사용할 수 있으며 빠르고 편리한 User Interface를 제공합니다.

시스템 설계자가 새로운 아날로그 회로를 설계하거나, 기존의 PCB의 회로도면을 재구성 또는 HDL 모듈로 디지털 회로를 구성하고자 할 때, OrCAD Capture는 이러한 입력, 수정 및 검증 작업을 위한 완벽한 작업환경을 제공합니다.

OrCAD Capture CIS (Component Information System)는 최신버전의 Capture에 Part List 작성기능, 대화 형식의 부품정보 시스템을 통합한 것으로 Capture의 설계도면을 벗어나지 않고, 부품 데이터베이스나 인터넷상의 온라인 부품데이터에 접속하여 선택한 부품의 제조 관련 데이터를 검색하고 도면에 등록시킬 수 있습니다. 부정확한 부품데이터의 사용으로 인한 보드의 재작업을 줄일 수 있으며, 부품의 재고 부족으로 인한 제품의 출시 지연을 줄일 수 있어 예상보다 높은 부품비용의 발생을 막을 수 있습니다.



mail: [hogijung@hanyang.ac.kr](mailto:hogijung@hanyang.ac.kr)  
<http://web.yonsei.ac.kr/hgijung>

# OrCAD and PSpice

## CADENCE PSpice A/D

### Advanced simulation for analog & mixed-signal environments

**PSpice**는 정확한 아날로그 및 아날로그-디지털 혼재회로 시뮬레이션의 산업표준 솔루션을 제공하며, **PSpice A/D**는 최적의 기능을 갖춘 고유의 **아날로그-디지털 혼재회로 시뮬레이터**입니다. 엔지니어들은 실제로 보드를 설계하기 전에 다양한 시뮬레이션을 통해 설계된 회로에 대한 검증을 할 수 있게 지원하며, 개선된 Model Editor, Magnetic Part Editor, Stimulus Editor 기능은 라이브러리를 사용자가 원하는 형태로 수정, 편집 및 생성 할 수 있습니다.

#### Bias Point Analysis

- 아날로그 노드의 전압 리스트
- 디지털 노드의 상태 리스트
- Device의 small signal parameter 리스트를 output file에 출력
- 비선형 제어전원이나 반도체 소자의 상세한 바이어스 포인트 결과 출력
- 민감도 해석 수행
- 입출력에 대한 전달함수 계산

#### Transient Analysis

- 시간 영역에서 입력 신호에 대한 출력을 결정
- Fourier 해석 수행 데이터를 푸리에 적분하여 결과를 출력
- Fourier 해석 수행 시 크기, 위상, 직류분 등에 대한 결과를 출력하므로 평균치, 기본파 실효치, 역률, THD 등을 계산

#### DC Sweep

- 특정 전압/전류의 값을 가변시켜 출력 결과 확인
- 특정 레벨 이상의 직류 입력에 의한 스위칭 특성을 확인할 때 사용

#### AC Sweep

- 입력 주파수를 가변시켜 회로시스템에 대한 주파수 응답을 계산
- 시스템 보드선도, 임피던스 해석 수행
- 등가 노이즈원을 이용하여 노이즈를 입력하고 출력되는 노이즈량을 해석

#### Parametric Sweep

- Transient Analysis, DC Sweep, AC Sweep에서 Parametric Sweep 기능 제공
- Global Parameter를 이용하여 회로내 소자 값을 임의로 변경하며 계산을 수행
- Parametric 해석 수행 후 특성평가의 편의를 위해 Goal Function 제공



# OrCAD and PSpice

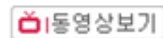
## CADENCE PSpice A/A

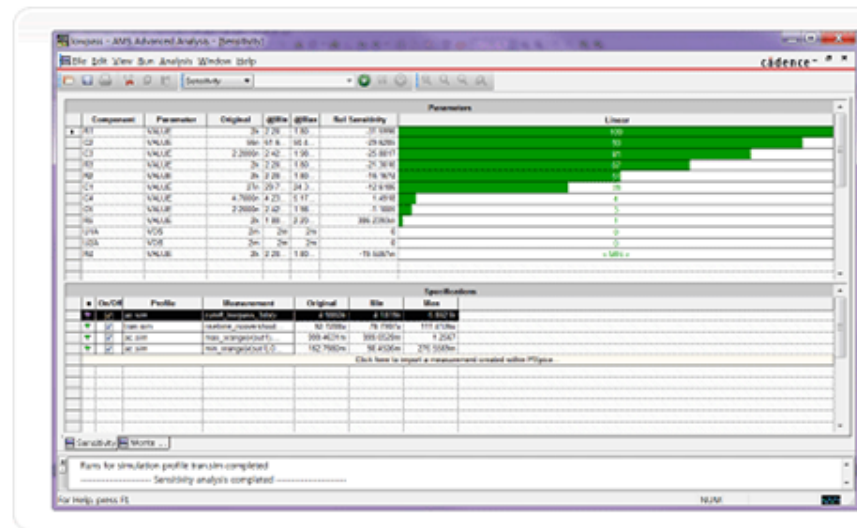
**PSpice Advanced Analysis (AA)**는 PSpice A/D 와 연동하여 성능, 생산성 및 신뢰성을 향상시킬 수 있는 강력한 툴입니다.

 Download Datasheet >>

### Sensitivity Analysis

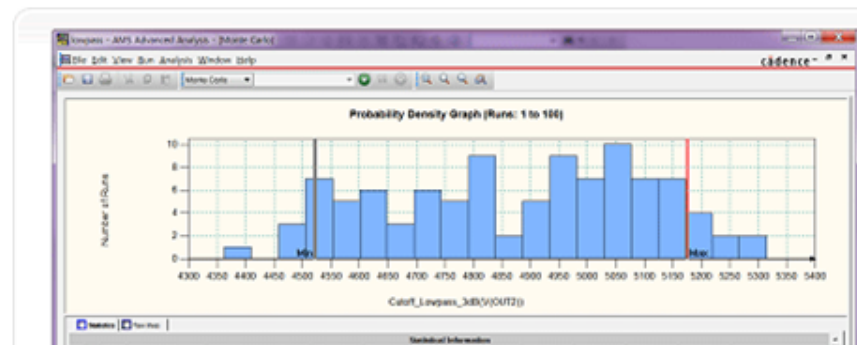
- 각각의 Measurement에 대한 소자의 허용오차 값에 의한 특성변화를 측정하여 각 소자별로 회로 내에 미치는 영향을 표현

 동영상보기



### Monte Carlo Analysis

- 회로 내 소자의 오차로 인한 특성변화 확인
- 회로 특성 분포를 사용자가 설정하여 만족하는지의 판별 가능
- Margin의 만족여부(Yield) 및 누적 분포 그래프를 이용하여 회로 특성 분석 가능
- 확률 분포함수 및 누적 분포함수





# OrCAD and PSpice

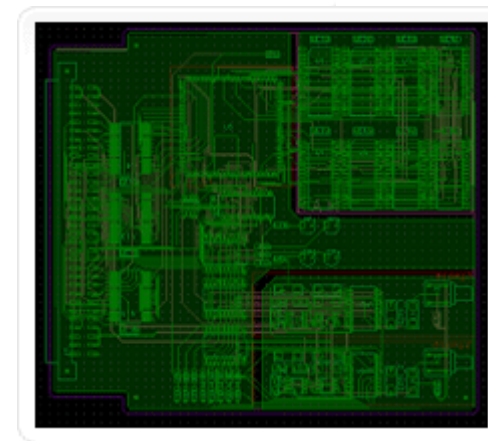
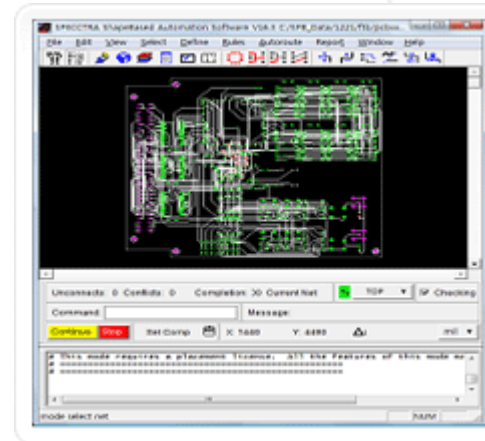
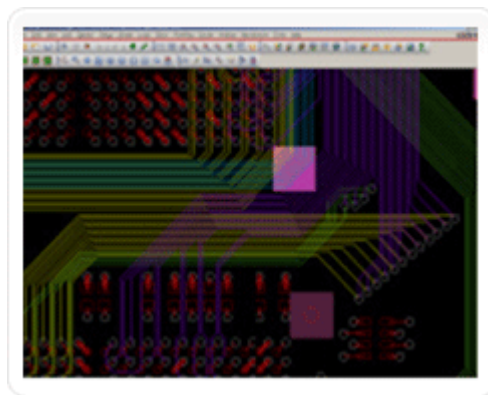
## OrCAD PCB Editor

### Cadence OrCAD PCB Editor

Proven, easy-to-use PCB place-and-route technology

**OrCAD PCB Editor Suites** 복잡한 고밀도 PCB의 설계에 적합한 강력한 PCB 설계도구입니다.

OrCAD PCB Editor는 기존 OrCAD Series의 Capture, SPECCTRA, PSpice A/D와의 완벽한 연동성과, Cadence Allegro PCB Editor로부터 이어받은 강력한 기능으로 PCB 생산성 향상과 Design Quality에 크게 기여할 것입니다.



# OrCAD and PSpice

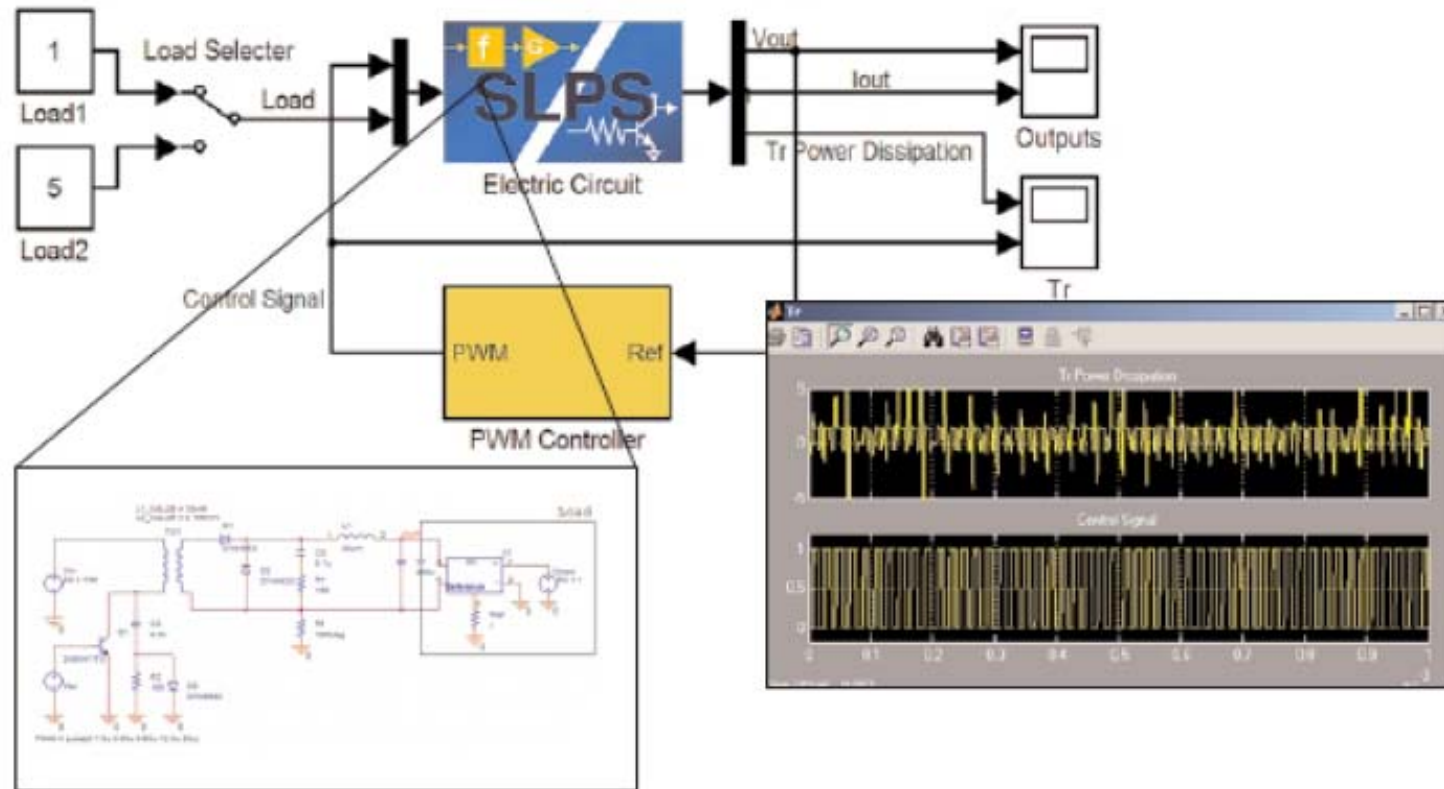


Figure 6: SLPS enables designers of electro-mechanical systems—such as control blocks, sensors, and power converters—to perform integrated system and circuit simulation

# OrCAD and PSpice

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## OrCAD Downloads

**Note:** To download the files we recommend using the [Internet Explorer](#) or [Firefox](#) web browsers.  
All OrCAD downloads require a valid email address.

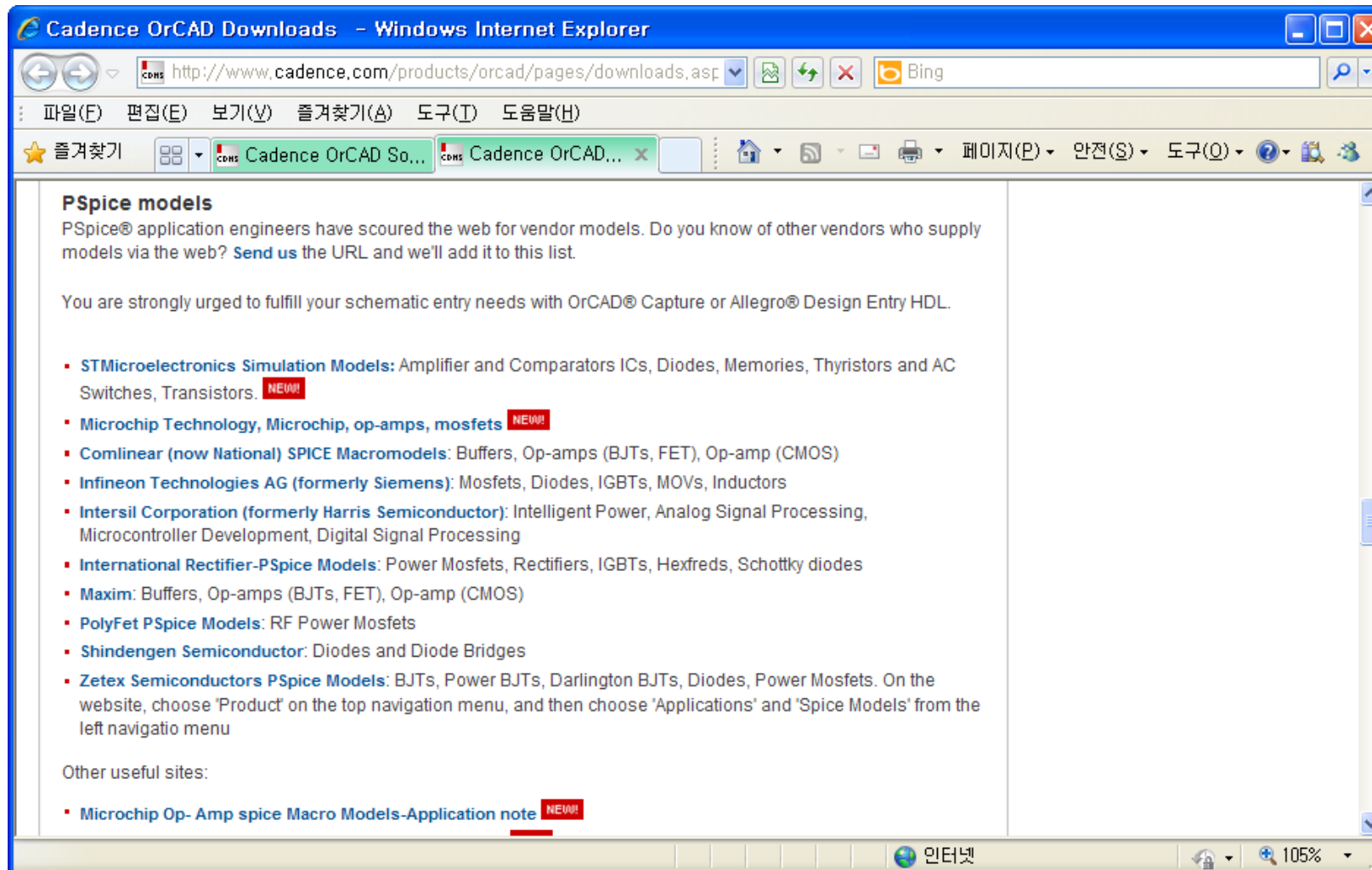
### High-speed PCB layout, routing, and manufacturing output

The latest product downloads are available free to all registered Cadence® customers. In some cases, you'll be asked to complete a brief user profile. All information supplied is used only to help us develop future products and technology.

- [OrCAD PCB Designer Lite DVD \(All Products\)](#)
- [OrCAD PCB Designer Lite DVD \(Capture & PSpice only\)](#)
- [CIS Admin Tool 10.x](#)
- [CIS Admin Tool 16.2](#)
- [OrCAD Capture/OrCAD Capture CIS ViewReader](#)
- [OrCAD CIS Wizard](#)
- [PSpice Schematics Installer](#)
- [Third-party translator](#)
- [PSpice models](#)
- [Allegro/OrCAD Starter Library](#)

<http://www.cadence.com/products/orcad/pages/downloads.aspx>

# OrCAD and PSpice



<http://www.cadence.com/products/orcad/pages/downloads.aspx>

# OrCAD and PSpice

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## Korea

NewLink Technology  
UnionCenter #1009, 837-11, Yeoksam-1dong, Gangnam-gu,  
Seoul, 135-754  
Phone: 82-70.7138.1231  
Fax: 82-505.827.1231  
Email: [jhchoi@newlinktek.com](mailto:jhchoi@newlinktek.com)  
Web site: [www.newlinktek.com](http://www.newlinktek.com)

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NINEPLUS EDA  
1502ho, Ace High-end Tower 8 Cha, 345-4, Gasan-dong, Geumcheon-gu, Seoul, 153-802  
Phone: 82.2.6123.3355  
Fax: 82.2.6123.3350  
Email: [sjkim@npeda.co.kr](mailto:sjkim@npeda.co.kr)  
Web site: [www.npeda.co.kr](http://www.npeda.co.kr)

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AceHitech 21-1410, 1470, U-dong, Haeundae-gu,  
Busan, 612-020  
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Fax: 82.51.758.4866  
Email: [sjkim@npeda.co.kr](mailto:sjkim@npeda.co.kr)  
Web site: [www.npeda.co.kr](http://www.npeda.co.kr)

## Korea

VT Korea  
Duksan B/D 3F  
114 Yangjae-dong, Seocho-gu  
Seoul, 137-130  
Phone: 82.2.2057.8815  
Fax: 82.2.2057.8810  
Email: [jhkim@veritytech.co.kr](mailto:jhkim@veritytech.co.kr)  
Web site: [www.veritytech.co.kr](http://www.veritytech.co.kr)  
Serves Korea.

[http://www.cadence.com/alliances/channel\\_partner/pages/default.aspx](http://www.cadence.com/alliances/channel_partner/pages/default.aspx)

# OrCAD 16.6 Lite Program

The screenshot shows the npeda.co.kr website in Internet Explorer. The browser title is "Cadence Channel Partner 나인플러스EDA(주) :: - Windows Internet Explorer". The address bar shows "http://npeda.co.kr/index.action". The website header includes "Electronic Design Automation Technology & Engineering Service Leader" and navigation links like HOME, 로그인, SITE MAP, and CONTACT US. A red banner at the top lists categories: 제품소개, 고객지원, 견적/제품문의, University Program, 교육/세미나/이벤트, 커뮤니티, and 회사소개. The main content area features a large banner for "OrCAD 16.6 RELEASE" with a "자세히보기" button. Below this is a "고객지원 CS CENTER" section with a "내용더보기" button. On the left, there's a "멤버로그인 / MEMBER LOGIN" section and an "교육일정 EDUCATION CALENDAR" for March 2013. The bottom section lists "최근게시물" (Recent Posts) and "교육세미나이벤트" (Education Seminar Events).

**교육일정 EDUCATION CALENDAR**

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						1
3	4	5	6	7	8	9
10	11	12	13	14	15	16
17	18	19	20	21	22	23
24	25	26	27	28	29	30
31						

\* 녹색 날짜를 클릭하시면 교육및 행사 일정이 표시됩니다.

> 방문자수 106,787

**최근게시물**

- OrCAD 16.6 Lite Program (All P..
- OrCAD 16.6 Lite Program (Captu..
- SPB 16.6 Hotfix\_004
- OrCAD & Allegro (SPB) v16.6 설치 ..
- 라이선스 매니저 v12.01

**교육세미나이벤트**

교육	제목	날짜
교육	Virtuoso Schematic..	13.03.27~13.03.29
교육	PCB 설계기초	13.03.27~13.03.29
교육	Cadence Virtuoso S..	13.03.25~13.03.26
교육	Allegro PCB Atwork..	13.03.20~13.03.22
교육	OrCAD 기본	13.03.19~13.03.22

<http://npeda.co.kr/index.action>



# OrCAD 16.6 Lite Program

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106,783

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교육세미나이벤트

DEMO OrCAD 16.6 Lite Program (All P..

DEMO OrCAD 16.6 Lite Program (Captu..

PATCH SPB 16.6 Hotfix\_004

INSTALL OrCAD & Allegro(SPB) v16.6 설치 ..

LICENSE 라이선스 매니저 v12.01

LIBRARY OrCAD PCB Editor 라이브러리 v16.3, ..

INSTALL Allegro Free viewer v16.5

DEMO OrCAD 16.5 Lite Program (Captu..

DEMO OrCAD 16.5 Lite Program (All P..

INSTALL OrCAD & Allegro(SPB) v16.5 설치 ..

교육 Virtuoso Schematic..

교육 PCB 설계기초 NEW

교육 Cadence Virtuoso S..

교육 Allegro PCB Atwork..

교육 [노동부] OrCAD 기본

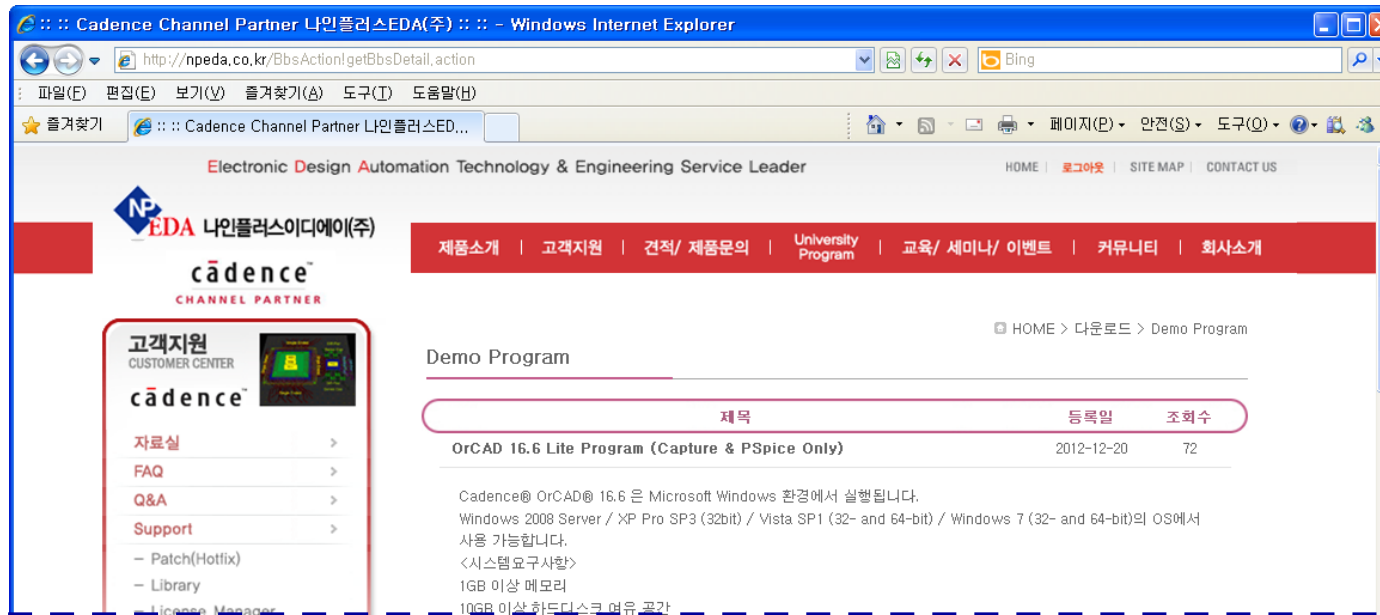
교육 OrCAD PSpice A/D

OrCAD 16.6 Lite Program (Capture & Pspice Only)

<http://npeda.co.kr/index.action>



# OrCAD 16.6 Lite Program



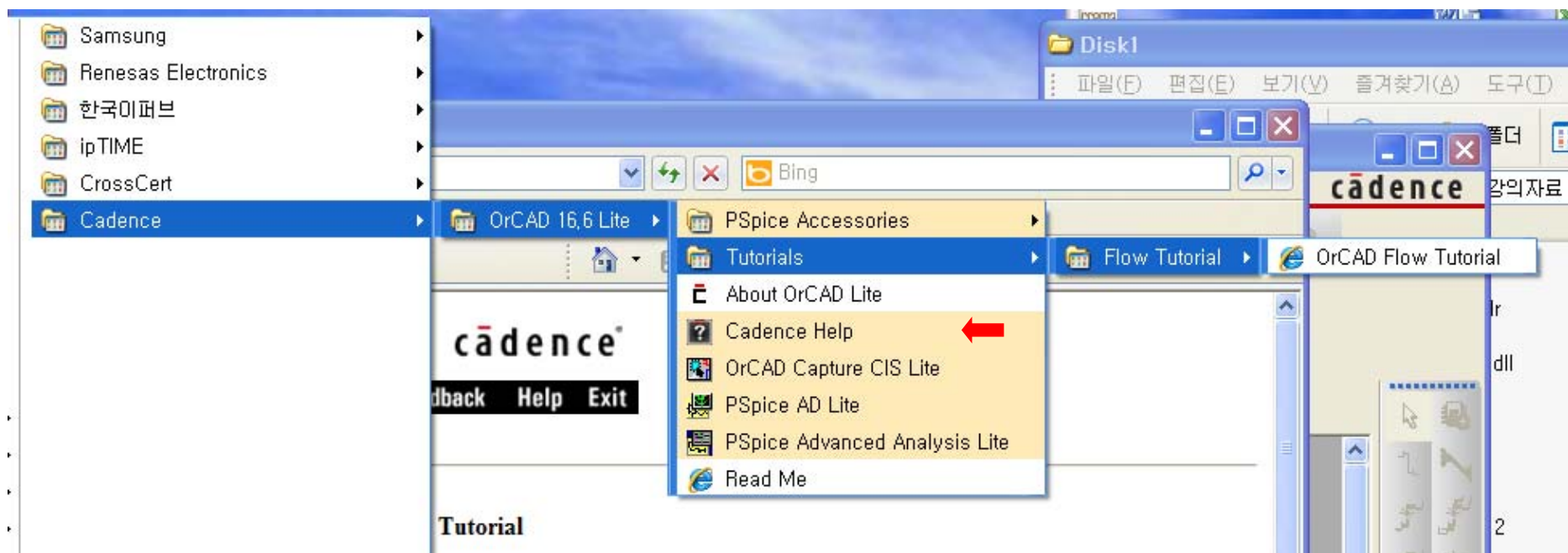
- Sensitivity Analysis
  - ☐ Only one measurement specification is allowed.
  - ☐ A maximum of three devices with tolerance are supported.
  - ☐ Maximum of 20 runs are supported.
- Encrypted parameterized models cannot be simulated.
- The Optimizer Random Engine can make a maximum of 5 runs.

다운로드

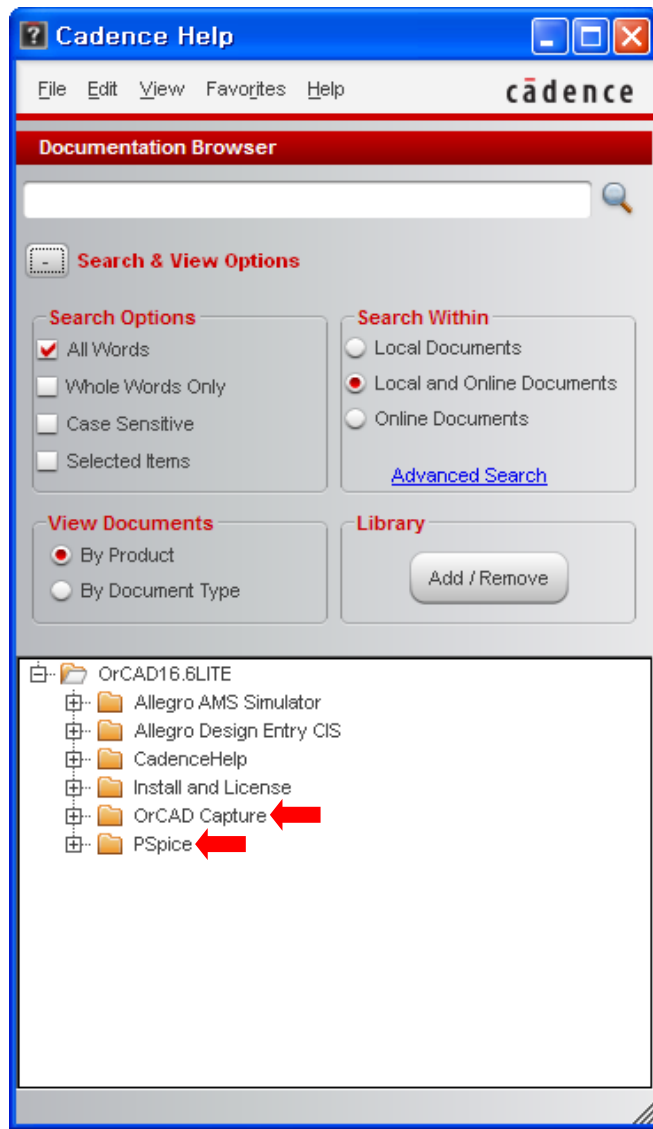
(위 파일은 Zip파일로 압축되어 있습니다. 임의의 폴더에 압축을 푸신 다음 실행하시면 됩니다.)  
(해당 자료에 대하여 링크하거나 재배포 행위를 금합니다.)

<http://npeda.co.kr/BbsAction!getBbsDetail.action>

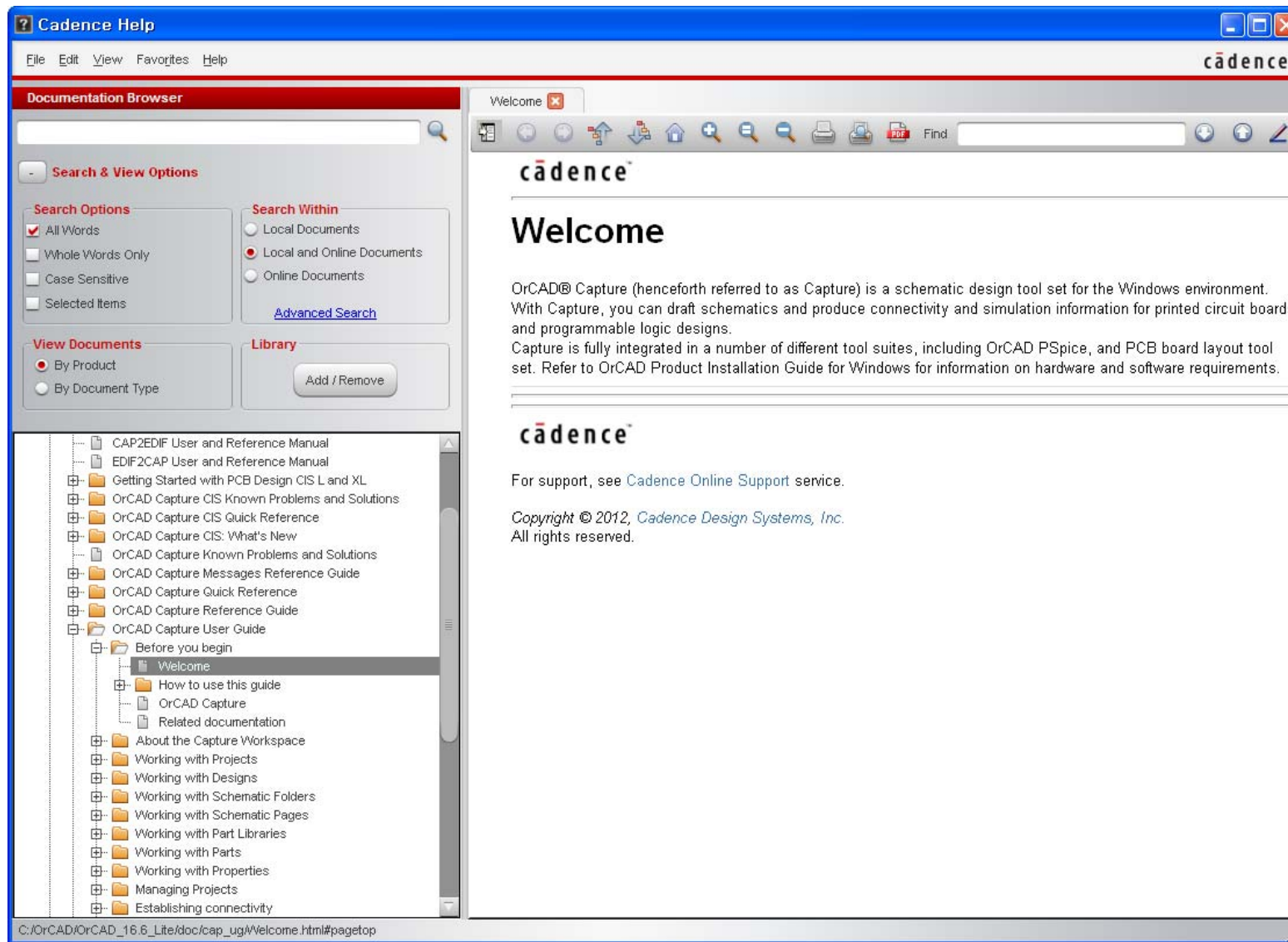
# OrCAD 16.6 Lite Program



# OrCAD 16.6 Lite Program



# OrCAD 16.6 Lite Program



# OrCAD 16.6 Lite Program

**Cadence Help**

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**Documentation Browser**

Search & View Options

**Search Options**

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- ☐ Whole Words Only
- ☐ Case Sensitive
- ☐ Selected Items

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- ☒ Local and Online Documents
- ☐ Online Documents

[Advanced Search](#)

**View Documents**

- ☒ By Product
- ☐ By Document Type

**Library**

Add / Remove

PSpice Known Problems and Solutions

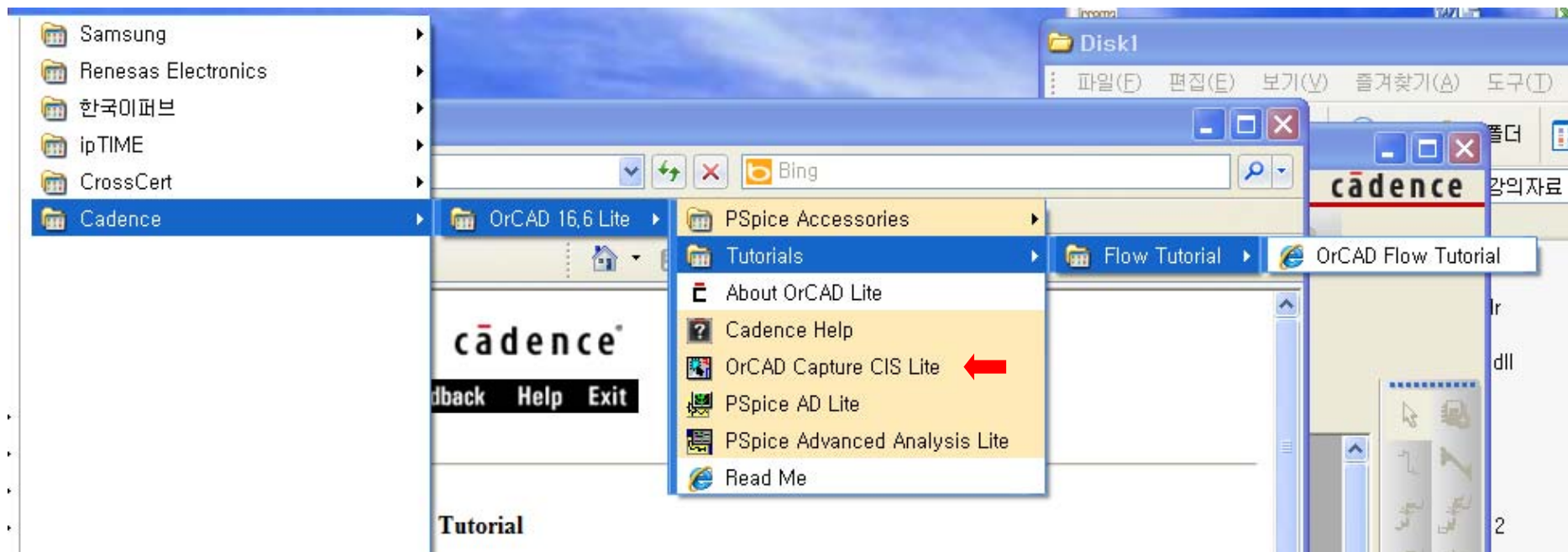
- PSpice Library List
- PSpice Library Models Data Book
- PSpice Quick Reference
- PSpice Reference Guide
- PSpice User Guide
- Before you begin
  - Part one: Simulation primer
  - Things you need to know
  - Simulation examples
    - Chapter overview
    - Example circuit creation
      - Using Capture**
      - Using Design Entry HDL
      - Using Design Templates
      - Finding out more about setting up your des...
- Running PSpice
  - DC sweep analysis
  - Transient analysis
  - AC sweep analysis
  - Parametric analysis
  - Performance analysis
- Part two: Design entry
  - Preparing a design for simulation
  - Creating and editing models
  - Creating parts for models

**Using Capture**

This section describes how to use OrCAD Capture to create the simple diode clipper circuit shown in Figure 2-1.

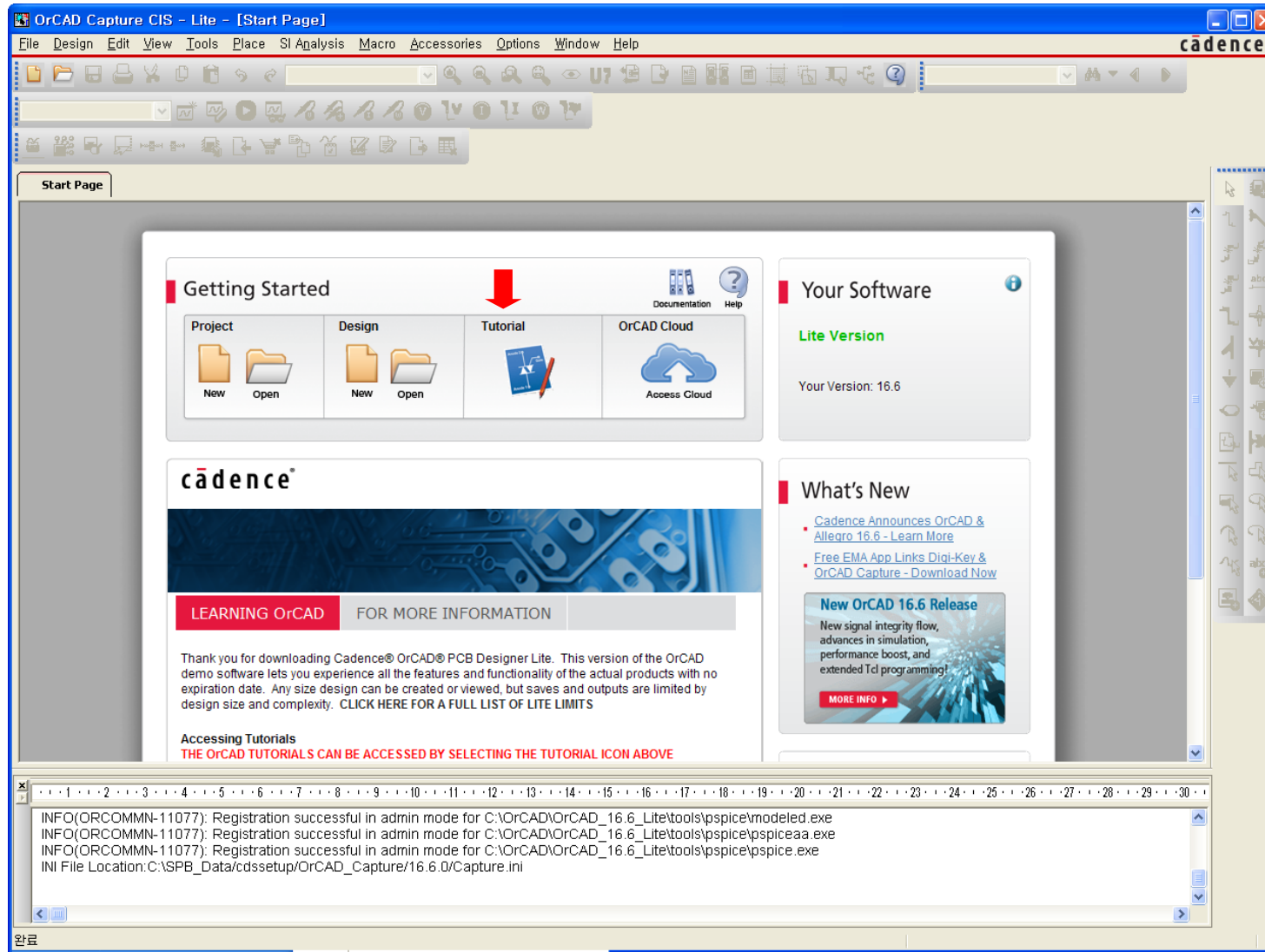
**Figure 2-1 Diode clipper circuit.**

# OrCAD 16.6 Lite Program



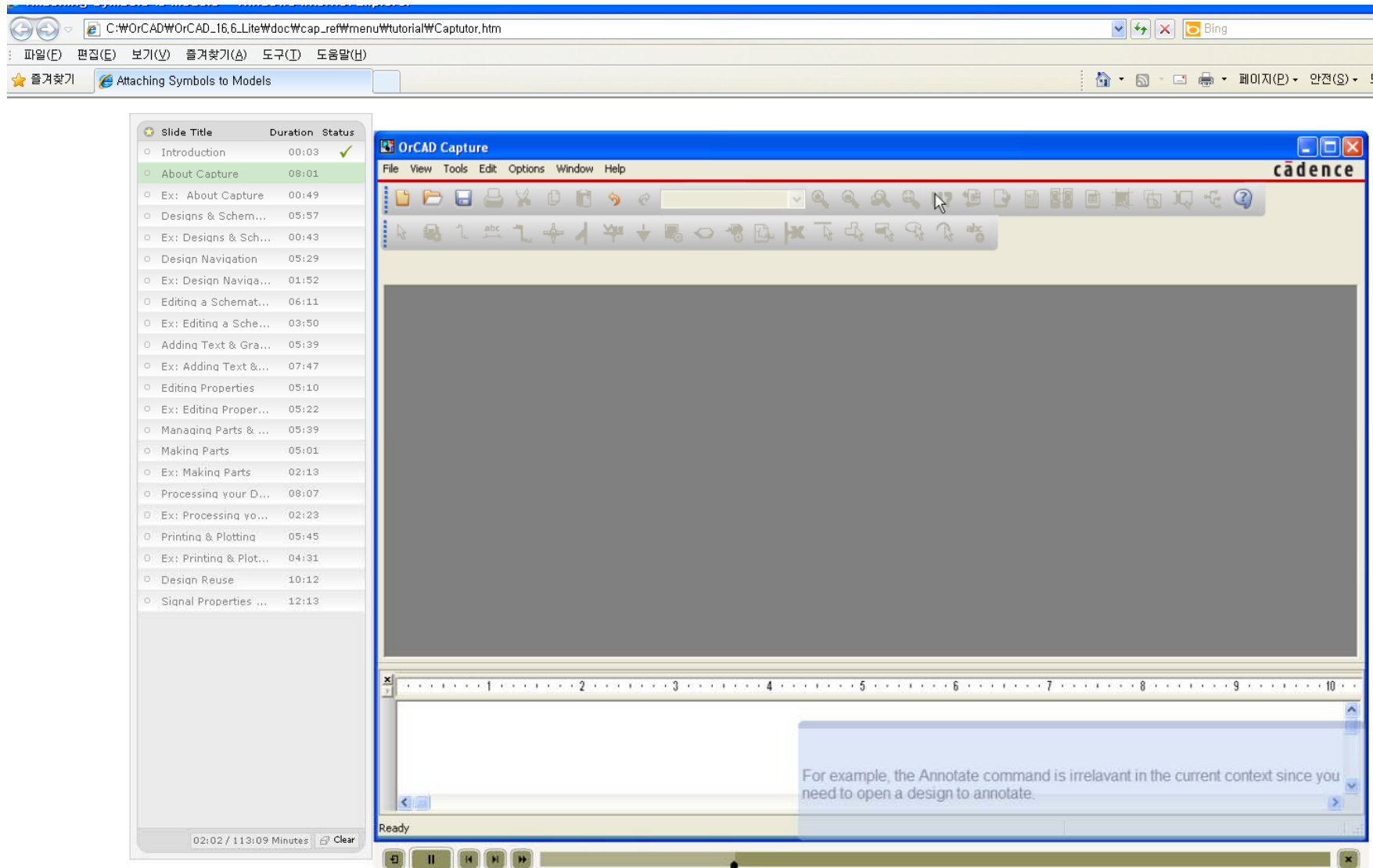


# OrCAD 16.6 Lite Program





# OrCAD 16.6 Lite Program



# OrCAD 16.6 Lite Program

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Cadence® OrCAD® 16.6 은 Microsoft Windows 환경에서 실행됩니다.

Windows 2008 Server / XP Pro SP3 (32bit) / Vista SP1 (32- and 64-bit) / Windows 7 (32- and 64-bit)의 OS에서 사용 가능합니다.

## <시스템요구사항>

1GB 이상 메모리

10GB 이상 하드디스크 여유 공간

300MB 이상 가상메모리

CD-ROM/ 드라이브

해상도 1024 x 768 이상의 64,000 컬러 윈도우 디스플레이 ( 1280 x 1024 권장 )

OrCAD PCB Editor는 그래픽 카드가 OpenGL 지원해야 함

# OrCAD 16.6 Lite Program

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## OrCAD Capture CIS Lite

- You cannot save designs that have more than **75 nets**, including the hierarchical blocks in the design. You can still view or create larger designs.
- You cannot save a design with more than **60 parts**, including the hierarchical blocks in the design. You can still view or create larger designs.
- You cannot have more than **1000 parts in the Capture CIS database**.
- The Internet Component Assistant (ICA) tab in the CIS Explorer window opens the About ActiveParts page ([www.activeparts.com](http://www.activeparts.com)) and not the component search page.
- You cannot create parts with more than 100 pins.
- The Capture FPGA flow is not available.
- You cannot validate Electrical Csets

# OrCAD 16.6 Lite Program

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## PSpice A/D Lite

- Circuit simulation limited to circuits with up to **75 nodes**, **20 transistors**, no sub-circuit limits but 65 digital primitive devices, and 10 transmission lines (ideal or non-ideal) with not more than four pairwise coupled lines.

- **Device characterization and parameterized part creation using the PSpice Model Editor limited to diodes.**

- No limit to stimulus generation using Stimulus Editor.

- Sample model library named eval.lib (containing analog and digital parts) and evalp.lib (containing parameterized parts) are provided.

- The library nomd.lib is configured for simulations. The nomd.lib file references the set of libraries that can be used with the lite version.

- You cannot simulate parameterized parts that are not from the evalp.lib library. This library consists of parametrized resistor, source, and diode.

- You cannot use Level 3 of Core model (Tabrizi), MOSFET BSIM 3.2, or MOSFET BSIM 4 models.

- Displays only simulation data created using the lite version of the simulator.

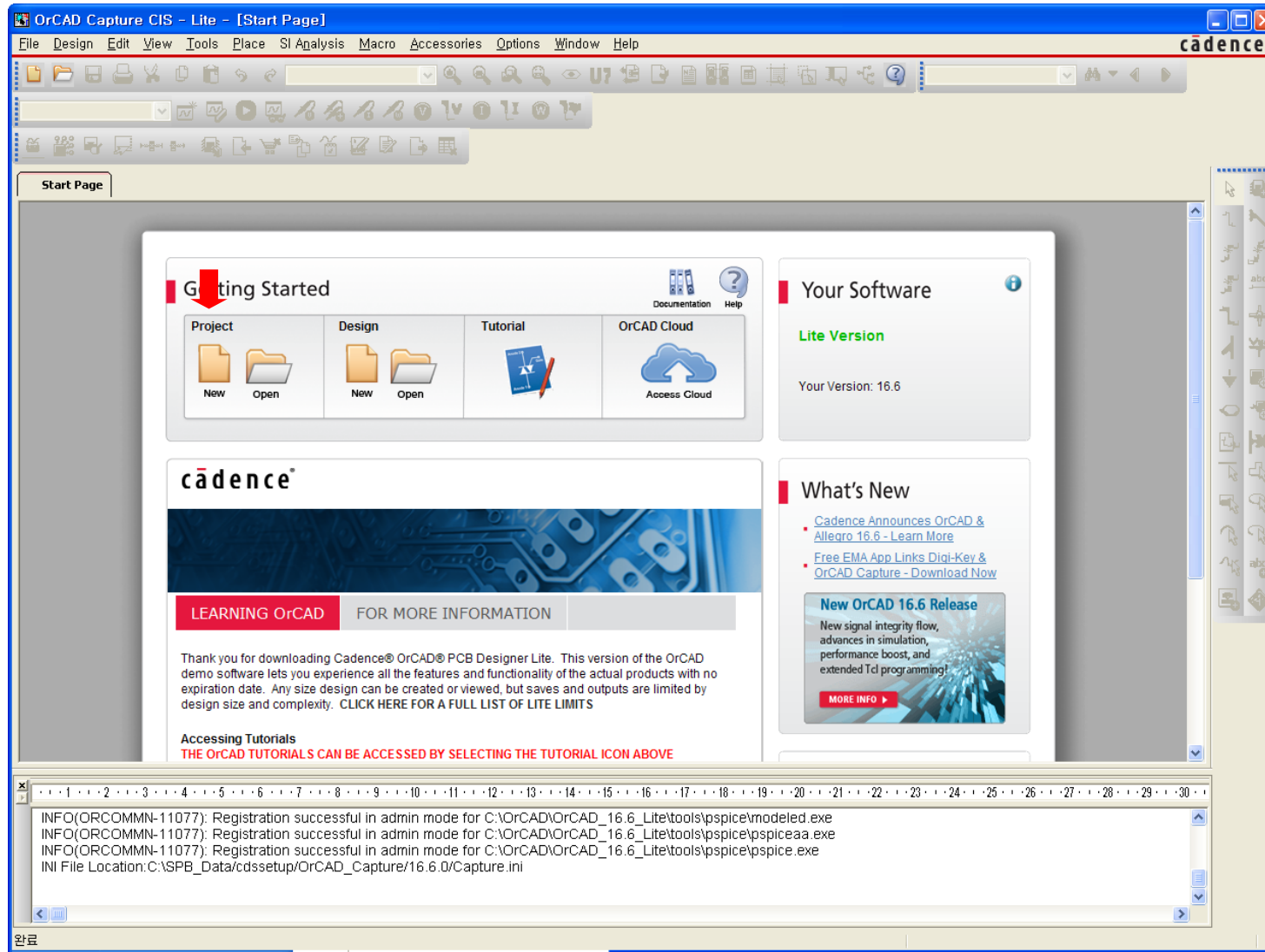
- Magnetic Parts Editor allows you to design power transformers only. The database shipped with Magnetic Parts Editor cannot be edited and contains a single core.

- The Model Import Wizard supports parts and simulation models that have a maximum of two pins or two terminals, respectively.

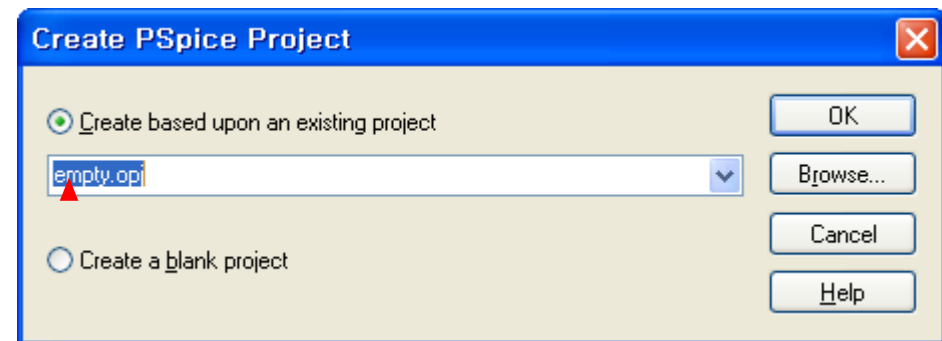
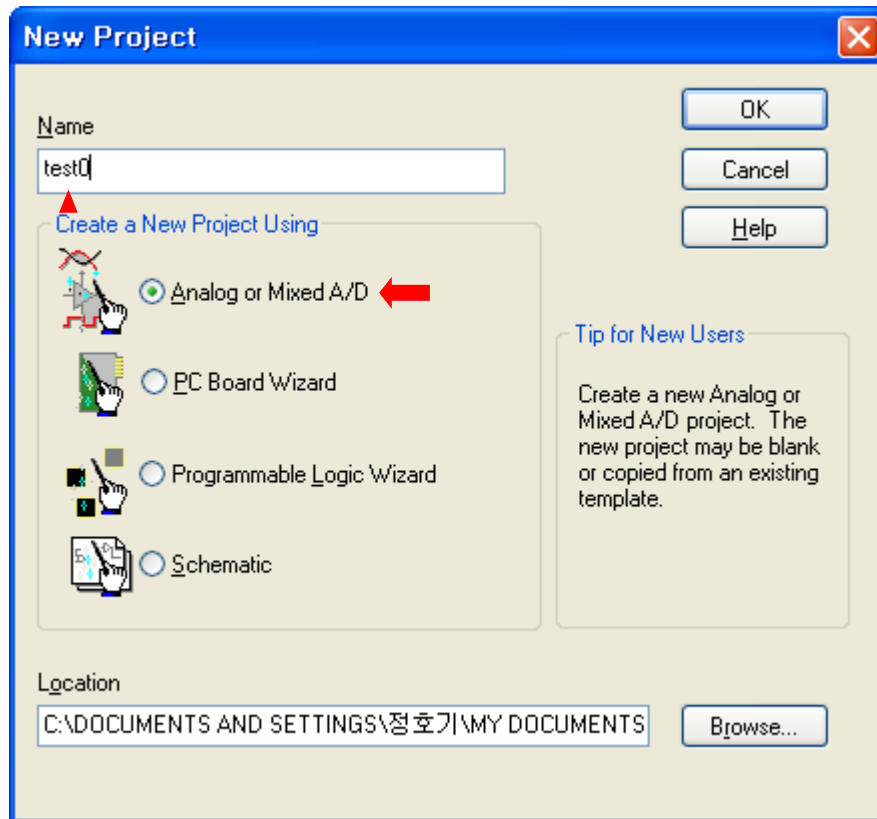
- The maximum nodes in a digital circuit can be equal to or less than 250.

- The non-ideal Tline is limited to 4.

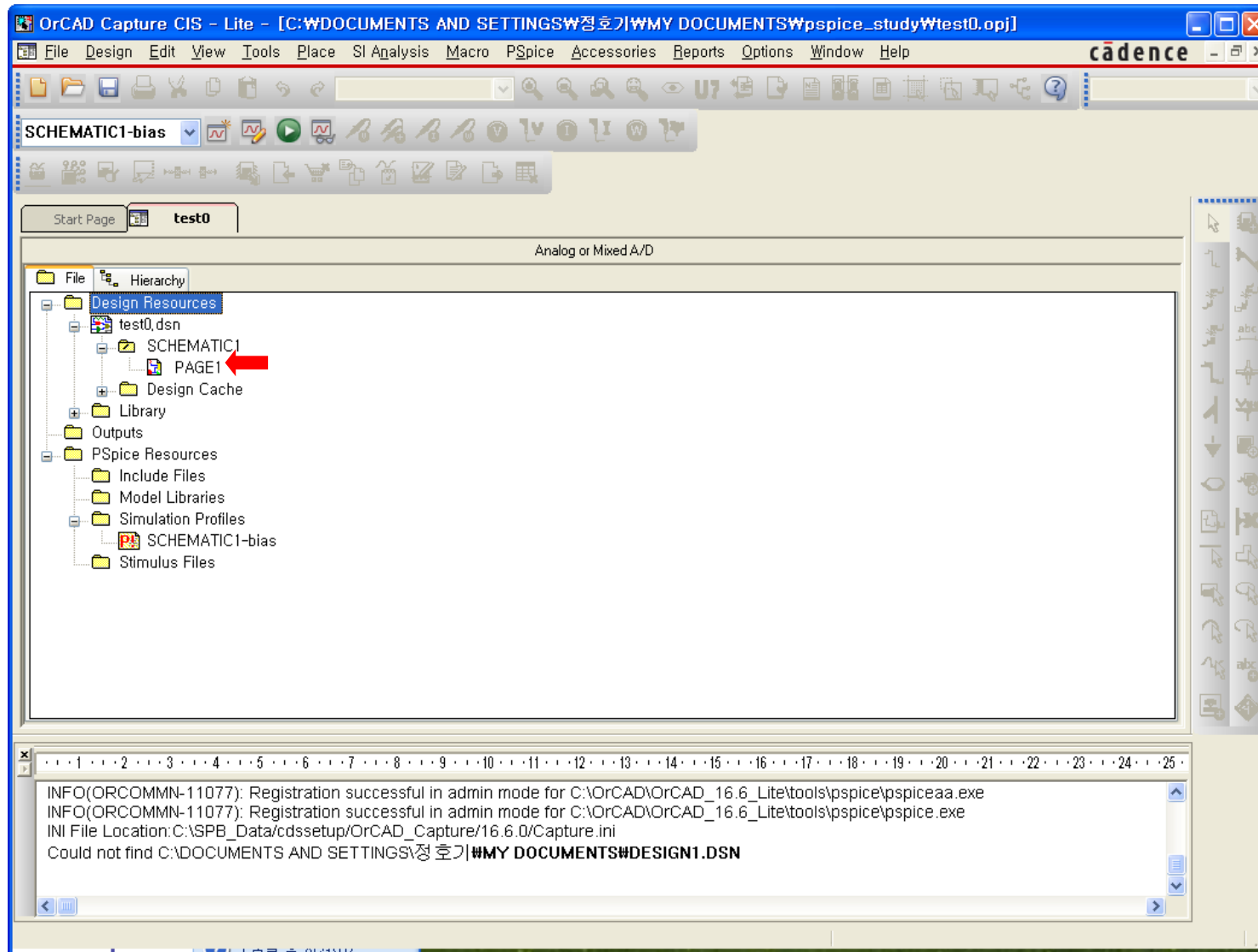
# Project



# Project

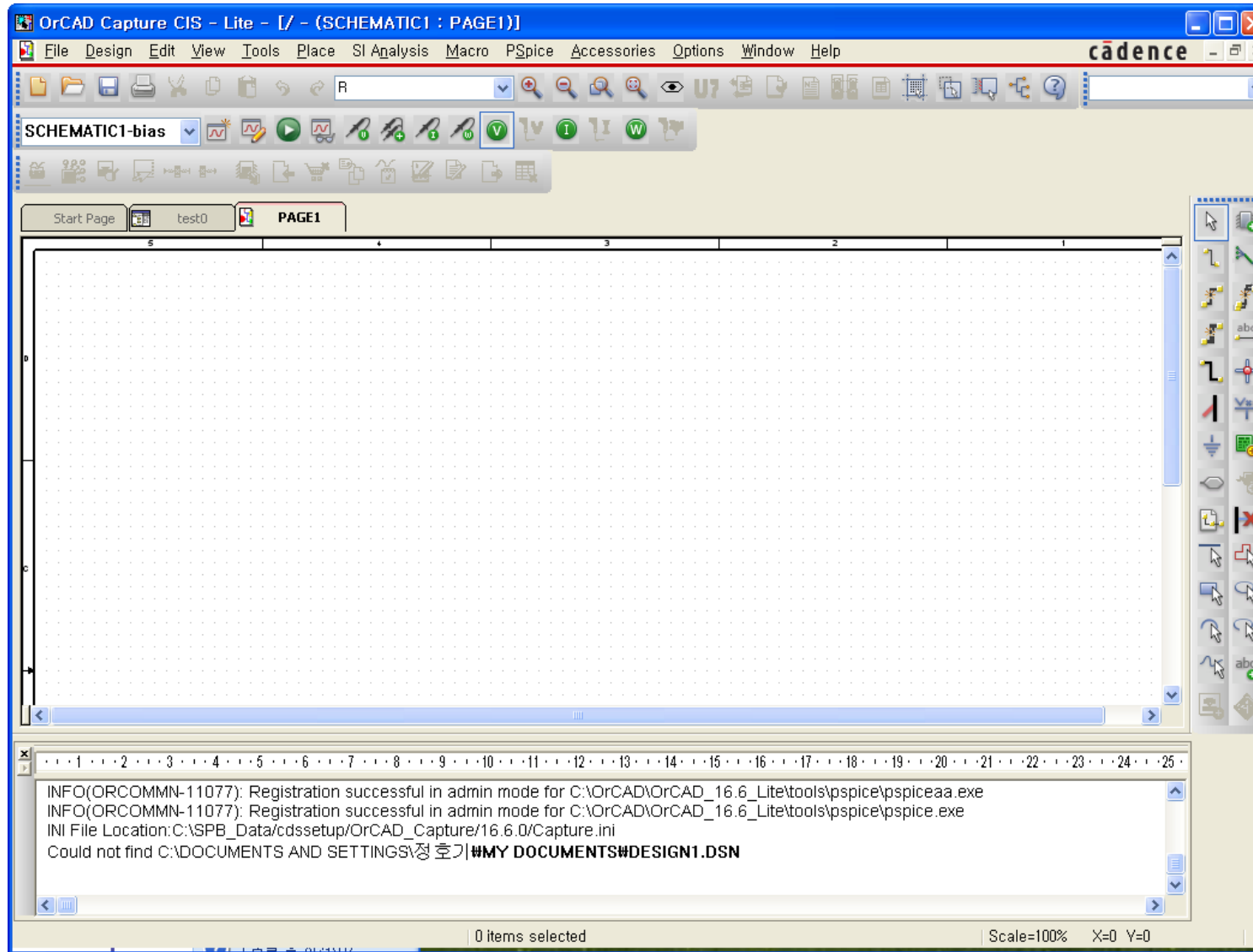


# Project

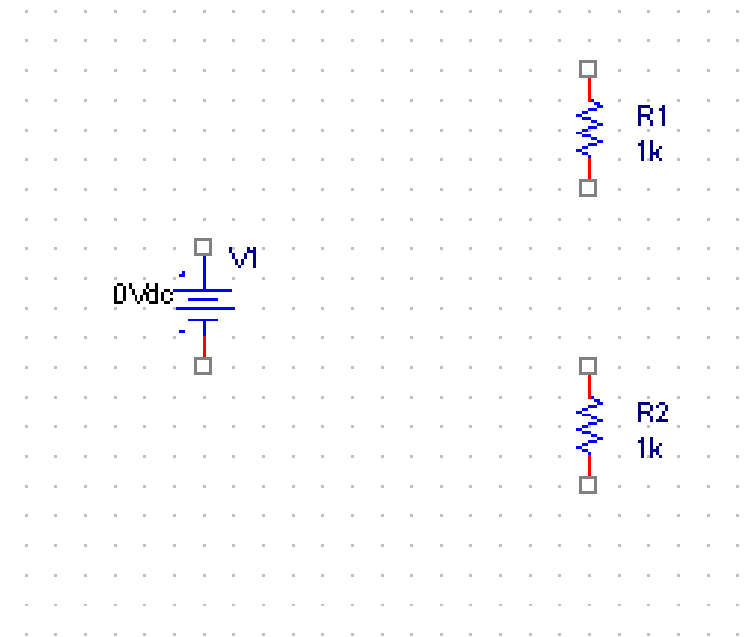
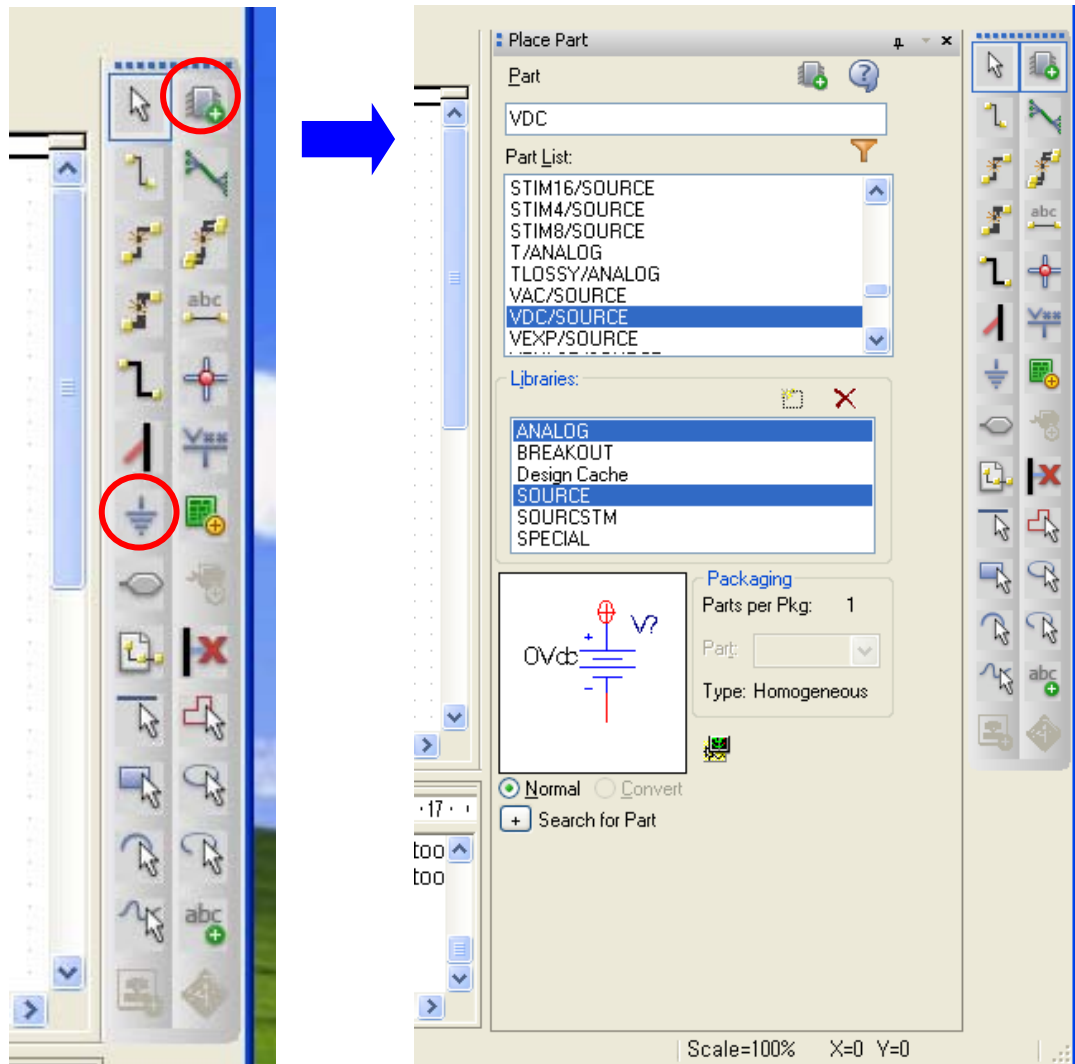




# Design



# Design

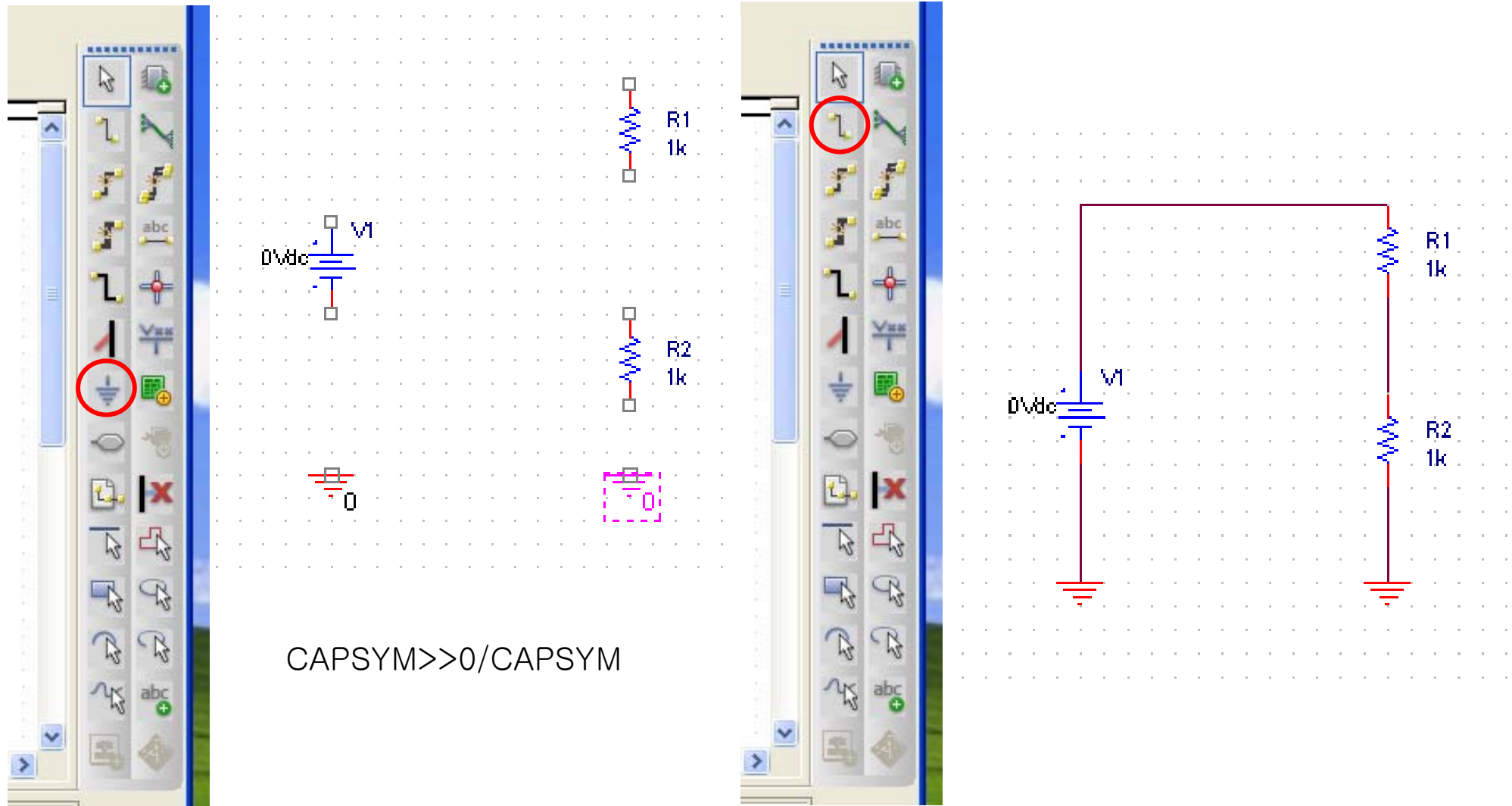


Libraries>>Part List

SOURCE>>VDC

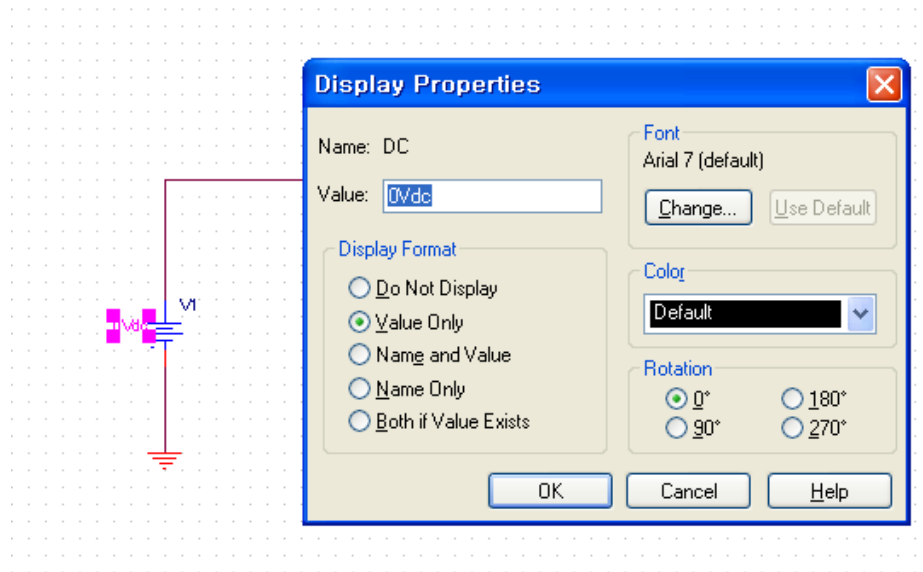
ANALOG>>R

# Design

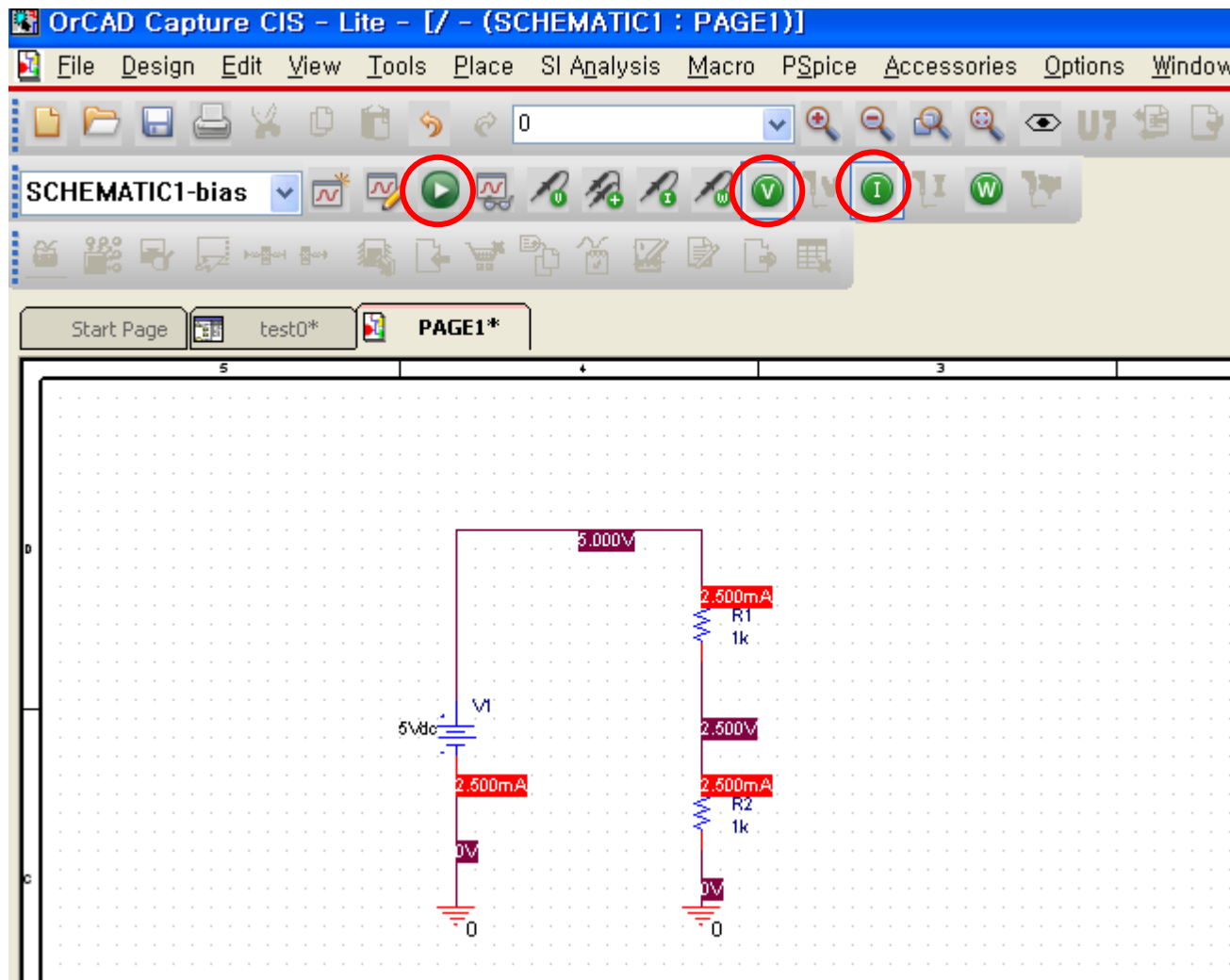


# Design

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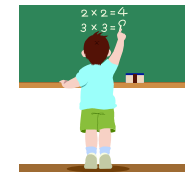
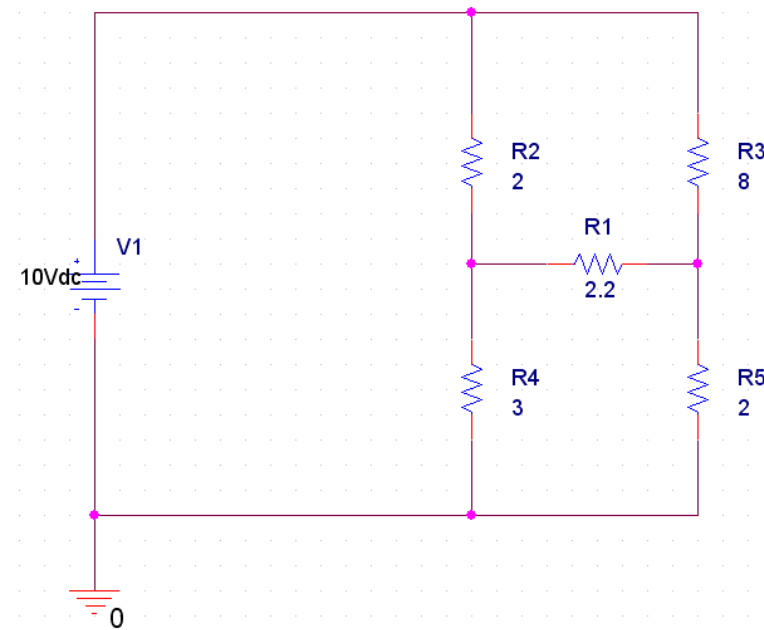
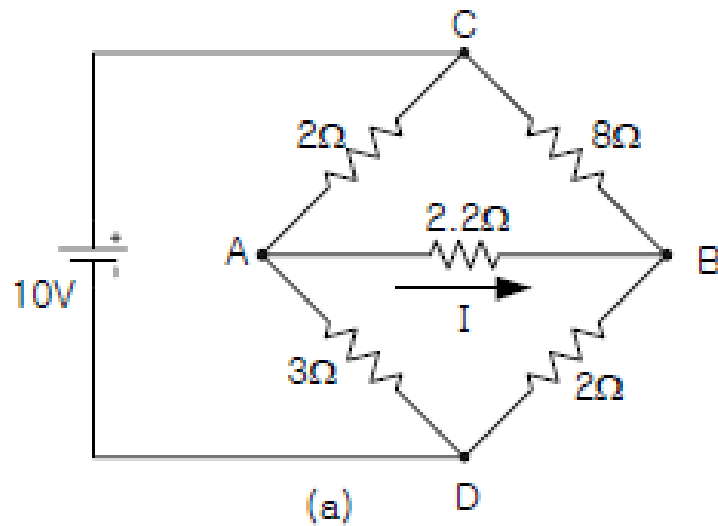


# Simulation



# 숙제

예제 3-19를 simulation을 이용해 푸시오.



# 숙제

