ECE 5730
Memory Systems

Spring 2009

Professor Dave Albonesi

Computer Systems Laboratory
School of Electrical and Computer Engineering

Welcome!

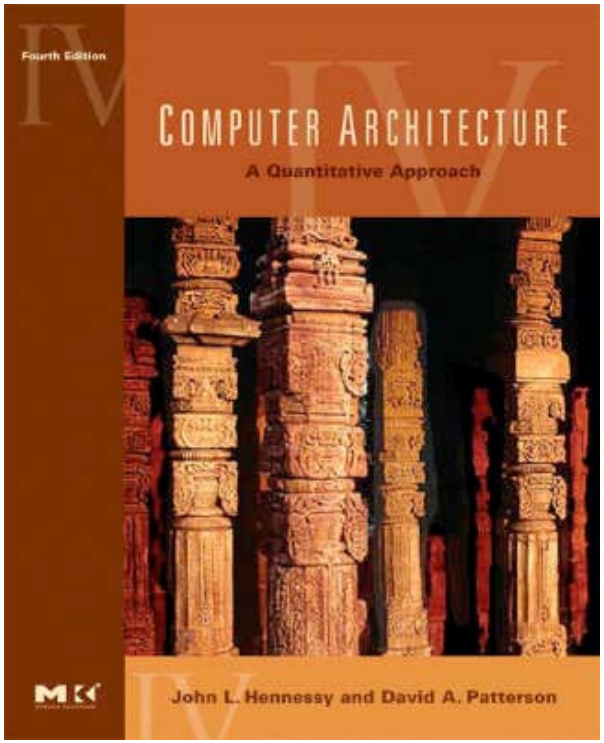
Cornell University

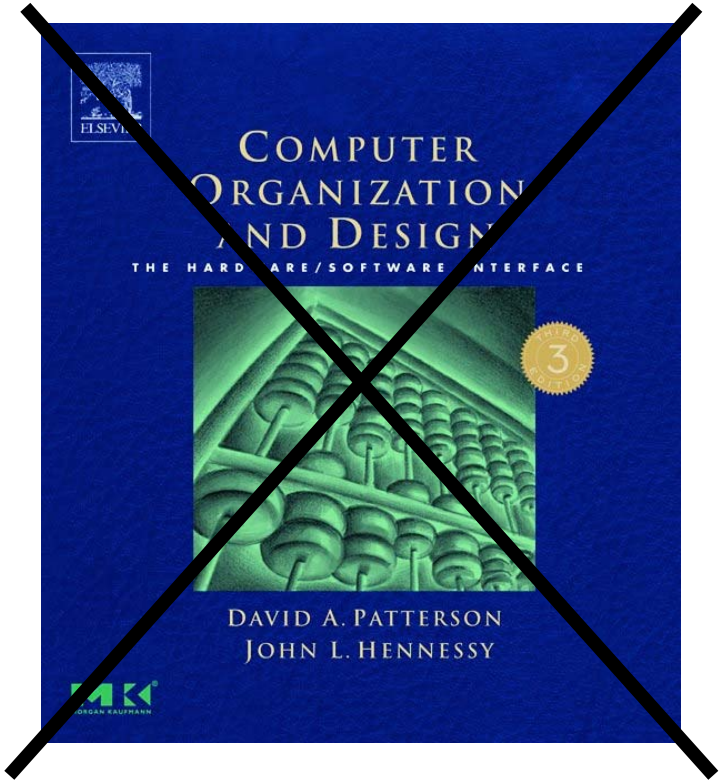
Instructor

- **Professor Dave Albonesi**
  - **333 Rhodes Hall**
  - **dha7@cornell.edu**
  - **254-5473**
  - **Office Hours: Tuesday & Thursday from 1-2pm and by appointment**

Prerequisites

- **You must have had ECE 4750 (or an equivalent course) to take this class!**





- **But you don't need ECE 5720!**

Course Logistics

- **Textbook**
  - **Memory Systems by Jacob, Ng, and Wang**
  - **Also technical papers**

- **Blackboard**
  - **Announcements, lecture slides, papers**
  - **Please self-enroll this week**

Grading

- **Grade Computation**
  - **Weekly quizzes: 25%**
  - **2 Exams: 50% (25% each)**
  - **Project: 25%**

Quizzes

- **First 10 minutes on Tuesdays**
  - **Will start on time (too bad if you show up late)**
  - **Covers lecture material from prior week**
  - **5 multiple choice questions (2 points each)**
  - **Open everything (including Blackboard site)**
  - **Lowest 3 quiz scores are dropped**
  - **No make-ups**

Exams

- **Two exams**
  - **Week of March 9th**
  - **Week of April 27th**
  - **Scheduled outside of class**
  - **Open everything**

- **No Final Exam**

Project

- Independent research project
- Use simulation tools to study some aspect of memory systems design
- Due in class on April 30th
- More about this in a few weeks…

Code of Academic Integrity

- **http://cuinfo.cornell.edu/Academic/AIC.html**
- **Strictly followed in this course (violators will be prosecuted)**
- **As Cornell students, you are responsible for reading and abiding by this policy**

Course Objectives

- **Understand in detail the issues, trade-offs, and techniques in designing memory systems**
  - **Cache hierarchies, main memories, disk systems**
  - **Physical, organizational, system-level**
  - **Performance, power, reliability**

down to magnetics on hard drives, etc

- **Gain knowledge of research in the field**

- **Acquire research experience via a project using simulation tools**

Course Topics

- **Caches**
  - Logical organization
  - Implementation issues
  - Management approaches
- **Main memories**
  - DRAM physical design
  - Organizational and signaling issues
  - Memory controllers
- **Disks**
  - Physical and data layers
  - Drive interface and bus standards
  - Disk caches
  - Disk controllers and systems

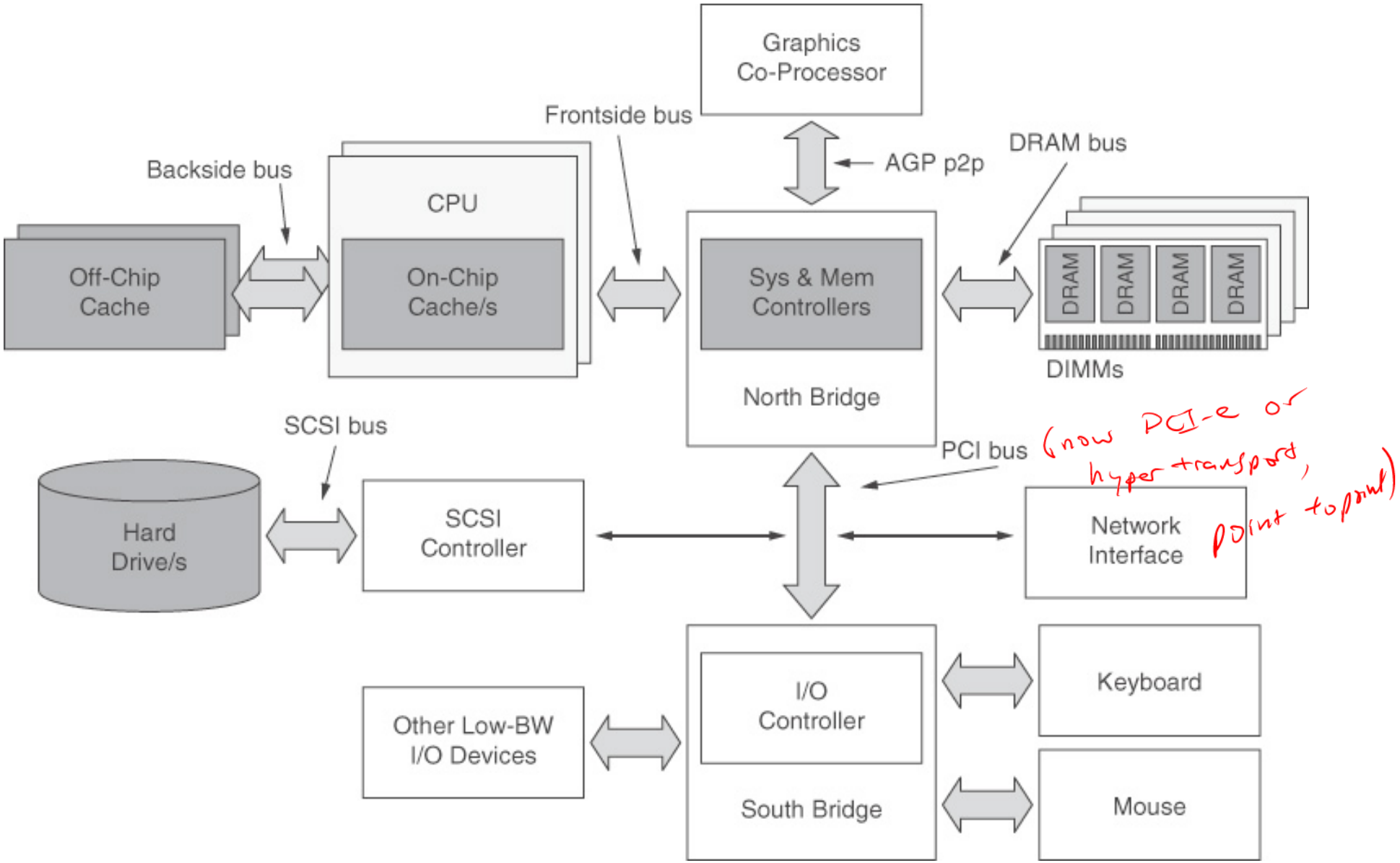
talk more about DRAM types, less about ECE 314/475 topics

Course Topics

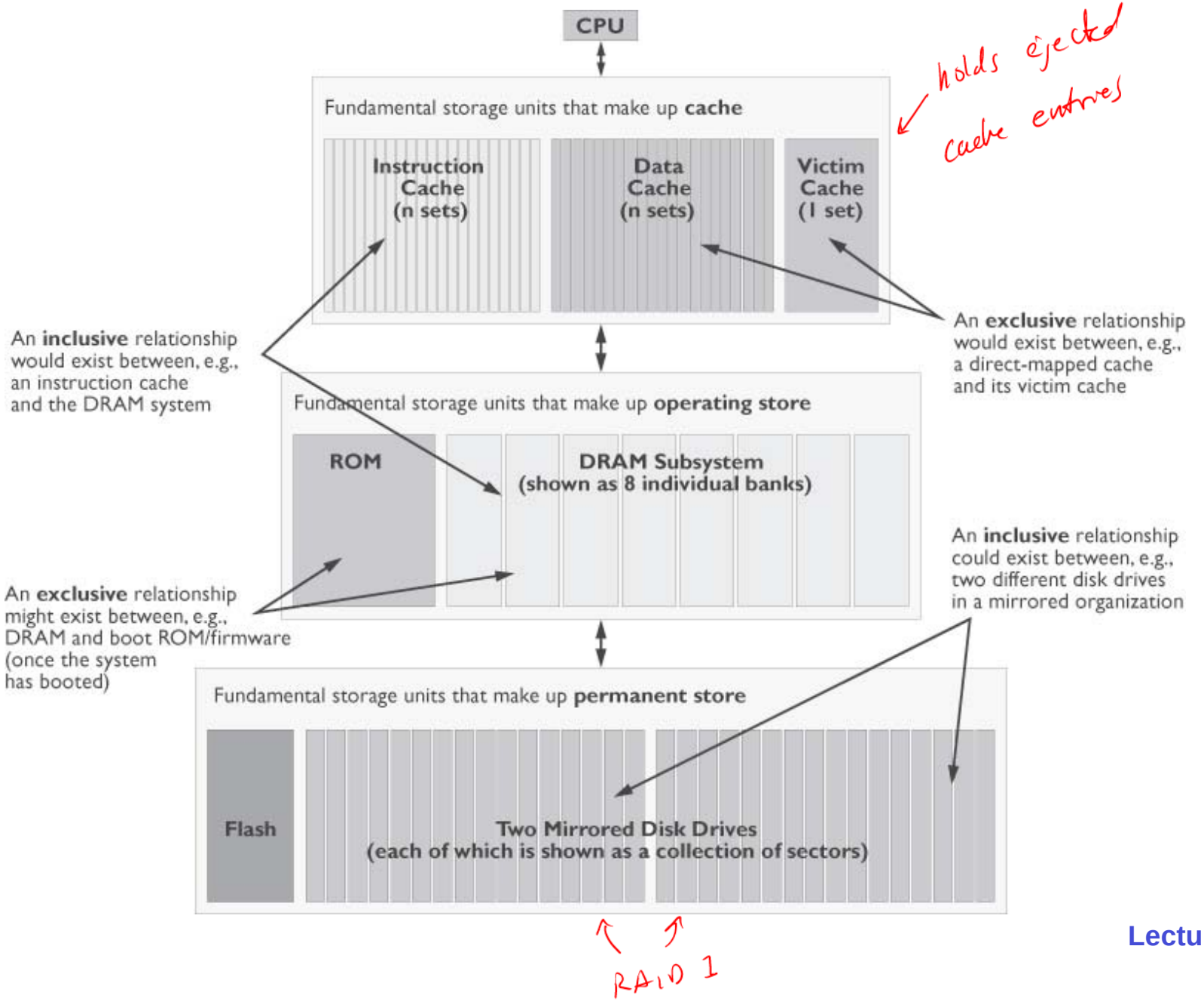
- **Case Studies**
- **Other topics**
  - **Power efficient memory system design**
  - **Memory systems for parallel computer architectures**
  - **Emerging memory technologies**

A very brief sampling of what's to come…

A Typical (Old) PC System

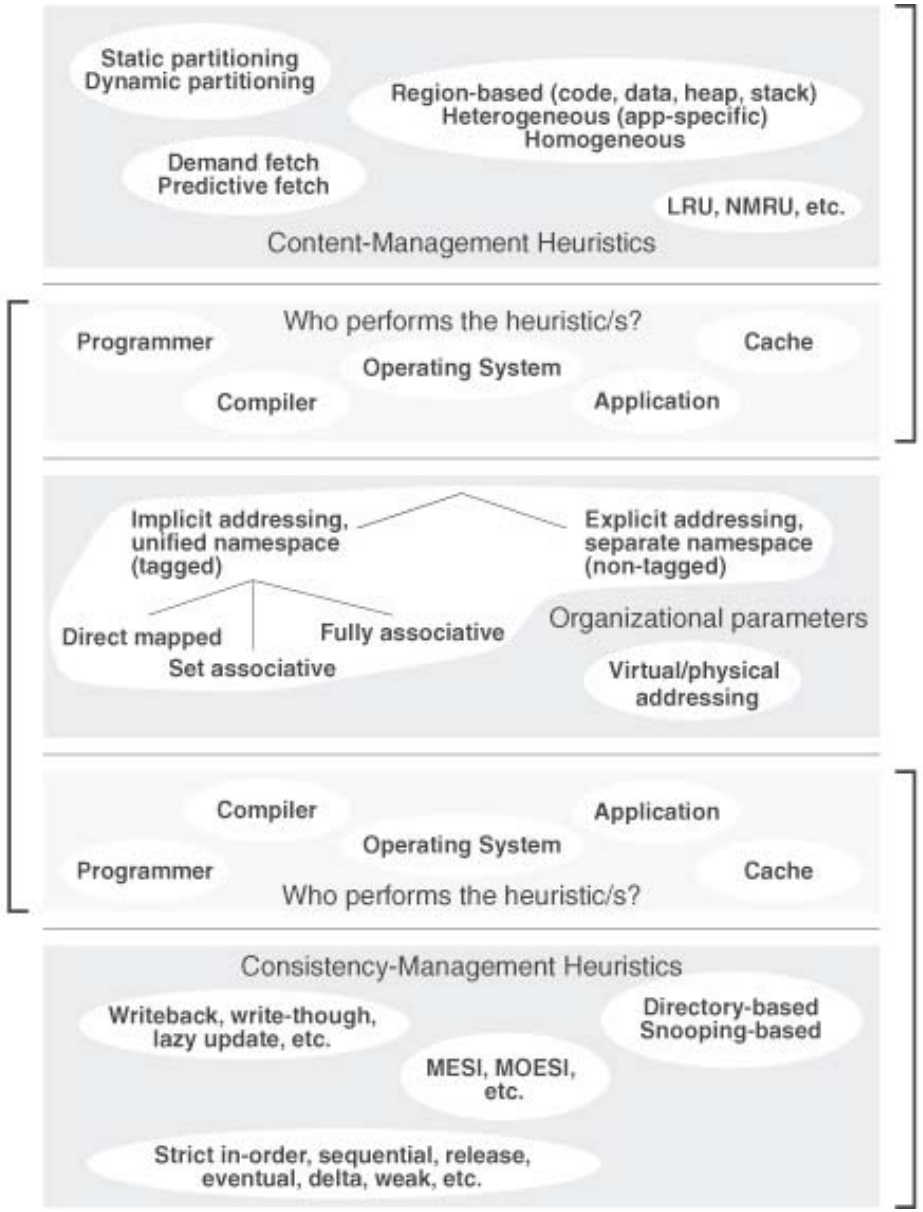


A Memory Hierarchy



A Few Cache Design Options…

many cache design options. Consistency is usually covered in ECE 5720



Logical Organization

Transparent Caches
Software-Managed Caches
Self-Managed Scratch-Pads
Scratch-Pad Memories

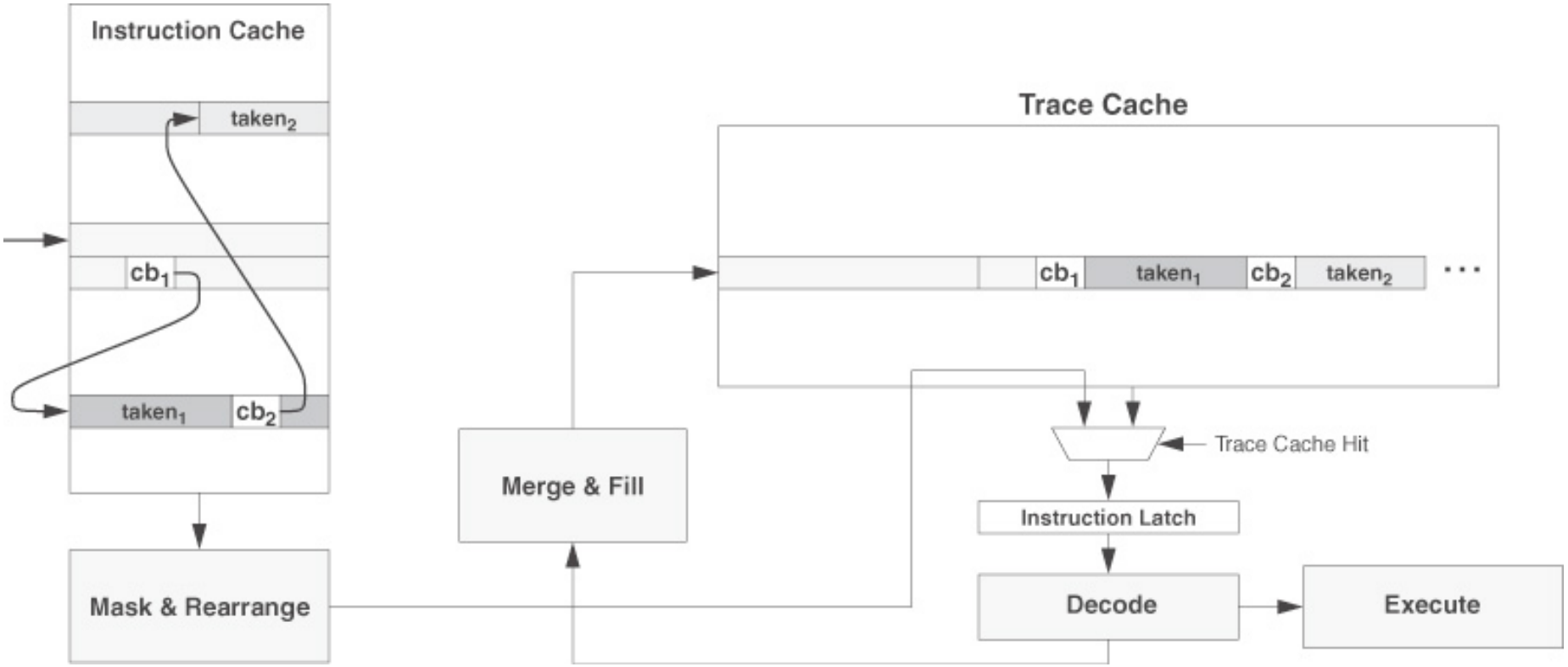
Content Management

Design-Time Heuristics
Run-Time Heuristics

Consistency Management

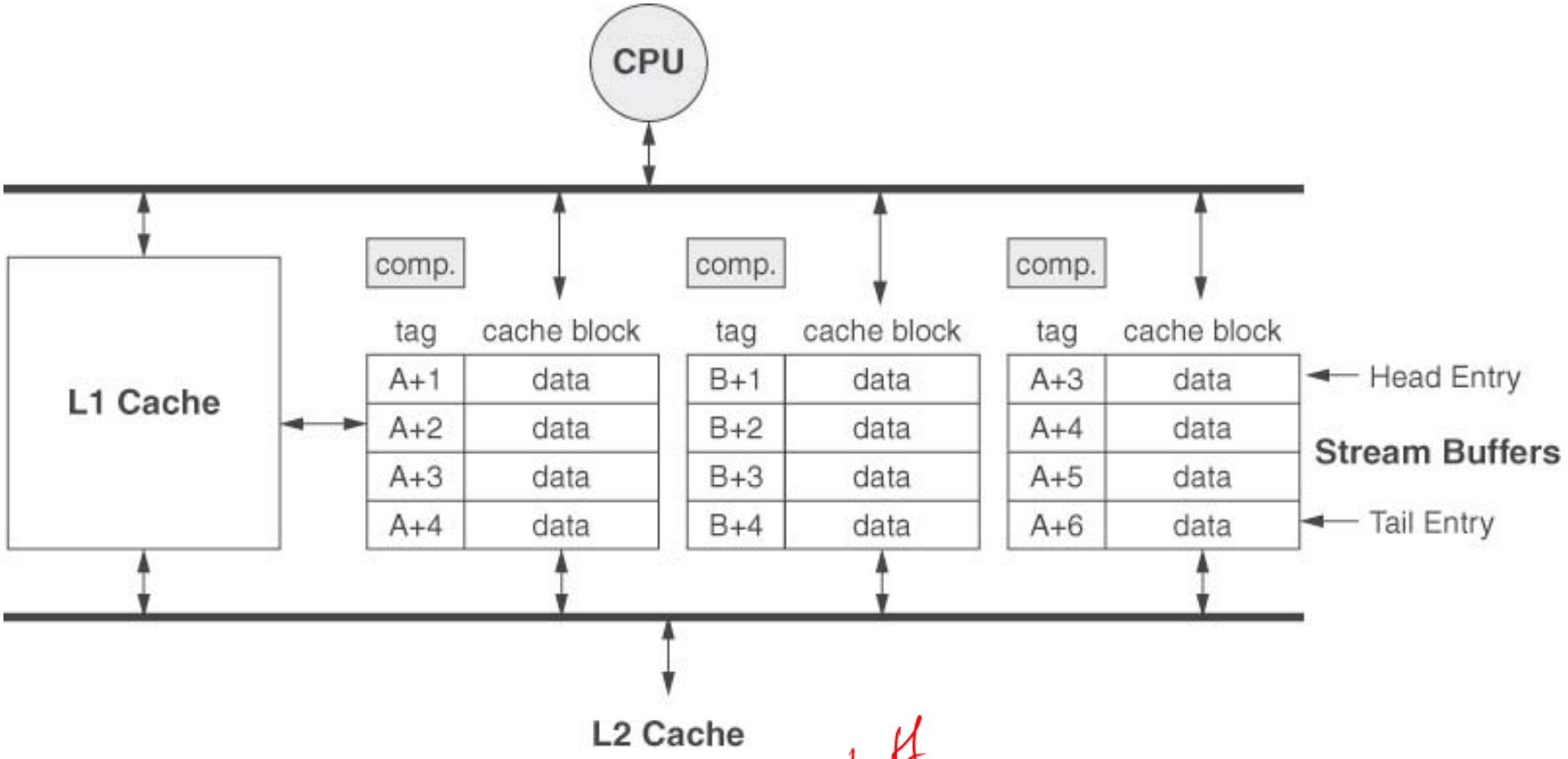
Consistency with Self
Consistency with Backing Store
Consistency with Other Caches

Trace Cache



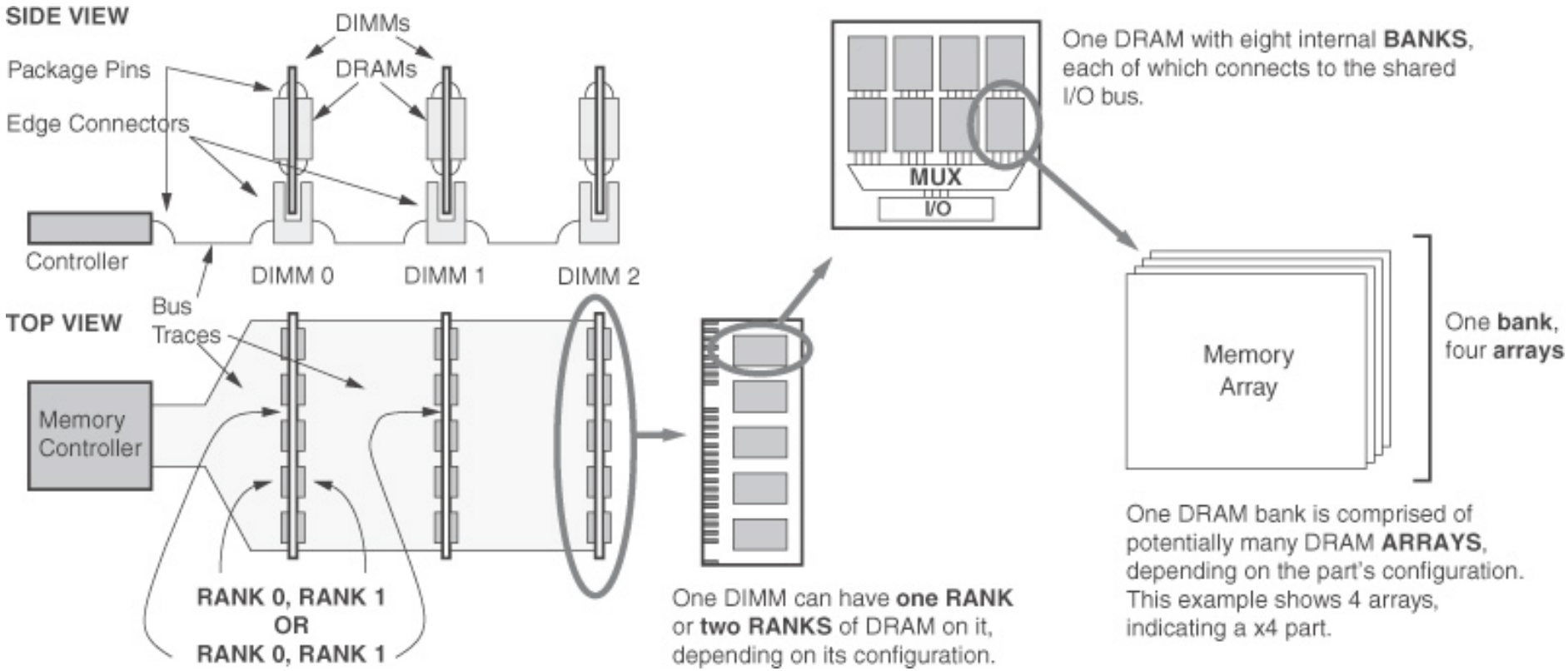
assembles instructions in a smart way to get better performance on next access

Stream Buffers

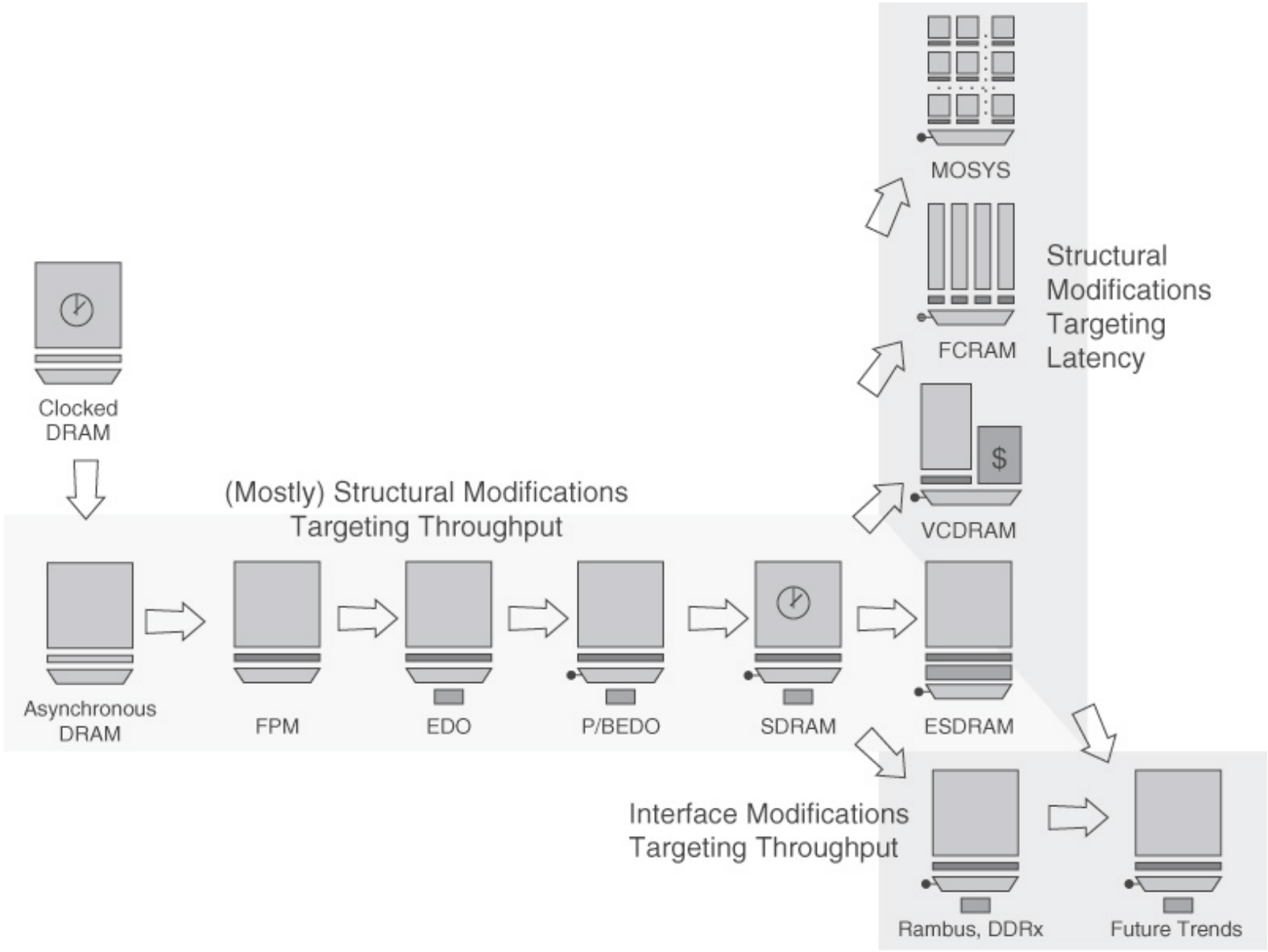


fancy prefetch stuff, apparently

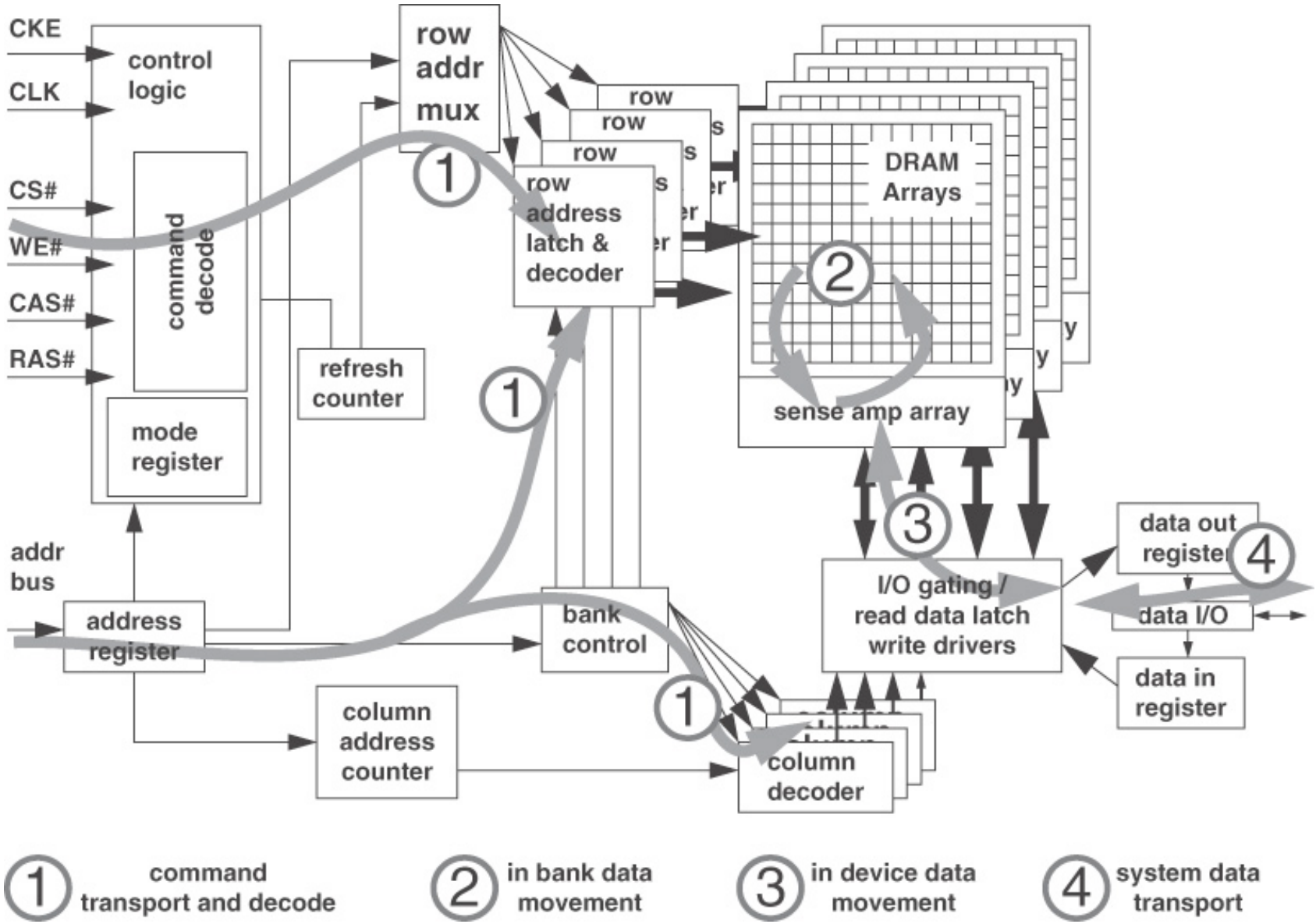
Main Memory


SIDE VIEW
DIMMs
DRAMs
Package Pins
Edge Connectors
Controller
DIMM 0
DIMM 1
DIMM 2
TOP VIEW
Bus Traces
Memory Controller
RANK 0, RANK 1
OR
RANK 0, RANK 1
One DIMM can have one RANK or two RANKS of DRAM on it, depending on its configuration.
MUX
I/O
One DRAM with eight internal BANKS, each of which connects to the shared I/O bus.
Memory Array
One bank, four arrays
One DRAM bank is comprised of potentially many DRAM ARRAYS, depending on the part's configuration. This example shows 4 arrays, indicating a x4 part.

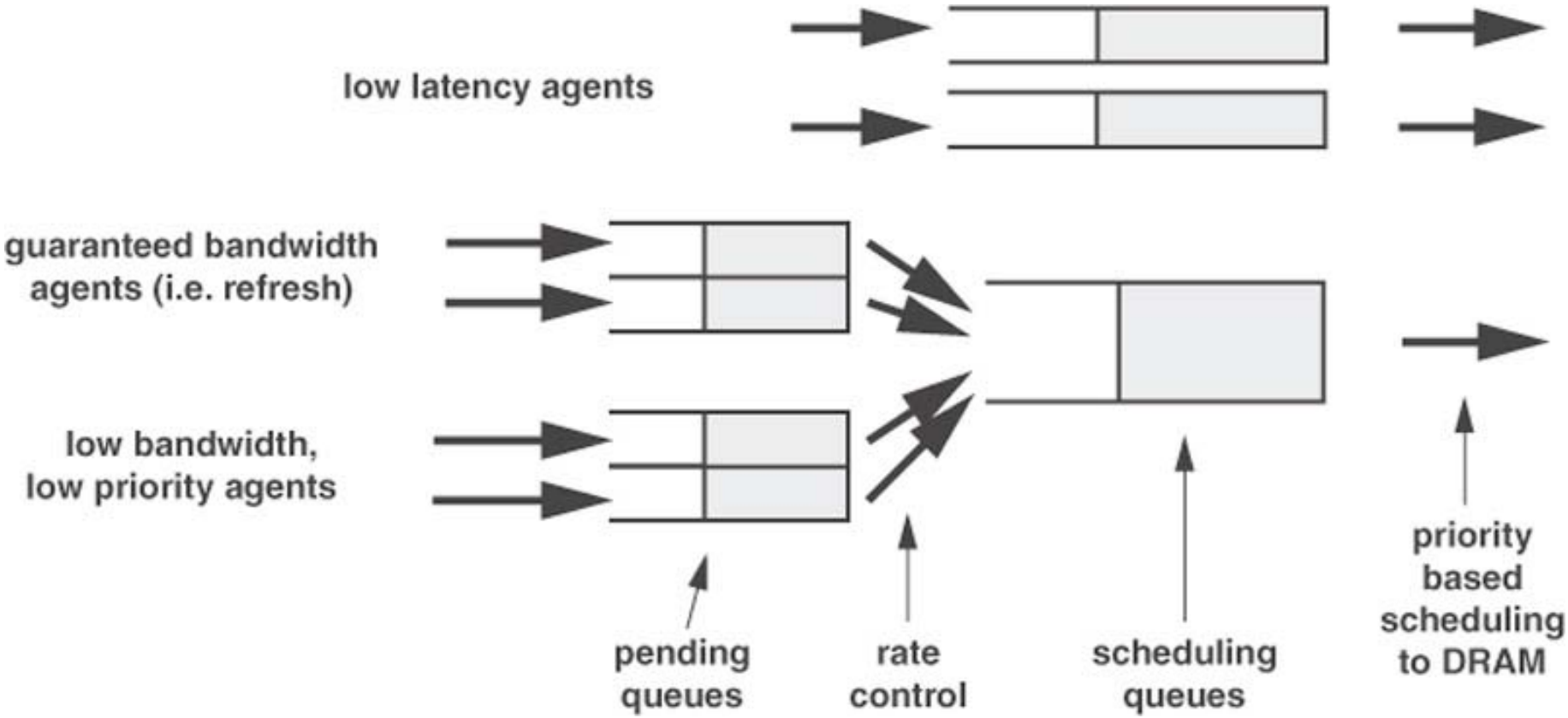
The Evolution of DRAMs



SDRAM Organization and Access

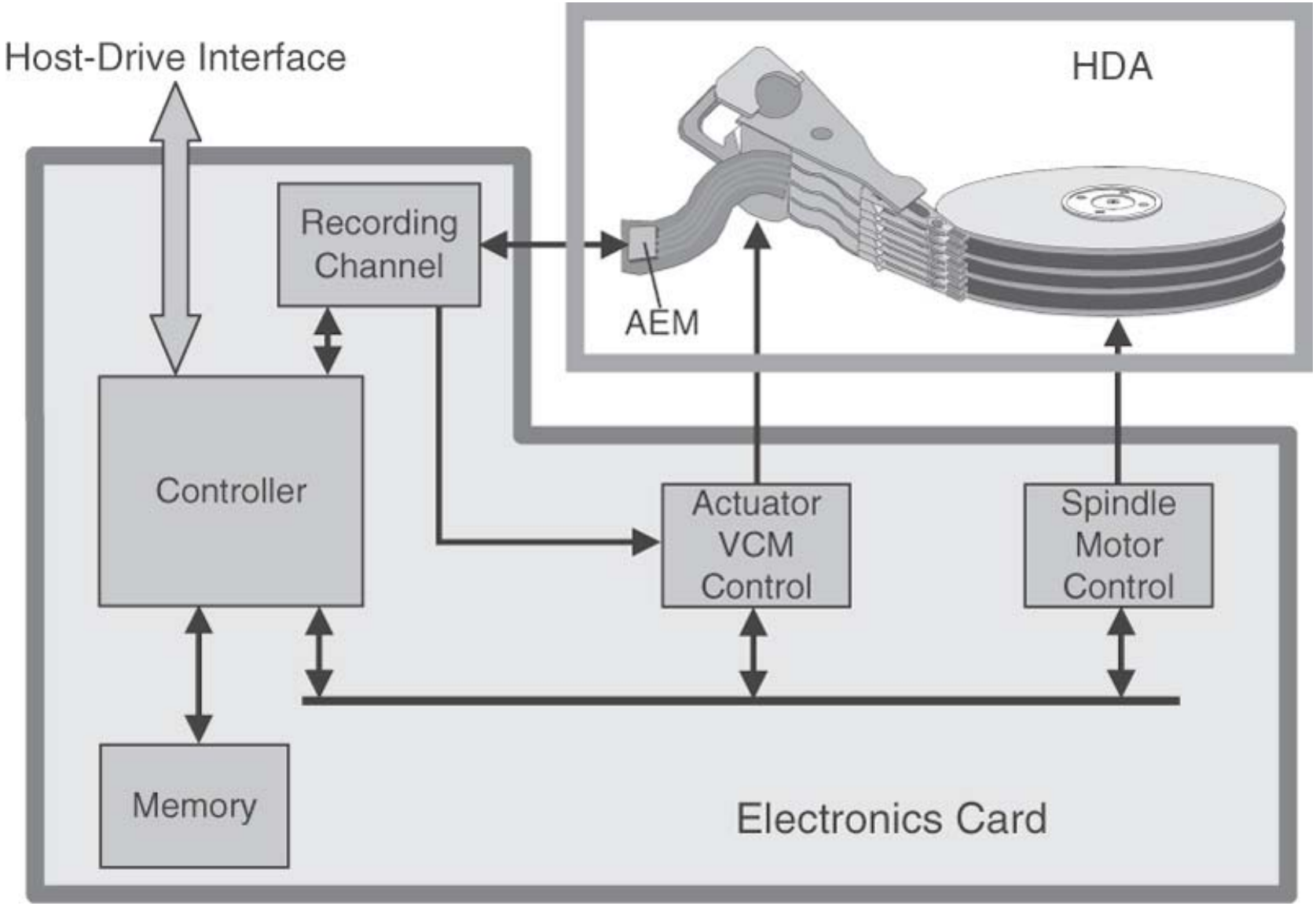


Memory Control

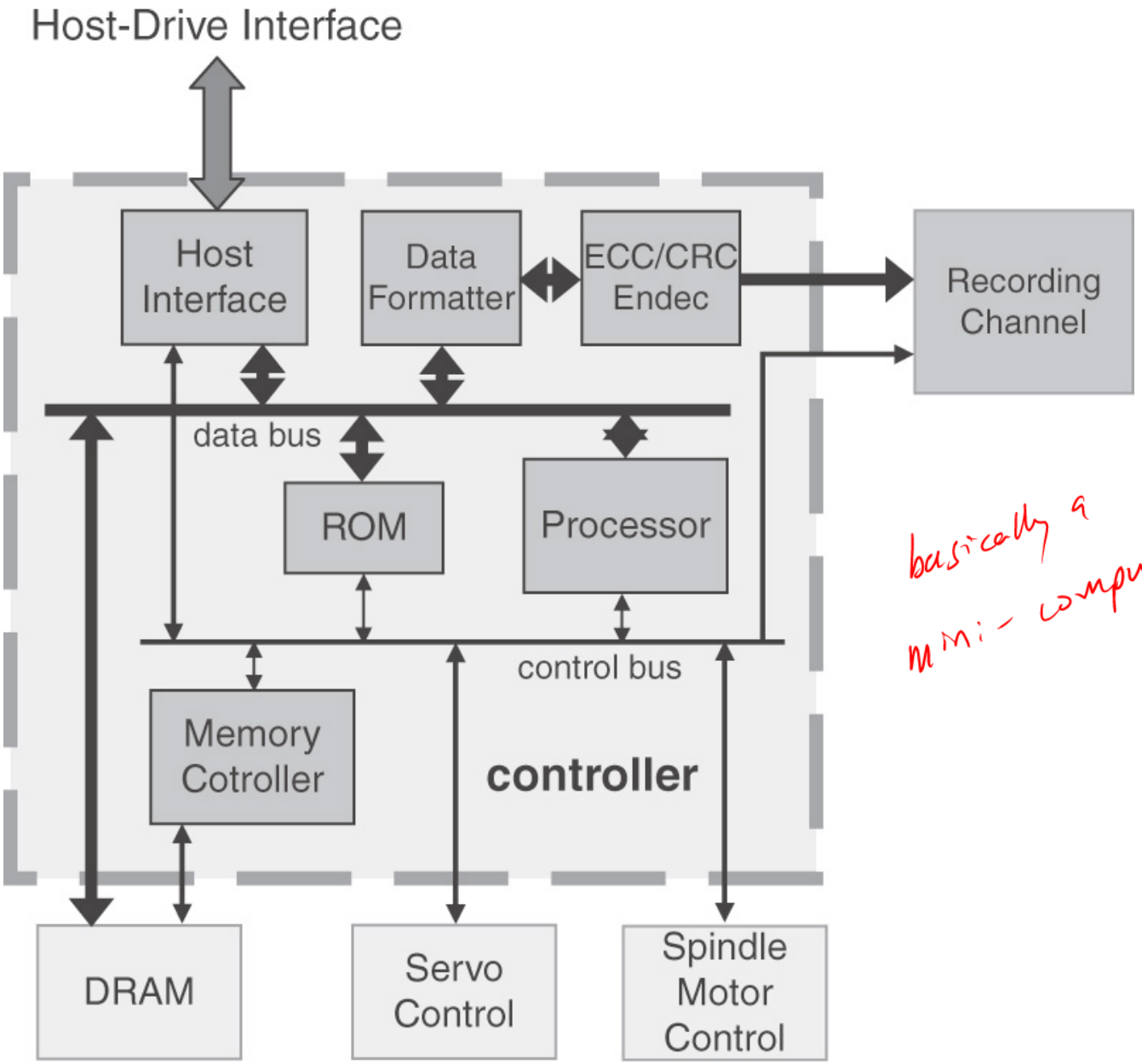


lots of things for a controller to consider

Disk Drives

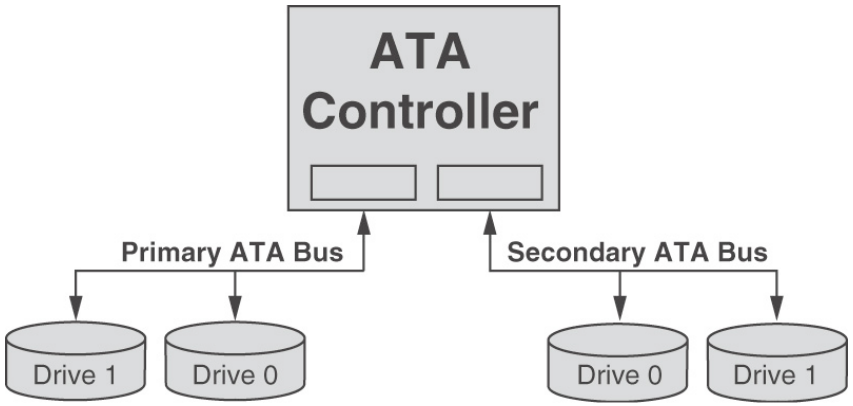

Host-Drive Interface
HDA
Recording Channel
AEM
Controller
Actuator VCM Control
Spindle Motor Control
Memory
Electronics Card

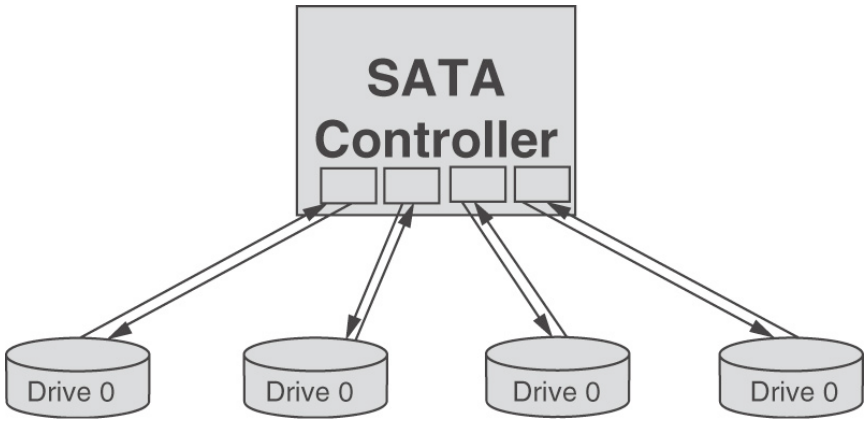
Disk Drive Controller

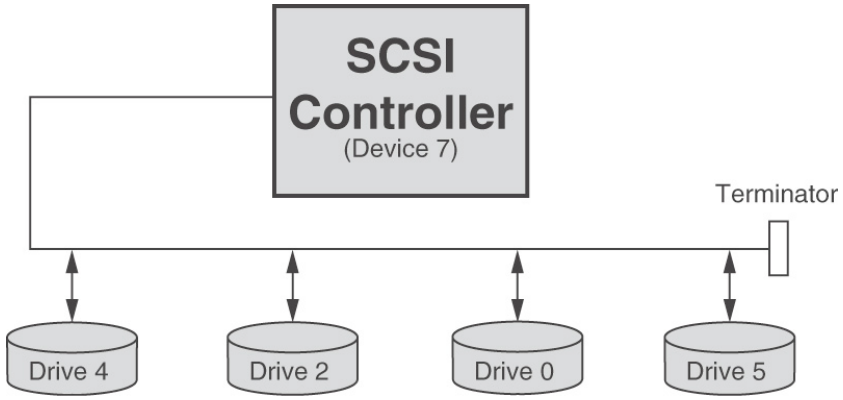


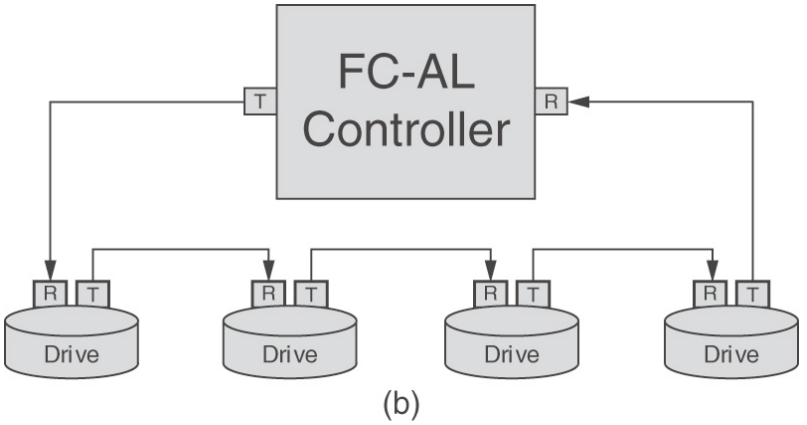
basically a mini-computer

Disk Interface Standards









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Next Time

Cache Organization