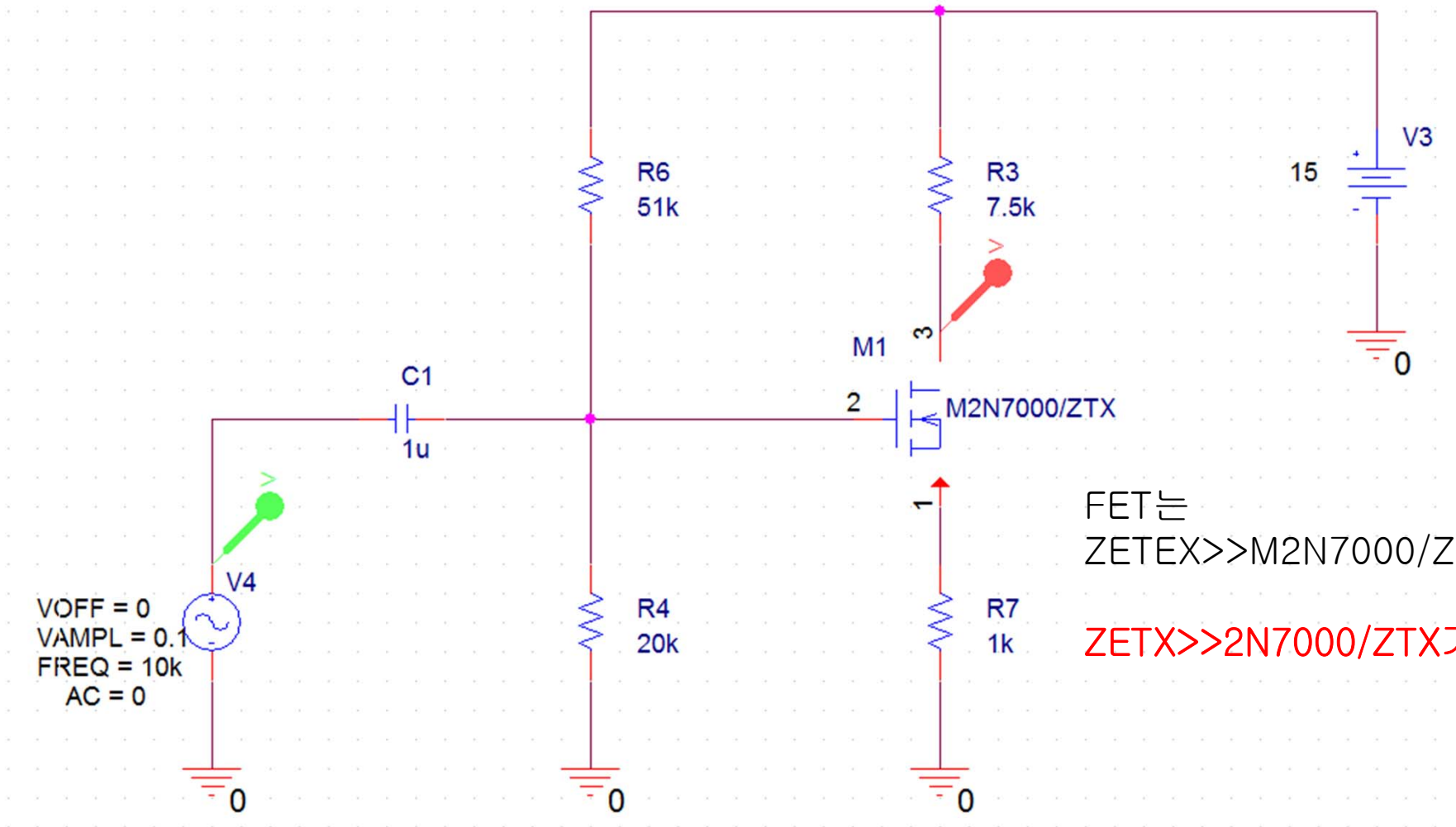


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# FET 증폭기

# 1. CS 증폭기



FET는  
ZETEX>>M2N7000/ZTX 사용

ZETEX>>2N7000/ZTX가 아님에 주의!

# 1. CS 증폭기



**2N7000**  
**2N7002**

N-channel 60 V, 1.8  $\Omega$ , 0.35 A, SOT23-3L, TO-92  
STripFET™ Power MOSFET

## Features

Type	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
2N7000	60 V	< 5 $\Omega$ (@10V)	0.35 A
2N7002	60 V	< 5 $\Omega$ (@10V)	0.20 A

- Low Q<sub>g</sub>
- Low threshold drive

## Application

- Switching applications

## Description

This Power MOSFET is the second generation of STMicroelectronics unique "single feature size" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

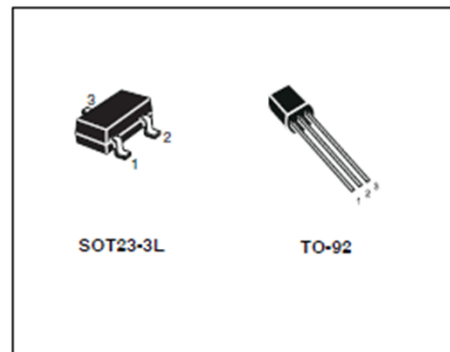


Figure 1. Internal schematic diagram

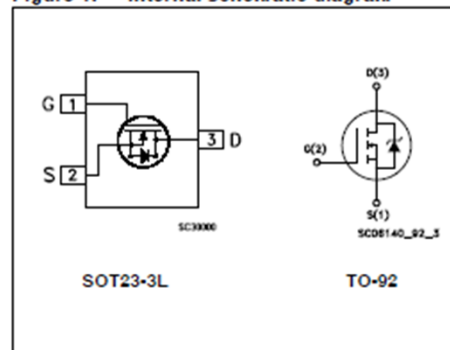


Table 1. Device summary

Order codes	Marking	Package	Packaging
2N7000	2N7000G	TO-92	Bulk
2N7002	ST2N	SOT23-3L	Tape and reel

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**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-92	SOT23-3L	
→ $V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	60		V
$V_{DGR}$	Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	60		V
$V_{GS}$	Gate- source voltage	$\pm 18$		V
→ $I_D$	Drain current (continuous) at $T_C = 25 \text{ }^\circ\text{C}$	0.35	0.20	A
$I_{DM}^{(1)}$	Drain current (pulsed)	1.4	1	A
$P_{TOT}$	Total dissipation at $T_C = 25 \text{ }^\circ\text{C}$	1	0.35	W

1. Pulse width limited by safe operating area

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**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	60			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{max rating}$ $V_{DS} = \text{max rating}, T_C = 125^\circ C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 18 V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1	2.1	3	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 V, I_D = 0.5 A$ $V_{GS} = 4.5 V, I_D = 0.5 A$		1.8 2	5 5.3	$\Omega$ $\Omega$

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**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10\text{ V}, I_D = 0.5\text{ A}$		0.6		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$		43 20 6		pF pF pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 30\text{ V}, I_D = 0.5\text{ A}$ $R_G = 4.7\ \Omega, V_{GS} = 4.5\text{ V}$ (see <a href="#">Figure 16</a> )		5 15 7 8		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 30\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 5\text{ V}$ (see <a href="#">Figure 17</a> )		1.4 0.8 0.5	2	nC nC nC

1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.



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**Table 6. Source drain diode**

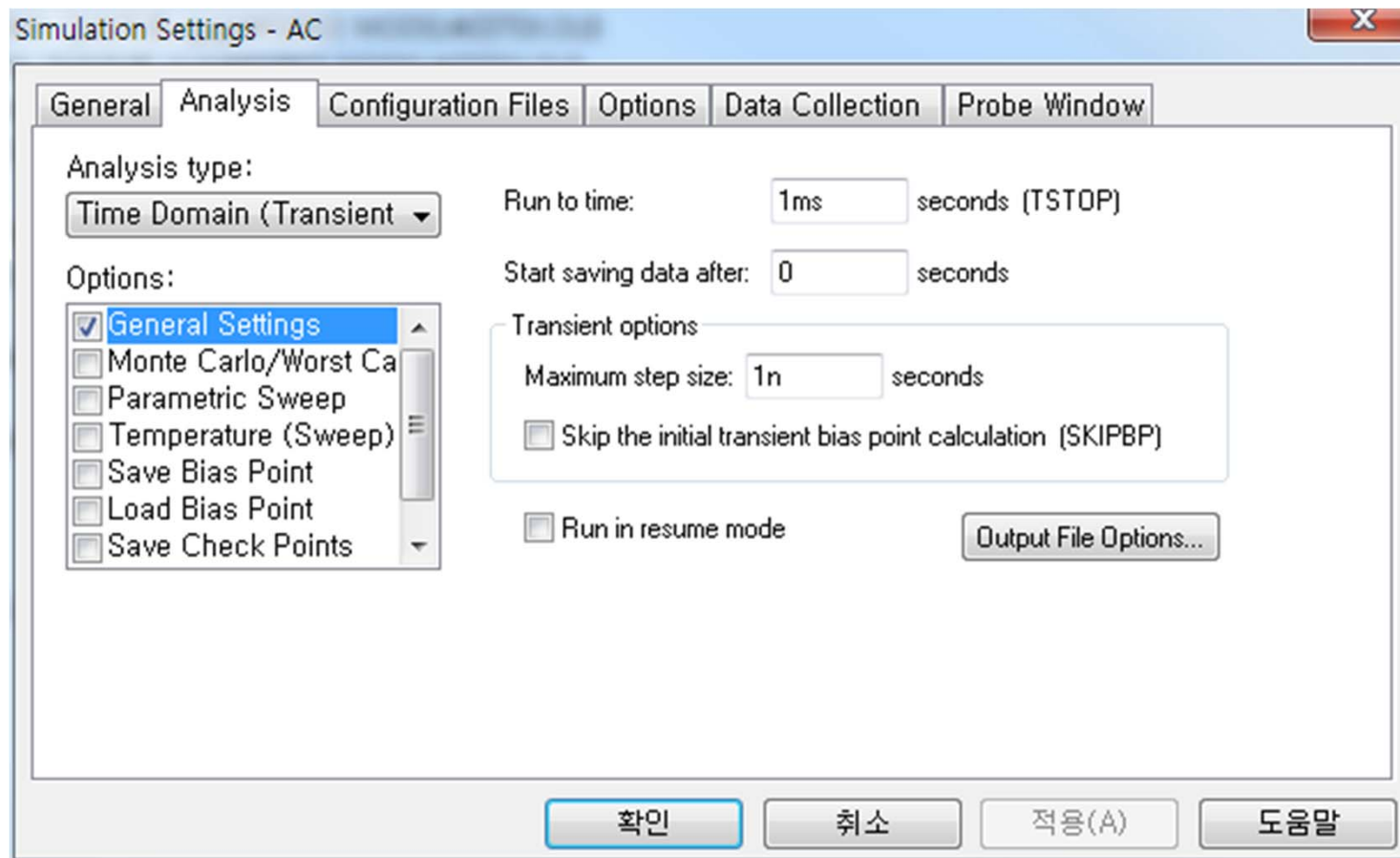
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				0.35 1.40	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 1 \text{ A}$ , $V_{GS} = 0$			1.2	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 1 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 20 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 18</a> )		32 25 1.6		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

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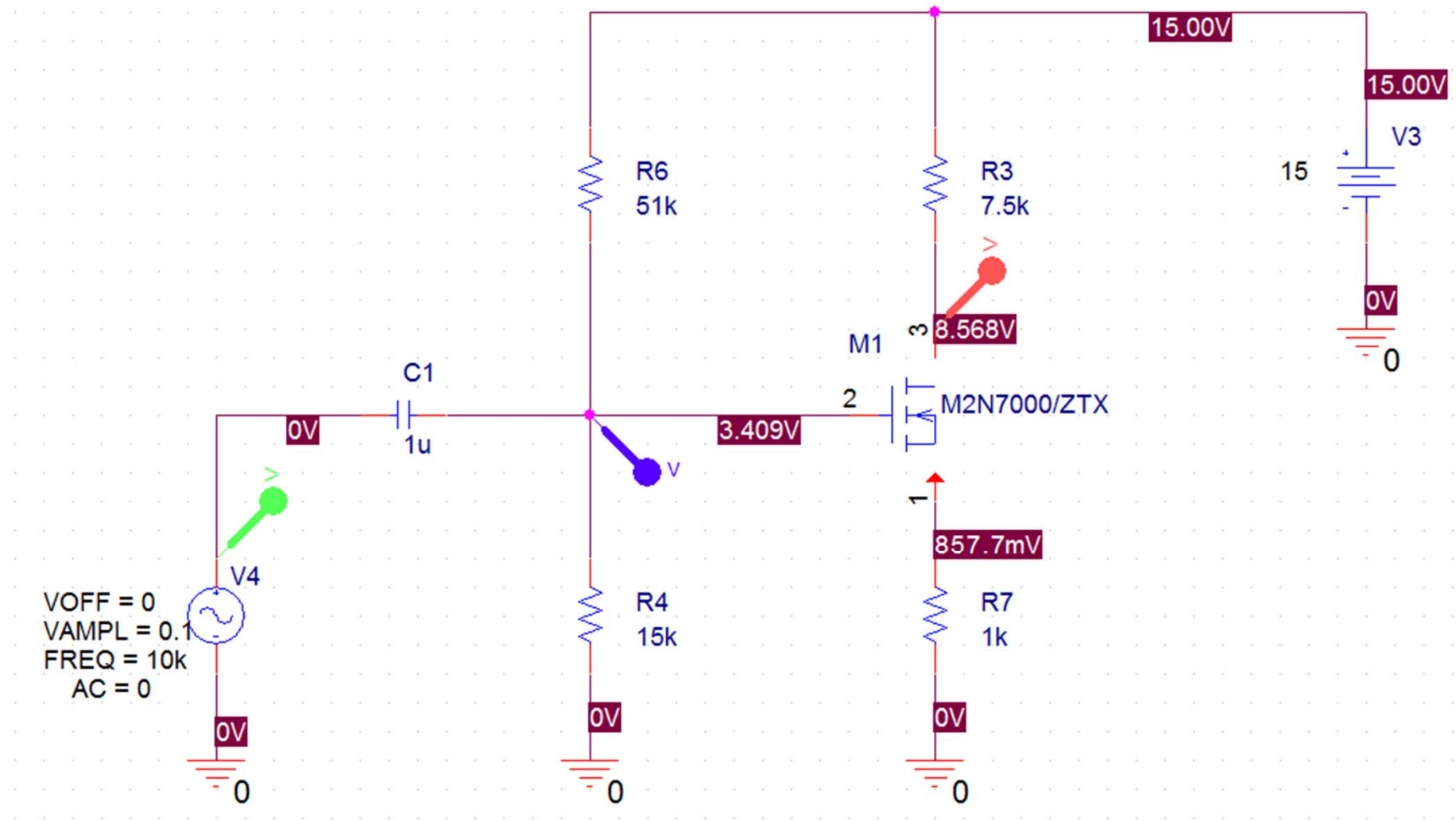
Transient Analysis

0~1ms까지, 1ns 정밀도

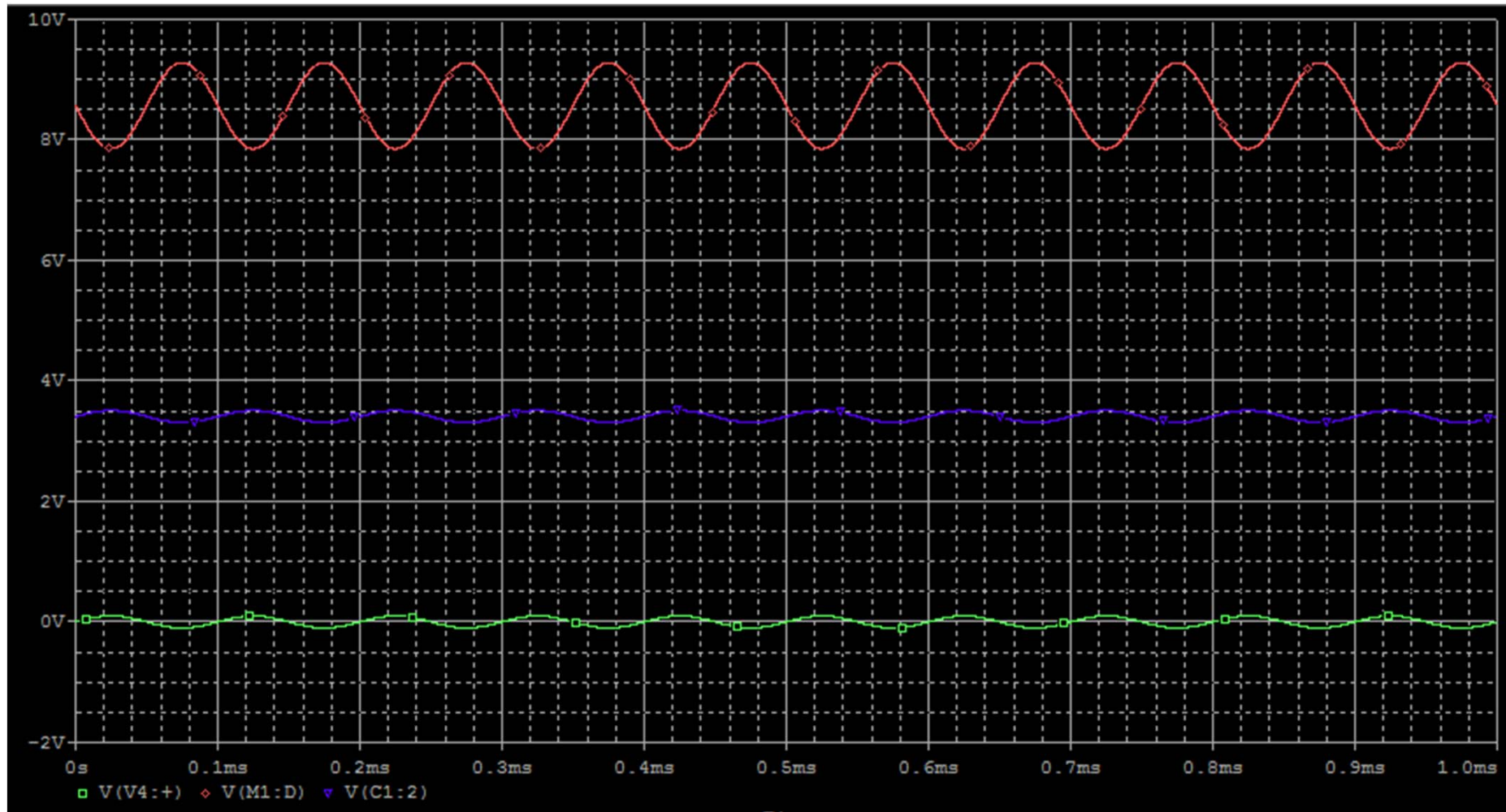




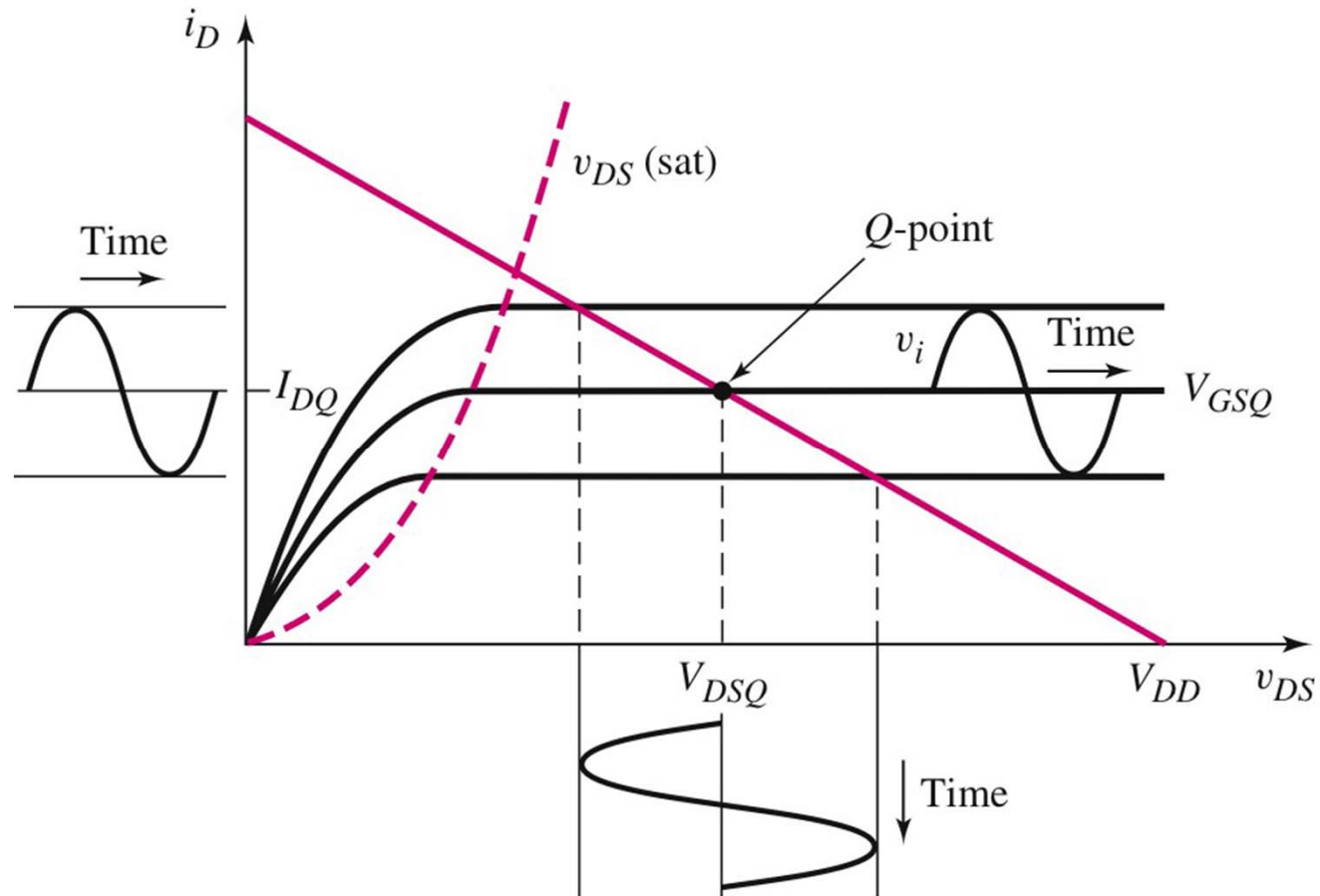
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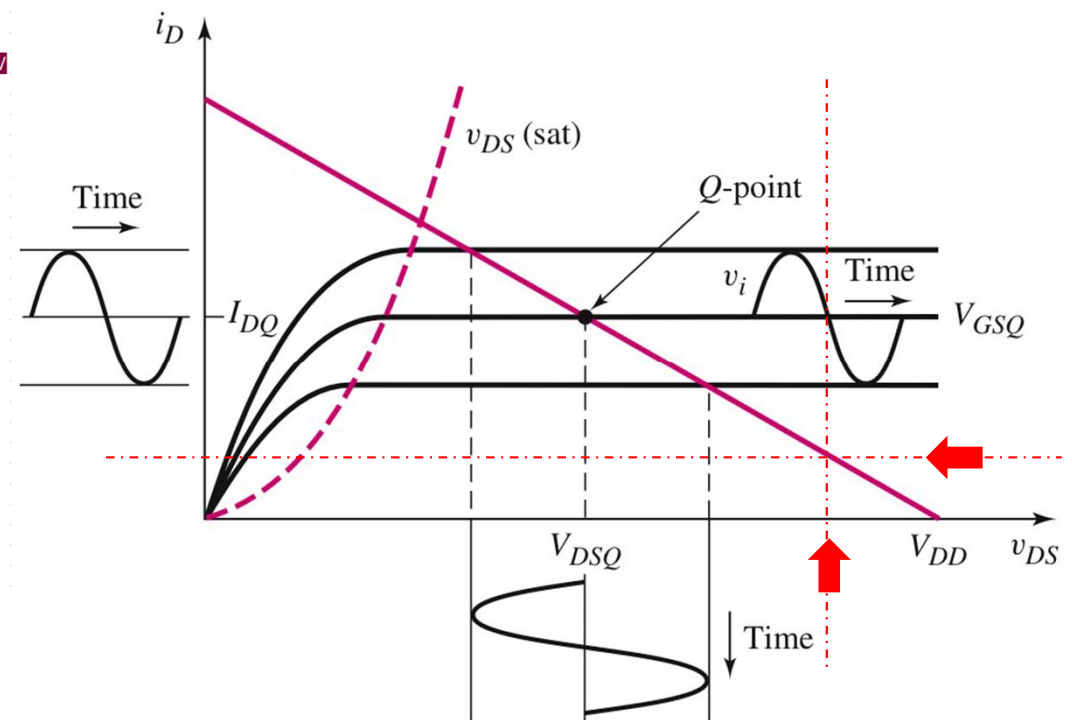
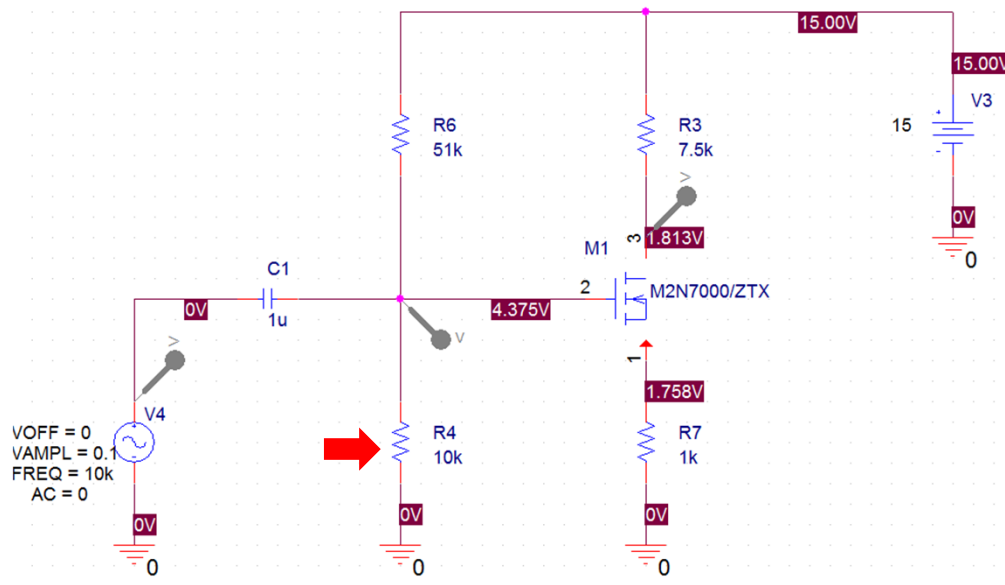


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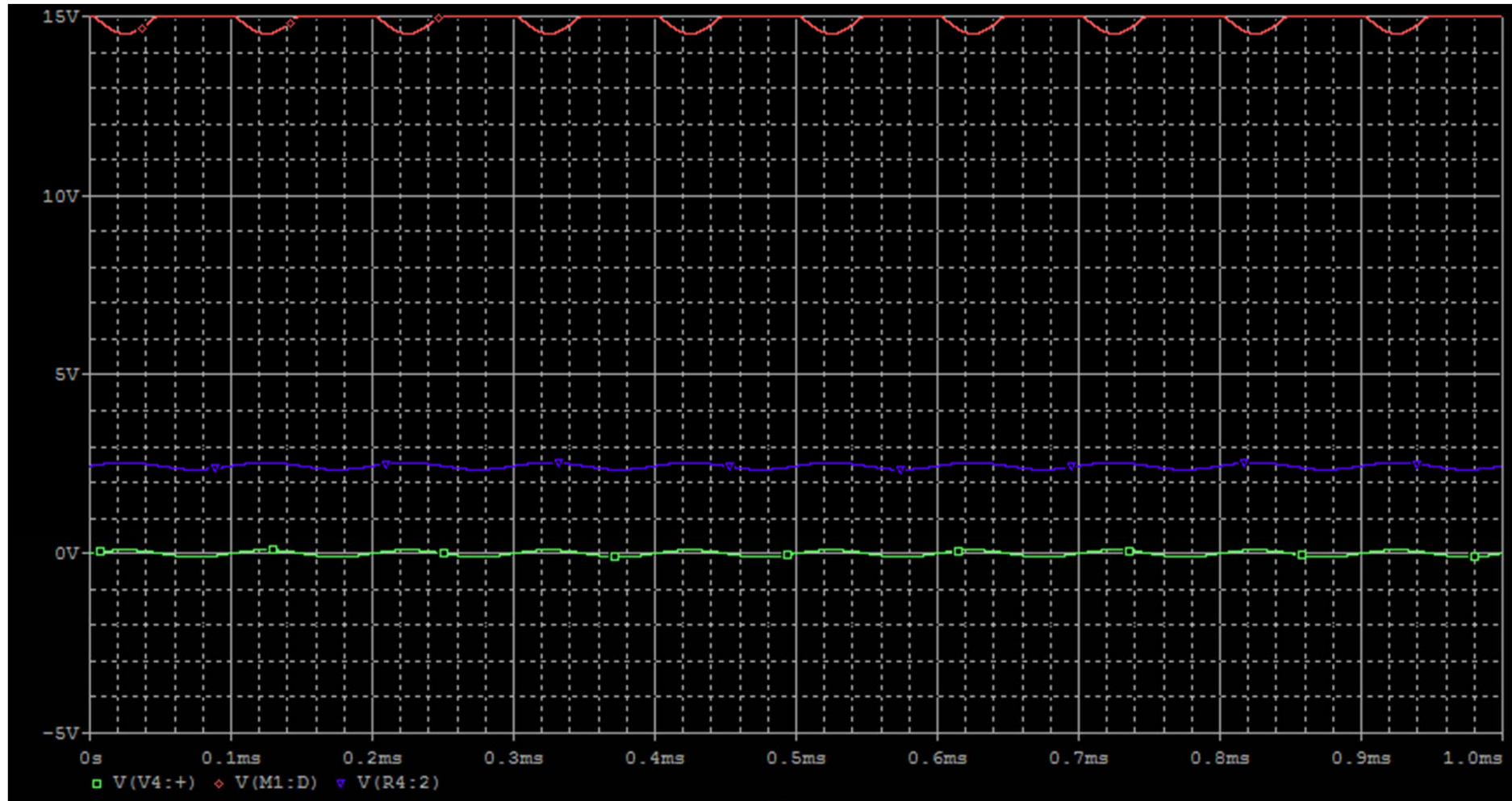
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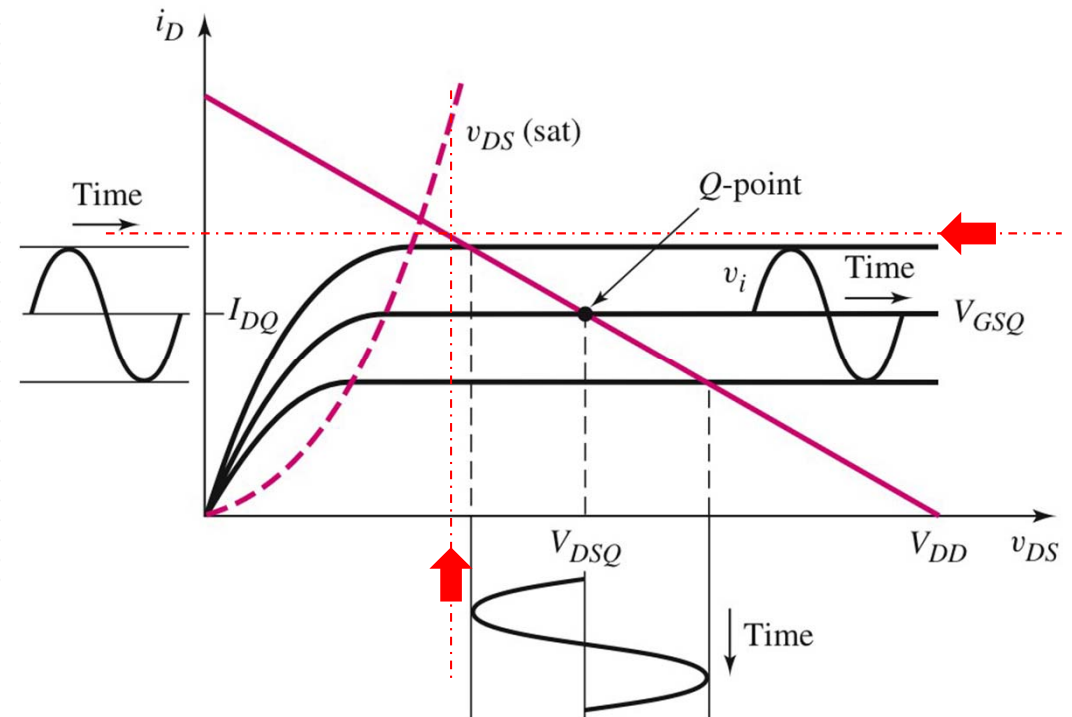
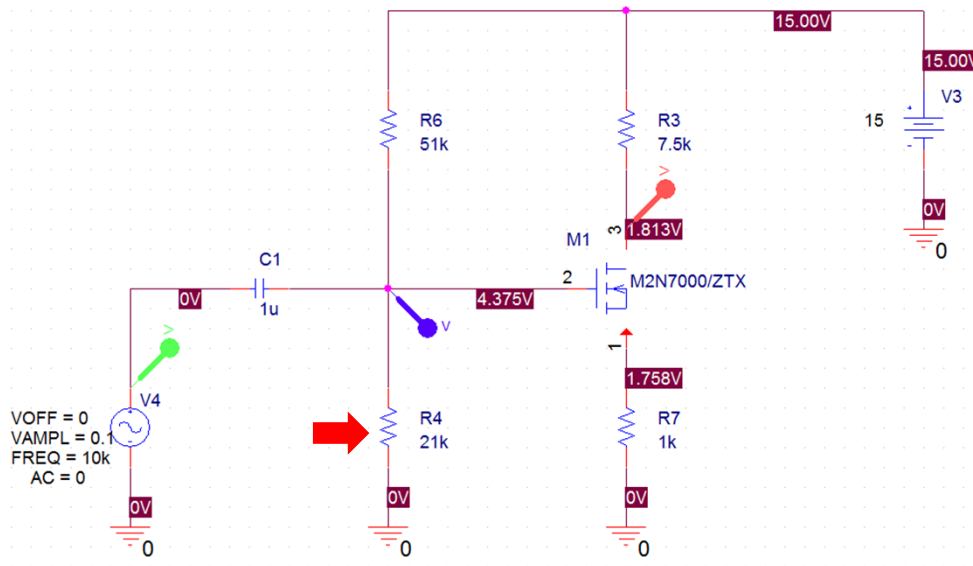


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