Overview

DRAM manufacturers use a number of different performance specifications to describe the speed and competitiveness of their products. Although useful for comparing the offerings of the various manufacturers, the importance of any one of the performance numbers depends a great deal on the design of the system in which the DRAM will be used. This document describes the most commonly quoted performance numbers.

Access Times

The performance figures that carry the most importance are the access times and cycle times for the various DRAM functions. Access times are defined in relation to a specific signal or event and are the maximum delays from the event to achieving data access. The most frequently quoted are Random access (t_{RAC}), and Column or Page access (t_{CAC}).

Random Access (t_{RAC})

t_{RAC} is the time required to read any random single memory cell on a DRAM. The t_{RAC} value quoted in the memory specification is the maximum amount of time required, after $\overline{RAS}$ goes low, to select a row and a column address on the DRAM, sense the charge on the selected memory cell, and send that information to the data output. To achieve t_{RAC}, the system designer must ensure that all the timings and delays shown in the memory specification are met.

Although t_{RAC} is one of the most widely quoted performance benchmarks for DRAMs, its importance to the user varies dramatically. For example, an engineer who designs a system that always selects random addresses will find t_{RAC} the most important measure of DRAM performance for his system. If the development engineer designs the system to read large blocks of data using the Fast Page Mode (FPM) feature, the importance of t_{RAC} will be much less.

Column or Page Access (t_{CAC})

t_{CAC} is the time required to get data at the output after $\overline{CAS}$ goes low, including the selection of the column address, sensing the stored signal, and transferring the data to the output. The maximum t_{CAC} shown in the memory specification is the basis for FPM and EDO (Extended Data Out Mode) performance rates.

Cycle Time

Cycle time is a measure of the overall data rate: the time required to perform the operation (a read or a write), plus any recovery time needed before the next operation can begin. Cycle time is arguably the most important measure of DRAM performance. There are cycle times associated with each type of memory read and write function: single cycle (random access), FPM , EDO, Read-Modify-Write, and so on.

Random Access Cycle Time (t_{RC})

t_{RC} is the cycle time associated with single cycle (random access). The minimum t_{RC} is the sum of the minimum amount of time $\overline{RAS}$ is required to be low to read from or write to a memory location (t_{RAS}), the minimum $\overline{RAS}$ precharge or recovery time (t_{RP}), and the time required for $\overline{RAS}$ to switch from high to low and, later, from low to high. The minimum cycle time is important in cases when multiple random accesses must occur in rapid succession, since the cycle time specifies the minimum amount of time required between random accesses.

Fast Page Cycle Time (t_{PC})

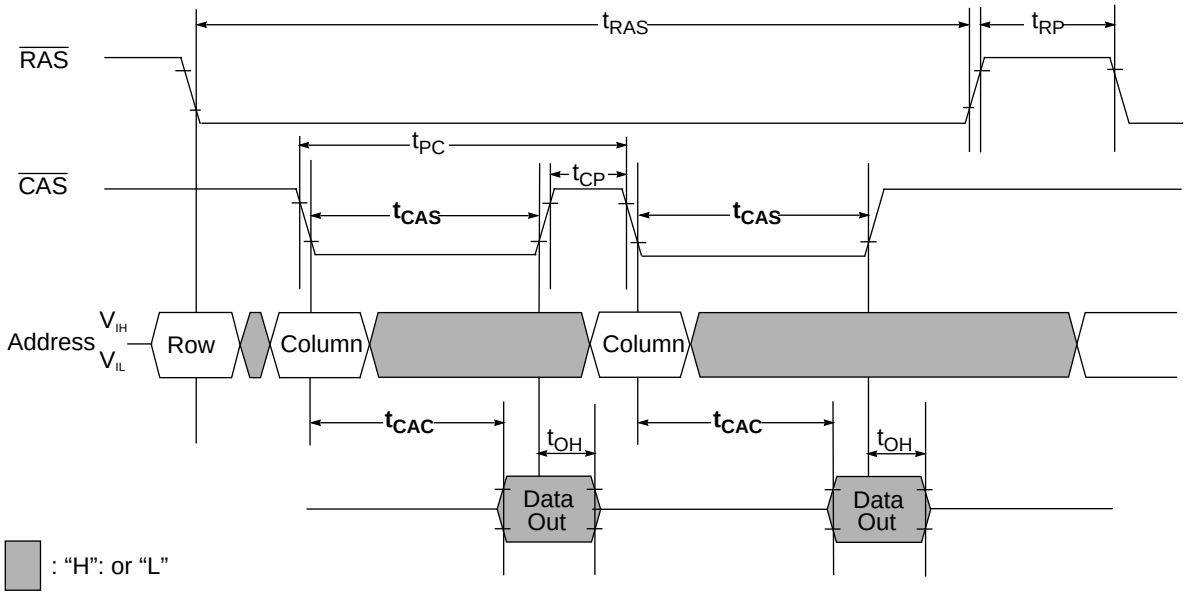
In many memory applications, data is read from or written to logically sequential memory locations, such as all of the locations on a row or page. Fast Page Mode permits the designer to take advantage of this fact, reading or writing the cells in a row without selecting a new row address for each memory location accessed.

t_{PC} is the time required to read or write a memory location on a page plus any recovery time needed to prepare the memory chip's circuits for the next read or write operation. The Fast Page Cycle begins when $\overline{CAS}$ is going low and ends when the minimum $\overline{CAS}$ precharge time (t_{CP}) has elapsed. The t_{CAS} portion ($\overline{CAS}$ low) of this cycle needs to be sufficient to allow data to be accessed. Since $\overline{CAS}$ going high initiates the end of the access in FPM, t_{CAS} must be equal to or greater than the time required to access the data (t_{CAC}). Otherwise, data would not become available.

With FPM, it should be noted that the first memory location accessed on a page requires the same amount of time as a standard random access. Once the first location has been accessed, only the column address changes and only $\overline{CAS}$ is cycled.

Figure 1 is a simplified Fast Page Mode read cycle that emphasizes three elements: t_{PC}, t_{CAS}, and t_{CAC}. Please refer to a datasheet to find a complete timing diagram of a Fast Page Mode read cycle.

Figure 1: Simplified Fast Page Mode Read



Note:
$t_{CAS} \geq t_{CAC}$

Extended Data Out (t_{HPC})

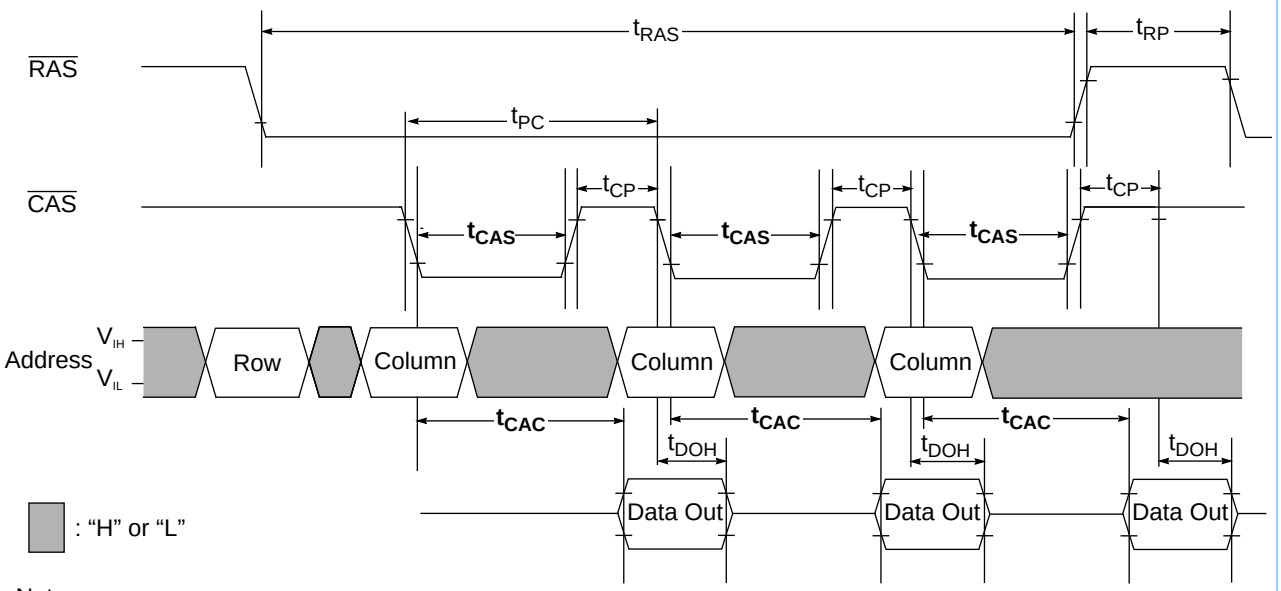
Extended Data Out (EDO), also called Hyper Page Mode (HPM), was developed to further decrease the amount of time required to read or write consecutive memory locations on a page.

With EDO, $\overline{CAS}$ going high does not initiate the end of the data access as it did with FPM. The memory output drivers have been redesigned to permit them to remain active when $\overline{CAS}$ is transitioned to a high level. This allows for the setup of the next address while data for the current data access is being maintained. The result is that t_{CAS} can now be less than t_{CAC}, reducing the overall cycle (t_{CAS} + t_{CP} + transition times). Otherwise, FP and EDO DRAMS function similarly.

Figure 2 is a simplified Extended Data Out read cycle that emphasizes t_{PC}, t_{CAS}, and t_{CAC}. Please refer to a datasheet to find a complete timing diagram of an EDO read cycle.

See the Applications Note "EDO (Hyper Page Mode)" for more information on Fast Page Mode and Hyper Page Mode operations.

Figure 2. Simplified EDO Mode Read



Notes:
1. $t_{CAS} < t_{CAC}$.
2. In the complete timing diagrams you will find in IBM’s datasheets, t_{CAS} is labeled t_{HCAS} and t_{PC} is labeled t_{HPC}.

SDRAM -- Burst Mode

The Synchronous DRAM offers a burst mode with a burst cycle time that is considerably faster than the cycle time associated with FPM or EDO Mode operation. SDRAMs use a self incrementing counter and a mode register to determine the column address sequence after the first memory location accessed on a page. Having predetermined addresses allows the DRAM operations to be performed faster (after the first access) since the time to set up subsequent column addresses in the external timing is removed.

The combination of this burst capability with the use of a clocked interface and multiple bank architecture produces the improved cycle time. It should be noted that random access (t_{RAC}) and other normal operations on the SDRAM are no faster than other DRAMs.

For applications that usually require streams of data from one or more pages on the DRAM, this feature can provide a performance advantage. For slower

applications (those in which the Fast Page Cycle time or Extended Data Out Cycle time are sufficient), or for applications that require frequent random accesses, the SDRAM's burst mode of operation provide little additional benefit over conventional DRAMs.

See the Applications Note "Synchronous DRAMs: The DRAM of the Future" for more information about SDRAM performance and operation.

Read-Modify-Write Cycle Time

Read-Modify-Write is a special function that permits the system to read the data in a memory location and then write data to that same location within a single memory cycle. Because the row and column addresses for the read operation and the write operation are the same, they must only be selected once. The Read-Modify-Write cycle time is the amount of time required to select a row and a column, read the data from the memory location, write new data to the same location, then end the operation and prepare for the next memory operation. The overall time required is usually longer than the standard $\overline{RAS}$ cycle time (t_{RC}), but considerably shorter than the time required to perform a standard read operation followed by a write operation. For applications that routinely read and write back data to the same address, this feature can improve system performance.

For more information contact your IBM Microelectronics sales representative or
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