Computer Organization and Architecture Laboratory

ISA DESIGN

Experiment: Design and Synthesize a 32-bit Processor using Verilog

GROUP 65

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INSTRUCTIONS:

R TYPE

OPCODE	rs	rt	rd	Don't care	function
5 bits	4 bits	4 bits	4 bits	10 bits	5 bits

Instruction	Opcode	Function
ADD	00000	00000
SUB	00000	00001
AND	00000	00010
OR	00000	00011
XOR	00000	00100
NOR	00000	00101
NOT	00000	00110
SL	00000	00111
SRL	00000	01000
SRA	00000	01001
INC	00000	01010
DEC	00000	01011
SLT	00000	01100
SGT	00000	01101
HAM	00000	01110
MOVE	00000	01111
CMOV	00000	10000

I TYPE

OPCODE	rs	rd	Immediate
4 bits	5 bits	5 bits	18 bits

Instruction	Opcode
ADDI	00001

SUBI	00010
ANDI	00011
ORI	00100
XORI	00101
NORI	00110
NOTI	00111
SLAI	01000
SRLI	01001
SRAI	01010
SLTI	01011
SGTI	01100
HAMI	01101
LD	01110
ST	01111
BMI	10000
BPL	10001
BZ	10010
LUI	10011

J TYPE

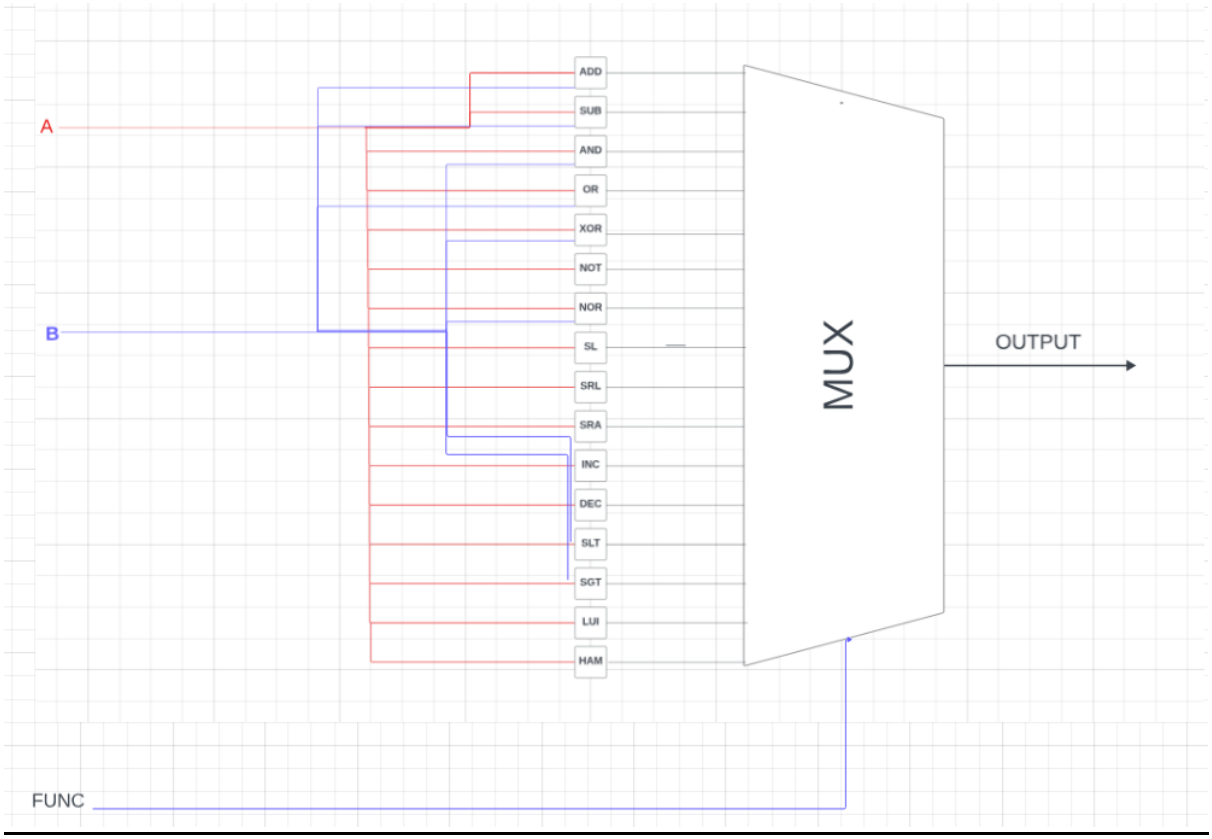
OPCODE	Immediate
5 bits	27 bits

Instruction	Opcode
BR	10100
HALT	10101
NOP	10110

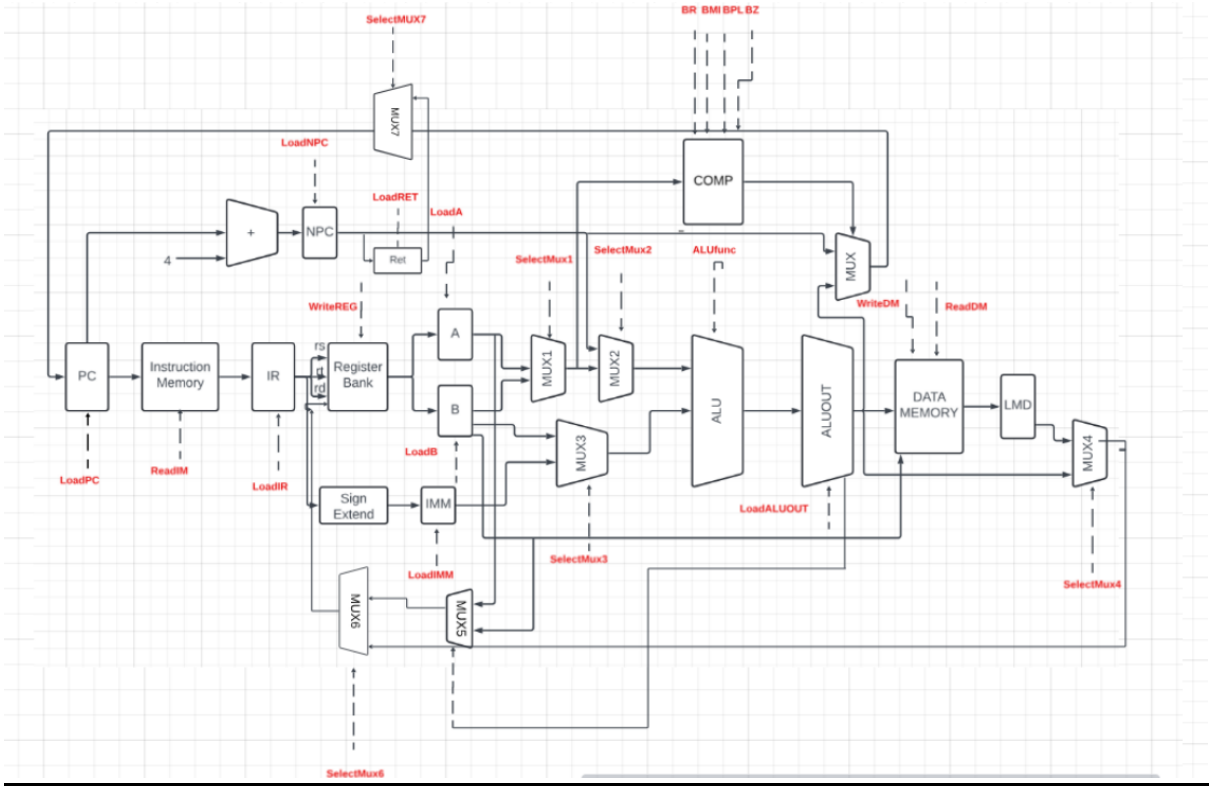
Assumptions :

1) The stack register is assumed to be in the Register Bank.
2) Instruction Memory and Data Memory are separate i.e. Harvard Architecture.

ALU Design



Data Path and Control Design



Control Signals

- LoadPC
- ReadIM
- LoadNPC
- LoadA
- LoadB
- LoadIR
- LoadIMM
- ALUfunc
- ReadDM
- WriteDM
- LoadLMD
- SelectMUX1
- SelectMUX2
- SelectMUX3
- SelectMUX4

- SelectMUX6
- WMFC
- LoadRet
- BR
- BMI
- BPL
- BZ

Microroutine specifications

Link : COAEX.xlsx