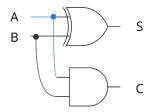


2. This diagram shows the logic circuit for a **half** adder.

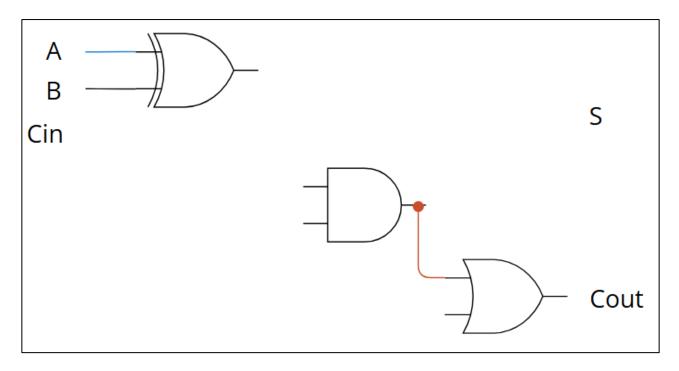


Complete the truth table for this half adder circuit.

Α	В	S	C (Out)
0	0		
0	1		
1	0		
1	1		

[4]

2. The diagram below has missing components of a logic circuit for a full adder. Complete the missing components for a full adder circuit.



i. Complete the table for a full adder circuit.

[5]





ii. Complete the truth table for the full adder circuit

Inp	uts	Outputs		
А	В	Cin	Cout	S
0	0			
0	0			
0	1			
0	1			
1	0			
1	0			
1	1			
1	1			

[3]

END OF QUESTION PAPER





Mark scheme

Que	stion		Marks	Guidance			
		1 mark for each o					
		А	В	s	С		
1		0	0	0	0	4	
-		0	1	1	0		
		1	0	1	0		
		1	1	0	1		
2	I	• 1 mark for • 1 mark for	3				





			Inputs			Outputs				
			Α	В	Cin	Cout	S			
			0	0	0	0	0			
			0	0	1	0	1			
			0	1	0	0	1			
			0	0 1 1 1 0						
	ii	ii	1	0	0	0	1		3	
			1 0 1 1	1	0					
			1	1	0	1	0			
			1	1	1	1	1			
			 1 mark for correctly filling out Cin column 1 mark for correctly filling out Cout Column 1 mark for correctly filling out S column 							
			Total						10	

