CSc.111-2074 ✡

Tribhuvan University
Institute of Science and Technology
2074

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Bachelor Level / First Year/ First Semester/ Science
Computer Science and Information Technology (CSc. 111)
(Digital Logic)

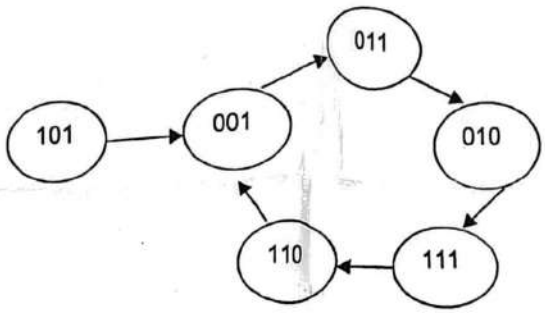
Full Marks: 60
Pass Marks: 24
Time: 3 hours.

Candidates are required to give their answers in their own words as for as practicable.
The figures in the margin indicate full marks.

Attempt any two questions: (2×10=20)

1. Implement the following function $F = \sum (0, 3, 5, 6, 7)$ using
   (a) Decoder
   (b) Multiplexer
   (c) PLA

2. Differentiate between PAL and PLA. Design a counter as shown in the state diagram below



3. Draw a block diagram, truth table and logic circuit of 1*16 Demultiplexer and explain its working principle.

Attempt any eight questions: (8×5=40)

4. Perform the arithmetic operation (+42)+(-13) and (-42)-(-13) in binary using the signed -2's-complement representation for negative numbers.

5. Express the complement of the following function in sum of minterms.
   $F(A, B, C, D) = \sum(0, 2, 6, 11, 13, 14)$

6. Reduce the following function using k-map
   $F = wxy + yz + xy'z + x'y$

7. Design a combinational circuit with three inputs and six outputs. The output binary number should be the square of the input binary number.

8. Design a 5 × 32 decoder with four 3 × 8 decoder with enable and one 2 × 4 decoder. Use block diagrams only.

9. Design and explain the Decimal adder with truth table and suitable diagram.

10. Explain shift register with parallel load. Highlight on its practical implications.

11. Explain master slave J-K flipflop.

12. Write short notes on **(any two)**:
   (a) State diagram
   (b) De-Morgan's theorem
   (c) TTL