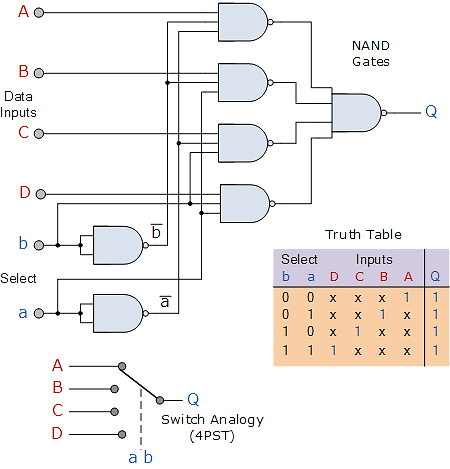
**4-to-1 Channel Multiplexer using Universal gate**



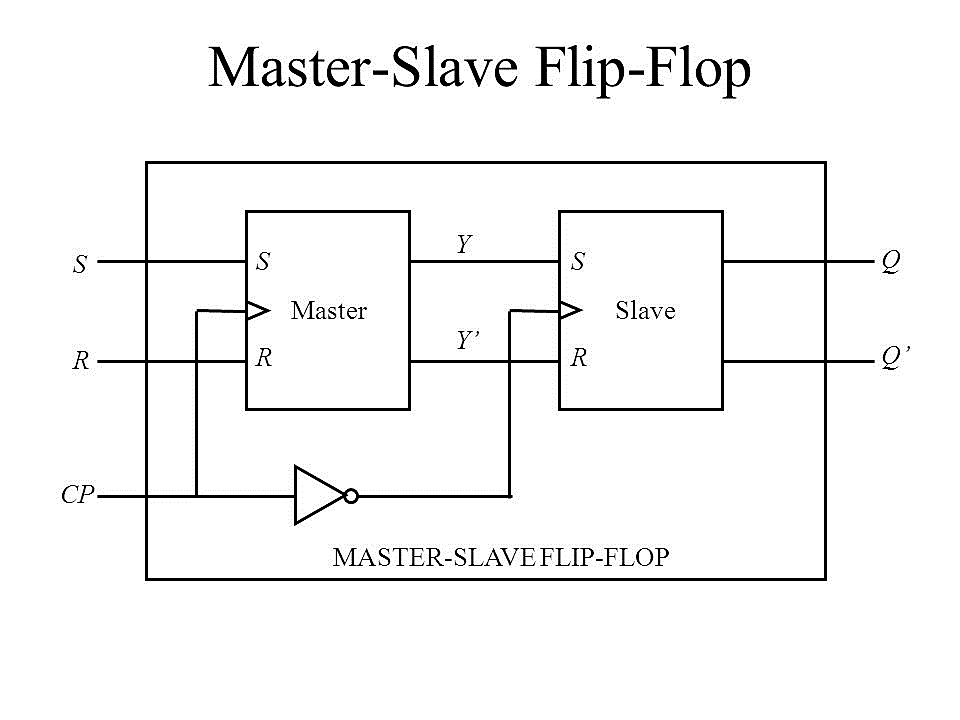
The Boolean expression for this 4-to-1 **Multiplexer** above with inputs A to D and data select lines a, b is given as:

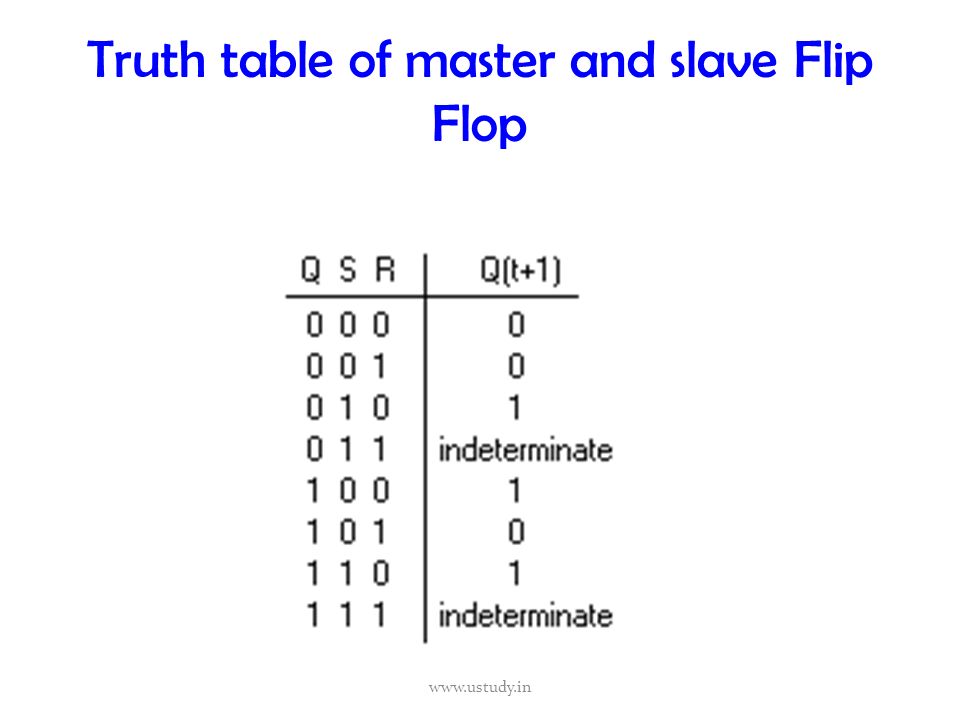
Q = a’b’A + ab’B + a’bC + abD

In this example at any one instant in time only ONE of the four analogue switches is closed, connecting only one of the input lines A to D to the single output at Q. As to which switch is closed depends upon the addressing input code on lines “a” and “b“, so for this example to select input B to the output at Q, the binary input address would need to be “a” = logic “1” and “b” = logic “0”.

**SR Master Slave Flip Flop**

A master-slave flip-flop is normally constructed from two flip-flops: one is the Master flip-flop and the other is the Slave. In addition to these two flip-flops, the circuit also includes an inverter. The inverter is connected to clock pulse in such a way that the inverted CP is given to the slave flip-flop. For example, if the CP=0 for a master flip-flop, then the output of the inverter is 1, and this value is assigned to the slave flip-flop. In other words if CP=0 for a master flip-flop, then CP=1 for a slave flip-flop.

A master-slave flip flop can be constructed using any type of flip-flop which forms a combination with a clocked SR flip-flop, and with an inverter as slave circuit.



*Fig (a): SR Master Slave Flip Flop Fig (b): Truth Table*

An SR master-slave flip-flop consists of two SR flip-flops; one is the master flip-flop and the other a slave. The inverted CP is given to the slave flip-flop. Now when CP=0, the master flip-flop is disabled. So the external inputs R and S of the master flip-flop will not affect the circuit until CP goes to 1. The inverter output goes to 1 and it enables the slave flip-flop. The output Q=Y and Q’=Y’.

When CP=1, the master flip-flop is enabled and the slave flip-flop remains isolated from the circuit until CP goes back to 0. Now Y and Y’ depends on the external inputs R and S of the master flip-flop.

Assume that the flip-flop is in a clear state and no clock pulse is applied to the circuit. The external inputs given are S=1 and R=0. This input will not affect the state of the system until the CP=1. Now the next clock pulse applied should change the state to SET state (S=1, R=0). During the clock pulse transition from 0 to 1, the master flip-flop goes to set state and changes the output Y to 1. However this does not affect the output of the system since the slave flip-flop is isolated from the system (CP=0 for slave). So no change is observed at the output of the system.

When the CP returns to 0, the master flip-flop is disabled while the slave is enabled. So the information from the master is allowed to pass through to the slave. Since Y=1, this changes the output Q to 1.

**Note:** *The Truth table for SR master slave flip flop is same as that of Clocked SR flip flop.*