

Module Computer Fundamentals (COMP1027 (CSF) (Semester 1)

Module Convenor(s) Fresa Chambesa 5 1 1 10 CS 7 7 F 7 F 7 F

**Assessment Name** 

Coursework 1

Weight

40%

rk has THREE parts, as detailed below:

focuses on Elementary Logic Gates
focuses on Combinatorial & Sequential Circuits
focuses on The Hack Computer

#### **Important Notes**

We Claroup will be assessed via the peer assessment.

You <u>MUST</u> maintain the provided folder structures. All files for Parts 1, 2 and 3 will be under THREE folders. Three additional sub-folders will be added for part 3 to reflect sections 3.1, 3.2 and 3.3. Please be observant to this and abide to

# Assignment Provided zip file Phell as its folder an Eulp-folder structure and file names. Files to Download

CW1-Files.zip provides all the skeleton .hdl and .asm (as well as most of the related

### Email: tuttorcs@163.com

1. Download the zip file, from the "Coursework 1" area on Moodle.

**Description and Deliverable(s)** 

Extract the files and fill in the required HDL and Assembly codes, as per the
detailed instructions given in this assessment sheet.

MAINTAIN the same folder structure, file name, and all test and compare files when you submit. You can add any additional files you may need to get your submissions working correctly.

## https://tutofg.Sfg.Gs.Sheementary Logic Gates

Tessa is a talented baker who wishes to open her own café in 2025. In order to realise her dreams, she needs to secure a location whereby her café can be open, purchased relevant furniture, enlist several helpers, and prepare a set of delightful choices for the customers to choose from. For the short-term, she will be happy to successfully fulfil two to three of the four conditions, namely a location **and** furniture **or** menu.

- Generate a truth table to represent the conditions that Tessa needs to fulfil
  to ensure her café is successfully operational by February 2025. Please
  represent location, furniture, helpers and menu as A, B, C, and D in your
  truth table. Output should be represented as F.
- Based on the truth table in (1), write out the pre-simplified expression followed by the simplified expression using the Basic Identities of Boolean Algebra in Figure 1. You are required to show your working details (Boolean Function, Boolean Expressions, Simplifications, ..., etc.) in the Truth Table and Simplification.docx.



	Identity Name	AND Form	QR Form	
程序代写	Identity Law	16 T	4 1	
在ハーレコ	Null (or Dominance) Law	DX=00	11.X4	
	Idempotent Law	XX = X	X+X=X	
	Inverse Law	$x\overline{x} = 0$	$X + \overline{X} = 1$	
	Commutative Law	xy = yx	X+y=y+X	
	Associative Law	(xy)z = x(yz)	(x+y)+z=x+(y+z)	
	Distributive Law	X+yZ = (X+y)(X+Z)	X(y+z) = Xy+Xz	
	Absorption Law	X(X+Y) = X	X+XY=X	
	DeMorgan's Law	$(\overline{X}\overline{Y}) = \overline{X} + \overline{Y}$	$(\overline{X+Y}) = \overline{X}\overline{Y}$	
	Double Complement Law	$\overline{\overline{X}} =$	X	
Extracted from: L. Null, L. and J. Lobur, The essentials of computer organisation and architecture, Jones & Barriett Publishers, 2003 (Fig. 1.3, F				

Figure 1

d on your answers in (1) and (2), respectively, implement a Tessa decision chip that prioritise what she needs to address to ensure a timely opening of her café. NOTE: to ensure that your test cases are aligned with our test cases, please only use 1-bit input.

SUBNIZE ON: 60 SWIT TO TO THE TESSA. Hall file. (and all associated testing scripts & compare files) and Truth Table and Simplication.pdf. NOTE: we'll also use our own test versions during marking.

Part 2 focuses on Combinatorial & Sequential Circuits 19 implement an ALU chip (MyALU), of your own design, that computes 20

functions (the 18 functions covered in the lecture, in addition to the X XOR Y and X XNOR Y).

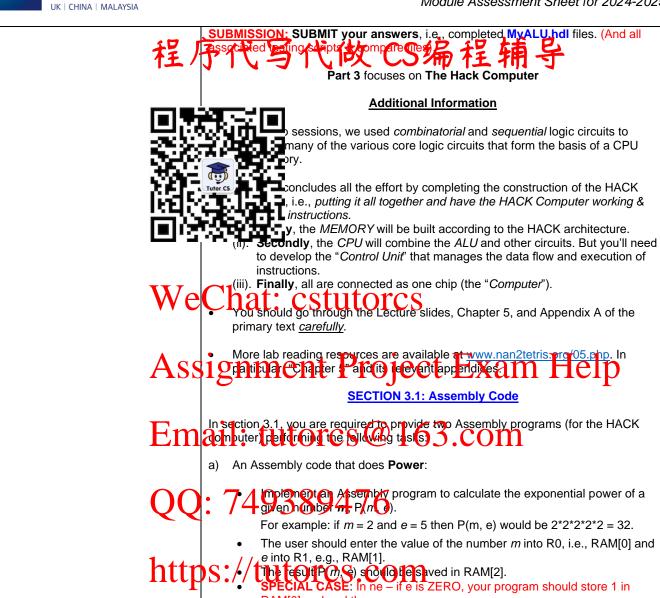
Table 1sh sife Consider Output a partie 120 ed order and the 5 control bits (C4, C3, C2, C1, C0) with some samples of their values (you are required to complete them according to the Decimal values in the left column).

The light specific provided, but you will need to create your .tst and .cmp

**Table 1: MyALU Functions (Output)** 

ttn	Decimal S of Cs	1164rc	C C3	C2	C1	C0	Output
up	300	TUGI U		0	0	0	0
	1						1
	2						-1
	3	0	0	0	1	1	X
	4						Y
	5	0	0	1	0	1	Χ'
	6						Y'
	7						-X
	8						-Y
	9						X+1
	10						Y+1
	11						X-1
	12						Y-1
	13						X+Y
	14						X-Y
	15						Y-X
	16						X AND Y
	17						X OR Y
	18						X XOR Y
	19						X XNOR Y





RAM[0] and end the program.

- An Assembly code that does Factorial:
  - Implement an Assembly program to calculate the factorial of a given number, **n**, F(n). A factorial of a number is given by:

$$F(n) = n*(n-1)*(n-2)*...*2*1$$

- The user should enter the value of the number **n** into **R0**, i.e., **RAM[0]**.
- The factorial result F(n) should be saved in RAM[1].

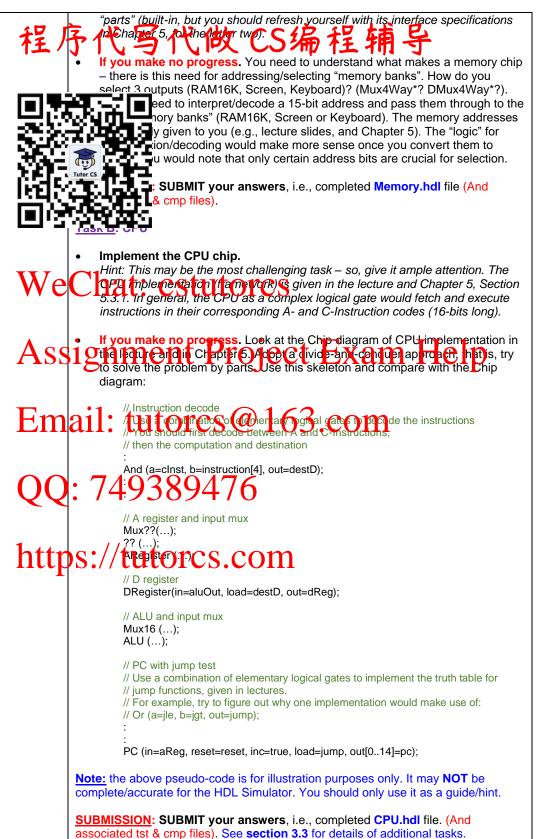
SUBMISSION: SUBMIT your answers, i.e., completed Power.asm & Factorial.asm files. (And associated tst & cmp files).

#### **SECTION 3.2: The HACK Computer**

#### Task A: Memory

Implement the Memory Chip. Hint: The specification for the memory chip is described in the lecture and Chapter 5. Note that you would have to use RAM16K, Screen and Keyboard





Task C: Computer



## 程序 Philip Tring's easy and as a books my hine 程 co 輔导

CPU (inM=??, instruction=??, reset=??, WriteM=??, outM=??, address=??, pc=??);

\_\_Memory (in=??, load=??, address=??, out=??);

32K (address=??, out=??);

ded zip file contains a couple of test files (e.g., ComputerMax, Add, ComputerRect), to test your Computer chip. Make sure to utilise properly test your chip before submission.

SUBMIT your answers, i.e., completed Computer.hdl file. (And & cmp files).

#### **SECTION 3.3: Circuitry Diagram and Justification**

In section 3.2 – task B, you would have designed a circuitry diagram prior to implementing the CPU chip. As such, you are required to submit your full circuit diagram of you CPU into ereptiation, slong with a 2-page summary justifying your circuitry design. Focus should be on part(s) of your CPU that you creatively designed and implemented, which are different to the default design we discussed in the lecture. Within folder PART 3 in the provided zip file contains a Word document Justification.docx) for your padd your justification. Please make sure to fill your lettill e.g., rame and suden(D) according to your justification. NOTE: your justification should not exceed 2 pages - additional pages will incur a 5% marks penalty for each page. You

Emailemission: Survice Survices of the Complete Micuitry Diagram.pdf and Justification.pdf files.

may add **relevant** figures and tables to support your justification.

#### Final Submission Instructions

Each group will have **ONE** submission **ONLY** (performed by *one nominated member of the group*).

We reserve the right to ask all/some students to explain any/all of your submitted work at any time. Failure to explain it properly could affect YOUR mark. / UUCL S. COM

Compress the whole folder structure/tree only (see the provided zip file, for an example). Avoid compressing each individual folder/file. Nested compression will prevent the marking process and could result in marking scripts failing. Should this occur to your submission, your entire coursework 1 mark WILL be awarded a 0%. So, please be careful!

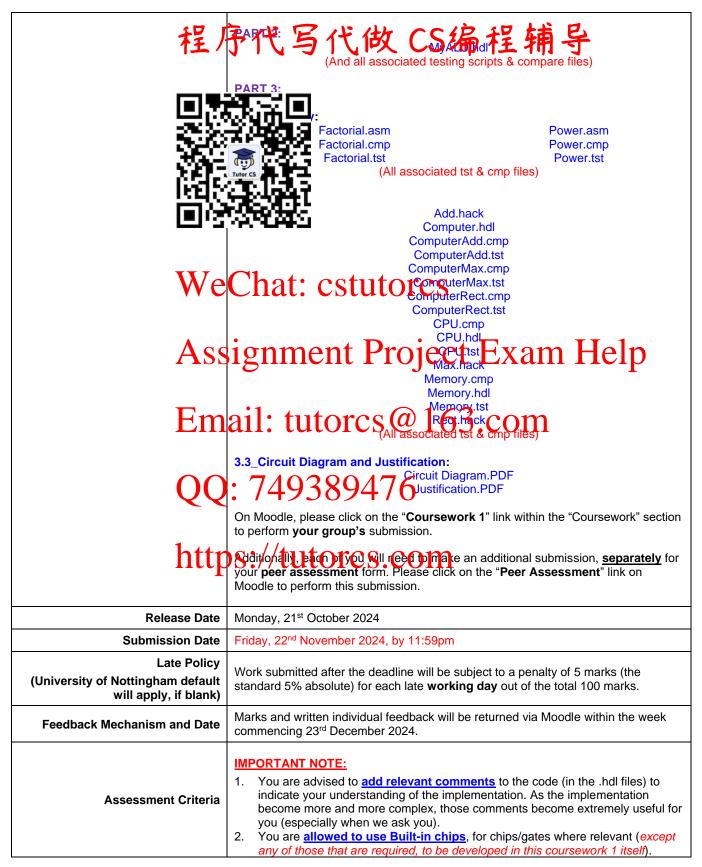
The group submission must be submitted via Moodle as a <u>ZIP</u> archive file. Any other archive file formats WILL result in a penalty of a 5%-mark deduction of your group's overall mark. Within your ZIP archive, it should contain all the requested files (same folder structure as per the downloaded files). Name that ZIP file as CSF-CW1-XXX.zip, where the "XXX" is your Group Number (*i.e.*, 001, 020, 043). Incorrect naming of the ZIP file WILL result in a penalty of a 10%-mark deduction of your group's overall mark. So, your attention to detail is pivotal here.

All the files should have the (**EXACT**) file names, and arranged under the (**EXACT**) subfolder name/structure as detailed below:

#### **PART 1:**

Tessa.hdl Tessa.tst Tessa.cmp
Truth Table and Simplication.PDF







程序 4. 5.	Marking & checks will be done through scripts, which expects specific file name chee specific hards. Will be ultrage room be refore, resulting all chips will be tested through automated testing scripts.  Missing any required file(s), using different formats, naming,, etc. will attract penalty of 10% of your overall mark.  The itted work that explicitly exhibit any cutting corners/plagiarism,, etc.
	in the entire coursework 1 being awarded 0%. It are unable to run will result in 0% being awarded for that task.  nent Breakdown:
160 503   10 505	Correct Truth Table 5 Correct Simplification 5 Chip structure & executes correctly 5
WeC	art 2 (10%):  1 CS LULIO FORSt chip structure & executes correctly  10  art 3:
Assi	1 - Assembly Code (10%):  Same Property of Program Help 5 Factorial Program
	2 - HACK Computer (25%):  11: tutorcs @   1ask A   Memory hall   5
	749389476  Pass "Max" test 5  Pass "Rect" test 5  3 - Circuitry Diagram & Justification (40%):
https	Circuitry Design 15  Justification of Circuitry Design 25  15  Justification of Circuitry Design 25