INTRODUCTION TO MEMORY SYSTEM (I)

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Lecture overview

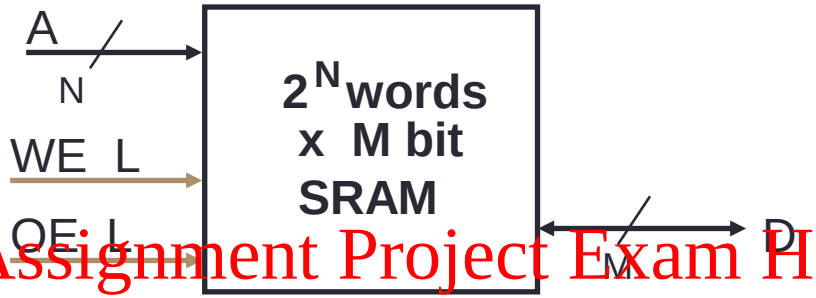
- **Topics**
  - **Memory technology**
    - **SRAM**
    - **DRAM**
    - **DISK**

- **Suggested reading**
  - **H&P Chapter 5.2**

Memory technologies

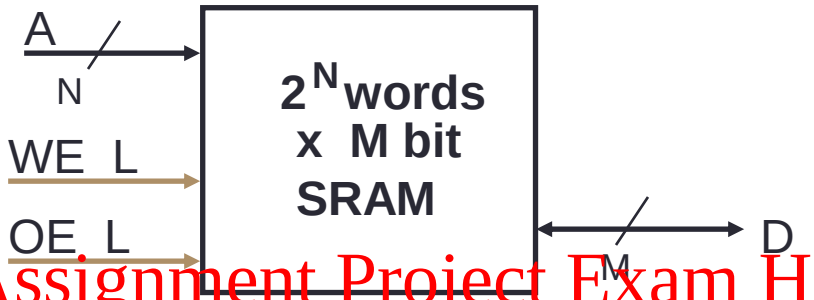
- **Volatile memory**
  - **Power is needed to maintain the stored information**
  - **SRAM:** Static Random Access Memory
    - **Low density, expensive, fast**
    - **Static: content will last "forever"(until power is off)**
  - **DRAM:** Dynamic Random Access Memory
    - **High density, cheap, slow**
    - **Dynamic: need to be "refreshed" regularly**
- **Non-volatile memory**
  - **Data stored will stay even power is off**
    - **Disk**
    - **Flash**

A typical SRAM



- **Write Enable is usually active low (WE_L)**
- **D_{in} and D_{out} are combined to save pins:**
  - **A new control signal, output enable (OE_L) is needed**
    - **When WE_L is asserted (low), OE_L is de-asserted (high)**
      - D serves as the data input pin
    - **When WE_L is de-asserted (High), OE_L is asserted (Low)**
      - D is the data output pin
    - **Both WE_L and OE_L are asserted:**
      - Result is unknown. Not allowed!

A typical SRAM



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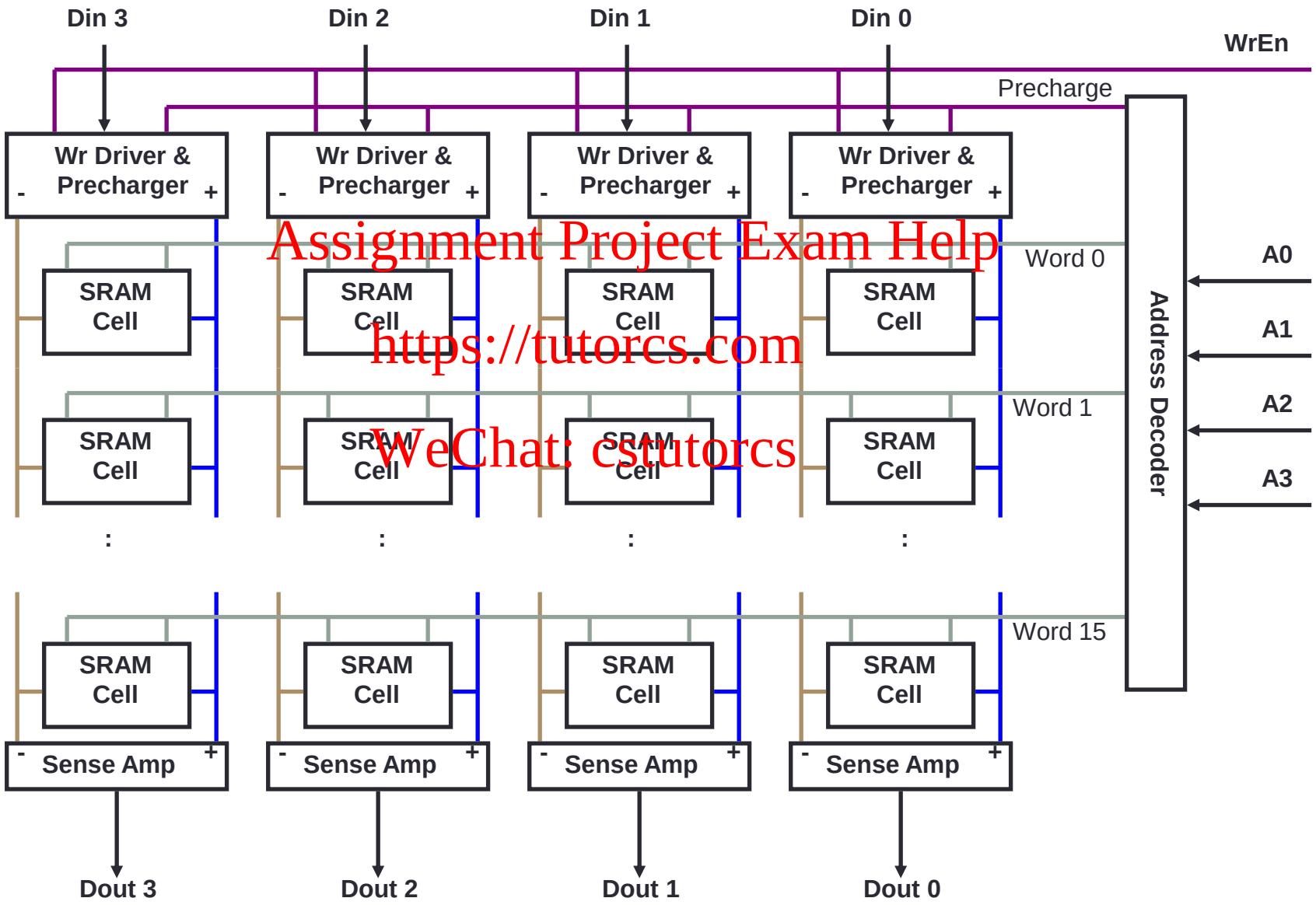
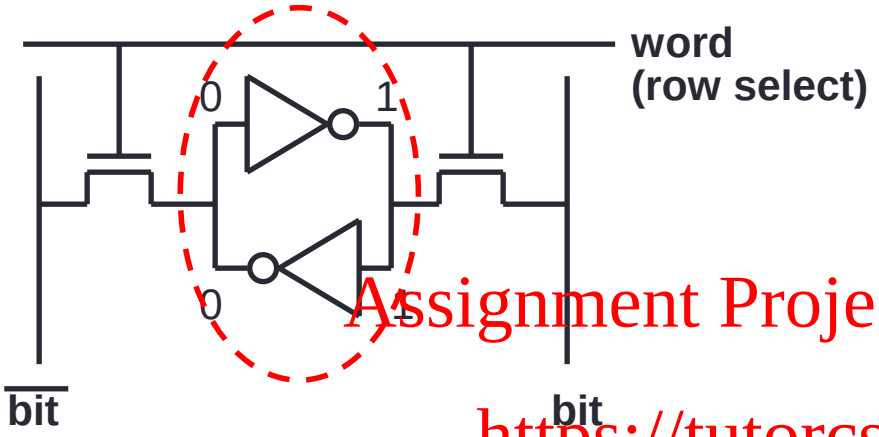
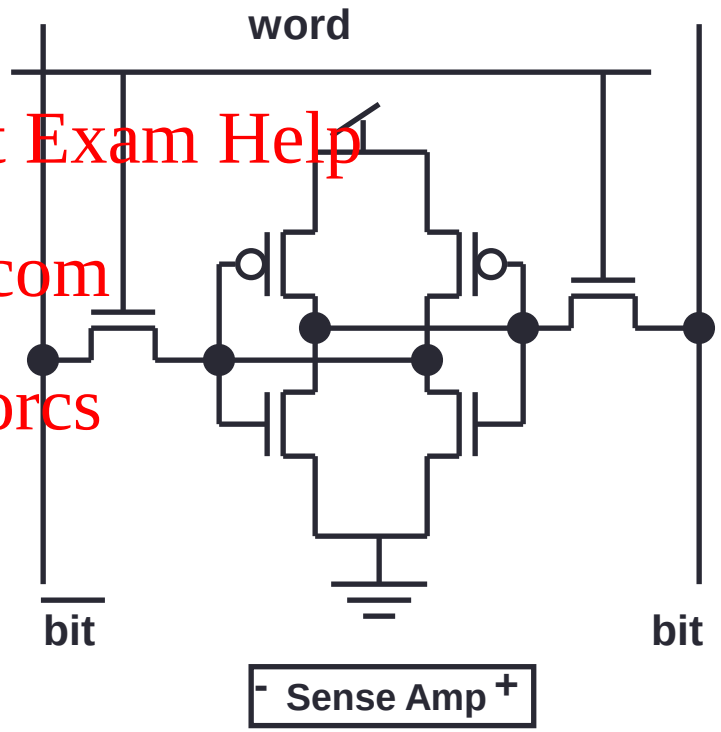
  - **Both WE_L and OE_L are asserted:**
    - Result is unknown. Don't do that!!!

A 16-word x 4-bit SRAM structure



6-transistor SRAM cell





Write:

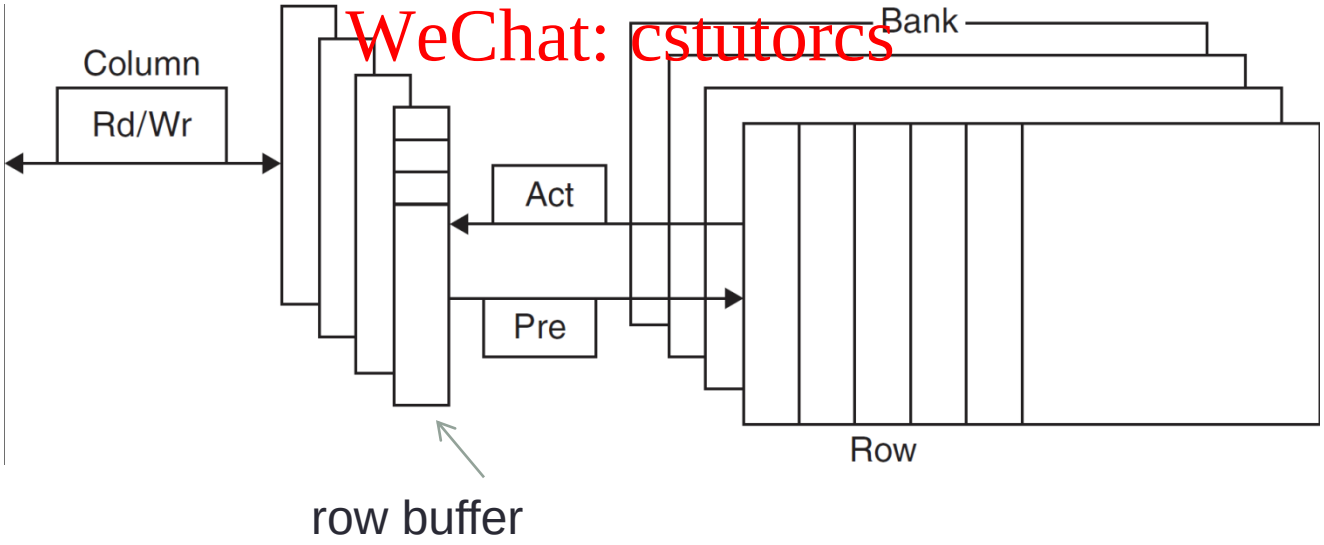
1. Drive bit lines (e.g. $\overline{bit}$=1, bit=0)
2. Select row

Read:

1. Precharge bit and $\overline{bit}$
2. Select row
3. Cell pulls one line low
4. Sense Amp on the column detects the difference between the two bit lines, and has the bit lines charged and discharged with the cell value

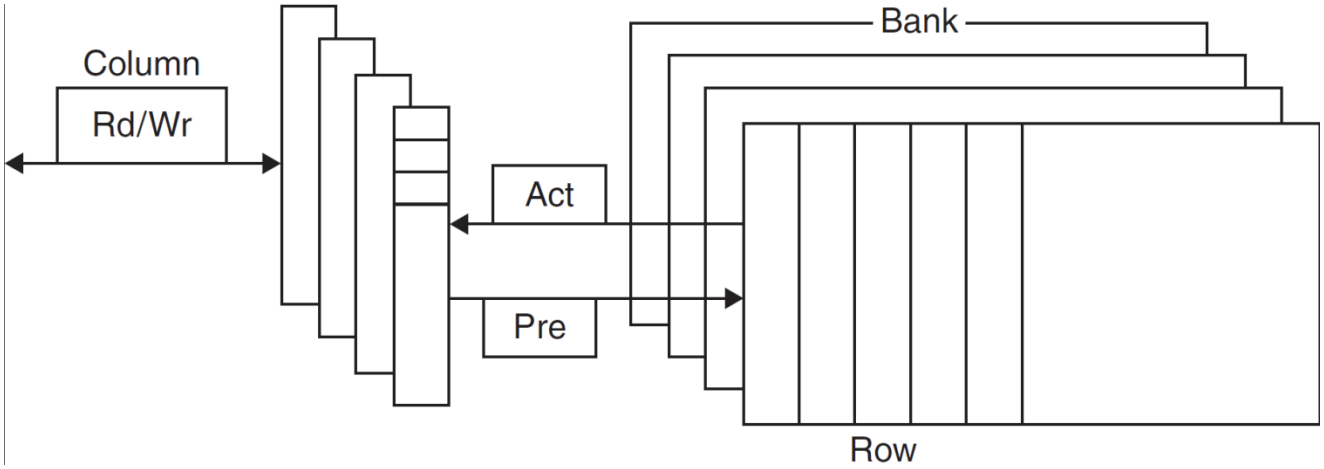
DRAM

- Offers higher capacity than SRAM
- Can be structured with multiple banks
- Each bank contains rows and each row may have multiple word columns

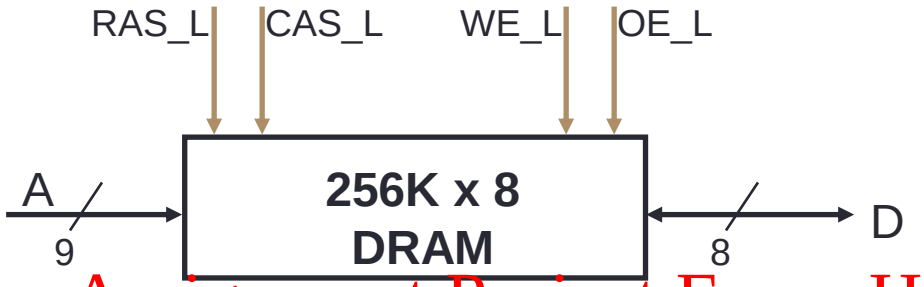


DRAM (cont.)

- **The DRAM interface usually has a separate data bus and command bus. They are shared by the multiple banks**
  - **Data bus: for transferring data to and from memory**
  - **Command bus: for sending commands and addresses.**



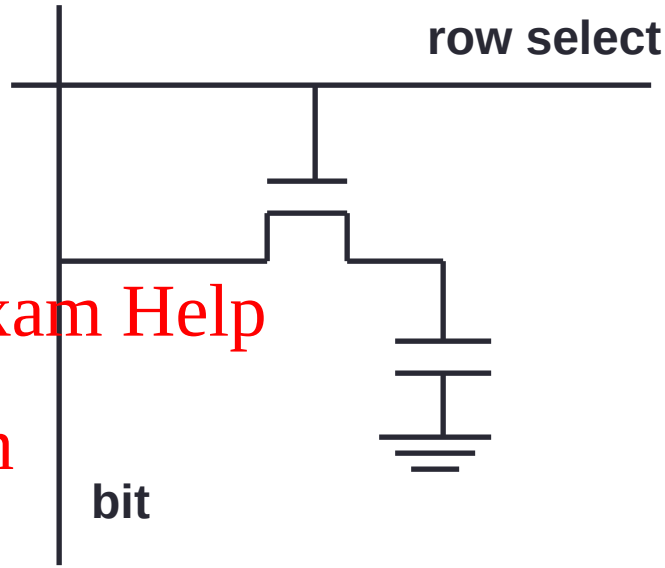
A typical DRAM bank



- Control signals (RAS_L, CAS_L, WE_L, OE_L) are all active low
- D_{in} and D_{out} are combined (D):
  - When WE_L is asserted (low), OE_L is de-asserted (high)
    - D serves as the data input pin
  - When WE_L is de-asserted (high), OE_L is asserted (low)
    - D is the data output pin
- Row and column addresses share the same pins (A)
  - Controlled by row/column address *strobe*
    - RAS_L goes low: input to A is latched in as row address
    - CAS_L goes low: input to A is latched in as column address

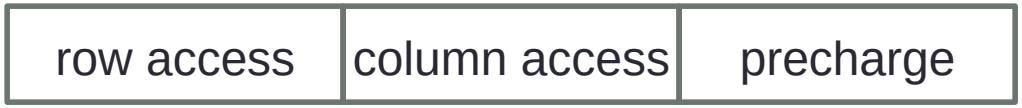
1-transistor DRAM cell

- **Write:**
  1. Drive bit line
  2. Select row
- **Read:**
  1. Precharge bit lines
  2. Select row
  3. Cell and bit lines share charges
  4. Sense (sense amp)
  5. Write: restore the value
- **Refresh**
  - do a dummy read to every cell (in a row)
    - power hungry and performance unwise
  - Usually done by special hardware refresh control component



DRAM access cycle

- DRAM is accessed on a row basis.
- Accessing a memory location (e.g. a word column) follows the following access cycle:
  - Open the row related to the memory location
    - When memory is ready (i.e. the bits lines have been pre-charged)
  - Access the column (read/write)
  - Precharge (bit lines) for next different row access

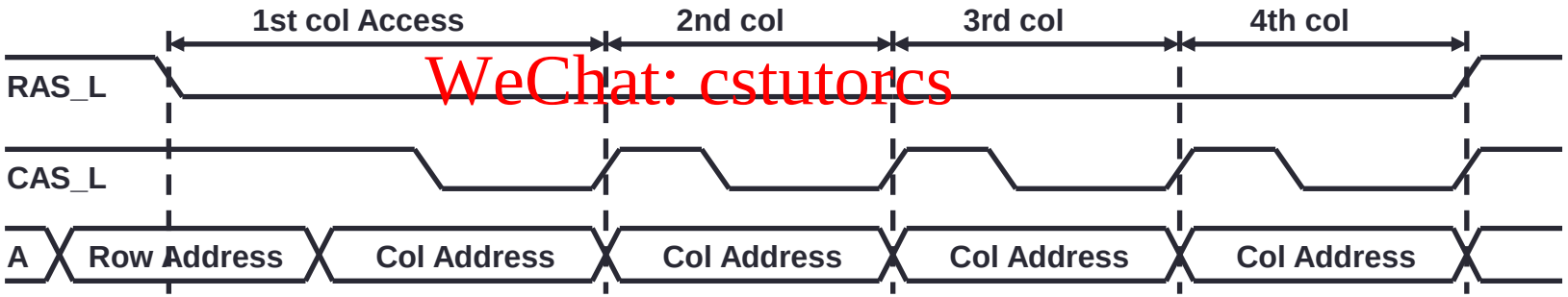


DRAM performance

- The time for a memory access is
  - $T_{rac} + T_{cac} + T_{precharge}$
    - rac: row access
    - cac: column access
- DRAM performance is affected by
  - memory design
  - memory operation control
  - data transfer
- The performance can be improved by
  - Increasing memory data access throughput
  - Increasing data transfer speed over the memory bus.

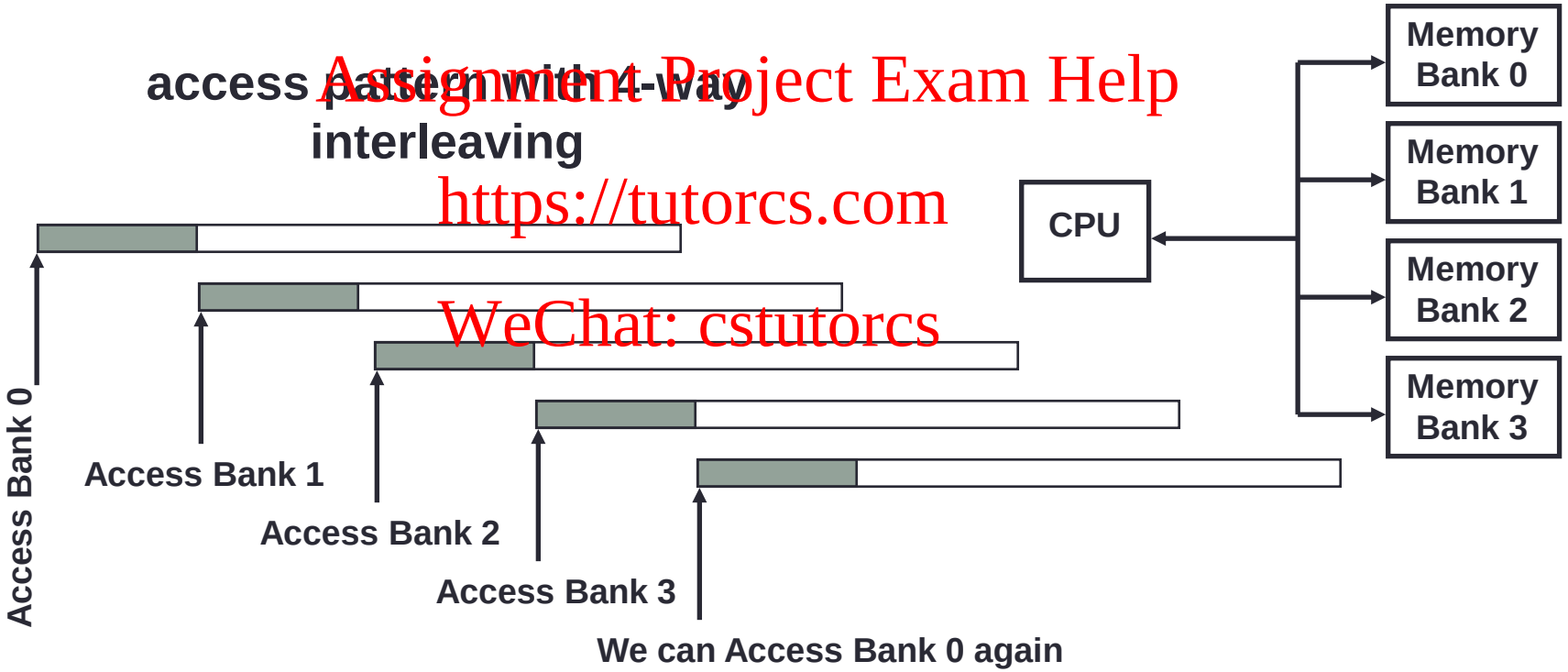
Increasing data throughput (1)

- **Burst mode**
  - **Consecutive accesses without need to send the address of each word in the row**
    - **The time for new access Trac for each word is saved**



Increasing data throughput (2)

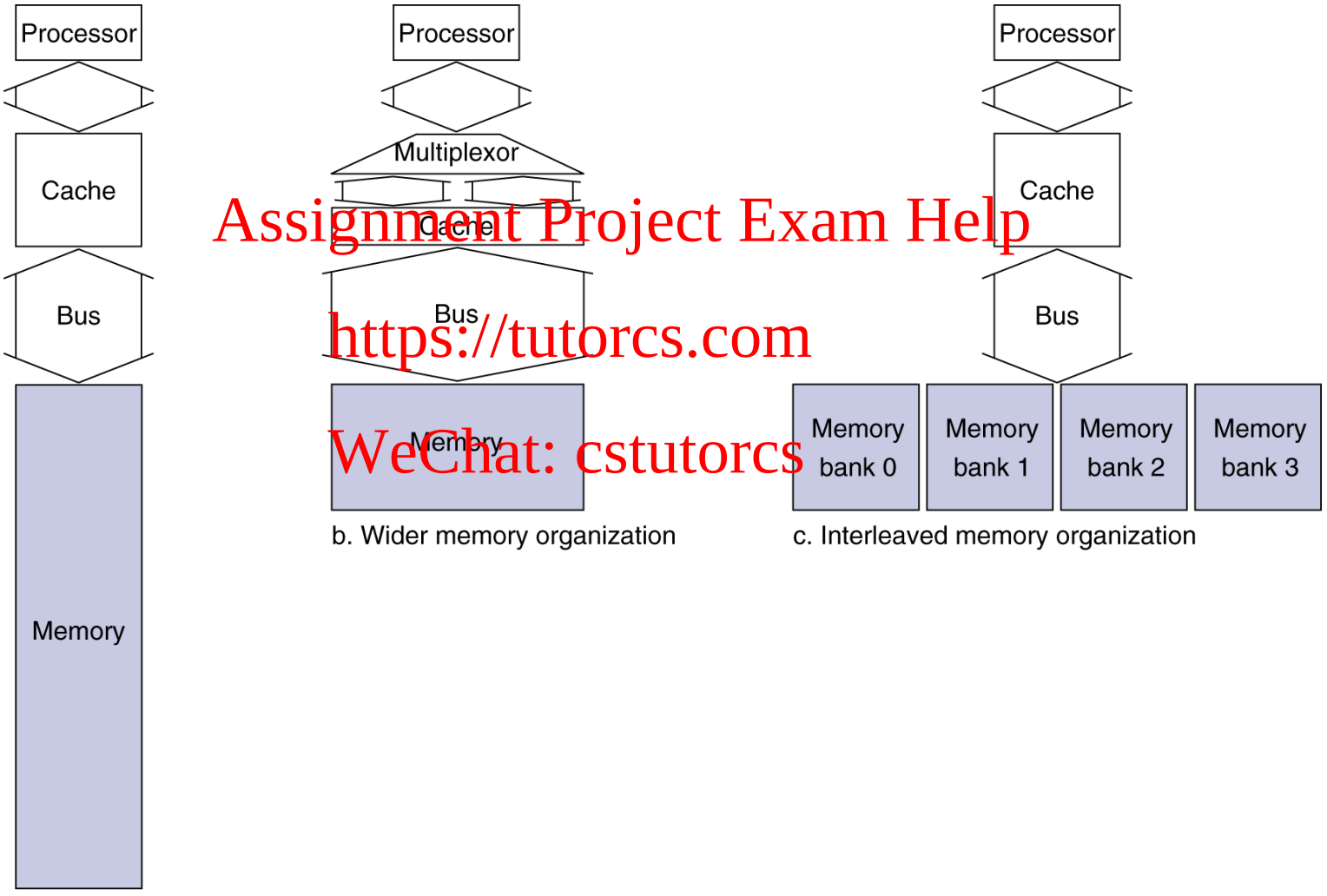
- **Multi-bank interleaved access**



Increasing data throughput (3)

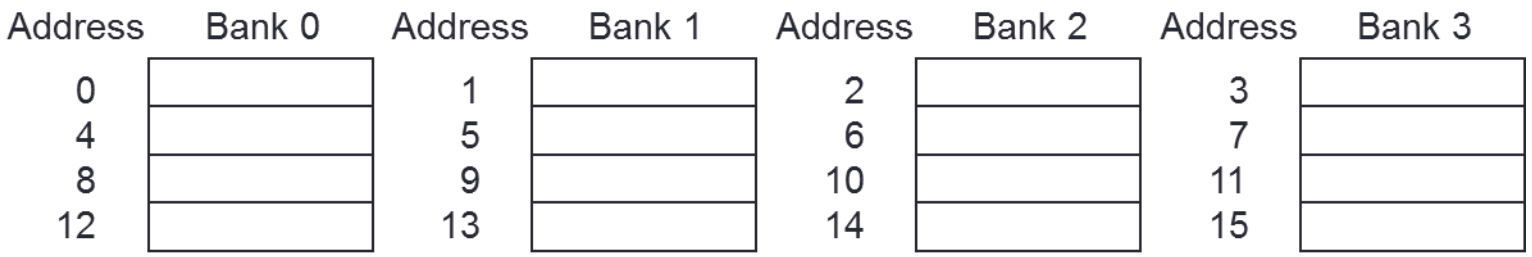
- **Wide memory data bus**
  - **A bus line can transfer multiple words**
  - **See next slide for comparison**

Three memory access organizations



Example

- **For a given memory:**
  - **1 cycle to send address,**
  - **6 cycles to access memory to fetch a word,**
  - **1 cycle to send data**
- **To get a block of 4 words**
  - **Simple Mem:** **= 4 x (1+6+1) = 32 cycles**
  - **Wide Mem:** **= 1 + 6 + 1 = 8 cycles**
  - **Interleaved Mem*:** **= 1 + 6 + 4x1 = 11 cycles**
    - Any limitations?



Increasing data transfer rate

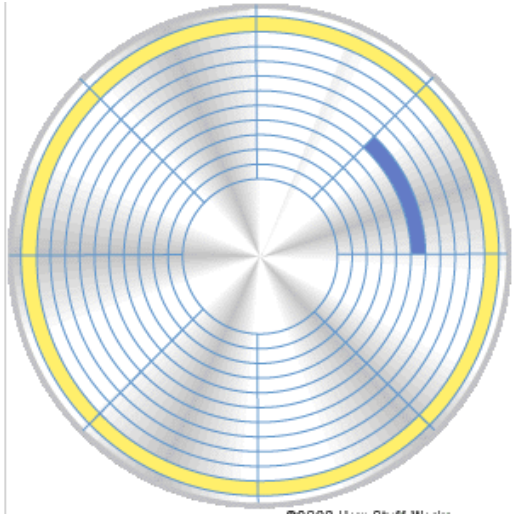
- **Double data rate (DDR) DRAM**
  - **Transfer on rising and falling clock edges**
- **Quad data rate (QDR) DRAM**
  - **Separate DDR input and output ports**

Hard disk drive

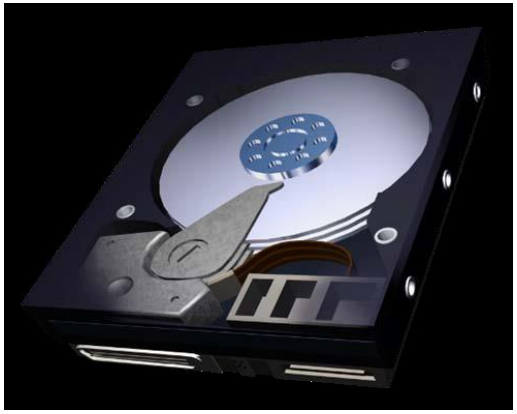
- A hard disk drive (HDD) has one or a set of hard platters
- Platters are circular disks
  - made of a non magnetic material
    - typically aluminium alloy, glass or ceramic
  - coated with a thin layer of magnetic material
    - used to hold data

Hard disk drive (cont.)

- Platters are partitioned into tracks and sectors
  - tracks are concentric circles
  - sectors are pie shaped wedges
- Data is stored digitally in the form of tiny magnetized fields on the platter
  - each field represents a bit
  - each field has two magnetic orientations
    - represent either '0' or '1'



Hard disk drive (cont.)

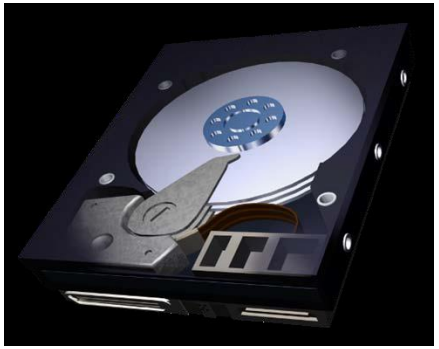


- Platter can spin
  - E.g. at 3600 or 7200 rpm
- The arm for each platter holds the read/write heads
  - able to move the heads from the hub to the edge of drive.
    - E.g. at 50 times/per second.
- To read/write, the head should be placed over the related location.

Hard disk drive (cont.)

- The electronic controller controls
  - the read/write mechanism and
  - the motor that spins the platters.
- The electronic circuits
  - turn bytes into magnetic domains (writing).
  - assemble the magnetic domains on the drive into bytes (reading)

HDD performance



- **There are two ways to measure the performance of a hard disk:**
  - **seek time**
    - **the amount of time between when the processor requests a *file* and when the first byte of the file is sent to the processor. Times between 10 and 20 milliseconds are common.**
  - **Rotational latency**
    - **the time required for the first bit of the data sector pass through the read/write head. Times between 2 to 4 ms are common.**
  - **data rate**
    - **the number of bytes per second that the drive can deliver to CPU. Rates between 5 and 40 megabytes per second are common.**

Seagate Cheetah 15k.4 DISC Drive

Geometry attribute	Value
Platters	4
Surfaces (read/write heads)	8
Surface diameter	3.5 in.
Sector size	512 bytes
Zones	15
Cylinders	50,864
Recording density (max)	628,000 bits/in.
Track density	85,000 tracks/in.
Areal density (max)	53.4 Gbits/sq. in.
Formatted capacity	146.8 GB

Performance attribute	Value
Rotational rate	15,000 RPM
Avg. rotational latency	2 ms
Avg. seek time	4 ms
Sustained transfer rate	58–96 MB/s

SSD*

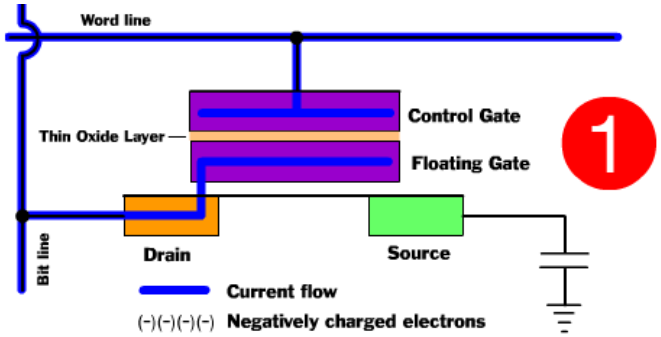
- **Solid State Disk**
  - **Storage technology based on Flash memory**

Flash memory*

- **Solid state storage device**
  - **Everything is electronic (no mechanical moving parts involved in accessing this memory)**
  - **A type of EEPROM device (Electronically Erasable Programmable Read Only Memory). It has a grid of columns and rows with a cell at each intersection**

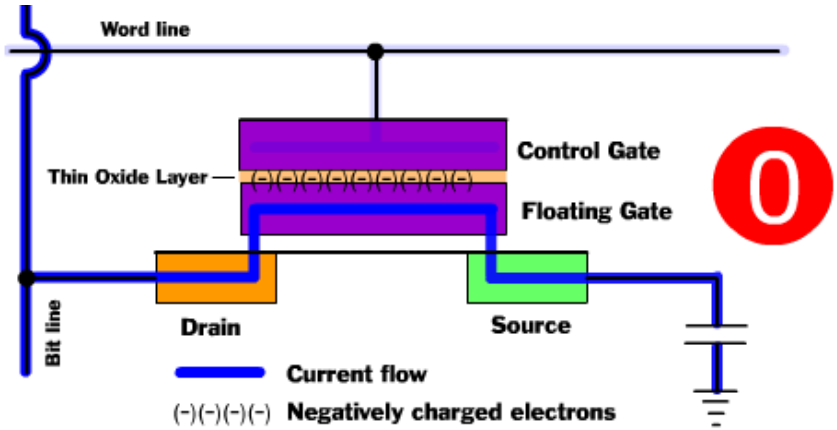
Flash memory*

- A cell is a modified transistor with two gates
  - floating gate and control gate
- The two gates are separated from each other by a thin oxide layer.
- The floating gate "links" to the wordline through the control gate with a small threshold
  - If linked, the cell has a value of 1, otherwise, 0

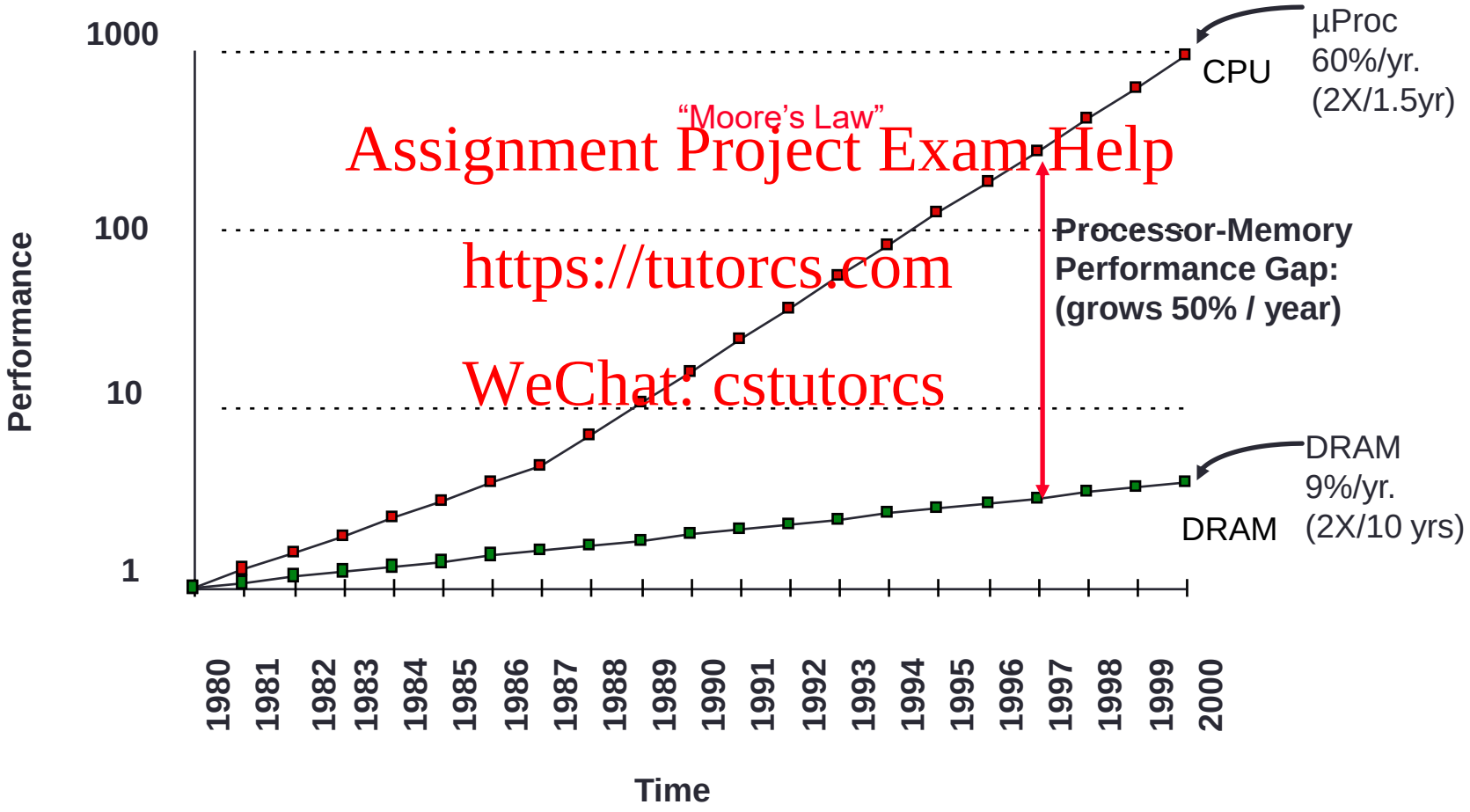


Flash memory*

- A blank flash memory has all of the gates linked, giving each cell a value of 1
- To erase 1, an electrical charge from the bitline is applied to the floating gate.
  - The negative electrons act as a barrier (large threshold) between the control gate and floating gate.



Processor-DRAM memory speed gap



Impact of the speed gap on performance

- Suppose a processor executes at
  - clock rate = 2 GHz
  - CPI = 1.1
  - 50% arith/logic, 30% ld/st, 20% control
- Suppose data memory operations get 50 cycle penalty
  - Pipeline has to wait 50 cycles for each memory access
- CPI
  - = ideal CPI + average stalls per instruction

  = 1.1 + 0.30 x 50

  = 16.1
- Because of the slowness of memory, on average, the pipeline outputs every 16 clock cycles!