COMP3222/9222 2021 PRACTICE PRACTICAL EXAM PROBLEM

Instructions for the Final Practical exam:

How will the exam be conducted?

- The Final Practical exam will be held on the **afternoon of Monday 29 November.**
- The exam will be held at a specified time on **WebCMS**.
- There are **4 questions** in total.
- The exam is worth **30 marks** in total. The exam contributes 30% to your final assessment in the course. You must score at least 40% of the available marks in this exam in order to pass the course.
- The exam has a **140 minute time limit** (consideration for 10 minutes reading time and time to upload files with momentary glitches in connectivity are included in this time allowance).
- All times stated for the exam are in Sydney time (AEDT = UTC+11).

What exam materials can be used?

- Make sure you have a quiet location with good internet connectivity where you can work on the exam undisturbed for the full 140 minutes.
- No exam materials are provided. You will need paper and pens and a means of scanning and uploading answers to some of the questions.
- You may use **any offline resources**, including your course notes, personal notes, textbooks, and lab files.
- You are not permitted to access web pages or other internet resources, except for the course and exam web pages
- You are not permitted to use code-synthesis tools such as GitHub Copilot
- Do not place your exam work in any location, including file sharing services such as Dropbox or GitHub, accessible to any other person.
- You may not request help from any person or service apart from the Course Coordinator, who will be available by email (o.diessel@unsw.edu.au) and on Teams.
- Even after you finish the exam, on the day of the exam do not communicate your exam answers to anyone. Some students have extended time to complete the exam.
- Ensure during the exam no other person in your household can access your work.
- Your **zpass** should not be disclosed to any other person. If you have disclosed your **zpass**, you should change it immediately.
- **Deliberate violation of exam conditions will be referred to Student Integrity as serious misconduct**

No help is allowed during the exam

- **You must not communicate with anyone while you are taking the exam.**
- **You are not permitted to use any online resources, e.g. searching for answers to questions using the Internet.**
- **Failure to comply with the above, if detected, will result in disciplinary action.**
- If you experience difficulties during the exam, or have a question about the exam, contact the Course Coordinator by email (o.diessel@unsw.edu.au) or via Teams as soon as possible.

Useful advice from UNSW on open book exams

https://www.student.unsw.edu.au/open-book-and-take-home-exams

Technical issues

If you experience a technical issue before or during the exam, you should follow these instructions:

- Take screenshots of as many of the following as possible:
  - error messages
  - screen not loading
  - timestamped speed tests
  - power outage maps
  - messages or information from your internet provider regarding the issues experienced
- All screenshots must include the date and time the issue occurred.
- Contact the Course Coordinator by phone (+61 2 9385 7384) email (o.diessel@unsw.edu.au) or via Teams immediately and advise of the issue.
- Submit a Special Consideration application immediately at the conclusion of your assessment and upload your screenshots.

Academic misconduct & Plagiarism

- **You must treat this exam as you would treat an in-person, supervised and invigilated exam.** Any evidence of academic misconduct will be treated seriously.

Student Declaration

You will complete a digital declaration prior to commencing the exam. By completing the declaration you are declaring that:

- As with any task conducted through UNSW, I am aware that online assignments and examinations require me to comply with the UNSW Student Code of Conduct (https://student.unsw.edu.au/conduct).
- I have read and understood the University requirements in respect of student academic misconduct outlined in the Student Code of Conduct (https://student.unsw.edu.au/conduct) and Annexure 1 of the Student Misconduct Procedures (https://www.gs.unsw.edu.au/policy/documents/studentmisconductprocedures.pdf)
- It represents my own work and that I did not give or receive assistance in any way that would violate the UNSW Student Code of Conduct (https://student.unsw.edu.au/conduct),
- I have taken proper and reasonable care to prevent this work from being copied by another student
- ***I understand the following actions, among others, constitute Academic Misconduct:***
  - ***Allowing others to complete an online task in my place, either in whole or in part.***
  - ***Taking or sharing screenshots of the assessment task or my responses unless expressly permitted by UNSW.***

    - ***Otherwise duplicating or distributing the assessment task in whole or in part.***
    - ***Communicating any assessment content, question or topic to any person prior, during or following the assessment unless expressly permitted by UNSW.***
    - ***Providing or seeking assistance from unauthorised information sources including, but not limited to, the Internet, any programs, chat servers, web services, or contact with any external parties to communicate, collude or get assistance in answering examination questions either prior to or during an online exam session.***
- I understand any breach of the above terms and conditions may result in university disciplinary action.

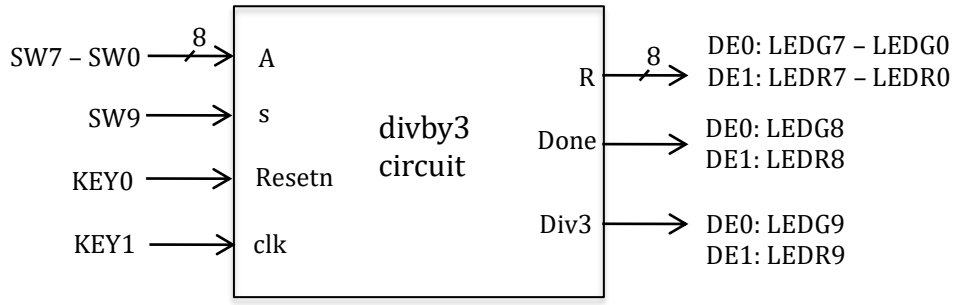
Special consideration

- This exam is covered by UNSW's Fit-to-Sit policy. That means that by sitting this exam, you are declaring yourself well enough to do so. You will be unable to apply for special consideration after the exam for circumstances affecting you before it began. If you have questions, or you feel unable to complete the exam, contact the Course Coordinator by phone (+61 2 9385 7384) email (o.diessel@unsw.edu.au) or via Teams

COMP3222/9222 Practice Problem Specification

Given an 8-bit number A, design and implement a circuit that determines whether A is divisible by 3 or not.

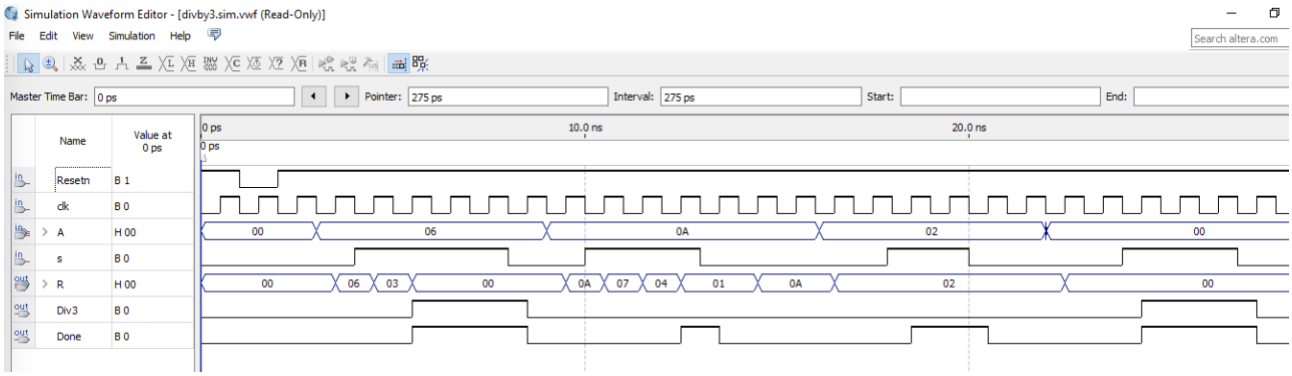
Your circuit should be connected to the components of the DE0/DE1 board as illustrated below:



Your circuit should operate as follows:

- When *KEY0 = Resetn* is pushed, the *Div3* and *Done* outputs should be deasserted and the circuit placed into a state in which it waits for the operator to assert the start signal *s* via switch SW9.
- The operator loads an 8-bit number *A* by setting switches *SW7–SW0*. Whatever number is set will be loaded on rising clock edges while *s* is deasserted. The *clk* is controlled by push button *KEY1*.
- When *s* is asserted, the circuit determines whether *A* is divisible by 3. One way of doing so is to repeatedly subtract 3 from *A* until the amount remaining is less than 3. If the amount remaining is 0, then *A* is divisible by 3, otherwise it is not.
- When the calculation is finished, the *Done* signal connected to *LEDG8* on the DE0 board and *LEDR8* on the DE1 board is to be asserted. If *A* is divisible by 3, the *Div3* output signal connected to *LEDG9* on the DE0 board and *LEDR9* on the DE1 board should also be asserted.
- The *Done* (and *Div3*) signal remains asserted until the operator deasserts *s*. This should cause the circuit to be placed into the initial reset state again.
- Output *R*, connected to *LEDG7–LEDG0* on the DE0 board and *LEDR7–LEDR0* on the DE1 board, is used to show the amount of *A* remaining before, during and after the calculation.

The timing diagram for four calculations is illustrated below:



You are provided with a Quartus Project Archive with pin assignments that map the circuit to the board you are using. The archives are named `divby3-DEn-exam.qar`, whereby you should use the archive named for the board you are using `n` = 0 for DE0 and `n` = 1 for DE1. The archive contains the outline of the top-level design entity for this problem, called `divby3`. (**To facilitate testing, do not modify the top-level ENTITY description for `divby3`.**) The archive contains the waveform file used to generate the timing diagram above. The archive also includes a bitstream for the working circuit, named `divby3-soln.sof`, in the `output_files` subdirectory.

Please ensure you download and use the correct archive for the board you are using!

Submission

You are required to submit:

1. [5 marks] A neat & legible listing of the **pseudocode** for this problem and a neat & legible sketch of your **initial ASM chart** for your design. Please take care with Mealy & Moore type outputs. Upload a SINGLE PDF, JPG or PNG format file containing your answer using the WebCMS submission tab for Part 1. of the exam.
2. [4 marks] A neat & legible sketch of the **datapath** for your design. The sketch MUST indicate the name of all signals as used in your VHDL description and correspond with the names used in your refined ASM chart of 3. Your datapath sketch MUST indicate the number of bits used for each signal and the size of all components. Upload a SINGLE PDF, JPG or PNG format file containing your answer using the WebCMS submission tab for Part 2. of the exam.
3. [3 marks] A neat & legible sketch of a **refined copy of your ASM chart** from 1. This diagram MUST use the same signal names and state names as used in your VHDL description and MUST indicate the state transitions and outputs of the control path. Upload a SINGLE PDF, JPG or PNG format file containing your answer using the WebCMS submission tab for Part 3. of the exam.
4. [18 marks] A **Quartus Project Archive** of your completed design. To facilitate testing, do not modify the top-level ENTITY description for `divby3`. Upload a SINGLE QAR format file containing your answer using the WebCMS submission tab for Part 4. of the exam.

   Your solution will be marked according to the following scheme:

   a. [15 marks] Still testing and debugging VHDL code – we will assess the completeness and correctness of your description
   b. [2 marks] Simulation complete – make sure we have your waveform file in the directory as we will check your simulation progress
   c. [1 marks] Implementation complete – we will test your design on the board

Disclaimer

This Practice Exam is representative of the type of problem, environment, and materials permitted during the COMP3222/9222 Practical Exam. The actual exam may contain substantially different instructions, including problem specification, submission requirements, and marking scheme.