

**COMP3222/9222 Digital Circuits & Systems**

9. Implementation Technology  
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# Objectives

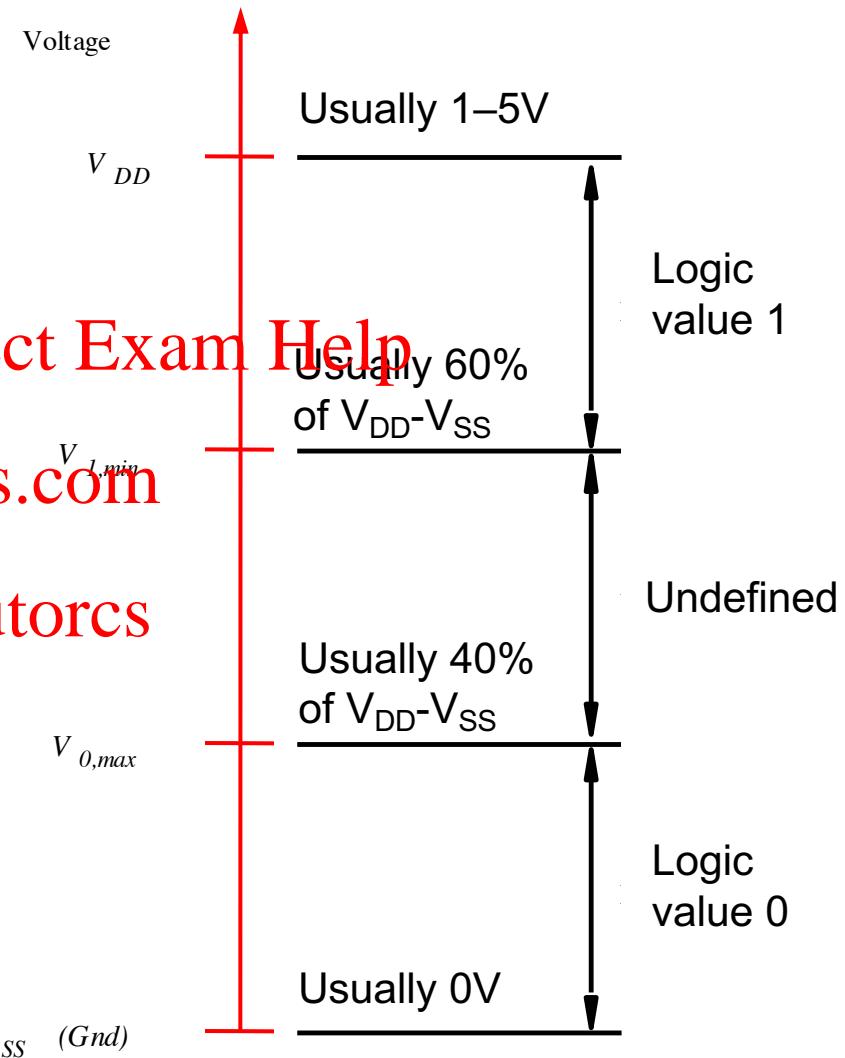
- Learn about integrated circuit implementation technologies
- Understand the structure and operation of CMOS logic gates
- Know about the variety of digital implementation technologies and their application
- Review the structure of field-programmable gate arrays and other programmable logic devices

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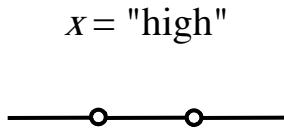
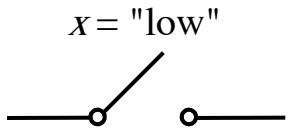
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# Logic values as voltage levels

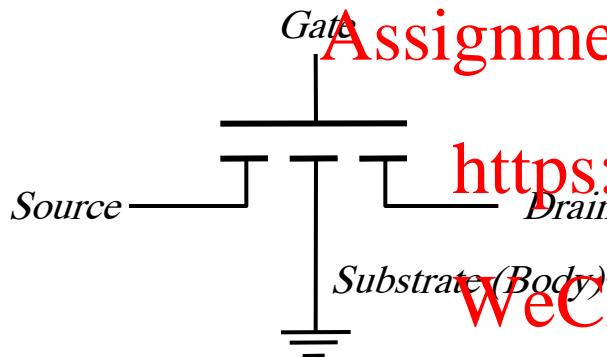
- Logic variables are physically represented using voltage or current levels
  - Use of voltage levels more common
- Usually, logic 0 is represented by a low voltage level and logic 1 by a high V level
  - Known as a *positive logic* system



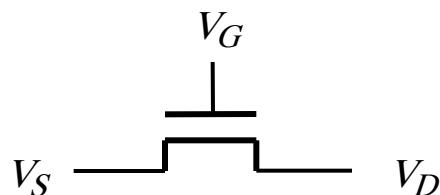
# nMOS transistor as a switch



(a) A simple switch controlled by the input  $x$



(b) nMOS transistor



(c) Simplified symbol for an nMOS transistor

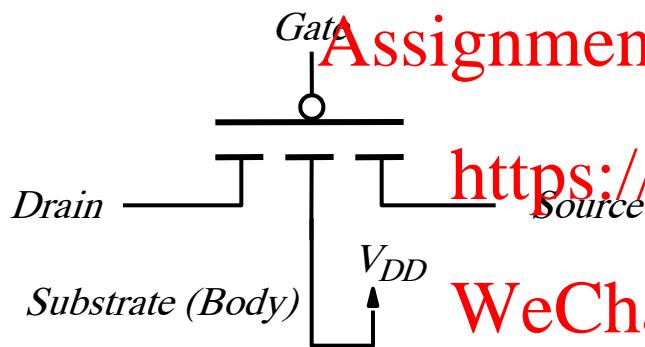
B&V3, Figure 3.2

- Logic circuits are built with transistors operated in *cutoff* or *saturation* modes
- The most popular type of transistor for implementing a switch is the metal oxide semiconductor field-effect transistor (MOSFET)
  - Two types: n-channel or nMOS and p-channel or pMOS
- In nMOS, the terminal with the lower voltage level is deemed to be the source (of electrons)
  - When  $V_G$  is below a so-called threshold voltage,  $v_t$ , there is no connection between the source and drain – the device is turned off
  - When  $V_G > v_t$ , the device is switched on and  $V_D \approx V_S$

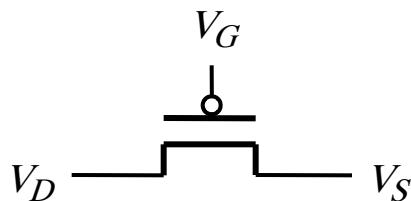
# pMOS transistor as a switch



(a) A switch with the opposite behavior of Figure 3.2 a



(b) pMOS transistor



(c) Simplified symbol for a pMOS transistor

- pMOS transistors have the opposite behaviour of nMOS transistors
  - Here, the voltage at the source (of holes) is higher than at the drain
  - The substrate is connected to  $V_{DD}$  (source voltage) rather than ground
  - $V_G < V_B$  to allow current to flow from source to drain and for  $V_D = V_S$

# nMOS operation – cutoff → subthreshold ( $v_{GS} < v_t$ )

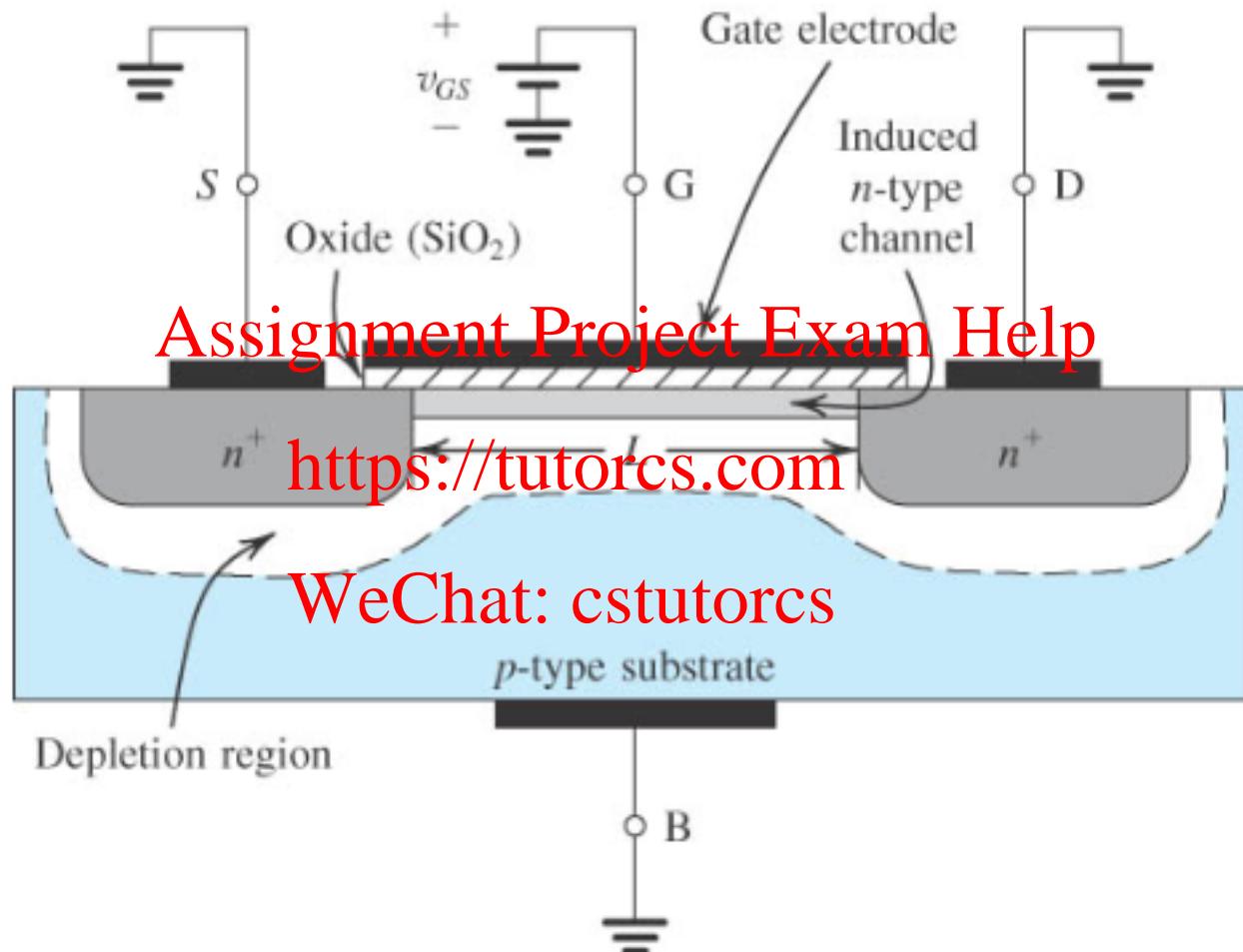


Image due to: F. Najmabadi, UCSD  
See 3222 website for his lecture notes

# nMOS operation – triode mode ( $v_{GS} > v_t$ & $v_{DS} < v_{GS} - v_t$ )

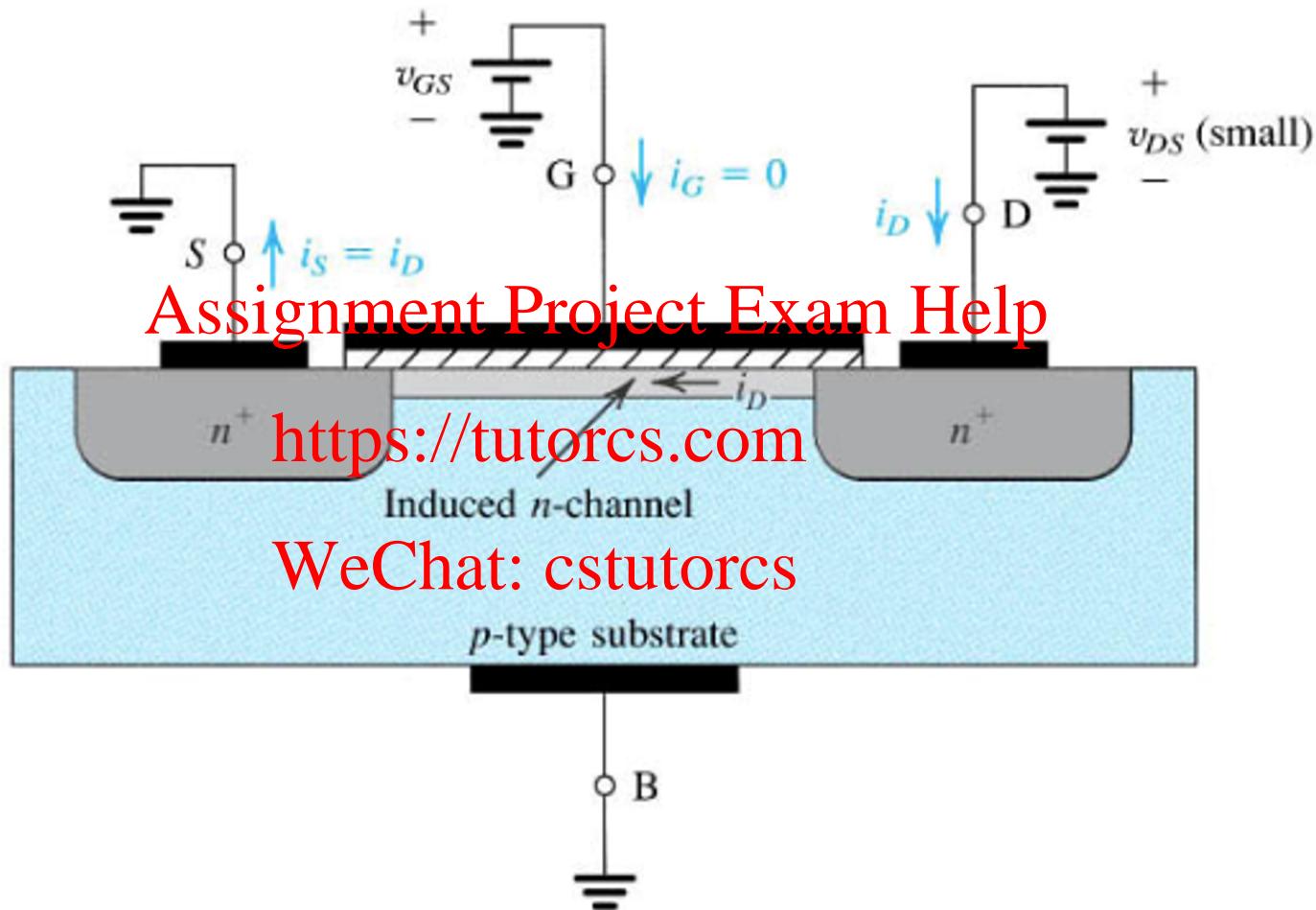


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# nMOS operation – pinchoff ( $v_{DS} \rightarrow v_{GS} - v_t$ )

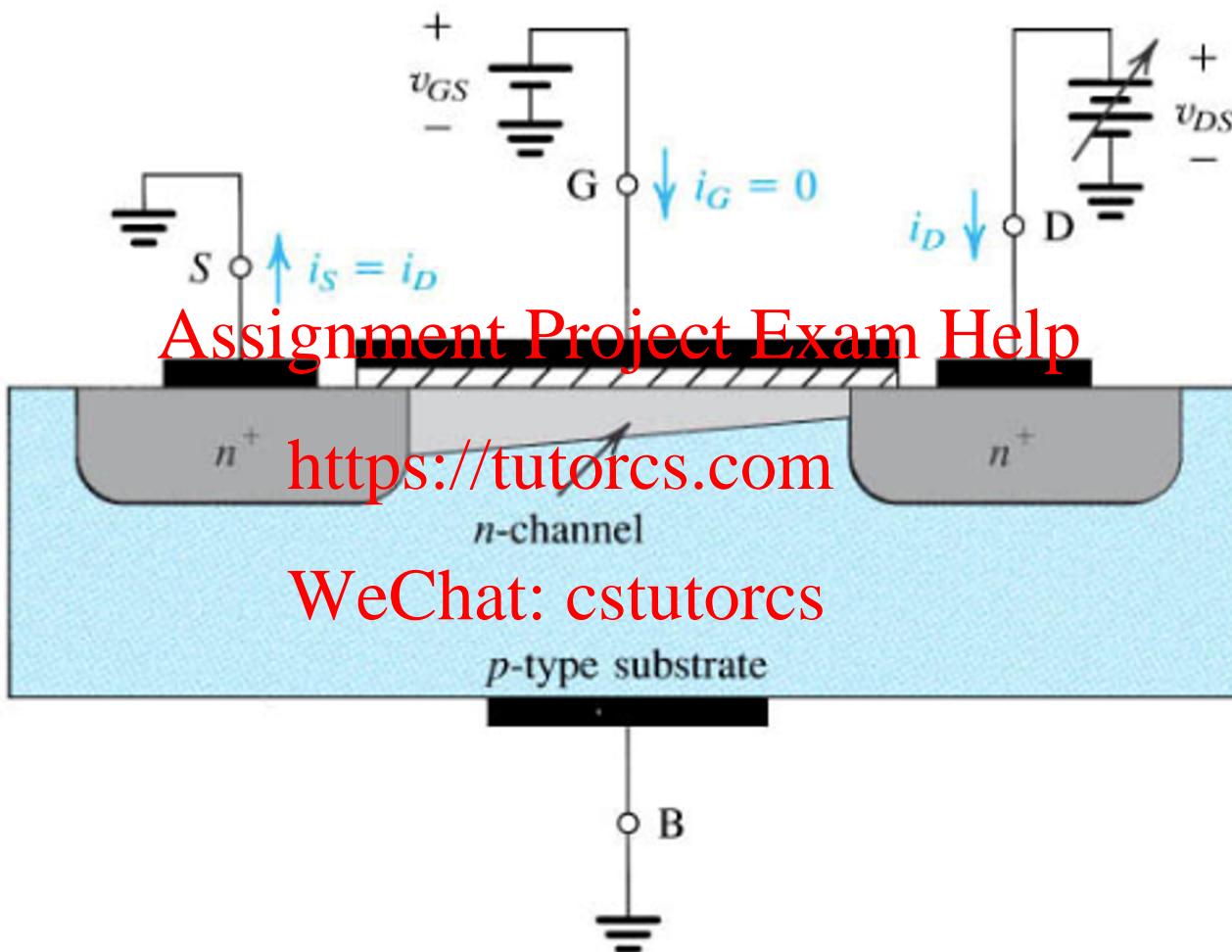


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# nMOS operation – saturation ( $v_{DS} \geq v_{GS} - V_t$ )

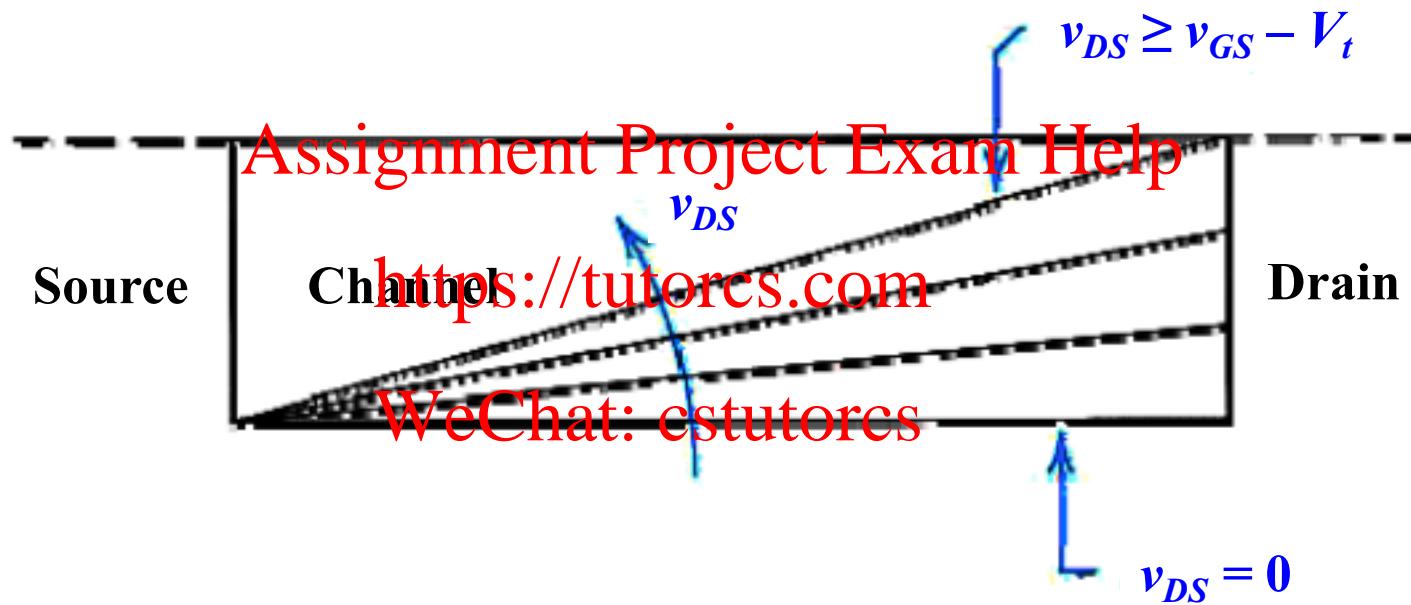


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# nMOS operation – V-I characteristic

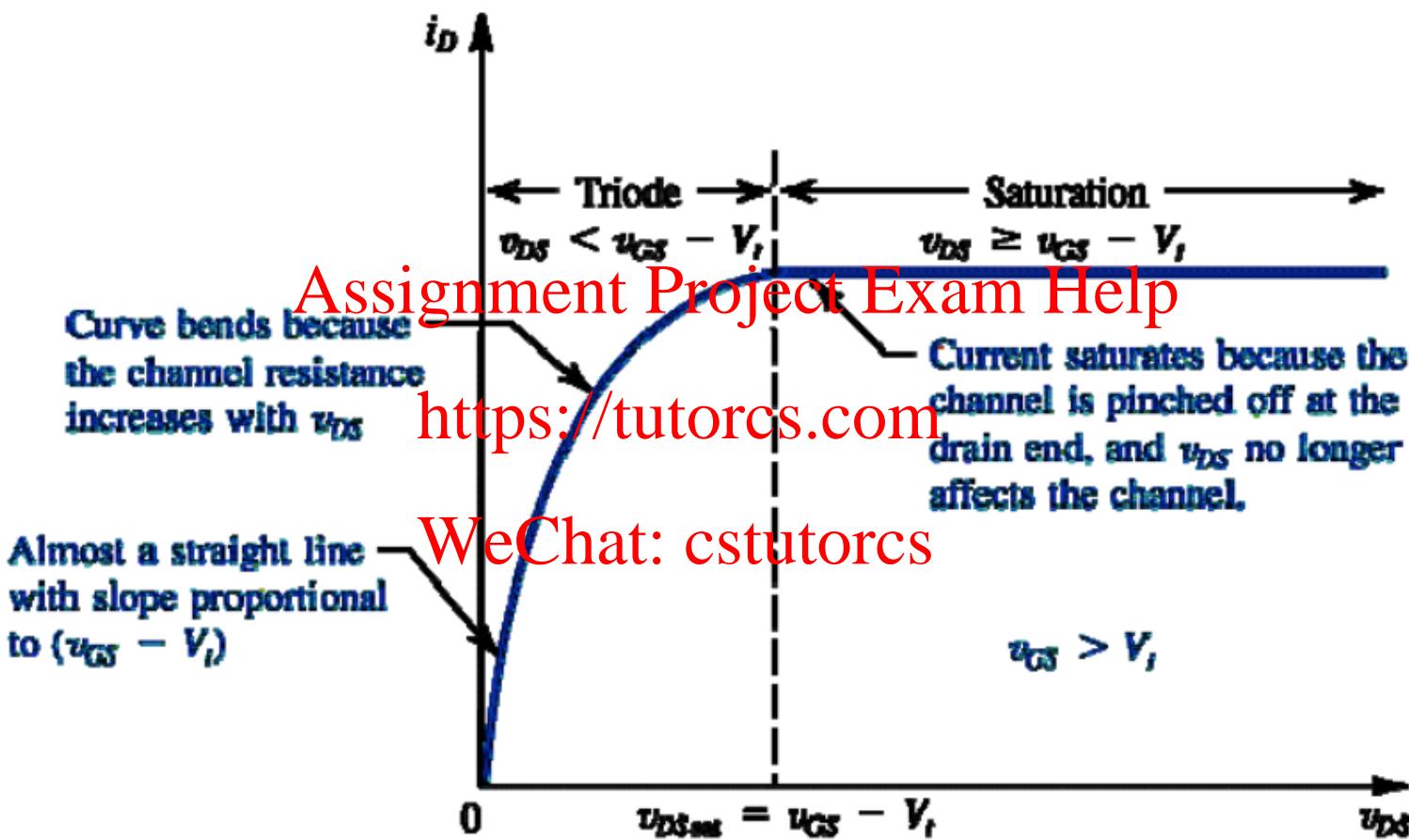
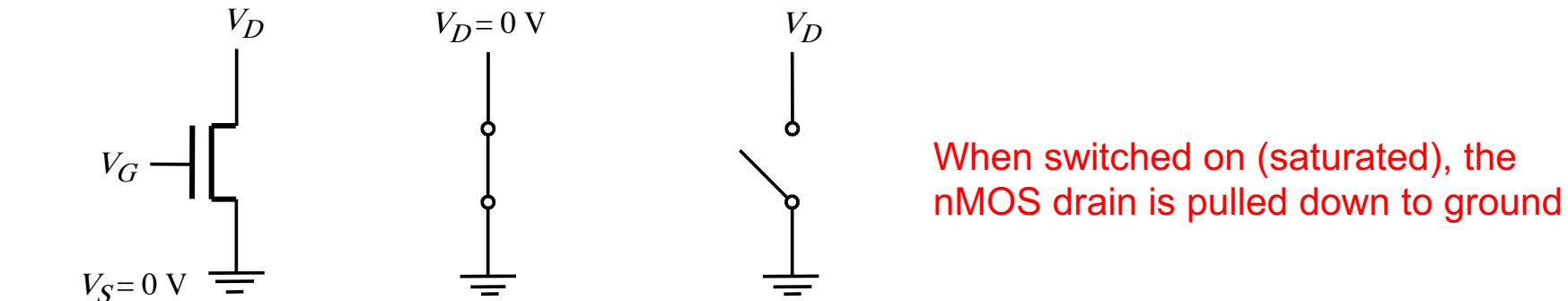


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# nMOS and pMOS transistors in logic circuits

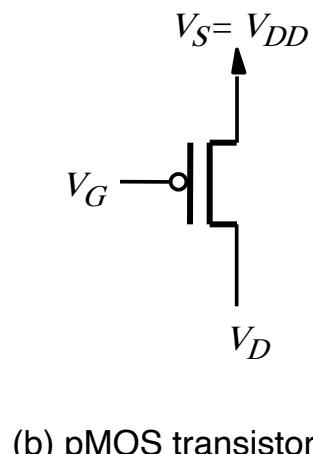


When switched on (saturated), the nMOS drain is pulled down to ground

(a) nMOS transistor

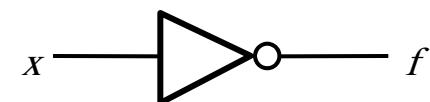
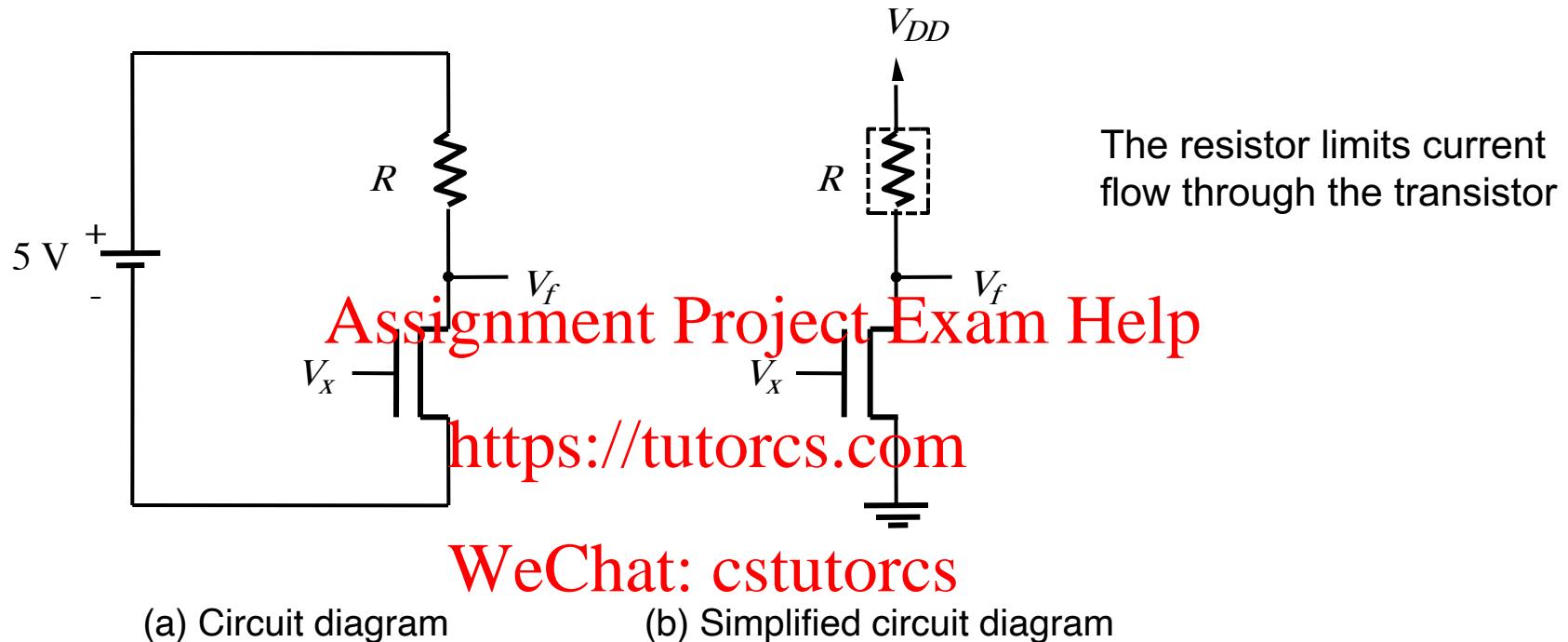
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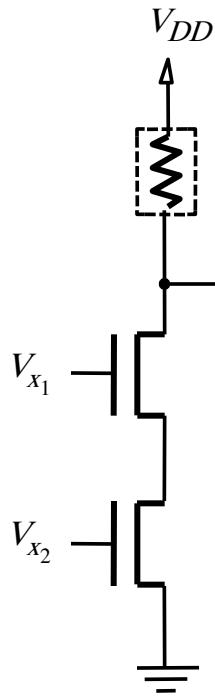
When switched on, the pMOS drain is pulled up to  $V_S = V_{DD}$

# A NOT gate built using nMOS technology



(c) Graphical symbol

# nMOS realization of a NAND gate



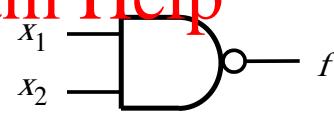
(a) Circuit

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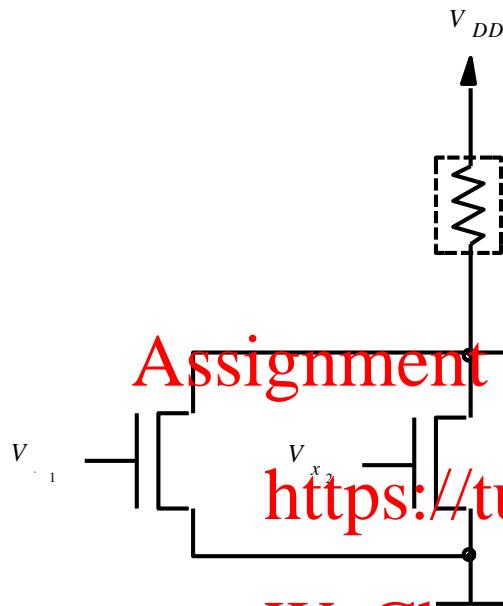
$x_1$	$x_2$	$f$
0	0	1
0	1	0
1	0	0
1	1	1

(b) Truth table



(c) Graphical symbol

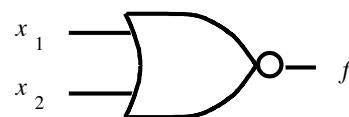
# nMOS realization of a NOR gate



(a) Circuit

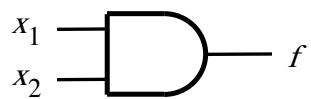
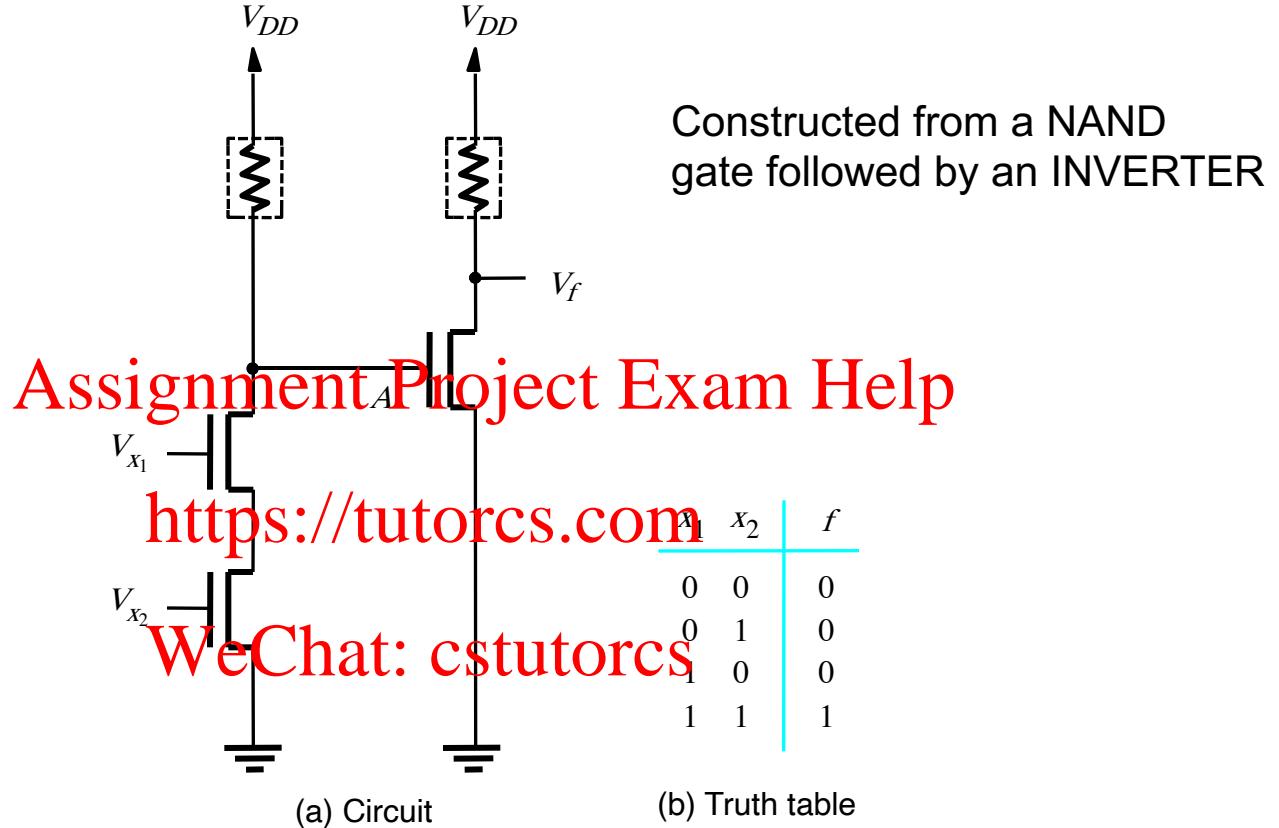
$x_1$	$x_2$	$f$
0	0	1
0	1	0
1	0	0
1	1	0

(b) Truth table



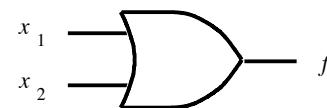
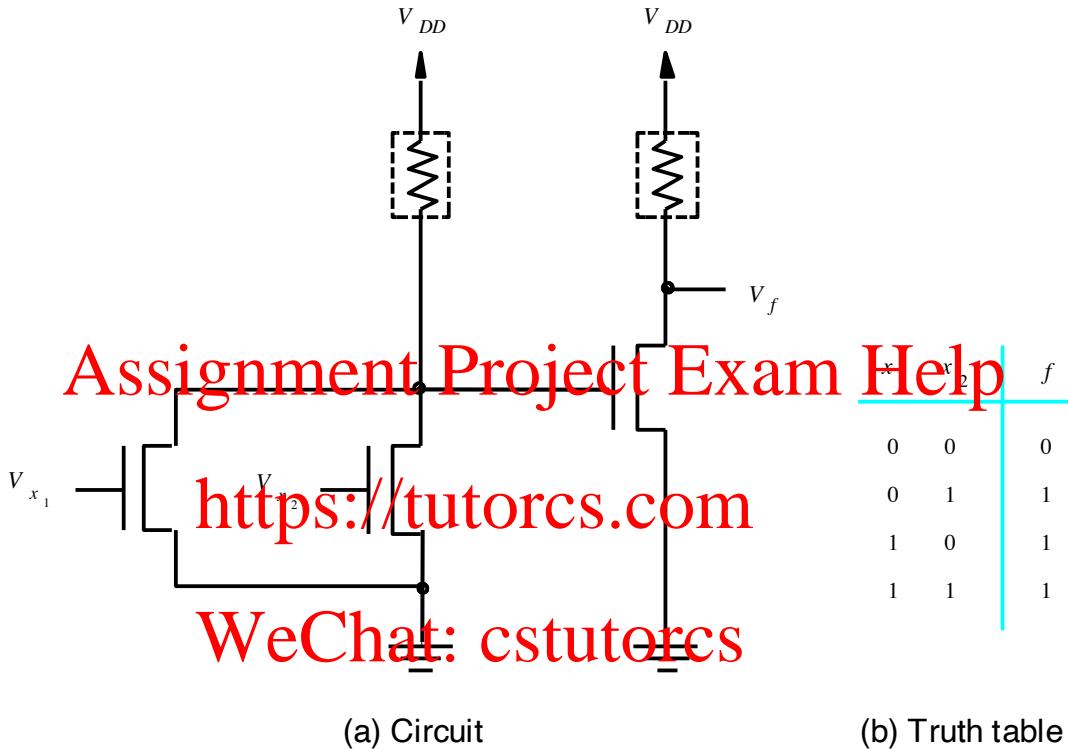
(c) Graphical symbol

# nMOS realization of an AND gate



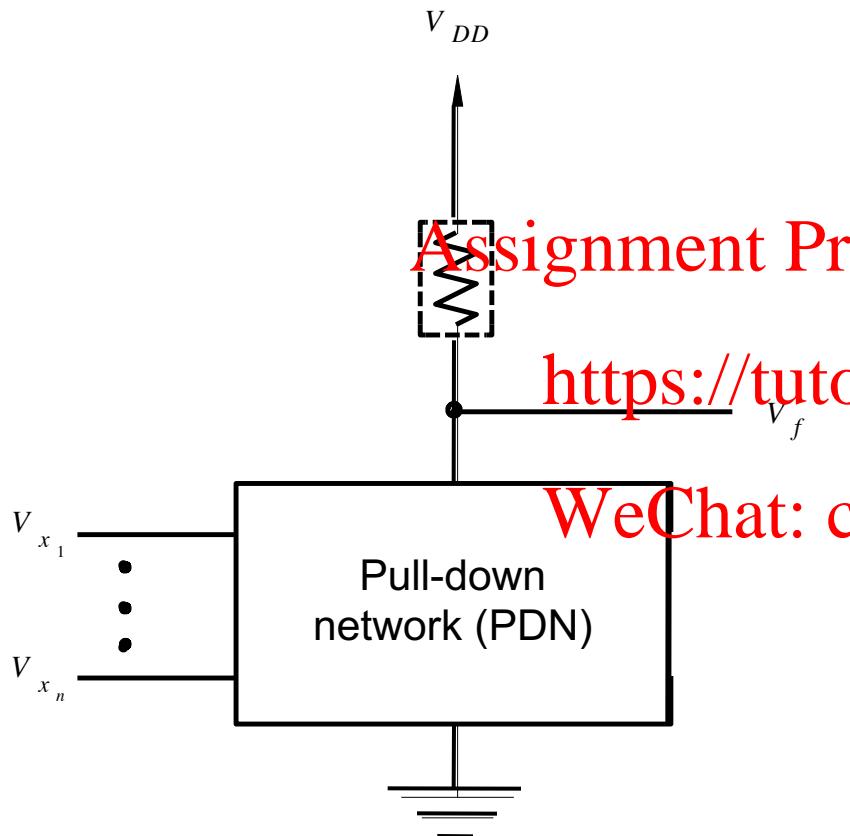
(c) Graphical symbol

# nMOS realization of an OR gate



(c) Graphical symbol

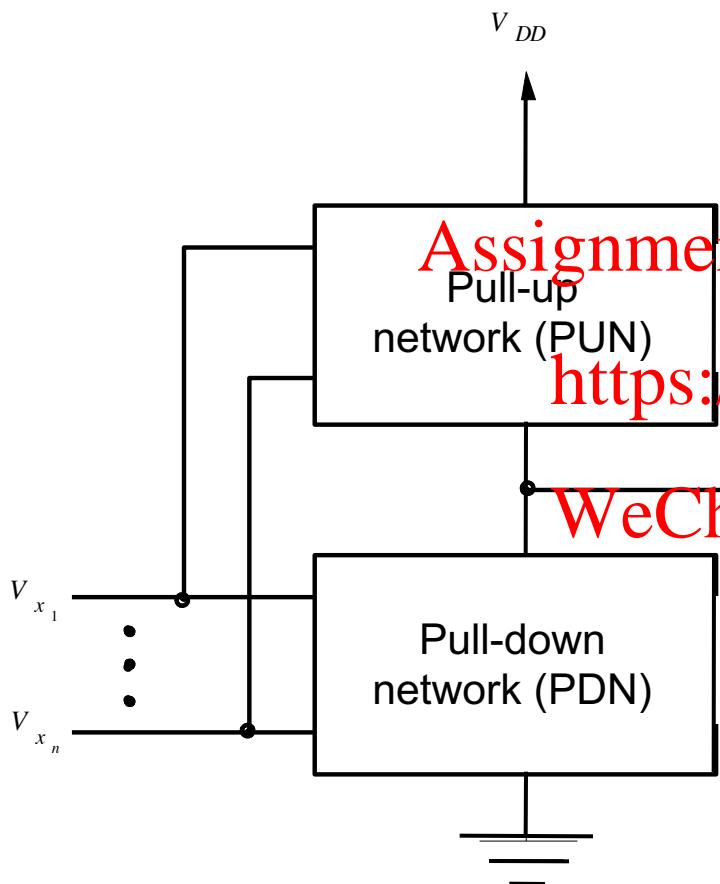
# Structure of an nMOS circuit



B&V3, Figure 3.10

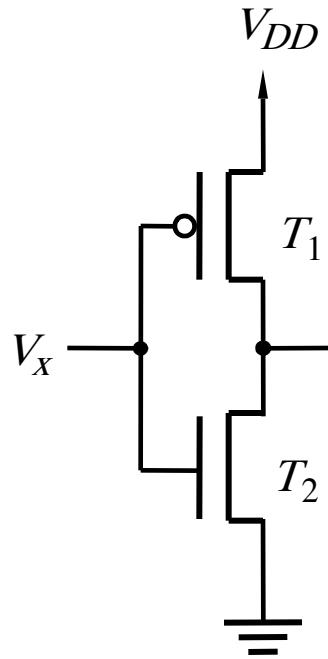
- Generalizing the forgoing structures, note that the nMOS transistor network acts to pull the drain to ground
- We can derive an equivalent pMOS circuit for each of the previous circuits
  - We can also combine both nMOS and pMOS networks together in what is known as complementary MOS (CMOS) technology
    - Involves replacing the pull-up resistor with a pull-up network that complements the structure of the nMOS-based pull-down network
    - Eliminates the power dissipation in the current-limiting resistor & simplifies fabrication

# Structure of a CMOS circuit



- The functions realized by the PUN and PDN are complements of each other
  - For any valuation of the inputs, either the PDN pulls  $V_f$  down to ground or the PUN pulls  $V_f$  up to  $V_{DD}$
- The PUN & PDN have equal numbers of transistors and are arranged such that the networks are duals of each other
  - Wherever the PDN has nMOS transistors in series, the PUN has pMOS transistors in parallel and vice versa

# CMOS realization of a NOT gate



(a) Circuit

$x$	$T_1$	$T_2$	$f$
0	on	off	1
1	off	on	0

(b) Truth table and transistor states

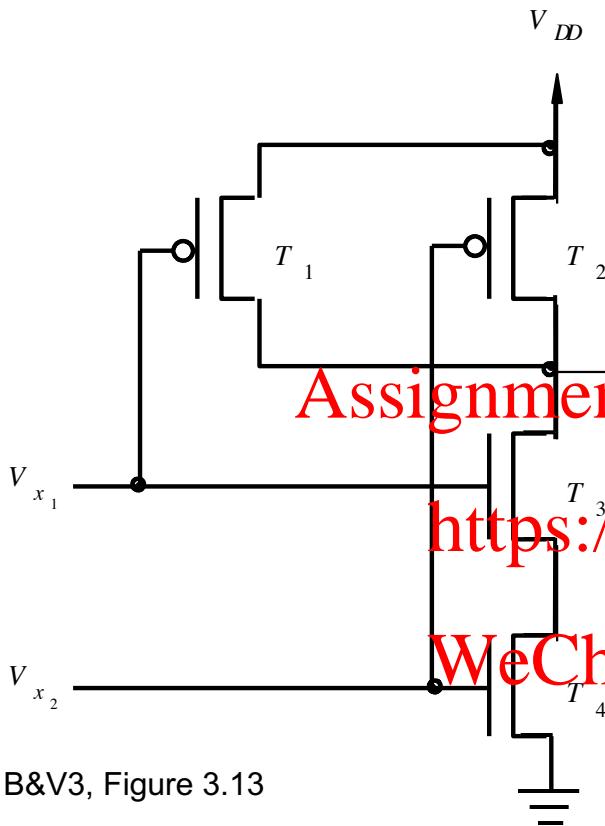
B&V3, Figure 3.12

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- Note that **ALMOST** no current flows in a CMOS inverter when the input is either low or high.
- This is true for all CMOS circuits; ALMOST no current flows, and hence ALMOST no power is dissipated under steady state conditions.
- However, such *leakage current* (through the gate) mounts as the transistor feature sizes and threshold voltages (gate voltage at which current just begins to flow) decrease
- So called *dynamic power* or *switching power* is transitionally dissipated when the gate changes state – the amount dissipated is *proportional to the clock frequency and the square of the supply voltage  $V_{DD}$*

# CMOS realization of a NAND gate



B&V3, Figure 3.13

x <sub>1</sub>	x <sub>2</sub>	T <sub>1</sub>	T <sub>2</sub>	T <sub>3</sub>	T <sub>4</sub>	f
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0

- The circuit can be derived from the NAND function  $f = \overline{x_1 x_2}$
- This expression specifies the conditions for which  $f = 1$ ; hence it defines the PUN:

From DeMorgan,

$$f = \overline{x_1 x_2} = \overline{x}_1 + \overline{x}_2$$

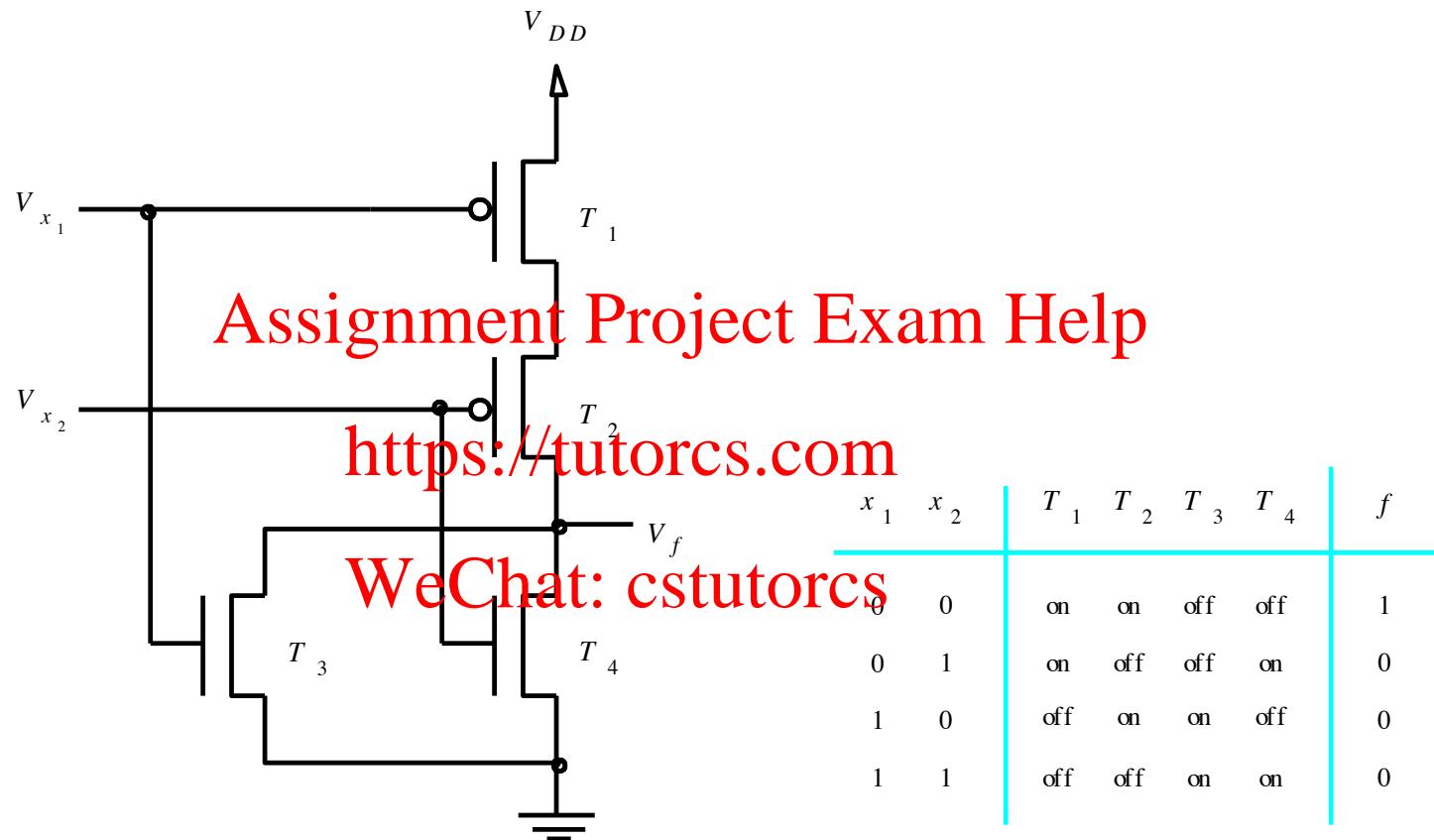
- Thus  $f = 1$  when either  $x_1$  or  $x_2$  have the value 0, which means the PUN must have two pMOS transistors connected in parallel

- The PDN must implement the complement of  $f$  which is

$$\overline{f} = x_1 x_2$$

- Since  $\overline{f} = 1$ , and thus  $f = 0$ , when both  $x_1$  and  $x_2$  are 1, the PDN must have two nMOS transistors in series

# CMOS realization of a NOR gate

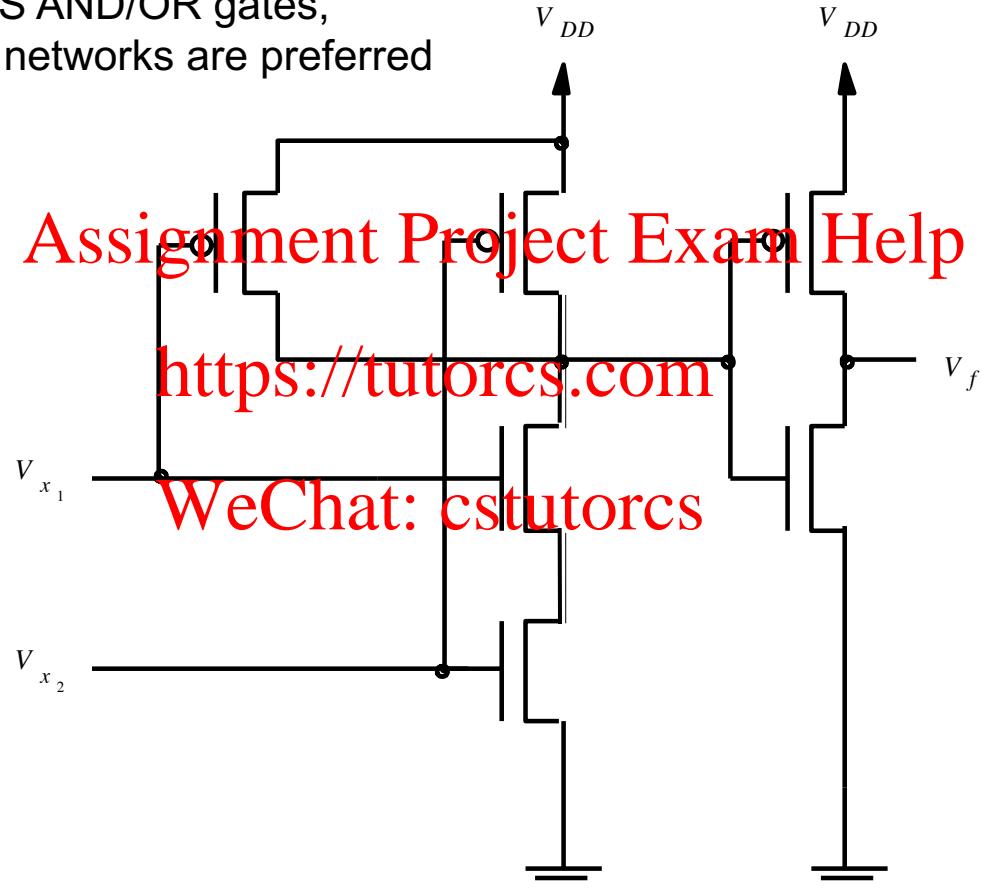


(a) Circuit

(b) Truth table and transistor states

# CMOS realization of an AND gate

Since two more transistors are needed  
to construct CMOS AND/OR gates,  
NAND/NOR logic networks are preferred



# The circuit for $f = \bar{x}_1 + \bar{x}_2\bar{x}_3$

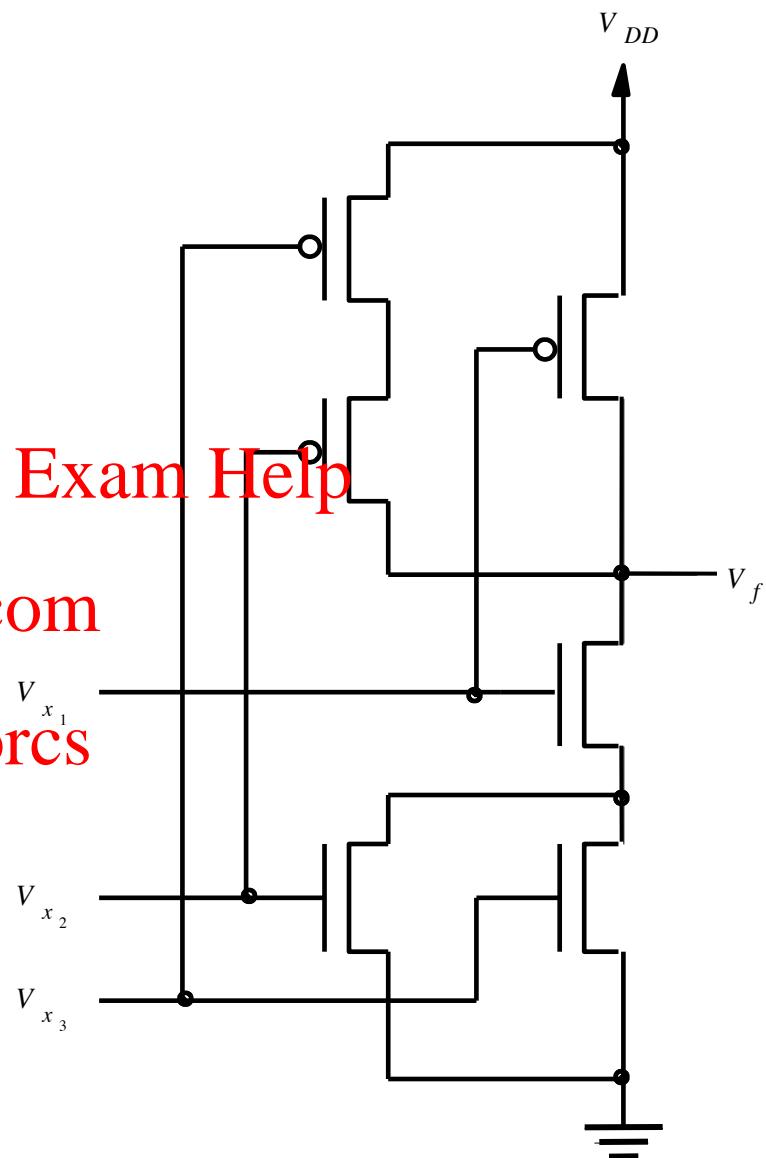
- The PUN is readily derived since all variables appear in complemented form
- Use DeMorgan to derive the PDN:

$$\bar{f} = \bar{\bar{x}}_1 + \bar{\bar{x}}_2\bar{\bar{x}}_3$$

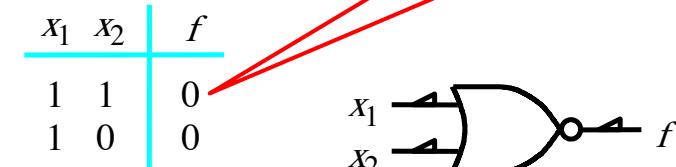
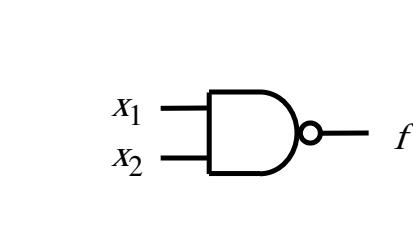
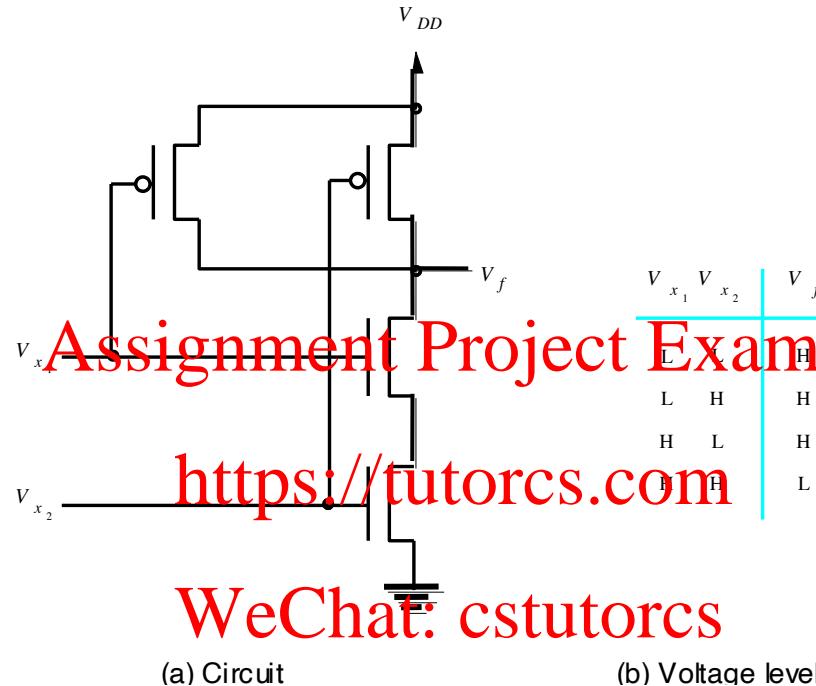
$$= x_1(x_2 + x_3)$$

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# Note voltage levels for the NAND circuit...





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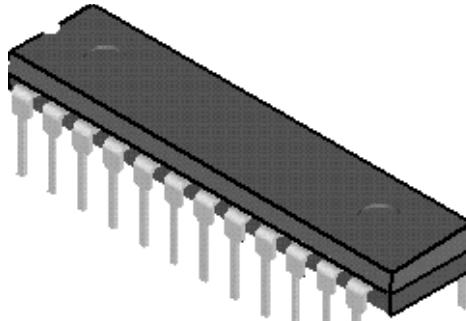
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# A 7400-series chip

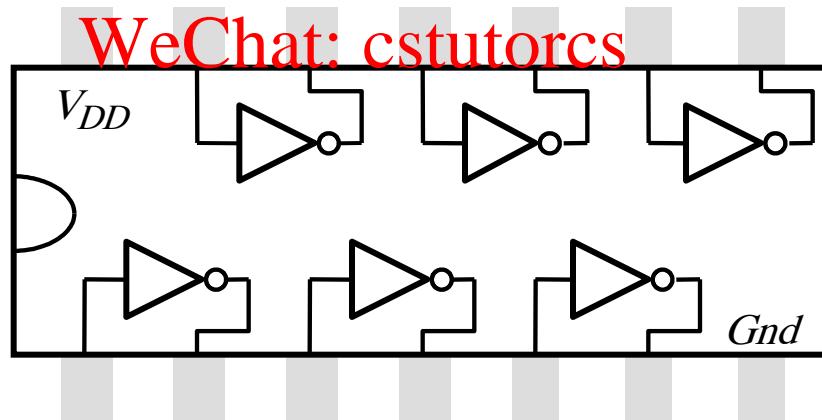


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(a) Dual-inline package  
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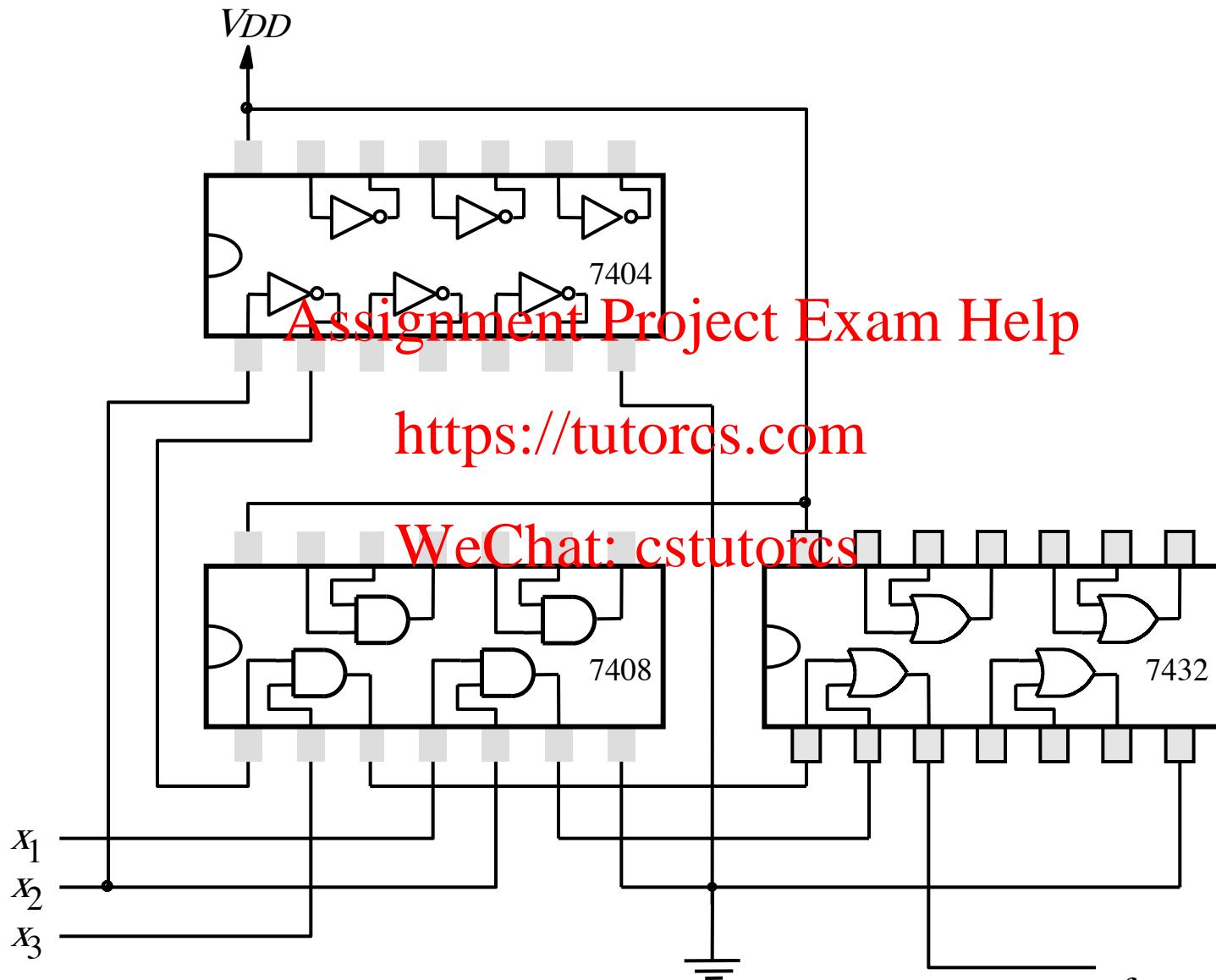
7400-series packages, a highly successful example of integrated circuit technology introduced in the 1960s, were widely used until the mid-1980s.

Because of their low logic capacity, these standard chips are seldom used today

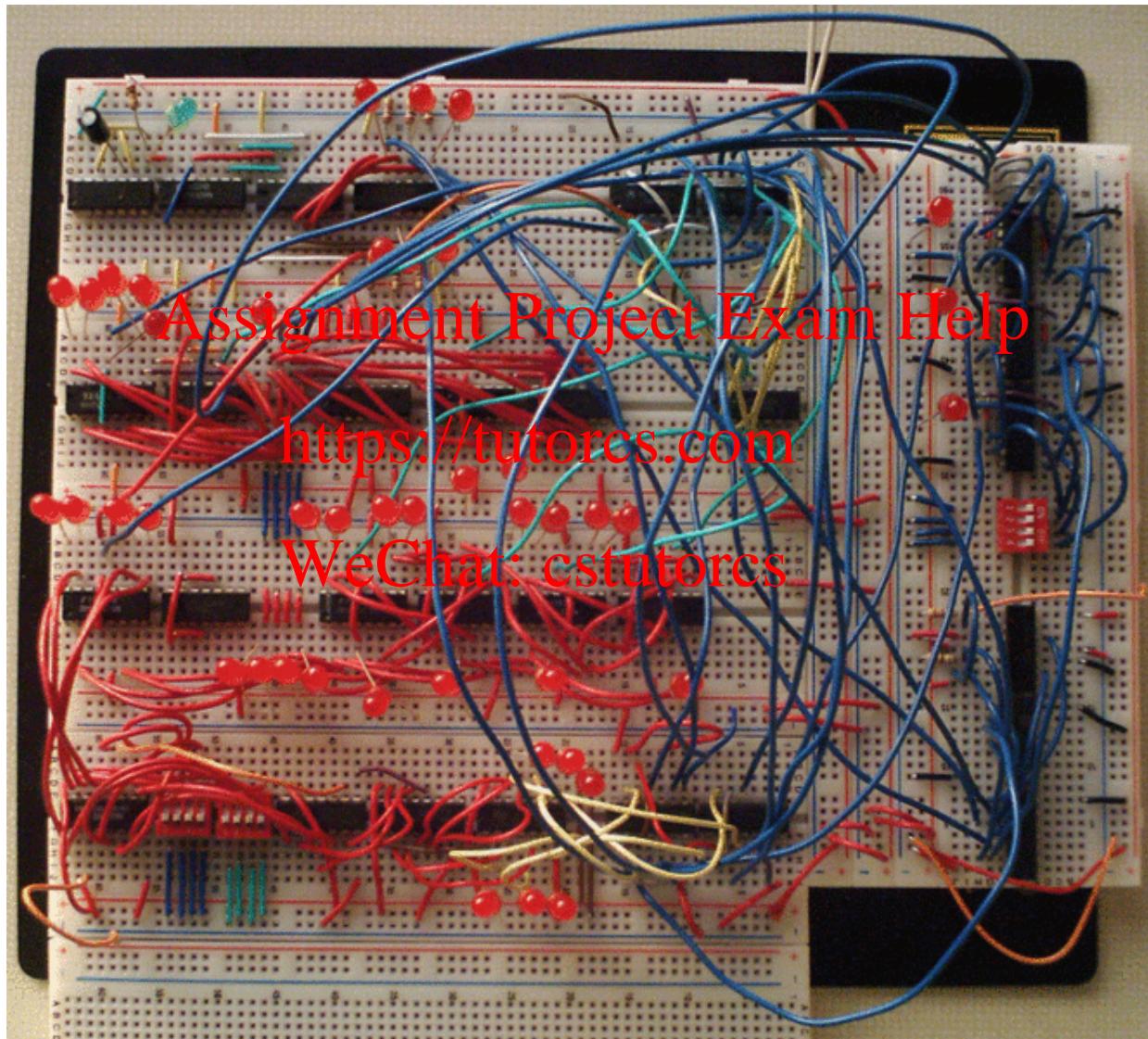


(b) Structure of 7404 chip

# An implementation of $f = x_1x_2 + \bar{x}_2x_3$



# A 4-bit, 2-register, 6-instruction 7400 series computer



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Wikipedia

# Evolution of integrated circuit technology

- Over time, chips have been classified according to their size
  - The earliest chips, such as 7400-series chips, comprise only a few logic gates – the technology used to produce these chips is referred to as small-scale integration (SSI)
  - Chips that included 10 to 100 gates represented medium-scale integration (MSI)
  - Until the mid-1980s, chips that were too large to qualify as MSI were classified as large-scale integration (LSI)
- More recently, this classification scheme has lost practical value, as most integrated circuits contain many 1,000,000s, if not billions, of transistors – these are all made with what is referred to as very large scale integration (VLSI) technology
  - These devices support the trend in digital hardware to integrate as much circuitry as possible onto a single chip
- This trend to ever greater levels of integration is driven by application needs, cost, performance, reliability and profit factors

# The problem with fixed devices...

- The functions provided by 7400-series parts are fixed and cannot be tailored to suit particular designs

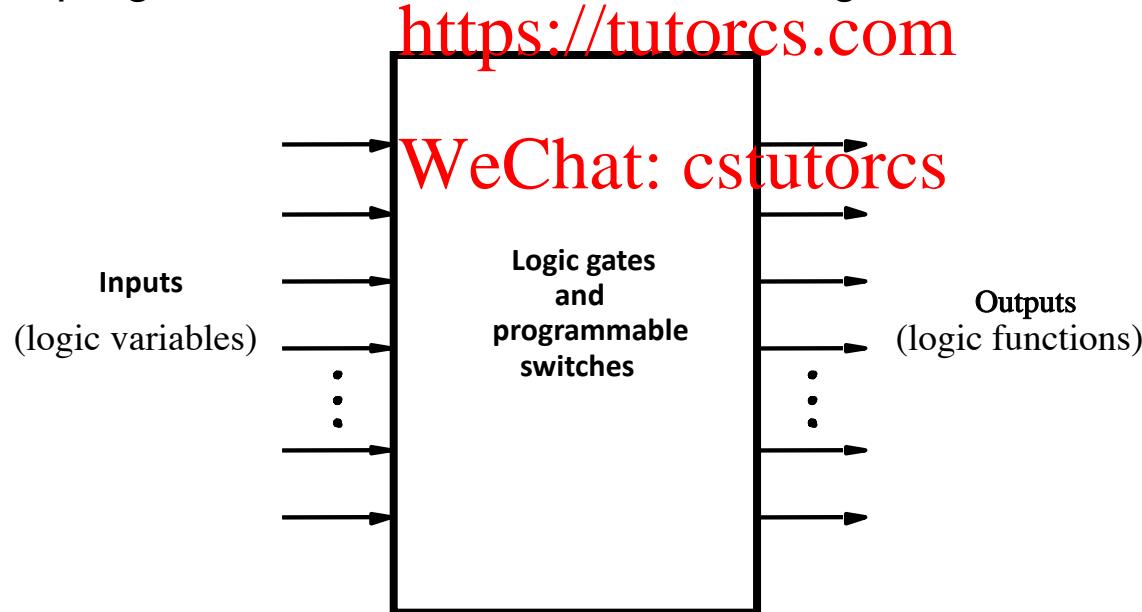
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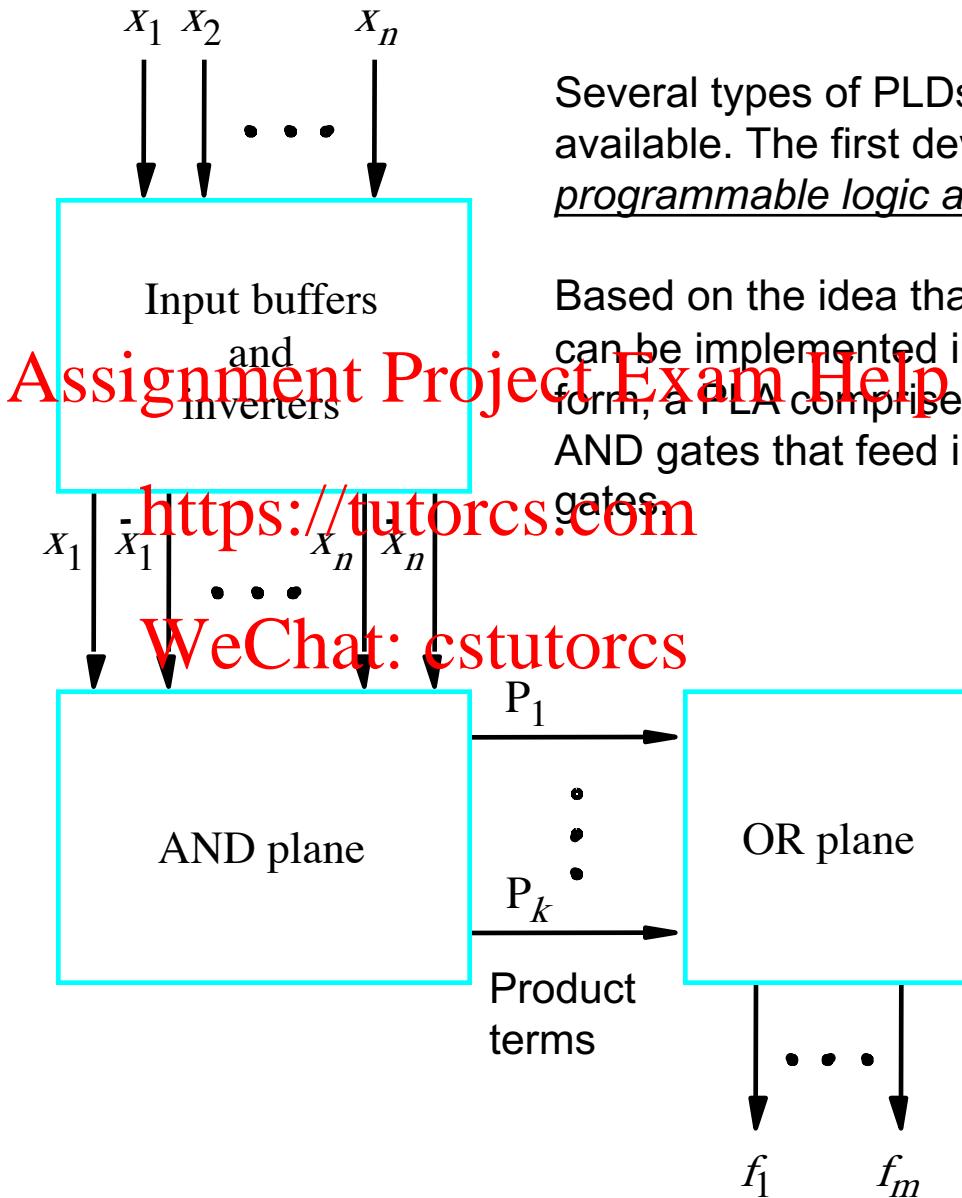
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# Programmable logic device as a black box

- It is possible to manufacture chips that contain relatively large amounts of logic circuitry with a structure that is **not fixed**
  - Such devices were introduced in the 1970s and are called programmable logic devices (PLDs)
  - PLDs are general-purpose chips for implementing logic circuitry
  - They can be viewed as a black box containing logic gates and programmable switches to allow the gates to be interconnected as desired



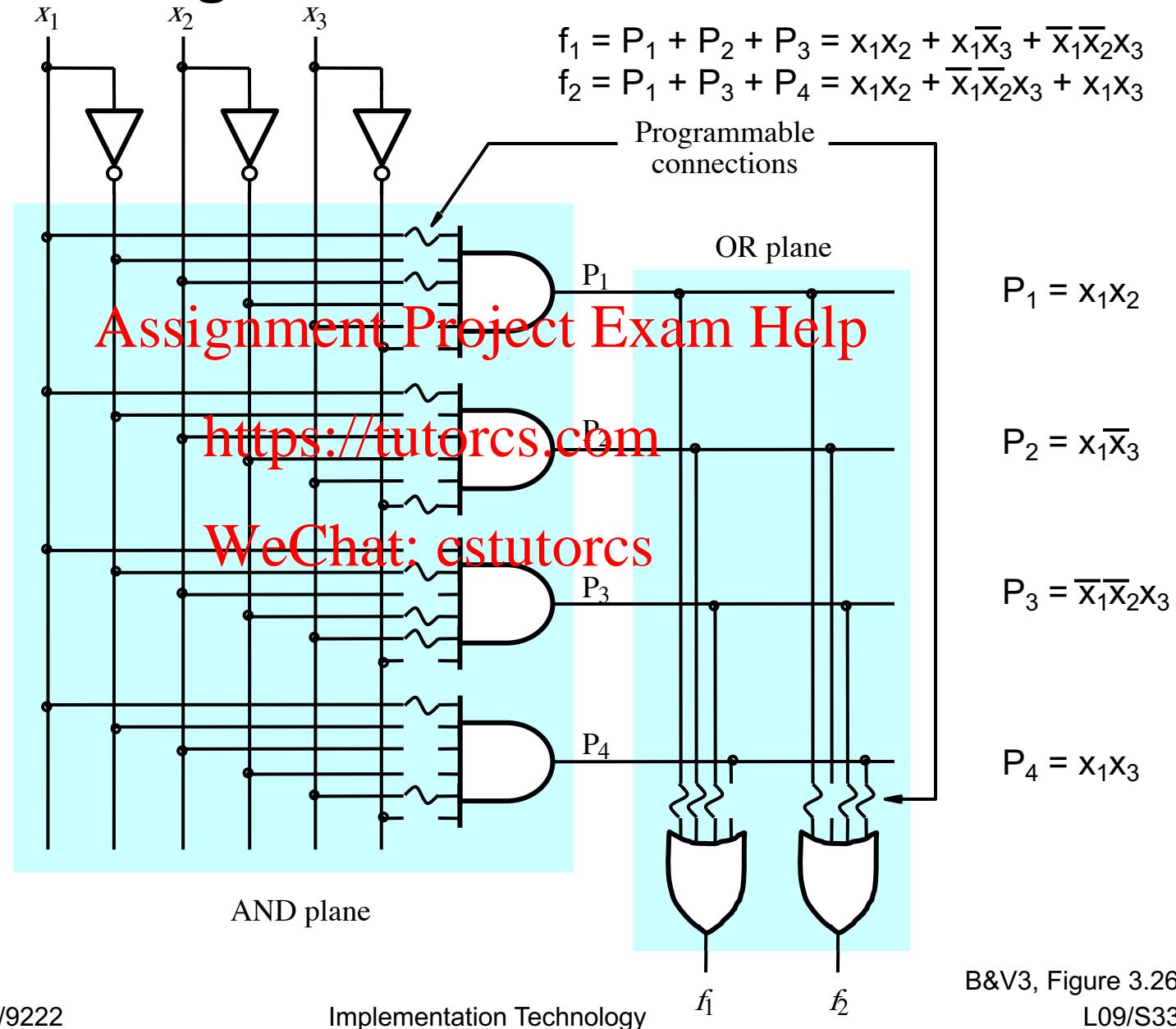
# Programmable Logic Array (PLA)



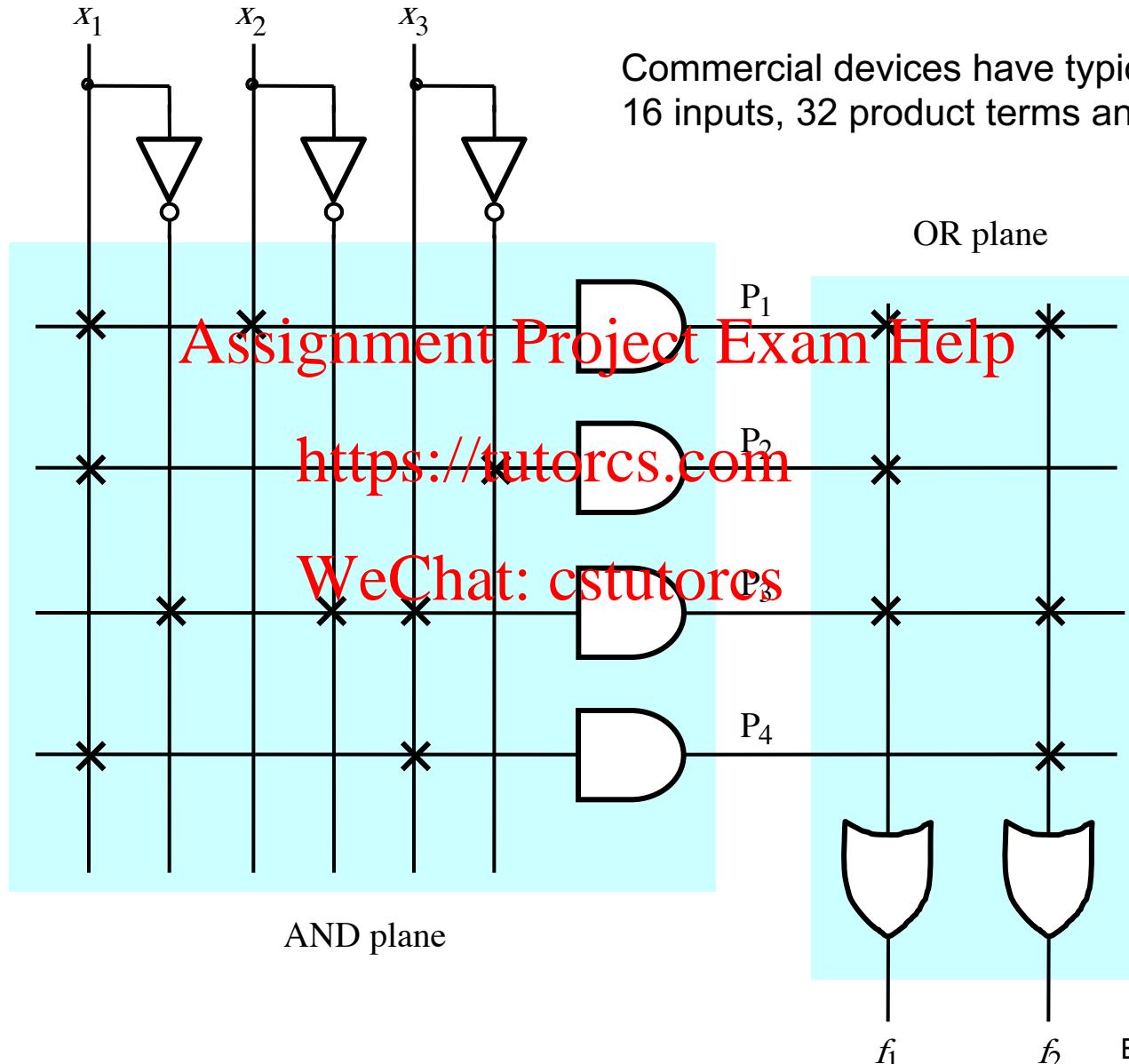
Several types of PLDs are commercially available. The first developed was the programmable logic array (PLA).

Based on the idea that logic functions can be implemented in sum-of-products form, a PLA comprises a collection of AND gates that feed into a set of OR gates.

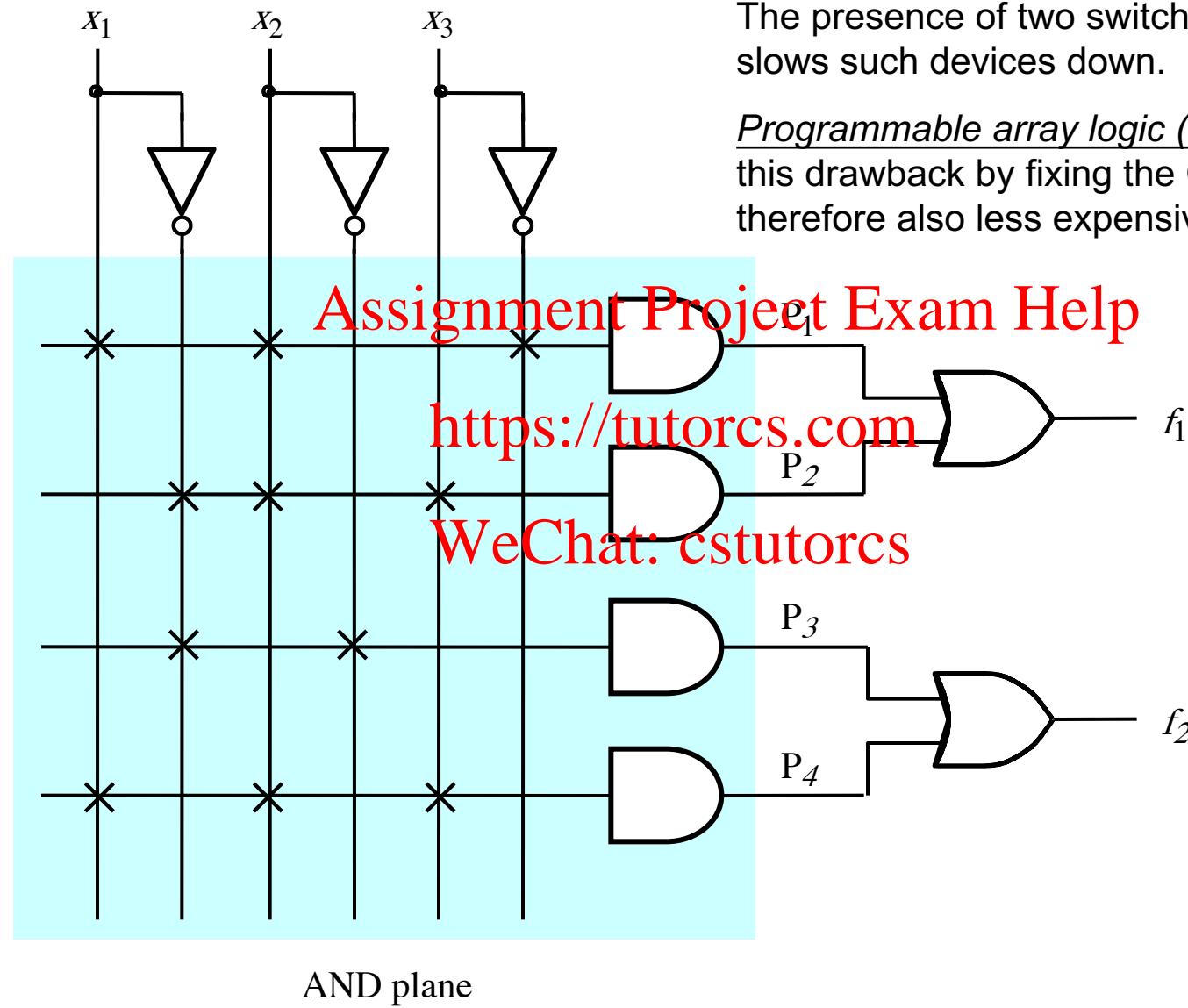
# Gate-level diagram of a PLA



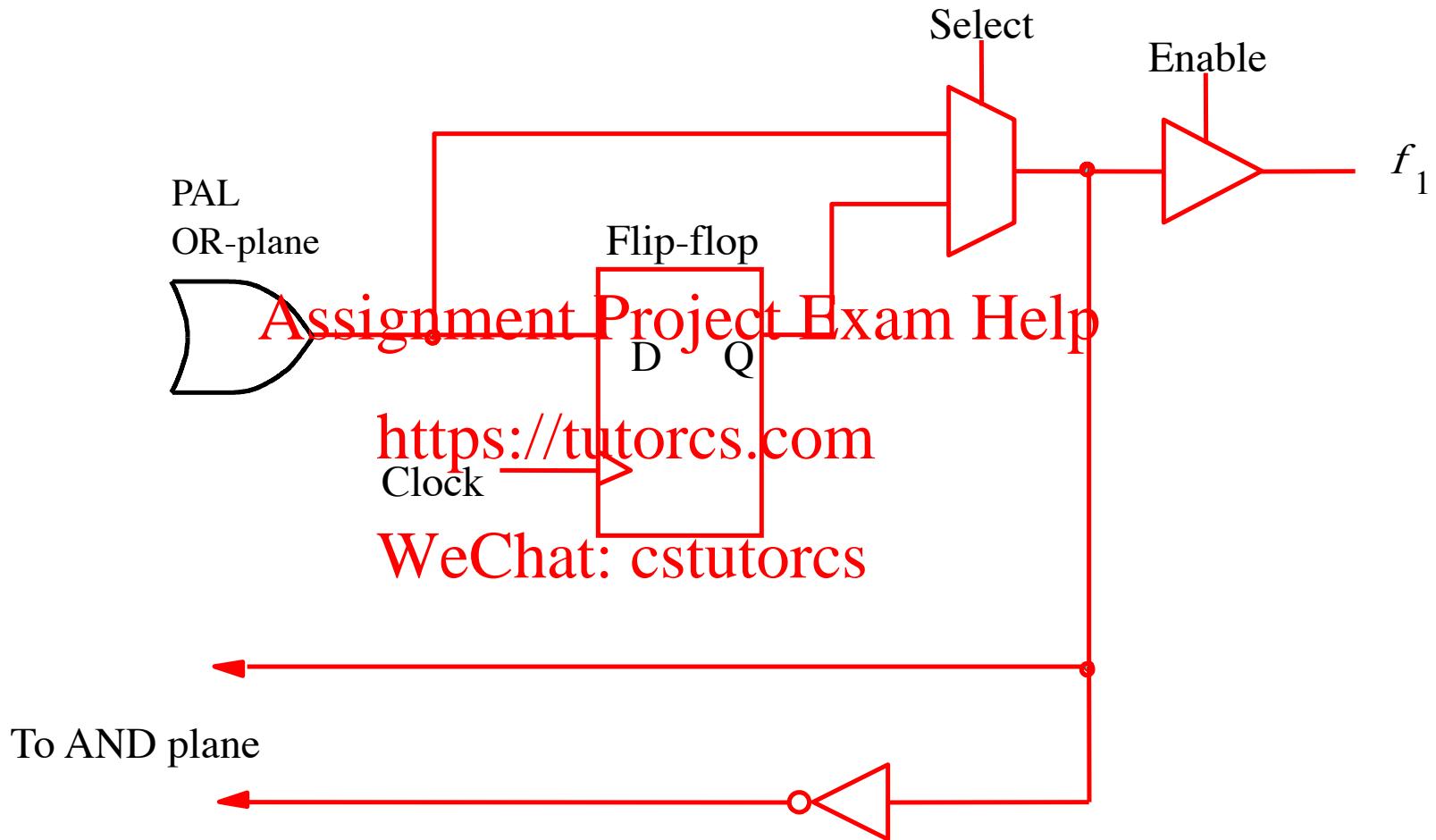
# More conventional schematic of the previous PLA



# Programmable Array Logic (PAL)



# Enhancing the flexibility of PAL outputs



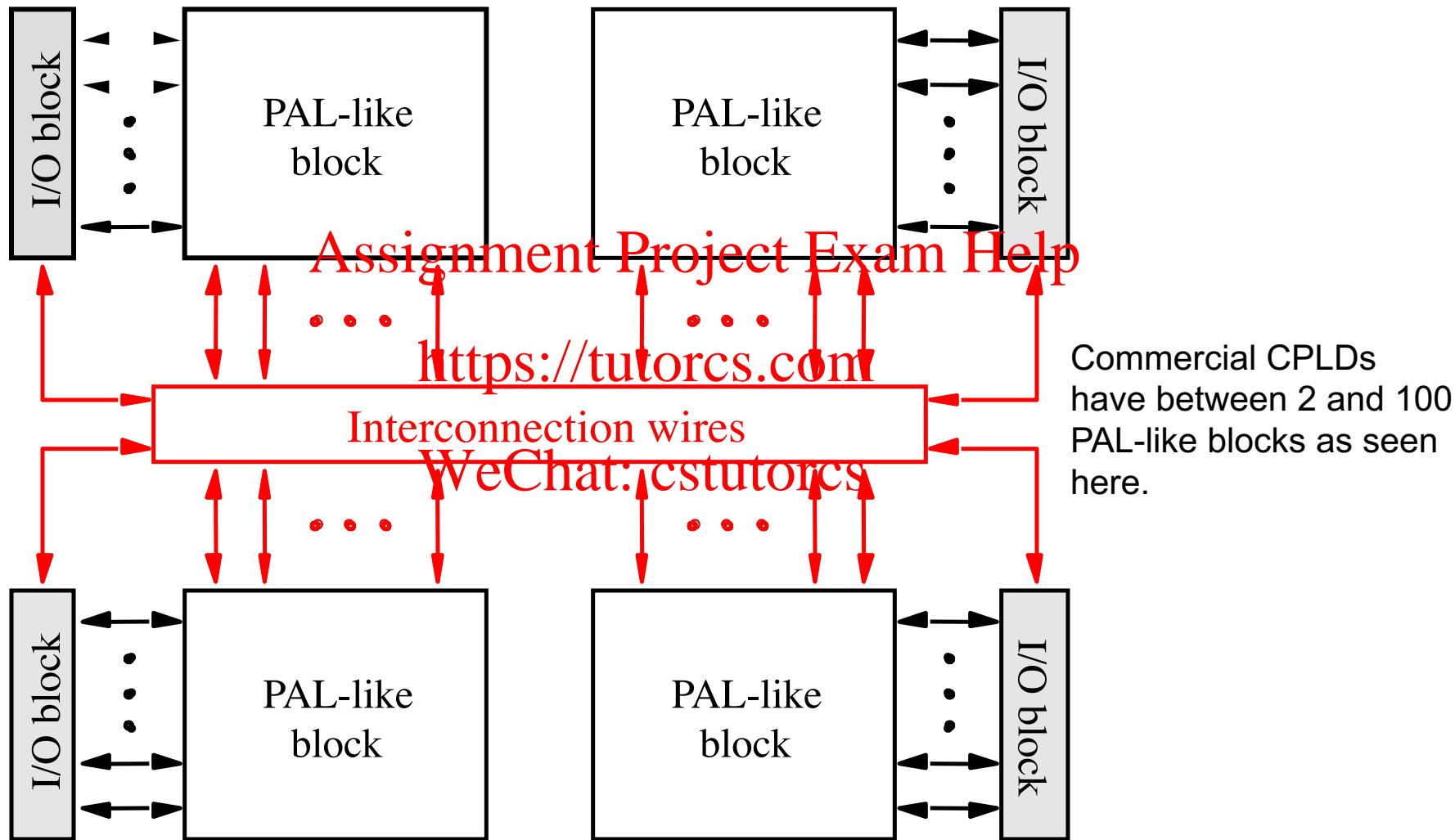
# A PLD programming unit



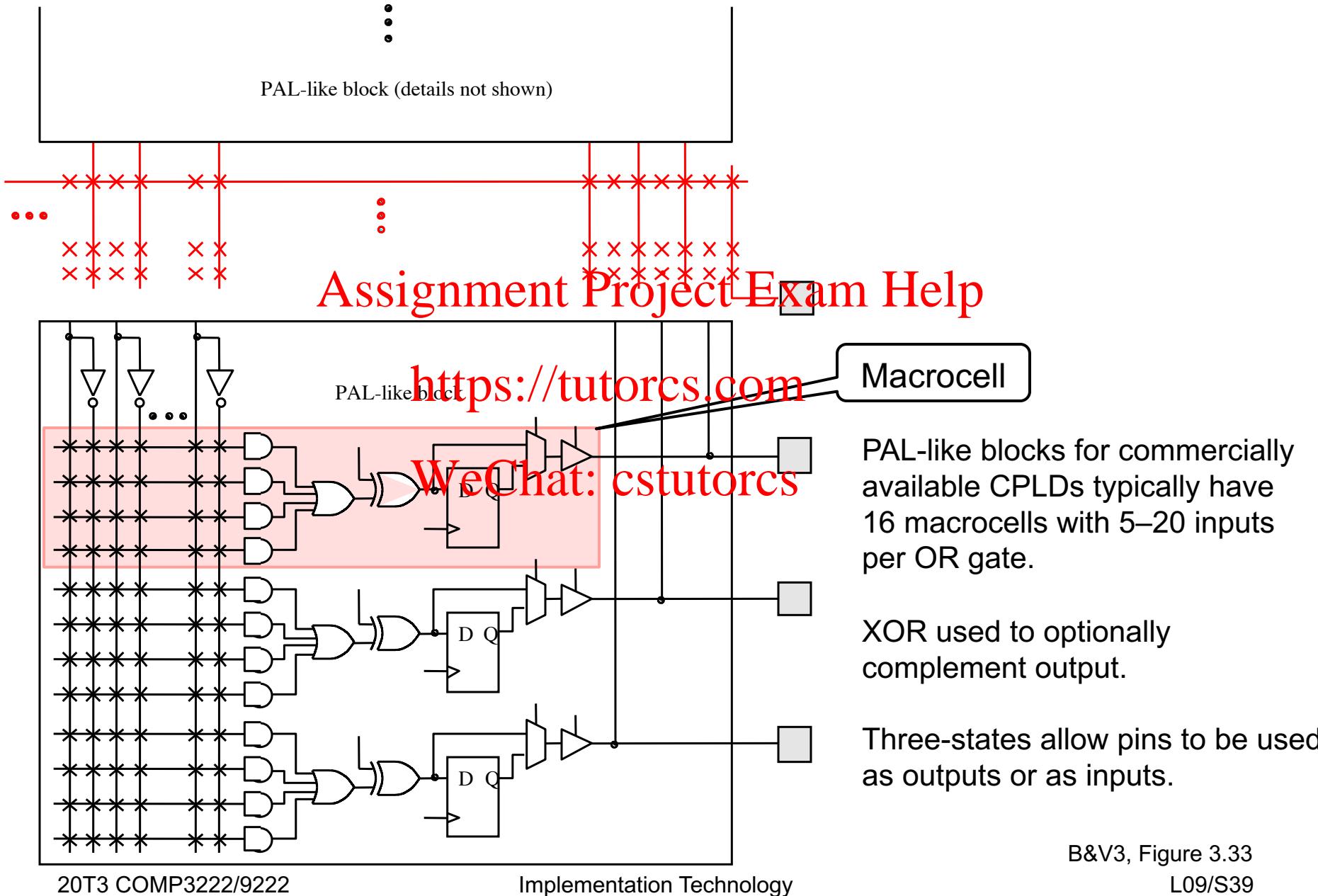
- Programming methods:
  - Fuse & anti-fuse
    - permanent
  - PROM, EPROM & EEPROM
    - slow & low density
  - SRAM
    - fast, but volatile
  - Flash
    - non-volatile, not as fast

B&V3, Figure 3.30 (courtesy of Data IO Corp)

# Structure of a complex programmable logic device (CPLD)

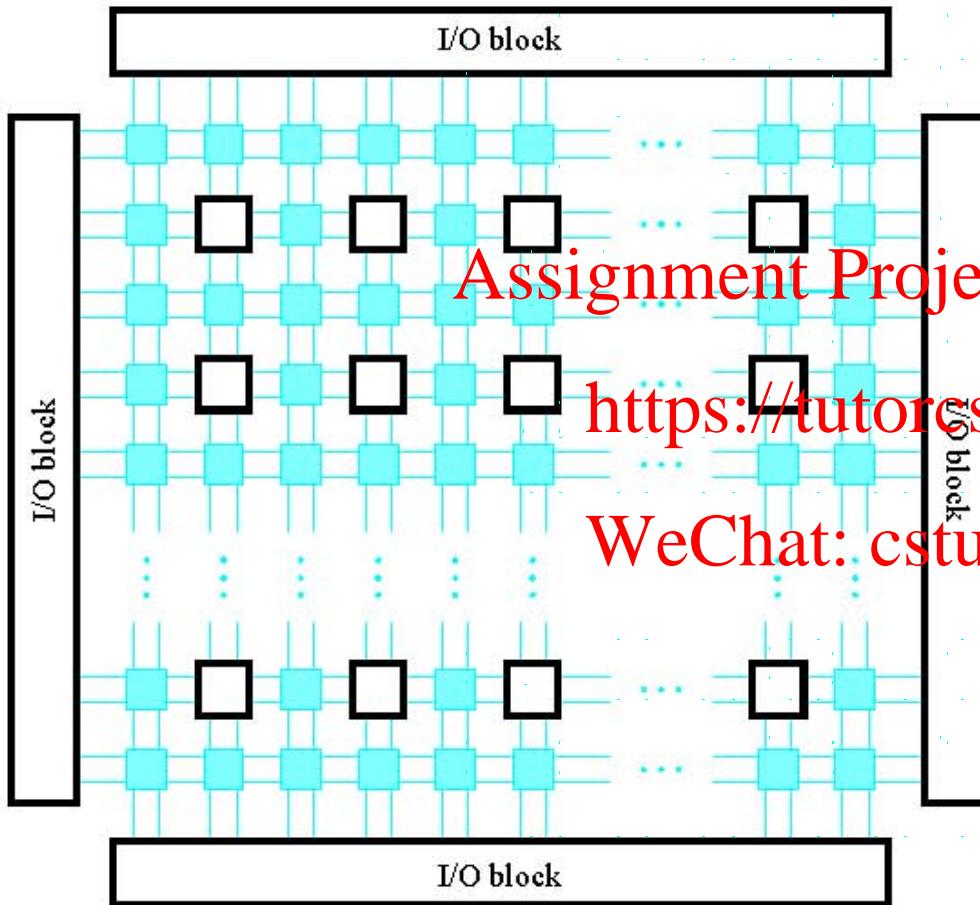


# A section of a CPLD



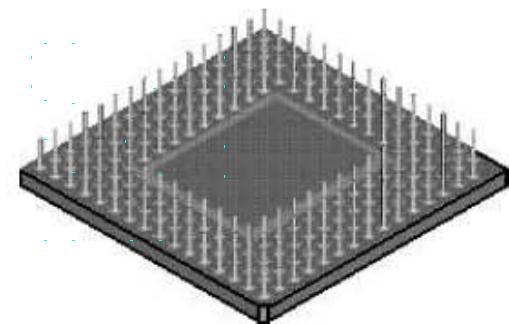
# A field-programmable gate array (FPGA)

□ Logic block    □ Interconnection switches



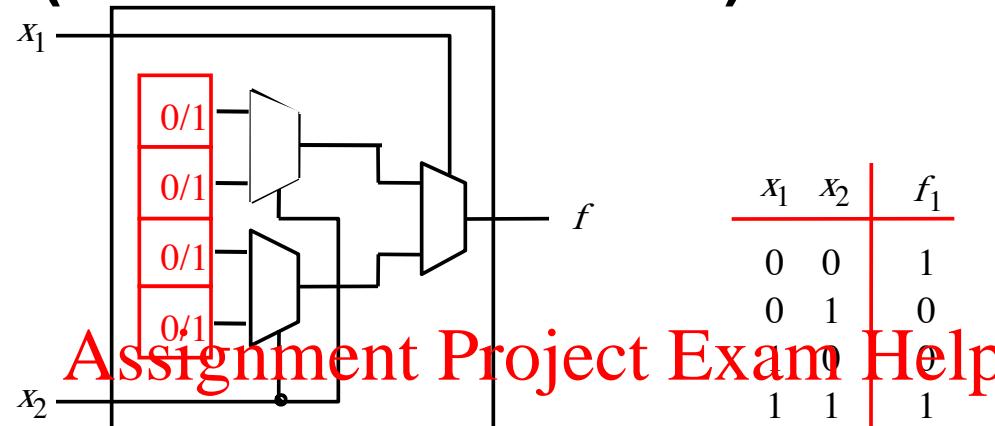
(a) General structure of an FPGA

- For cost and performance reasons, as few chips as possible are used to implement a design
  - 7400-series chips implement the equivalent of just a few two-input NAND gates (the prevalent metric for chip size)
  - An SPLD or CPLD macrocell represents about 40 equivalent gates; thus a PAL with 8 macrocells can accommodate a circuit that needs up to about 160 gates and a large CPLD with 500 macrocells can implement circuits of up to 10,000 equivalent gates
  - Modern FPGAs can be used to implement circuits of millions of equivalent gates in size



(b) Pin grid array (PGA) package (bottom view)

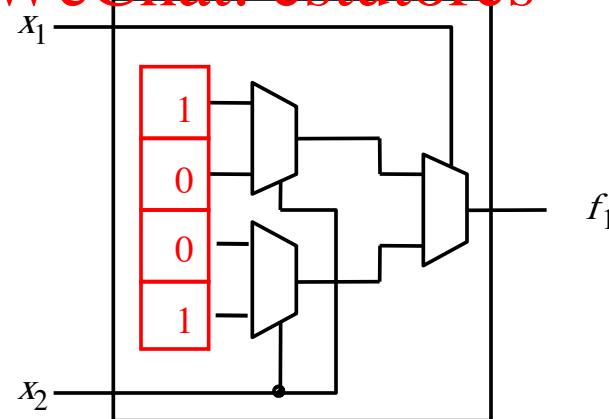
# A two-input lookup table (LUT) as an FPGA logic cell (recall from Week 1)



(a) Circuit for a two-input LUT

$$(b) f_1 = \bar{x}_1 \bar{x}_2 + x_1 x_2$$

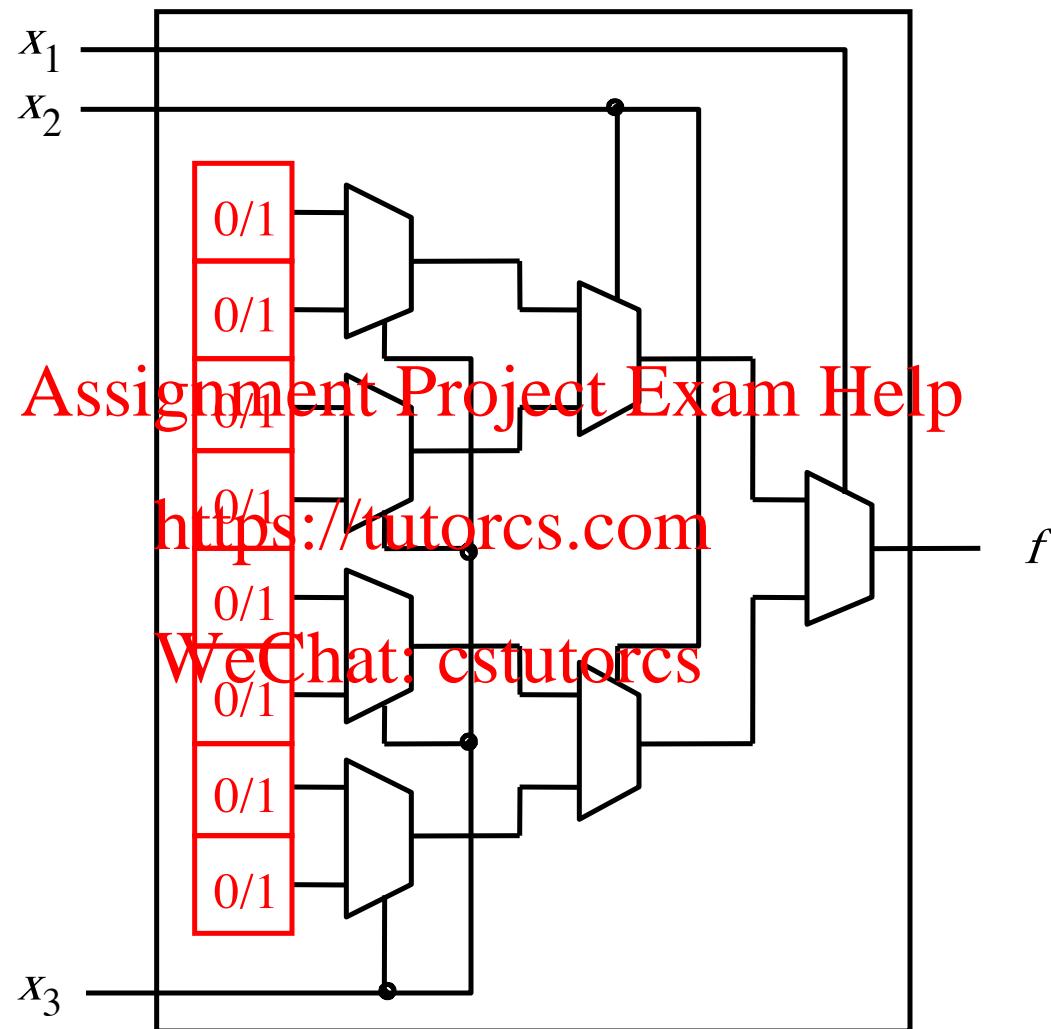
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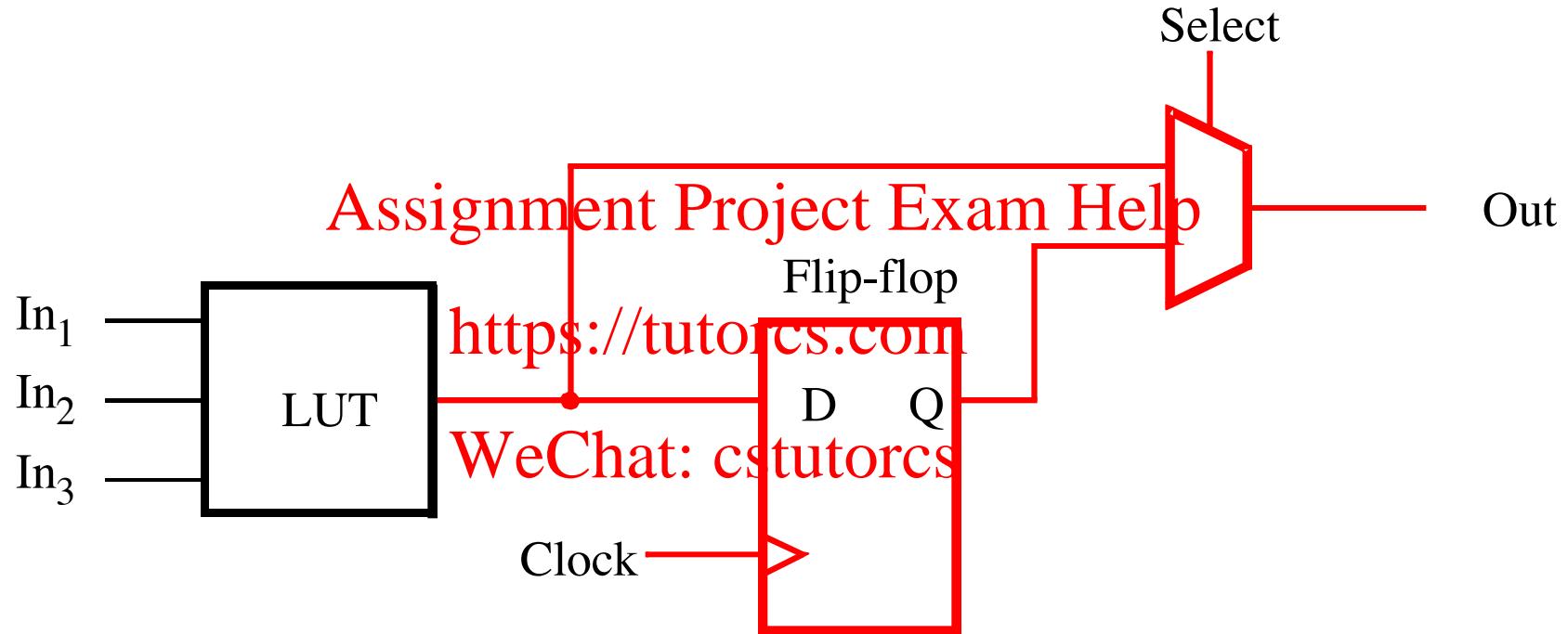
(c) Storage cell contents in the LUT

An  $n$ -input LUT serves as a small  $2^n$  address memory to implement an arbitrary Boolean function of  $n$  variables

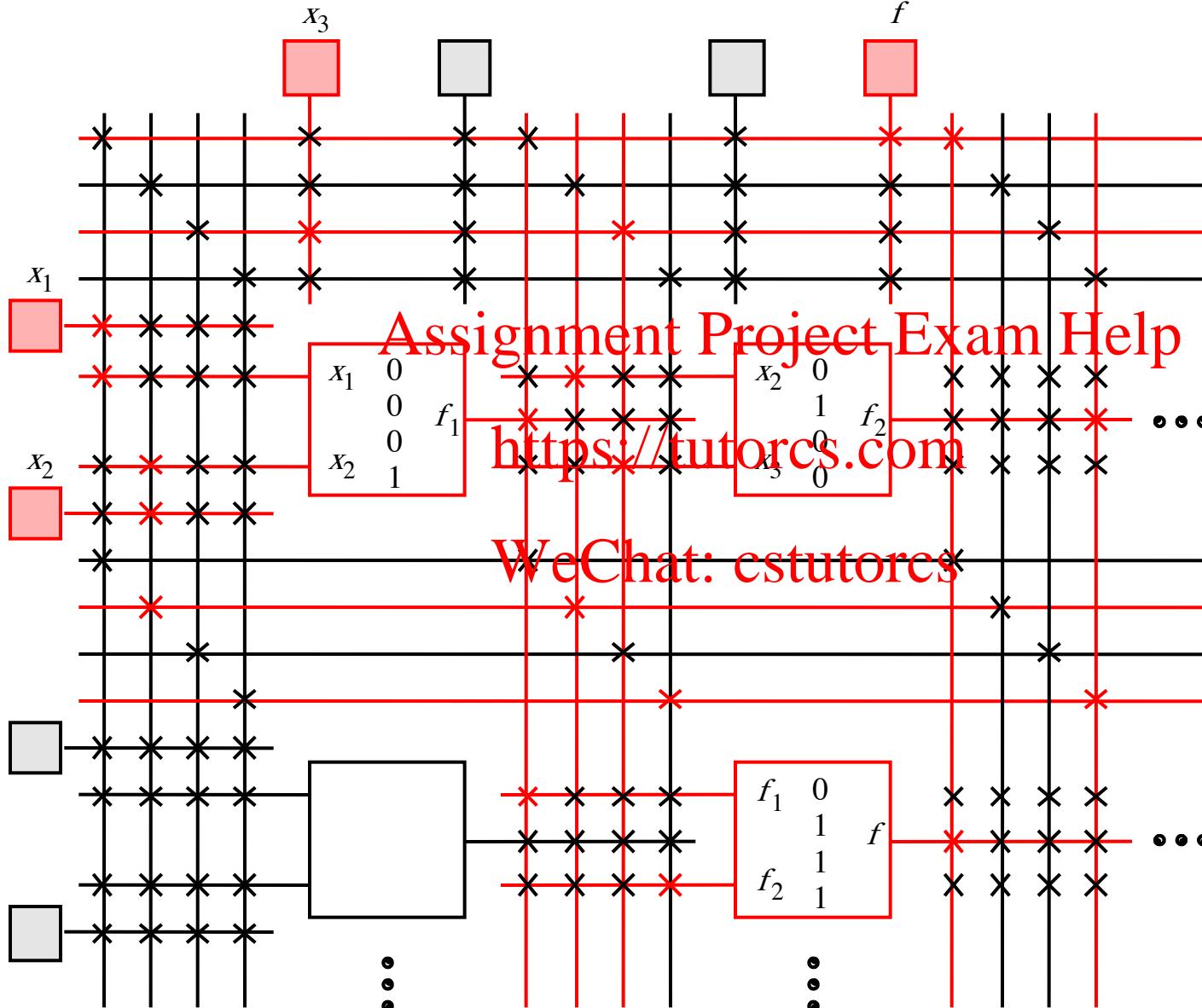
# A three-input LUT



# Inclusion of a flip-flop in an FPGA logic block



# A section of a programmed FPGA



In an FPGA, the LUT contents, routing switches and connection boxes are most commonly provided by SRAM cells

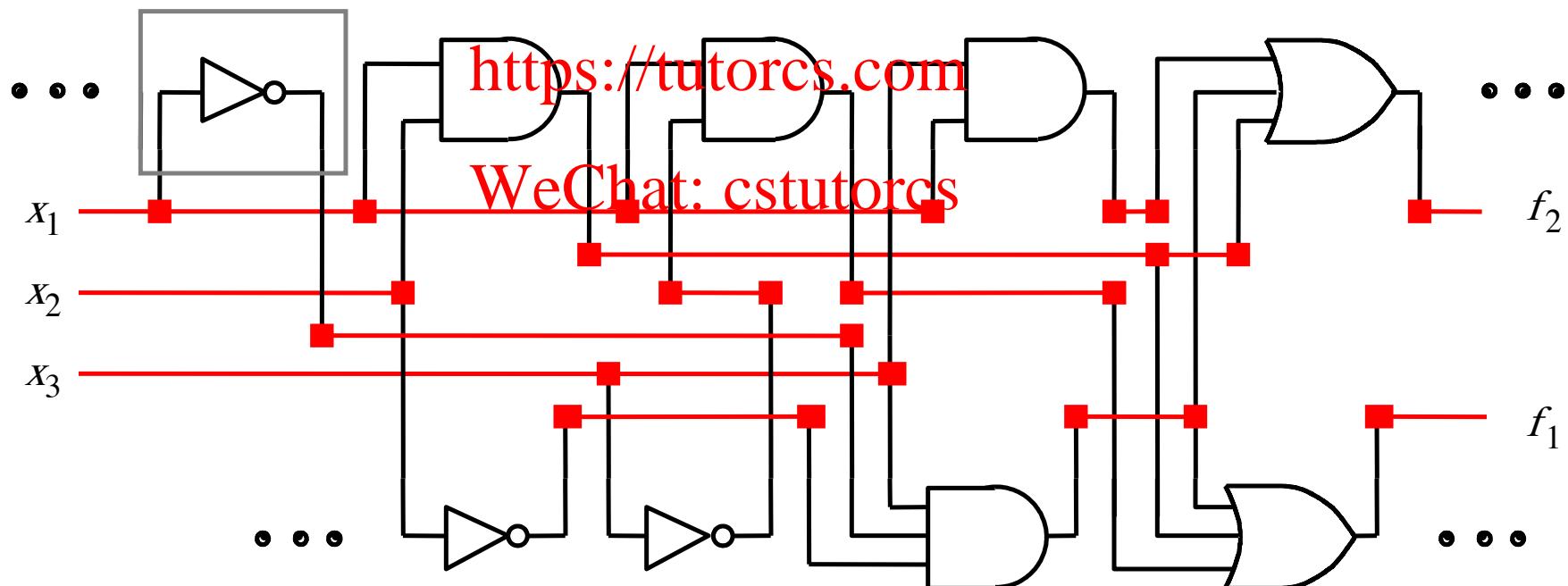
# Custom chips

- The key factor that limits the size of a circuit that can be accommodated in a PLD is the presence of the programmable switches
- Although the *switches afford PLDs their flexibility*, they *consume significant amounts of space* and thus *lead to increased cost, increased power consumption and reduced speed*
- To provide the largest number of logic gates, highest circuit speed or lowest power, a so-called *custom chip* can be manufactured
- Whereas PLDs are prefabricated and available off-the-shelf, *custom chips are created from scratch – the designer has complete flexibility to determine the number of transistors, their placement, and how they are to be interconnected*
- This enormous design effort leads to *significant expense*, and thus they are *only produced when standard parts do not meet requirements or the quantity that is to be sold justifies the cost*
  - Examples of products usually realized as custom chips include: *microprocessors, memory chips, GPUs, FPGAs, WiFi transceivers, digital broadcast receivers, engine management units,...*

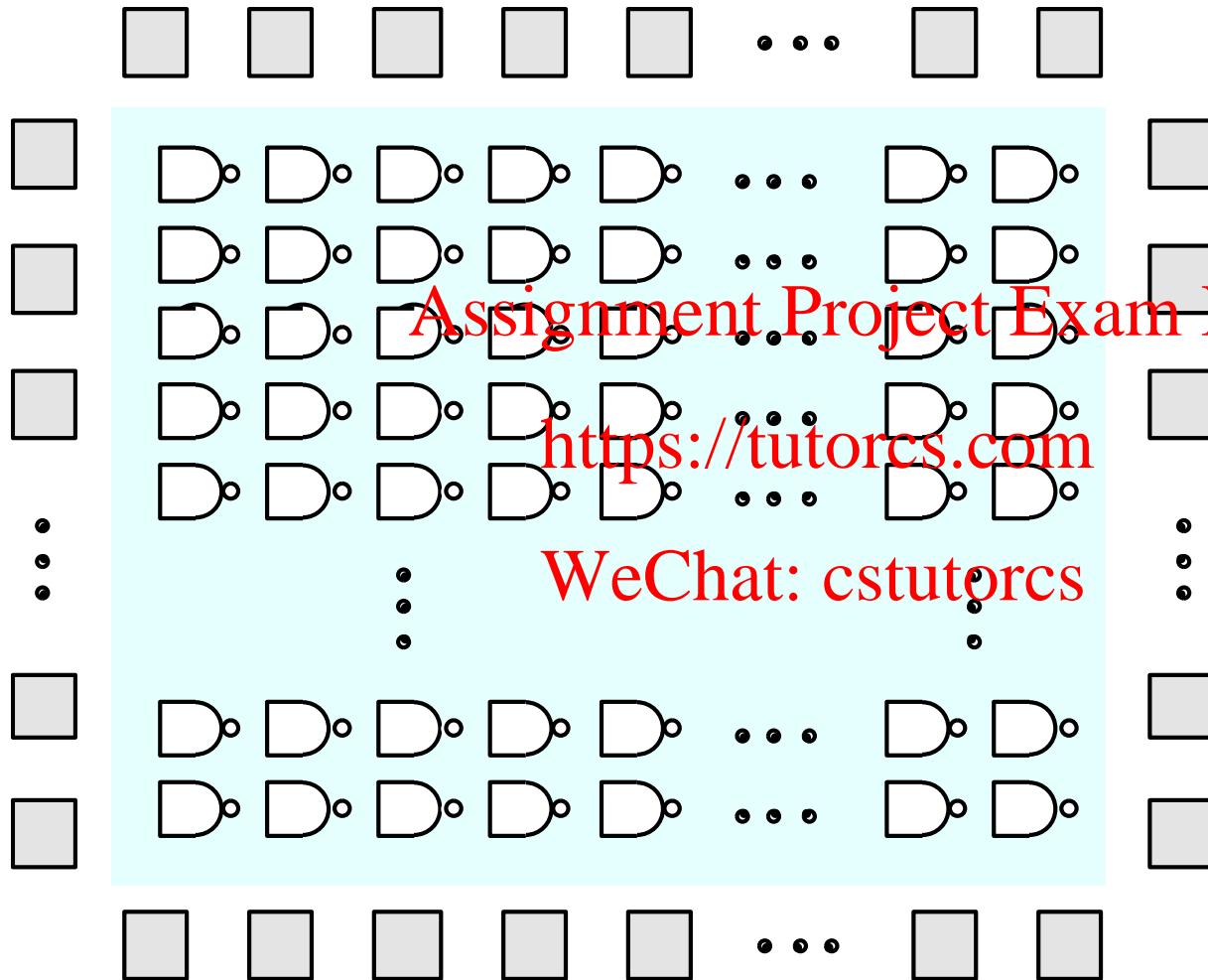
# A section of two rows in a standard-cell chip

- When the designer doesn't need complete flexibility over the layout of individual transistors, a technology known as *standard cells* can be used
- Chips made using this technology are also called *application-specific integrated circuits (ASICs)*
- A standard cell design uses standard gates available from a library and is thus mostly concerned with their interconnection rather than the layout of transistors to create the cell

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# A sea-of-gates gate array



In *gate array* technology, a predefined array of gates is prefabricated onto the silicon wafer.

The designer is then only concerned with the interconnections that are required to implement the design.

These are added in a late fabrication step. Such devices are referred to as *mask programmable*.

# The logic function $f_1 = x_2\bar{x}_3 + x_1x_3$ in a gate array

