COSI 131 – Spring 2020 Operating Systems Problem Set 2

Due Friday 02/14, 11:59pm on LATTE

- 1. What is the purpose of interrupts? What are the differences between a trap and an interrupt? Can traps be generated intentionally by a user program? If so, for what purpose?
- 2. Direct memory access is used for high-speed I/O devices in order to avoid increasing the CPU's execution load.
 - a. How does the CPU interface with the device to coordinate the transfer?
 - b. How does the CPU know when the memory operations are complete?
 - c. The CPU is allowed to execute other programs while the DMA controller is transferring data. Does this program interference are caused.

3 What is the purpose of the command interpreter? Why is it usually separate from the kernel? Would it be possible of the command interpreter? Why is it usually separate from the kernel? Would it be possible of the command interpreter? Why is it usually separate from the kernel? Would it be possible of the command interpreter? Why is it usually separate from the kernel? Would it be possible of the command interpreter? Why is it usually separate from the kernel? Would it be possible of the command interpreter? Why is it usually separate from the kernel? Would it be possible of the command interpreter? Why is it usually separate from the kernel?

- 4. Describe the actions taken by a Hernel to context-switch between processes.
- 5. Which of the following components of program state are shared across threads in a multithreaded process?
 - a. Register values
 - **b.** Heap memory
 - c. Global variables
 - d. Stack memory
- 6. Discuss how the following pairs of scheduling criteria conflict in certain settings.
 - a. CPU utilization and response time
 - b. Average turnaround time and maximum waiting time
 - c. I/O device utilization and CPU utilization
- 7. Consider a system implementing multilevel queue scheduling. What strategy can a computer user employ to maximize the amount of CPU time allocated to the user's process?

8. Consider the following set of processes, with the length of the CPU-burst time given in milliseconds:

Process	Burst Time	Priority
P1	10	3
P2	1	1
P3	2	3
P4	1	4
P5	5	2

The processes are assumed to have arrived in the order P1, P2, P3, P4, P5, all at time 0.

- **a** Draw four Gantt charts illustrating the execution of these processes using FCFS, SJF, a non- preemptive priority (a smaller priority number implies a higher priority), and Round Robin (quantum = 1) scheduling.
- **b.** What is the turnaround time of each process for each of the scheduling algorithms in part a?
- c. What is the waiting time of each process for each of the scheduling algorithms in part a?
- d Which a result of the man test of the model of the control of th
- 9. Consider a system running ten 1/0/tount tasks and one officinound task. Assume that the I/O-bound tasks issue an I/O operation once for every millisecond of CPU computing and that each I/O operation takes 10 milliseconds to complete. Also assume that the context switching overhead is 0.1millisecond and that all processes are long-running tasks. What is the CPU utilization for a round-lotte schedular whee STUTOTCS
 - a. The time quantum is 1 millisecond
 - b. The time quantum is 10 milliseconds