程序代写代做 CS编程辅导

Microprogram Design

- Use ASM from Figure 16 to design the Microprograms

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- See Symbolic/Binary Microprogram on next slide

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Symbolic/Binary Microprogram

Address	NXT ADD	MS	MC				TD	TA	TB	MB	FS	MD	RW	MM	MW
IF	EX0	CNT	—				—	—	—	—	—	—	NW	PC	NW
EXO	—	NXT	OPC				—	—	—	—	—	—	NW	—	NW
ADI	IF	NXT	NXA	NLI	NLP	NLP	DR	SA	—	Constant	$F = A + B$	FnUt	WR	—	NW
LD	IF	NXT	NXA	NLI	NLP	NLP	DR	SA	—	—	—	Data	WR	MA	NW
ST	IF	NXT	NXA	NLI	NLP	NLP	SA	SB		Register	—	—	NW	MA	WR
INC	IF	NXT	NXA	NLI	NLP	NLP	DR	SA	—	—	$F = A + 1$	FnUt	WR	—	NW
NOT	IF	NXT	NXA	NLI	NLP	NLP	DR	SA	—	—	$F = \overline{A}$	FnUt	WR	—	NW
ADD	IF	NXT	NXA	NLI	NLP	NLP	DR	SA	SB	Register	$F = A + B$	FnUt	WR	—	NW

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Address	NXT ADD	MS	MC	IL	PI	PL	TD	TA	TB	MB	FS	MD	RW	MM	MW
192	193	000	0	1	1	0	0	0	0	0	00000	0	0	1	0
193	000	001	1	0	0	0	0	0	0	0	00000	0	0	0	0
000	192	001	0	0	0	0	0	0	0	1	00010	0	1	0	0
001	192	001	0	0	0	0	0	0	0	0	00000	1	1	0	0
002	192	001	0	0	0	0	0	0	0	0	00000	0	0	0	1
003	192	001	0	0	0	0	0	0	0	0	00001	0	1	0	0
004	192	001	0	0	0	0	0	0	0	0	01110	0	1	0	0
005	192	001	0	0	0	0	0	0	0	0	00010	0	1	0	0

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This is not our control memory but similar

Indirect Instruction ASM

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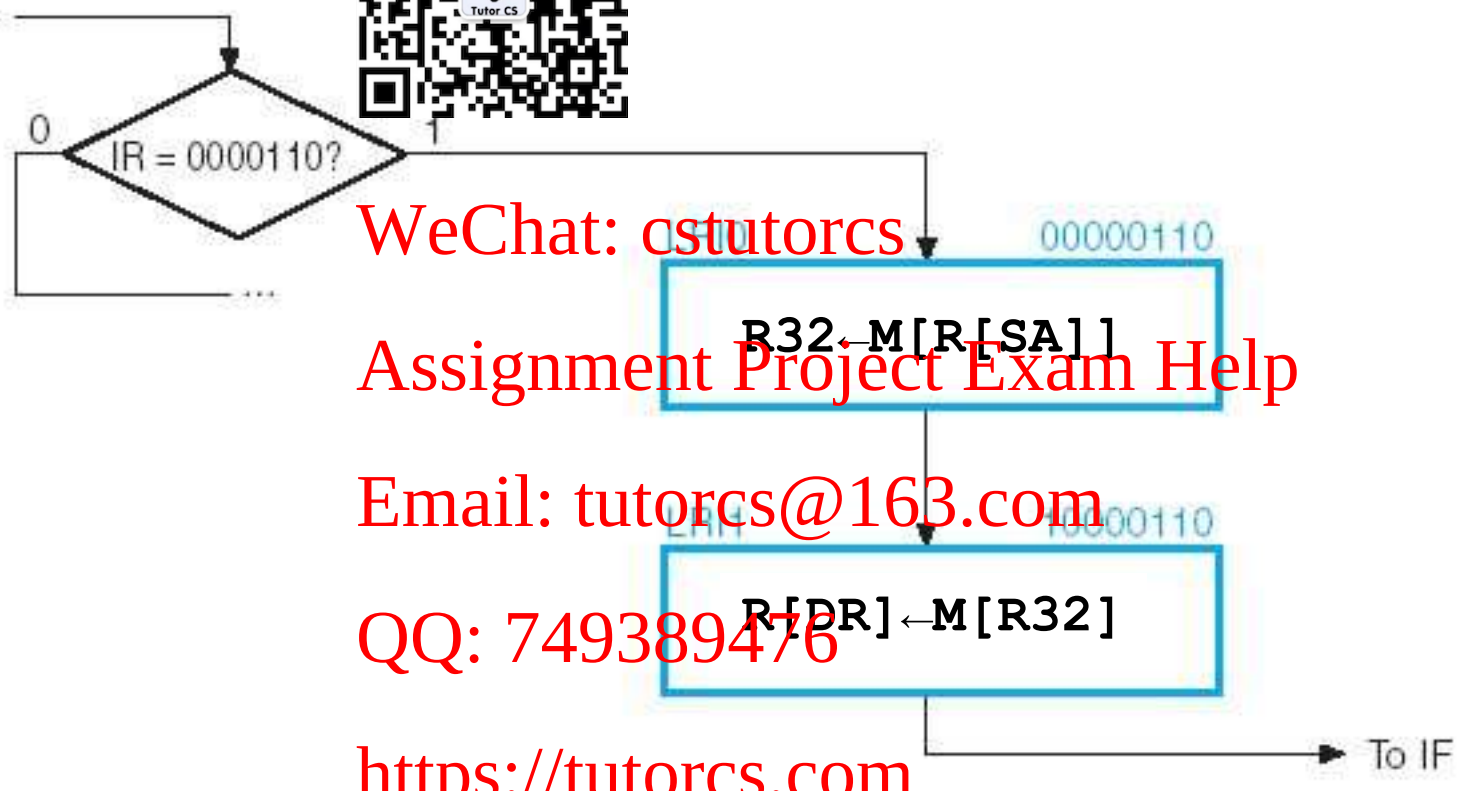

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Right-Shift Instruction ASM

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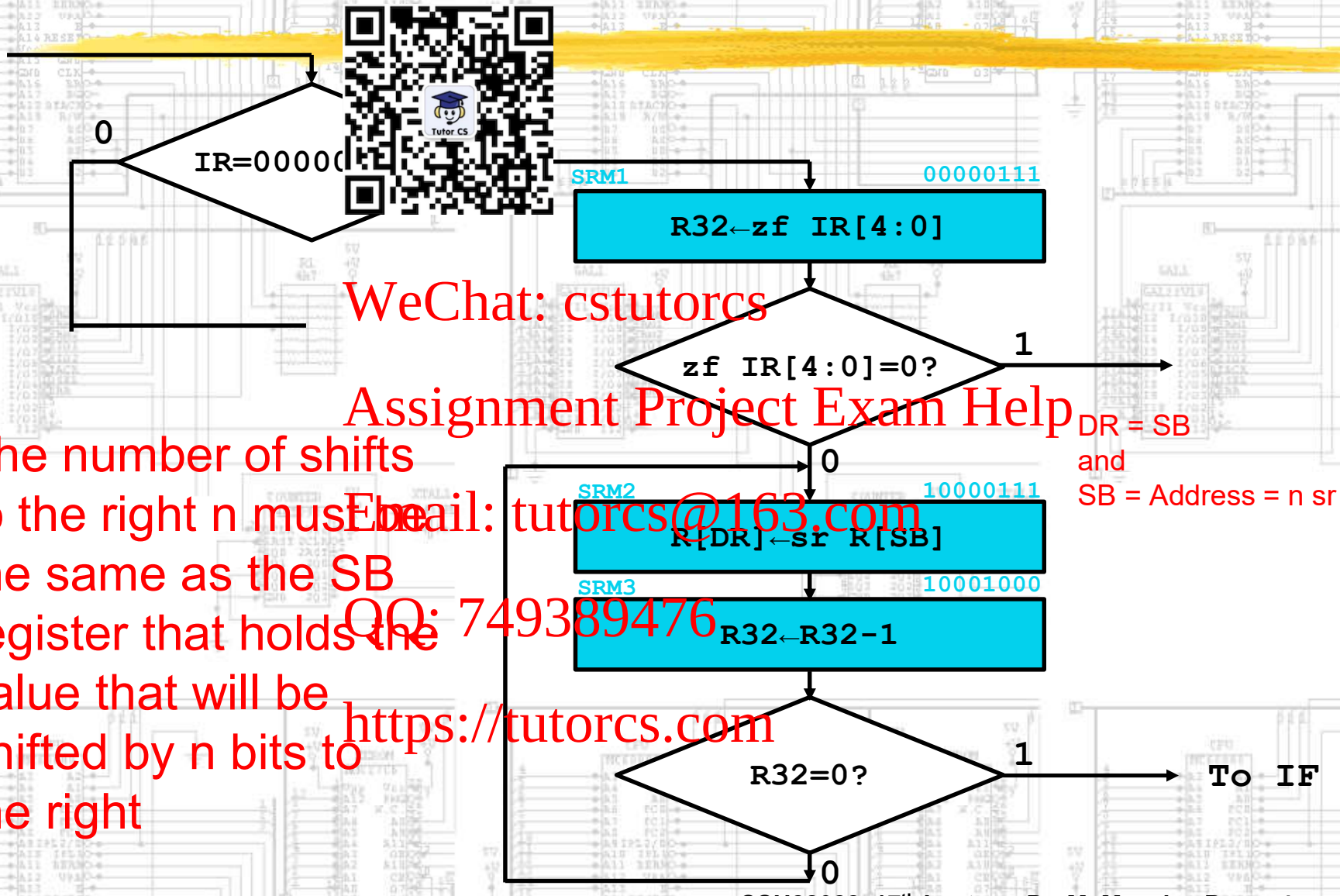

The number of shifts to the right n must be the same as the SB register that holds the value that will be shifted by n bits to the right

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Hardwired Multiple-Cycle Control

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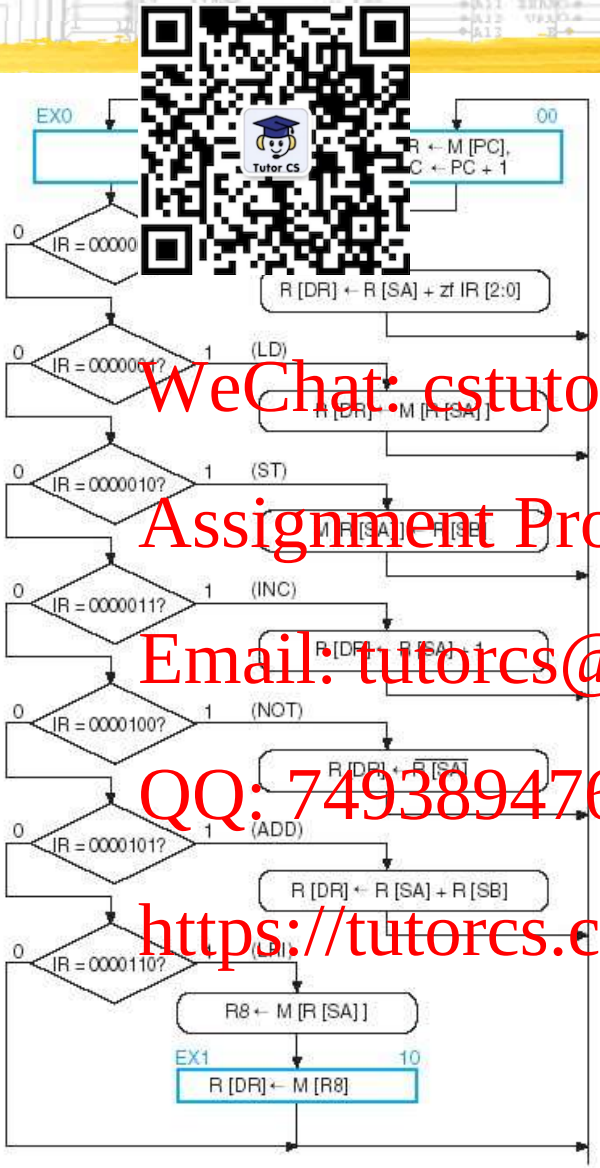

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Hardwired Control Unit

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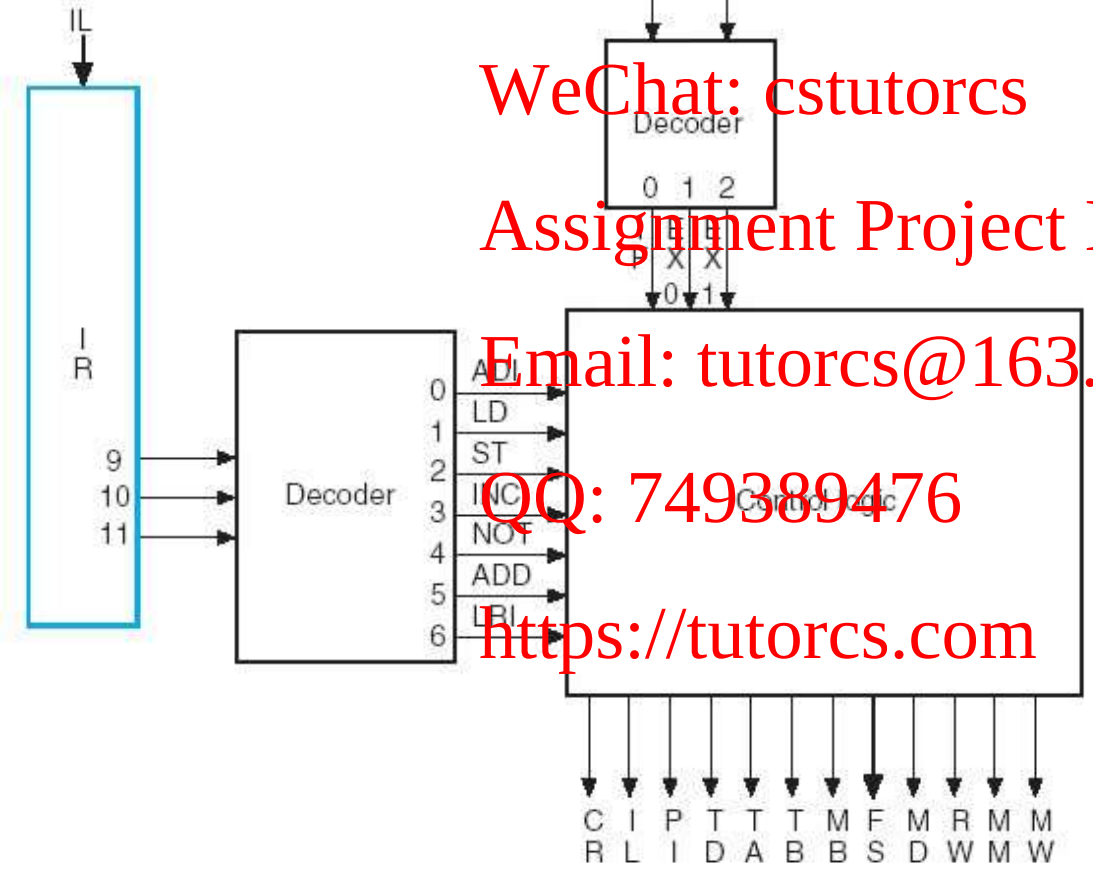

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Pipelined (based on single-cycle)

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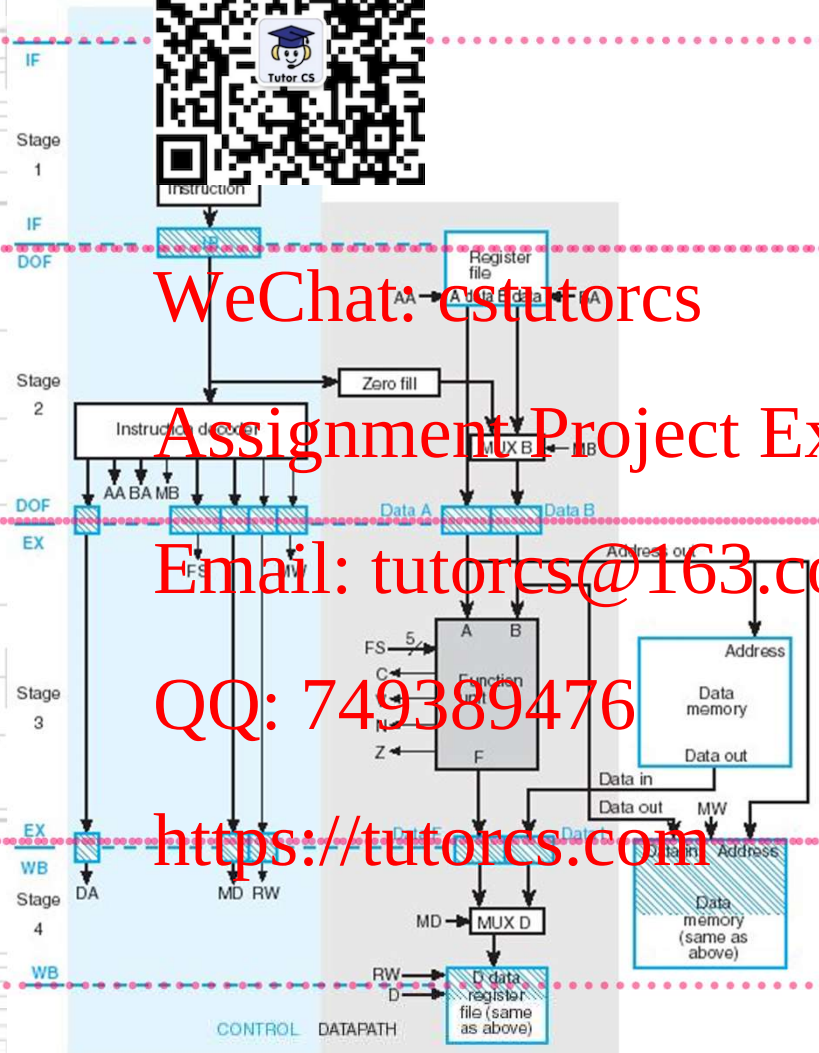
Instruction Fetch

Decode and Operand Fetch

Execution

Write-back



Pipelined Execution Pattern

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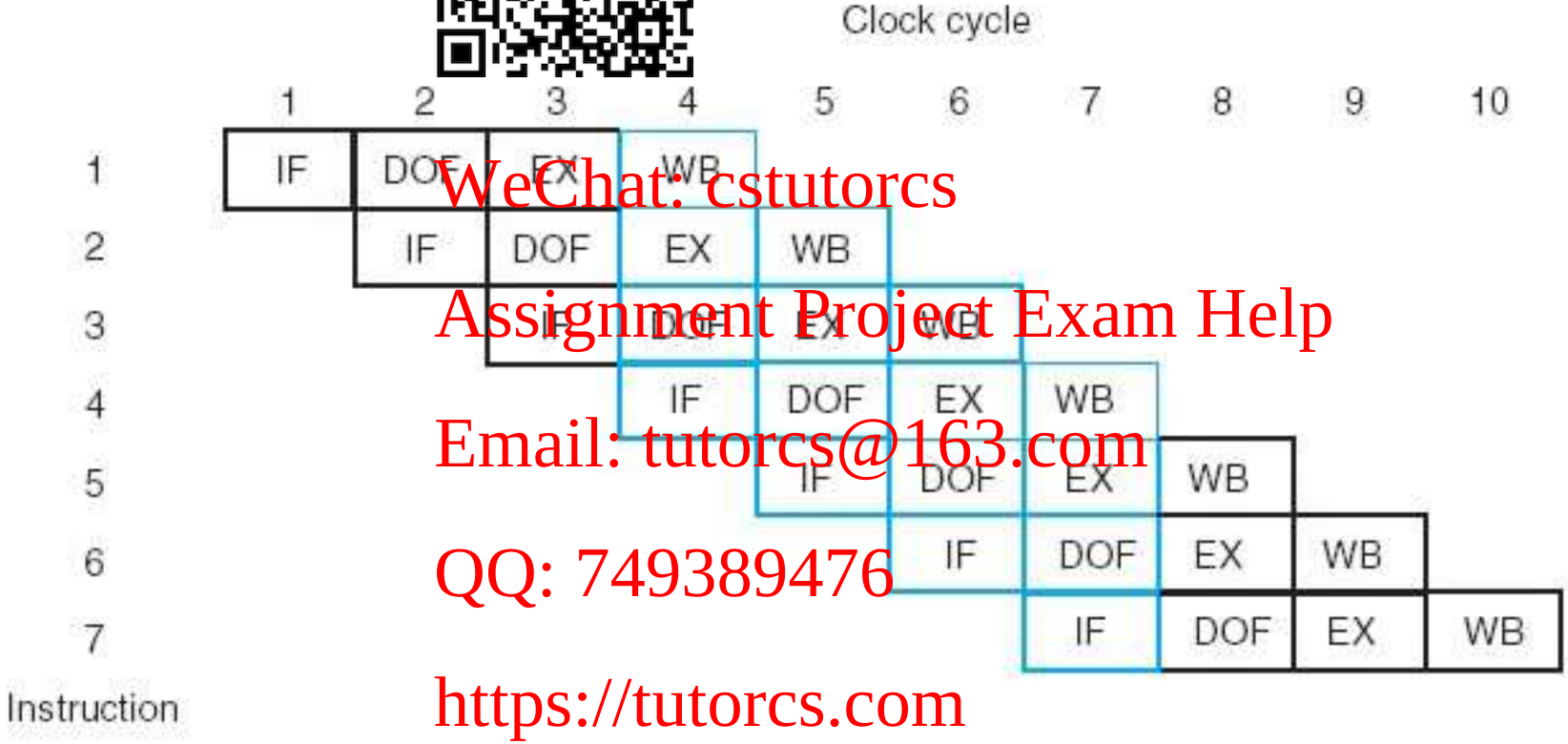

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Computer Architecture and Microprocessor Systems

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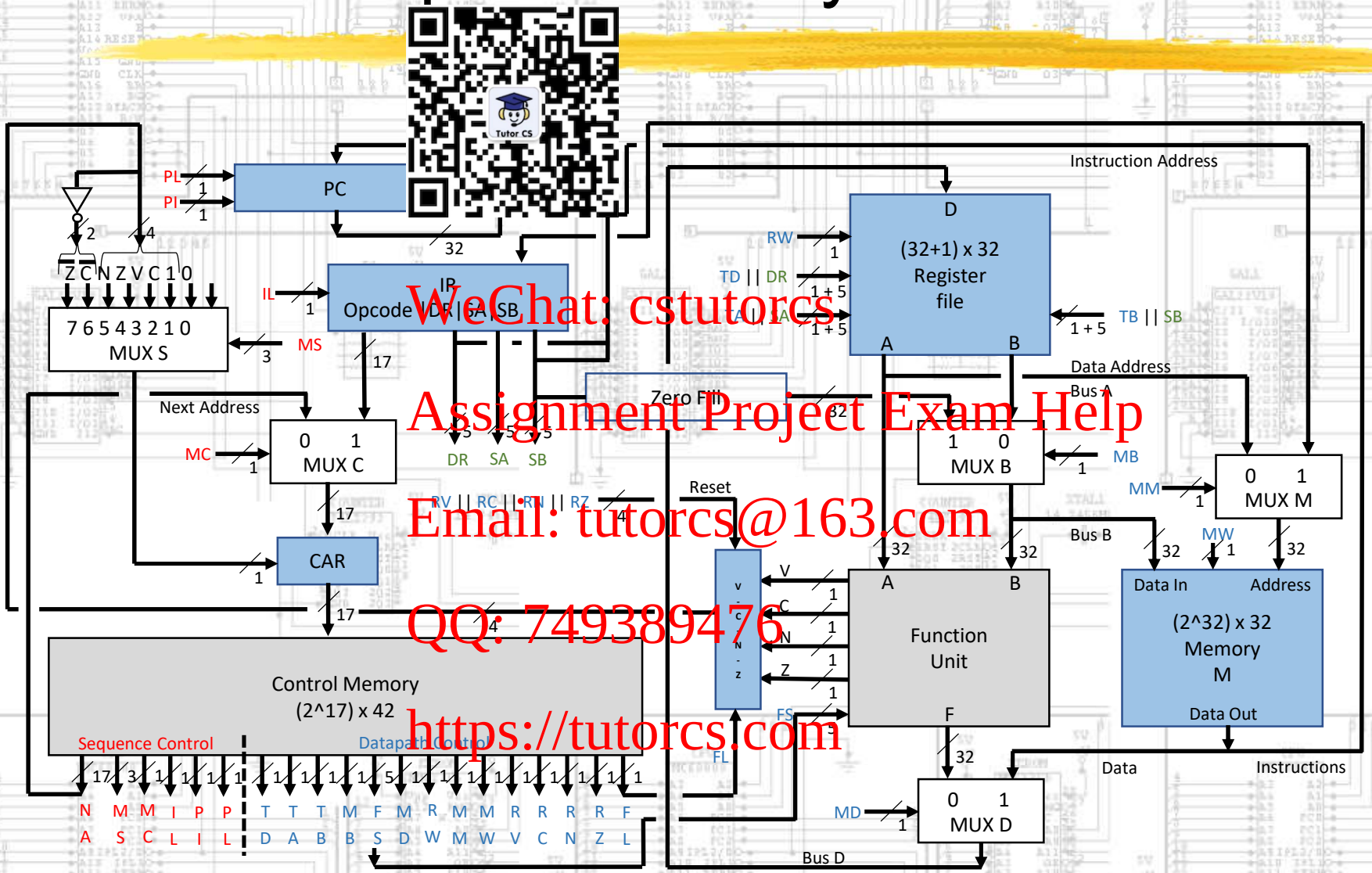

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