



ECE 2560 Introduction to Microcontroller-Based Systems

~~程序代写代做 CS 编程辅导~~



Lecture 5

~~Memory Map Assignment Project Exam Help~~

of **MSP430FR6989**

~~QQ: 749389476~~

<https://tutorcs.com>

~~WeChat: cstutorcs~~

~~Assignment Project Exam Help~~

Email: tutorcs@163.com



Coming Up Next

~~程序代写代做 CS 编程辅导~~

Friday we will start coding Finally!!

For that you will need you  ad and Code Composer Studio (CCS)

Posted a guide on how to download CCS – Find it under Resources in Carmen and follow the steps carefully!

[CCS Installation Guide.pdf](#)

[Download CCS Installation Guide.pdf \(258 KB\)](#)

Assignment Project Exam Help

Email: tutorcs@163.com

[Code Composer Studio Download Instructions](#)

QQ: 749389476

- Go to <https://www.ti.com/tool/CCSTUDIO>
- Or type 'Code Composer Studio Download' into your search engine and navigate to the first result
- Go to the Downloads section and select Download Options

<https://tutorcs.com>

Evaluate in the cloud
Download options



- Select the installer for whichever operating system your machine is running (web installer is recommended because the offline installer is a very large download)



Last Time: Units of Memory

程序代写代做 CS 编程辅导

Pop Quiz: What is a kilobyte?

Is it $1\text{ kB} = 1000 \text{ B}$?



Is it $1\text{ kB} = 1024 \text{ B}$?

The SI unit prefix k (kilo) is 1000 !

Powers of 10

M (mega) is always 10^6 !

WeChat: cstutorcs

But, there is a reason for measuring memory in powers of 2

Assignment Project Exam Help

Hence the prefixes for binary multiples: “**kilo binary**” or **kibi** written as **Ki**

Email: tutorcs@163.com

1 KiB = 1024 B = 2^{10} B

1 MiB = 1,048,576 B = 2^{20} B

...

<https://tutorcs.com>

e.g., see <https://physics.nist.gov/cuu/Units/binary.html>

Last Time: Essential Components of an MCU



程序代写代做 CS编程辅导

A **microcontroller** contains at the bare minimum

- Central processing unit (CPU)
- Program memory – non-volatile
- Data memory – usually RAM
- Clock
- Address and data busses
- Input and output (I/O) ports

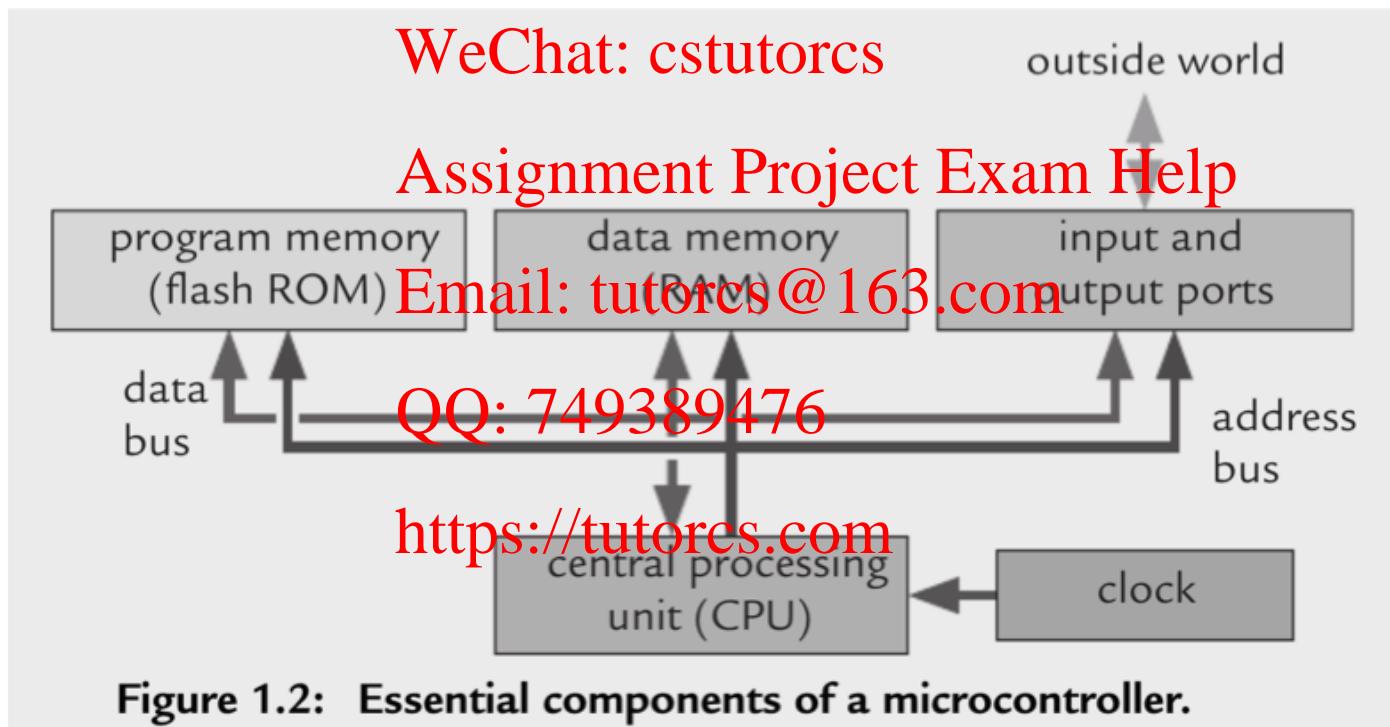
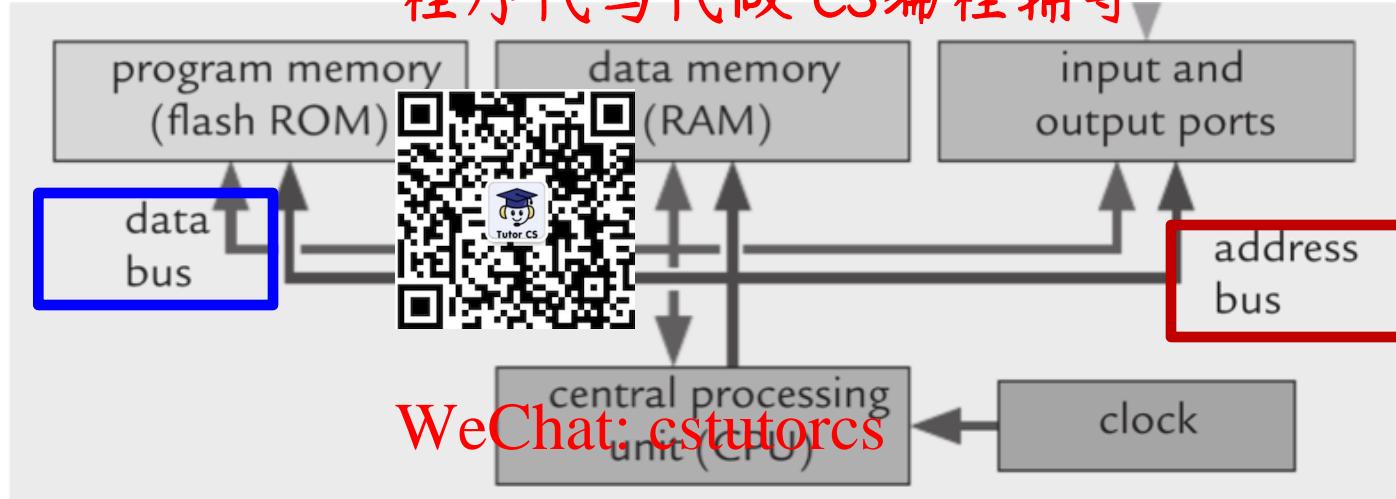


Figure 1.2: Essential components of a microcontroller.

Last Time: Essential Components of an MCU



程序代写代做 CS 编程辅导



All memory is linked to the CPU by busses for data, address and control

The width of the **data bus** determines the architecture of the MCU
Email: tutorcs@163.com

e.g., 16-bit processor

The width of the **address bus** determines the size of the memory that can be addressed
QQ: 749389476

e.g., 16 bits can address $2^{16} = 65,536$ different memory locations in **total**

<https://tutorcs.com>

i.e., program **and** data memory **and** peripheral registers

If each individual byte is addressed, we can address **65,536 B = 64 KiB**

The MSP430FR6989 Launchpad



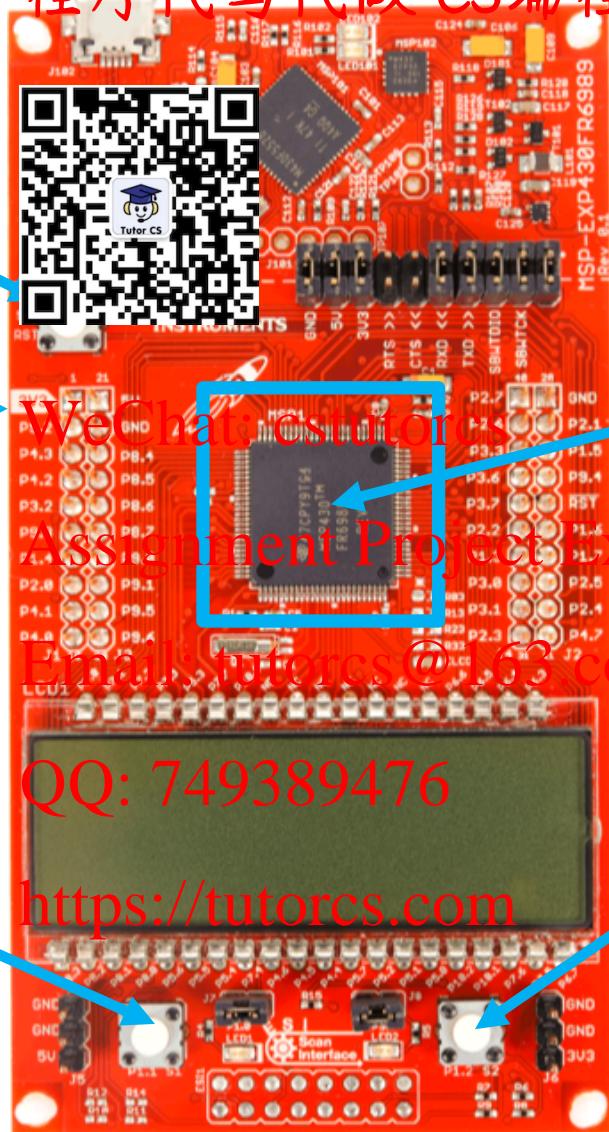
程序代写代做 CS 编程辅导

Reset Button RST S3

Power $V_{CC} = 3.3\text{ V}$

Push Button S1

LEDs Red & Green



eZ-FET emulator

MSP430FR6989IPZ
100 Pins

40 Headers with access
to selected pins

Push Button S2

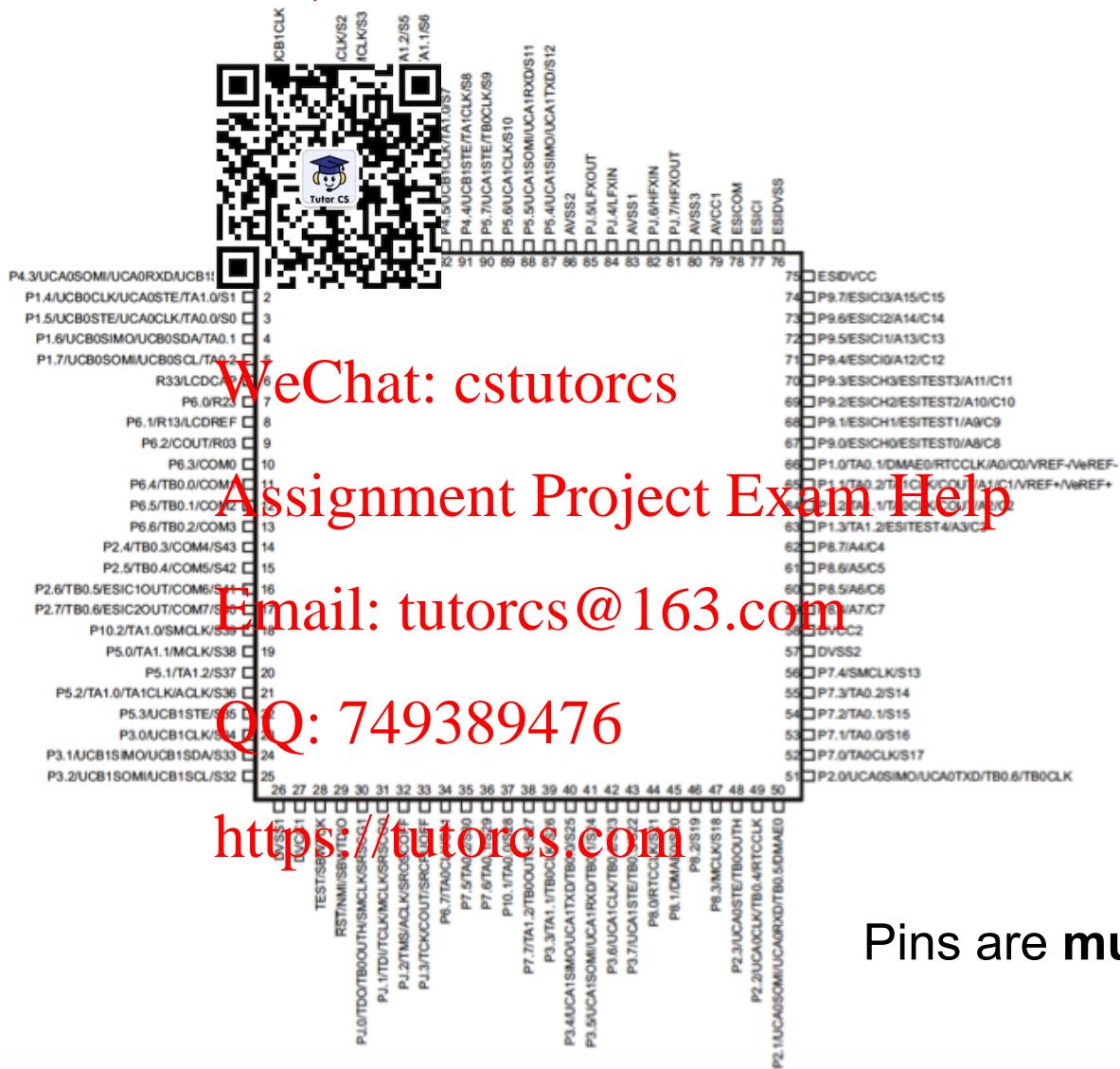
Ground



MSP430FR6989IPZ Pinout

~~程序代写代做 CS 编程辅导~~

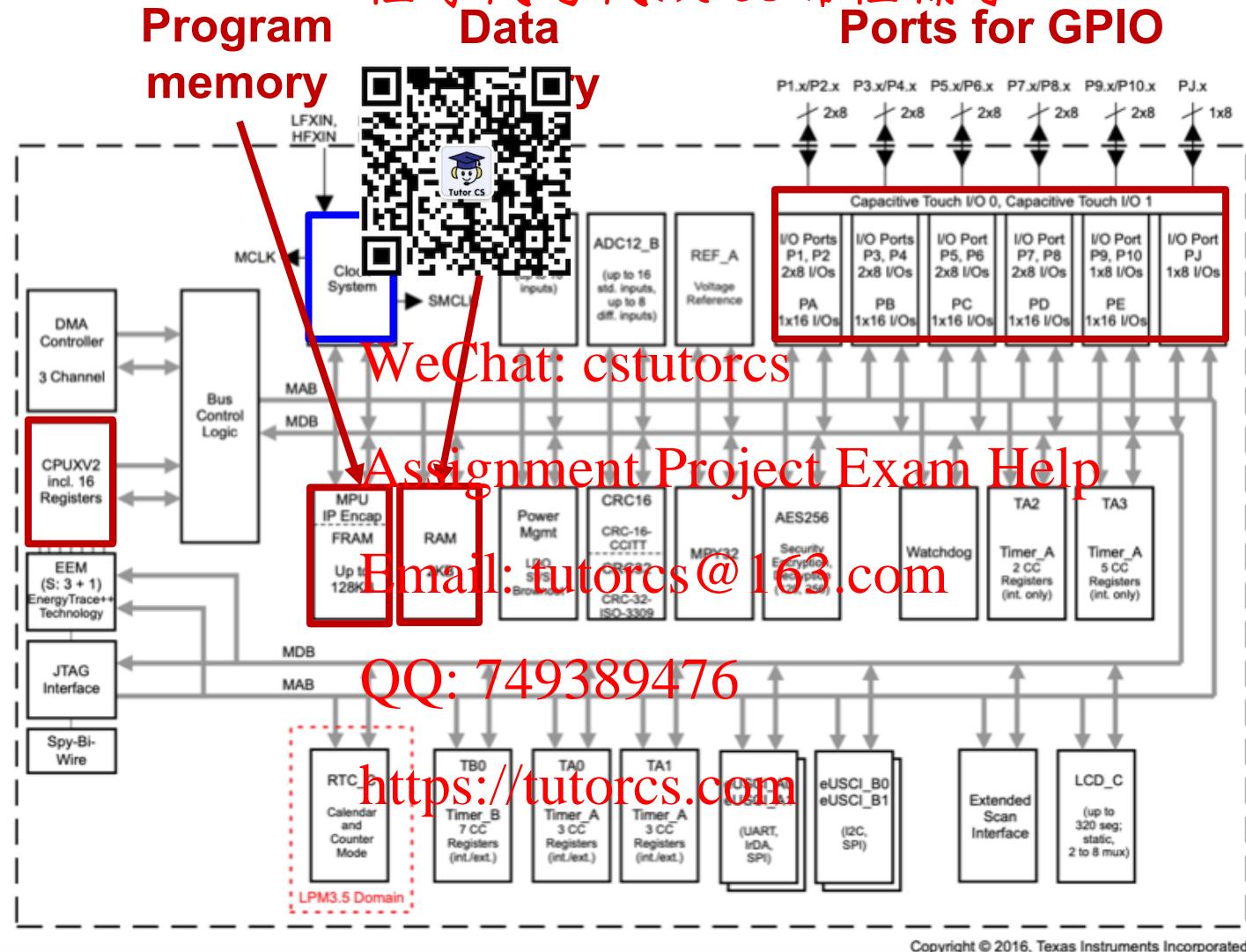
slas789d.pdf





Inside MSP430FR6989

程序代写代做 CS 编程辅导





Memory Map

~~程序代写代做 CS 编程辅导~~

We can view the memory as a pile of **registers**

Each register holds 8 bits

Register 0
Register 1
.
.
.



The registers reside in different locations

- RAM registers (Data memory – 2048 B)
- FRAM registers (Program memory – 48 kB)
- 8-bit peripheral registers (GPIO P1-P10)
- 16-bit peripheral registers

Assignment Project Exam Help

Every register (except the 16 core registers in the CPU) is mapped to a unique 16-bit memory address

⇒ **Memory mapping**
QQ: 749389476

This is a design choice – all registers are on the **same address bus**

<https://tutorcs.com>

There are two different architectures

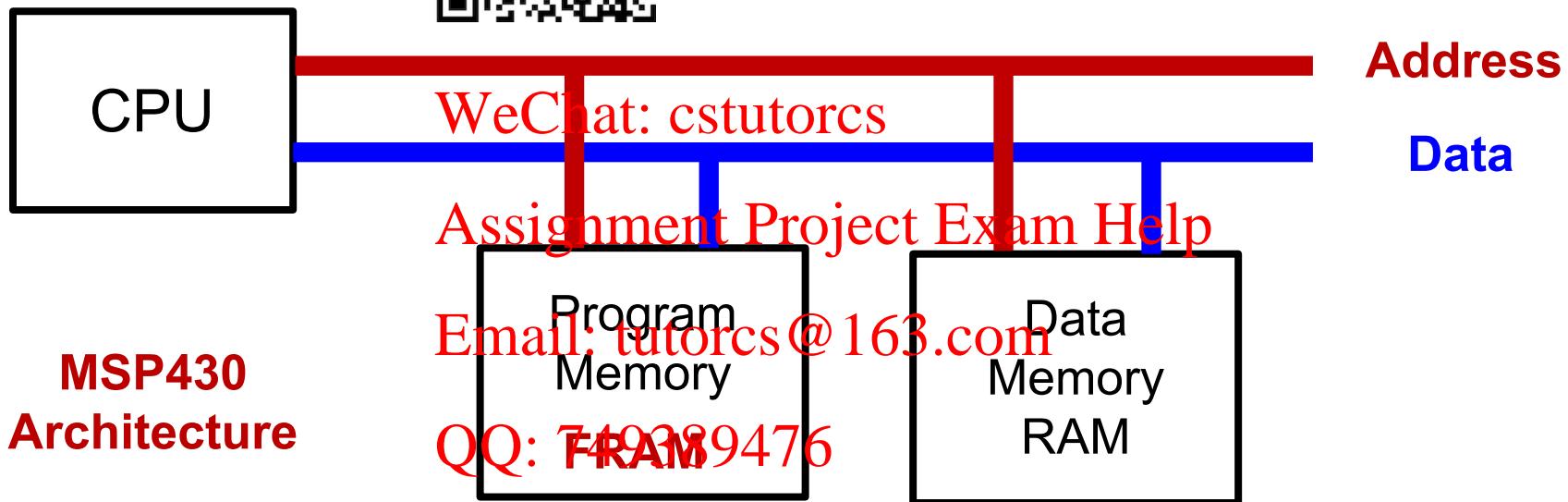
- von Neumann Architecture
- Harvard Architecture



von Neumann Architecture

~~程序代写代做 CS 编程辅导~~

In the **von Neumann Architecture** (aka Princeton Architecture) the one data and one address bus connect the CPU with the program and the data memory
⇒ There is one set of addresses



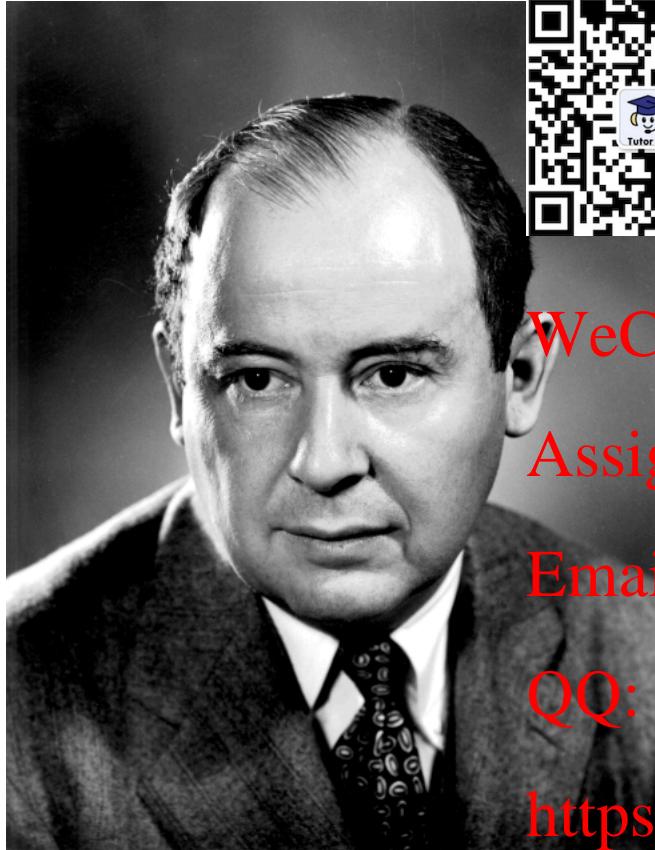
<https://tutorcs.com>

Same data and address bus and **same** set of addresses for program and data memory and all other peripheral registers



John von Neumann

~~程序代写代做 CS 编程辅导~~



903 – 1957

Hungarian-American polymath

Mathematician

- Computer scientist

WeChat: cstutorcs

Quantum physicist

- Economist (Game theory)

- Engineer

Email: tutors@163.com

Institutions

- Princeton University

QQ: 749389476

- Manhattan Project

<https://tutors.com> US Atomic Energy Commission

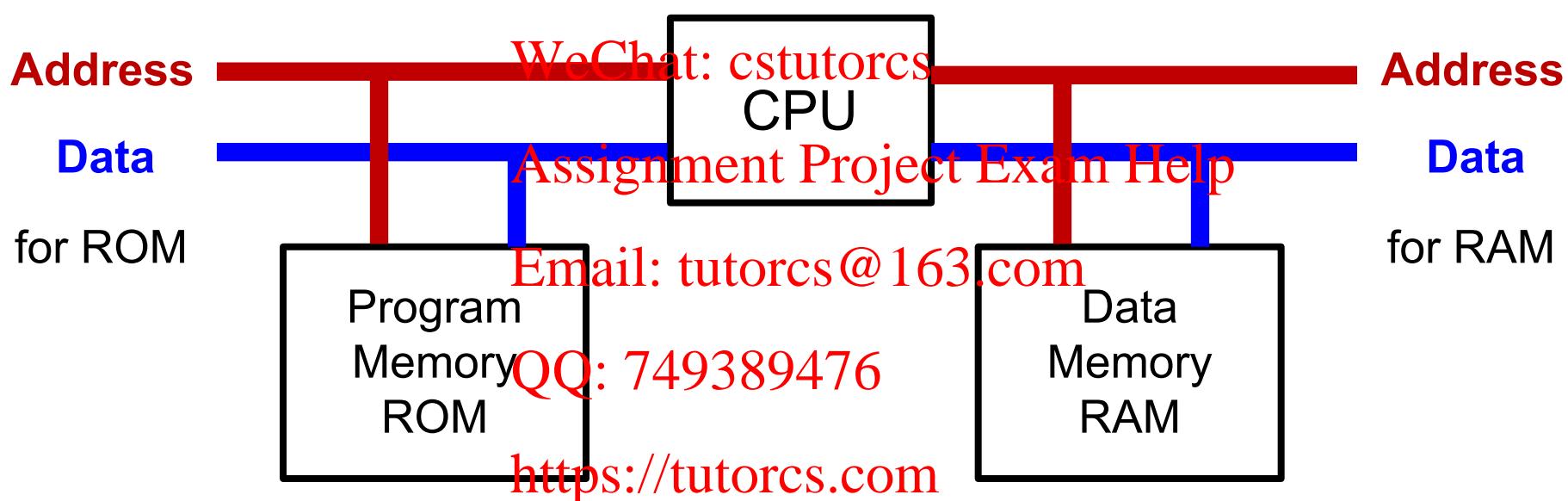


Harvard Architecture

~~程序代写代做 CS 编程辅导~~

In the **Harvard Architecture** the program and data memory are served by different data and address busses.

⇒ Program and data memory have different address sets, widths etc.



There are also separate control busses serving RAM and ROM

v. Neumann vs. Harvard Architecture



程序代写代做 CS 编程辅导

Harvard Architecture



Efficient

- Simultaneous access to program and data memory

WeChat: cstutorcs

But complex

- Constants (in program memory) and variables (in data memory) live in different address spaces and must be treated differently

QQ: 749389476

<https://tutorcs.com>

von Neumann Architecture

Less efficient

- Program and data memory must be accessed one at a time
- von Neumann bottleneck

Assignment Project Exam Help

Email: tutorcs@163.com

Simpler

- Constants (in program memory) and variables (in data memory) are addressed in the same way

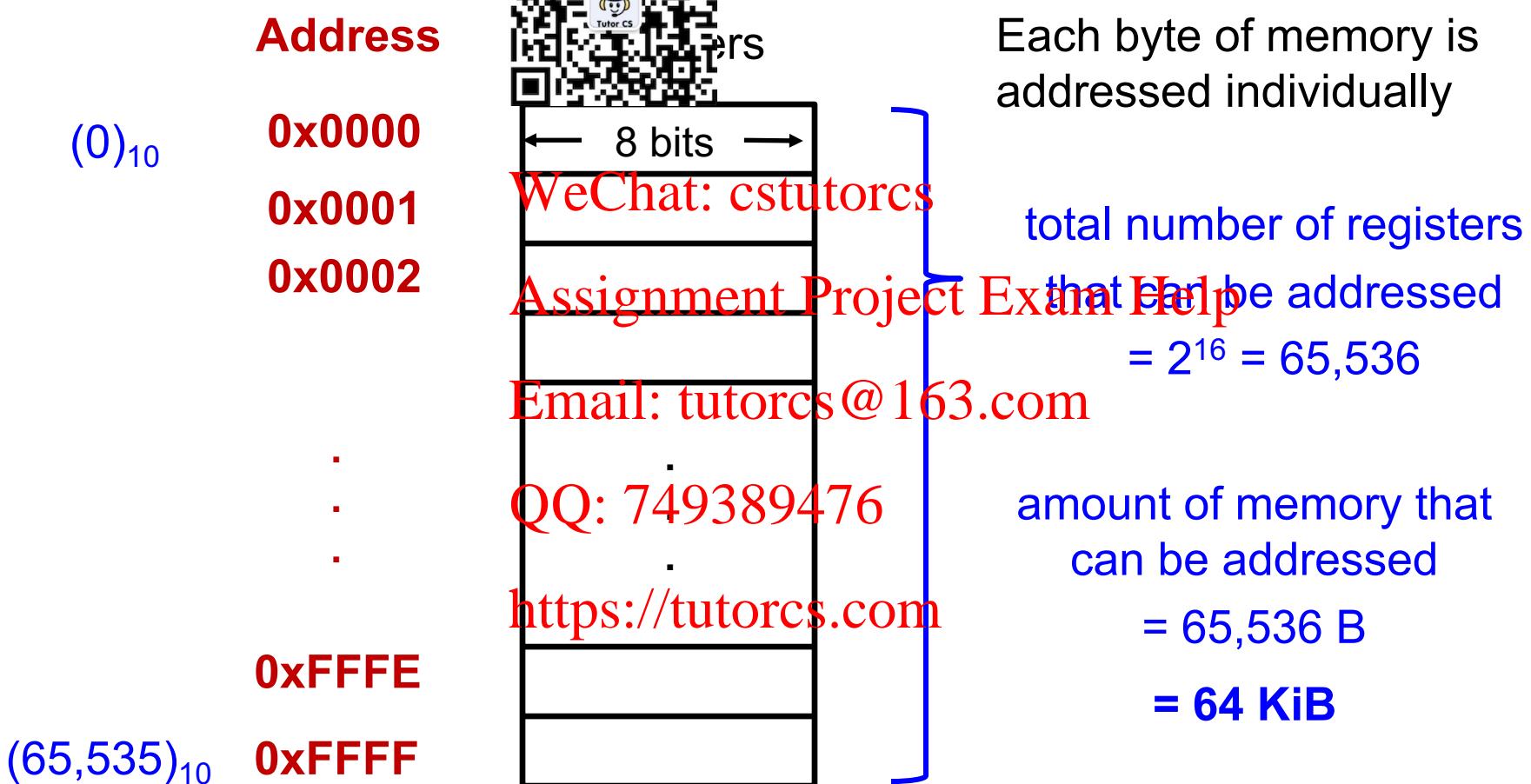


Memory Map

程序代写代做 CS 编程辅导

The **address bus** is 16 bits wide, i.e., each address is 16 bits

Addresses are expressed as numbers from 0x0000 to 0xFFFF

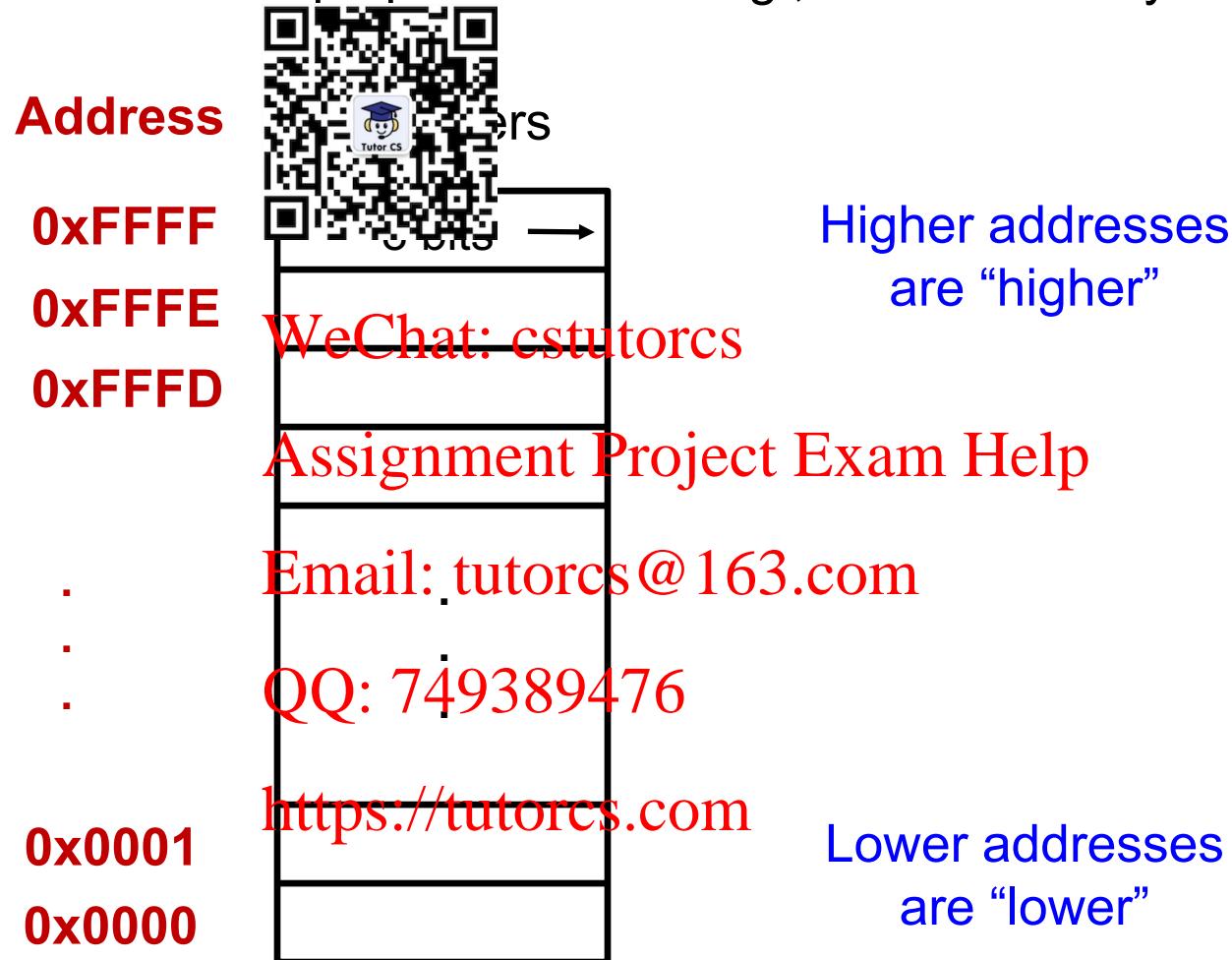




Memory Map

~~程序代写代做 CS 编程辅导~~

Some sources draw the map upside down e.g., TI uses this style





Word Addressing

程序代写代做 CS 编程辅导

The **data bus** is 16 bits wide \Rightarrow 16-bit architecture

The data bus can transfer



- a **byte** (i.e., 8 bits)

or

- a **word** of 16 bits

is addressed

address corresponds to a byte

Not so fast! What is the address of a word???

WeChat: cstutorcs

The **address of a word** is address of the byte with the lower address

Assignment Project Exam Help

\Rightarrow the address of a word is always even

- Bytes with addresses 0x0000 and 0x0001 \Rightarrow word with address 0x0000
- Bytes with addresses 0x0002 and 0x0003 \Rightarrow word with address 0x0002
- ...
- Bytes with addresses 0xFFFF and 0xFFFF \Rightarrow word with address 0xFFFF

Email: tutorcs@163.com

QQ: 749389476

Bytes w/ addresses 0x0001 and 0x0002 cannot be accessed as a word



Endianess

~~程序代写代做 CS 编程辅导~~

Bytes with addresses 0x0000 and 0x0001 => word with address 0x0000

How is the word (two bytes) stored over these two addresses?

e.g.,

word **0x1234** **0x12** most significant byte (MSB or HSB)

0x34 lower significant byte (LSB)

WeChat: cstutorcs

There are two ways of storing these bytes over two addresses

Assignment Project Exam Help

HSB at lower address
LSB at higher address

HSB at higher address
LSB at lower address

0x0201
0x0200

0x34
0x12

QQ: 749389476

<https://tutorcs.com>

0x12
0x34

0x0201
0x0200

Big-Endian Ordering

Little-Endian Ordering



Endiannes

程序代写代做 CS编程辅导

How is the word (two bytes) ordered over these two addresses?

e.g.,

word **0x1234** **0x12** most significant byte (MSB or HSB)
 0x34 least significant byte (LSB)



There are two ways of storing these bytes over two addresses

Big-Endian Order **Assignment Project** **Little-Endian Order**

HSB at lower address
LSB at higher address

HSB at higher address
LSB at lower address

Email: tutorcs@163.com

0x0200
0x0201

0x12
0x34

QQ: 749389476

<https://tutorcs.com>

0x34
0x12

0x0200
0x0201



Little-Endian Ordering

~~程序代写代做 CS 编程辅导~~

The MSP430 uses **little-endian ordering** – more common format today

word **0x1234** is stored in



HSB at higher address

LSB at lower address

WeChat: cstutores



0x0201

0x0200

In CCS addresses increase from left to right **when displaying bytes**

Assignment Project Exam Help

0x0200

Email: tutorcs@163.com

0x34

0x12

QQ: 749389476

⇒ **0x1234**

No issue when **displaying words**

0x0200

0x1234

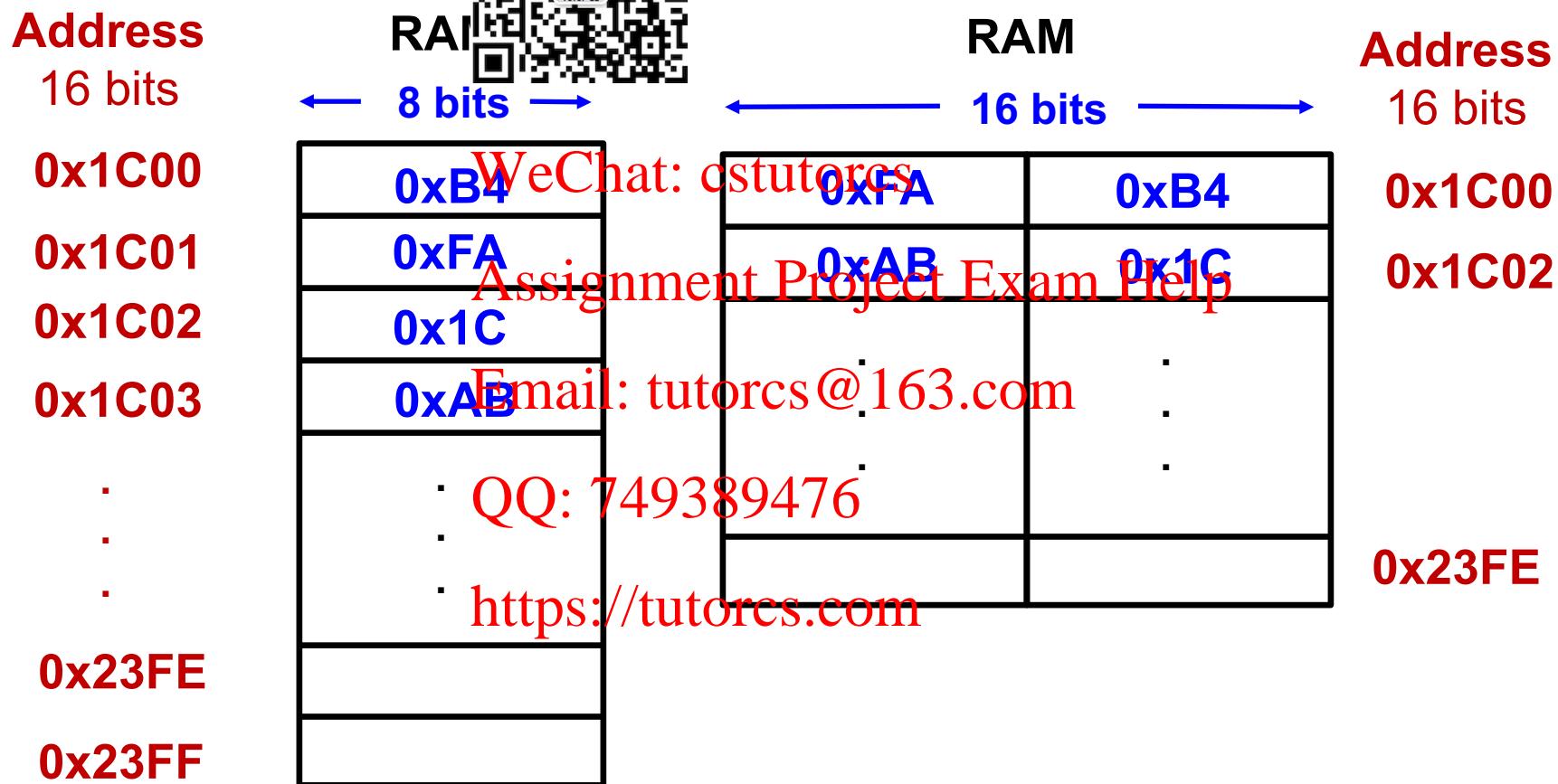


Memory Mapping – RAM

程序代写代做 CS 编程辅导

The **RAM** is the data memory – stores run-time variables and the **stack**

Size: 2048 B = 2 KiB
RAM is addressed – memory mapped

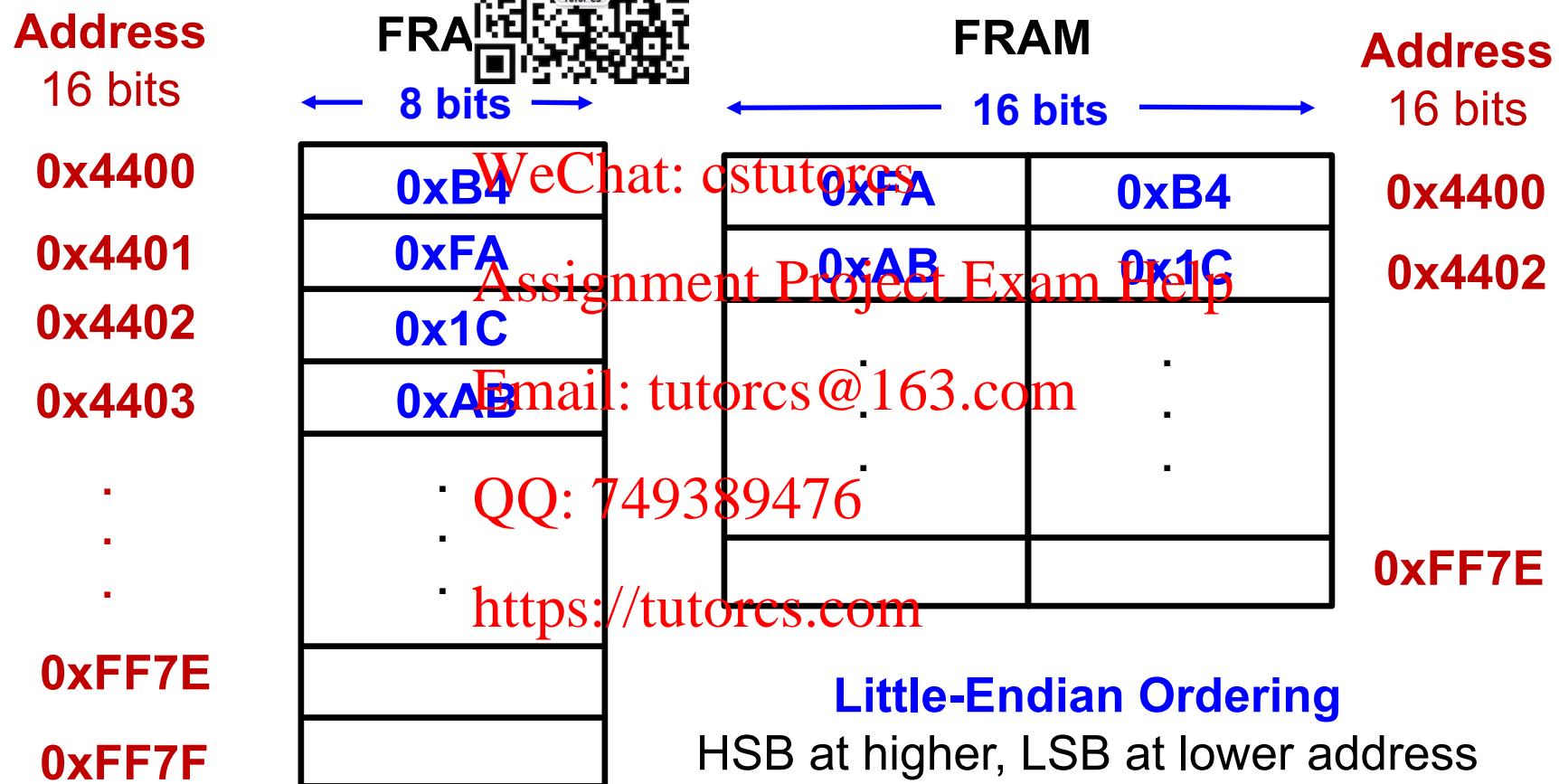




Memory Mapping – FRAM

程序代写代做 CS 编程辅导

The **FRAM** (Ferroelectric RAM) is the program memory of MSP430FR6989
Size: 48,000 B = 48 kB





Memory Map

~~程序代写代做 CS 编程辅导~~

The linker file `Ink_msp430fr6989.cmd` contains the memory map

```
MEMORY
{
    TINYRAM
    PERIPHERALS_8BIT
    PERIPHERALS_16BIT
    RAM
    INFOA
    INFOB
    INFOC
    INFOD
    FRAM
    FRAM2
    JTAGSIGNATURE
    BSLSIGNATURE
    IPESIGNATURE
    INT00
    INT01
    INT02
    INT03
    INT04
    INT05
    INT06
    INT07
    INT08
    INT09
}
```



```
= 0x0006, length = 0x001A
= 0x0020, length = 0x00E0
= 0x0100, length = 0x0100
: origin = 0x1C00, length = 0x0800
: origin = 0x1980, length = 0x0080
: origin = 0x1900, length = 0x0080
: origin = 0x1880, length = 0x0080
: origin = 0x1800, length = 0x0080
: origin = 0x4400, length = 0xBB80
: origin = 0x10000, length = 0x13FF8 /* Boundaries changed
: origin = 0xFF80, length = 0x0004, fill = 0xFFFF
: origin = 0xFF84, length = 0x0004, fill = 0xFFFF
: origin = 0xFF88, length = 0x0008, fill = 0xFFFF
: origin = 0xFF90, length = 0x0002
: origin = 0xFF92, length = 0x0002
: origin = 0xFF94, length = 0x0002
: origin = 0xFF96, length = 0x0002
: origin = 0xFF98, length = 0x0002
: origin = 0xFF9A, length = 0x0002
: origin = 0xFF9C, length = 0x0002
: origin = 0xFF9E, length = 0x0002
: origin = 0xFFA0, length = 0x0002
: origin = 0xFFA2, length = 0x0002
```

WeChat: cstutorcs
Assignment Project Exam Help
Email: tutors@163.com

QQ: 749389476

<https://tutorcs.com>



The 16 Core Registers

~~程序代写代做 CS 编程辅导~~

The 16 **core registers** R0 – R15 are 16-bit registers that

- sit in the CPU
- are memory mapped – no memory address
- can be accessed directly by their name R4 – R15



The first four core registers have dedicated functions

WeChat: cstutorcs

Program Counter

PC/R0

Stack Pointer

SP/R1

Status Register

Assignment Project Exam Help

SREG/CCR1/RE

Constant Generator

Email: tutorcs@163.com

CCR/B3

General-Purpose Register

R4

QQ: 749389476

...

General-Purpose Register

R15



Announcements

~~程序代写代做 CS 编程辅导~~

Will post Quiz 2 by the end of the week tomorrow

- You will have one week to answer all questions and submit
- MCU architecture: CPI, Pipelining, Cache/Data Memory, Address and Data Bus
- von Neumann and Harvard Architectures
- Byte and word addressing
- Little-Endian and Big-Endian ordering
- Memory map of MSP430FR6989 – RAM and FRAM

WeChat: cstutorcs

Assignment Project Exam Help

Email: tutorcs@163.com

QQ: 749389476

<https://tutorcs.com>

