School of Electrical Engineering and Telecommunications

Term 1, 2023

Assignment 1 Marking Guidelines

ELEC 2141
Digital Circuit Design

Assignment I has one design problem with the following the marking breakdown.

1. Design approach: (20 marks)
   - Clearly explain the design approach (are you using functional blocks? hierarchical design? Five or four variable k-maps?) (8)
   - Any assumptions made must be explicitly stated (2)
   - You may concisely re-write the specification including your design assumptions if needed (10)
2. Formulation: (20 marks)
   - Draw any truth table required and clearly indicate input and output columns (10)
     - If appropriate "Do not care conditions" are not used, two marks will be deducted
     - Wrong Truth table – deduct 5 marks
   - Show any hierarchical block diagram if used.
   - If Boolean function is generated directly from the specification, explain how you arrive at the Boolean function and clearly indicate the function. (10)
     - Boolean function – 5 marks
     - Correct explanation – 5 marks
3. Optimization: (20 marks)
   - Show all K-maps used and indicate clearly which essential prime implicates or prime implicates are selected in your optimized Boolean expression (16)
     - If the Boolean expression is not correct or not optimized correctly, 1mark will be deducted per expression
   - If multi-level circuit implementation is employed, show the optimization steps
   - Indicate GIC of your optimized design (4)
4. Circuit implementation (20 marks)
   - Draw logic diagram. It should be neat and clearly labelled (inputs and outputs) (14)
   - Clearly indicate your choice of implementation (NAND only, NOR only etc) (6)
5. Verification (20 marks)
   - Draw the schematics of your implementation in Xilinx ISE
   - Provide the Verilog test file – (10)
   - Include the simulation result from Xilinx (attach the file or screenshots in pdf format). It has to clearly show the waveforms for all inputs and output. – (10)