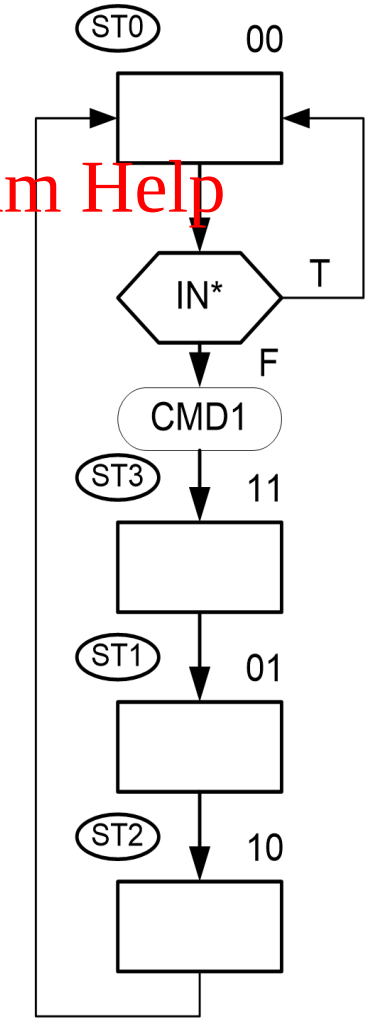
Digital Systems Design

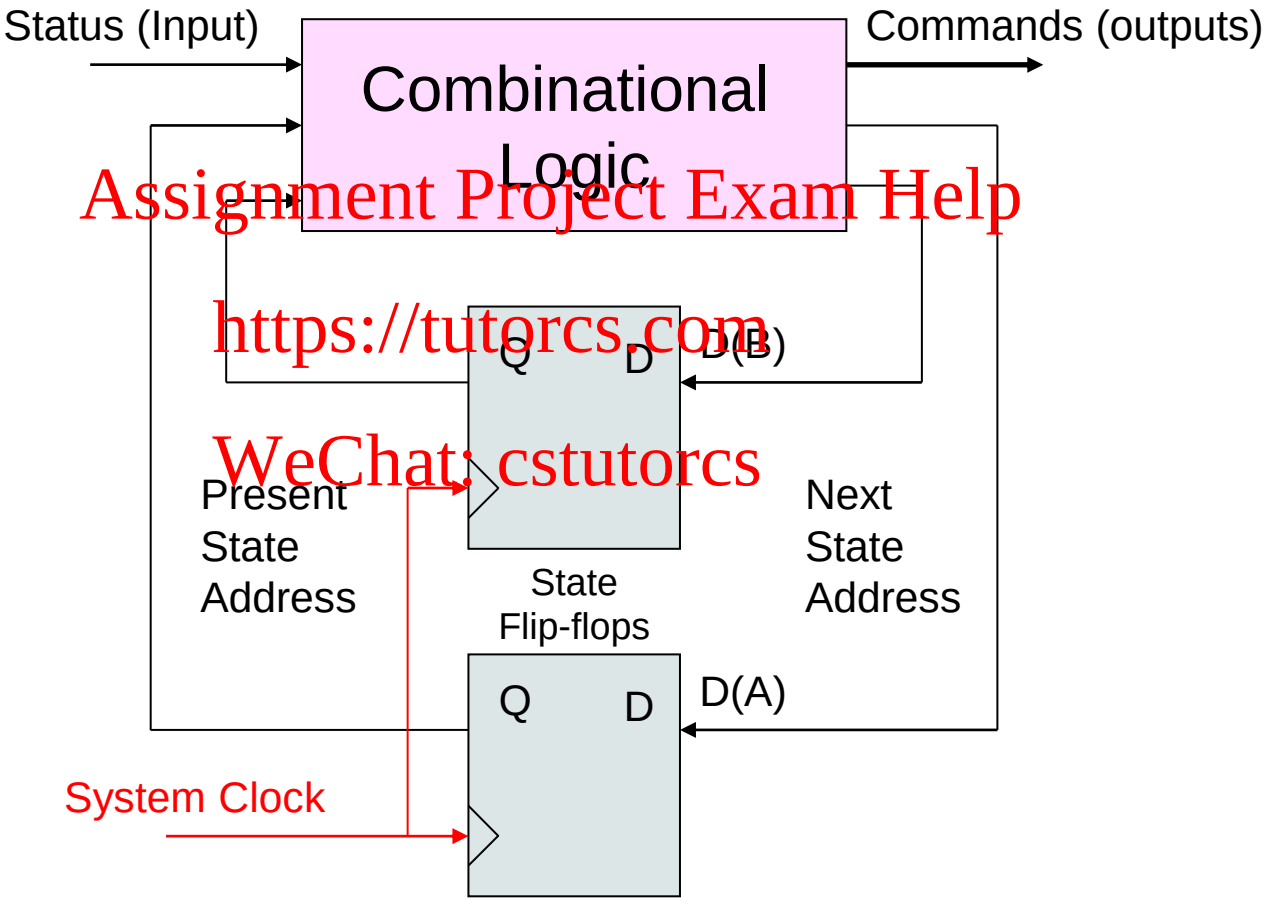
Asynchronous inputs and Synchronisers

Asynchronous Inputs and Races

- The timing changes of inputs occurring from sources outside our digital circuit are beyond our control.
- Such inputs are asynchronous and they are indicated by adding an asterisk * to their variable name.
- Consider the following:



Process Model



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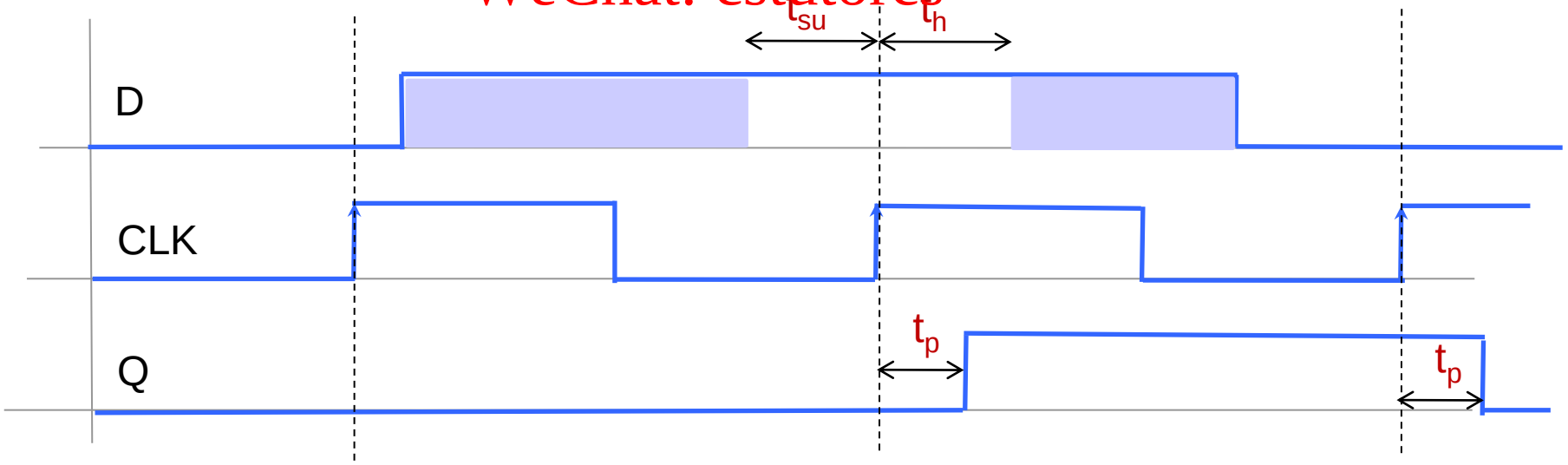
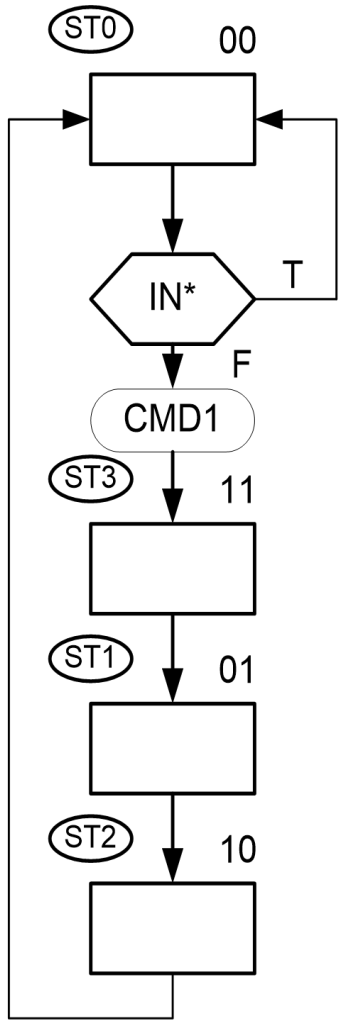
Setup and Hold Times for D Flip-flops

- For the proper function of the edge triggered FF
  - D input must be stable for t_{su} time (setup time) before the active edge of the clock.
  - D input must be stable for t_h time (hold time) after the active edge of the clock.



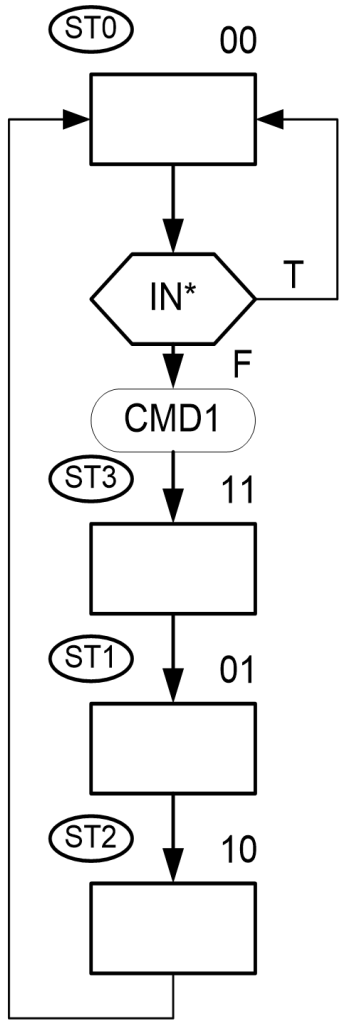
Asynchronous Inputs and Races cont.

- Each bistable requires that its' input be stable for a few nanoseconds prior to the clock edge.
- If the input changes during the *set-up time* the value of the bistable's output after the clock edge will be unpredictable.
- i.e. after settling, the output will be either a T or F value, but which is uncertain.
- If we assume that we are in ST0 and IN* = T, then the inputs to both state bistables is F and the system is preparing to move to ST0. If IN* = F then the inputs to the bistables will be 11 in preparation to move to ST3. However if we have a transition in IN* during the bistable set-up time or hold time we cannot predict their output.
- The next state could become ST0, ST1, ST2 or ST3.
- The situation where the next state depends on the exact timing of the bistable input changes, is called a *transition race*.

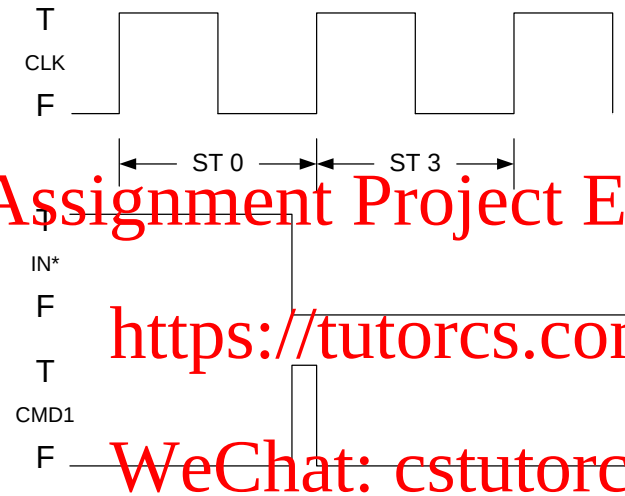


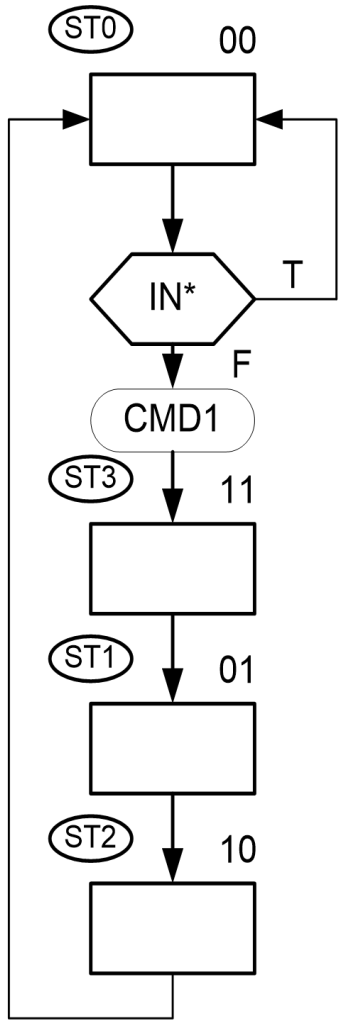
Output Races

- Examining the conditional output CMD1 when IN* changes (ignoring transition races).
- In state ST0, when IN* is T, CMD1 is F, whilst when IN* is F, CMD1 is T.
- A change in IN* causes an immediate change to CMD1.
- If IN* changes from T to F in state ST0 time, the output CMD1 will be T for only a short period of the clock time, before the system moves to state ST3.
- This problem can be serious as the output CMD1 may cause problems if it is too short.



Output Races cont.



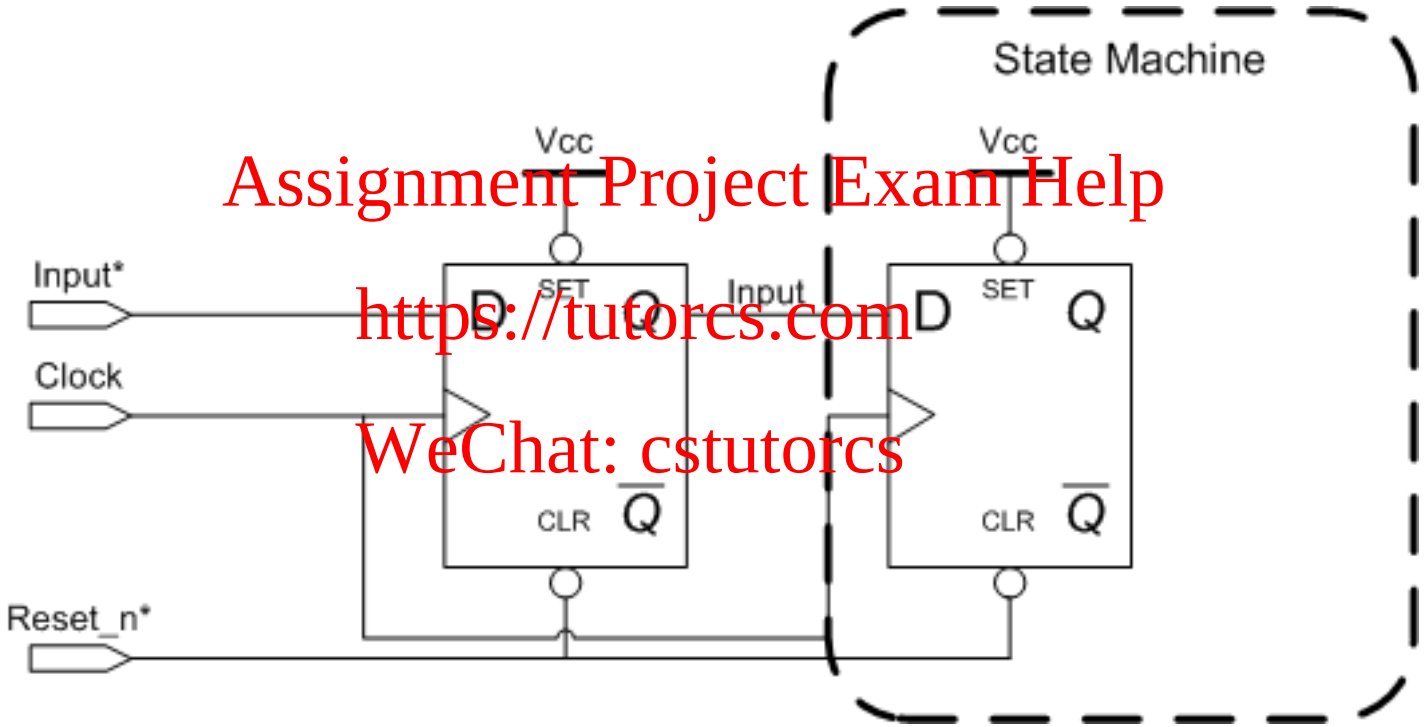


- This problem is called an *output race* and is the direct result of an ASM output being conditional on an asynchronous input.
- You would only get this problem in Mealy machines as in Moore machines the output is only a function of the current state.

Avoiding Races

- There is no way to avoid output races, except to avoid conditional outputs that depend on asynchronous inputs.
- We eliminate problems caused by asynchronous inputs by synchronising the inputs using a ‘D’ type flip-flop clocked by the system clock.
- The ASM uses the output of the flip-flop and, as the output changes synchronously with the clock, there will never be a race in the ASM caused by that input.
- Many useful synchronous IC’s have asynchronous inputs for setting, clearing or loading.
- The only routine use of asynchronous inputs is a master clear signal to be used when power is first applied or when the system ‘hangs up’.

Synchroniser Flip-Flop



Note that the state machine will now detect the asynchronous "Input*" up to one clock cycle later as it is "delayed" by the Synchronising D-Type flip-flop.

Do the Asynchronous inputs cause problems in these ASMs?