Digital System Design ELEC373/473

Quartus DE2 Tips

Expected design style for assignments

- Design from the top down
  - I know that many of you are keen to start coding in the HDL as quickly as possible but that does not lead to good designs.
- Start with a block diagram that shows inputs and outputs, then add some functional blocks to the architecture, i.e. does the design need counters? What controllers are you going to implement?
  - You should end up with a block diagram showing inputs and outputs between the architectures and the controllers.

ASM design

- For each block, whether it be a controller or architecture you should draw an ASM chart to show the algorithm of the block.
  - Note that even combinational logic can be described by a single state ASM chart.
  - You should then use the ASM chart to write your Verilog code.
  - You should then simulate your Verilog code using the ASM chart to check that you simulate every pathway in your ASM chart.

Design stages

1. Block Diagram showing inputs/outputs for all modules in the design.
2. ASM charts for all modules in the design.
3. Verilog code for all modules
4. Simulation showing that every path in each ASM works correctly.

- Note that the design is undertaken during steps 1 & 2, that is where the intellectual property is added. Moving from stages 2 to 3 and 3 to 4 is mechanistic.

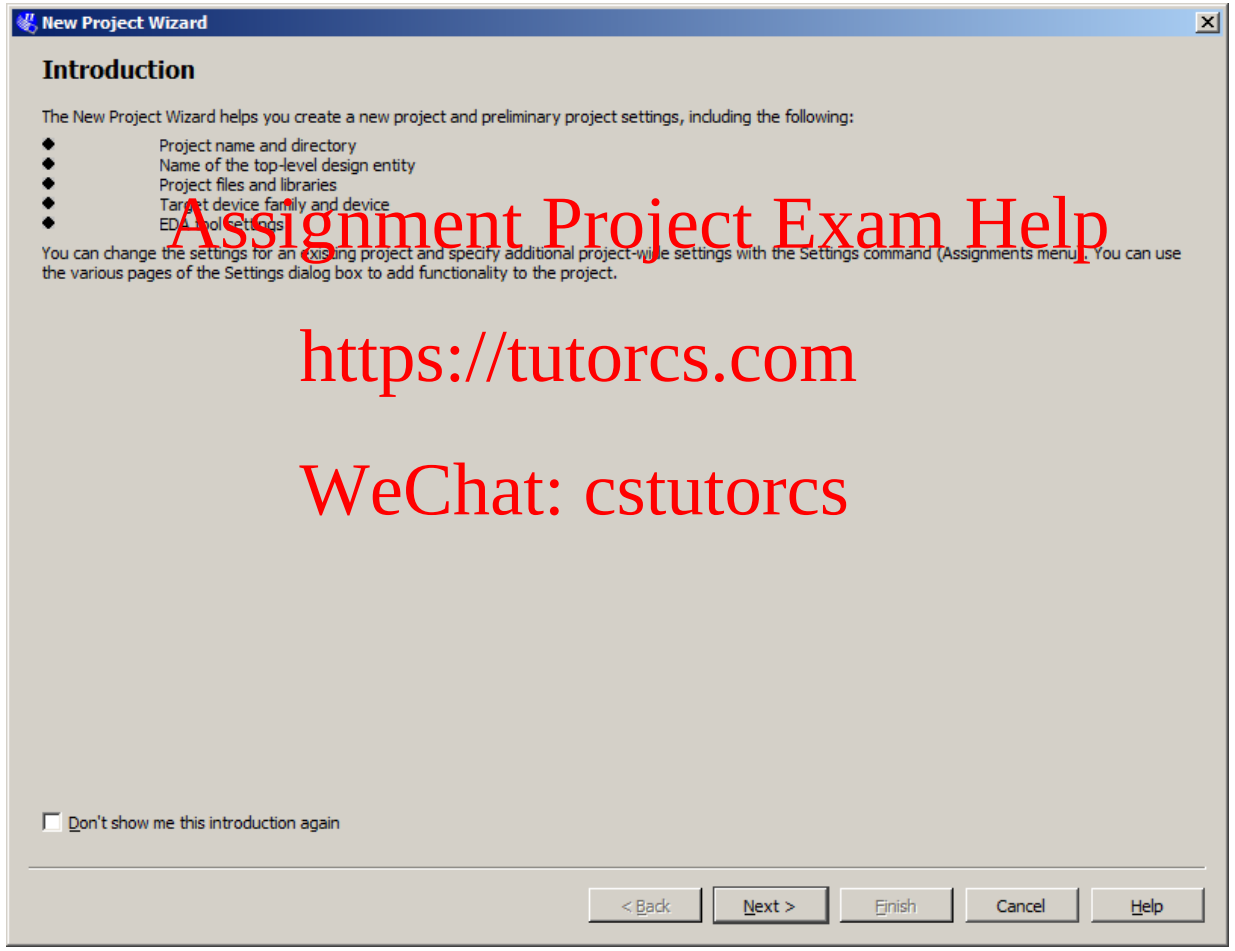
Early coding.

- You can start coding the Verilog for a module as soon as its ASM is complete.
  - You don’t need to have all the ASMs complete before you start coding.
  - Some people start by coding and testing blocks they are 100% sure they need. For example in assignment 1 you will need a 4 to 7 segment decoder.

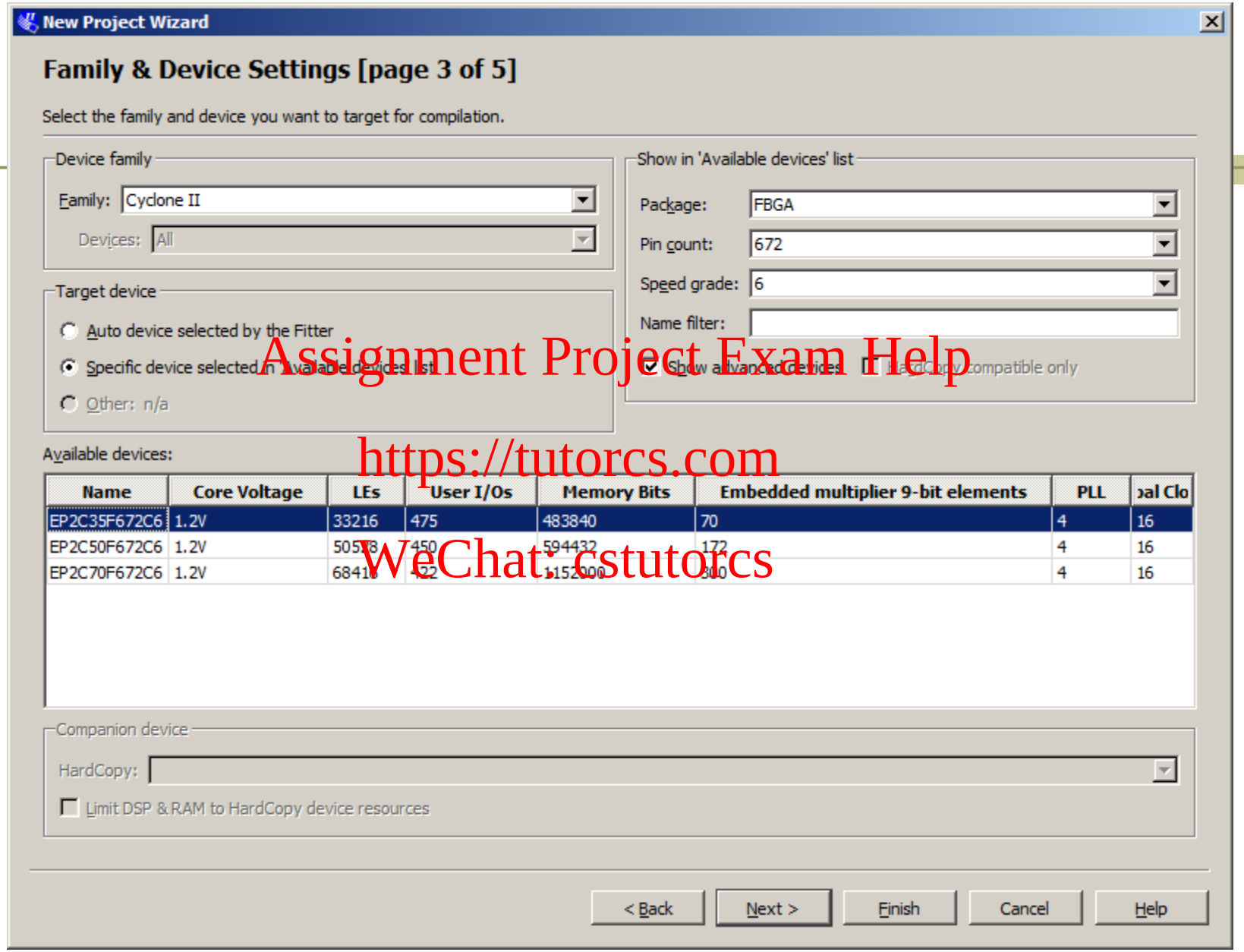
Simple Verilog program for the DE2 Board

- Simple combinational logic design
  - LEDG0 = KEY0 AND KEY1
  - LEDG1 = KEY0 OR KEY1
- Pin assignments on the DE2 Board
  - KEY[0] = PIN_G26
  - KEY[1] = PIN_N23
  - LEDG[0] = PIN_AE22
  - LEDG[1] = PIN_AF22
- Note that this is a combinational design so no clock is needed
  - CLOCK_50 = PIN_N2 is a 50MHz clock

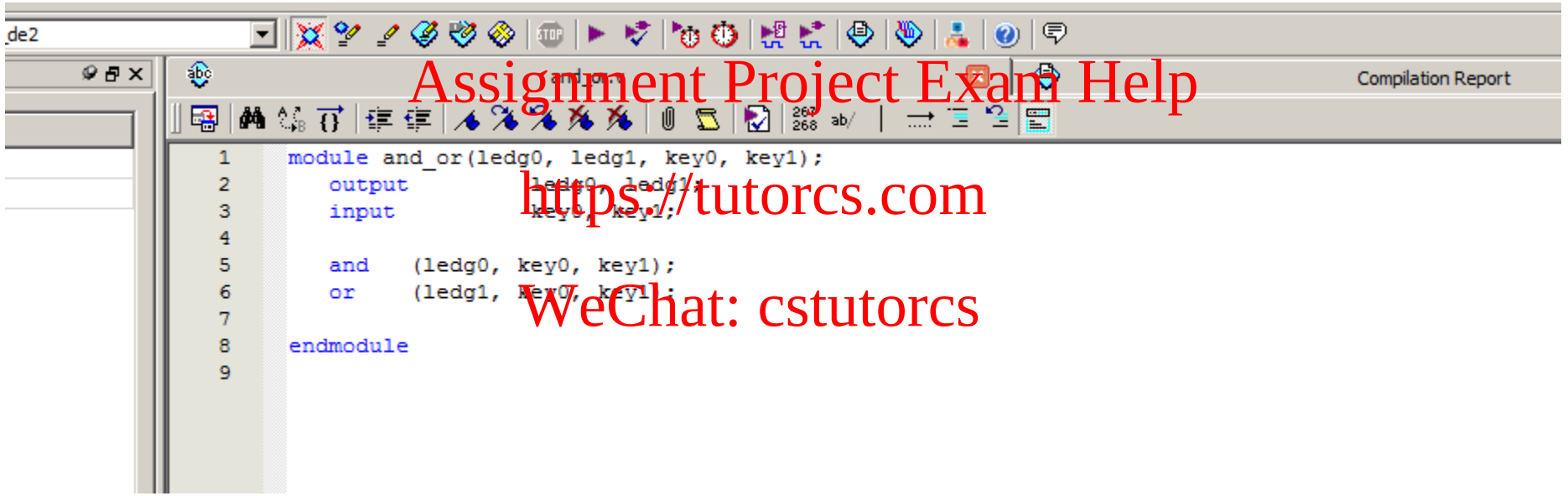
Quartus - Creating a new project



- Use the new project Wizard

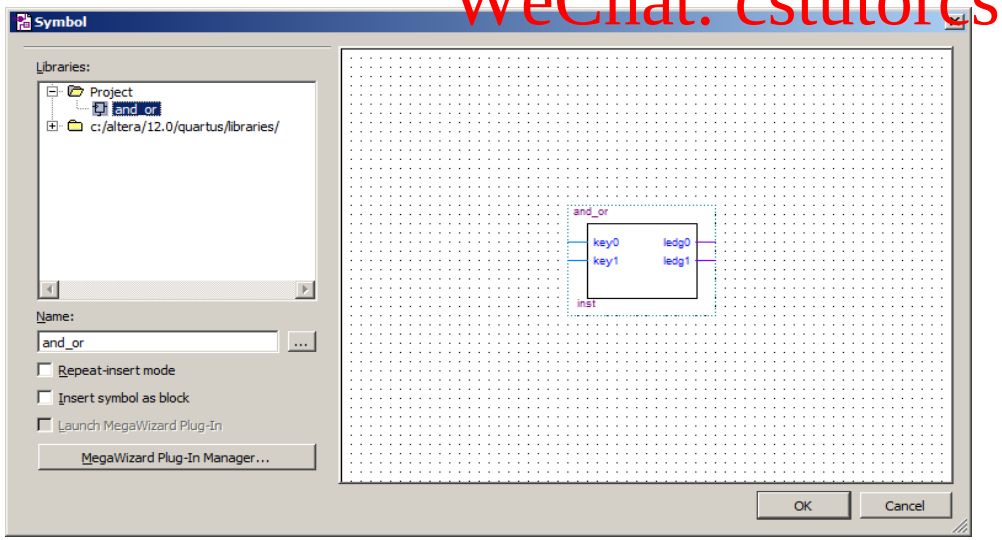


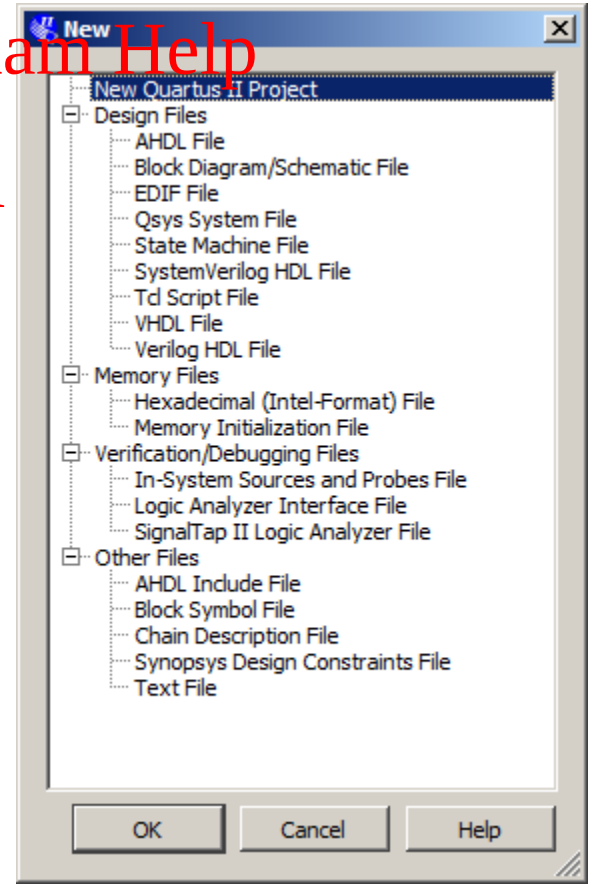
Module and_or



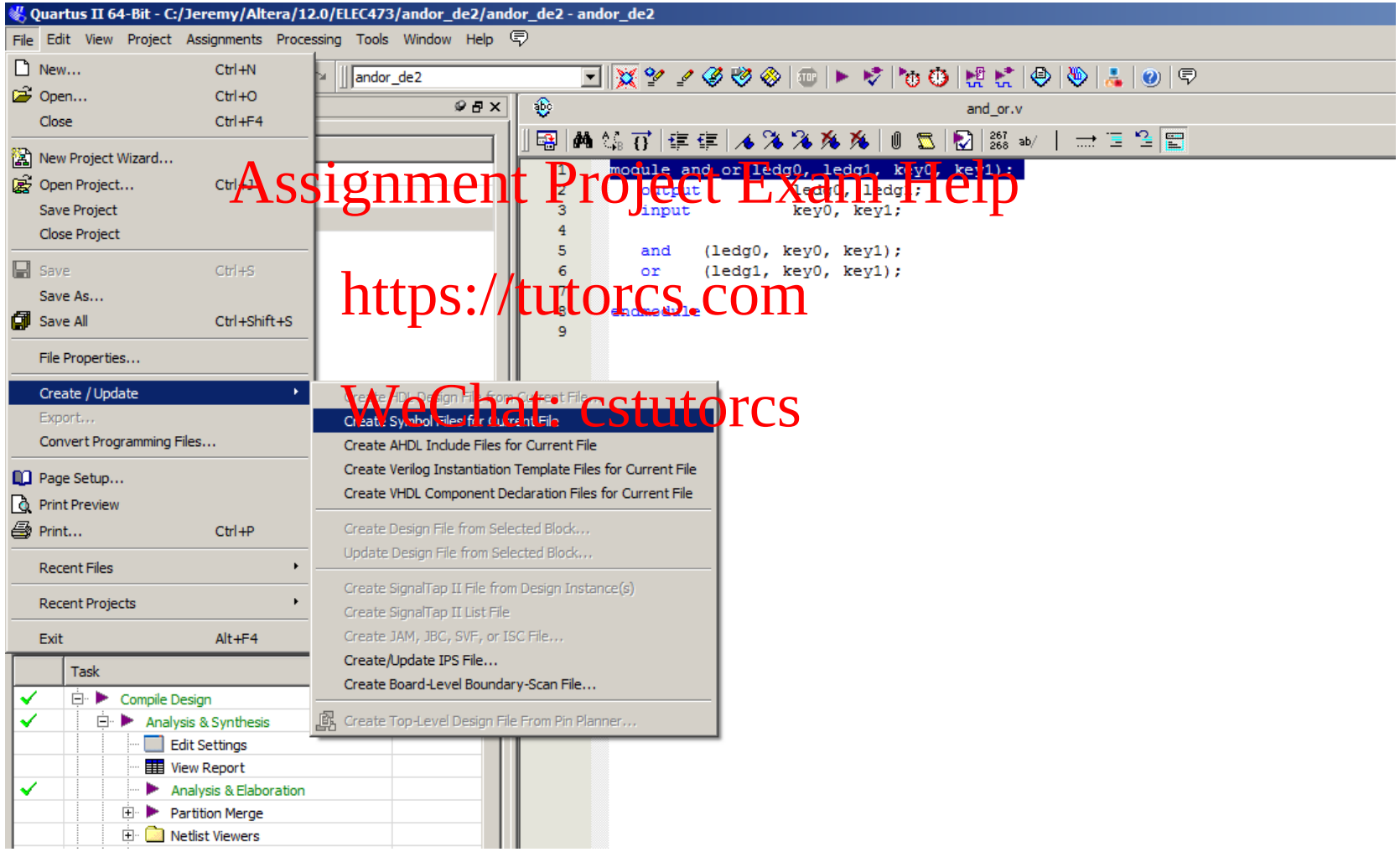
Using a top level bdf to connect modules

- Some people prefer to connect their modules using a top level bdf file
- The top level name should be the same as the project name



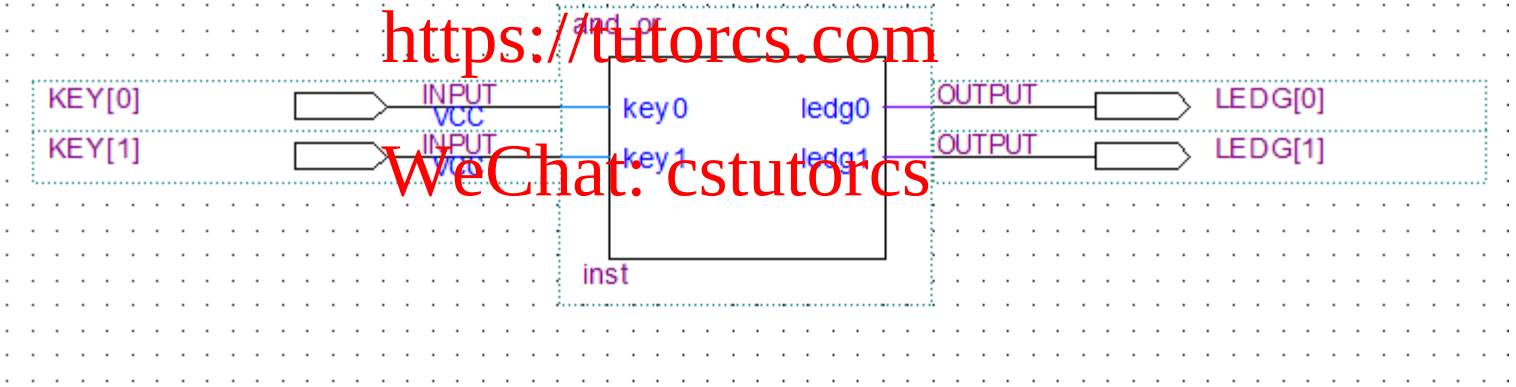


How to create a symbol file for a module?



Assigning pins

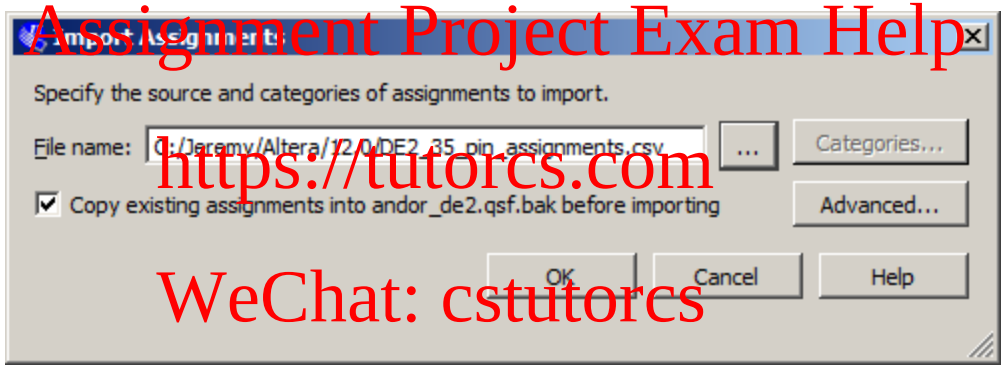
- Easiest to use the same names as defined in the Altera supplied CSV file



- Processing -> Start -> Start Analysis and Elaboration

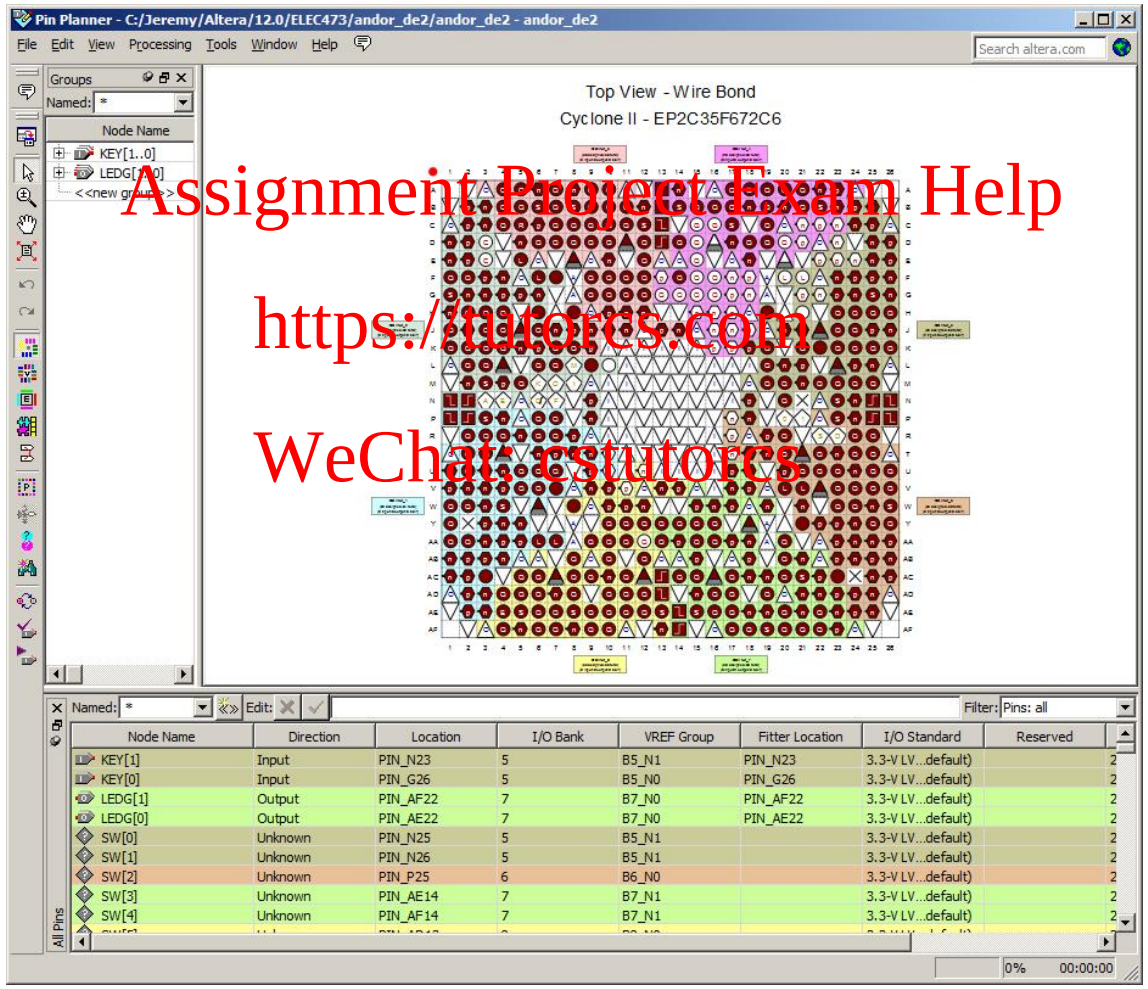
Assigning pins…

- Assignments -> import assignments

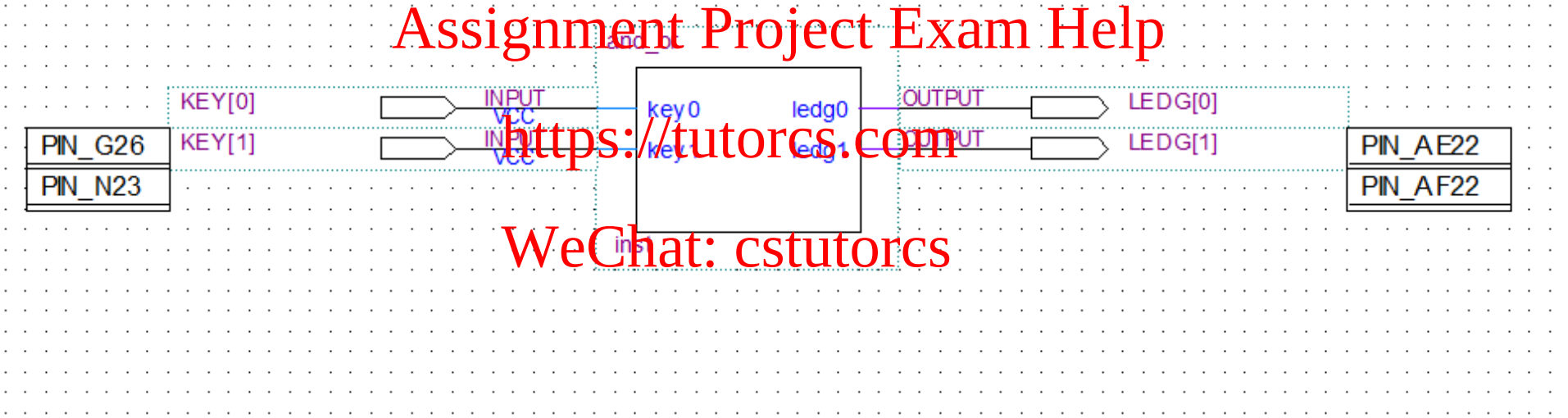


- Using the pre-defined names can save lots of typing later on

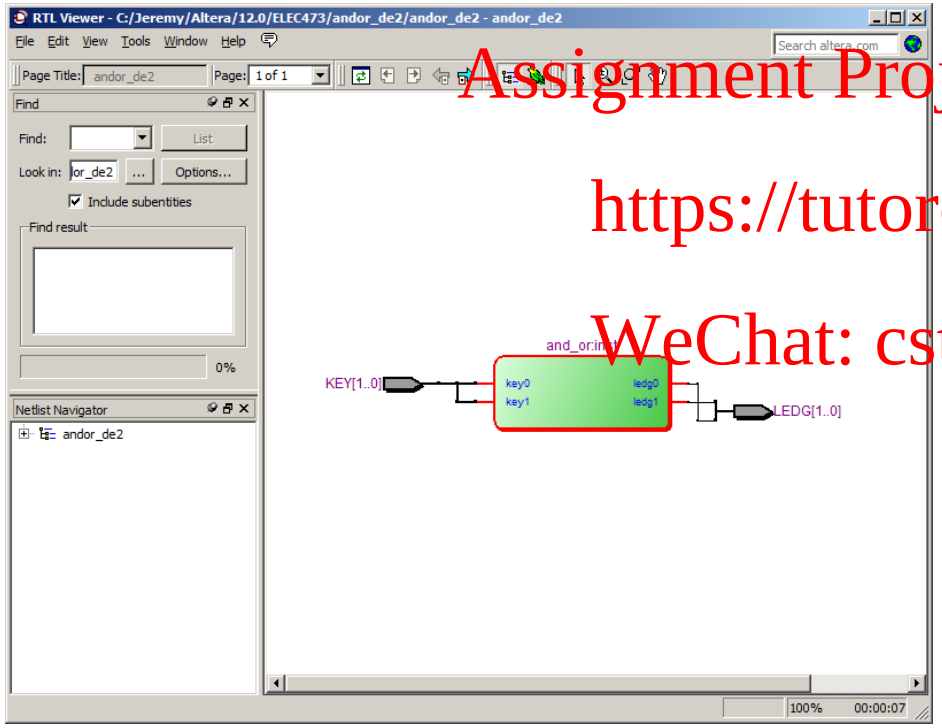
Checking pin assignments - Pin Planner

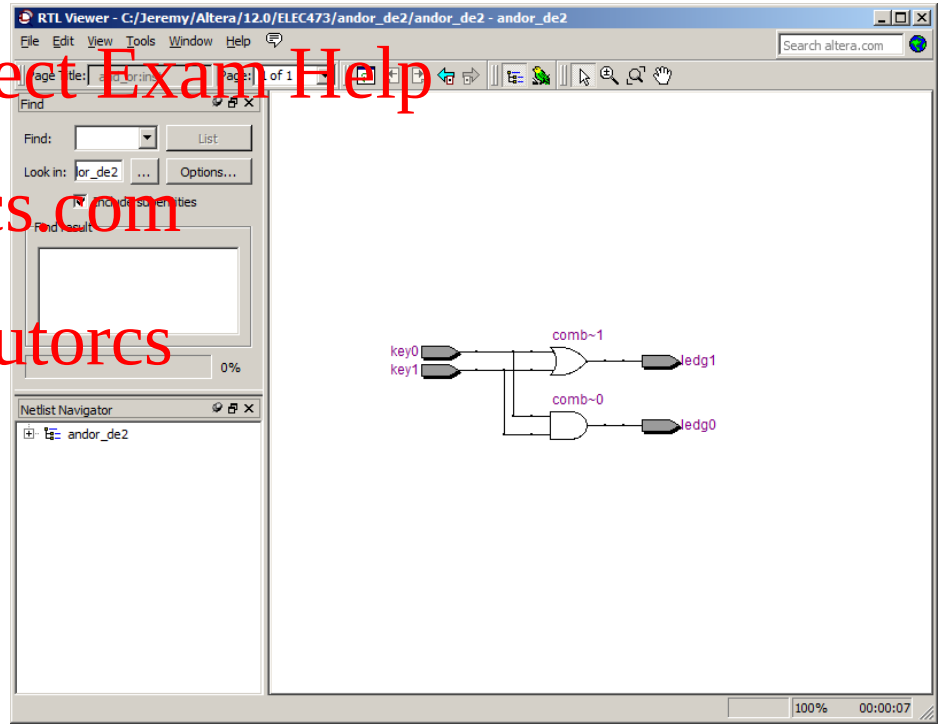


Pin assignments- shown on bdf

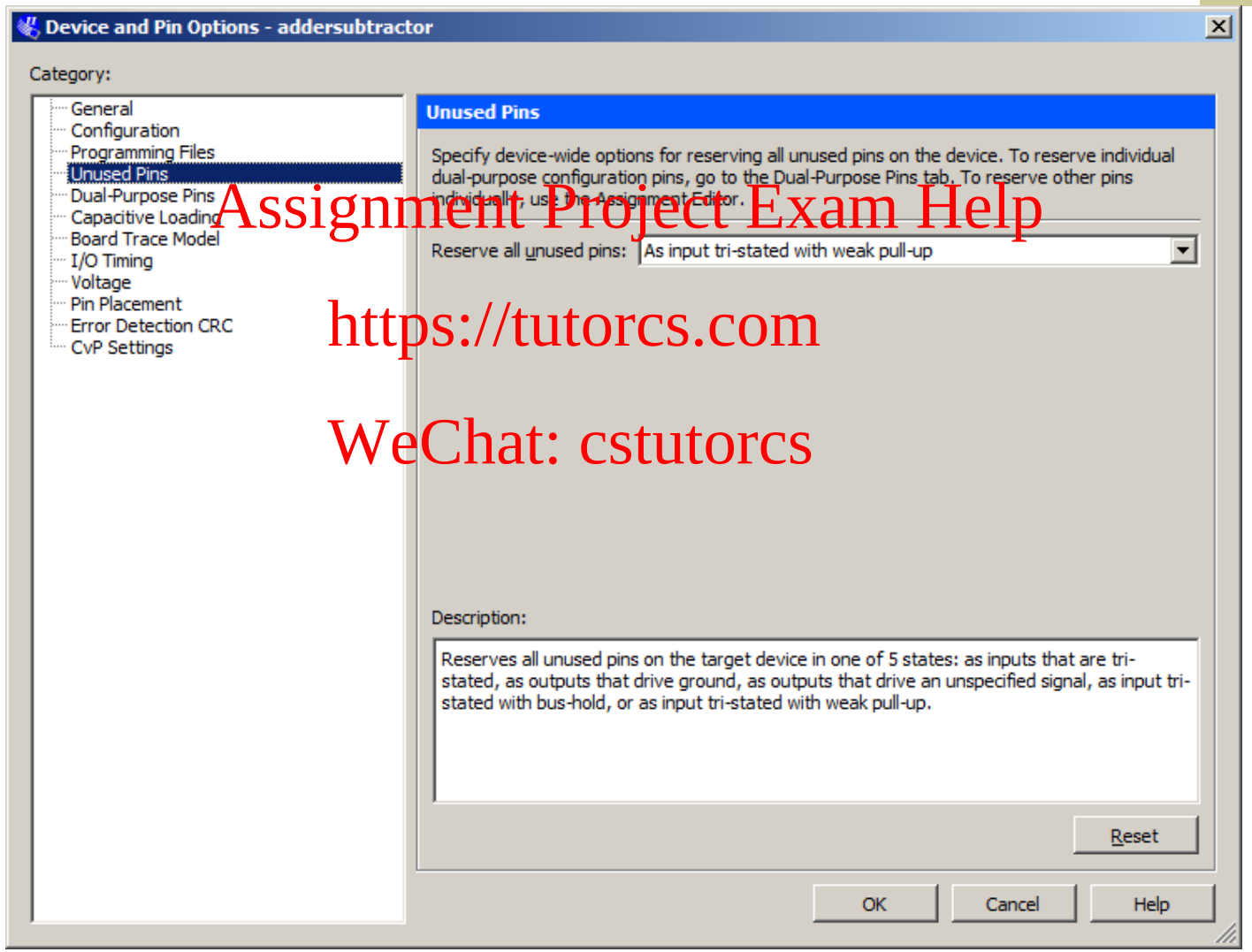


RTL Viewer

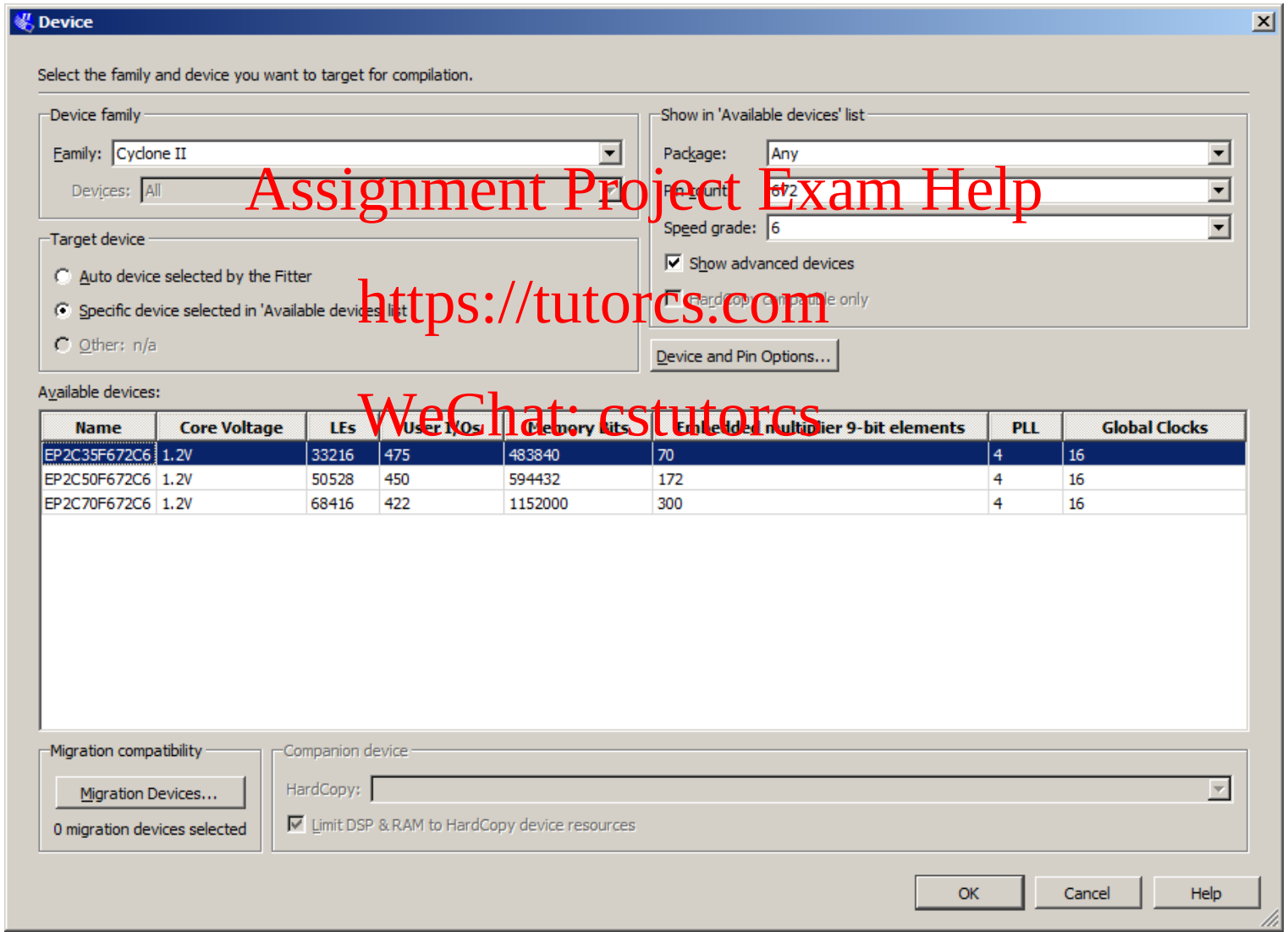




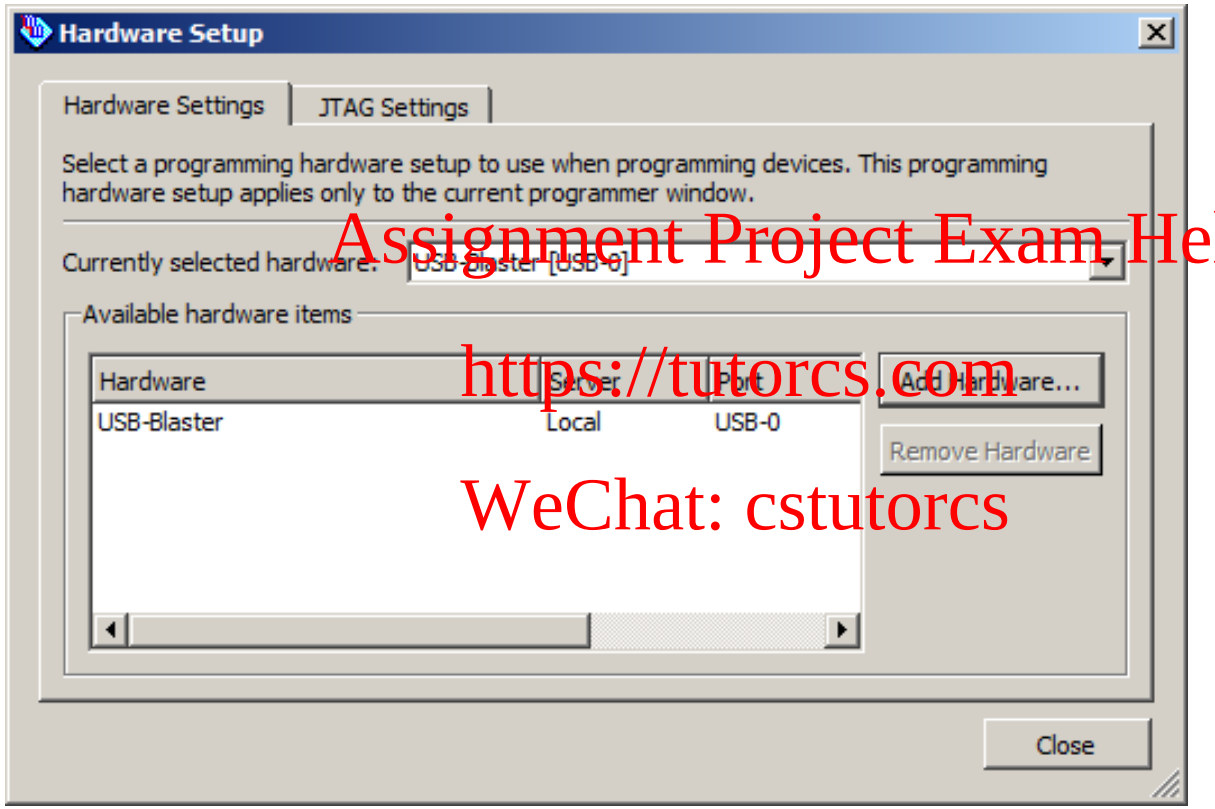
What to do with un-used pins?



From Assignments - Device

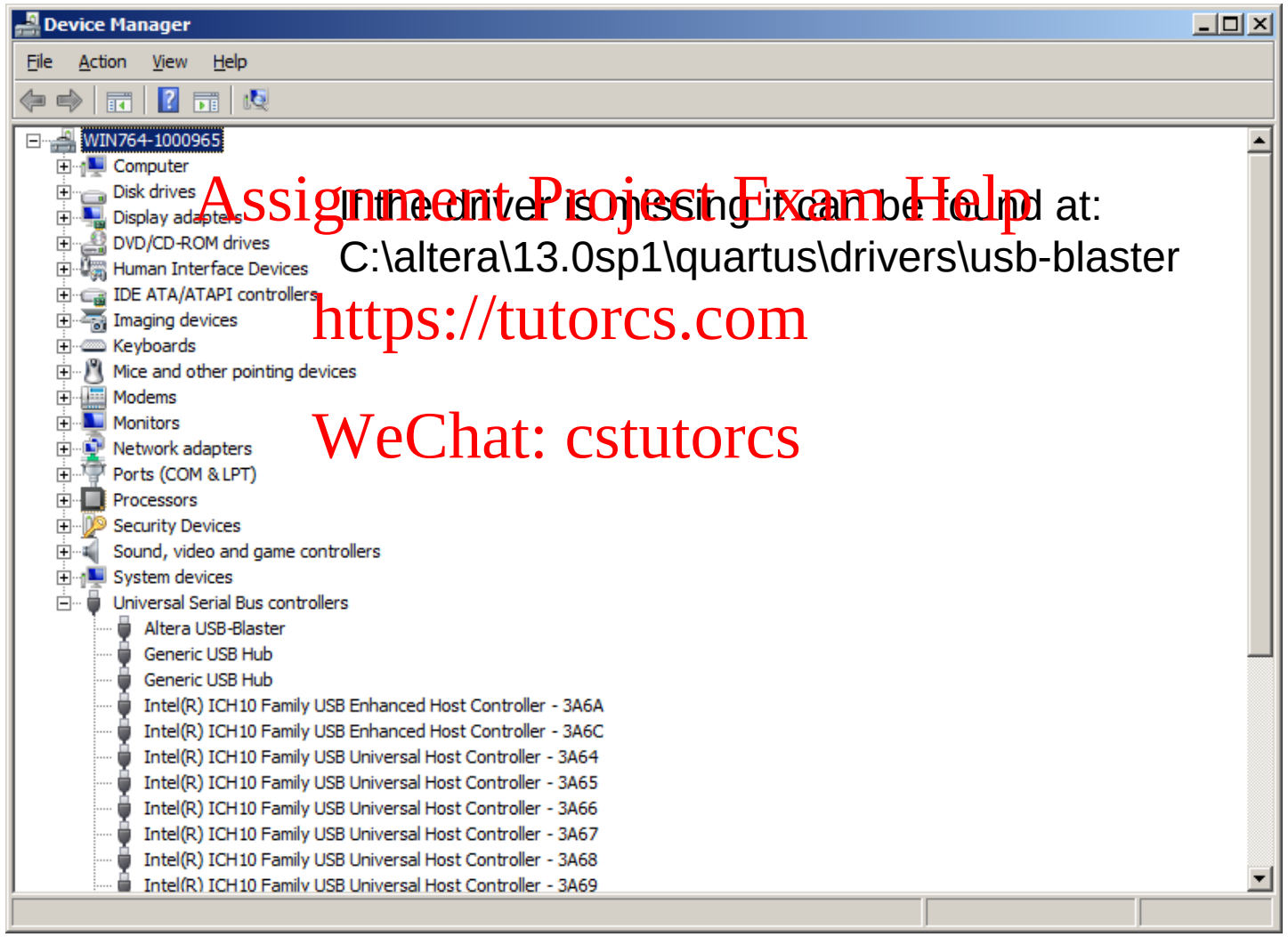


Programmer Hardware setup



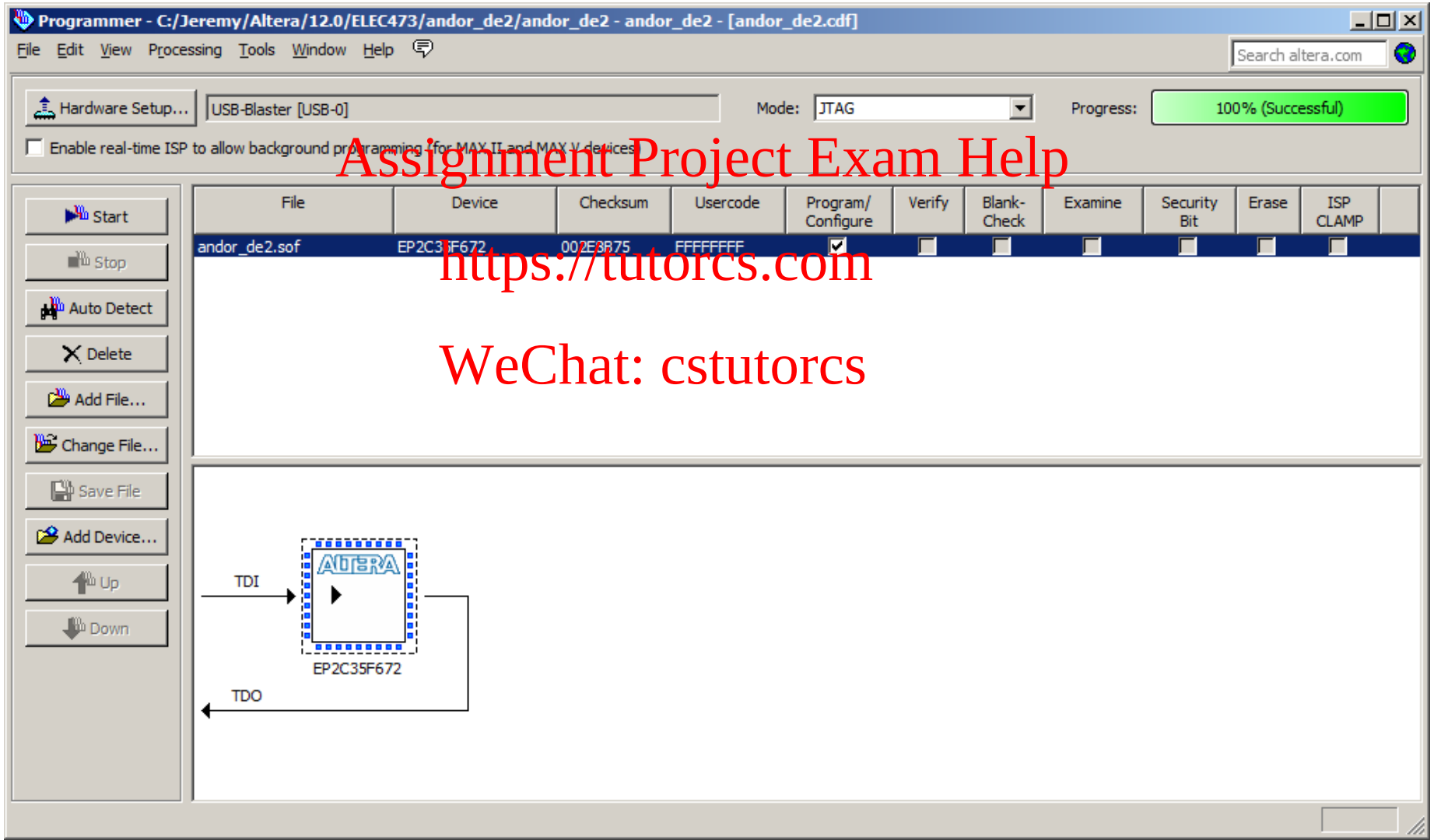
If no hardware is found check the hardware settings of the programmer.

Altera USB-Blaster Device Driver



If the driver is missing it can be found at:
C:\altera\13.0sp1\quartus\drivers\usb-blaster

Programming



Does it work as expected?

- LEDs

There are 27 user-controllable LEDs on the DE2 board. Eighteen red LEDs are situated above the 18 toggle switches, and eight green LEDs are found above the pushbutton switches (the 9th green LED is in the middle of the 7-segment displays). Each LED is driven directly by a pin on the Cyclone II FPGA; driving its associated pin to a high logic level turns the LED on, and driving the pin low turns it off. A schematic diagram that shows the pushbutton and toggle switches is given in Figure 4.4. A schematic diagram that shows the LED circuitry appears in Figure 4.5.

Does it work as expected?

- Switches

The DE2 board provides four pushbutton switches. Each of these switches is debounced using a Schmitt Trigger circuit, as indicated in Figure 4.3. The four outputs called *KEY0*, …, *KEY3* of the Schmitt Trigger device are connected directly to the Cyclone II FPGA. Each switch provides a high logic level (3.3 volts) when it is not pressed, and provides a low logic level (0 volts) when depressed. Since the pushbutton switches are debounced, they are appropriate for use as clock or reset inputs in a circuit.

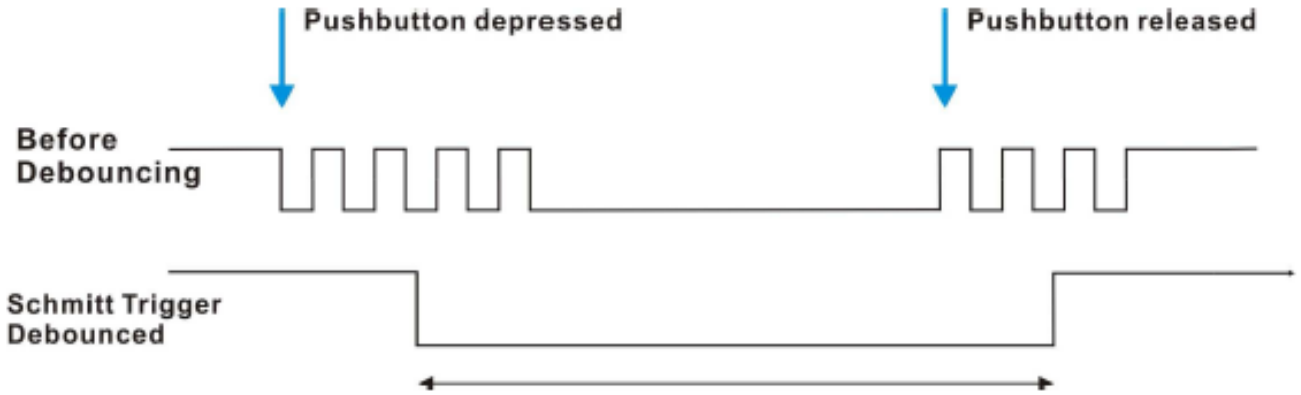


Figure 4.3. Switch debouncing.

Port Inversion