Digital System Design ELEC373/473

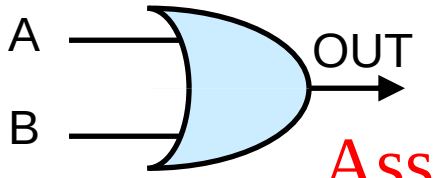
Verilog Four-Value Logic

(HDLs)

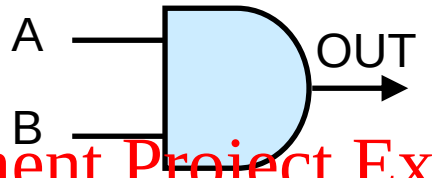
Four-Value Logic

- In Verilog a single bit can have one of four values
  - **0** Numeric 0, logical FALSE
  - **1** Numeric 1, logical TRUE
  - **x** Unknown or ambiguous value
  - **z** No value (high impedance)
- Why **x**?
  - Could be multiple drivers conflicting on a wire. Strong signals cause short circuit and weak signals cause unexpected results.
  - Could be lack of initialization
  - In reality there is no '**x**' value for a signal, just **0**,**1**, and **z**.
- Why **z**?
  - Nothing driving the signal (Tri-states)

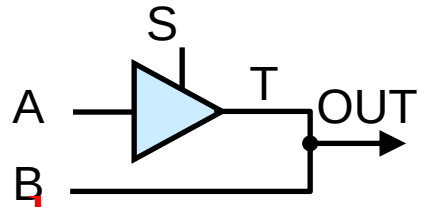
Resolving 4-Value Logic



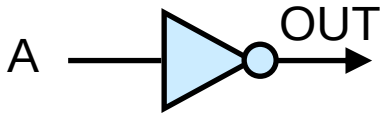
A	B	OUT
0	0	
0	1	
1	1	
0	x	
0	z	
1	x	
1	z	



A	B	OUT
0	0	
0	1	
1	1	
0	x	
0	z	
1	x	
1	z	

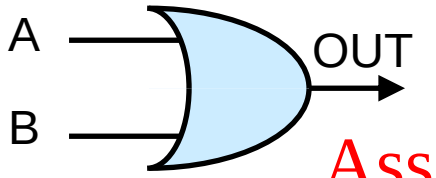


S	A	T	B	OUT
0	0		z	
0	1		x	
0	x		1	
0	z		0	
1	0		1	
1	0		z	
1	1		z	
1	x		z	
1	z		0	

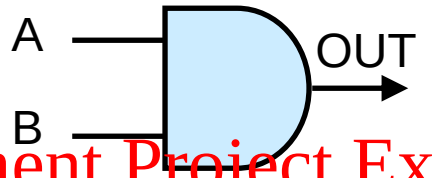


A	0	1	x	z
OUT				

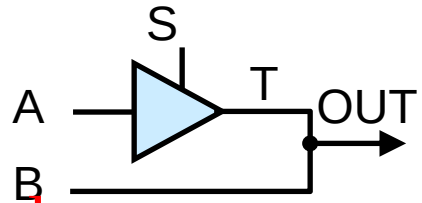
Resolving 4-Value Logic



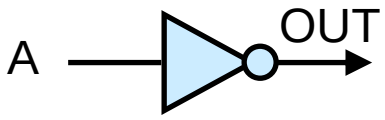
A	B	OUT
0	0	
0	1	
1	1	
0	x	
0	z	
1	x	
1	z	



A	B	OUT
0	0	
0	1	
1	1	
0	x	
0	z	
1	x	
1	z	

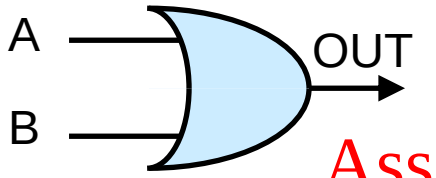


S	A	T	B	OUT
0	0			
0	1			
0	x			
0	z			
1	0			
1	0			
1	1			
1	x			
1	z			

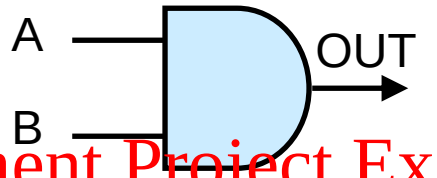


A	0	1	x	z
OUT	1	0	x	x

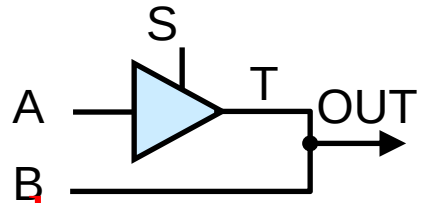
Resolving 4-Value Logic



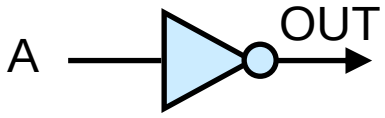
A	B	OUT
0	0	0
0	1	1
1	1	1
0	x	x
0	z	x
1	x	1
1	z	1



A	B	OUT
0	0	
0	1	
1	1	
0	x	
0	z	
1	x	
1	z	

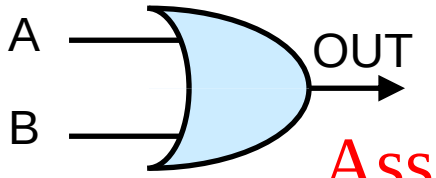


S	A	T	B	OUT
0	0			
0	1			
0	x			
0	z			
1	0			
1	0			
1	1			
1	x			
1	z			

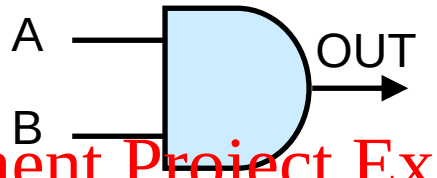


A	0	1	x	z
OUT	1	0	x	x

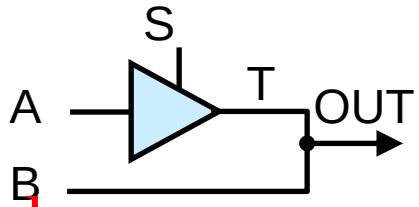
Resolving 4-Value Logic



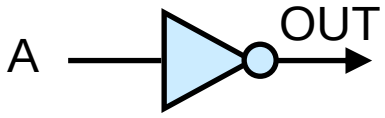
A	B	OUT
0	0	0
0	1	1
1	1	1
0	x	x
0	z	x
1	x	1
1	z	1



A	B	OUT
0	0	0
0	1	0
1	1	1
0	x	0
0	z	0
1	x	x
1	z	x

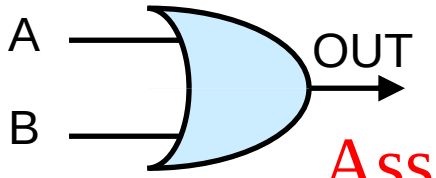


S	A	T	B	OUT
0	0		z	
0	1		x	
0	x		1	
0	z		0	
1	0		1	
1	0		z	
1	1		z	
1	x		z	
1	z		0	

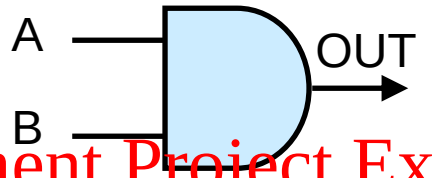


A	0	1	x	z
OUT	1	0	x	x

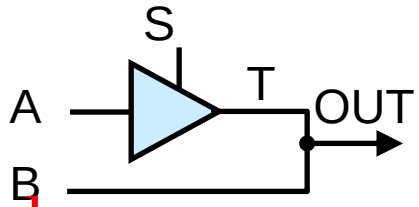
Resolving 4-Value Logic



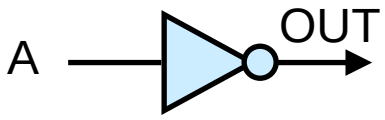
A	B	OUT
0	0	0
0	1	1
1	1	1
0	x	x
0	z	x
1	x	1
1	z	1



A	B	OUT
0	0	0
0	1	0
1	1	1
0	x	0
0	z	0
1	x	x
1	z	x

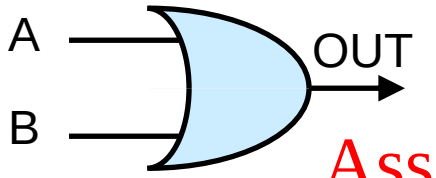


S	A	T	B	OUT
0	0	z	z	
0	1	z	x	
0	x	z	1	
0	z	z	0	
1	0	0	1	
1	0	0	z	
1	1	1	z	
1	x	x	z	
1	z	x	0	

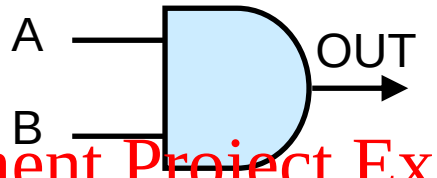


A	0	1	x	z
OUT	1	0	x	x

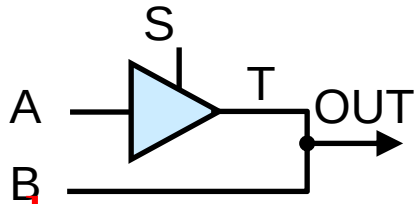
Resolving 4-Value Logic



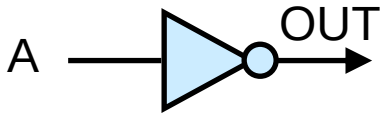
A	B	OUT
0	0	0
0	1	1
1	1	1
0	x	x
0	z	x
1	x	1
1	z	1



A	B	OUT
0	0	0
0	1	0
1	1	1
0	x	0
0	z	0
1	x	x
1	z	x



S	A	T	B	OUT
0	0	z	z	z
0	1	z	x	x
0	x	z	1	1
0	z	z	0	0
1	0	0	1	x
1	0	0	z	0
1	1	1	z	1
1	x	x	z	x
1	z	x	0	x



A	0	1	x	z
OUT	1	0	x	x

Verilog Primitives

Table 31—Built-in gates and switches

n_input gates	n_output gates	three-state gates	pull gates	MOS switches	bidirectional switches
and	buf	bufif0	pulldown	cmos	rtran
nand	not	bufif1	pullup	nmos	rtranif0
nor		notif0		pmos	rtranif1
or		notif1		rcmos	tran
xnor				rnmos	tranif0
xor				rpmos	tranif1

- The first three columns of primitives are supported by Quartus package.
- *MOS switches*, *bidirectional switches*, and *pull gates* are not supported by Quartus.

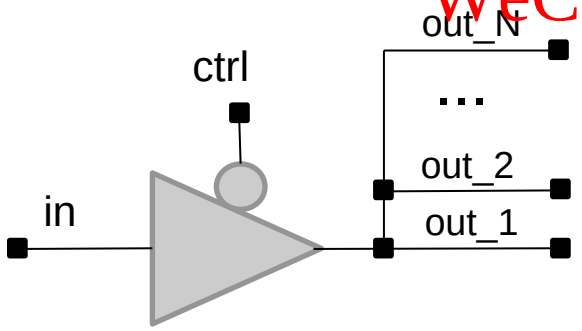
Three-State Gates

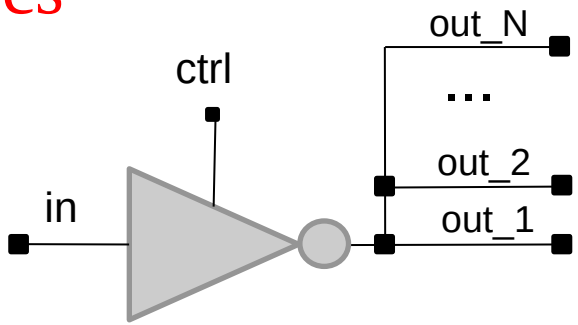
Control

	bufif0	0	1	x	z
input	0				
	1				
	x				
	z				

Control

	notif1	0	1	x	z
input	0				
	1				
	x				
	z				





L means 0 or z
H means 1 or z

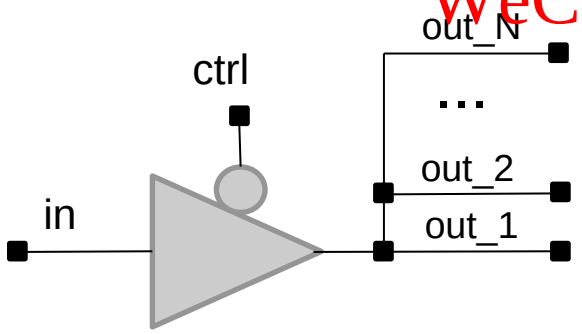
Three-State Gates (Tri-State Gates)

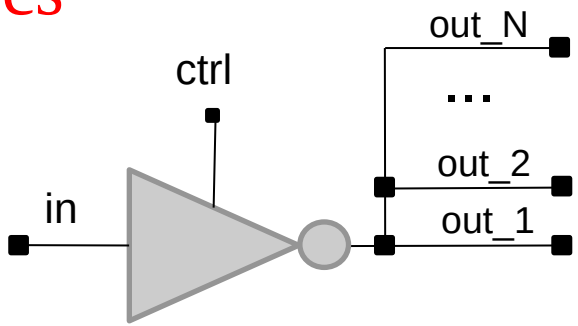
Control

	bufif0	0	1	x	z
input	0	0	z	L	L
	1	1	z	H	H
	x	x	z	x	x
	z	x	z	x	x

Control

	notif1	0	1	x	z
input	0				
	1				
	x				
	z				





L means 0 or z
H means 1 or z

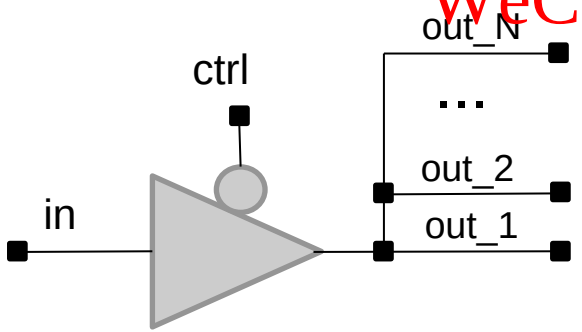
Three-State Gates

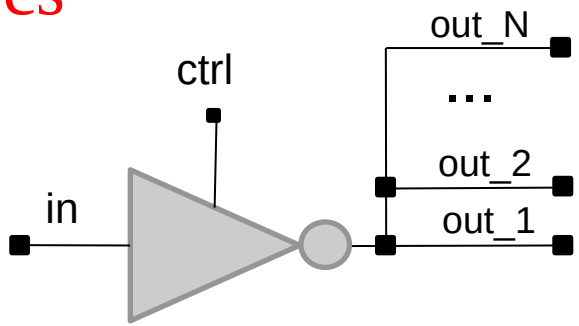
Control

	bufif0	0	1	x	z
input	0	0	z	L	L
	1	1	z	H	H
	x	x	z	x	x
	z	x	z	x	x

Control

	notif1	0	1	x	z
input	0	z	1	H	H
	1	z	0	L	L
	x	z	x	x	x
	z	z	x	x	x





L means 0 or z
H means 1 or z