UNIVERSITY OF LIVERPOOL

Department of Electrical Engineering and Electronics

ELEC373

Digital Systems Design
Assignment 2
UART (Universal Asynchronous Receiver and Transmitter)

Module	ELEC373
Coursework name	Assignment 2
Component weight	Assignment 2 = 25%
Semester	1 + 2
HE Level	6
Lab location	EEE Building PC labs 301, 304 as timetabled – Friday 2-5pm
Work	Individually
Timetabled time	15 hours (3 hours per week – Friday 2pm – 5pm)
Suggested private study	10 hours including report writing
Assessment method	Individual, formal word-processed reports (Block diagrams and ASMs can be hand drawn and scanned into the report)
Submission format	Online via CANVAS
Submission deadline	Assignment 2: Friday Week 1 Semester 2 - 4th February 2022
Late submission	Standard University penalties apply
Resit opportunity	Students Failing Assignment 2 and the full module will have an equivalent Assignment 2 as the resit opportunity to complete over the Summer.
Marking policy	Marked and moderated independently
Anonymous marking	Yes
Feedback	Via comments on CANVAS submission on-line
Learning outcomes	LO1: Ability to design digital systems using the ASM design method LO2: Ability to implement digital systems using the Verilog Hardware Description Language

Marking Criteria

Section	Marks available	Indicative characteristics	
		Adequate / pass (40%)	**Very good / Excellent**
Presentation and structure	10%	• Contains cover page information, table of contents, sections with appropriate headings. • Comprehensible language; punctuation, grammar and spelling accurate. • Equations legible, numbered and presented correctly. • Appropriately formatted reference list.	• Appropriate use of technical, mathematic and academic terminology and conventions. • Word processed with consistent formatting. • Pages numbered, figures and tables captioned. • All sections clearly signposted. • Correct cross-referencing (of figures, tables, equations) and citations.
Introduction, Method and Design	50%	• Problem background introduced clearly. • Evidence of a Top Down Design approach • Conceptual Design Choices introduced. • Design of each module follows a logical sequence. • ASMs correspond to designs for required blocks.	• Appropriate range of references used. • Design decisions justified with alternatives given. • Calculations shown in full, justifying and explaining any decisions. • Correct ASM Syntax used. • Well-structured Verilog Code • Fully synchronous design
Results	30%	• Simulation results present for each block and well annotated. • Results of full system in both simulation and experimentally presented. • Results for each task accompanied by a commentary. • Screen shots of results presented.	• Simulations demonstrate that every pathway in each ASM is functioning correctly. • Tests indicate that there are no problems caused by asynchronous inputs.
Discussion	10%	• Discussion on what worked and what didn't. • Critical assessment on the design – strength and weaknesses	• Discussion on how the system was fully tested.

ELEC 373 Verilog Assignment 2 (2021-2022)

Assignment Overview

This assignment continues from Assignment 1 which was set to get you familiar with designing digital systems and synthesising them from a Verilog description. Again, you should develop your design using Altera's Quartus II V13.0-SP1.

The second assignment is for you to undertake the full design process i.e. the conceptual design, communicated by block diagrams, and the embodiment design communicated by ASM charts. You should then code in Verilog and test the design on the DE2 boards in the lab. You will use a USB->RS232 cable to connect the DE2 Board to the PC.

Assignment Outline

The DE2 Board has a 9 pin D type connector and associated level shifting circuitry to allow the board to be connected to the RS232 port of another electronic device. Figure 1 shows the circuit on the DE2 board which includes a MAX232 device that performs the voltage conversion and also two LEDs which indicate if there is any activity on the transmit or receive signals.

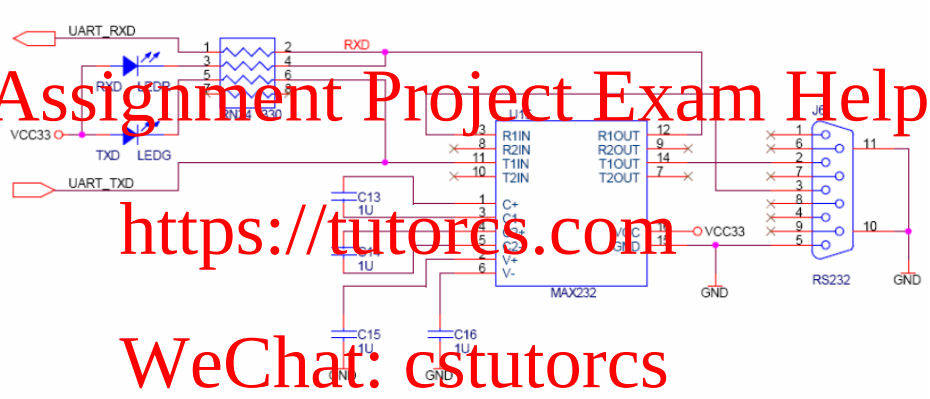

Figure 1 RS232 Level conversion circuit

Table 1 shows which pins of the FPGA are connected to the MAX232 device. Note that UART_RXD is the input received signal as received on pin 3 of the 9 pin D-Type and UART_TXD is the output transmitted signal sent to pin 2 of the 9 pin D-Type. Pin 5 carries the GND signal between the two systems.

Table 1 FPGA Pin connections

Signal Name	FPGA Pin No.	Description
UART_RXD	PIN_C25	UART Receiver
UART_TXD	PIN_B25	UART Transmitter

For the first assignment you developed a UART transmitter to serially transmit data from the DE2 board via the serial link to a PC running a terminal program. The PC should then have displayed the ASCII value of the data transmitted. For example if 0x41 was transmitted a capital 'A' should be displayed. The data is entered by keying in the binary data on the "inputs" and then transmitted when the "send" key is pressed. You should also have displayed in HEX on the T-Display seven segment displays (indicated in Table 2) the value of the data to be transmitted. The data should be transmitted with the baud, parity and number of bits indicated in Table 2.

For the second assignment you are allowed to modify your design for the 1st Assignment but also include a receiver in your design such that when a keyboard character is pressed in Putty (or any other terminal emulator on the PC) the ASCII code is displayed in HEX on the R-Display 7 segment displays. You should also drive 2 LEDs to indicate if the last character received had a Parity Error or if it had a Framing Error. A Framing Error is when, instead of a stop bit (Logic 1) being received, a Logic 0 is received.

Make sure that your design is fully synchronous, i.e. all the D type flipflops should be clocked by the system clock. You should also aim to re-use modules, for example you probably need two shift registers, one for the transmitter and one for the receiver. It is best to design once and use twice as you will then only need to design, test and document one shift register rather than two. If logic isn't used in a block then the synthesiser will remove the logic so it won't be wasting resources. Similarly you may want to design a single counter but use it a number of times with the count value set by a parameter.

You should include a top level file to connect your modules together. This top level file can be either a "bdf" or Verilog file.

Remember you need to follow a top-down design methodology.

Report – Assignment 2

Your report should include the following.

1) Description of Architecture(s) and Controller(s) (with block diagram showing interconnections). (Maximum 2 pages A4)
2) Description of each module to be documented by the following information
    a. ASM Charts for any Algorithmic State Machines and any combinational logic (Remember Combinational Logic can be treated as a single state ASM).
    b. Commented Verilog code for each module.
    c. Full simulation of each module. (With annotations indicating what the simulation proves).

    This information should be grouped together for each module i.e. there should be a single section covering the above for each module. Don't list all the ASMs then all the Verilog, Document each block almost as a stand-alone report.

3) Schematic of the full system.
4) Simulation of the full system. (With annotations and maximum ½ page on any comments)
5) Explanation of experimental test results. (Max 1 page)
6) Conclusion (Maximum ½ page)
7) You should also submit your design via Canvas. Make sure all the files need to compile simulate and test the design are included.

Please format your report in the order indicated above, i.e. fully document each module before describing the next module. Also, as this is being marked on a computer screen, please rotate any landscape pages in the pdf file so that they are the correct way up when viewed on the screen. Note that you can reuse any text, diagrams from your Assignment 1 report for the Assignment 2 report.

Warning

When marking the reports I will be looking very closely for any signs of collusion, as this is unacceptable. I need to assess your own ability not that of your friend or colleague. If I find any evidence of collusion then the formal University rules will be followed which may result in your suspension.

Assignment 2 Submission Deadline

Bench inspections where you will demonstrate your system (1st Lab of Semester 2)
You only need to submit an Electronic copy: Friday 4th February 2022 @ 11:59pm.
You also need to submit a ZIP file of your modules by the same date and time.

J.S. Smith
11th November 2021 (Corrected 23rd November 2021)

Table 2 – Assignment parameters

ID	Student Name	Baud Rate	Parity	Data Bits	Inputs	Send	T-Display	R-Display	Parity Error	Framing Error
201403467	Afflick, William	9600	Odd	7	Sw[6:0]	Key0	Hex7-6	Hex5-4	LEDR[1]	LEDR[0]
201387721	Al-Kuwari, Saad Nasser Y	19200	Odd	7	Sw[7:1]	Key1	Hex6-5	Hex4-3	LEDR[2]	LEDR[1]
201361177	Ali, Wasif	38400	Odd	7	Sw[8:2]	Key2	Hex5-4	Hex3-2	LEDR[3]	LEDR[2]
201414740	Barraclough, Luke	57600	Odd	7	Sw[9:3]	Key3	Hex4-3	Hex2-1	LEDR[4]	LEDR[3]
201357415	Chan, Alvin John	9600	Even	7	Sw[10:4]	Key0	Hex3-2	Hex1-0	LEDR[5]	LEDR[4]
201608805	Chapman, Kathryn Julia	19200	Even	7	Sw[11:5]	Key1	Hex2-1	Hex7-6	LEDR[6]	LEDR[5]
201521677	Chen, Kaien	38400	Even	7	Sw[12:6]	Key2	Hex1-0	Hex6-5	LEDR[7]	LEDR[6]
201520758	Chen, Yanbing	57600	Even	7	Sw[13:7]	Key3	Hex7-6	Hex5-4	LEDR[8]	LEDR[7]
201520796	Dong, Lizhi	9600	Odd	8	Sw[14:7]	Key0	Hex6-5	Hex4-3	LEDR[9]	LEDR[8]
201521819	Fan, Ye	19200	Odd	8	Sw[15:8]	Key1	Hex5-4	Hex3-2	LEDR[10]	LEDR[9]
201521835	Gao, Chenxi	38400	Odd	8	Sw[16:9]	Key2	Hex4-3	Hex2-1	LEDR[11]	LEDR[10]
201522071	Liang, Xiaotian	57600	Odd	8	Sw[17:10]	Key3	Hex3-2	Hex1-0	LEDR[12]	LEDR[11]
201522104	Liu, Hechen	9600	Even	8	Sw[7:0]	Key0	Hex2-1	Hex7-6	LEDR[13]	LEDR[12]
201522114	Liu, Mengyuan	19200	Even	8	Sw[8:1]	Key1	Hex1-0	Hex6-5	LEDR[1]	LEDR[0]
201431464	McNally, Jack	38400	Even	8	Sw[9:2]	Key2	Hex7-6	Hex5-4	LEDR[2]	LEDR[1]
201454028	Muralidharan, Sabareesh	57600	Even	8	Sw[10:3]	Key3	Hex6-5	Hex4-3	LEDR[3]	LEDR[2]
201522241	Qin, Xiye	9600	Odd	7	Sw[14:8]	Key0	Hex5-4	Hex3-2	LEDR[4]	LEDR[3]
201521147	Shen, Qifeng	19200	Odd	7	Sw[15:9]	Key1	Hex4-3	Hex2-1	LEDR[5]	LEDR[4]
201522275	Shu, Junyang	38400	Odd	7	Sw[16:10]	Key2	Hex3-2	Hex1-0	LEDR[6]	LEDR[5]
201429869	Tripathi, Roshan	57600	Odd	7	Sw[17:11]	Key3	Hex2-1	Hex7-6	LEDR[7]	LEDR[6]
201521301	Wu, Fan	9600	Even	7	Sw[10:4]	Key0	Hex1-0	Hex6-5	LEDR[8]	LEDR[7]
201448613	Xia, Lei	19200	Even	7	Sw[11:5]	Key1	Hex7-6	Hex5-4	LEDR[9]	LEDR[8]
201522485	Xing, Xiangjing	38400	Even	7	Sw[12:6]	Key2	Hex6-5	Hex4-3	LEDR[10]	LEDR[9]
201521369	Xu, Xiuyuan	57600	Even	7	Sw[13:7]	Key3	Hex5-4	Hex3-2	LEDR[11]	LEDR[10]
201522575	Yin, Yanyang	9600	Odd	8	Sw[14:7]	Key0	Hex4-3	Hex1-0	LEDR[12]	LEDR[11]
201224948	Yuan, Yifei	19200	Odd	8	Sw[15:8]	Key1	Hex3-2	Hex7-6	LEDR[1]	LEDR[0]
201522627	Zhang, Hailong	9600	Odd	8	Sw[17:10]	Key2	Hex1-0	Hex5-4	LEDR[2]	LEDR[1]
201521502	Zhang, Yechengnuo	19200	Odd	8	Sw[7:0]	Key3	Hex7-6	Hex5-4	LEDR[3]	LEDR[2]