Digital System Design ELEC373/473

UNIVERSITY OF LIVERPOOL

Quartus State Machine Wizard

For the Single Pulser example

State Machine Wizard

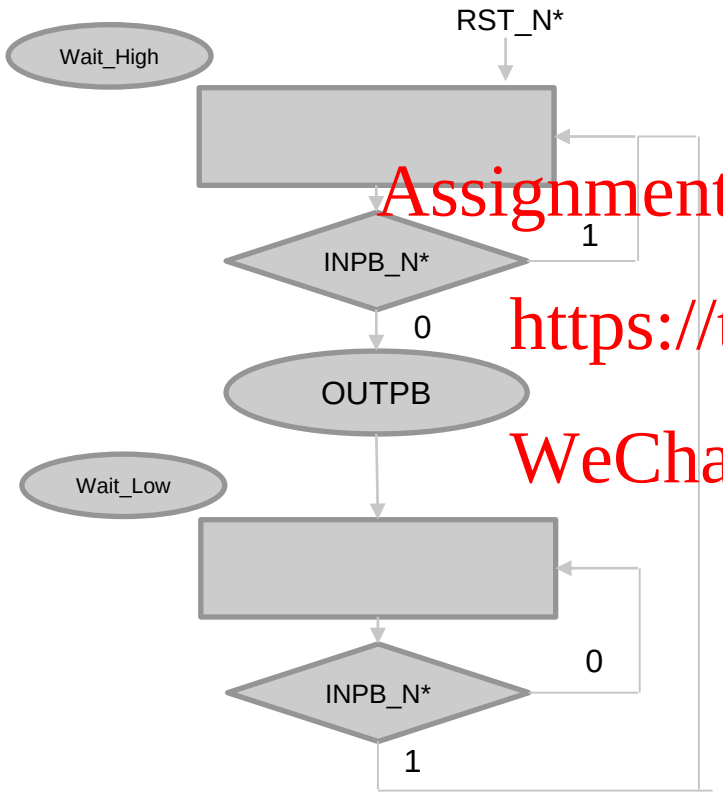
- Some comments
  - It works
  - But….. The Verilog code produced isn't very good.
  - However if you're having difficulty writing Verilog for state machines you could start with the State Machine Wizard and then examine the code.

Single Pulser example

- Objective
  - For push button inputs designers just want to generate a pulse lasting a single clock period rather than for the entire time the button is pressed.
    - For example if it was connected to a counter enable it would just increment once every time the button is pressed.
  - Such a circuit is called a single pulser.
  - On the DE2 Board the input goes low when the button is pressed and high when it is released.

Single Pusler Block Diagram

Single Pulser – ASM (Chart)



Two States:

Wait_High (wait whilst it's high)
Wait_Low (wait whilst it's low)

Two Inputs:

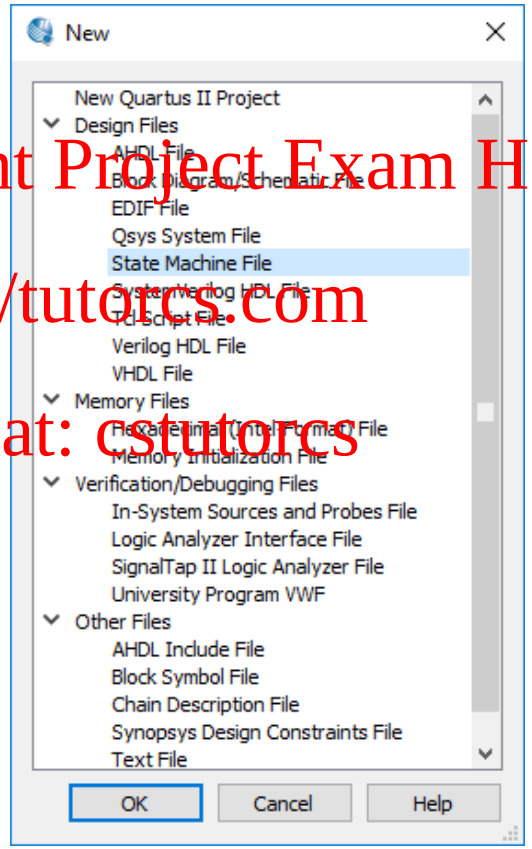
RST_N* (Active low Reset)
INPB_N* (Active low Input)
Note "*" indicates asynchronous input.

One Conditional Output:

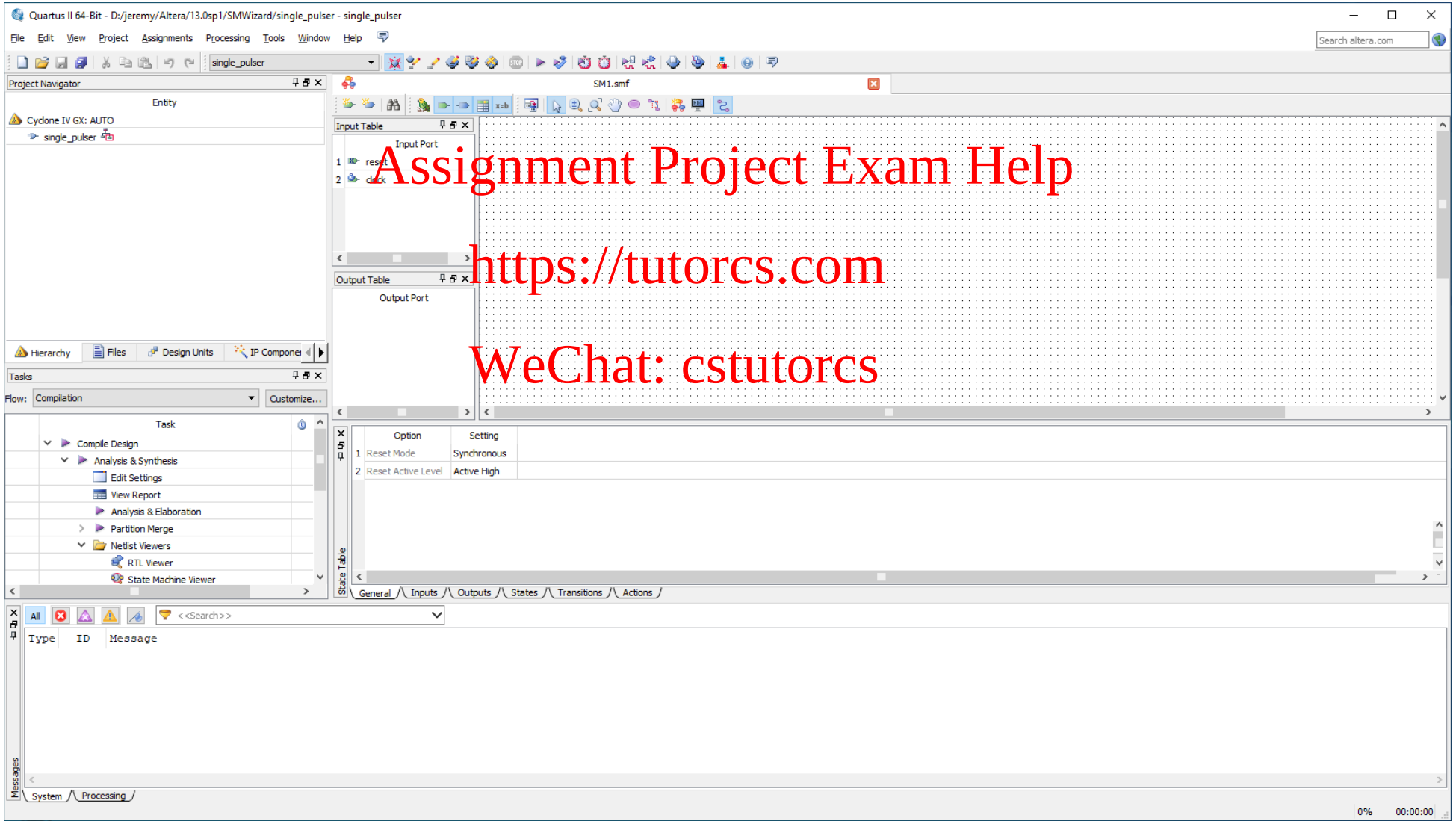
OUTPB (Active High Output)

State Machine Wizard

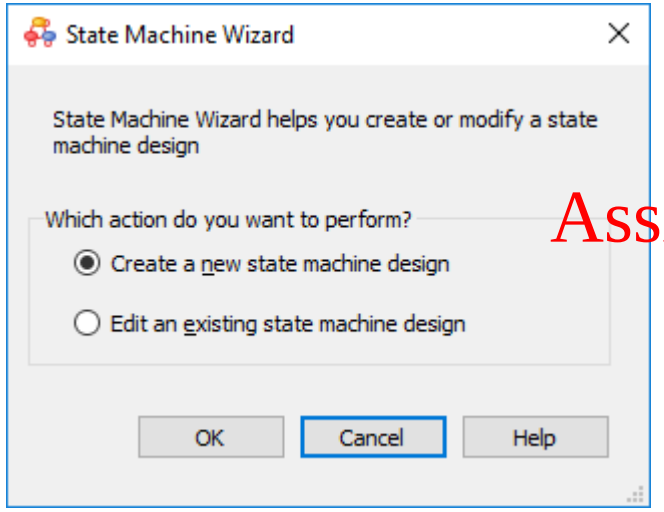
- File -> New
  - State Machine File



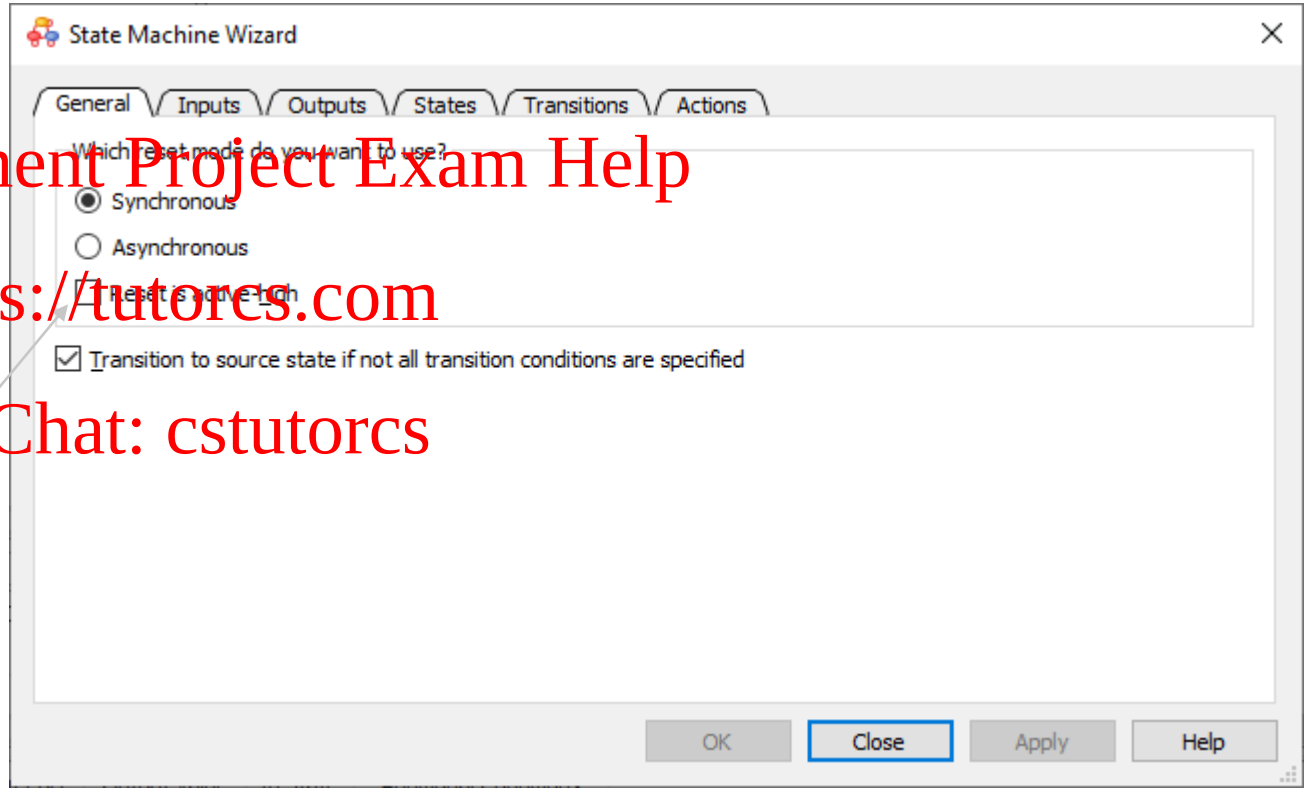
State Machine Wizard - Default



State Machine Wizard

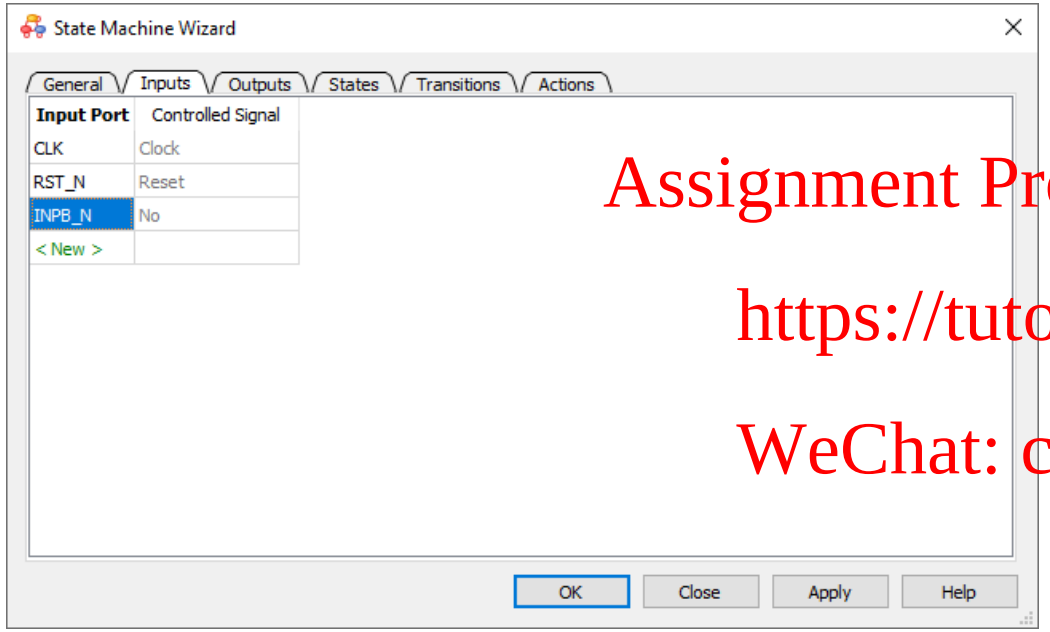


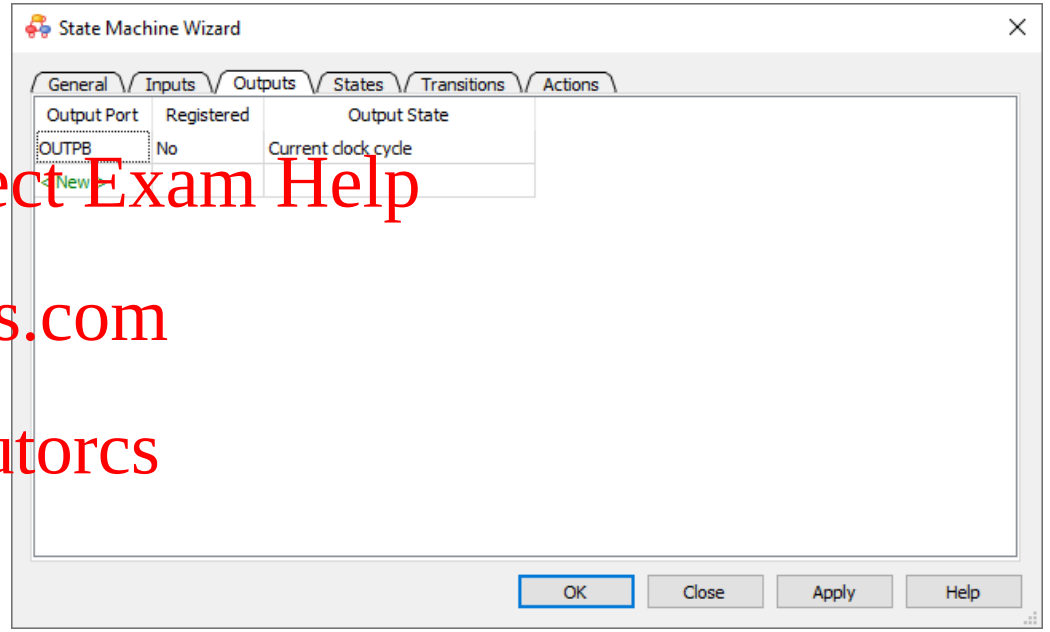
Specify Reset Polarity



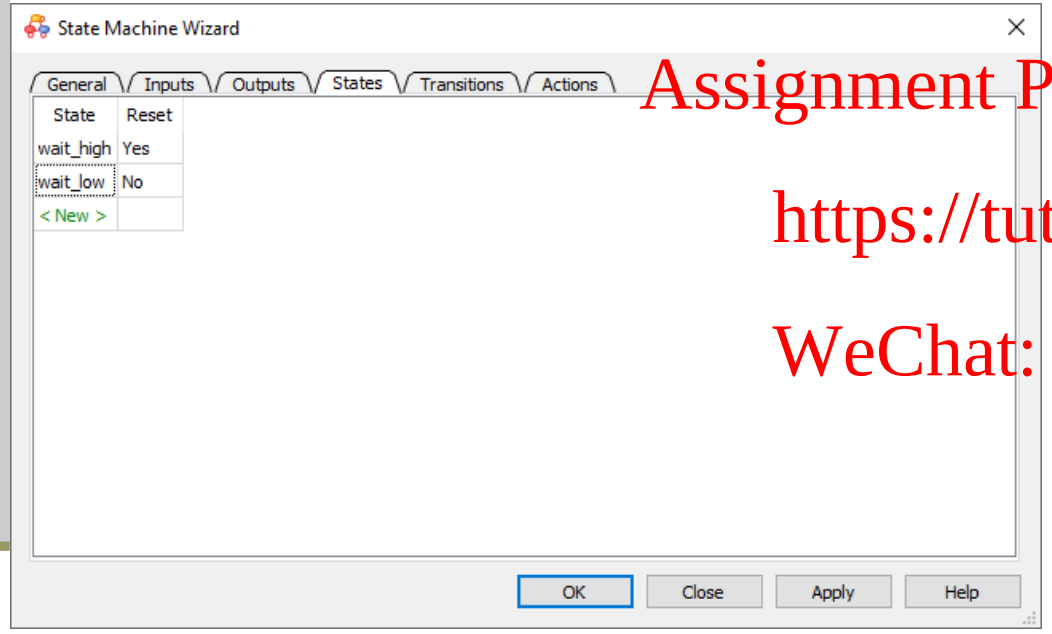
Ideally all transition paths should be specified but if not have it stay in the same state

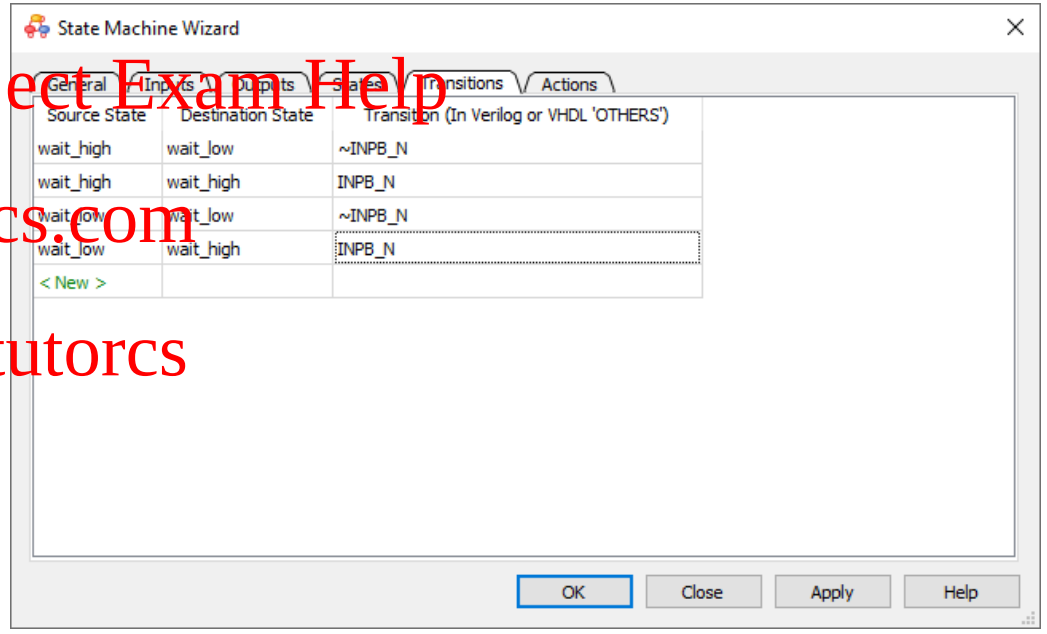
Add Inputs and Outputs



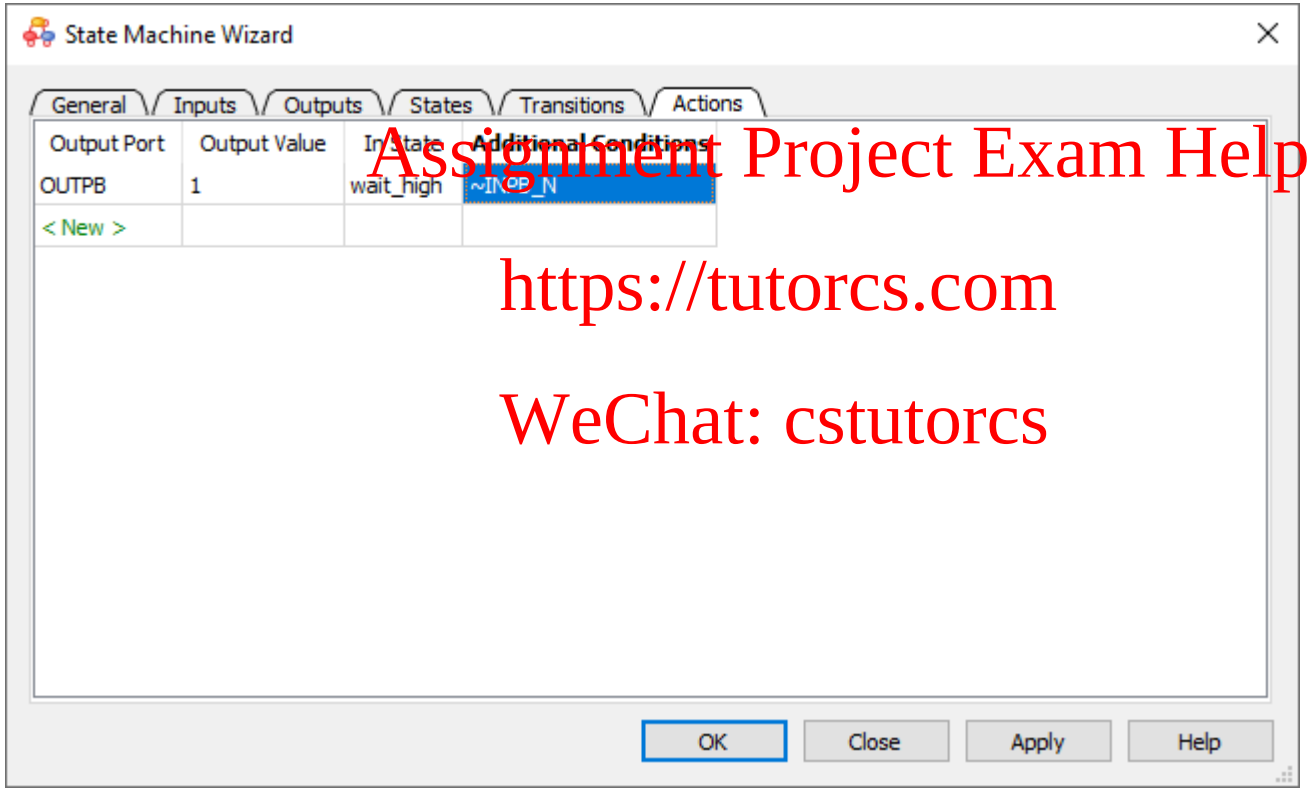


Add States and State Transitions

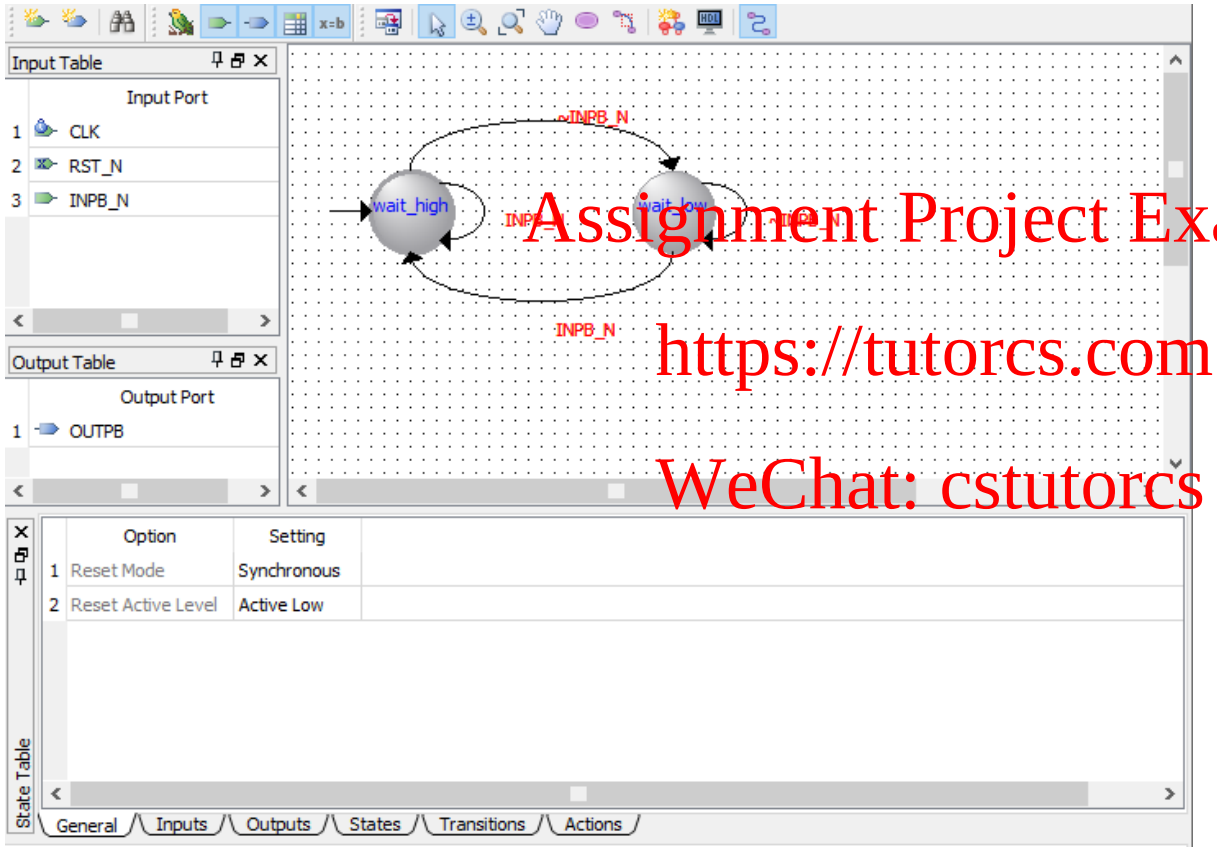


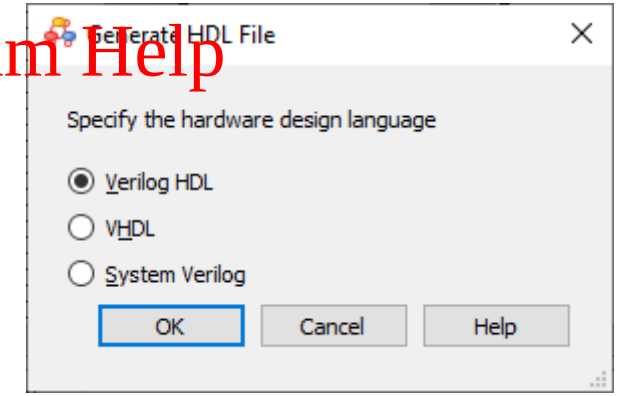


Add Actions - Outputs

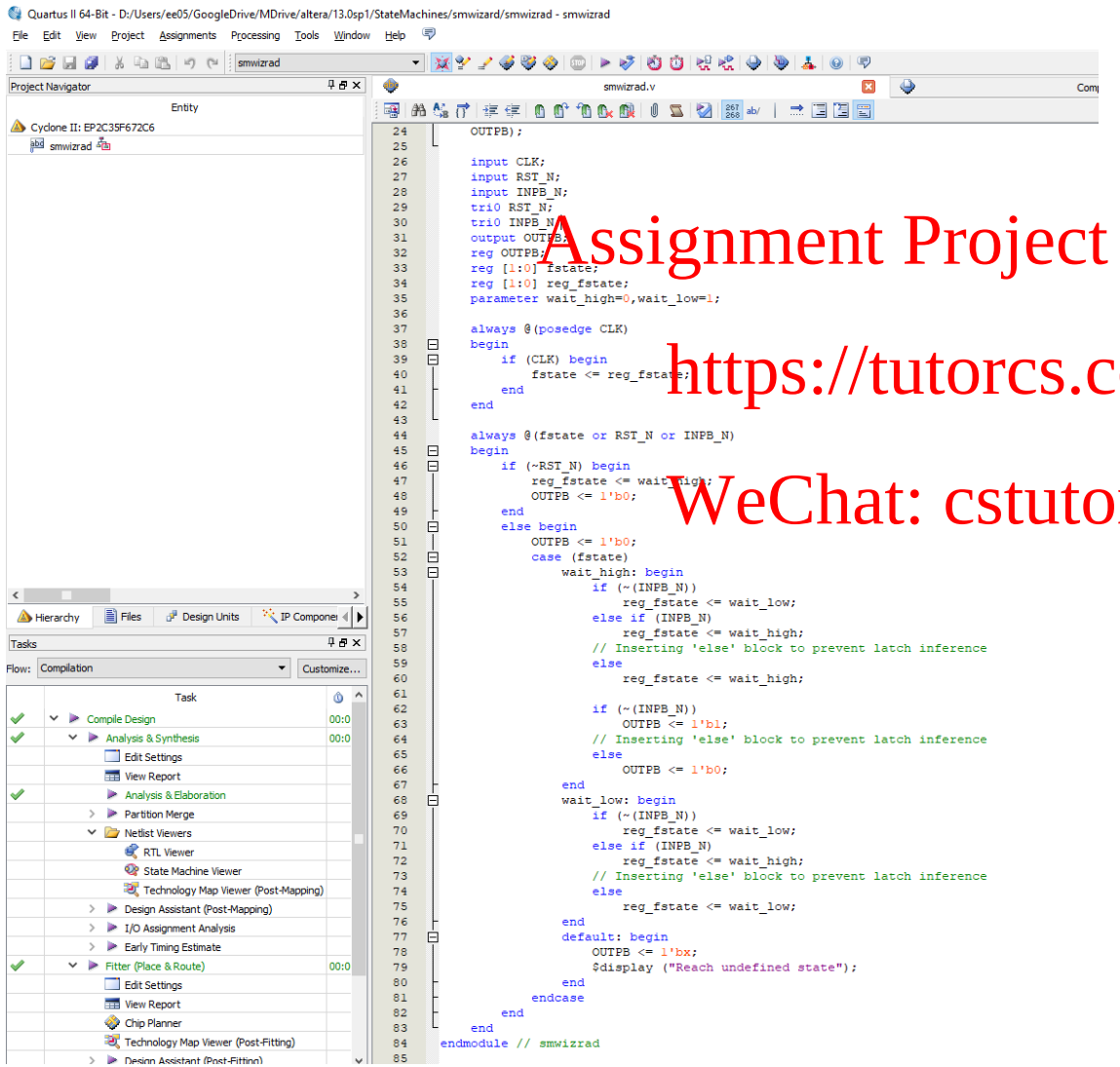


Apply and Generate HDL

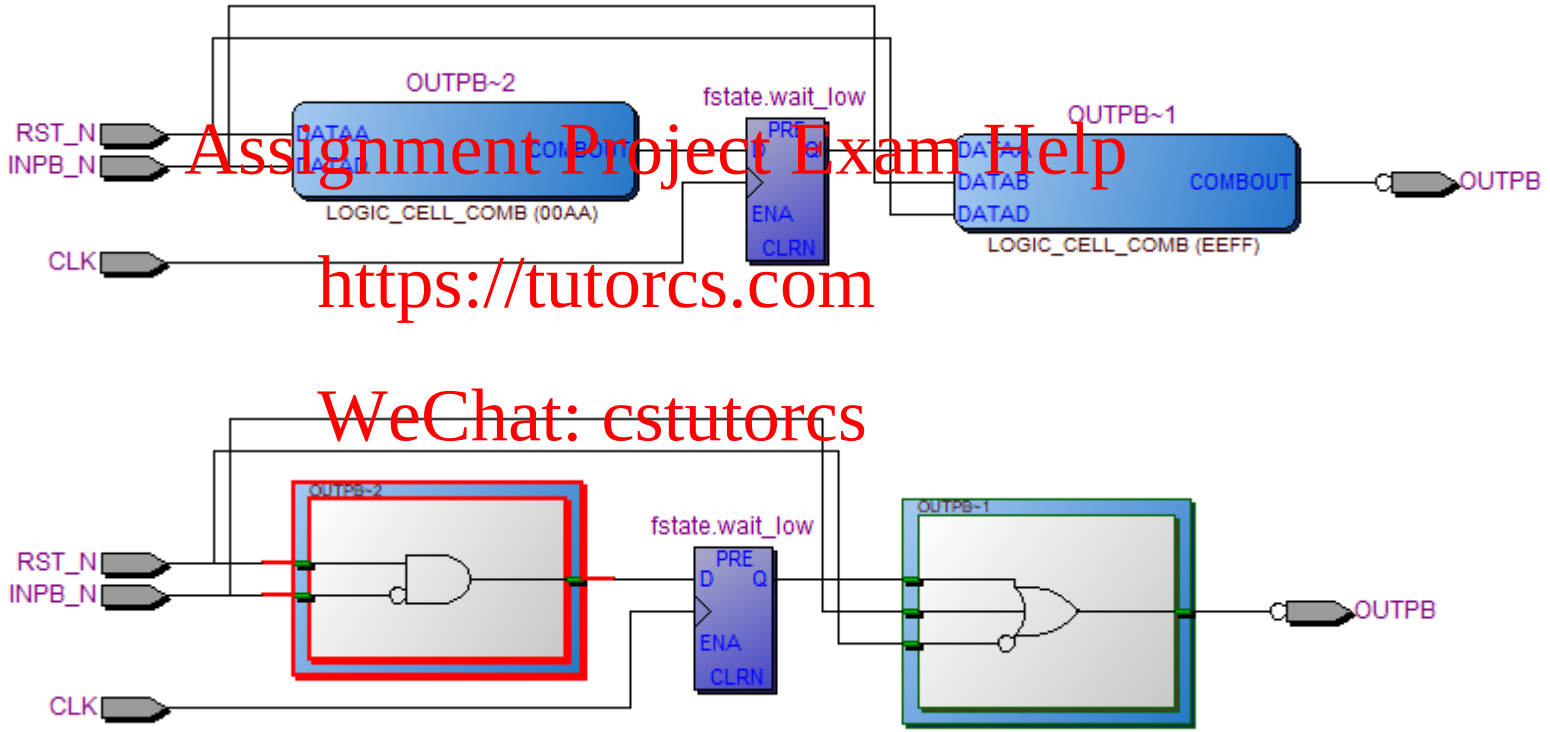




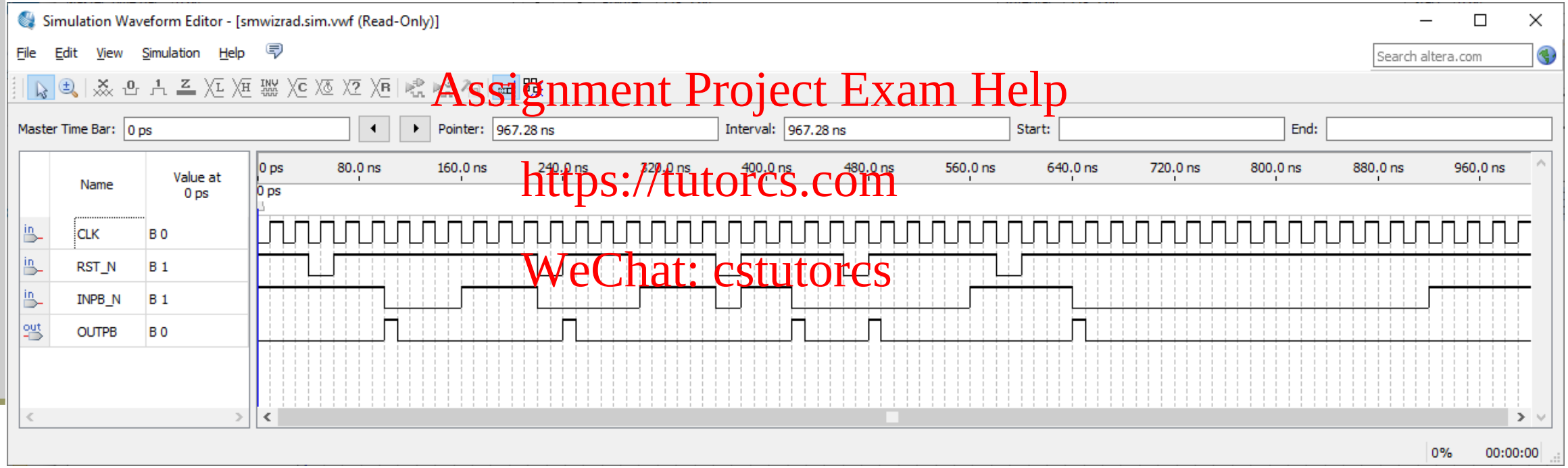
Examine Verilog



Synthesise it and examine design Technology Map Viewer (Tools->Netlist Viewers)



Simulate it



Note: Avoid Asynchronous inputs changing at the same time as the clock edge as this violates the setup and hold requirements.
Best to have inputs changing on the falling edge of the clock.