1 Tensor (Kronecker) Product

For matrices $A = [a_{ij}],\ B = [b_{ij}]$ their tensor product is $A \otimes B = [a_{ij}B]$.

Example 1

$$A = \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix},\ A \otimes B = \begin{pmatrix} a_{11}B & a_{12}B \\ a_{21}B & a_{22}B \end{pmatrix}.$$

The properties of the tensor product that we will use:

$$(A+B) \otimes C = A \otimes C + B \otimes C, C \otimes (A+B) = C \otimes A + C \otimes B, \quad (1)$$
$$(A \otimes B) \otimes C = A \otimes (B \otimes C), \quad (2)$$
$$(A \otimes B)(C \otimes D) = AC \otimes BD. \quad (3)$$

Let $\mathbf{v}_1$ be a vector from the standard basis of $\mathbb{C}^{n_1}$ and $\mathbf{v}_2$ be a vector from the standard basis of $\mathbb{C}^{n_2}$. It is not difficult to see that $\mathbf{v}_{12} = \mathbf{v}_1 \otimes \mathbf{v}_2$ is a vector from the standard basis of $\mathbb{C}^{n_1 n_2}$. It is easy to check that the concatenation rule for vectors in Dirac notation, which we introduced before, is in fact the tensor product.

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Example 2

$$\mathbf{v}_1 = \begin{pmatrix} 0 \\ 1 \end{pmatrix}, \mathbf{v}_2 = \begin{pmatrix} 0 \\ 0 \\ 1 \\ 0 \end{pmatrix}, \mathbf{v}_{12} = \mathbf{v}_1 \otimes \mathbf{v}_2 = \begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 1 \\ 0 \end{pmatrix}.$$

In Dirac notation we have

$$\mathbf{v}_1 = |1\rangle,\ \mathbf{v}_2 = |10\rangle,\ \textit{and}\ \mathbf{v}_{12} = |110\rangle.$$

The concatenation of these vectors in Dirac notation, which we introduced before, gives the same result:

$$|1\rangle|10\rangle = |110\rangle = \mathbf{v}_{12}.$$

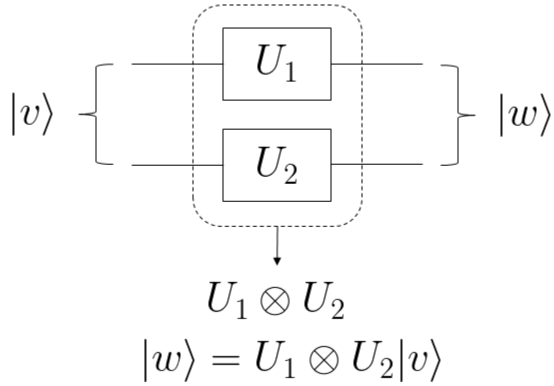

Figure 1: Tensor product of unitary gates

In quantum circuits all gates, except measurements, conducted at the same time mean the unitary operation obtained as the tensor product of the individual unitary operators corresponding to the gates, like it is shown in Fig. 1.

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Example 3 *Let*

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$$U_1 = X = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}, \; U_2 = Z = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}$$

So,

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$$U_1 \otimes U_2 = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix}$$

For a generic quantum state $|v\rangle$ *we have*

$$|v\rangle = \alpha_{00}|00\rangle + ... + \alpha_{11}|11\rangle = \begin{pmatrix} \alpha_{00} \\ \alpha_{01} \\ \alpha_{10} \\ \alpha_{11} \end{pmatrix}$$

$$\begin{aligned} |w\rangle = U_1 \otimes U_2 |v\rangle = U_1 \otimes U_2 \begin{pmatrix} \alpha_{00} \\ \alpha_{01} \\ \alpha_{10} \\ \alpha_{11} \end{pmatrix} &= \begin{pmatrix} \alpha_{10} \\ -\alpha_{11} \\ \alpha_{00} \\ -\alpha_{01} \end{pmatrix} \\ &= \alpha_{10}|00\rangle - \alpha_{11}|01\rangle + \alpha_{00}|10\rangle - \alpha_{01}|11\rangle. \end{aligned} \tag{4}$$

We can do these calculations using only Dirac notations (no linear algebra notations), and in fact it is easier to do computations in this way. Recall that

$$X|0\rangle = |1\rangle,\ X|1\rangle = |0\rangle,\ Z|0\rangle = |0\rangle,\ Z|1\rangle = -|1\rangle.$$

Using this, we get

$$\begin{aligned} U_1 \otimes U_2|v\rangle = X \otimes Z|v\rangle &= \alpha_{00}(X \otimes Z)|00\rangle + ... + \alpha_{11}(X \otimes Z)|11\rangle \\ &= \alpha_{00}(X|0\rangle \otimes Z|0\rangle) + ... + \alpha_{11}(X|1\rangle \otimes Z|1\rangle) \end{aligned}$$

Usually we drop "$\otimes$" and write the last expression as

$$\begin{aligned} &\alpha_{00}(X|0\rangle Z|1\rangle) + ... + \alpha_{11}(X|1\rangle Z|1\rangle) \\ =&\alpha_{00}|1\rangle|0\rangle + \alpha_{01}|1\rangle(-|1\rangle) + \alpha_{10}|0\rangle|0\rangle + \alpha_{11}|0\rangle(-|1\rangle) \\ =&\alpha_{00}|10\rangle - \alpha_{11}|11\rangle + \alpha_{10}|00\rangle - \alpha_{11}|01\rangle. \end{aligned}$$

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Thus we obtained (4).

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Example 4 *Let us consider the next circuit*

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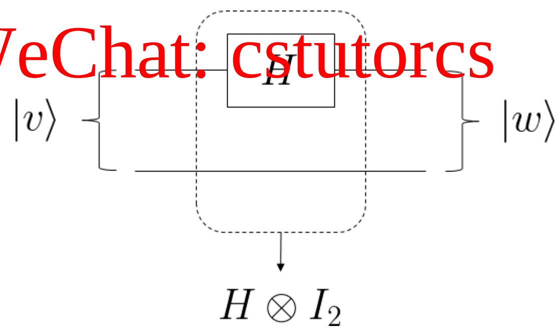

Figure 2: The tensor product of a gate and wire

We recall that

$$H|0\rangle = \frac{1}{\sqrt{2}}(|0\rangle + |1\rangle),\ H|1\rangle = \frac{1}{\sqrt{2}}(|0\rangle - |1\rangle),$$

and therefore

$$|w\rangle = (H \otimes I_2)|v\rangle.$$

We can obtain this result using only Dirac notation:

$$(H \otimes I_2)|v\rangle = \alpha_{00} H|0\rangle|0\rangle + \alpha_{01} H|0\rangle|1\rangle + \alpha_{10} H|1\rangle|0\rangle + \alpha_{11} H|1\rangle|1\rangle$$

$\boxed{\textit{We used that } I_2|0\rangle = |0\rangle,\ I_2|1\rangle = |1\rangle}$

$$= \alpha_{00}\frac{1}{\sqrt{2}}(|0\rangle + |1\rangle)|0\rangle + \alpha_{01}\frac{1}{\sqrt{2}}(|0\rangle + |1\rangle)|1\rangle + \alpha_{10}\frac{1}{\sqrt{2}}(|0\rangle - |1\rangle)|0\rangle + \alpha_{11}\frac{1}{\sqrt{2}}(|0\rangle - |1\rangle)|1\rangle$$

$$= \frac{1}{\sqrt{2}}\Big(\alpha_{00}(|00\rangle + |10\rangle) + \alpha_{01}(|01\rangle + |11\rangle) + \alpha_{10}(|00\rangle - |10\rangle) + \alpha_{11}(|01\rangle - |11\rangle)\Big)$$

$$= \frac{1}{\sqrt{2}}\Big((\alpha_{00} + \alpha_{10})|00\rangle + (\alpha_{01} + \alpha_{11})|01\rangle + (\alpha_{00} - \alpha_{10})|10\rangle + (\alpha_{01} - \alpha_{11})|11\rangle\Big).$$

2 Circuit for Preparing EPR Pairs

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As we discussed an EPR pair is two qubits in the state $\frac{1}{\sqrt{2}}(|00\rangle + |11\rangle)$. The following simple circuit produces for us an EPR pair:

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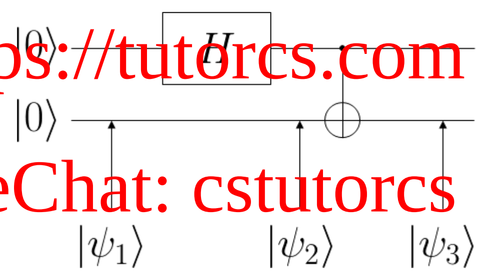

Figure 3: Preparing an EPR pair

$$|\psi_1\rangle = |00\rangle,$$
$$|\psi_2\rangle = (H \otimes I_2)|00\rangle = \frac{1}{\sqrt{2}}(|0\rangle + |1\rangle)|0\rangle = \frac{1}{\sqrt{2}}(|00\rangle + |10\rangle),$$
$$|\psi_3\rangle = \frac{1}{\sqrt{2}}(|00\rangle + |11\rangle).$$

3 Superdense Coding

Superdense coding allows one to send two classical bits by sending only one qubit, under the condition that we shared in advance an EPR pair between the transmitter and receiver.

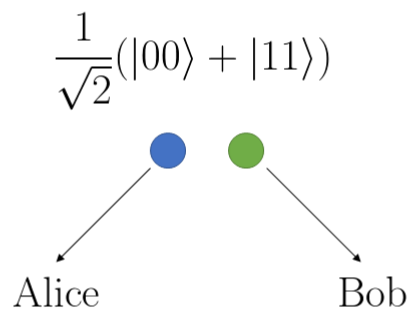

Figure 4: EPR pair is shared in advance between Alice and Bob

1. We prepare 2 qubits in the state $\frac{1}{\sqrt{2}}(|00\rangle + |11\rangle)$. We will use Pauli Matrices:

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$$X = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}, \ Z = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}, \ Y = \begin{bmatrix} 0 & -i \\ i & 0 \end{bmatrix}$$

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2. Alice wants to send 2 classical bits to Bob.

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2 Classical Bits	Alice's Action	New state of the 2 qubits
00	Nothing	$\|\psi_{00}\rangle = \frac{1}{\sqrt{2}}(\|00\rangle + \|11\rangle)$
01	Apply X to 1st qubit	$\|\psi_{01}\rangle = \frac{1}{\sqrt{2}}(\|10\rangle + \|01\rangle)$
10	Apply Z to 1st qubit	$\|\psi_{10}\rangle = \frac{1}{\sqrt{2}}(\|00\rangle - \|11\rangle)$
11	Apply iY to 1st qubit	$\|\psi_{11}\rangle = \frac{1}{\sqrt{2}}(\|01\rangle - \|10\rangle)$

3. Alice sends her qubit to Bob.

4. Now Bob has two qubits in one of the states

$$|\psi_{00}\rangle, \ |\psi_{01}\rangle, \ |\psi_{10}\rangle, \ |\psi_{11}\rangle.$$

5. Bob uses these two qubits as the input for the quantum circuit shown in Fig. 5 and obtains classical bits j_1, j_2.

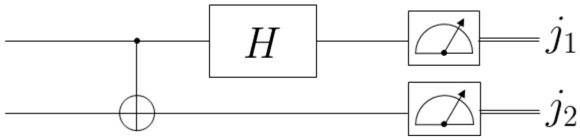

Figure 5: Circuit for restoring classical bits j_1 and j_2

Input States	j_1	j_2
$\lvert\psi_{00}\rangle$	0	0
$\lvert\psi_{01}\rangle$	0	1
$\lvert\psi_{10}\rangle$	1	0
$\lvert\psi_{11}\rangle$	1	1

4 Simulation of Classical Circuits with Quantum Circuits

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Quantum circuits are always reversible (before the measurement blocks) since they are unitary operations. Classical circuits are typically not reversible, for example any 2 inputs and 1 output gate (like AND gate) is not reversible. However, it is possible to convert any classical circuits into reversible form. The complexity of the new classical reversible circuit is only about 2 times larger than the complexity of the original circuit.

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Any classical circuit can be simulated by a quantum circuit. The following quantum circuits, that involve only Toffoli gate, can be used to simulate classical gates. In these circuits quantum states $|a\rangle$ and $|b\rangle$ can take only values $|0\rangle$ or $|1\rangle$ and therefore their behaviour is classical.

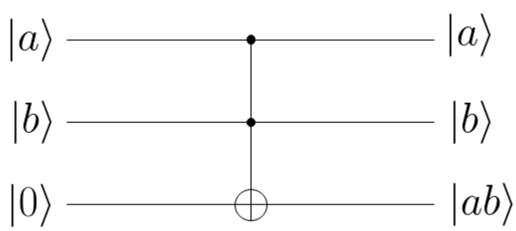

Figure 6: Simulation of AND gate

Example 5 *The quantum circuits shown on Fig. 9 and Fig. 10 simulate classical NAND gate (the second circuit is simpler of course):*

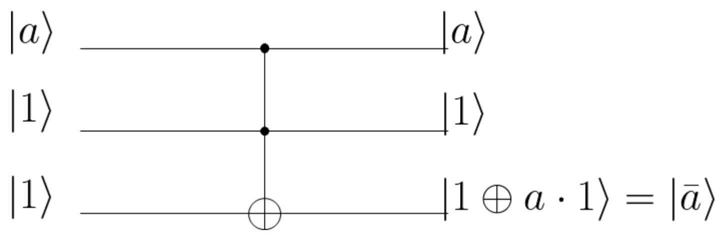

Figure 7: Simulation of NOT gate

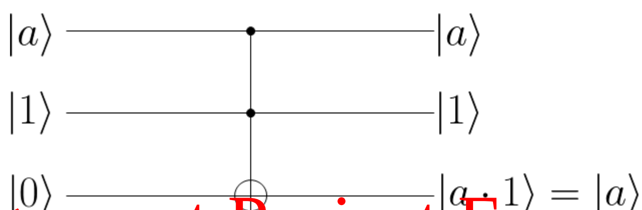

Figure 8: Simulation of FANOUT gate

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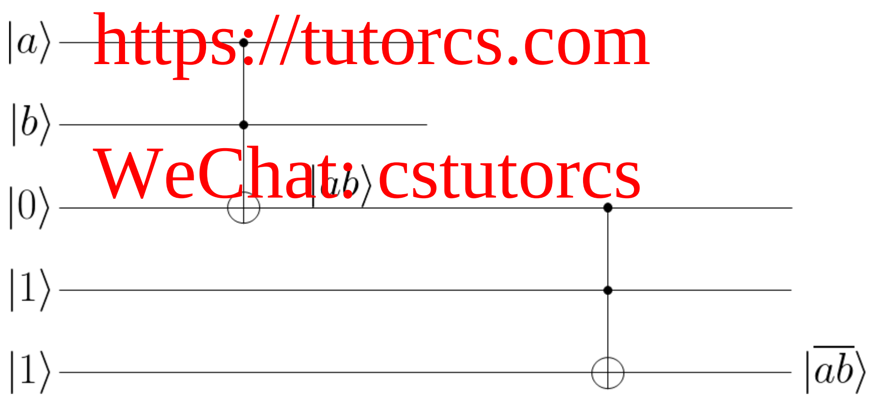

Figure 9: Simulation of NAND gate

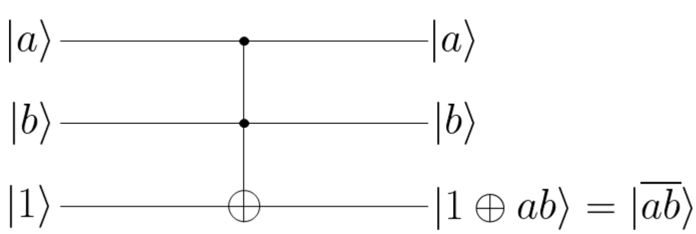

Figure 10: More efficient simulation of NAND gate