RIPPLE Carry Adder

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -4

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 13.433ns

Timing Detail:

All values displayed in nanoseconds (ns)

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Timing constraint: Default path analysis
Total number of paths / destination ports: 49 / 5

Delay: 13.433ns (Levels of Logic = 6)
Source: b<1> (PAD)
Destination: c_out (PAD)

Data Path: b<1> to c_out

Cell:in->out	Gate fanout	Net Delay	Delay	Logical Name (Net Name)
IBUF:I->O	2	0.821	1.216	b_1_IBUF (b_1_IBUF)
LUT2:I0->O	2	0.551	0.903	Mxor_c_1_xor0000_Result1 (c_1_xor0000)
LUT4:I3->O	3	0.551	0.975	c_out_and000111 (add0001_and0000)
LUT4:I2->O	1	0.551	0.869	Madd_c_out_Madd_xor<0>11_SW0 (N22)
LUT3:I2->O	1	0.551	0.801	Madd_c_out_Madd_xor<0>11 (c_out_OBUF)
OBUF:I->O		5.644		c_out_OBUF (c_out)
Total		13.433ns (8.669ns logic, 4.764ns route) (64.5% logic, 35.5% route)		

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Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 3.99 secs

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Total memory usage is 255316 kilobytes

Number of errors   :   0 (0 filtered)
Number of warnings :   9 (0 filtered)
Number of infos   :   0 (0 filtered)

HYBRID Adder

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -4

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 15.133ns

Timing Detail:

All values displayed in nanoseconds (ns)

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Timing constraint: Default path analysis
  Total number of paths / destination ports: 433 / 9

Delay: 15.133ns (Levels of Logic = 10)
  Source: a<1> (PAD)
  Destination: c_out (PAD)

  Data Path: a<1> to c_out
                          Gate   Net
    Cell:in->out   fanout   Delay   Delay Logical Name (Net Name)
    -- ------------
     IBUF:I->O   4   0.821   1.256 a_1_IBUF (a_1_IBUF)
     LUT4:I0->O   1   0.551   0.000 A2/Madd_AUX_1_addsub0001_cy<0>12
(A2/Madd_AUX_1_addsub0001_cy<0>11)
     MUXF5:I0->O   5   0.360   0.989 A2/Madd_AUX_1_addsub0001_cy<0>1_f5
(A2/Madd_AUX_1_addsub0001_cy<0>)
     LUT4:I2->O   1   0.551   0.000 A4/Madd_AUX_1_addsub0001_cy<0>11
(A4/Madd_AUX_1_addsub0001_cy<0>1)
     MUXF5:I1->O   5   0.360   0.989 A4/Madd_AUX_1_addsub0001_cy<0>1_f5
(A4/Madd_AUX_1_addsub0001_cy<0>)
     LUT4:I2->O   1   0.551   0.000 A6/Madd_AUX_1_addsub0001_cy<0>11
(A6/Madd_AUX_1_addsub0001_cy<0>1)
     MUXF5:I1->O   5   0.360   0.989 A6/Madd_AUX_1_addsub0001_cy<0>1_f5
(A6/Madd_AUX_1_addsub0001_cy<0>)
     LUT4:I2->O   1   0.551   0.000 A8/Madd_AUX_1_addsub0001_cy<0>11
(A8/Madd_AUX_1_addsub0001_cy<0>1)
     MUXF5:I1->O   1   0.360   0.801 A8/Madd_AUX_1_addsub0001_cy<0>1_f5
(A8/Madd_AUX_1_addsub0001_cy<0>)
     OBUF:I->O   5.644   c_out_OBUF (c_out)

    Total   15.133ns (10.109ns logic, 5.024ns route)
                              (66.8% logic, 33.2% route)

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Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 3.71 secs

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Total memory usage is 257364 kilobytes

Number of errors   :   0 (0 filtered)
Number of warnings :   0 (0 filtered)
Number of infos   :   0 (0 filtered)

BIT Serial Adder

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

Clock Signal	Clock buffer(FF name)	Load
clk	BUFGP	25

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -4

Minimum period: 4.216ns (Maximum Frequency: 237.192MHz)
Minimum input arrival time before clock: 5.021ns
Maximum output required time after clock: 9.038ns
Maximum combinational path delay: No path found

Timing Detail:

All values displayed in nanoseconds (ns)

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Timing constraint: Default period analysis for Clock 'clk'
Clock period: 4.216ns (frequency: 237.192MHz)
Total number of paths / destination ports: 27 / 23

```
---------------------------------------------------------------------------
Delay:               4.216ns (Levels of Logic = 2)
  Source:            SL1/s_0 (FF)
  Destination:       D/d_rnm0 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: SL1/s_0 to D/d_rnm0
                          Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q              3   0.720   1.246  SL1/s_0 (SL1/s_0)
     LUT3:I0->O           2   0.551   0.945  A/Madd_AUX_1_addsub0001_cy<0>11
(A/Madd_AUX_1_addsub0001_cy<0>)
     LUT3:I2->O           1   0.551   0.000  D/d_rnm0_mux00001 (D/d_rnm0_mux0000)
     FD:D                 0.203          D/d_rnm0
    ----------------------------------------
    Total                 4.216ns (2.025ns logic, 2.191ns route)
                             (48.0% logic, 52.0% route)

===========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 50 / 27
---------------------------------------------------------------------------
Offset:              5.021ns (Levels of Logic = 2)
  Source:            load (PAD)
  Destination:       S/s_0 (FF)
  Destination Clock: clk rising

  Data Path: load to S/s_0
                          Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O           17   0.821   1.540  load_IBUF (load_IBUF)
     LUT2:I1->O           8   0.551   1.083  S/s_7_not00011 (S/s_7_not0001)
     FDR:R                1.026          S/s_7
    ----------------------------------------
    Total                 5.021ns (2.398ns logic, 2.623ns route)
                             (47.8% logic, 52.2% route)

===========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 17 / 13
---------------------------------------------------------------------------
Offset:              9.038ns (Levels of Logic = 2)
  Source:            SL1/s_0 (FF)
  Destination:       c_out (PAD)
  Source Clock:      clk rising

  Data Path: SL1/s_0 to c_out
                          Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
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    ----------------------------------------  ------------
     FD:C->Q              3   0.720   1.246  SL1/s_0 (SL1/s_0)
     LUT3:I0->O           2   0.551   0.877  A/Madd_AUX_1_addsub0001_cy<0>11
(A/Madd_AUX_1_addsub0001_cy<0>)
     OBUF:I->O                 5.644         c_out_OBUF (c_out)
    ----------------------------------------
    Total                     9.038ns (6.915ns logic, 2.123ns route)
                                  (76.5% logic, 23.5% route)

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 Total REAL time to Xst completion: 3.00 secs
 Total CPU time to Xst completion: 3.56 secs

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 Total memory usage is 255764 kilobytes

 Number of errors   :    0 (   0 filtered)
 Number of warnings :    2 (   0 filtered)
 Number of infos    :    0 (   0 filtered)
```