

# CS & IT ENGINEERING

Digital Logic  
Combinational Circuit



DPP 02 Discussion Notes



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## TOPICS TO BE COVERED

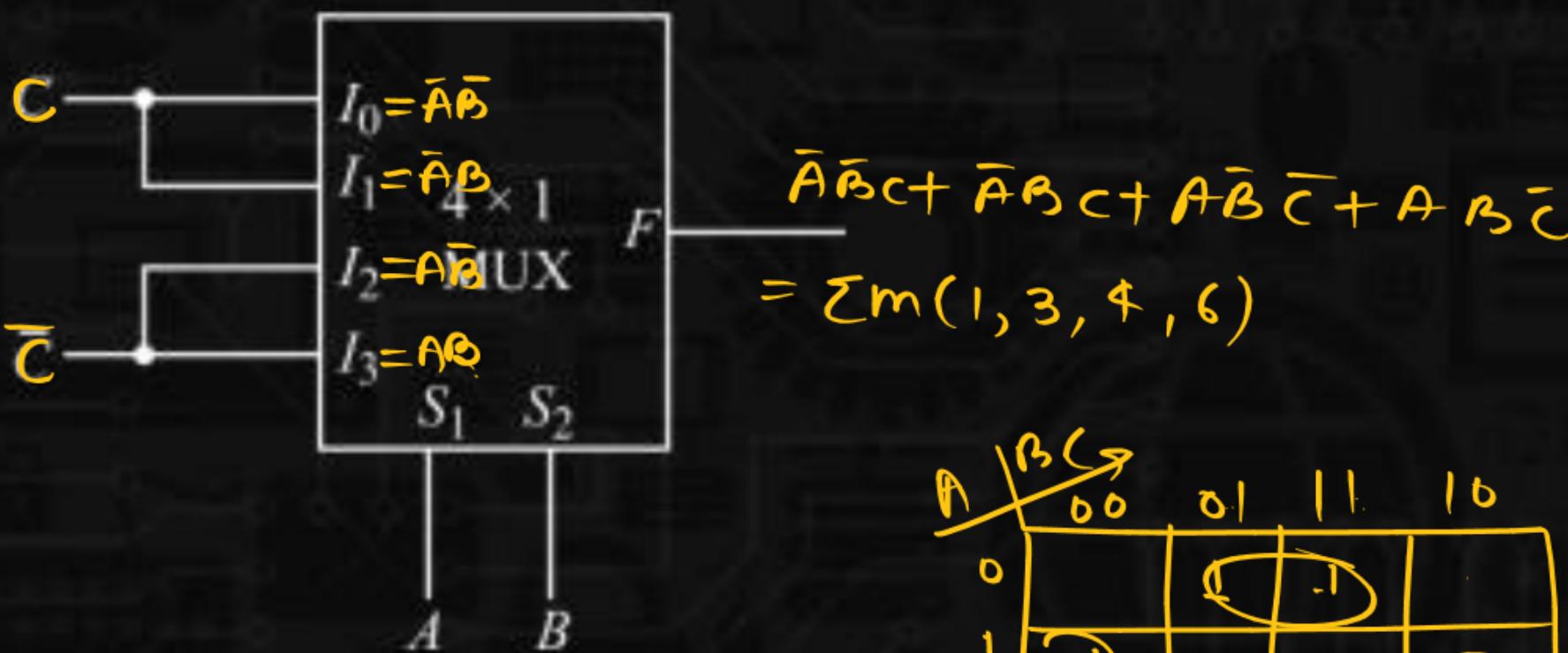
01 DPP Question

## K Map - Basics

- ✓ Attend the class with positive attitude.
- ✓ Punctuality is necessary.
- ✓ Follow the day-wise study plan.
- ✓ Attempt DPP daily as per the schedule.
- ✓ Hold chat while attending the class. We will allow you to ask and put your questions in the comment box.

Q.1

The logic realized by the circuit shown in figure is



A	B	C	00	01	11	10
0	1	1	1	0	0	1
1	0	0	0	1	1	0

- A.  $F = A \odot C$
- B.  $F = B \odot C,$

C.

D.

$F = A \oplus C$

$F = B \oplus C$

$$\bar{A}C + A\bar{C}$$

$$A \oplus C$$

**Q.2**

The minimum number of 2-to-1 multiplexers required to realize a 4-to-1 multiplexer is

- A. 1
- B. 2
- C. 3
- D. 4

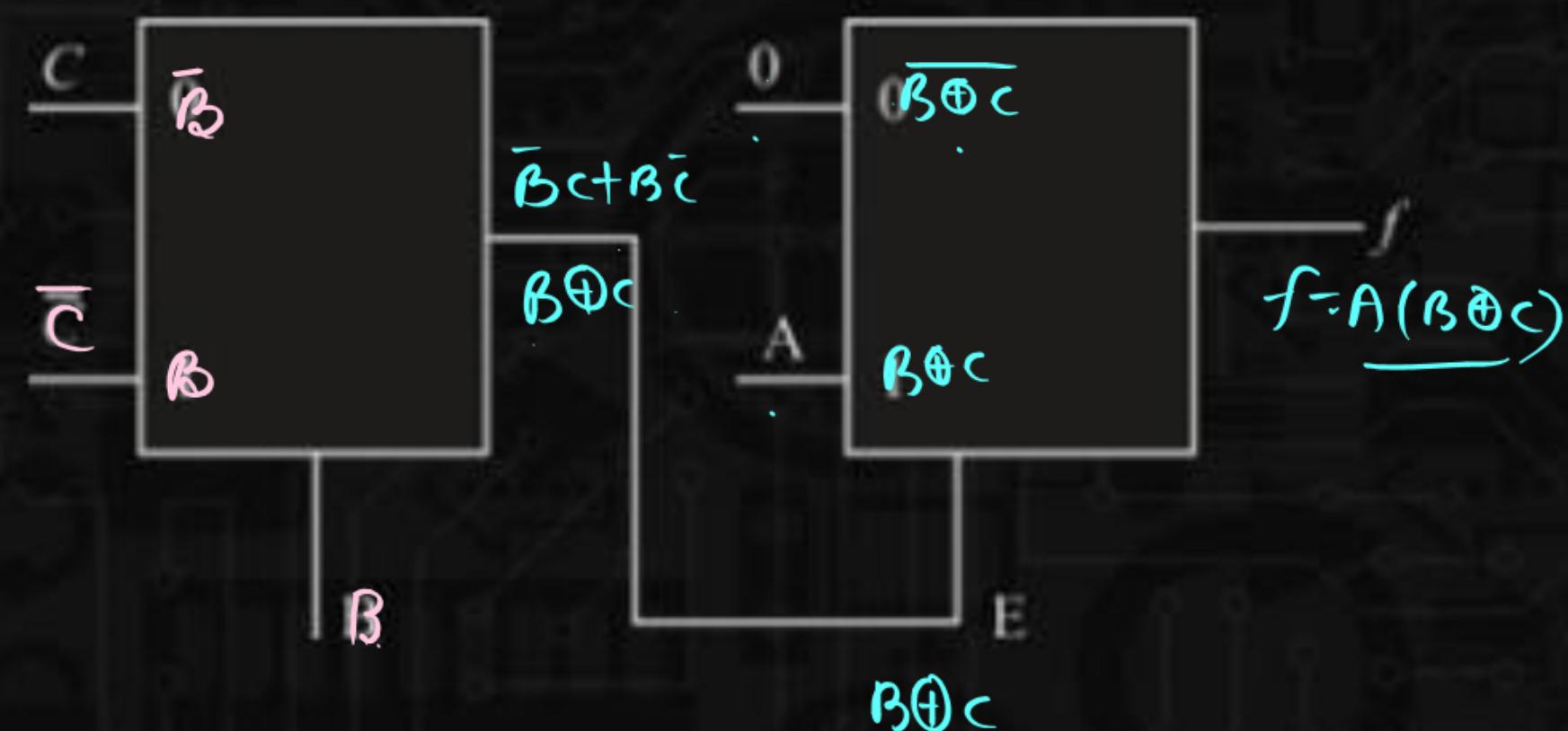
$$\begin{array}{ccc} 2 \times 1 \text{ MUX} & \xrightarrow{\frac{4}{2} + \frac{2}{2}} & 4 \times 1 \text{ MUX} \\ \downarrow & 2+1 = \textcircled{3} & \end{array}$$

Q.3

The Boolean function  $f$  implemented in the figure using two input multiplexers is

- A.  $\overline{A}\overline{B}C + A\overline{B}\overline{C}$
- B.  $ABC + A\overline{B}\overline{C}$
- C.  $\overline{A}BC + \overline{A}\overline{B}\overline{C}$
- D.  $\overline{ABC} + \overline{A}\overline{B}\overline{C}$

$$A[\overline{B}C + B\overline{C}] = A\overline{B}C + AB\overline{C}$$



**Q.4**

A designer has multiplexer units of size  $2 \times 1$  and multiplexer of size  $16 \times 1$  is to be realized. The number of units of  $2 \times 1$  MUXs required, will be

- A. 30
- B. 7
- C. 15
- D. 11

$$\begin{array}{ccc} & & \\ \text{2x1 MUX} & \xrightarrow{\frac{16}{2} + \frac{8}{2} + \frac{4}{2} + \frac{2}{2}} & 16 \times 1 \text{ MUX} \\ = & & \\ & 8 + 4 + 2 + 1 = 15 & \end{array}$$

Q.5

The logic function implemented by  $4 \times 1$  MUX, is

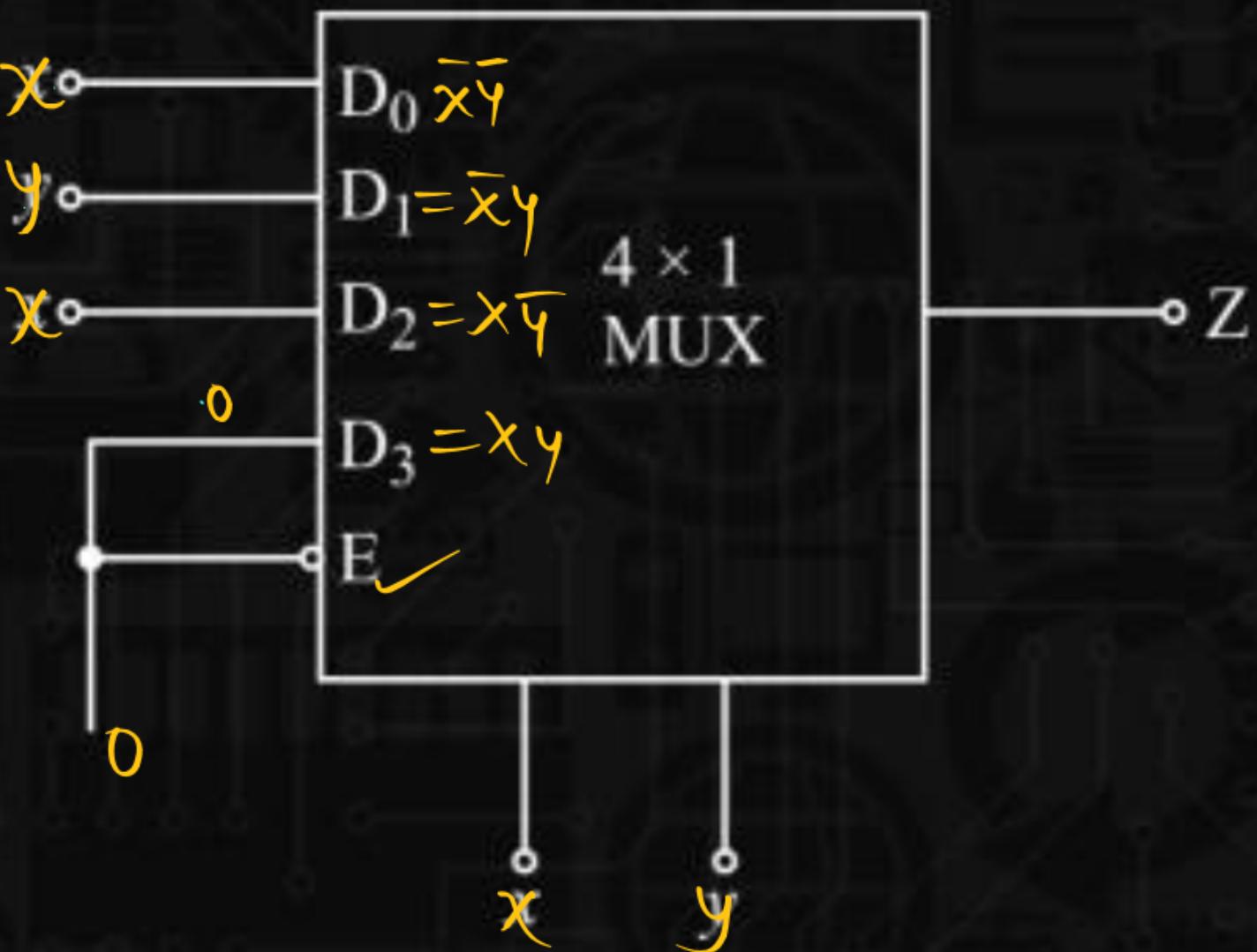
- A.  $Z = xy$
- B.  $Z = x + y$
- C.  $Z = \overline{x + y}$
- D.  $x \oplus y$

$$Z = x\bar{x}\bar{y} + y\bar{x}y + x\bar{x}\bar{y}$$

$$Z = 0 + \bar{x}y + x\bar{y}$$

$$Z = \bar{x}y + x\bar{y}$$

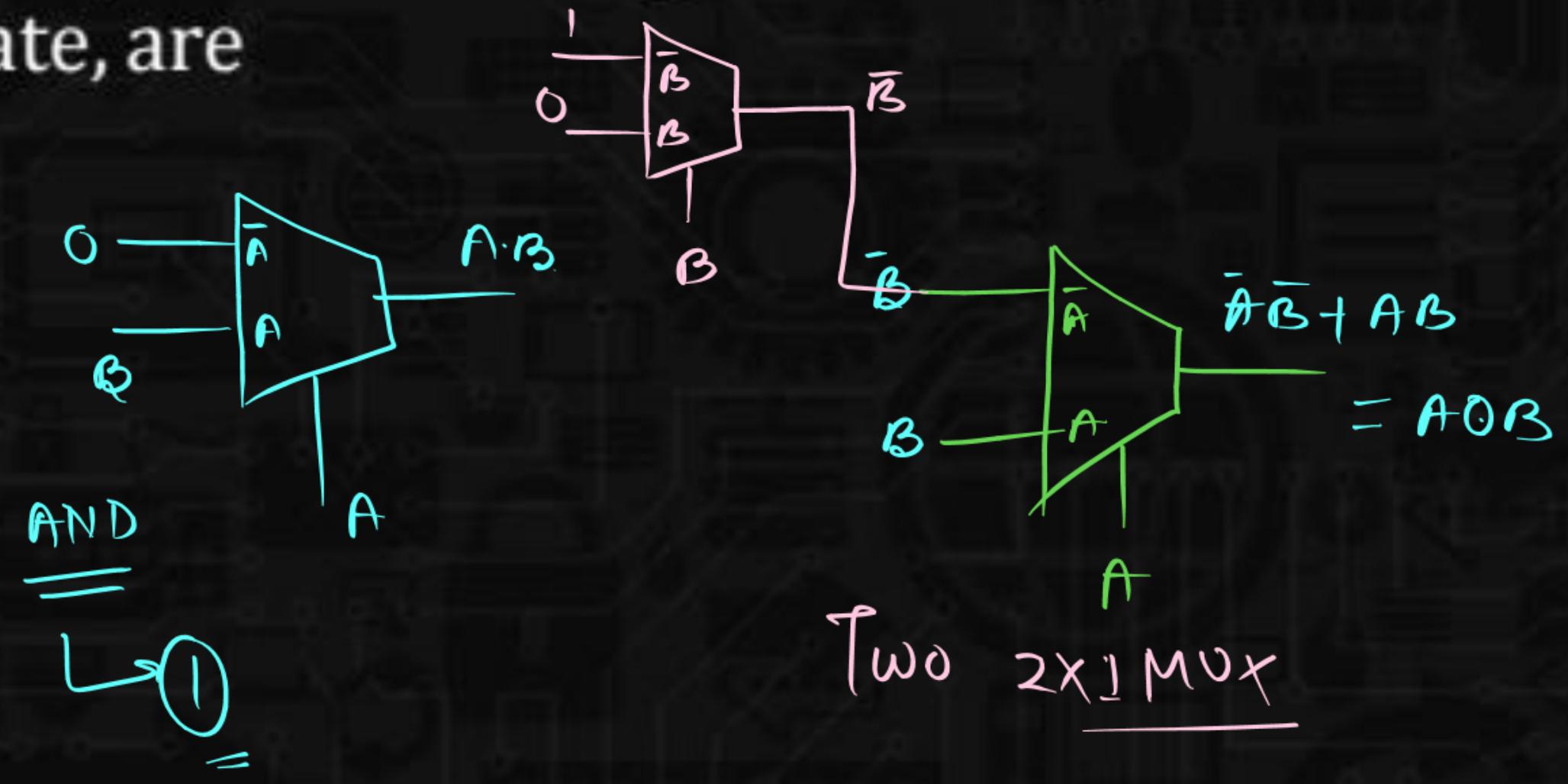
$$Z = x \oplus y$$



**Q.6**

The minimum number of multiplexers of size  $2 \times 1$  required to implement a 2-input XNOR gate and 2-input AND gate, are

- A. 1 and 1
- B. 2 and 1
- C. 2 and 2
- D. 3 and 1



# Answer Key

1. (b)
2. (c)
3. (a)
4. (c)
5. (d)
6. (b)

