TEAM: SiliconB
MEMBERS: ARPIT BAL (IIT BOMBAY)
KOWSHIK (IIT BOMBAY)
TRACK: Digital Design Track
MENTORS: Tim Edwards, James Stine, Amro Tork

CHIPATHON 2025

3-INPUT AND 4-INPUT NAND GATES (1X) FOR GF180MCU_OSU_SC_GP9T3V3

DELIVERABLES

Library	**GF180MCU_OSU_SC_GP9T3V3**
Cells	**1. Gf180mcu_osu_sc_mcu9t3v3__nand3_1 (3 INPUT NAND GATE)** **2. Gf180mcu_osu_sc_mcu9t3v3__nand4_1 (4 INPUT NAND GATE)**
Drive Strength	**1X**
Track	**9 Track**
VDD	**3.3 V**

NAND3_1 TARGETED SPECIFICATIONS

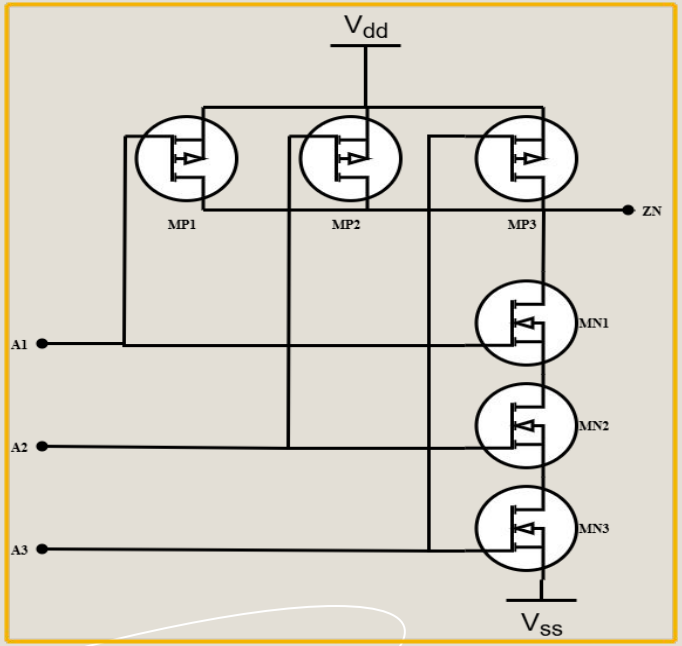


Fig.1 3-INPUT NAND GATE

Parameter	Targeted Spec.	Output Load
Input Capacitance	<0.01 pF	0.001 pF
Leakage Power	<0.15 nW	0.001 pF
Area	<25 μm^2	-
Delay	<0.2 ns	0.001 pF

NAND4_1 TARGETED SPECIFICATIONS

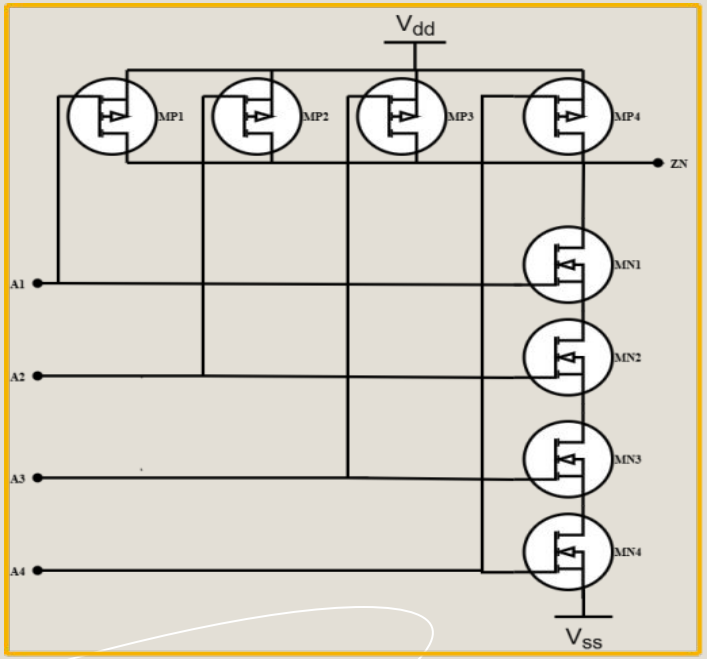
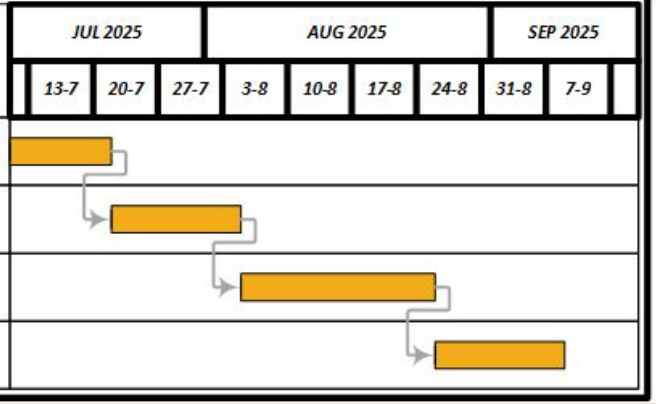


Fig.2 4-INPUT NAND GATE

Parameter	Targeted Spec.	Output Load
Input Capacitance	<0.01 pF	0.001 pF
Leakage Power	<0.2 nW	0.001 pF
Area	<30 μm^2	-
Delay	<0.2 ns	0.001 pF

TASK TIMELINE

ID	TASK NAME	START	FINISH	DURATION
1	DESIGN AND SCHEMATIC LEVEL SIMS	11-07-2025	21-07-2025	7D
2	LAYOUT+DRC+LVS	22-07-2025	04-08-2025	10D
3	CHARACTERIZATION	05-08-2025	25-08-2025	15D
4	INTEGRATION OF CELLS INTO LIBRARY	26-08-2025	08-09-2025	10D



WORK DIVISION

MEMBER NAME	ARPIT BAL	KOWSHIK
BLOCK ALLOTED	4-INPUT NAND_1x	3-INPUT NAND_1X
DETAILED DESCRIPTION OF TASK ALLOTED	Schematic+Layout+DRC+LVS+ Characterization of 4-INPUT NAND_1X	Schematic+Layout+DRC+LVS+ Characterization of 3-INPUT NAND_1X

REFERENCES

[1] https://gf180mcu-pdk.readthedocs.io/