Table 1

32 bit adders	adder structure	adder	ps for 99 add test	time for init ps	average time/add ps	throughput GHz	function gates	completeness gates	total gates	throughput per gate	function transitions	completeness transitions	total transitions	throughput per transition	oscillation period	
full word pipelined with full complete tetbench	zeroD_adder32	adder A	124780	3500	1225.05	0.82	128	44	172	4.75	64	44	108	7.56		
	zeroD_adder32	adder B	131500	3500	1292.93	0.77	256	44	300	2.58	112	44	156	4.96		
digit pipelined digit complete testbench	oneD_adder32	adder A	58000	3500	550.51	1.82	128	95	223	8.15	64	95	159	11.42		
	oneD_adder32	adder B	66350	3500	634.85	1.58	256	95	351	4.49	112	95	207	7.61		
Two D pipelined digit complete testbench	twoD_adder32	adder A	51090	3500	480.71	2.08	128	155	283	7.35	64	192	256	8.13		
	twoD_adder32	adder B	57260	3500	543.03	1.84	256	155	411	4.48	112	192	304	6.06		
digit pipelined with input full complete testbench	zeroDoneD_adder32	adder A	80341	2500	783.44	1.28	128	95	223	5.72	64	95	159	8.03		
	zeroDoneD_adder32	adder B	80061	2500	783.44	1.28	256	95	351	3.64	112	95	207	6.17		