(Following Roll No. to be filled by candidate)

Roll No. 1 4 0 0 3 1 0 0 5 0

B.Tech.
THIRD SEMESTER EXAMINATION 2015-16
ECS301
DIGITAL LOGIC DESIGN

Time: 3 hours **Max Mark: 100**

Note

- Attempt all questions.
- Marks and number of question to attempt from the section is mentioned before each section.
- Assume missing data suitably .Illustrate the answer with suitable sketch.

1. Attempt **any four parts** of the following [4x5]

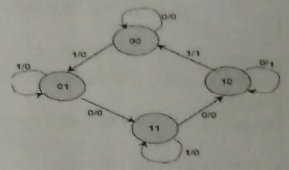
a. I) Subtract $(9)_{10}$ - $(4)_{10}$ using 1's compliment.
II) Perform $(9)_{10}$ - $(5)_{10}$ using 2's compliment.
b. I) Convert $(2AC5)_H$ to decimal, octal, binary.
II) Perform $(3)_{10}$ - $(8)_{10}$ in BCD using 10's compliment.
c. What is the hamming code and how to correct error at receiving side?
d. Generate the CRC code for data word 110010101 and divisor is 10101.
e. Convert the expression Y= AB+AC' +BC into standard SOP form and result is covert to POS form.
f. Minimize the following Boolean expression using K-map and realize it using basic gates $Y=\sum m(1,3,5,9,11,13)$

2. Attempt **any four parts** of the following [4x5]

a. Give circuit diagram of full adder using NAND gate and explain. Give truth table.
b. Implementation of the following logic function using 4:1 multiplexer
$f(A,B,C)=\prod M(0,1,3,5,7)$
c. What is magnitude Comparator explain it.
d. Simplify the following Boolean expressions using K map and verify the using quine Mccluskey method.
e. Implementation the following Boolean function using 3:8 decode and external gates
$f(A,B,C)=\sum m(2,4,5,7)$

f. Design a BCD to excess 3 code converter using minimum number of NAND date.

3. Attempt **any two parts** of the following [2x10]
a. Explain JK flip-flop. What is the problem of toggling in JK flip flop and how its remove it.
b. Design clocked sequential circuit using T flip-flop for following state diagram



c. Explain following
i) Melay machine
ii) Moore machine
iii) Ripple counter
iv) Shift register

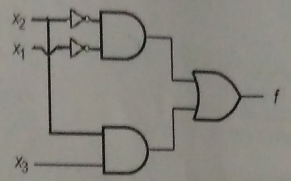
4. Attempt **any two parts** of the following [2x10]
a. i) Differentiate between PAL & PLA.
ii) Differentiate between RAM and ROM.
b. Design 3 bit gray to binary converter implement using suitable PROM. Draw the prom table & logic design.
c. State the advantage of asynchronous state machine. Find the critical and non critical races for following transition table

	00	01	11	10
00	01	00	00	10
01	11	00	01	10
11	10	00	00	11
10	10	00	01	10

5. Attempt **any two parts** of the following [2x10]

a. Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 1, input X is transferred to Z. When Y is 0, the output does not change for any change in X. Use SR latch for implementation of the circuit.

b. Explain hazard with its types. Modify the circuit given the figure to make hazard free.



c. Explain minimization of state reduce the state given below using any state minimization technique

Present state	Next state	
	X=0	X=1
a	d,0	b,0
b	e,0	a,0
c	g,0	f,1
d	a,1	d,0
e	a,1	d,0
f	c,0	b,0
g	a,1	e,0